SIGNAL TO POWER COUPLING AND NOISE INDUCED JITTER IN DIFFERENTIAL SIGNALING

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SIGNAL TO POWER COUPLING AND NOISE INDUCED JITTER IN DIFFERENTIAL SIGNALING

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SUMMARY

Differential interconnects are extensively used in high-speed digital circuits at fast data rates and in environments of high noise like backplanes. For such applications they are preferred over single-ended lines owing to their ability to reject common-mode noise. Differential schemes like Low Voltage Differential Signaling (LVDS) are used for wireless base stations and ATM switches in telecommunication applications, flat panel displays and servers and for system-level clock distribution.

LVDS applications use data rates from 100 Mbps to about 1.5 Gbps and are expected to be highly immune to noise. However, noise will also be injected into differential signals at these high data rates, if there are irregularities in the interconnect setup.

These anomalies may be via transitions from differential lines through power planes in power distribution systems, via stubs, asymmetric lengths of differential lines, different transition points for each of the differential vias etc. The differential setup is expected to be immune to such imbalances; however, investigation of these discontinuities indicate that sufficient signal energy can be leaked to power distribution networks (PDN) of packages and boards.

The effect of this energy loss was examined in time-domain and was found to cause signal integrity effects like jitter. Irregular differential structures were compared with the equivalent single-ended configuration and symmetrical perfect differential lines.

This thesis work quantifies signal to power coupling caused by irregular differential structures in the presence of PDN planes in frequency domain. Presence of noise in differential signaling is verified through a set of test vehicles. The jitter induced as a result of signal to power coupling from differential lines was also investigated.

CHAPTER 1

INTRODUCTION

1.1 IC Packaging

The design of packages for Integrated Circuits (IC) has been made more complex by the rising frequency of operation of digital circuits. Noise effects like EMI, crosstalk and impedance mismatches which were considered secondary at lower data rates can not be underestimated any longer. The copper traces connecting various parts of the electronic system can no longer be approximated as lumped elements or short circuited wires. Instead at higher frequencies, interconnections must be modeled as transmission lines accounting for the minimum time of flight and the attenuation of high frequency components of the transmitted signal. Thus integrity of signal transmission becomes critical at high frequencies in IC packaging.

According to the International Roadmap for Semiconductors (ITRS), the trend of increasing frequency of operation in semiconductor devices will continue, albeit at a slower rate, as shown in Figure 1 [7]. Moreover, ITRS also indicates that miniaturization of electrical packages will accompany increasing performance speeds. Figure 2 shows a mini Peripheral Card Interface(PCI) serial ATA card that is an example of this trend; it is quarter the size of other PCI cards [8] and is designed for small portable devices like laptops.

Thus layout designers face constraint for space, forcing them to introduce discontinuities and irregularities while routing signal traces. Also, with the advent of technologies like System-In-Package (SIP), dissimilar modules have become more vertically integrated [9]. Consequently, to provide the required signal and power connections to the ICs, vertical transitions like through-hole vias are needed between metal layers.

Therefore imperfections like vertical transitions, bends, crowded signal lines etc. introduced in interconnect design create impedance mismatch causing signal reflections and distortion. However, due to the industry emphasis on high performance speeds, such trace

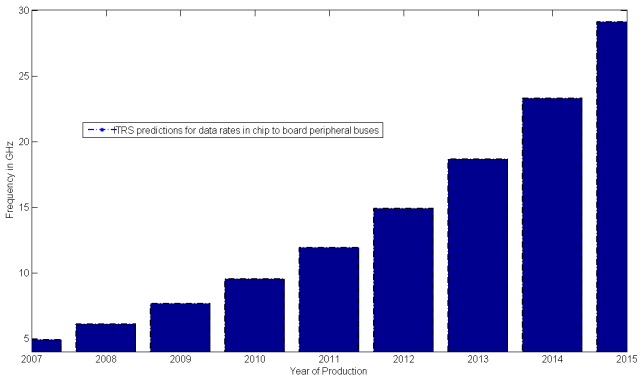

Figure 1. Increase of operating frequency with year of production

Figure 2. Advantech Mini PCI serial ATA card

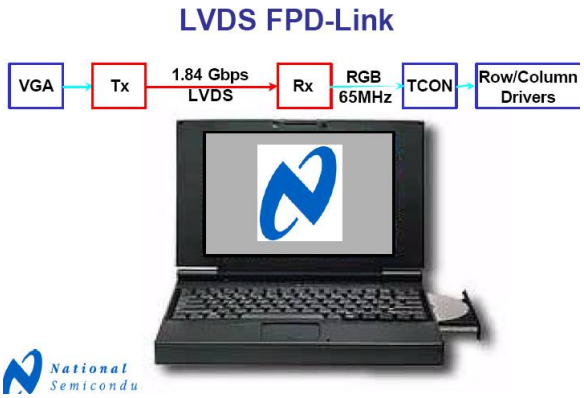

Figure 3. Application of differential signaling - LVDS in Flat Panel Display - courtesy National Semiconductors [1]

imperfections must be minimized to avoid excessive noise effects.Thus to combat noise effects in single-ended traces, differential signaling using coupled transmission lines was introduced.

A very common differential signaling scheme is Low Voltage Differential Signaling (LVDS)which is used in computer buses like Firewire, PCI Express and Hyperport. Figure 3 shows one application of LVDS in Flat Panel Displays (FPD) used in notebooks [1] at data rates of 1.84 Gbps. Differential signaling has become commonplace in end-user applications such high resolution displays in luxury cars which use 1.5 GBit/s LVDS Serializer/Deserializer (SerDes) video links [2]. Figure 4 shows a national semiconductor SerDes chip that converts LVTTL/LVCMOS to a single differential pair.

This chapter provides a high-level introduction to differential signaling, the concept of differential impedance, mixed-mode parameters and describes the method to perform differential 4-port measurements. Secondly, the concept of coupling signal energy to power distribution networks is explained and its importance in differential signaling is highlighted. The last part of this introductory chapter describes jitter, its relationship with power supply noise and its common causes. All these subsections provide a good background to the effects investigated in this thesis work and the results published.

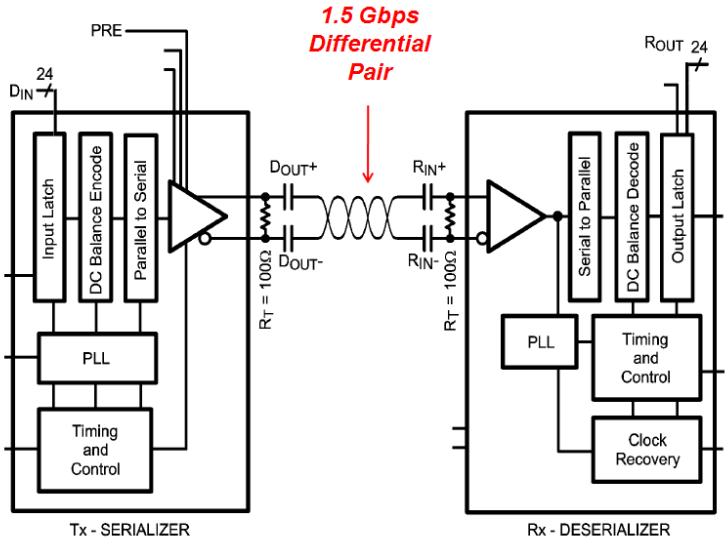

Figure 4. Application of differential signaling - SerDes video link chip [2]

1.2 Differential Signaling

In IC chips and packages, transmission lines are commonly used for connecting the output of on-chip drivers to other transistor circuits. A transmission line refers to a pair of conductors in which one is used for transmission of the signal and the other provides the return path for the loop current as shown in Figure 5 [10].

Voltage of the signal conductor in a transmission line is always measured with reference to the ground conductor. This type of voltage signaling is often referred to as single-ended signaling scheme. Single transmission lines are found to be very susceptible to noise at mid to high frequencies due to non-idealities in their current return path [11] [12].

Planes are employed for power delivery in IC packages and boards since usage of interconnects increases parasitic inductances in the current loop. They alternatively function as the return path for currents in signal traces. Thus slots in the planes or change in the reference ground plane during via transition can create non-ideal return current paths as shown in Figures 6 and 7. For that reason there is need to find better signaling schemes for critical signal nets that reduce the dependence of the signal traces on the reference conductors.

Differential lines consist of a pair of closely coupled transmission lines that are excited

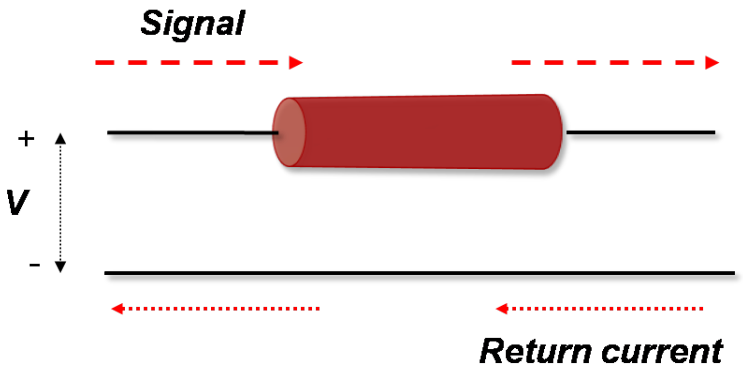

Figure 5. Transmission line with single-ended signaling

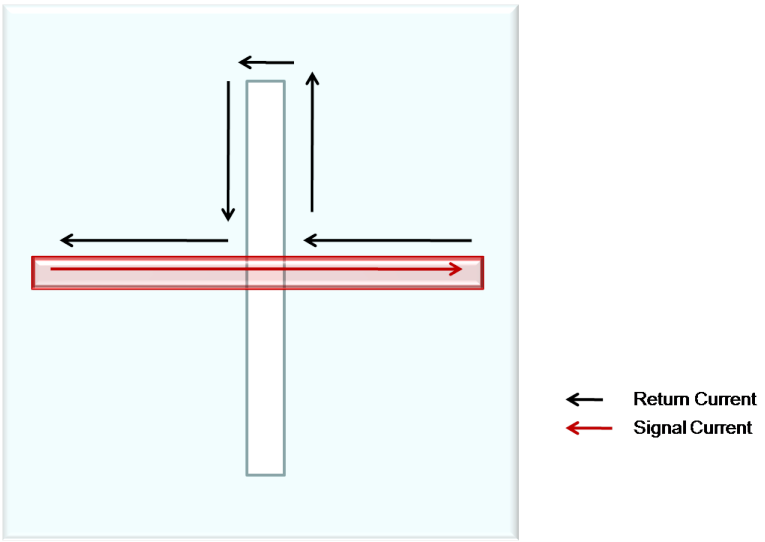

Figure 6. Single transmission line over slot in reference plane

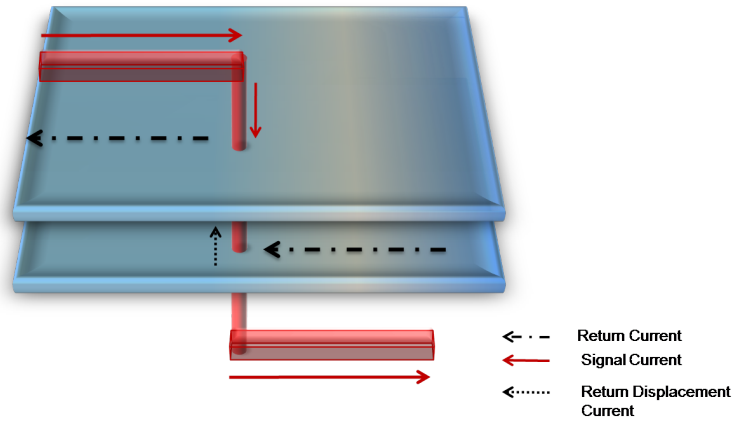

Figure 7. Single transmission line with reference plane change - return path discontinuity

using differential signaling. This signaling utilizes two voltage sources, one for each transmission line, such that the first source (V1) transmits complementary bits when compared to the second one (V2) as shown in Figure 8. In this manner differential lines transmit balanced signals where the voltage difference between traces communicates bit information [13]. Thus the differential voltage V_{diff} can be computed as given in Equation 1.

$$V_{diff} = V1 - V2 \tag{1}$$

where,

$V2 = -V1$

The main advantage of using differential signaling is its ability to reject any noise common to the individual traces [14]. This is made possible by referencing voltage on one line to the other such that any common noise infiltration will be canceled and hence not detected by the receiver.

However, a major disadvantage of using differential signaling is the creation of common-mode noise in differential lines due to the presence of imperfections and discontinuities. Common-mode noise refers to fluctuations of the common-mode voltage which results in signal integrity effects like jitter in interconnects.

Discontinuities like via transitions cause power noise and signal energy loss in differential signaling which is otherwise absent in ideal coupled lines. Experiments and simulations performed proves the above premise in this thesis. The rest of this introductory section provides background information on differential signaling and prior work performed in this area:

1. Differential versus odd mode impedance
2. Introduction of common-mode noise
3. Mixed-mode parameters

4. Measurement of differential mixed-mode S-parameters

5. Prior work on differential signaling

1.2.1 Differential impedance versus odd mode impedance

When a pair of transmission lines are in close proximity then the electric and magnetic fields from one line couple to the neighboring line. Then the method of individual trace excitation decides the type of coupling between the conductor pair and consequently, the type of propagation through the lines. Therefore, there are two types of propagation modes for a coupled pair of transmission lines - even mode and odd mode propagation.

Odd mode propagation occurs when the signal traces are provided with complementary voltage excitation or differential excitation as shown previously in Figure 8. Then the corresponding electric and magnetic fields are shown in Figure 9.

The characteristic impedance of a transmission line, Z_0, is the ratio of the instantaneous voltage and current in the line at any given instant. Thus for a pair of differentially excited transmission lines that are sufficiently far apart such that coupling between them is minimal, the characteristic impedance of each trace is the same as Z_0 of a single transmission line as shown in Figure 10 [13]. In Figure 10 I1 disappears into the paper while I2 emerges from the paper; that is, $I1 = -I2$. Therefore odd mode impedance for each trace is equal to Z_0 as shown in Equation 2.

$$Z_{odd} = Z_0 = \frac{V1}{I1} \tag{2}$$

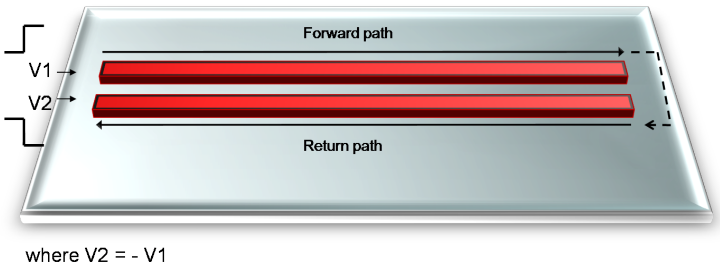

Figure 8. Differential excitation of coupled lines

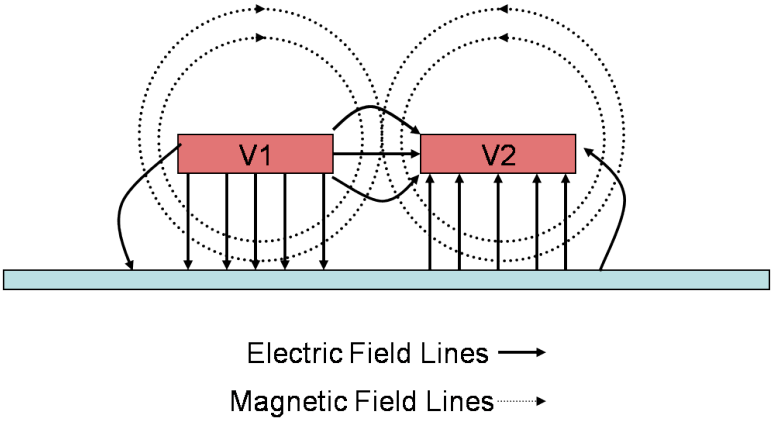

Figure 9. Electrical and magnetic fields for a coupled line pair with odd mode excitation

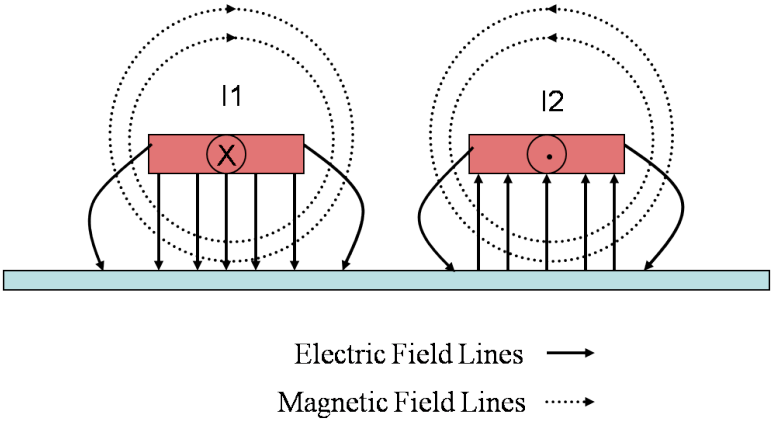

Figure 10. Electrical and magnetic fields for a pair of uncoupled microstrip lines with odd mode excitation

Differential impedance for a coupled transmission line pair is the impedance observed by a differential current, I_{diff} from an odd mode excitation as shown in Figure 8. Here I_{diff} appears as a loop current that just travels between the pair of lines and V_{diff} is the voltage of one line measured with respect to the other as shown in Equation 1 [13].The relation between the differential impedance between the pair of traces,Z_{diff} and Z_{odd} is given in Equation 3.

$$Z_{diff} = \frac{V_{diff}}{I_{diff}} = \frac{V1 - V2}{I1} = \frac{2 * V1}{I1} = 2 * Z_{odd} \tag{3}$$

where,

$V2 = -V1$

However when the lines move closer to each other the odd mode impedance reduces; that is, $Z_{odd} < Z0$ for each transmission line. This phenomenon is caused by the fringe coupling of the electromagnetic (EM) fields between the lines. Differential lines can reject common-mode noise only when they are tightly coupled and $Z_{odd} < Z0$. This is because when $Z_{odd} = Z0$ and the lines are uncoupled, then the return current for each trace flows undisturbed, underneath it. Therefore these traces are susceptible to noise introduction by non-idealities in the reference plane. However when $Z_{odd} < Z0$, the return currents for the lines overlap and any noise injected due to non-idealities cancels out.

In electronic systems differential lines are usually designed for a differential impedance of 100 Ω. The method to design differential lines is to calculate Z_{diff} from the corresponding Z_{odd}. Z_{odd} can be calculated using commercial transmission line impedance calculators or from the analytical equations. A coupled microstrip line can be described by the equation given in Equation 4 [15]. The capacitances in the formula are indicated in Figure 11. Equivalent equations also exist for other transmission line configurations [16].

$$Z_{odd} = \frac{c}{\sqrt{C_o C_o^a}} \tag{4}$$

where,

c - Speed of light

C_o - odd mode capacitance = $C_p + C_f + C_{ga} + C_{gd}$

$C_p = \frac{\epsilon \epsilon_r W}{h}$

C_f, C_{ga} and C_{gd} - Various fringe capacitances

C_o^a - signifies capacitance with air as dielectric

1.2.2 Common-mode noise in differential signaling

A differential signal can be defined in terms of individual excitation voltages V1 and V2 for a pair of coupled lines as shown in Equation 1. Similarly, a common-mode signal can

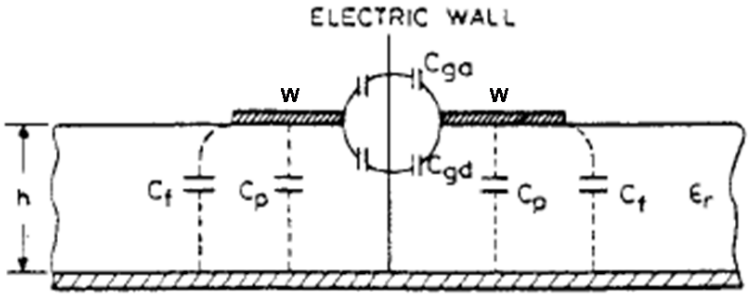

Figure 11. Electrical and Magnetic fields for a coupled line pair with odd mode excitation

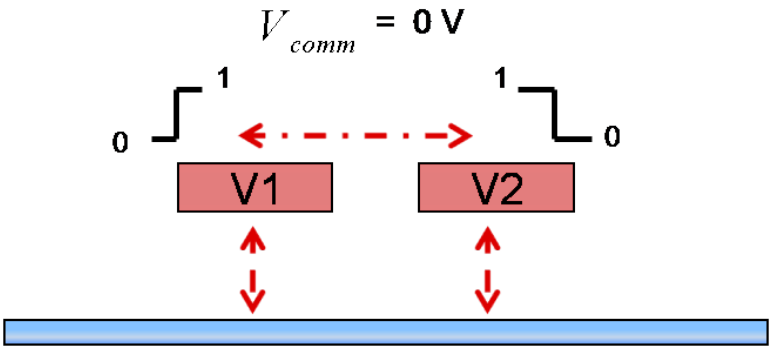

Figure 12. Measuring common-mode voltage in a differential pair

also be defined using the two single-ended voltages V1 and V2 as shown in Equation 5. Often common-mode signals are confused with single-ended signals; V_{comm} is indicative of the DC bias between the complementary inputs that form the differential signal V_{diff}.

For example, if V1 switches from low to high while V2 switches from high to low, then V_{comm} indicates the DC level between the individual traces as illustrated in Figure 12. Single-ended voltages on the other hand are the actual input signals V1 and V2 measured with reference to the ground reference plane, also shown in Figure 12.

When V1 and V2 are balanced then V_{comm} is a constant DC value. However when there are slight perturbations in the circuit like discontinuities in the traces,impedance mismatch or crosstalk then a part of the differential signal is converted to common-mode noise [13]. Therefore fluctuations of the common-mode voltage is defined as common-mode noise and V_{comm} acts like a noise indicator in differential signaling.

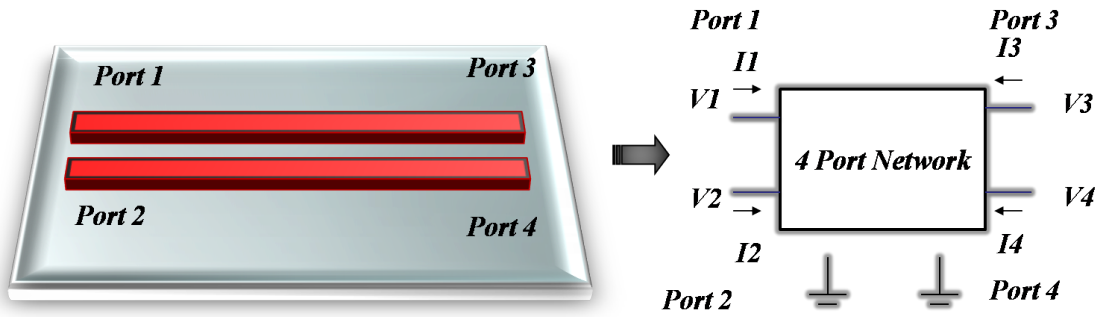

Figure 13. 4-port Parameters for differential transmission lines

$$V_{comm} = \frac{V1 + V2}{2} \tag{5}$$

1.2.3 Mixed-mode parameters

Given an N port network , an admittance matrix or impedance matrix completely describes the behavior of the network at those N ports by relating incident and reflected voltages and currents. Similarly a scattering matrix can be defined for an N port network which relates the voltages incident on each of those ports to the reflected voltages [10].One way to characterize differential pair of lines is to measure their S-Parameters at the two input points of voltage excitation and the two output points of termination. This gives rise to a 4-port network as shown in Figure 13. The 4-port S-Parameter matrix for this network can be given as [17]:

$$\begin{pmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{pmatrix} \tag{6}$$

where,

a = stimulus

b = response

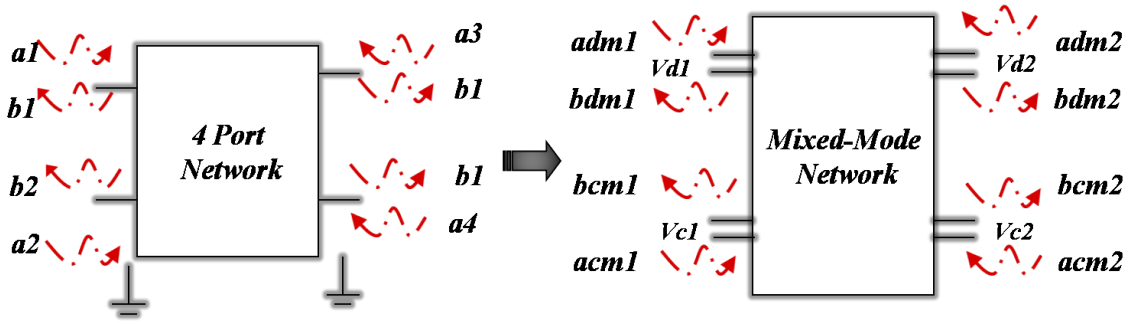

Figure 14. Mixed-mode parameters from 4-port parameters

$S_{ij} = \frac{b_i}{a_j}$ is the scattering parameter given stimulus a_j and response b_i

This 4×4 array of single-ended S-parameters can be converted to mixed-mode S-Parameters which are more intuitive as far as differential signaling is concerned. The 4-port network calculates voltages at each of the four ports V_i with respect a some common ground point. In contrast, the equivalent mixed-mode parameters define differential voltages V_{D_i} and common-mode voltages V_{C_i} across each pair of rails as shown in Figure 14.

Thus a 4×4 array of single-ended S parameters can be thought of as a matrix of four 2×2 matrices each also called quadrants - pure differential, mixed-mode and pure common as shown in equations below [17]:

$$\begin{pmatrix} b_{dm1} \\ b_{dm2} \\ b_{cm1} \\ b_{cm2} \end{pmatrix} = \begin{pmatrix} S_{DD11} & S_{DD12} & S_{DC13} & S_{DC14} \\ S_{DD21} & S_{DD22} & S_{DC23} & S_{DC24} \\ S_{CD31} & S_{CD32} & S_{CC33} & S_{CC34} \\ S_{CD41} & S_{CD42} & S_{CC43} & S_{CC44} \end{pmatrix} \begin{pmatrix} a_{dm1} \\ a_{dm2} \\ a_{cm1} \\ a_{cm2} \end{pmatrix} \tag{7}$$

Therefore,

$$\begin{pmatrix} b_{dm1} \\ b_{dm2} \\ b_{cm1} \\ b_{cm2} \end{pmatrix} = \begin{pmatrix} S_{DD} & S_{DC} \\ S_{CD} & S_{CC} \end{pmatrix} \begin{pmatrix} a_{dm1} \\ a_{dm2} \\ a_{cm1} \\ a_{cm2} \end{pmatrix} \tag{8}$$

where S_{DD}, S_{DC}, S_{CD} and S_{CC} are the pure differential, mixed-mode and pure common-mode

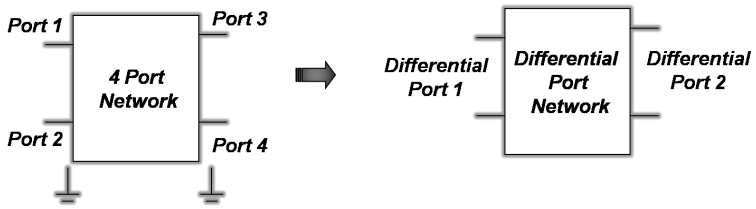

Figure 15. Conversion of four-port network to differential port network

quadrants.

For differential signaling, the mixed-mode parameters are highly insightful - usually the 4-port network is differentially excited and its differential response is measured between two output ports as shown in Figure 15. Therefore mixed-mode parameters, S_{DDij}, can be used to identify reflection and transmission at the differential ports. Only the 1st quadrant in Equation 7 is required to define differential S-parameter S_{DDij} and they are related to the single-ended 4-port parameters using the equations 9 and 10.

$$S_{DD11} = 0.5 * (S_{11} - S_{12} - S_{21} + S_{22}) \tag{9}$$

$$S_{DD12} = 0.5 * (S_{13} - S_{14} - S_{23} + S_{24}) \tag{10}$$

Differential to single-ended S-parameters S_{DSij} are related to the 3-port network in the manner shown in Figure 16. Differential to single-ended S-parameters are useful in determining the response between power supply planes when coupled lines are differentially excited; that is, they measure signal to power coupling in differential structures.

As illustrated in Figure 16, in order to convert a 3 port network to an equivalent mixed-mode network, single-ended S parameters of ports 1 and 2 need to be converted to differential parameters. Equations 11 to 15 can be utilized for this purpose. S-parameters for single-ended ports cab be defined using Equation 11 where a measures the stimulus and b measures the response of the port; equations for a and b are shown in Equations 14 and 15. Similarly, for a differential port, a and b are as given in Equations 14 and 15.

$$S = \frac{b}{a} \tag{11}$$

$$a = \frac{1}{2 * \sqrt{Re(Z)}}[V + ln(Z)] \tag{12}$$

$$b = \frac{1}{2 * \sqrt{Re(Z)}}[V - ln(Z)] \tag{13}$$

where

V = Voltage at single-ended port

I = Current at single-ended port

Z = Impedance at single-ended port = $\frac{V}{I}$

However, for a differential port:

$$a = \frac{1}{2 * \sqrt{Re(Zd)}}[Vd + ln(Zd)] \tag{14}$$

$$b = \frac{1}{2 * \sqrt{Re(Zd)}}[Vd - ln(Zd)] \tag{15}$$

where

Vd = Voltage at differential port = V1-V2

Id = Current at differential port = 0.5(I1-I2)

Zd = Impedance at differential port = $\frac{Vd}{Id}$

Therefore S_{DS31} is related to the single-ended S-parameters as given in Equation 16 (this can be deduced using the Equations 11 to 15).

$$S_{DS31} = \frac{(S_{13} - S_{23})}{\sqrt{2}} \tag{16}$$

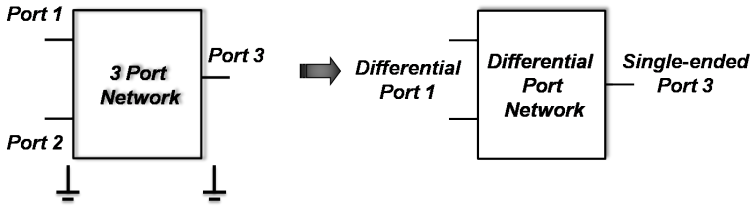

Figure 16. Conversion of three-port network to differential port network - differential to single-ended signaling

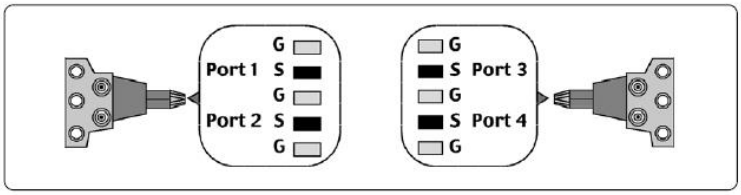

Figure 17. Location of ports in a 4-port measurement using ACP GSGSG 500 probes

1.2.4 Measurement of differential mixed-mode S-parameters

Differential mixed-mode parameters can be obtained for the Device-Under-Test (DUT) by measuring the equivalent 4-port single-ended parameters and converting them using linear algebra defined in section 1.2.3 [17]. This is the methodology used in this thesis for performing measurements on all the test vehicles with differential line structures.

All measurements were performed using a Air Coplanar Probe- ACP GSGSG 500 which has a probe pitch of 500 microns. For the 4-port measurement the ports were considered as shown in Figure 17 [18].

The calibration test chosen to remove the effect of the measurement equipment was the 4-port SOLT calibration. This microwave calibration technique utilizes four known structures to predict the parasitics in the measurement and correspondingly negate its effects. S-O-L-T stands for Short-Open-Load-Thru signifying the four tests required to calibrate

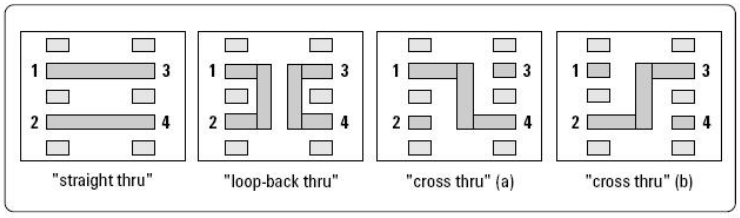

Figure 18. Types of thru calibration available for 4-port measurement using ACP GSGSG 500 probes

the DUT. The S-O-L standards for the GSGSG probes were performed for each of the 4-ports.

There are separate thru standards used for differential GSGSG probing - the three distinct types are straight-thru, loop-back thru and cross thru shown in Figure 18. All of them can be used in calibration but the optimum method of calibrating utilizes only straight-thru between Port 1 and Port 3, loop-back thru between Port 1 and Port 2 and cross-thru between Port 1 and Port 4. After performing the 4-port SOLT calibration, the single ended S-Parameters were measured using Agilent Vector Network Analyzer(VNA) for all the test vehicles described in section 2.1.

1.2.5 Prior work on differential signaling

Prior work on differential signaling focused on perfectly symmetric differential lines where each line in the pair has the same dimensions and is perfectly identical [12]. However, noise due to high data rates has increased the importance of study of imbalances in differential signaling. Delay skew introduced by differential sources increases the electromagnetic radiation in differential signaling to high levels as if it were caused by a pure common mode input[19].

It was found that the presence of differential vias causes an additional delay that may

be critical in some timing circuits and also degrades signal quality at high frequencies[20]. FDTD simulation was used to prove that differential lines couple considerably to reference planes that are in close proximity [21]. Therefore differential signaling is affected by non-idealities like via transitions, via stubs, slots in reference planes and asymmetric via spacing in packages.

Previous work on discontinuities in differential signaling have not examined the effect of these irregularities in the presence of a non-ideal Power Distribution Network (PDN). Though non-idealities in differential lines will cause immediate signal integrity effects like time delay, they will also result in signal energy loss. This energy gets coupled to power supply planes in packages and boards causing additional power noise.

In a differential pair the traces are ideally supposed to reference only between themselves; however,due to the high level of miniaturization in electronic packages, some fringe EM fields do couple to nearby conductors. Thus return currents on planes do not cancel even in differential signaling causing differential lines to be susceptible to noise fluctuations on power supply planes. Therefore, increased power noise due to signal to power coupling from differential signaling will in turn cause signal integrity degradation on the differential lines.

This thesis work proves by simulations and measurements the significant effect of discontinuities on the energy coupling from differential lines to planes in the PDN. Moreover, it has also been demonstrated by means of time domain simulations that jitter is introduced in differential lines owing to the noise coupling effects of these irregularities.

1.3 Signal to Power Coupling

A major part of this thesis work deals with the leaking of signal energy to the Power Distribution Network (PDN). In modern packages and boards the signal distribution network (SDN) is placed in close proximity to power supply components. Thus electromagnetic interference (EMI) can couple noise between these two seemingly separate parts of the

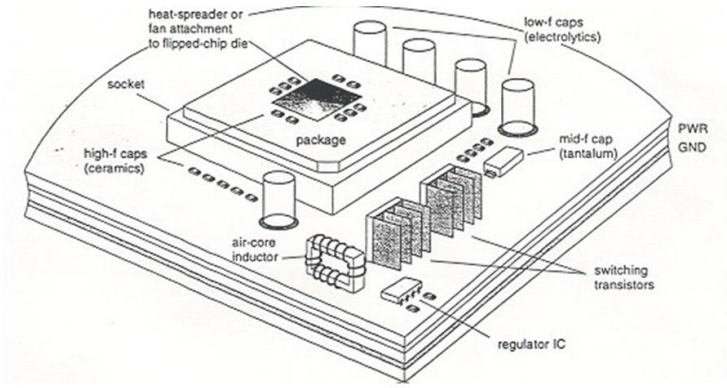

Figure 19. Power Distribution Network (PDN)

electronic system. This section explains the underlying principles at work in a PDN and how they interact with imperfections in differential interconnects.

1.3.1 Simultaneous Switching Noise (SSN)

An important issue in high frequency digital circuits is providing clean power to chips in packaged electronic systems. The PDN in a typical computer system consists of a power supply, Voltage-Regulator-Modules (VRM), decoupling capacitors and interconnections that connect a remote power supply to the power rails of the chip as shown in Figure 19 [22].

On the motherboard, high voltage provided by the power supply is down-converted using DC-DC converters. From here transmission lines provide connections to the IC package and chip. On-package and on-chip power is delivered by parallel planes. Decoupling capacitors act like charge reservoirs at low, mid and high frequencies depending on their proximity to the switching circuits.

When a CMOS transistor switches on-chip then an instantaneous transient current is demanded from the PDN. This switching current $\frac{dI}{dt}$ experiences significant parasitic resistance and inductance since it has to travel from the power supply on the motherboard to the power rails of the CMOS circuit as shown in Figure 20. Consequently, significant Simultaneous Switching Noise (SSN) is caused by the voltage drop across distributed parasitics

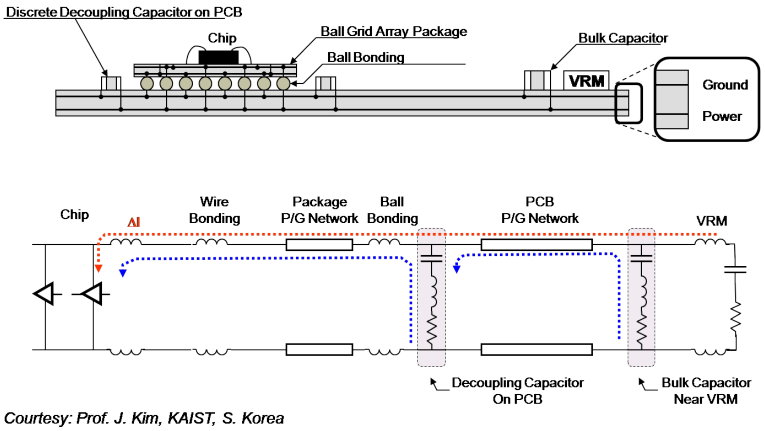

Figure 20. Typical parasitics in PDN

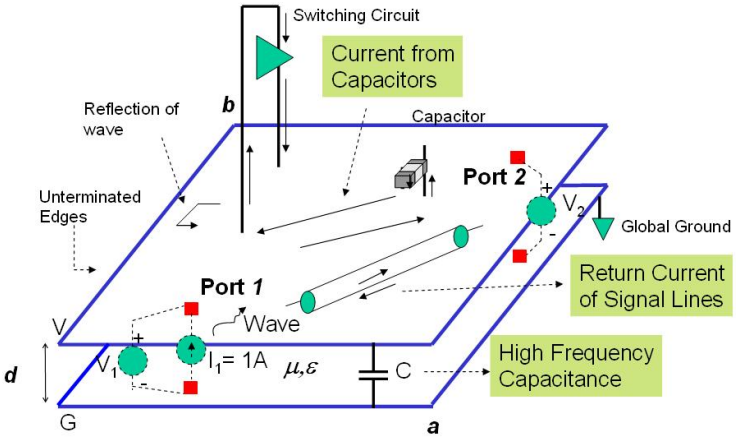

Figure 21. The roles of power supply planes

during on-chip switching as given by Equation 17 [3]. Therefore, it is critical to accurately predict the amount of SSN and its effects in packaged electronic systems.

$$V_L = L\frac{dI}{dt} \tag{17}$$

Power or ground planes are used instead of interconnects for power distribution in packages and chips because of their ability to provide high frequency decoupling. Thus the PDN of an IC package consists of alternating layers of metal sandwiched between thin dielectrics. Power supply planes also play critical roles other than providing power to circuits and this is illustrated in Figure 21 [3].

Presence of power supply planes in power distribution networks (PDN) aggravates the

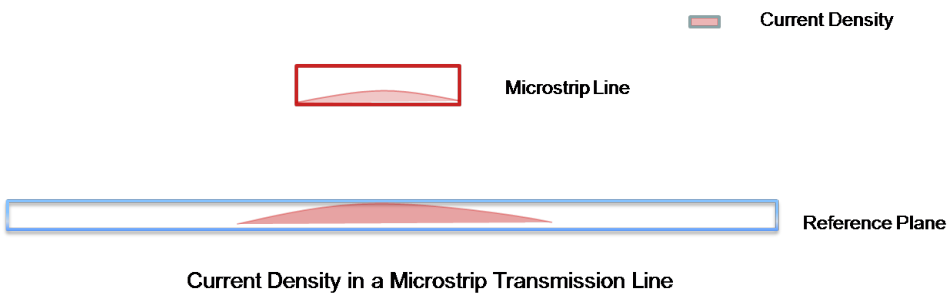

Figure 22. Current density in microstrip trace

problem of SSN since these planes act like cavity resonators at high frequencies [23] [24]. The frequency at which the planes resonate can be calculated for the size of planes a×b as given in Equation 18.

$$f_{mn} = \frac{1}{2\pi\sqrt{\mu\epsilon}}\sqrt{\frac{m\pi^2}{a} + \frac{n\pi^2}{b}} \tag{18}$$

One major role that planes play is to provide a path for the return current for signal interconnects as shown in Figure 21. This is because at high speeds return currents follow the path of least inductance and for a signal trace the smallest inductive loop between signal and return current lies directly beneath it [14]. This is indicated for a microstrip line in Figure 22.

In the presence of trace discontinuities like via transitions the return current has to then travel through the dielectric in-between plane pairs as shown in Figure 23. This displacement current aggravates power supply noise because it faces a high impedance path at resonant frequencies of plane pairs.

From another perspective, plane pairs can be considered as microwave cavities with a high quality factor Q. Q for a passive network measures loss. Therefore, any periodic current excitation causes noise on the planes that accumulates over time and remains within the cavity [3].

Therefore, discontinuities couple some of the signal energy to the power/ground planes creating cavity noise and increasing the overall power noise. Accurate modeling techniques

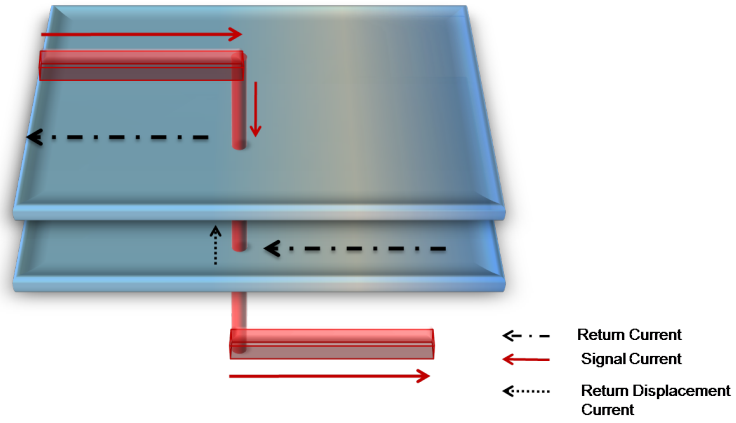

Figure 23. Return path discontinuity caused by non-idealities

to capture the effect of signal coupling to planes with good correlation to measurements have been developed previously [25].

1.3.2 Imperfections in differential signaling

Coupling of signal energy to the power/ground planes is lesser in differential signaling when compared to the single-ended scheme [12][11]. But the amount of energy coupled is still significantly more than that found in absence of discontinuities or irregularities. Therefore vertical signal transitions and reference plane changes cause an increase in signal to power coupling even if the differential lines are matched in length. This is due to coupling of EM fields from differential lines to reference planes. Therefore, the differential signal not only references the other line but also the planes [21] [11].

Thus due to presence of discontinuities in symmetric and matched differential lines signal energy couples to planes. However, this phenomenon is not restricted to via transitions. Presence of differential via stubs or asymmetric lengths of differential lines also contribute to the increase of signal to power coupling. Therefore imbalances in differential signaling increase signal to power coupling which in turn amplifies SSN. This thesis identifies the amount of signal energy coupled to power planes in various irregular differential structures by simulation and measurements as described in Chapter 2.

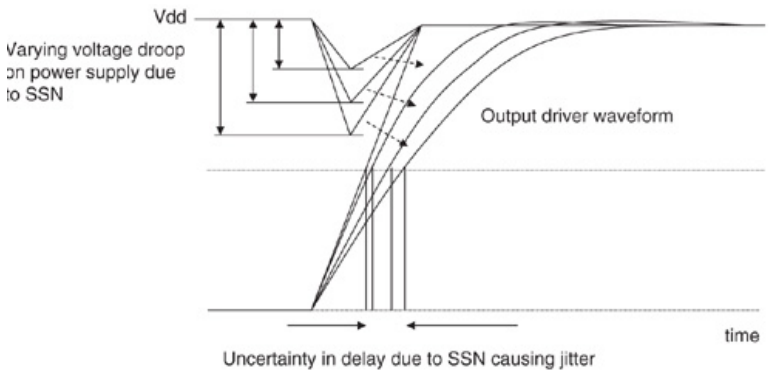

Figure 24. SSN and jitter [3]

1.4 Jitter

Signals are transmitted as a sequence of bits with logic levels 0 or 1 in a digital system. However in practice digital signals are never perfect trapezoids with finite rise and fall times; instead noise infiltrates a signal during its transmission. This noise can cause the logic level deviation in the signal which is commonly referred to as amplitude noise. However, when noise causes a timing deviation in a digital signal such that the rising and falling edges are altered then this noise effect is defined as timing jitter or jitter as shown in Figure 24.

1.4.1 SSN and Jitter

Figure 24 also shows how fluctuation in the power supply voltage or SSN can attribute to jitter on signal lines. Variation in power supply is caused by the myriad parasitic inductances and resistances in the PDN. Especially if I/O circuits are being driven by on-chip drivers powered by the PDN then the maximum voltage drop across the inductances in the PDN is given by Equation 19 [3].

$$\Delta v \approx \frac{NL \times V_{dd}}{Z_0 t_r} \tag{19}$$

where,

Δv - Voltage drop across all the parasitic inductance,L

N - Number of I/O connections

t_r - Rise time of the signal provided by the driver

Z_0 - Characteristic impedance of the I/O transmission lines

There is a delay introduced in the 50% rise time of the input voltages of the I/O lines because of the parasitic inductances in the PDN. This delay can be computed by substituting v(t) as $0.5V_{dd}$ in Equations 20 or 21. Thus with increase in SSN the 50% delay also increases and this causes jitter on signal lines. There will also be an increase in the 50% delay if N, the number of I/O interconnects, increase as shown in Figure 25.

$$v(t) = \frac{Z_0 \times V_{dd}}{Lt_r}\left(\frac{L^2}{Z_0^2}\left[e^{\frac{-t}{\frac{L}{Z_0}}} - 1\right] + \frac{L}{Z_0}t\right) \tag{20}$$

where,

$t \leq t_r$

and

$$v(t) = A + B\left(1 - e^{\frac{-t}{\frac{L}{Z_0}}}\right) \tag{21}$$

where,

$t > t_r$

$A = V_{dd} - [V_{dd} - v(t_r)]\, e^{\frac{t_r}{\frac{L}{Z_0}}}$

$B = [V_{dd} - v(t_r)]\, e^{\frac{t_r}{\frac{L}{Z_0}}}$

For an I/O interconnect bus the number of bits switching simultaneously varies randomly; if all the bits switch simultaneously high then the maximum current is drawn from the power supply causing maximum 50% delay. If bits switch in a pseudo-random pattern, different amounts of currents are drawn creating random SSN [3]. Thus SSN creates a timing uncertainty in the rising and falling edges causing timing jitter in signal lines [3].

This concept was extended to differential transmission lines with discontinuities. Model to hardware correlation proved that there is significant signal to power coupling from differential lines with irregularities to planes in the PDN. Therefore, there is an increase in the overall SSN in the system. Consequently jitter is augmented even on matched differential

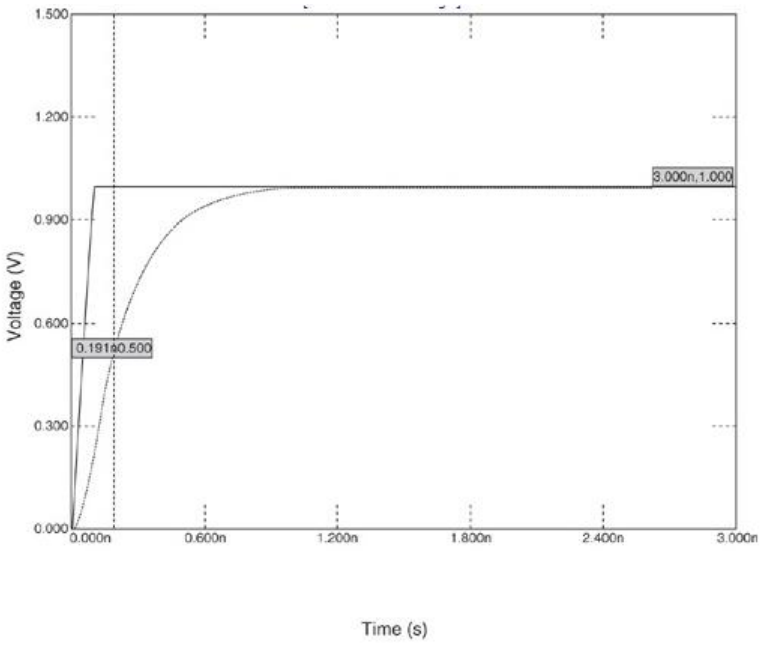

Figure 25. The 50% delay for 1 driver switching and 100 drivers switching [3]

lines. Amount of jitter produced on differential structures with via transitions, via stubs and staggered via transitions was quantified and compared to jitter in differential lines with no discontinuities.

1.4.2 Types of jitter

Previous section correlated jitter and SSN in packaged electronic systems. This thesis work limits the jitter studied to be only that cause by power supply noise. In reality, total jitter in a signal can be described as a combination of random and deterministic jitter [26] [4] as shown in Figure 26. Random jitter is the due to the intrinsic noise present in all semiconductor devices like thermal noise, shot noise and flick noise.

Deterministic jitter is design-related and is caused by ground bounce, reflections, electromagnetic interference (EMI), crosstalk and pattern dependency. Signal to power coupling causes ground bounce and other power supply variations. Power noise produced in this manner causes jitter on the signal lines referenced to these planes. Thus the jitter studied in this thesis work is deterministic and it will not increase with an increase in the number of samples as long as sufficient input bits are provided to the circuit model.

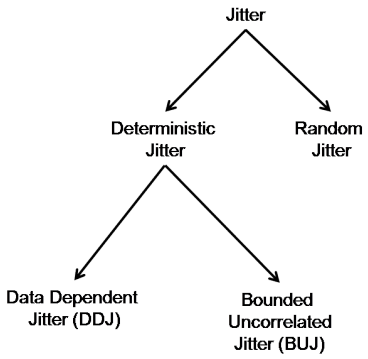

Figure 26. Types of jitter [4]

1.4.3 Data-Dependent Jitter(DDJ)

Specifically, the jitter due to SSN is a combination of data dependent jitter (DDJ) and bounded uncorrelated jitter (BUJ). DDJ is caused by the capacitive effect of electronic systems; where depending on the sequence of bits, transition time for a particular bit is affected by the transition time taken by the bits preceding it. Thus current bit transition times affect the transition of the future bits [4].

Also, as described in the previous section on jitter and SSN the delay caused in copper interconnects because of power noise is highly dependent on the number of simultaneously switching bits. For a data bus, if all bits transition from low to high then the 50% time delay is the highest. Correspondingly there will be very little delay if only one of N bits switch - all these delays in unison cause rise time uncertainty contributing to jitter. Thus jitter due to SSN is highly data dependent ; which is why all simulations performed in time-domain utilized only pseudo-random bit sequences (*PRBS*) to accurately predict jitter.

However, some amount of the jitter measured in these simulations will not be correlated to the data sequence provided to it- instead it could be more dependent on the structure of the interconnect itself such as reflections in the signal path and impedance mismatches. This is referred to as BUJ or Bounded Uncorrelated Jitter.

DDJ can be modeled using a LTI system - where an ideal bit pattern is provided and the response obtained contains DDJ as shown in Figure 27 [4]. Thus if the impulse response of the LTI system is a non-Dirac delta function then output $V_o(t)$ will have deviations at 50%

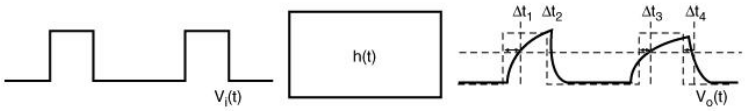

Figure 27. Model of Data-Dependent Jitter (DDJ) [4]

voltage level. From this definition of DDJ certain properties of DDJ can be inferred based on Equation 22 [4].

1. DDJ depends on the impulse response of the interconnect system
2. DDJ depends on the input pattern
3. DDJ will not be created in a lossless, noise-free system where $V_o(t) = V_i(t)$

$$V_o(t) = V_i(t) * h(t) \tag{22}$$

Therefore DDJ will only be caused in lossy systems and depends on the impulse response function of the interconnect through which the signal bits are transmitted. Therefore it can be inferred that smaller the bandwidth of the impulse response then more DDJ is introduced. The type of jitter measured in simulations is peak to peak jitter. Since jitter produced by SSN is only deterministic and not random RMS jitter need not be considered.

1.5 Thesis Outline

Rest of this thesis is organized in the following manner:

1. Signal to Power coupling is described in Chapter 2:

(a) Passive test vehicles designed to capture the noise effects of irregular differential lines are described.

(b) Comparison between measurements and simulations for signal to power coupling in the different test cases is presented.

(c) Model to hardware correlation is performed and equivalent circuit models of the different test structures is created using Agilent ADS [27].

2. Jitter is presented in Chapter 3:

(a) Jitter in differential test structures with irregularities is predicted using the equivalent ADS circuit model in time domain simulations.

(b) SSN is predicted for these differential structures

3. Conclusion of this thesis work is presented in Chapter 4

CHAPTER 2

SIGNAL TO POWER COUPLING

As described in Chapter 1 irregularities in differential signaling can couple significant signal energy to the system PDN. This section delves into the reasoning behind this phenomenon and provides model to hardware correlation for the same. Measurements and simulations were performed for three types of structures with discontinuities:

1. Differential Via Transitions
2. Differential Via Stubs
3. Staggered Differential via transitions

Model to hardware correlation was performed with simulations using the Multi-layer Finite Difference Method (MFDM) [6] implemented in tools Mixed Signal Design Tool 1 (MSDT1) [28] and Panswitch [5]. The methods implemented in Panswitch is described in [5]. These simulations were compared compared to measurement results. The test vehicles manufactured for the above structures are described below:

2.1 Description of Test Vehicle with Irregularities

Different test structures were created to quantify the energy coupled from signal lines to plane pairs in power distribution networks (PDN). All test structures contain a 30mm by 30mm pair of square planes. The dielectric used was FR4 with dielectric constant,ϵ_r = 4.4 and tan(δ) = 0.02 with the dielectric thicknesses indicated in Figure 28. The traces and planes were made from copper whose conductivity,σ = 5.8 x $10^7 S/m$. Detailed description of each type of measurement structure is given below:

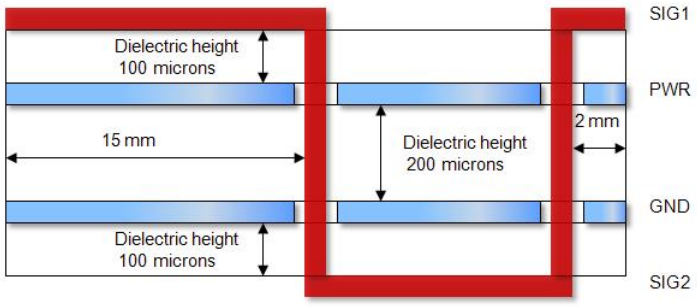

Figure 28. Cross section of the via transition structure to investigate signal to power coupling

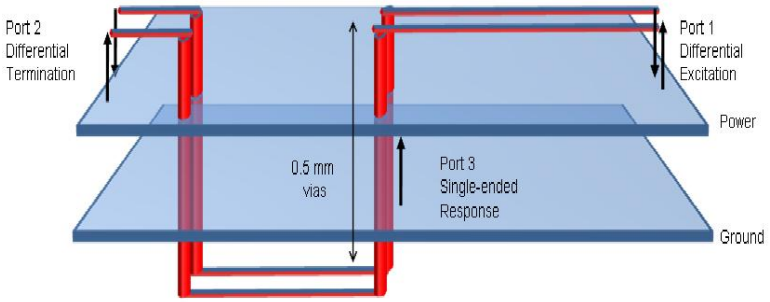

Figure 29. Differential via transition structure with measurement ports 1, 2 and 3

2.1.1 Via transitions

Single-ended and differential structures with via transitions were manufactured with identical cross-sections as illustrated in Figure 28. The signal lines undergo a microstrip-to-microstrip transition from layer SIG1 to layer SIG2 through a pair of planes, PWR and GND. Via transitions for single-ended and differential microstrip lines occur in the manner indicated in Figure 28; one via pair passes through the center of the planes while the other transitions 2 mm away from the edge of the planes.

The single via transition structure consists of transmission lines, designed on layers SIG1 and SIG2, with characteristic impedance, $Z_0 = 50\ \Omega$ and a via transition with 300 μm pads and 150 μm drill size. To investigate the effect of the via discontinuity, an equivalent

$\frac{S}{W}$ ratio used in differential structures.

Spacing by width ratio $\frac{S}{W}$
1.5
2.5
3.3
4

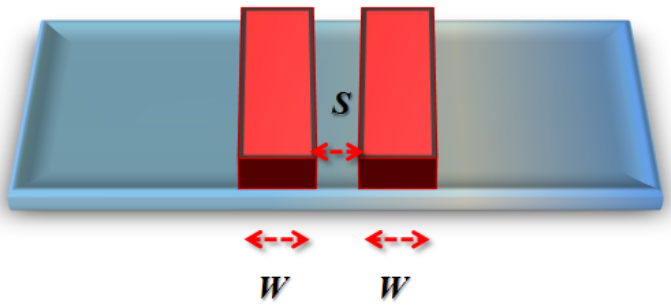

Figure 30. $\frac{S}{W}$ ratio used in differential structures

single transmission line structure was also manufactured on layer SIG1 with $Z_0 = 50\ \Omega$.

In contrast, differential via transition structures were designed with differential lines of $Z_{diff} = 100\ \Omega$ for varying $\frac{S}{W}$ ratios as shown in Figure 30. S and W are the edge-to-edge spacing and width of differential lines respectively as illustrated in Figures 29 and 30. The differential via dimensions matched that of single vias and separation between them varied with change in $\frac{S}{W}$ ratios. Equivalent differential lines were also manufactured for varying $\frac{S}{W}$ ratios.

2.1.2 Via stubs

Another irregular structure in boards and packages is caused by through-hole vias used in lieu of blind/buried vias. These through-hole vias act like via stubs that radiate significant signal energy into the PDN. The via stub structure considered specifically in this thesis was a through hole via hanging from a microstrip line on SIG1 layer in both the differential and single-ended test vehicles as shown in Figure 31. The dimensions of the signal lines and vias were identical to the via transition case shown in Figure 28.

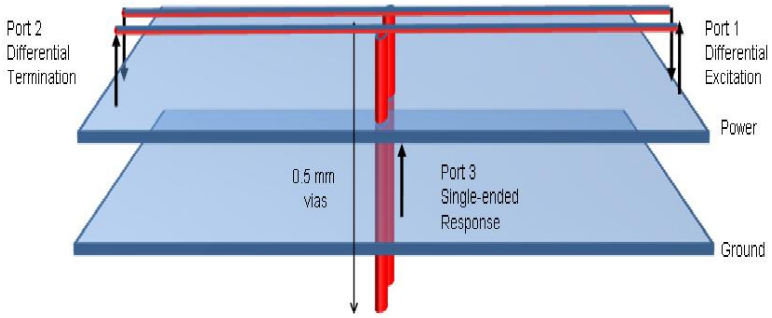

Figure 31. Differential via stub

Table 1. Staggered spacing 'a' used in differential via transition structures.

Staggered Spacing 'a'
0 mm
0.1 mm
0.2 mm
0.5 mm
1.0 mm

2.1.3 Staggered differential via transitions

High noise rejection is the main advantage of differential signaling and it can be utilized only by routing the individual traces in close proximity. Moreover, the traces have to be symmetric so that any common mode noise injected into the lines can cancel out. Thus the general rule of thumb is to route discontinuities like via transitions in a symmetric manner so that noise infiltrates both the lines in the differential pair equally.

Test vehicles were designed to probe into the effects of staggered differential via spacing on the signal to plane coupling. Staggered spacing refers to increasing asymmetry in the placement of vias in differential lines as shown in Figure 32. The total physical length of each line in the differential pair still remains the same, that is, there was no skew introduced in the differential structures. All other dimensions were identical to the case described in the differential via transition section. In all the test vehicles effect of staggered vias on plane pair coupling was investigated by increasing spacing 'a' from 0 mm to 1 mm as shown in Table 1.

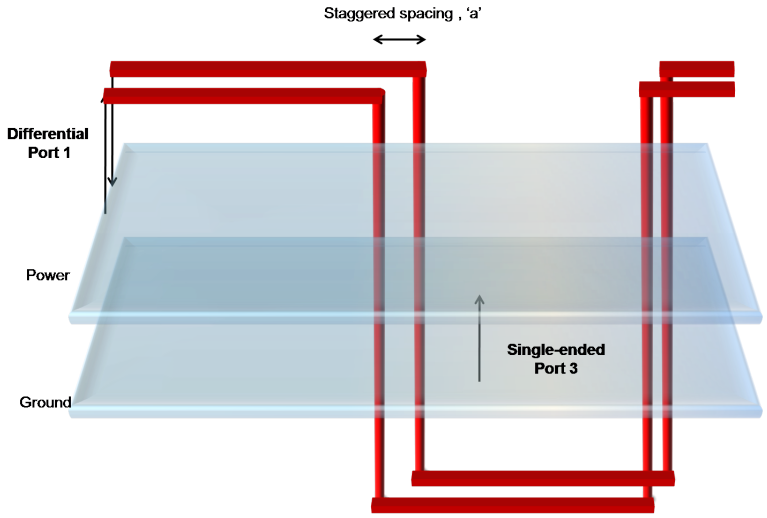

Figure 32. Staggered differential via transition

2.2 Coupling to Planes for Ideal Differential Transmission Lines

Signal to power coupling in ideal differential lines were investigated to accurately ascertain the significance of the increase in signal energy loss due to discontinuities. Simulations and measurements were performed for both single-ended and differential lines. Coupling to planes was observed by exciting the signal lines at one end and simultaneously probing at a point between the plane pairs. That is, signal to plane coupling is measured by the S_{31} parameter in single-ended structures and the differential to single-ended mixed-mode parameter, S_{DS31}, in differential structures.

In the differential via transition structure, ports 1 and 2 are considered to be differential ports while port 3 is single-ended as illustrated in Figure 29 while all three ports are single ended for the equivalent single via transition structure. Figure 33 presents the measured coupling parameters for three cases; for a differential via transition, single via transition and a differential transmission line with Z_{diff} = 100 and $\frac{S}{W}$ = 3.3.

1. Differential Via Transition with Z_{diff} = 100 Ω, W = 0.17 mm and S = 0.55 mm
2. Single Via Transition with W=0.17 mm and Z_0 = 50 Ω
3. Differential Transmission line with Z_{diff} = 100 Ω, S = 0.55 mm and W = 0.17 mm.

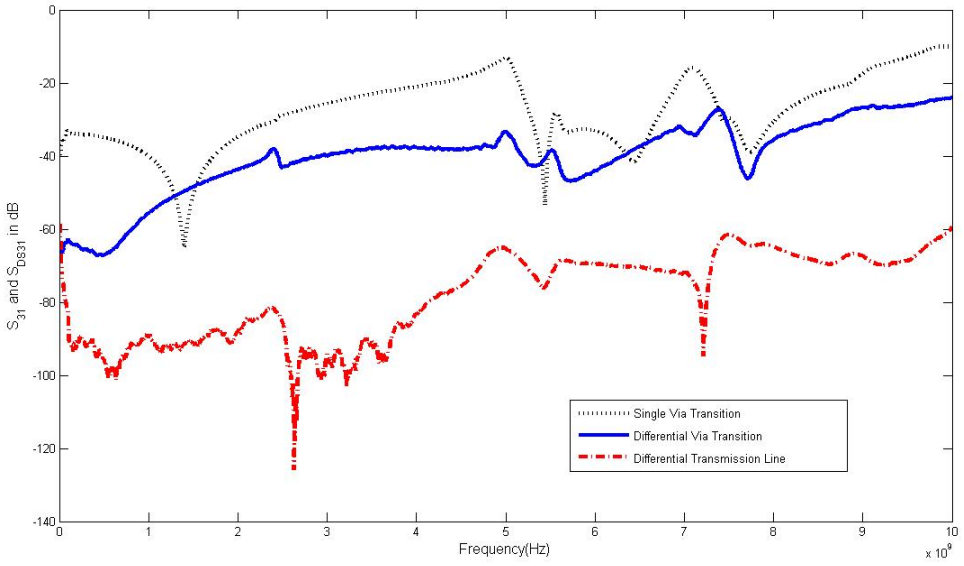

Figure 33. Signal coupling to planes for single via transition, single transmission line and differential via transition - S_{31} parameters in dB

Therefore simulations indicated that although energy coupling due to differential vias is lower than that for a single via transition, it is still significantly more than the coupling for differential lines with no discontinuity. This proves that presence of irregularities such as via transitions increases the signal coupling to planes from -80 dB to -30 dB in differential signaling.

2.3 Variation of Coupling with $\frac{S}{W}$ Ratio in Differential Via Transitions

There is good correlation between Panswitch simulations [5] and measurements for differential via transitions - one example with $\frac{S}{W} = 4$ is illustrated in Figure 34. Measurement results for all other structures in which $\frac{S}{W}$ ratio was varied also compares well with the simulated results using Panswitch (MFDM solver) [5] [6]; one such example is shown in Figure 35.

Correspondingly, comparison of simulations from Panswitch (MFDM Solver) [5] [6] and measurements results for signal to power coupling in a single via transition structure is presented in Figure 36. Therefore there exists good model to hardware correlation for

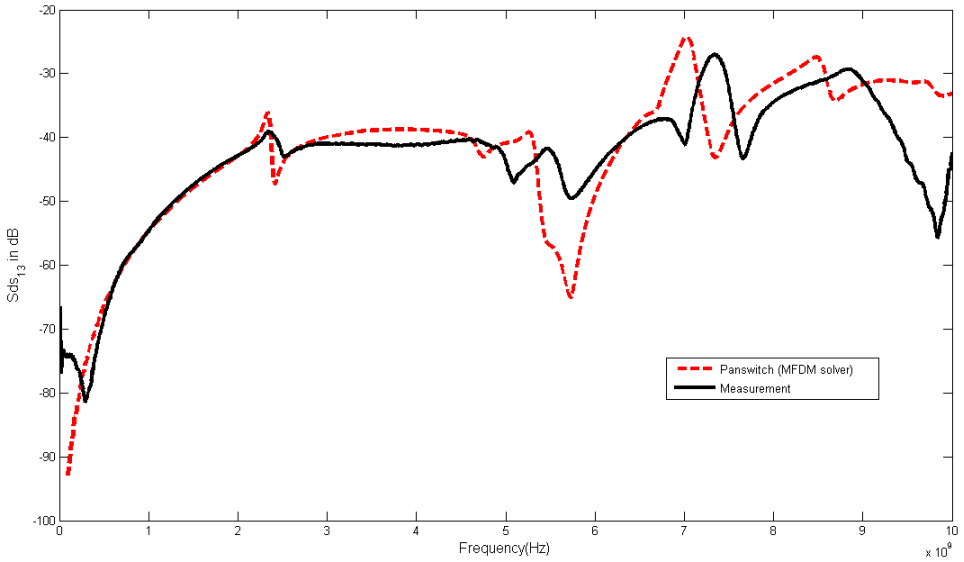

Figure 34. Measurement versus simulation results for coupling to planes for differential via transition with $\frac{S}{W} = 4$

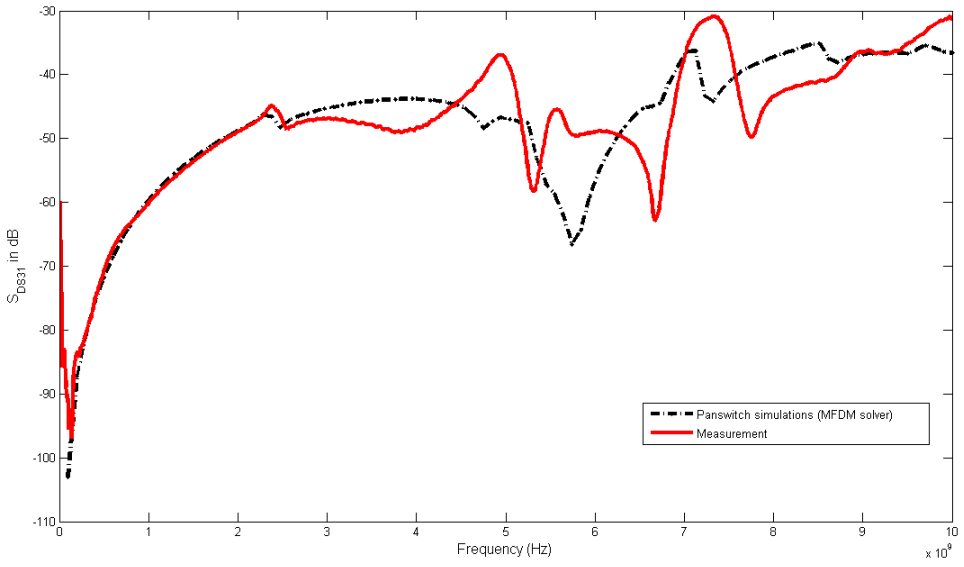

Figure 35. Measurement versus simulation results for coupling to planes for differential via transition with $\frac{S}{W} = 1.5$

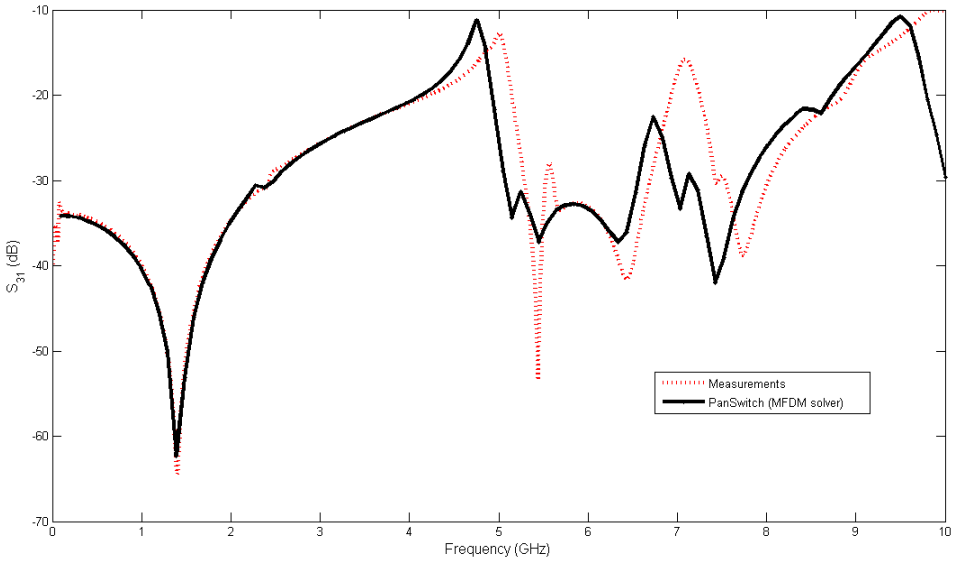

Figure 36. Coupling to planes for single via transition structure S_{31} in dB

signal to power coupling in single ended structures also.

Next,the change in energy coupling to planes from differential lines with via transitions due to the variation of $\frac{S}{W}$ ratios was investigated. Spacing, S refers to the edge-to-edge spacing between each line in the differential pair and W is the width of the line as indicated in Figure 30. The mixed-mode S-parameter S_{DS31} for structures with $\frac{S}{W}$ ratio of 1.5, 2.5, 3.3 and 4 were measured.

As expected, it was found that increase in $\frac{S}{W}$ ratio results in the augmentation of coupling to planes which is shown in Figure 37. This implies that in the presence of via transitions one must ensure tight coupling between differential lines to reduce energy leaking to planes.

Thus, the rule of thumb is to keep $\frac{S}{W} \leq 3$ to ensure adequate coupling between the lines in the differential pair [13]. Model to hardware correlation proves that coupling to planes is significantly larger in the presence of via transitions than in symmetric and closely-coupled differential lines

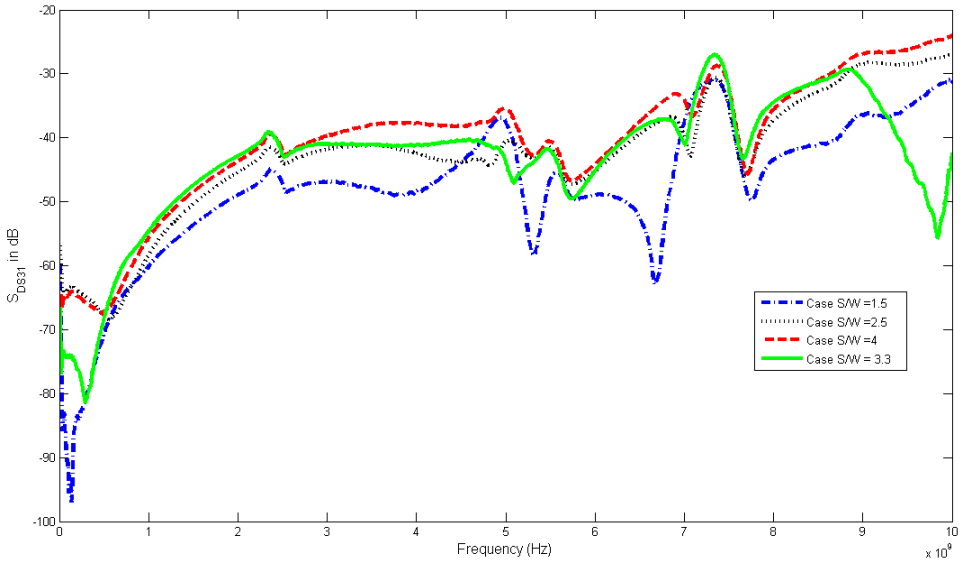

Figure 37. Coupling to planes for differential via transitions: varying spacing by width ratios($\frac{S}{W}$) (S_{DS31}) in dB

2.4 Coupling to Planes in Via Stub Structure

The difference in signal to power coupling was investigated for a single via stub structure and the equivalent differential via stub structure. Measurements indicate that the level of coupling in differential via stub structure is lower than that of single via stubs as presented in Figure 38. Differential via stubs still produce significant coupling at approximately 10 GHz as indicated by measurements of this test vehicle. Therefore, at high data rates unexpected power noise could be produced if this anomaly is ignored.

2.5 Coupling to Planes in Staggered Via Transitions Structure

Measured S_{DS31} for the different values of asymmetric spacing, 'a' are displayed in Figure 39. Increase in via asymmetry amplifies the signal to plane coupling from -35 dB to -25 dB. A rule of thumb can be formulated from these results; staggering via transitions by more than 0.2 mm causes significant increase in energy coupling to PDN. Therefore to minimize signal to plane coupling, differential vias must be routed in a symmetric manner with 'a' $\leq$ 0.2 mm.

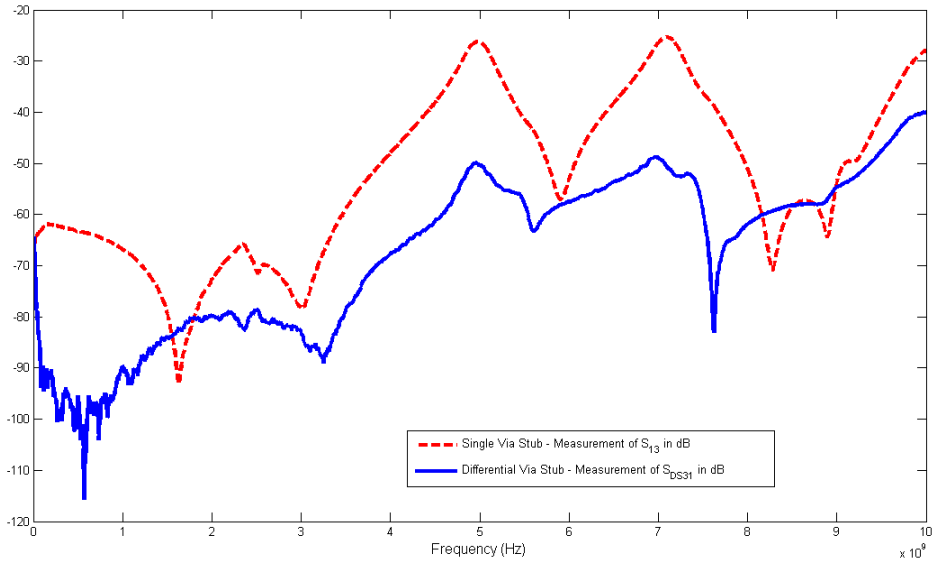

Figure 38. Coupling to plane pair due to differential and single via stubs S_{31} in dB

In this section it was quantitatively established that irregularities in differential lines like via transitions, via stubs and staggered vias amplify signal to plane coupling. It is important to be aware of such discontinuities while designing differential lines for high data rates. Loss of signal energy could deteriorate the quality of signal transmitted at high frequencies, hereby causing jitter and fall in the voltage margin.

2.6 Model to Hardware Correlation

Simulations performed using Panswitch (MFDM solver) [5] [6] provided good model to hardware correlation with measurements for various irregular differential structures as illustrated in Chapter 2. However in order to examine the effects of signal to power coupling in time domain we need a time-domain simulator. Another method of examining frequency domain effects in time is to convert S-parameter results to an equivalent time-domain circuit model and this is performed using Agilent ADS [27].

In order to adopt this method an equivalent circuit model incorporating both PDN and Signal Distribution network (SDN) was created and at first tested in frequency domain.

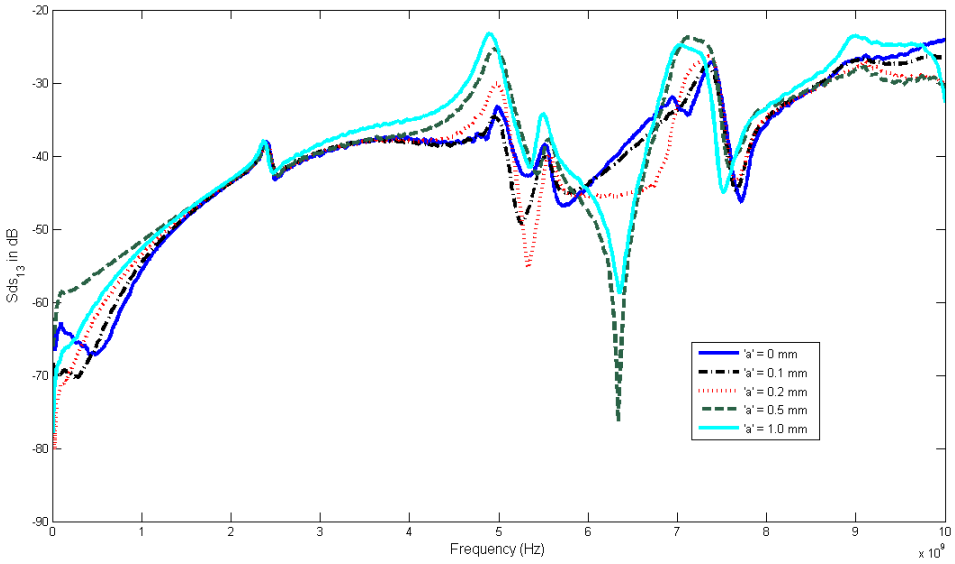

Figure 39. Coupling to planes due to staggered differential via transitions S_{DS31} in dB

Every test structure considered consists of a pair of planes representing the PDN and differential microstrip lines forming the SDN. Using the multiconductor transmission line theory (MTI) the power/ground planes are also defined as conductors in addition to the signal traces [29] [3].

However, combining the models for power supply planes and the signal transmission lines generally results in numerous coupling terms. The concept of modal decomposition [30] can be applied here to simplify the model; by decomposing the MTL modes associated the SDN and PDN, complex coupling terms can be removed. Thus power/ground planes and SDN can be modeled separately and combined together by superposition of the decoupled modes at the terminals using controlled sources as indicated in Figure 40 [3]. For microstrip lines referenced to ground planes the coupling factor, k = 0 and if referenced to power planes then k= -1 in the figure.

The modal decomposition method is simpler for microstrip lines referenced to PDN planes. The fields in the microstrip are shielded from the fields between the power/ground planes by the reference plane at high frequencies as illustrated in Figure 41; therefore

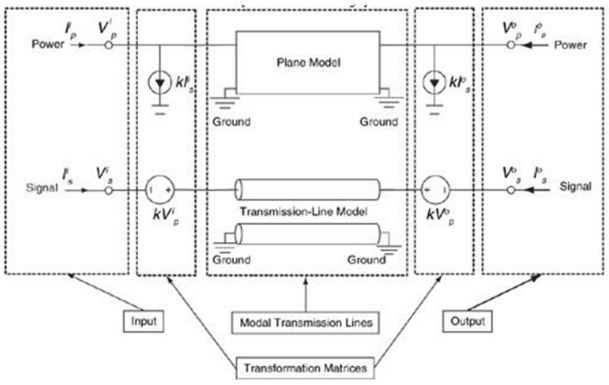

Figure 40. Generic modal decomposition method for signal lines referenced to non-ideal PDN [3]

microstrip modes and power plane modes are decoupled and can be modeled separately. Thus the multiconductor transmission line theory model considers microstrip and the plane pair model as two uncoupled transmission lines [23].

This modal decomposition method was applied to the structures under consideration, namely, differential via transition and single via transition to obtain equivalent circuit models. The S-parameter frequency domain response was compared to measurements and suitable m atch was obtained as described in the following subsections.

2.6.1 Equivalent model for differential via transition

The equivalent model for the differential via transition structure had to incorporate the non-idealities in the PDN and SDN accurately. In order to construct the model ,initially, a structure containing a single transmission line with one via discontinuity was considered; the ground reference for such a structure was assumed to be very far away as indicated in Figure 42. The single via transition structure was considered as an equivalent 9 port network with the port locations as indicated in Figure 42; all the ports are with reference to the ideal ground shown in the figure.

Therefore the equivalent model for this single via transition structure with 9 ports was deduced as shown in Figure 43. Matrices Y_l and Y_p signify the 2 port admittance matrices

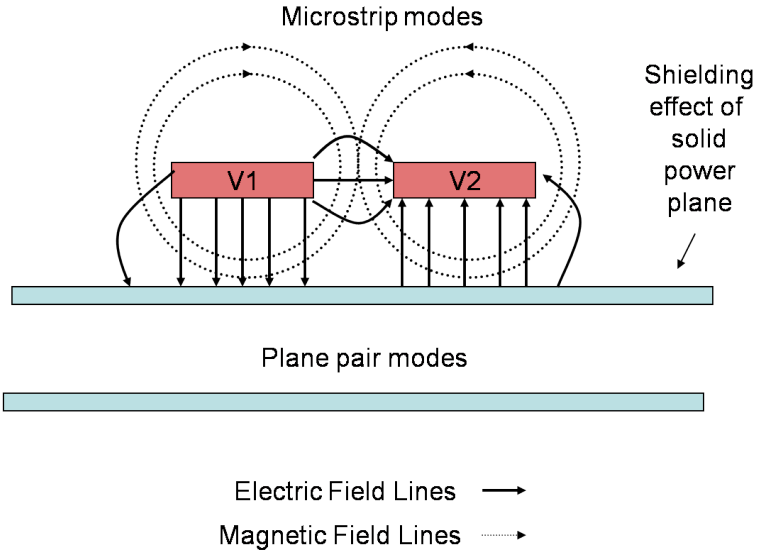

Figure 41. Uncoupled microstrip and plane pair modes

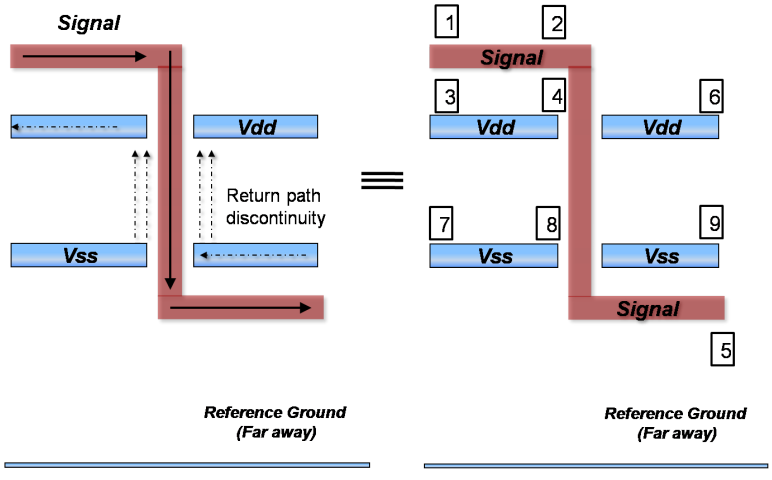

Figure 42. Single via transition and equivalent 9-port network

for the microstrip transmission line and the two layer plane pair respectively. For simplicity, initially the via was considered to be ideal short circuit.

Since the ideal reference ground exists far away from the plane pair, another two port network exists between ports (7,8) and (8,9) with the admittance matrix Y_i signifying the parasitic impedances that exist in the ground network from the V_{ss} plane to the ideal ground. Matrices Y_l,Y_i and Y_p can be defined as follows:

$$Y_l = \begin{pmatrix} Y11l & Y12l \\ Y21l & Y22l \end{pmatrix} \tag{23}$$

$$Y_p = \begin{pmatrix} Y11p & Y12p \\ Y21p & Y22p \end{pmatrix} \tag{24}$$

$$Y_i = \begin{pmatrix} Y11i & Y12i \\ Y21i & Y22i \end{pmatrix} \tag{25}$$

The parasitic impedances in the ground reference loop given by 2-port Y matrix,Y_i, can be represented by equivalent lumped inductance L_i and capacitance C_i to the ideal ground. In practical circuits the loop to ideal ground is very long since the current has to travel from the on-chip transistors to the power supply on the motherboard. Therefore, $L_i \approx \infty$ and capacitance $C_i \approx 0$ which converts Y_i to a zero matrix.

This assumption simplifies the equivalent 9-port Y parameter matrix resulting from the model in Figure 43 to a 6-port Y parameter matrix shown in Equation 26 after matrix column and row operations. Therefore, the complicated 9-port equivalent model can be simplified to 6-port model that accounts for non-ideal power distribution network and signal trace references to planes.

Thus the 9-port network model shown in Figure 43 reduces to the equivalent 6-port model illustrated in Figure 44 because of the assumptions of $L_i \approx \infty$ and $C_i \approx 0$. In this 6-port model, although the second microstrip line is referenced to an ideal ground the parasitics in the ground reference were taken into account while simulating the power/ground

planes. The simulation procedure in the MFDM solver takes care of this by considering loop inductances instead of partial inductances.

The admittance matrix for this 6-port network when calculated will give rise to the same Y parameter matrix in Equation 26. Therefore the model in Figure 44 considers all the non-idealities in the via transition structure like the non-ideal planes and hence can be utilized for all time domain simulations.

$$\begin{pmatrix} Y11l & Y12l & -Y11l & -Y12l & 0 & 0 \\ Y21l & Y22l + Y11l & -Y21l & -Y22l & Y12l & 0 \\ -Y11l & -Y12l & Y11p + Y11l & Y12p + Y12l & 0 & 0 \\ -Y21l & -Y22l & Y21p + Y21l & Y22p + Y11p + Y22l & 0 & Y12p \\ 0 & Y21l & 0 & 0 & Y22l & 0 \\ 0 & 0 & 0 & Y21p & 0 & Y22p \end{pmatrix} \tag{26}$$

The equivalent model should include a 2-port lumped model for the via transition as shown in Figure 45 for accuracy. Via discontinuities exhibit a capacitive coupling to reference planes and also an extra series inductance because of current crowding near the via hole [31]. However, the capacitive coupling was found to be insignificant using parametric sweep simulations and only self-inductance of the vias was considered.

When the equivalent model in Figure 45 was utilized for the differential via transition structure then a few changes had to be performed. For one, the number of interconnects in the microstrip model was doubled and the via transition model had to account for mutual inductance. The number of reference points on the power/ground planes were also increased. In spite of these changes the basic methodology for modeling the structure remains the same and the non-idealities were still captured by the model.

When modal decomposition was applied to the differential via transition structure then coupled microstrip lines and power/ground planes were initially separately simulated. Then their S-parameter responses were combined as illustrated in Figure 45. The differential via

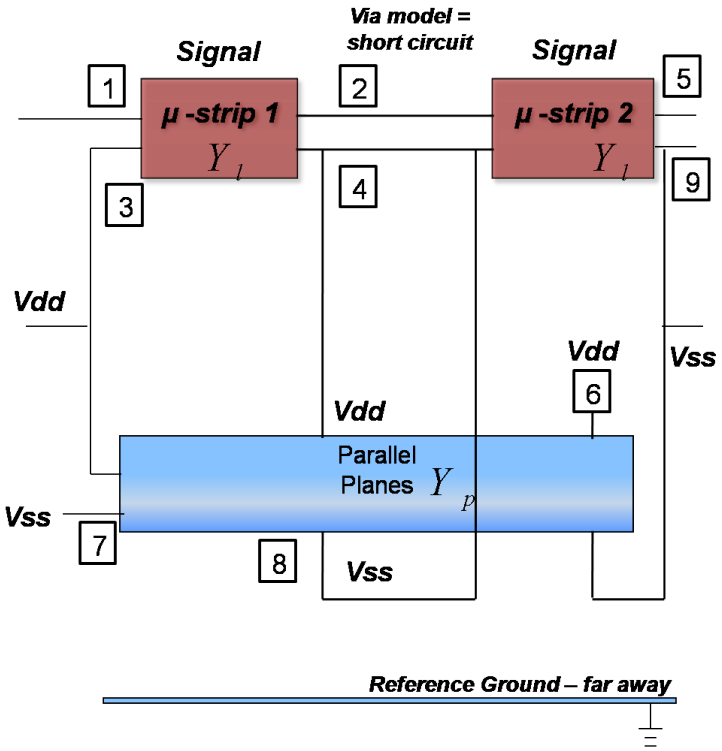

Figure 43. Equivalent model for single via transition with 9-port network

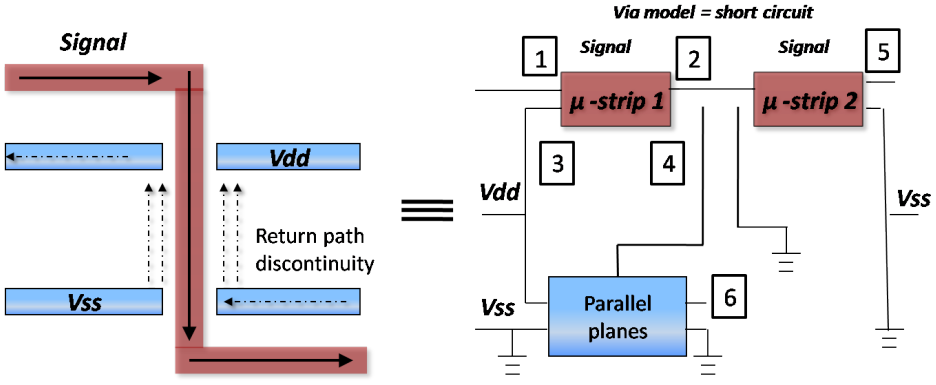

Figure 44. Equivalent model for microstrip-to-microstrip via transition - Ideal ground reference

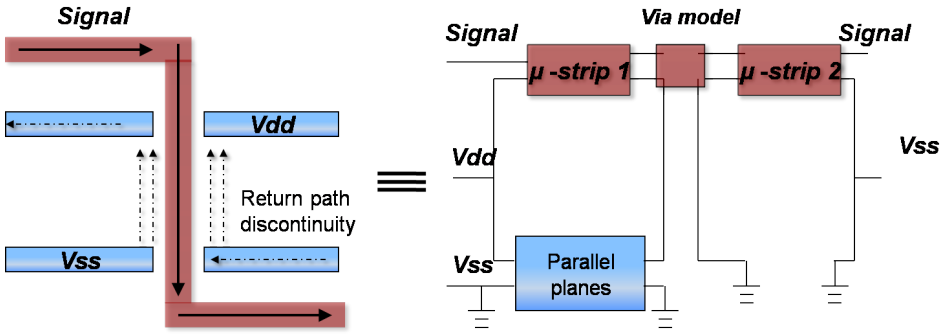

Figure 45. Equivalent model for a microstrip-to-microstrip via transition with lumped via model

transition was broken into three blocks, two microstrip lines and one plane pair, to construct the equivalent model.

In the model, the top plane is the power (V_{dd}) plane while the bottom is the ground (V_{ss}) plane. Each block in the model consists of pre-simulated S-parameter files. The S-parameter frequency response for the microstrip lines was obtained from Agilent ADS which uses analytical models for transmission lines from [32]. The plane pair block was simulated using Panswitch (MFDM solver) [5] [6].

A 2-port lumped model was considered for each of the vias in the differential pair since they are electrically short when compared to the considered frequency range [33]. The via model was constructed from two simple inductors, one for each differential line. The model accounted for mutual inductance as well. Formulae for self inductance, 'L' and mutual inductance, 'M' are given in Equations 27 and 28 [34] respectively.

$$L = \frac{\mu b}{2\pi}\left[\ln\frac{2b}{a} - \frac{3}{4}\right] \tag{27}$$

where,

a - Radius of the via

b - Length of the via

$$M = \frac{\mu b}{2\pi}\left[\ln\left(\frac{b}{d} + \sqrt{1+\frac{b^2}{d}}\right) - \sqrt{1+\frac{d^2}{b}} + \frac{d}{b}\right] \tag{28}$$

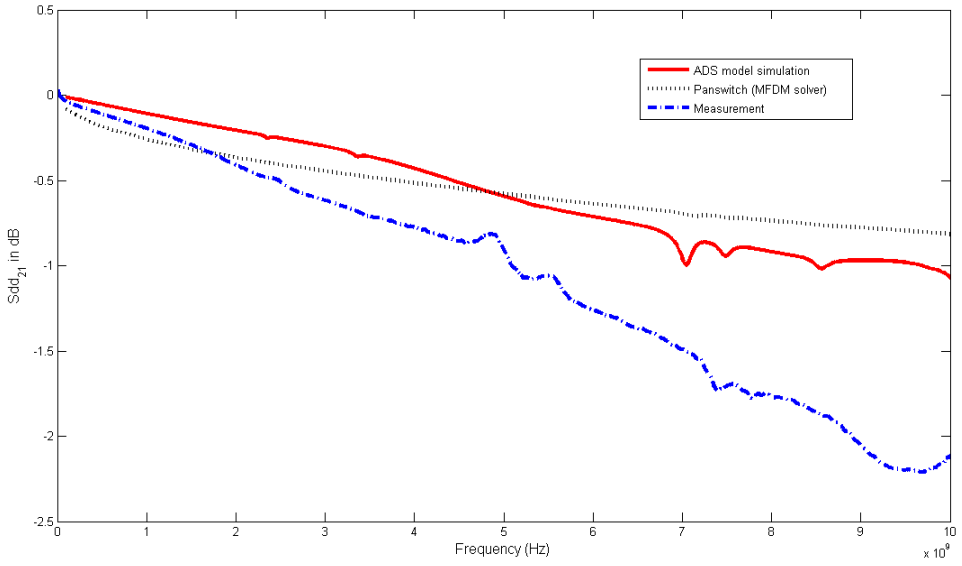

Figure 46. Comparison of differential insertion Loss S_{DD21} between the equivalent model, measurement results and other simulations

where,

d - Separation between the via pair

b - Length of the vias

The differential insertion loss S_{DD21} obtained from the model was compared to measurements and simulations as indicated in Figure 46. Signal to plane coupling, S_{DS31} was also compared as shown in Figure 47. It was found that the equivalent circuit model correlated well with measurements for the differential via transition structure.

2.6.2 Equivalent model for single via transition

Modal decomposition method and the equivalent model did not vary from the differential via transition structure to the corresponding single-ended one. The only obvious difference is that the extracted S-parameters for the microstrip block in Figure 45 are for a single-ended transmission line. S_{21} results from the circuit model are compared with measurements and simulations as shown in Figure 48.

Thus jitter caused by SSN can be accurately calculated from the equivalent models developed for differential via transition and single via transitions. Certain conclusions can

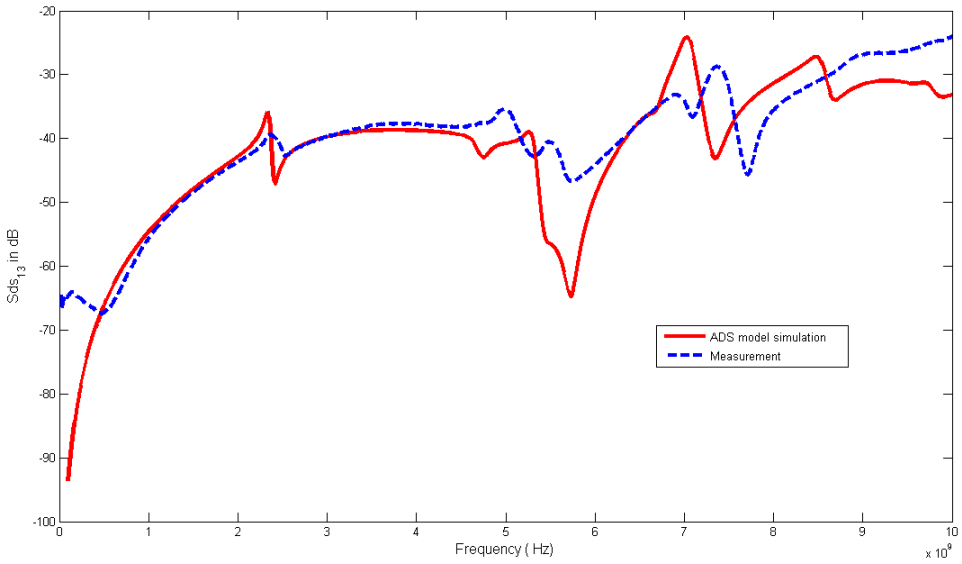

Figure 47. Comparison of signal to power coupling S_{DS31} between the equivalent model, measurement results and other simulations

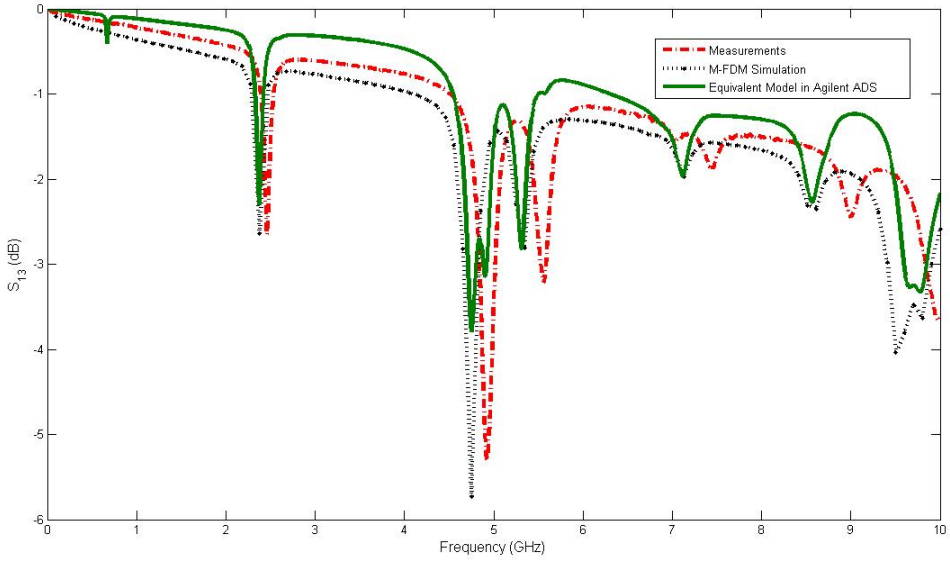

Figure 48. Comparison of insertion loss S_{21} between the equivalent model, measurement results and other simulations for single via transition

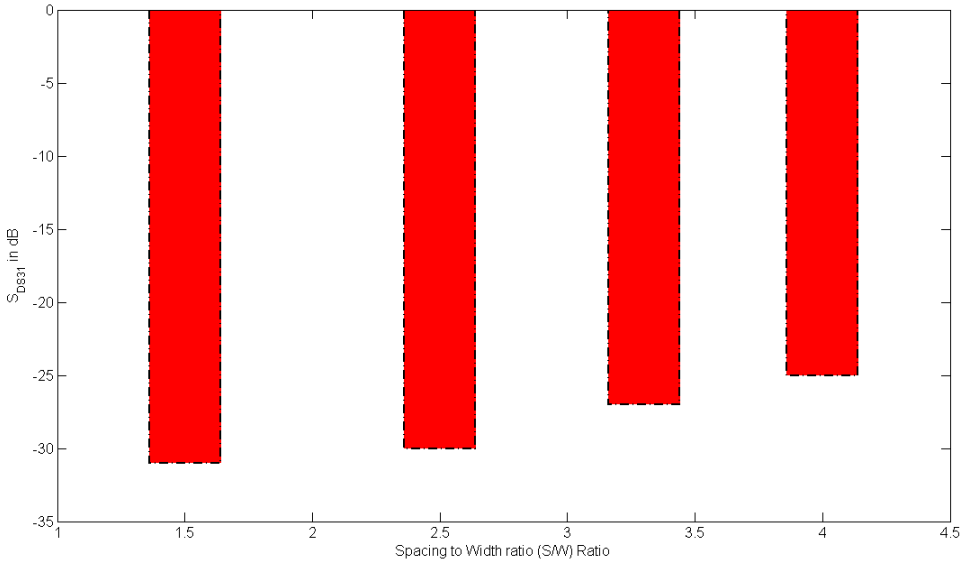

Figure 49. Variation of signal to power coupling with $\frac{S}{W}$ ratio

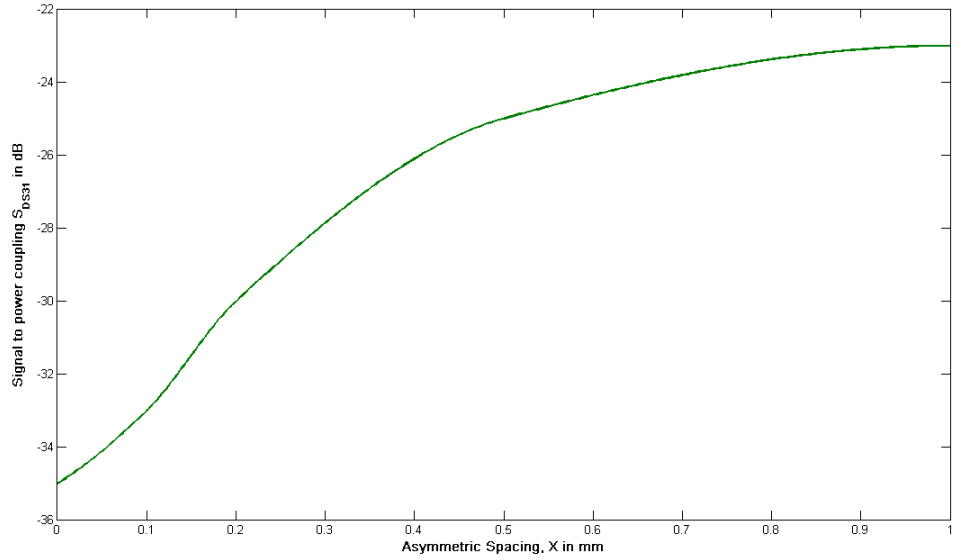

Figure 50. Variation of signal to power coupling with staggered spacing 'a'

be drawn on signal to power coupling in differential signaling from the results presented in this section. First, increase of spacing by width ratio $\frac{S}{W}$ in differential lines with via transitions results in the corresponding amplification of noise coupling to PDN planes as

shown in Figure 49. Thus a prudent designer should space differential lines with non-idealities as close together as possible and keep $\frac{S}{W} \leq 2.5$.

Second, increase in asymmetric spacing of via transitions in differential signaling was found to amplify signal to power coupling as shown in Figure 50. A general rule of thumb for designing asymmetric via transitions can be formulated from these results; staggered spacing X $\leq$ 2.5 in order to control signal energy loss and noise coupling to planes.

In the next section simulations were performed in the time domain to determine if discontinuities in differential signaling produce equivalent degradation effects in signal integrity.

CHAPTER 3

NOISE INDUCED JITTER

Previous chapter provided model to hardware correlation for energy coupling from signal traces to the PDN in a few differential structures. Although the amount of energy coupled to planes for differential signaling is lower when compared to single-ended structures, it was found to cause power noise on the plane pair. In reality differential traces also reference to planes in the PDN therefore, some of this switching noise could get coupled to signal lines causing jitter.

In ideal differential traces this phenomenon was less pronounced because of the differential voltage considered between the lines. However, in the presence of discontinuities the common mode effects produced on differential lines do not cancel out, causing SSN and consequently produce jitter.

For observing jitter on each type of irregularity(via transition or staggered vias) different models were constructed as described in detail in Section 2.6.1. Hence jitter was first examined for differential via transition structures with varying $\frac{S}{W}$ ratios and was compared to jitter found in the corresponding single-ended structure. Finally the amount of jitter caused by staggering differential via transitions was quantitatively determined.

3.1 Driver Model

The type of driver considered in simulations will have considerable impact on the results obtained. Hence, an inverter circuit was implemented in Agilent ADS circuit solver using a voltage-controlled voltage switch. This switch approximated a CMOS transistor by varying the output resistance between two saturation states depending on the input voltage. A pseudo-random bit source (PRBS) with a linear feedback shift register design was utilized to provide random input bits to the inverter circuit as shown in Figure 51.

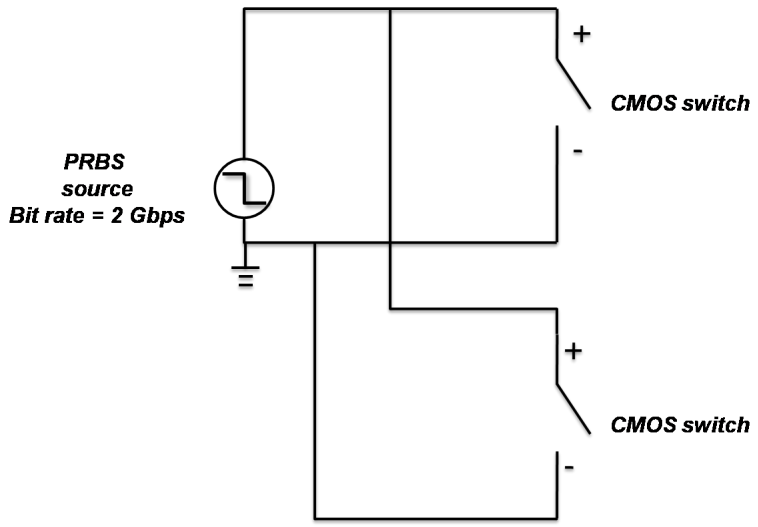

Figure 51. Driver model : simulates CMOS inverter switching.

3.2 Jitter in Differential Via Transitions

From measurements it was observed that increase in $\frac{S}{W}$ ratio of differential lines resulted in a corresponding amplification of signal to power coupling in differential via structures (illustrated in Figure 37). In this section, results of a time domain analysis of the signal to power coupling is presented. The equivalent model developed in Section 2.6.1 was used to determine the amount of jitter on differential lines in the presence of vias. The effect of $\frac{S}{W}$ ratio of differential lines on jitter was also investigated.

Initially, 2-D voltage distribution plot of the power/ground planes was performed to verify the fluctuations caused by the return path discontinuity. Then to estimate the amount of SSN caused by via transitions, simulation of the time-domain fluctuation of supply voltage was performed. The power rail supplying $V_{dd} = 1.0$ volts was simulated over the entire time of simulation. SSN measured during simulations is reported in the following sections.

In this thesis work only peak to peak jitter is considered because jitter due to SSN is design-related and hence deterministic. RMS jitter was omitted in the analysis because it is indicative of the random jitter components rather than deterministic ones [4]. Peak to peak jitter is measured as shown in Figure 52.

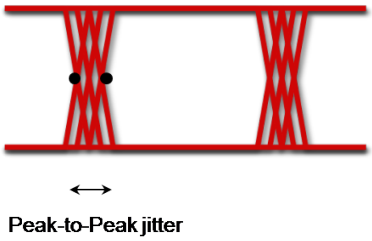

Figure 52. Peak to peak jitter.

3.2.1 Return current path in differential via transition structure

Frequency spectrum of the input signal contains components at many frequency points due to the randomness of the voltage bit stream (Pseudo-Random Bit Sequence). The return current in the differential structure is dependent on the input voltage; hence it will also contain significant components at many frequencies. The return current path is indicated for a differential via transition in Figure 45.

Moreover, in the differential via transition structure the return current flows through the dielectric between the planes because of the via discontinuity. Since the impedance profile of the plane pair is frequency dependent, a return displacement current with many frequency components will face varying impedance. This will cause variance in the rising and falling slopes of the output signal during transitions between voltage levels causing jitter on these lines. Jitter will be further exacerbated when the impedance of the plane pair increases due to signal to power coupling. Thus actual amount of jitter caused will largely depend on the quantity of noise coupled to the power/ground planes increasing the PDN impedance.

On a separate note as shown in Figure 45, when the drivers switch from low to high or high to low, return currents of the transmission lines flow on the power/ground planes. This is because at high speeds return currents follow the path of least inductance and for a signal trace the smallest inductive loop between signal and return current lies directly beneath it [14]. Current distribution for a microstrip trace and its reference plane illustrate this phenomenon in Figure 22.

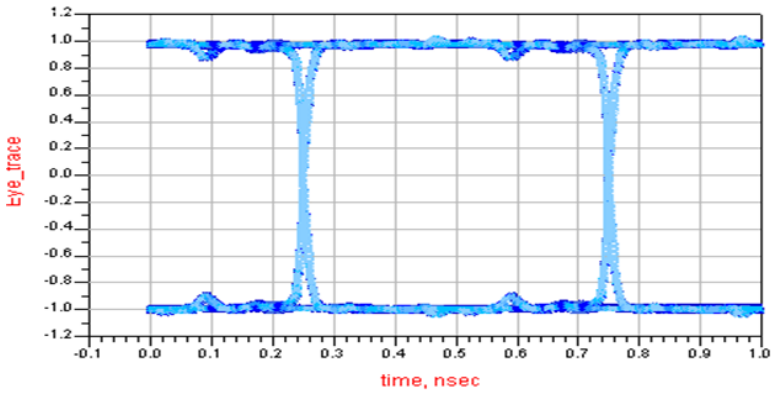

Figure 53. Eye diagram for differential line with spacing by width ratio $\frac{S}{W}$ equal to 1.5.

Table 2. Peak to peak jitter calculated for differential signaling.

Spacing by Width Ratio $\frac{S}{W}$	Peak to Peak jitter for differential lines with no vias	Peak to Peak jitter for differential lines with vias
1.5	0.26 psec	11.09 psec
2.5	0.35 psec	12.10 psec
3.3	1.20 psec	12.30 psec
4	0.64 psec	13.30 psec

3.2.2 Comparison with perfect differential lines

Jitter in differential lines without any discontinuities or irregularities was computed to provide a basis for the other structures. For differential lines with spacing to width ratio, $\frac{S}{W}$ at 1.5, 2, 3.3 and 4 jitter was calculated after simulating the time domain model in Agilent ADS at a data rate of 5 Gbps. The eye diagram for a 29 mm long differential line with spacing to width ratio $\frac{S}{W}$ = 1.53 and 100Ω differential impedance is shown in Figure 53. The eye diagram was plotted for the differential output voltage V_{diff} and peak to peak jitter was calculated to be 0.26 psec. The jitter for all the other differential line cases with varying $\frac{S}{W}$ ratio is displayed in Table2. Thus differential lines display negligible jitter in the absence of via discontinuities.

3.2.3 Jitter from simulations

The time domain simulation of differential via transitions used the equivalent model shown in Figure 45. Differential excitation was provided by two pseudo-random bit sources and the lines were correctly terminated with a 100Ω resistor. The jitter caused due to the loosely

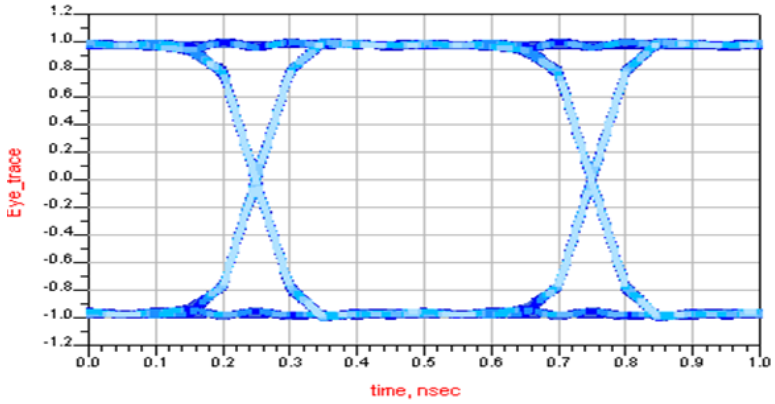

Figure 54. Eye diagram for differential via transition with spacing by width ratio $\frac{S}{W} = 4$.

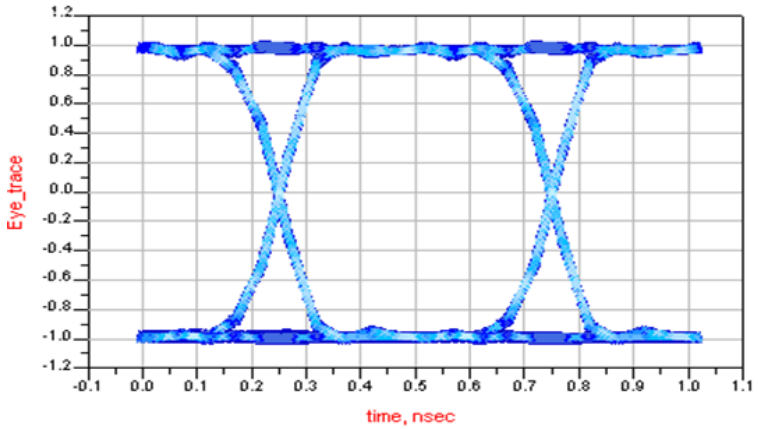

Figure 55. Eye diagram for differential via transition with spacing by width ratio $\frac{S}{W} = 1.5$.

coupled differential via transition structure lines where $\frac{S}{W} = 4$ is shown in Figure 54. The data rate of the random input bit stream was maintained at 2 Gbps. The jitter computed for this case was equal to 13.3 psec. Eye diagram for the tightly coupled differential via transition was also plotted $\frac{S}{W} = 1.5$and is displayed in Figure 55. Peak to peak jitter was computed for differential via transitions with spacing to width ratio $\frac{S}{W}$ of 1.5 ,2 ,3.3 and 4 and displayed in Table 2. The eye diagram for $\frac{S}{W}$ of 2.5 is also displayed in Figure 56.

It was found that there is a definite increase in the amount of peak to peak jitter in differential signaling due to via transitions. Jitter increases from approximately 0.64 psec to nearly 13.3 psec in the case where $\frac{S}{W}$ ratio is 4 as shown in Table 2. This trend is observed in differential signaling irrespective of the $\frac{S}{W}$ ratio.

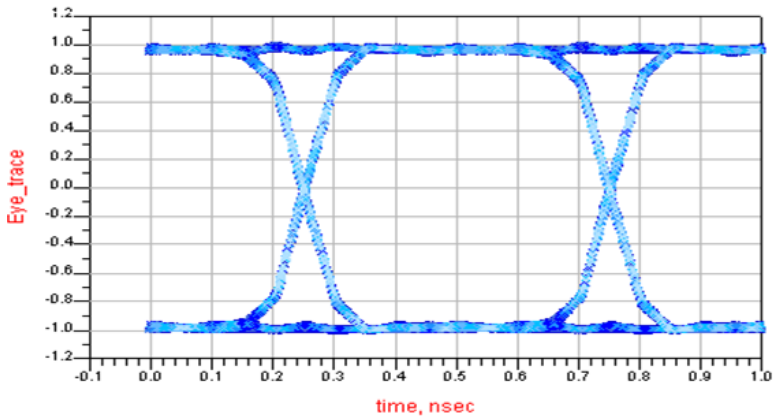

Figure 56. Eye diagram for differential via transition with spacing by width ratio $\frac{S}{W} = 2.5$.

It was also determined that increase in the $\frac{S}{W}$ ratio of differential via transitions does not correspondingly amplify jitter. Jitter increases from 11.09 psec to only 13.3 psec with a corresponding change in $\frac{S}{W}$ from 1.5 to 4. Thus it can be concluded that even in tightly coupled differential lines the effect of via transitions still can not be ignored or compensated by a reduction in edge-to-edge spacing.

In a bus of differential lines with via transitions every pair of lines could experience a jitter of greater than 11 psec. This is because, all these differential lines will switch in random patterns and the combined signal energy coupled to the PDN will be excessive. The corresponding SSN caused will be several multiples of SSN caused due to a pair of differential lines with via transitions. Increased SSN will only result in augmented jitter. Therefore, though jitter of 12 psec in a differential via transition pair may seem small in comparison to its 2 Gbps pulse width it will be non-negligible when considering jitter on a differential bus with via transitions.

3.2.4 Power supply noise or SSN

Signal energy coupled to the plane pair causes power supply noise or SSN due to displacement return currents. The presence of fluctuations in power supply due to via transitions was verified by performing simulations to determine the 2-D voltage distribution plots of the plane pair for differential via transition structure with $\frac{S}{W} = 1.5$. The voltage distribution

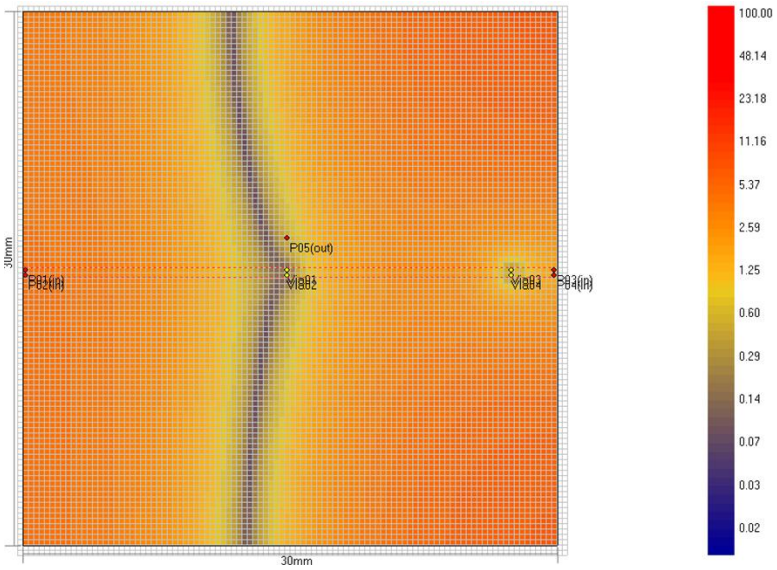

Figure 57. 2D Voltage distribution plot of power supply planes in differential via transition structure at 2.77 GHz simulated with Panswitch (MFDM solver) [5] [6].

plot was captured at 2.77 GHz and as shown in Figure 57 high voltage is produced on the reference power plane.

A comparison performed with the equivalent ideal differential line structure indicated that in the absence of via transitions no fluctuations were produced on the power/ground planes as illustrated in Figure 58.

Therefore, the V_{dd} rail in the equivalent model for the differential via transition was simulated to determine exact SSN produced due to switching circuits and signal to power coupling. Power supply for the equivalent model of differential via transition structure corresponds to V_{dd} and V_{ss} shown in Figure 45.

While simulating jitter and power supply noise care was taken to provide enough time delay in the driver circuit so that the frequency bandwidth truncation does not produce non-physical results. Thus a delay of about 2 nsec was provided to allow the initial switching of circuits to be gradual and avoid very high frequency components.

Figure 59 shows the fluctuation of the power supply around 1 V for the differential via transition structure with $\frac{S}{W} = 1.5$; thus peak to peak power supply noise is = $322mV$. Figure 60 indicates that this fluctuation happens only at switching ,that is, the edges of the

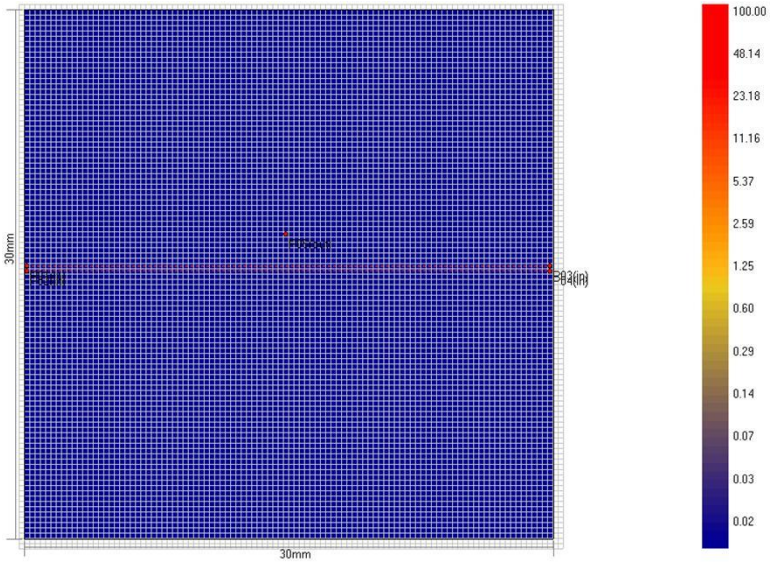

Figure 58. 2D Voltage distribution plot of power supply planes in ideal differential lines at 2.77 GHz simulated with Panswitch (MFDM solver) [5] [6].

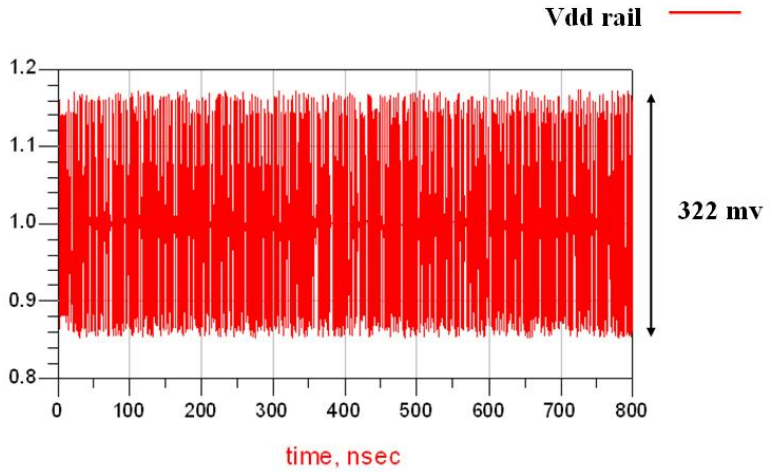

Figure 59. SSN for differential via transition with $\frac{S}{W} = 1.5$.

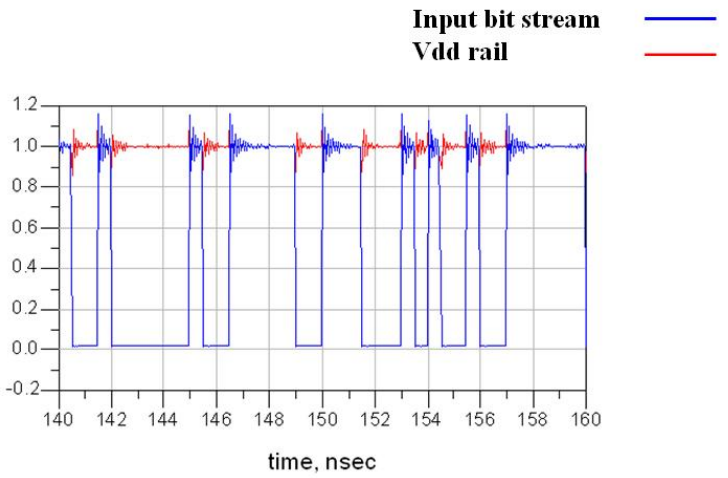

Figure 60. V_{dd} **and input voltage for differential via transition with** $\frac{S}{W} = 1.5$**.**

low to high and high to low transitions. However, because of the high data rates bounce on the V_{dd} is not allowed to settle down contributing to high jitter.

3.3 Jitter in Single Via Transitions

Comparison of the jitter in differential lines with via transitions and the equivalent single-ended model was performed. The model described in section 2.6.1 was used for time-domain simulations. Jitter was calculated to be 29.3 psec; this is nearly twice the jitter found in differential via transition structures as shown in Figure 61. Jitter in differential signaling happens to be lower due to partial common-mode cancelation.

Thus comparing single-ended and differential structures it can be concluded that - drop in signal to power coupling from -10 dB to -20 dB resulted in a corresponding decrease of jitter from 29.3 psec to 13.3 psec. Therefore increase in signal to power coupling causes a direct amplification of jitter.

Simulation of the 2-D voltage distribution plot for the single via transition model also verified the SSN produced due to signal to power coupling. Figure 62 illustrates the bounce on the power supply planes at 2.77 GHz due to the return displacement current. Therefore, the V_{dd} rail in the equivalent model for the single via transition was simulated to determine the exact amount of power noise produced.

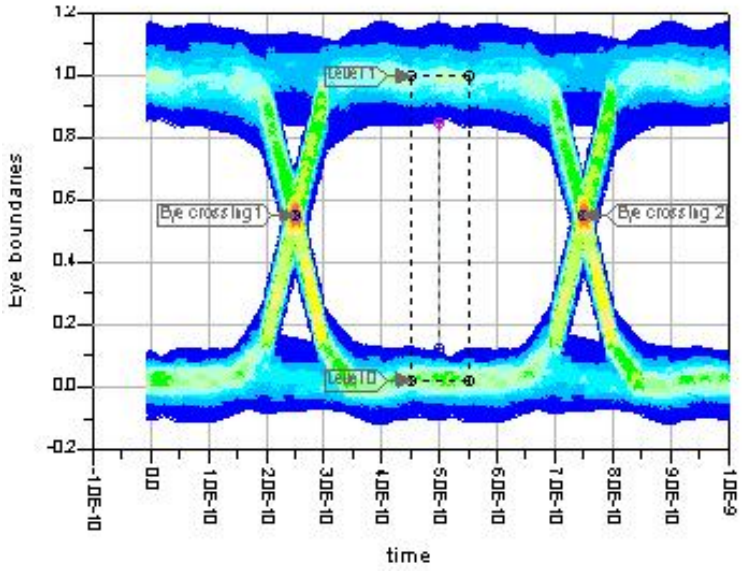

Figure 61. Eye diagram for single via transition .

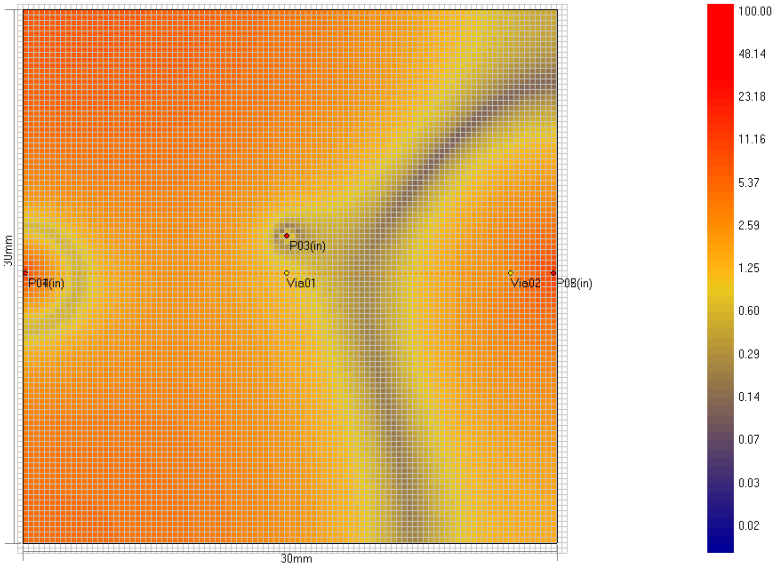

Figure 62. 2D Voltage distribution plot of power supply planes in single via transition structure at 2.77 GHz simulated with Panswitch (MFDM solver) .

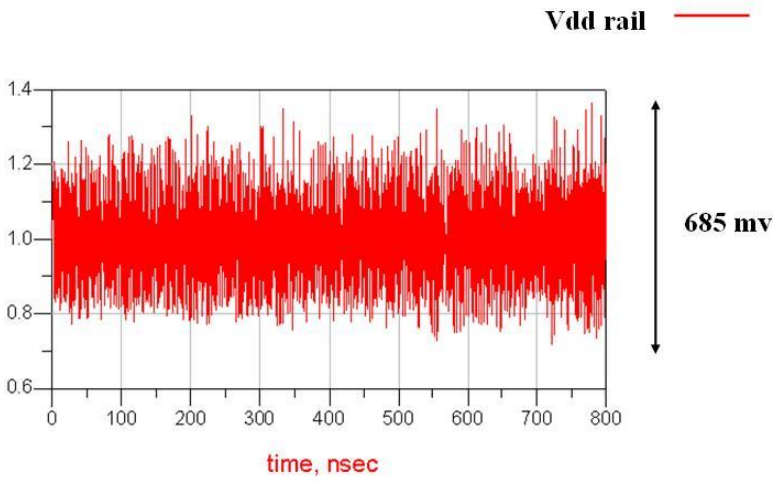

Figure 63. SSN for single via transition.

Table 3. Relation between signal to power coupling, SSN and jitter

	Signal to power Coupling	Simultaneous Switching Noise(SSN)	Jitter for 2 Gbps PRBS input
(a) Differential Transmission Line (with no via transitions) for Spacing by Width ratio $\frac{S}{W} = 4$	≈ -70 dB	Negligible	0.64 psec
(b) Differential Via Transition (with vias) for Spacing by Width ratio $\frac{S}{W} = 4$	≈ -30 dB	322 mV	13.30 psec
(c) Single Via Transition	≈ -12 dB	685 mV	29.30 psec

SSN found on the power rail V_{dd} also supports the theory that signal to power coupling causes SSN and in turn producing jitter. Power supply noise was found to be = $685mV$ as indicated in 63 and this is more than double the amount of jitter found in differential signaling (322 mV). Therefore as explained before increase of signal energy coupled to the PDN results in augmentation of SSN. And SSN causes jitter on traces referenced to planes in PDN.

Although noise effects in differential signaling are more subdued than that found in the single-ended scheme, jitter and SSN are significantly amplified when compared to differential lines with no irregularities. Thus differential signaling is not immune to the effects

of discontinuities.

Therefore, it can be concluded from simulations performed in the time domain that amplification of signal to power coupling from ideal differential lines to differential via transition results in a corresponding augmentation of SSN. Consequently, jitter also increases due to amplified signal to power coupling in differential via transition structure when compared to ideal differential traces. This trend is captured in table 3 which summarizes results from measurements and simulations. Therefore, signal to power coupling in differential signaling generates SSN and produces noise-induced jitter.

CHAPTER 4

CONCLUSION

Signal to power coupling was investigated to test the robustness of differential signaling in the presence of non-idealities. Model to hardware correlation proved that anomalies in differential signaling such as via transitions and asymmetry in differential vias couple significant energy to the power distribution network. This signal to power coupling was found to amplify in differential via transition structures with the increase of spacing by width ratio $\frac{S}{W}$ in differential lines.

Measurements indicated that differential vias must not be staggered by more than 0.2 mm; beyond this point energy coupling from signal lines to planes increased monumentally. Signal coupling from via stubs proved to be quite significant for the single-ended case but the coupling from differential stubs to the package PDN still remained at a minimal level at lower frequencies. The significance of energy loss in S-parameters of differential lines was also investigated in the time-domain.

Time-domain simulations performed on the comparable circuit model for differential via transition structure indicated an increase in peak to peak jitter in the presence of via transitions. This jitter was found to vary very little with spacing by width ratio $\frac{S}{W}$ of differential lines. However, jitter in differential via transitions was observed to be significantly more that the amount found in perfectly symmetrical differential lines as shown in table 2. Figure 64 underlines this fact and indicates that augmentation of jitter due to via discontinuity is consistent, irrespective of the coupling between differential traces.

Differential signaling was still found to be more robust than single-ended traces; Jitter in differential lines with via transitions was predictably half the value of jitter found in single-ended via transitions as verified in section 3.3.

The power noise fluctuations were also simulated in time-domain and correlated to the amount of jitter found. SSN due to differential via transitions caused a fluctuation in V_{dd}

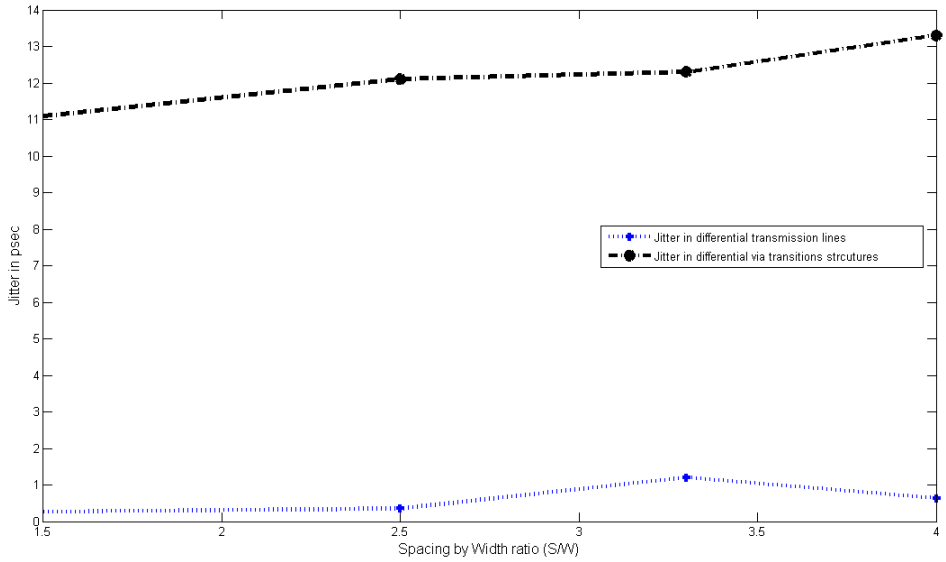

Figure 64. Increase in jitter due to via transitions

rail of about 322 mV. Therefore it was conclusively proven that signal to power coupling in differential signaling causes an amplification of power noise on planes in PDN. This augmentation of SSN coupled back to non-ideal differential lines causing increased signal integrity degradation on these lines.

However, both signal to power coupling and jitter induced by SSN was found to occur only on differential lines with discontinuities like via transitions. Ideal differential lines are still robust and resistant to common-mode noise. Experiments and simulations have been performed conclusively validate the above claims.

Therefore the effect of discontinuities and irregularities in differential signaling can not be underestimated at high frequencies. Such structures couple significant amount of signal energy to power planes causing increased power supply noise and signal integrity effects like jitter. Though the amount of jitter caused on a differential pair with irregularities is minimal it will prove to be non-negligible and critical when irregular differential bus structures are routed in packages and boards.

REFERENCES

[1] S. Kempainen, "Buslvds expands applications for low voltage differential signaling (LVDS)," in *DesignCon 2000*, National Semiconductors, 2003.

[2] V.Zwillich, M.Wollitzer, T.Wirschem, W.Menzel, and H.Leier, "Signal integrity analysis of a 1.5 gbit/s LVDS video link," in *IEEE International Symposium on Electromagnetic Compatibility*, pp. 1–6, July 2007.

[3] M. Swaminathan and A. E. Engin, *Power Integrity Modeling and Design for Semiconductors and Systems*. Prentice Hall, 2007.

[4] M. P. Li, *Jitter, Noise and Signal Integrity at High Speed*. Prentice Hall, 2007.

[5] K. Bharath, E.Engin, M.Swaminathan, K.Uriu, and T.Yamada, "Computationally efficient power integrity simulation for system-on-package applications," in *Design Automation Conference*, pp. 612–617, June 2007.

[6] A. Engin, K. Bharath, and M. Swaminathan, "Multilayered finite-difference method (MFDM) for modeling of package and printed circuit board planes," *IEEE Trans. on EMC*, vol. 49, no. 2, pp. 441–447, 2007.

[7] "International roadmap for semiconductors (ITRS) - 2007 update."

[8] "Advantech."

[9] K.Bharath, E.Engin, M.Swaminathan, K.Uriu, and T.Yamada, "Efficient simulation of power/ground planes for sip applications," in *Proc. of 57th IEEE ECTC*, pp. 1199–1205, June 2007.

[10] D. M. Pozar, *Microwave Engineering, 2nd Ed.* John Wiley and Sons, 1998.

[11] J.Lee, J.Kim, J.Kim, A.C.W.Lu, F.Wei, and L.L.Wei, "Efficiency of differential signaling on cavity noise suppression in applications with reference plane change," in *IEEE International Symposium on Electromagnetic Compatibility*, pp. 203–208, Aug. 2004.

[12] G.Shiue and R.Wu, "Reduction in reflections and ground bounce for signal lines through split power plane by using differential coupled microstrip lines," in *Proc. of 12th IEEE EPEP*, pp. 107– 110, Oct. 2003.

[13] E. Bogatin, *Signal Integrity - Simplified*. Prentice-Hall, 1993.

[14] H.Johnson and M.Graham, *High-Speed Digital Design: A Handbook of Black Magic*. Prentice-Hall, 1993.

[15] R. Garg and I. Bahl, "Characteristics of coupled microstriplines," *IEEE Trans. on Microwave Theory and Techniques*, vol. 32, pp. 83–89, January 1984.

[16] K. C. Gupta and R. Garg, *Microstrip Lines and Slotlines 2nd Ed.* Artech House, 1996.

[17] D. Bockelman and W. Eisenstadt, "Combined differential and common-mode scattering parameters: theory and simulation," *IEEE Trans. on Microwave Theory and Techniques*, vol. 43, pp. 1530–1539, July 1995.

[18] Agilent Technologies, *Agilent PNA-L Network Analyzer - Application Note*, Oct. 2006. Application Note.

[19] C.Wang and J.L.Drewniak, "Quantifying the effects on EMI and SI of source imbalances in differential signaling," in *IEEE International Symposium on Electromagnetic Compatibility*, pp. 865–868, Aug. 2003.

[20] C.Wang, J.Fan, J.L.Knighten, N.W.Smith, R.Alexander, and J.L.Drewniak, "The effects of via transitions on differential signals," in *Proc. of 10th IEEE EPEP*, pp. 39–42, Oct. 2001.

[21] P.E.Fornberg, M. Kanda, C.Lasek, M.Piket-May, and S. Hall, "The impact of a non-ideal return path on differential signal integrity," *IEEE-Trans- EMC*, vol. 44, pp. 11–15, November 2002.

[22] D. Herrell and B. Beker, "Modeling of power distribution systems in pcs," in *Proc. of 7th IEEE EPEP*, pp. 159–162, Oct. 1998.

[23] L. Smith, "Simultaneous switch noise and power plane bounce for CMOS technology," in *Proc. of 8th IEEE EPEP*, pp. 163–166, Oct. 1999.

[24] N. Na, J. S.Chun, M.Swaminathan, and J. Srinivasan, "Modeling and transient simulation of planes in electronic packages," *IEEE Trans. on Adv. Pakag.*, vol. 23, pp. 340–352, Aug 2000.

[25] P.Muthana, K.Srinivasan, E.Engin, M.Swaminathan, R.Tummala, D.Amey, K.Dietz, and S.Banerji, "I/O decoupling in high speed packages using embedded planar capacitors," in *Proc. of 57th IEEE ECTC*, pp. 299–304, May. 2007.

[26] J.Patrin and M.Li, "Comparison and correlation of signal integrity measurement techniques," in *DesignCon*, 2002.

[27] "Agilent advanced design system (ADS)."

[28] "Mixed signal design tools 1 - power ground network simulator and optimizer."

[29] C.R.Paul, *Analysis of Multiconductor Transmission Lines*. Wiley, 1994.

[30] L. M. Wedepohl, "Application of matrix methods to the solution of travelling-wave phenomena in polyphase systems," in *Proc.IEEE*, pp. 2200–2212, Dec. 1963.

[31] A.E.Engin, M.Coenen, H.Koehne, G.Sommer, and W.John, "Modeling and analysis of the return path discontinuity caused by vias using the 3-conductor model," in *Proc. of IEEE EMC Symposium*, pp. 1110–1113, May 2003.

[32] E.Hammerstad and O.Jensen, "Accurate models for microstrip computer-aided design," in *MTT Symposium Digest*, 1980.

[33] S.Hall, G.Hall, and J.McCall, *High-Speed Digital System Design : A Handbook of Interconnect Theory and Design Practices*. John Wiley and Sons, 2000.

[34] B. Young, *Digital Signal Integrity - Modeling and Simulation with Interconnects and Packages*. Prentice Hall, 1993.