ELECTROMAGNETIC BAND GAP (EBG) SYNTHESIS AND ITS APPLICATION IN ANALOG-TO-DIGITAL CONVERTER LOAD BOARDS

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ELECTROMAGNETIC BAND GAP (EBG) SYNTHESIS AND ITS APPLICATION IN ANALOG-TO-DIGITAL CONVERTER LOAD BOARDS

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Dedicated to my family

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SUMMARY

With increase in frequency and convergence toward mixed signal systems, supplying stable voltages to integrated circuits and blocking noise coupling in the systems are major problems. Electromagnetic band gap (EBG) structures have been in the limelight for power/ground noise isolation in mixed signal applications due to their capability to suppress unwanted electromagnetic mode transmission in certain frequency bands. The EBG structures have proven effective in isolating the power/ground noise in systems that use a common power supply. However, while the EBG structures have the potential to present many advantages in noise suppression applications, there is no method in the prior art that enables reliable and efficient synthesis of these EBG structures.

Therefore, in this research, a novel EBG synthesis method for mixed signal applications is presented. For one-dimensional periodic structures, three new approaches such as current path approximation method, border to border radius, power loss method have been introduced and combined for synthesis. For two-dimensional EBG structures, a novel EBG synthesis method using genetic algorithm (GA) has been presented. In this method, genetic algorithm (GA) is utilized as a solution-searching technique. Synthesis procedure has been automated by combining GA with multilayer finite-difference method and dispersion diagram analysis method. As a real application for EBG structures, EBG structures have been applied to a GHz ADC load board design for power/ground noise suppression.

CHAPTER 1

INTRODUCTION

With increasing clock speed and decreasing supply voltages in today's mixed signal applications, the design of power distribution networks (PDN) is becoming an increasingly difficult challenge for modern technologies. The PDN needs to provide stable and uniform voltages for all devices, and should not cause noise coupling between the devices. However, for high-speed systems, power/ground pairs in the PDN form resonators. As a result, when the power/ground plane resonances are excited, the power/ground noise can be significantly large [1], [2]. The noise can produce false switching in digital circuits and malfunctioning in analog circuits.

There has been significant research effort to isolate the sensitive RF/analog circuits from power/ground noise generated by the digital circuits. Traditional isolation methods have used split power and ground planes [3], [4] and ferrite beads [5]. However, the split power and ground planes cannot be used for a system requiring a common power supply. Although split planes with ferrite bead filters can be used with a common power supply, such filters cannot be used at high frequencies because of the parasitics of the ferrite beads.

As an alternative power/ground noise suppression technique, electromagnetic band gap (EBG) structures have been recently introduced [6]-[9]. EBG structures are periodic structures in which the propagation of electromagnetic waves is forbidden in certain frequency bands. In these EBG structures, the constructive and destructive interference of electromagnetic waves results in passband and stopband characteristics. EBG structures also make it possible to use a common power supply. Therefore, in recent years, EBG structures have become very attractive for high-speed mixed signal system design and integration.

The applications of EBG structures are not limited to mixed signal applications. EBG structures have become a very important part for antenna applications and filter applications, as well. EBG structures can be used to miniaturize microstrip type planar antenna using the periodicity concept. It is also possible to enhance the performance of planar antennas by improving their impedance as well as radiation pattern characteristics using EBG structures [10]-[14]. For filter applications, in addition to size miniaturization, high isolation relative to other planar filters can be achieved since substrate noise is eliminated using the properties of EBG structures [15].

However, in spite of the fact that EBG structures have become important for power/ground noise management in mixed signal applications, antenna applications, and filter applications, there has been little work done for the synthesis of EBG structures based on specifications. All of the papers in this area have relied on an ad-hoc approach whereby a design is analyzed based on its electromagnetic response and then modified if the structure did not meet the specification.

In this research, a novel EBG synthesis method is presented. As a real application, EBG techniques are applied to a GHz ADC load board design to isolate power/ground noise coupling from digital circuits to analog circuits. The major contributions of this research can be summarized as follows:

1) Three new approaches have been proposed namely, current path approximation method, border to border radius, and power loss method for one-dimensional electromagnetic band gap synthesis for mixed signal applications;

2) Development of a novel one-dimensional (1-D) and two-dimensional (2-D) EBG synthesis method using genetic algorithm for efficiently and effectively synthesizing EBG structures for mixed signal applications;

3) Development of a method to automatically synthesize EBG structures;

4) Development of a method to automatically determine when the synthesis of an EBG structure with a particular set of design specifications is not possible;

5) Finally, suggesting a methodology for reducing power/ground noise on a high-speed and high-resolution analog-to-digital converter (ADC) load board using EBG techniques.

1.1 Technology Trend

Over a long period in the past, the performance of digital semiconductor systems followed Moore's Law, which states that the number of transistors on a chip doubles about every two years, as shown in Figure 1.1.

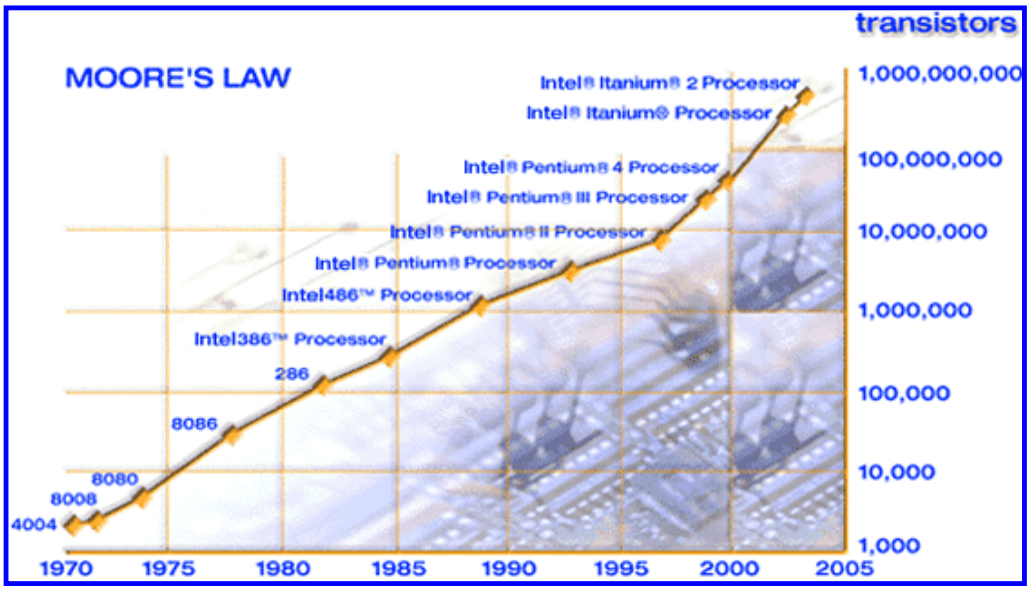


Figure 1.1: Moore's Law states that the number of transistors on a chip doubles about every two years: Courtesy of Intel.

While the functionality and speed of all kinds of devices are increasing, size and weight have to be reduced. This has created a major design challenge for the reliable and efficient distribution of power in high performance digital systems. The cause for this design challenge is that the increasing frequencies and miniaturization of power distribution network require analysis of various parasitic effects that could be ignored in the past. Finally, with increasing speeds and decreasing supply voltages in the devices, the design of power distribution networks (PDNs) is becoming an increasingly difficult challenge for modern technologies.

1.2 Power Distribution Network (PDN)

A power distribution network (PDN) is designed to provide stable and uniform voltages for all devices. It is very important that the power level be kept uniform across the board because fluctuations in reference and/or supply voltages will significantly affect the performance of individual components. Figure 1.2 shows a typical power distribution network. The PDN consists of cables, backplanes, and PC boards to several integrated circuit packages. Each package supplies power to one or more chips. Power is supplied to circuits on each chip through a hierarchy of distribution networks.

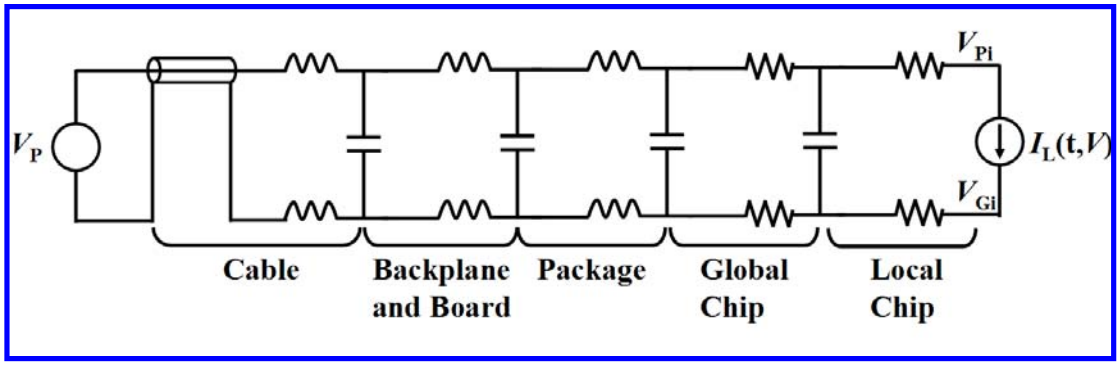


Figure 1.2: A typical power distribution network.

If the components were connected directly to the power supply or the voltage regulator module (VRM), there would be no need to worry about system-wide power delivery. However, as shown in Figure 1.2, unfortunately, the supply and ground are distributed over a network with inductive and resistive components. Subsequently, when numerous gates switch simultaneously on several different components, the inductance and resistance of the network will exhibit high-impedance characteristics and will generate undesired voltage fluctuation, called simultaneous switching noise (SSN), on the PDN because the high-impedance characteristics meet the switching current. Therefore, for a superior design of the power distribution network, the impedance of the

power/ground planes should be designed to be as low as possible over the entire bandwidth of the signal.

One method of specifying a power distribution system is in terms of target impedance [16], which is the maximum allowed impedance for the system to meet a specified noise level.

For example, consider a component operating at a voltage V_{DD} and dissipating an average of P watts. The average current is $I_{avg} = P / V_{DD}$. Assuming that the allowed ripple on the power supply is $V_{ripple} = xV_{DD,}$ where typical values for x are 5% to 10%, then the target impedance is

$$Z_{Target} = \frac{V_{ripple}}{I_{avg}}. \tag{1.1}$$

Finally, the power distribution system should be designed so that the impedance looking into the system at the site of the component is less than the target impedance over a specified bandwidth. The definition of target impedance is sketched in Figure 1.3.

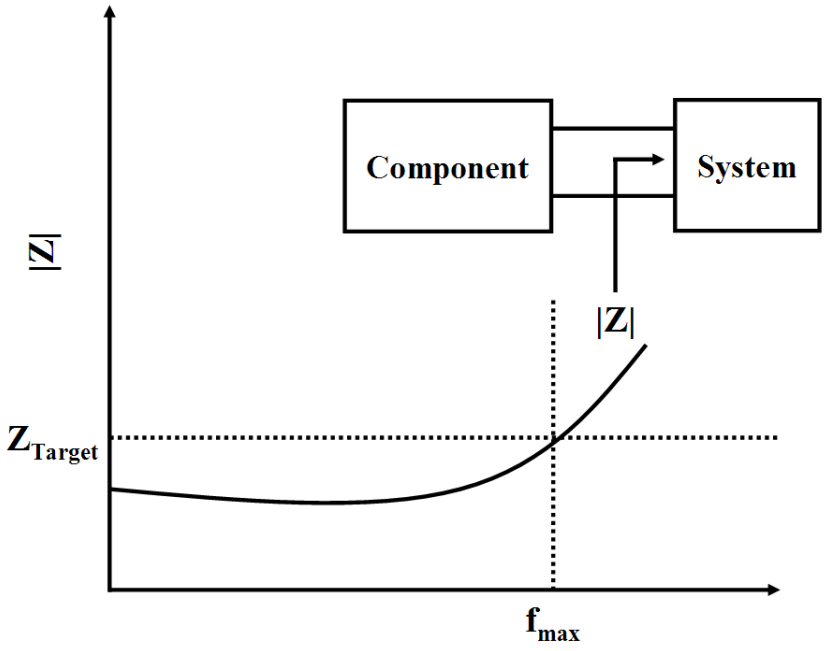


Figure 1.3: Target impedance sets the maximum impedance magnitude of the power distribution network as seen from the position of a component [17].

1.3 Simultaneous Switching Noise (SSN) Issue

Simultaneous switching noise (SSN) refers to noise generated in a digital system because of rapid changes in voltage and current caused by many circuits switching at the same time [17]. It is also known as delta-I noise since it results from the rate of change of current across the power distribution network inductance.

SSN is typically very difficult to quantify because it depends heavily on the physical geometry of the system. The basic mechanism, however, is the familiar equation

$$V_{SSN} = NL_{tot}\frac{di}{dt}, \tag{1.2}$$

where V_{SSN} is the simultaneous switching noise, N the number of drivers switching, L_{tot} the equivalent inductance in which current must pass, and di/dt the switching current per driver. When a large number of signals switch at the same time, the power supply must deliver enough current to satisfy the sudden demand. Since the current must pass through an inductance, L_{tot}, a noise of V_{SSN} will be introduced onto the power supply.

SSN can occur at both the chip level and the board level. At the chip level, the power supply is not perfect. Any sudden demand for current must be supplied by the board-level power through the inductive chip package and lead frame (or other interconnection technologies). On the board level, sudden current demands must be supplied through inductive connectors.

Therefore, for both cases, to reduce effective path inductance of power distribution network (PDN) is very important to reduce SSN because controlling the driver's slew rate (di/dt) will result in driver slowdown so that it is not a proper solution.

There have been many efforts to suppress SSN. A well-known method to suppress SSN is to mount decoupling capacitors on the board, package, and chip. The idea behind decoupling capacitors is not only to provide reduced path impedance for power supply, but also to supply current bursts for fast switching circuits [18]-[21]. However, it has

been found that the parasitic inductance of the decoupling capacitors can actually worsen the impedance of the power delivery [22].

Figure 1.4 shows the equivalent circuit model for a realistic capacitor. Decoupling capacitors can be represented by equivalent R, L, and C circuits as shown in Figure 1.4. The parasitic parameters R and L are known as the equivalent series resistance (ESR) and the equivalent series inductance (ESL). The self-resonant frequency of a decoupling capacitor is a function of its capacitance and ESL and given by the equation

$$f_r = \frac{1}{2\pi\sqrt{C \times ESL}}. \tag{1.3}$$

Because decoupling capacitors are not purely capacitors above the resonant frequency, decoupling capacitors show an inductive behavior, as shown in Figure 1.5.

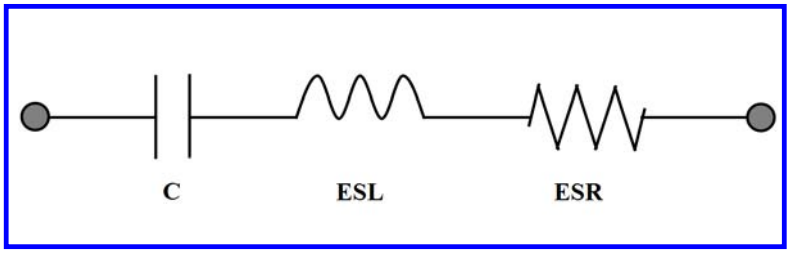


Figure 1.4: Equivalent circuit model of a real decoupling capacitor.

Because of this kind of characteristic of the decoupling capacitors, different kinds of decoupling capacitors should be used over the wide frequency range, depending on the structure and noise frequencies. Based on the resonant frequency, the decoupling capacitors can be categorized into low-frequency, mid-frequency, and high-frequency capacitors. Typically, low-frequency and mid-frequency decoupling capacitors are mounted on the package and board, and high-frequency decoupling capacitors are buried. However, it is almost impossible to lower the impedance of the PDN at frequencies greater than 1 GHz using decoupling capacitors since the parasitic inductance of the decoupling capacitor is dominant at high frequencies.

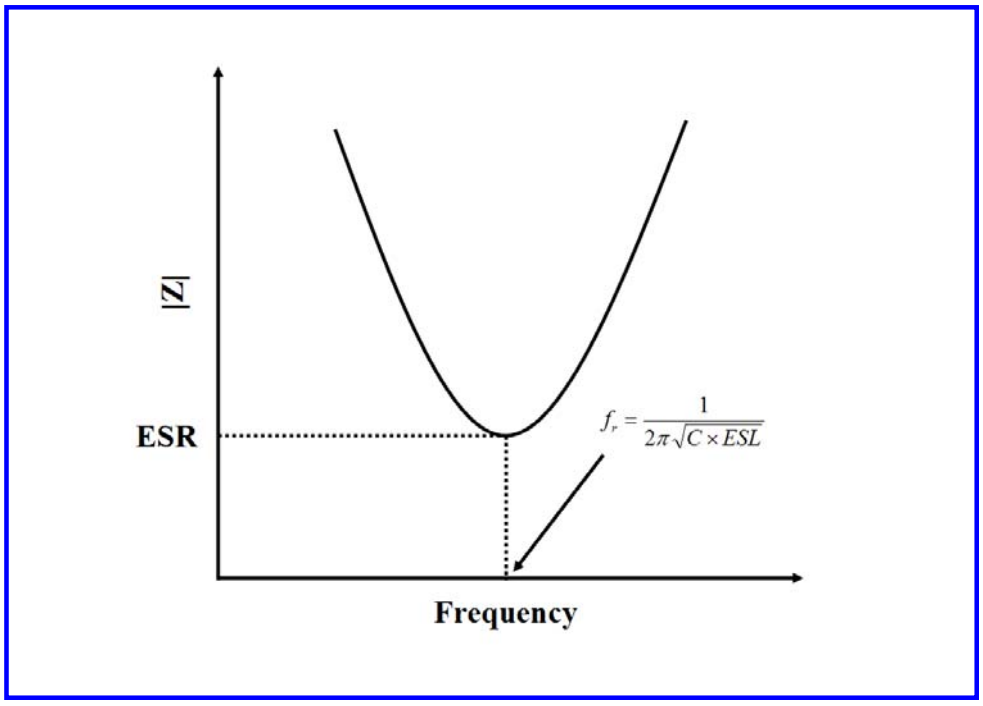


Figure 1.5: Frequency response of a decoupling capacitor.

1.4 Noise Coupling Issue in Mixed Signal Applications

With the evolution in system integration technologies, heterogeneous functions such as high-speed digital processors, radio-frequency (RF) circuits, microelectromechanical systems (MEMS), memory, analog devices, and optoelectronic devices have been integrated into a system. This integration is required for convergent microsystems that support communication and computing capabilities in a tightly integrated module. A major bottleneck faced by such heterogeneous integration is supplying clean power to the integrated circuits and managing the noise coupling in the system [23].

Figure 1.6 shows the noise generation and coupling in mixed-signal systems. When aggressor circuits (digital circuits) operate, they need a certain amount of switching current ($\triangle i_{aggressor}$). When the switching current meets power/ground impedance, Z_{11} at the location of the digital circuits, it will generate voltage fluctuation (

$\triangle V_{aggressor}$). The generated noise (voltage fluctuation) will couple to victims such as RF and analog chips through S_{21} characteristic of the power and ground planes [24]. The coupled noise will destroy the functionality of those sensitive circuits. Therefore, it is very important to keep Z_{11} and S_{21} as low as possible.

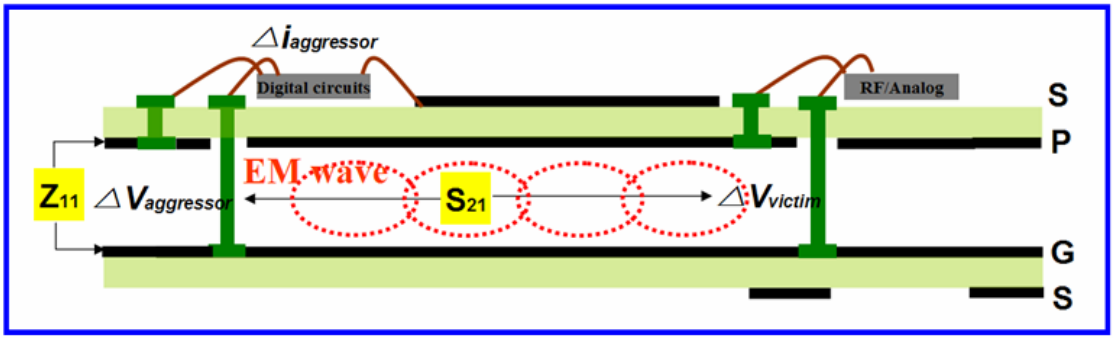


Figure 1.6: Noise generation and coupling in mixed signal systems.

1.5 Conventional Noise Isolation Techniques

There have been many research efforts to isolate sensitive RF/analog circuits from the power/ground noise generated by the digital circuits in high-speed mixed signal systems where digital and RF/analog circuits coexist. Noise isolation techniques used in the prior art can be summarized as follows:

1) Split power and ground planes [3], [4]

The slots in power/ground planes can partially block the propagation of power/ground noise. However, a portion of the electromagnetic energy can still couple through the slot depending on the slot width at high frequencies. Because of that, this method typically provides marginal isolation (i.e., -20dB to -60dB) at high frequencies above 1GHz. In addition, the split power and ground planes can not be used for a system requiring a single power supply. As systems become

more complex, multiple power supplies become a luxury designers cannot afford. Figure 1.7 shows split power planes in a real application.

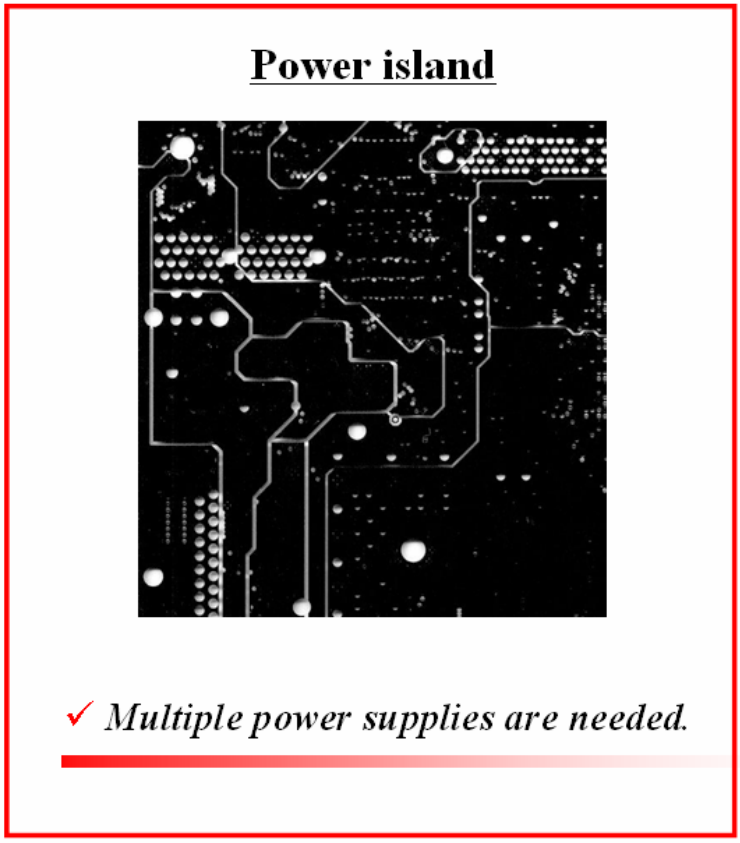


Figure 1.7: A photo of split power planes.

2) Ferrite beads [5]

An alternative technique used in the prior art for systems requiring a common DC power supply is to use split planes and ferrite beads. Real ferrite bead filters are shown in Figure 1.8. Ferrite beads act as high impedance to high frequency electromagnetic interference (EMI) noise. The absorbed energy is converted to heat, and dissipated by the ferrite. Ferrite bead filters can be used in mixed signal applications using a common power supply for isolating noise coupling from digital circuits to RF/analog circuits. However, ferrite beads are not effective at high frequencies due to parasitics.

Figure 1.8: A photo of real ferrite bead filters.

1.6 Electromagnetic Band Gap (EBG) Structures

An alternative noise suppression technique to prior art techniques such as split planes and ferrite beads involves the use of band gap structures.

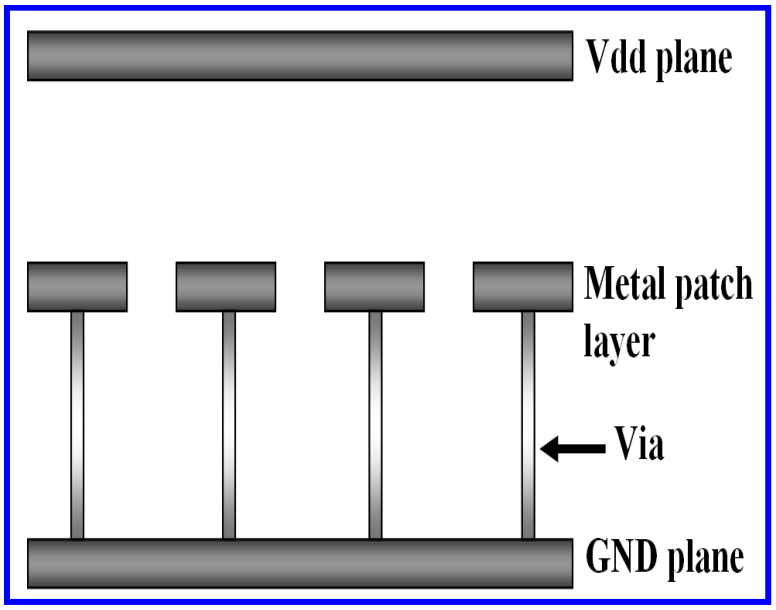
Electromagnetic band gap structures have become very popular due to their capabilities to suppress unwanted electromagnetic transmission and radiation in the area of microwave and millimeter waves [25]-[27]. Electromagnetic band gap structures are periodic structures in which the propagation of electromagnetic waves is restricted in a specified frequency band. As these structures allow only certain frequencies to propagate, they act like filters [28]. Consequently, these structures have passband and stopband characteristics. The passband and stopband characteristics depend on the shape and size

of the structures. The stopband characteristics of the EBG structures can be used in mixed signal applications to isolate noise coupling.

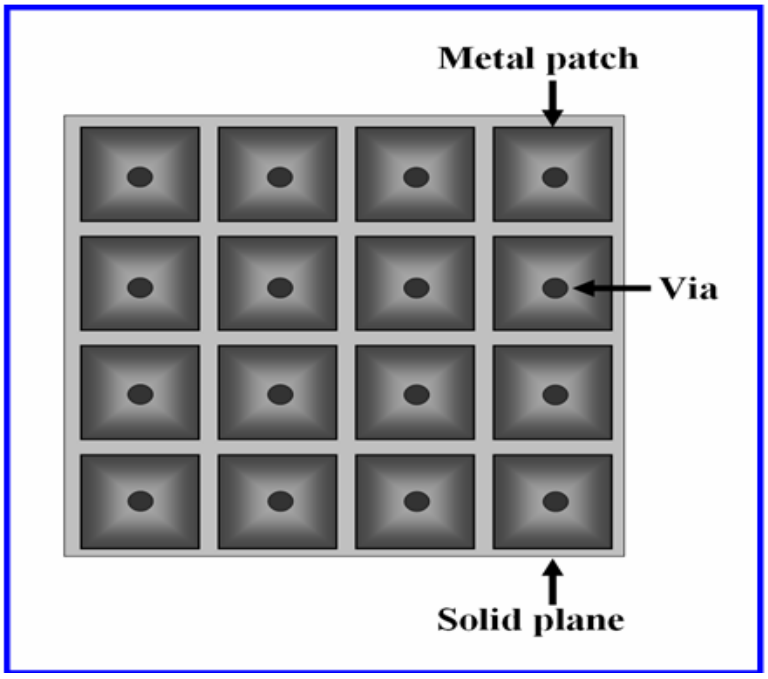
In the last few years, mushroom-type EBG structures were proposed for simultaneous switching noise (SSN) reduction in high-speed digital systems [6], [7], [22], but the mushroom-type EBG structures require buried vias, additional metal layers, and very thick dielectric layers (60 mils ~ 180 mils), which represent an expensive solution for most applications. Figure 1.9 shows the cross-section and top view of the mushroom-type EBG structure.

Recently, many new EBG structures have been suggested [29]-[33]. The EBG structures consist of two metal layers separated by a thin dielectric material. While one metal layer is a solid plane, the other metal layer has a periodic pattern. In addition, the EBG structures require no additional vias and layers, which are necessary for the mushroom-type EBG structures. Therefore, standard printed circuit board fabrication technique is easily applicable, which is a cost-effective solution. Figure 1.10 and 1.11 show the schematic of AI-EBG structure [29] and other unit cell structures for two-layered EBG structures suggested in [30]-[33], respectively.

In addition to noise suppression in mixed signal applications, electromagnetic band gap structures can be used in a variety of applications. For example, electromagnetic band gap structures can enhance the performance of planar antennas by placing an electromagnetic band gap shield structure in close proximity to a microstrip patch. The inclusion of the electromagnetic band gap structure close to a microstrip patch can improve the front to backward radiation ratio of the antenna. Additionally, an electromagnetic band gap structure can be incorporated as the ground plane for a rectangular microstrip antenna for enhanced performance. In filter applications, electromagnetic band gap substrates can be incorporated to achieve greater isolation.



(a)



(b)

Figure 1.9: (a) Cross-section of the mushroom-type EBG structure and (b) Top view of the GND plane in (a) [26].

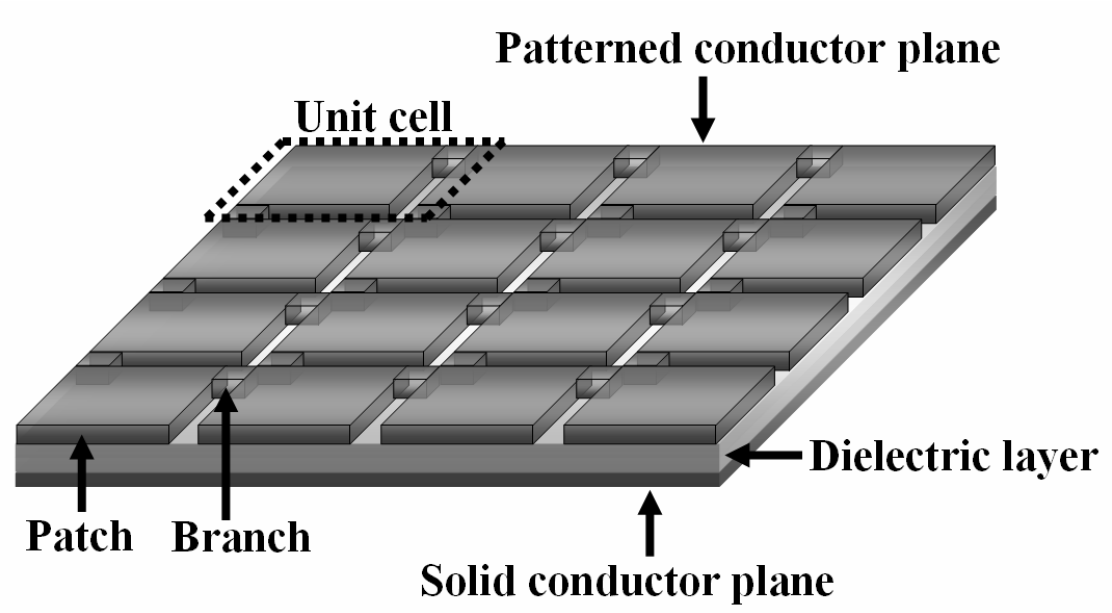


Figure 1.10: Schematic of alternating impedance electromagnetic band gap (AI-EBG) structure [29].

Figure 1.11: Examples of two-layered EBG unit cells: (a) EBG with slits, (b) UC-PBG, and (c) L-bridged EBG (refer to Figure 1.10 for the definition of a unit cell).

However, despite the potential benefits of electromagnetic band gap structures, conventional implementation of these structures is costly and prohibitive. More particularly, the most popular method of electromagnetic band gap structure design in the prior art involves a manual process that is time consuming, computationally expensive, and unreliable. Therefore, in this research, a novel EBG synthesis method is presented for mixed signal applications.

1.7 Effects of Electromagnetic Band Gap (EBG) Structures

Electromagnetic band gap (EBG) structures can be used as an effective solution for reducing the noise propagation. Since EBG structures can provide isolation in a specific frequency range according to its structure and periodicity, they are effective in reducing the noise coupling through the power/ground planes. However, since in recent high-speed and high-density digital systems, numerous functional blocks have been integrated in a single system, various noise sources can be created through the power/ground distribution plane. The noise sources could be a periodic pattern such as the waveforms generated by a clock signal or random noise patterns generated by non-periodic circuit patterns. Therefore, it is very important to verify the effect of EBG structures under two different noise source environments.

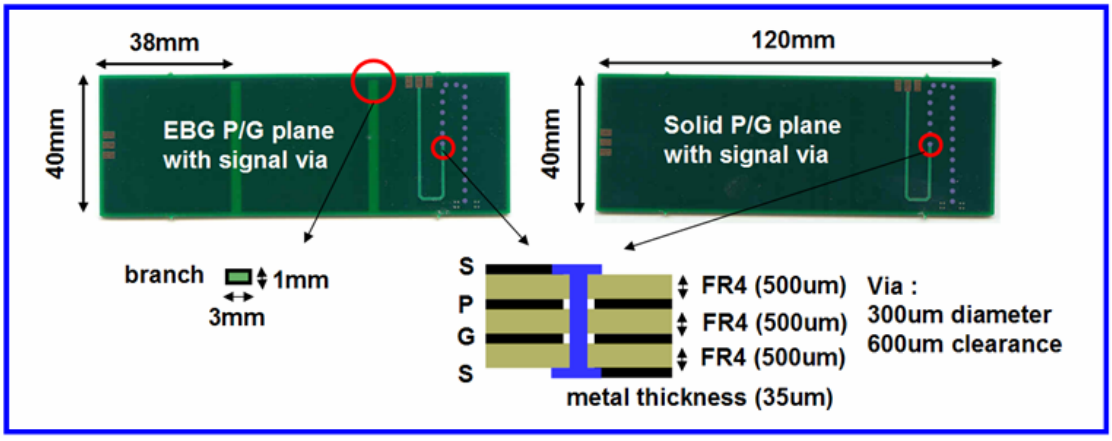
In this Section, the effect of EBG structures under two different noise source environments are investigated and analyzed. One is a periodic noise source environment and the other is a random noise source environment. In both cases, a signal transition via structure is used as a victim of the noise sources. When a signal experiences multiple reference planes by changing its layers through a signal via structure, the signal quality is degraded by the power/ground noise which is propagated from a noise source and coupled to the via structure [44]. For the investigation of the effect of EBG structures under two different noise source environments, one-dimensional EBG structure (1D-EBG) is implemented using a single layer with the combination of patches and branches which show small and big impedance characteristic respectively.

1.7.1 Implementation of EBG Structure and Measurement Setup

Two different types of test vehicles have been implemented to investigate the effect of EBG structures for reducing noise. In both cases, a signal transition via structure is used as a victim of the noise sources. When a signal experiences multiple reference

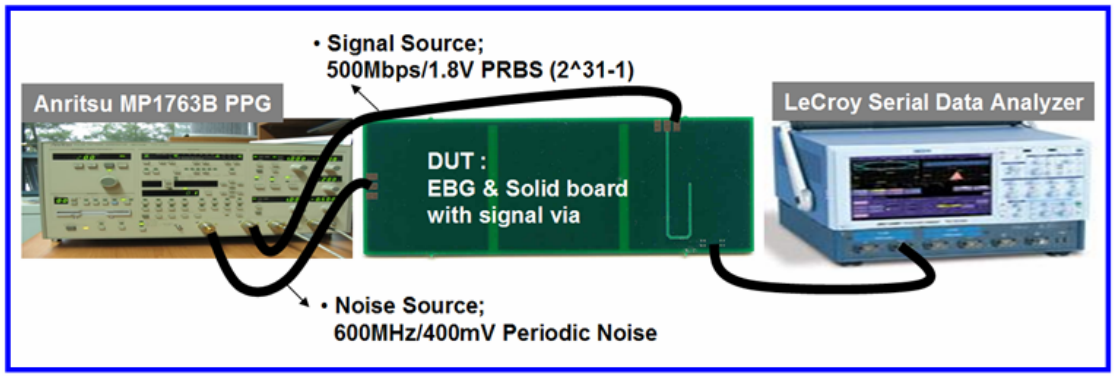
planes by changing its layers through a signal via structure, the signal quality is degraded by the switching noise which is propagated from a noise source and coupled to the via structure. For these tests, one-dimensional EBG (1D-EBG) structure has been applied to implement the isolation characteristic between the noise source and the victim that is a signal via structure. Figure 1.12 shows fabricated devices for measurements and measurement set-up. As shown in Figure 1.12(a), the devices have a 4-layer stack-up, and the signal starts from the top-layer and arrives to the bottom layer through one via structure in the middle of the signal path. The only difference between the test vehicles is on the second layer of the stack-up. One has 1D-EBG pattern consisting of 3 unit cells in the second layer as a power plane, and the other test vehicle has a solid plane instead of the EBG pattern. Figure 1.12(b) shows the measurement set-up. The noise source is located at the far edge from the via as shown in Figure 1.12(b).

The 1D-EBG structure in Figure 1.12(a) has been designed to have the band gap frequency from 600 MHz to 1.8 GHz. Figure 1.13 shows both the simulation result and the measurement result of the 1D-EBG structure. Both of them are well matched and show the band gap frequency between 600 MHz and 1.8 GHz with a -70dB isolation level.



(a)

Figure 1.12: Devices under test and measurement set-up: (a) 1D-EBG structure implemented as a power plane under the signal line with a single via at the middle of the signal path and a solid plane (b) measurement set-up to investigate clock jitter and data eye.



(b)

Figure 1.12: Continued.

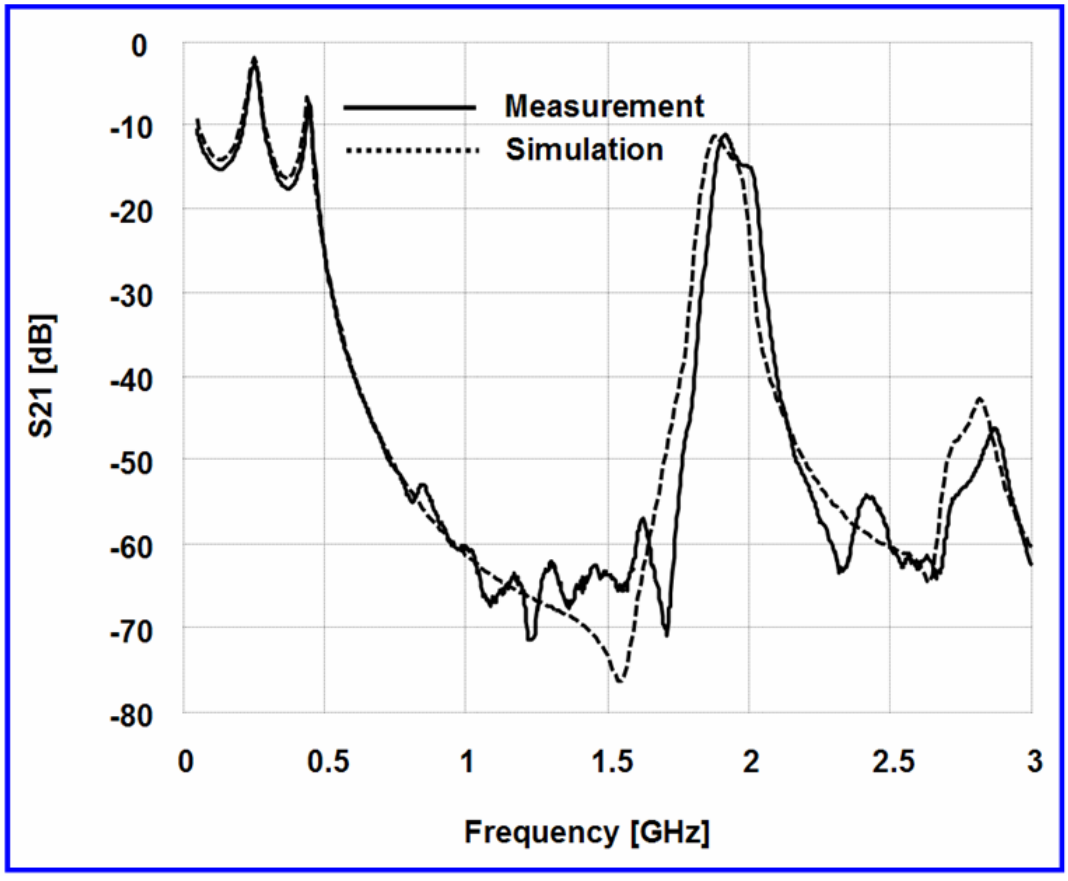
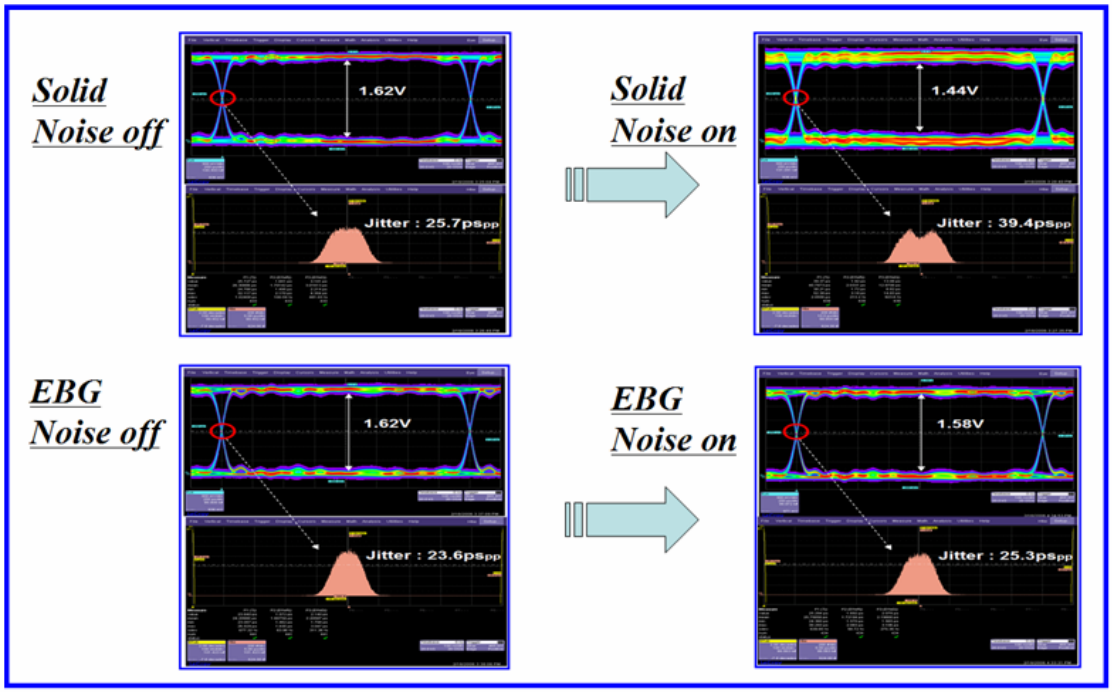


Figure 1.13: Simulation and measurement results of 1D-EBG structure in Figure 1.12.

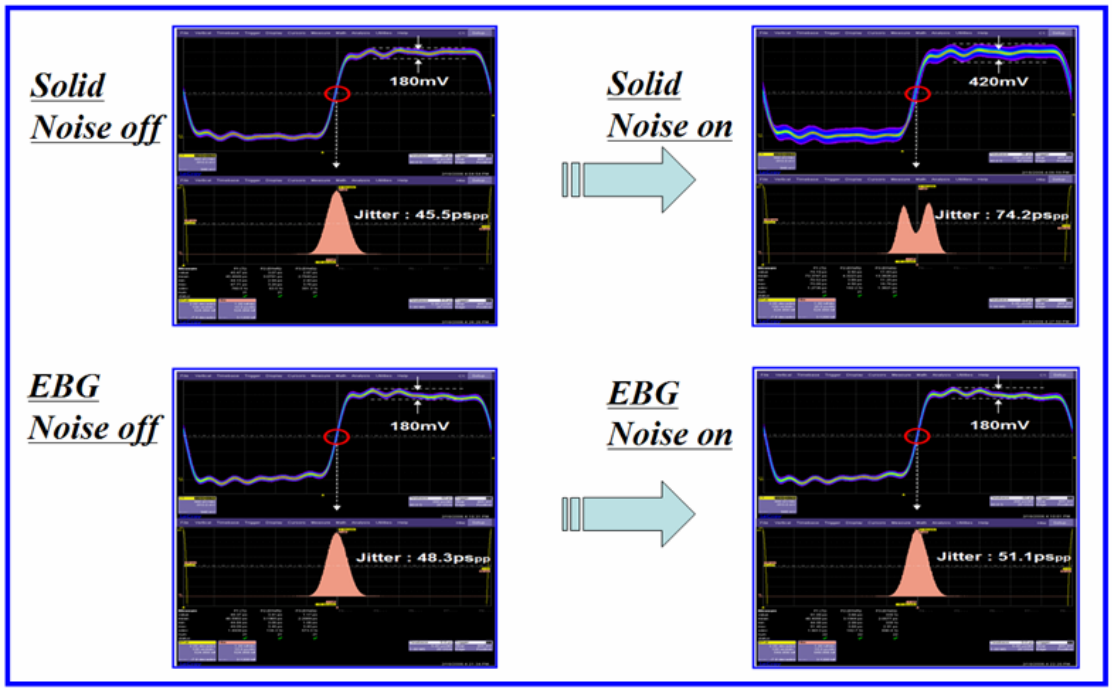
1.7.2 Effect of EBG Structure in Periodic and Random Noise Source Environments

Figure 1.14 shows the measurement results for a periodic noise. The noise source used in this experiment is periodic and has a 600MHz fundamental frequency so that the EBG structure can mitigate up to the 3rd harmonic frequency of the noise signal. As shown in Figure 1.14(a), a 500Mbps data signal on the EBG board guarantees 1.58V eye opening with 25.3ps timing jitter, while a general solid board deteriorates the eye opening and the timing jitter into 1.44V and 39.4ps respectively. Similar results can be acquired by investigating the clock signal as shown in Figure 1.14(b). A 500MHz clock signal running on the EBG board generates 180mV voltage noise and 51.1ps timing jitter by a single via transition at the middle of the signal path, while the same clock signal running on a general solid board generates 420mV voltage noise and 74.2ps timing jitter. These results indicate that the EBG structure is effectively able to prevent the switching noise from coupling into the via structure.

The results in Figure 1.14 have been acquired from the case of a periodic noise, which means the noise signal is assumed to be generated by periodic operation such as clock signaling. However, the noise source could have a random pattern generated by random operation. In that case, the effect of the EBG structure is different. As shown in Figure 1.15, a 500MHz clock signal running on the EBG power plane has worse timing margin than that of the same clock signal on a general solid power plane. Similar results are investigated in eye diagram in Figure 1.16. The eye opening of the 500Mbps data signal on the EBG power plane shows smaller eye opening and more timing jitter than the case of a solid power plane. These results indicate that the EBG structure should be carefully implemented in random noise environments.



(a)



(b)

Figure 1.14: Effect of the EBG structure on periodic noise: (a) measurement of 500Mbps 1.8V data signal under 600MHz 400mV periodic noise. Bigger eye opening and less jitter were achieved by the EBG structure (b) measurement of 500MHz 1.8V clock signal under 600MHz 400mV periodic noise. Less voltage fluctuation and less jitter were achieved by the EBG structure.

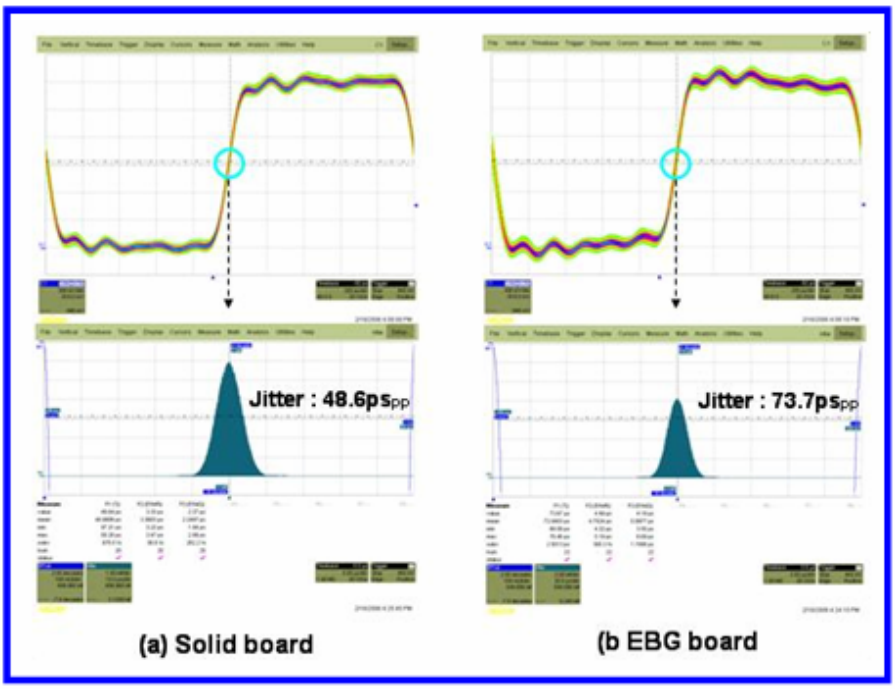


Figure 1.15: Effect of the EBG structure on random noise: measurement of 500MHz 1.8V clock signal under 600MHz 400mV random noise for (a) solid board and (b) EBG board.

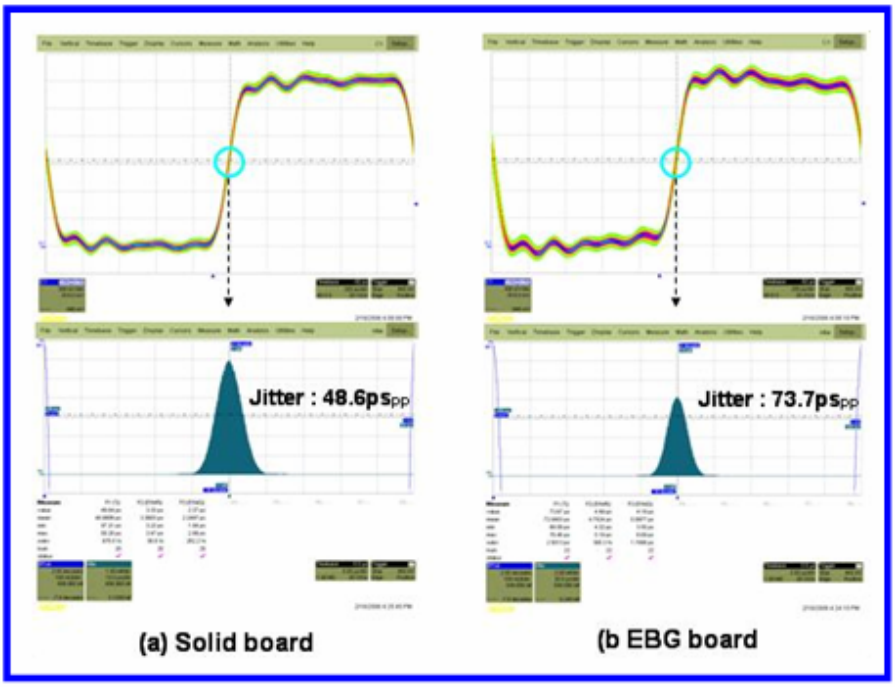


Figure 1.16: Effect of the EBG structure on random noise: measurement of 500Mbps 1.8V data signal under 600MHz 400mV random noise for (a) solid board and (b) EBG board. Smaller eye opening and more jitter were observed for the EBG structure.

1.7.3 Analysis of the Effects of EBG Structure in Periodic and Random Noises

The reason, why the same EBG structure shows different results for the periodic noise and the random noise, is analyzed by investigating noise spectrums and transfer characteristics. The frequency spectrum of the periodic noise used in the experiment of Figure 1.14 is well confined within the band gap of the 1D-EBG implemented as a power plane as shown in Figure 1.17. However, the frequency spectrum of the random noise applied to the experiment in Figure 1.15 and Figure 1.16 has a widely spread form starting from a dc range as shown in Figure 1.18. Although the EBG structure can provide deep isolation in a specific frequency range, the random noise spectrum cannot be confined within the band gap due to the wide spreading characteristic. Especially, in a low frequency range, a general solid power plane surpassed the EBG power plane from the view point of a noise transfer characteristic as shown in Figure 1.19. Since the most energy of the random noise spectrum is distributed within a low frequency range below 500MHz, the EBG could not mitigate the switching noise efficiently with the band gap implemented above 600MHz. Finally, since the frequency components of random noise is unknown, it is impossible to make the EBG work for all random patterns. However, since the noise components are known for all periodic noises, EBGs will be effective solutions to isolate noise coupling.

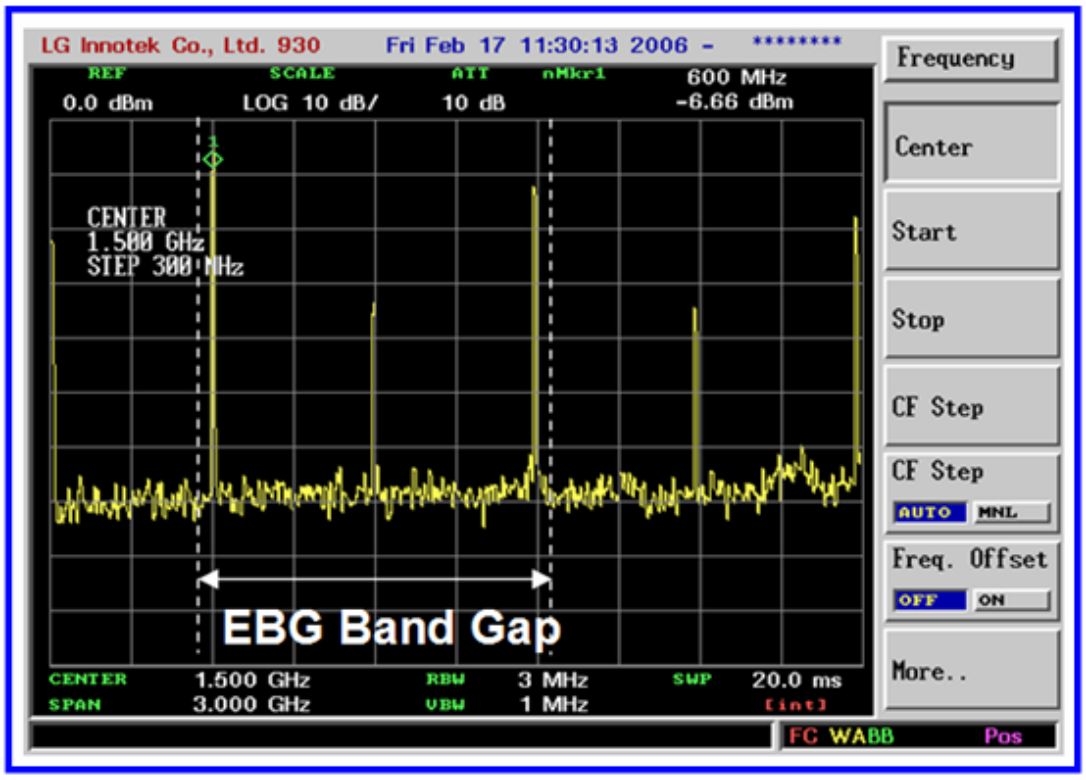


Figure 1.17: Frequency spectrum of the periodic noise source.

Figure 1.18: Frequency spectrum of the random noise source.

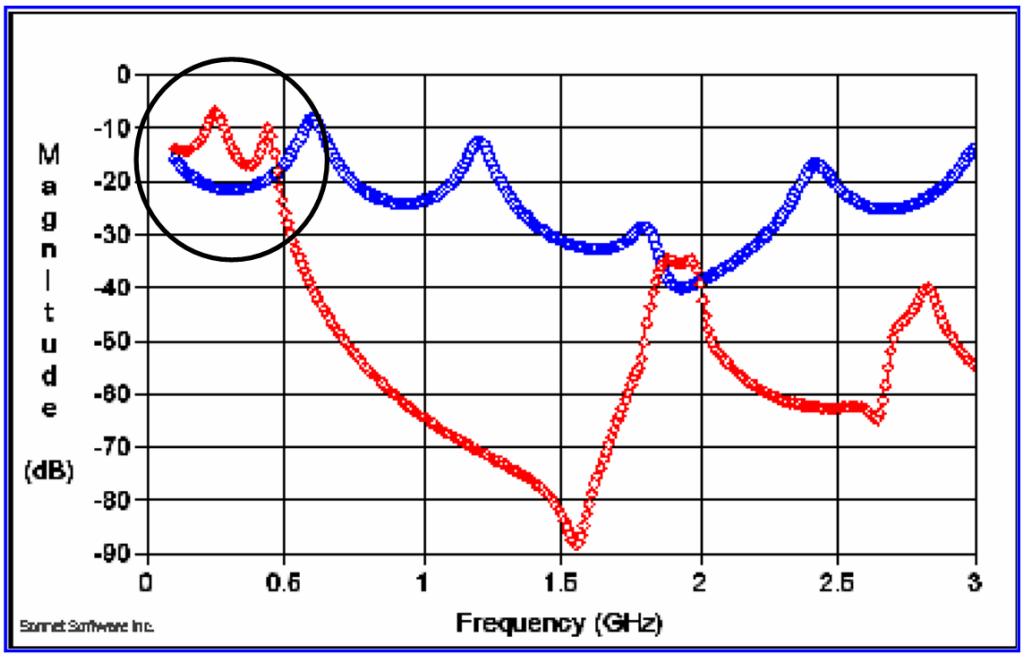


Figure 1.19: Transfer characteristics of the EBG structure (red) and the solid board (blue).

1.7.4 Summary

In this Section, the effect of EBG structures in periodic and random noise source environments has been investigated. While the EBG structure used in a periodic noise environment guarantees much lower noise coupling and timing jitter, the EBG structure in a random noise environment increased the noise coupling and timing jitter. Since the frequency components of random noise is unknown, it is impossible to make the EBG work for all random patterns. However, for specific busses such as the 1.2GHz bus, PCI-X etc. where the noise components are known and fall within the band gap, EBG structures will work very well. For periodic noise sources, EBG structures will always work very well.

So, make the case for mixed signal. For analog circuits, EBG only needs to cover a narrow band. Hence, in this thesis, the focus is on mixed signal.

1.8 Completed Research and Dissertation Outline

The objective of this research is the development of electromagnetic band gap (EBG) synthesis method and its application to mixed-signal systems for simultaneous switching noise (SSN) reduction. The synthesis of EBG structures means the construction of EBG structures based on specifications. As an application, a prototype load board for a high-resolution and high-frequency (gigahertz) analog-to-digital converter (ADC) is considered in this research.

The following work has been completed in this dissertation:

- The development of synthesis method for one-dimensional electromagnetic band gap (EBG) structures.

1. Three new approaches have been suggested: current patch approximation method (CPA-Method), border to border radius (B2BR), and power loss method (PLM). CPA-Method is based on the current flow on a periodically patterned power/ground plane. CPA-Method gives a final dimension of EBG structure for a desired stop band frequency. The B2BR method determines the maximum number of patches implementable within a given area. The PLM method calculates isolation level of an EBG structure based on the transmitted power.

2. The proposed approaches have been combined together to synthesize an EBG structure for a given specification. The synthesized EBG structure with these approaches have been fabricated and verified with electromagnetic (EM) simulation and measurement.

- The development of electromagnetic band gap (EBG) synthesizer using genetic algorithm (GA).

1. GA concepts have been adopted for the development of the EBG synthesizer. A new method has been suggested to encode an EBG structure as genes and to create a string of the genes to form a chromosome. A patch making up an EBG

structure is discretized into square cells. Each cell is expressed with digital symbols according to whether it is a void or a solid. For a void cell, '0' is assigned, and for a solid cell, '1' is assigned. Finally, a patch is expressed by a string of the digital symbols.

2. General GA has been modified to achieve faster and more efficient convergence to a final EBG structure meeting given input specifications. Two new methods have been introduced to ensure continuity in current paths and connectivity between ports. Randomly generated genes result in discontinuous patch shapes for EBG structures. These discontinuous patch shapes (populations) decrease the possibility of convergence to a final solution while going through generations. Therefore, in this synthesizer, instead of creating initial populations at random, it starts with the most reliable population (a solid patch having no holes), and then chooses columns and rows which will be created in terms of genes at random. Also, with constraining the number of columns and rows having holes to be less than 50% of the total number of columns and rows, the synthesizer lowers the possibility of generating discontinuous patch shapes. The connectivity between ports is ensured in the following manner: Starting with a port, identify all square cells that are connected either directly to this port or indirectly through other cells to this port. If at least a neighbor cell of a port (other than the first port) is one among the cells connected to the initial port, then this port is also connected to the initial port. This process is repeated for all ports that are not the initial port. If for a particular port, the connectivity test has failed, then this port is not connected to at least one of the other ports. Therefore, the population containing such a port arrangement is discarded, and the test is started with a new population.

3. The EBG synthesizer using genetic algorithm (GA) has been fully automated by combining GA with multilayer finite-difference method (M-FDM) and

dispersion diagram analysis method. Populations, which are patch shapes in this application, are generated by GA. The M-FDM is used to solve the patch shapes (populations in a generation) in terms of Z-parameter, and the Z-parameter of each population is converted to S-parameter and is transferred to the dispersion diagram analysis part through a conversion code. The dispersion diagram calculates stop band frequencies with the results from the M-FDM.

4. In addition to the automation, synthesized EBG structures are cost-effective solutions because the EBG structures don't require blind vias and additional layer. In addition, since dispersion diagram analysis method has been implemented into the synthesizer to calculate stop band frequencies, only a unit cell is required to be solved, which makes the method computationally effective.

- Analyses of simultaneous switching noise effect on ADC and EBG effect on the noise reduction.

1. Analysis has been conducted on possible switching noise sources for high-speed and high-resolution ADC test boards. It has been found that digital parts of ADC could be an internal noise source, and clock chips and digital chips for data processing could be external noise sources.

2. The effects of the switching noise on ADC performance have been analyzed. It has been found that the switching noise could affect 4 main parts of ADC: i) reference voltage, ii) input voltage, iii) sampling clock, and iv) comparator.

3. ADC performance has been modeled in the presence of the switching noise. It has been observed that the switching noise should be kept at least below 0.5 least significant bit (LSB) for ADCs to operate correctly. Based on the result, design specifications and guidelines for high-speed and high-resolution ADC test board design have been suggested.

4. As a solution to reduce the switching noise, EBGs have been introduced. The effects of the EBGs have been researched with simulations and measurements in various noise environments. It has been verified that EBGs are very effective for periodic noise reduction. However, because of wide-spread spectrum characteristic of random noise, EBGs need very careful application to random noise reduction.

- Low-noise load board design for gigahertz analog-to-digital converters with EBG technique.

1. As an application of EBG technique, a prototype load board for high-resolution and gigahertz ADC has been considered from National Semiconductor. Pre-modification board has been analyzed with simulations and measurements in both frequency-domain and time-domain.

2. Based on the pre-modification board analysis results, three major modifications have been made to the load board. First, the gap between analog power plane and digital power plane on the board has been widened as long as it doesn't affect the connections of all pins to the proper plane to minimize the chance of noise coupling from the aggressors to the victims. Second, the digital power plane on the board has been made larger to decrease the switching noise generation by increasing the plane capacitance. Third, an EBG structure has been created on the digital power plane to minimize the area of the gap by which noise generated in digital plane can couple to analog plane.

3. Based on these modifications, post-modification board has been successfully simulated, designed, fabricated, and measured. The post-modification board showed improvements at 11 locations, no change at two locations, and deterioration at one location among a total of 16 locations. In addition, the post-

modification board has shown fewer fluctuations like saw teeth, which usually result from noise, on each step of digital output.

The rest of this dissertation is organized as follows. One-dimensional EBG synthesis method is suggested in Chapter 2. For two-dimensional EBG structures, a novel EBG synthesis method using genetic algorithms is introduced in Chapter 3. In Chapter 4, simultaneous switching noise effects on ADC is analyzed. In Chapter 5, EBG effects on the noise reduction are discussed in various noise environments. The EBG technique is applied to a real load board design from National Semiconductor in Chapter 6. Finally, the conclusion and the scope of future work are discussed in Chapter 7.

CHAPTER 2

ONE-DIMENSIONAL EBG SYNTHESIS METHOD

With increasing clock frequencies and demands for low supply voltage, today's mixed-signal systems are very sensitive to power/ground noise. For high-speed systems, it has been verified that power/ground pairs form resonators. Consequently, when the power/ground plane resonances are excited, the power/ground noise can be very large [1], [2]. Therefore, power plane resonances are very important for control of power/ground noise.

There have been many research efforts to isolate the sensitive RF/analog circuits from power/ground noise generated by the digital circuits in high-speed mixed-signal systems where digital and RF/analog circuits coexist. The typical approach is to split the power/ground plane [34]. The slot in power/ground plane can partially block the propagation of power/ground noise. However, the power/ground noise can still couple through the slot at high frequencies. In addition to this, split power/ground planes cannot be used for systems requiring a common DC power supply. Hence, filters using ferrite beads have been used to isolate power/ground noise while keeping the same DC power supply [5], but it is not effective at high frequencies.

Electromagnetic band gap (EBG) structures have been also researched and developed to control power/ground noise [6], [7], [9], [25], [26], [27]. EBG structures are periodic structures and exhibit stop band response which can be used to prevent the propagation of electromagnetic waves over a desired frequency range. An EBG structure also makes it possible to use a common DC power supply. Therefore, EBG structures have become very attractive for high-speed system design and integration. However, while there have been numerous papers on the shapes and analysis of EBG structures, there has not been any synthesis method proposed for design of these structures.

In Chapter 2, a synthesis method for one-dimensional (1-D) AI-EBG structures is proposed. One-dimensional EBG structures consist of identical metal patches either in vertical direction or in horizontal direction. The method consists of three newly developed approaches called the current path approximation method (CPA-Method), border to border radius (B2BR) method, and power loss method (PLM), for designing EBG structures.

The CPA-Method is based on the current flow on a periodically patterned power/ground plane. The current flow is another method for expressing transverse magnetic (TM) mode propagation. As the band gap of EBG structure is determined by propagating and non-propagating TM modes, the EBG structure is synthesized for desired stop band frequencies by calculating the TM mode frequencies that determine the band gap. According to CPA-Method, for a one-dimensional EBG structure having N patches, the low frequency edge of band gap is determined by TM(N-1,0) mode, and the high frequency edge of band gap is determined by TM(0,1) mode. The B2BR method is used to determine the maximum number of patches within a given area. The PLM method calculates isolation level for an EBG structure with finally transmitted power. Therefore, for a given design specification, three approaches will work together, and those will give a final EBG structure which not only meets the specification but also gives the optimized performance within a limited area.

2.1 Alternating Impedance Electromagnetic Band Gap (AI-EBG) Structure

An alternating impedance electromagnetic band gap (AI-EBG) structure is an EBG structure that consists of two metal layers separated by a thin dielectric material, as shown in Figure 2.1. In the AI-EBG structure, only one metal layer has a periodic pattern. For two-dimensional (2-D) AI-EBG structures, the periodic pattern is a two-dimensional

(2-D) rectangular lattice with each element consisting of a metal patch with four connecting metal branches, as shown in Figure 2.1. For one-dimensional (1-D) AI-EBG structures, the periodic pattern is a one-dimensional (1-D) rectangular lattice with each element consisting of a metal patch with two connecting metal branches, as shown in Figure 2.2.

The AI-EBG structure can be created by etching metal patches connected by metal branches either on the power plane or on the ground plane depending on design. The unit cell of AI-EBG structure is shown in Figure 2.1. Metal branches are located on the edges of metal patch. The shape of the metal patch and branch can be a square or a rectangle. The AI-EBG structure does not require blind vias. Dielectric thickness can be very thin (1 mil ~ 4 mils), which results in a low-cost process. Hence, the AI-EBG structure can be fabricated using a standard printed circuit board (PCB) process without the need for blind vias, which are essential for mushroom-type EBG structures.

In this Chapter, an EBG synthesis method for one-dimensional AI-EBG structures is presented.

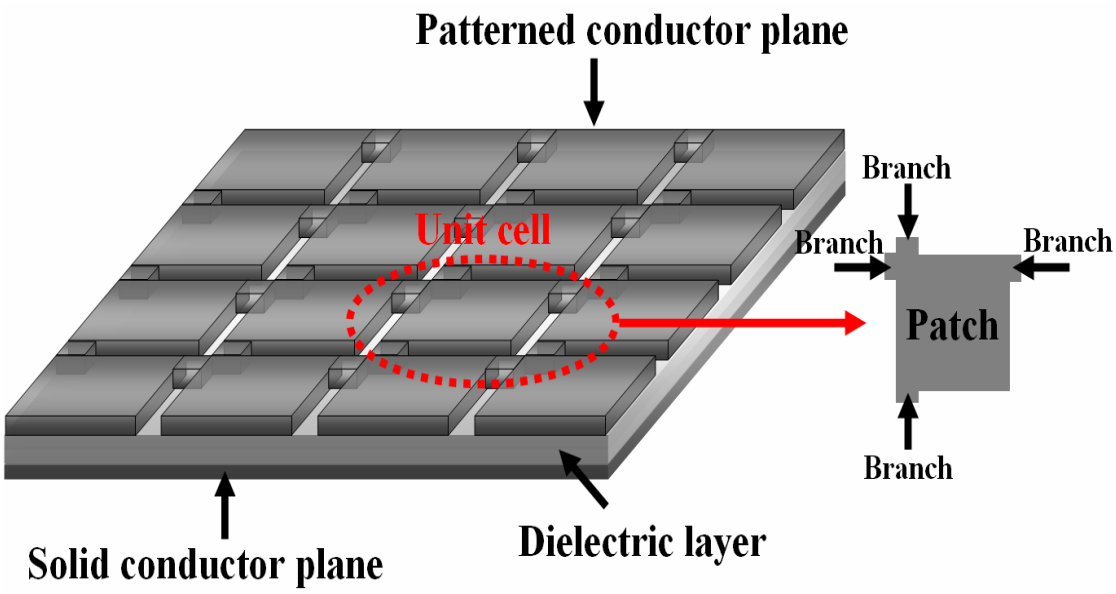


Figure 2.1: Schematic of two-dimensional (2-D) alternating impedance electromagnetic band gap (AI-EBG) structure.

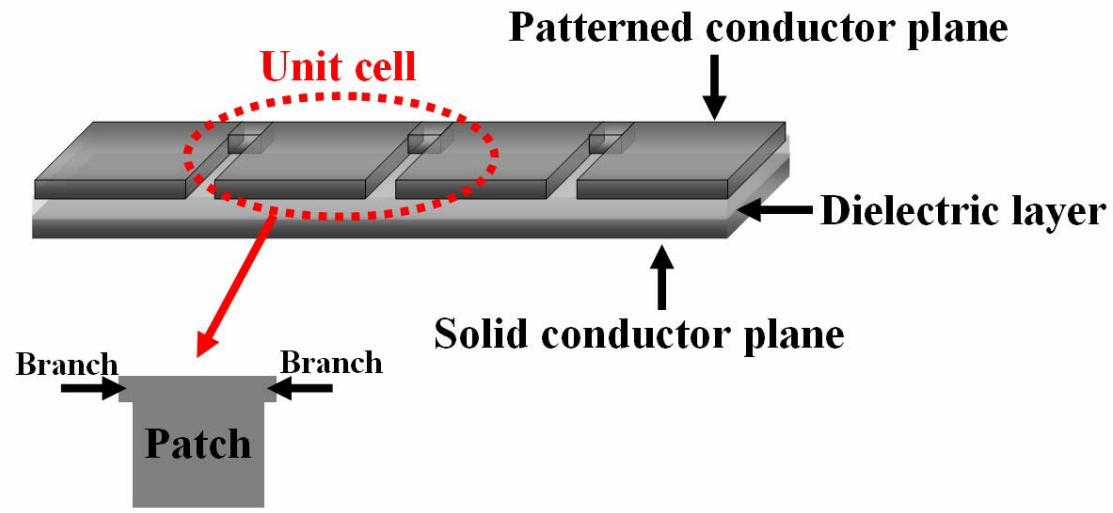


Figure 2.2: Schematic of one-dimensional (1-D) alternating impedance electromagnetic band gap (AI-EBG) structure.

2.2 Proposed Approaches for EBG Synthesis

Design specifications of EBGs consist of three major elements: stop band, isolation level, and available board space for design. Stop band determines the size of a patch and a branch. Isolation level is dependent on the number of patches. Available board space will constrain the maximum number of patches that can be implemented. Finally, if all three major elements can be taken into account during the synthesis phase, not only the final dimension of electromagnetic band gap (EBG) structure can be determined for desired stop band, but also the maximum isolation level with the EBG structure within the available board space can be achieved. Therefore, for optimal synthesis of an EBG structure with given design specifications, analytical methods to combine three elements together are crucially needed.

In this section, three methods will be introduced: CPA-Method, B2BR method, and PLM. CPA-Method will determine the size of a patch and a branch according to the stop band. B2BR will determine the maximum number of patches which can be

implemented within available board space. PLM will calculate isolation level for the EBG structure.

2.2.1 Current Path Approximation Method (CPA-Method)

Resonances on a parallel plate waveguide occur due to energy accumulation in the structure at certain frequencies. For a standard rectangular parallel plate waveguide having much smaller dielectric thickness compared to the width and length of the waveguide, resonance frequencies can be calculated as:

$$f_{mn} \approx \frac{c}{2\pi\sqrt{\mu_r \varepsilon_r}} \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \tag{2.1}$$

where 'a' and 'b' are the length and width of the rectangular parallel plate waveguide, and 'c', 'μ_r', and 'ε_r' are velocity of light in free-space, relative permeability, and relative permittivity.

However, for periodic structures having rectangular unit cells with different sizes, it is not easy to calculate resonance frequencies because electromagnetic field distributions are not simple like a standard rectangular parallel plate waveguide at discontinuities. Therefore, since the surface current is related to the magnetic field, the approximated current path needs to be used for calculating resonance frequencies based on the current flowing along the path with the lowest impedance. In one-dimensional periodic structure as shown in Figure 2.3, each unit cell consisting of a patch and a branch is connected to an adjacent unit cell. Branches are relatively small (as shown in Figure 2.3) compared to the length and width of a patch and the ratio of length and width of a patch is not too large. Hence, the current path can be predicted approximately. Finally, the current path approximation method (CPA-Method) uses the approximated current paths to predict resonance frequencies for one-dimensional periodic structures.

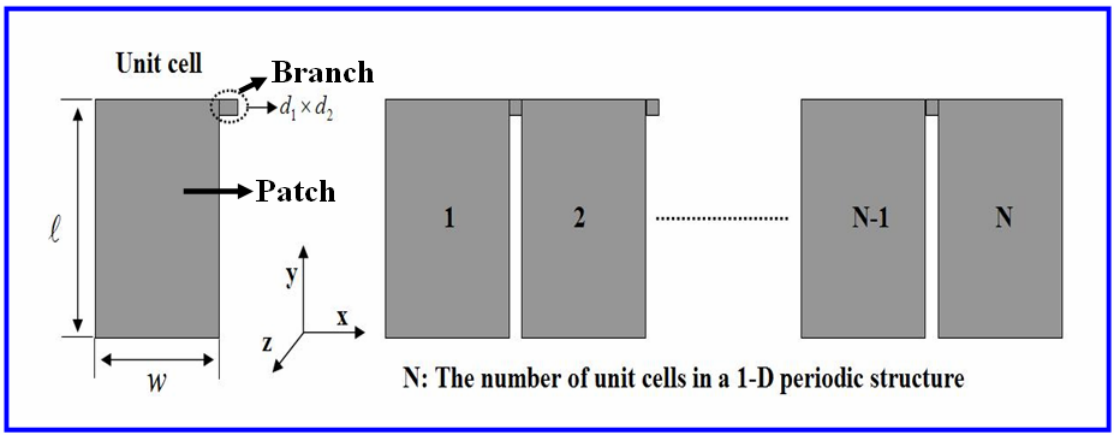


Figure 2.3: Unit cell structure consisting of a patch and a branch and one-dimensional periodic structure consisting of unit cells.

In this Section, CPA-Method is applied to the one-dimensional periodic structure in Figure 2.3 to derive equations to calculate mode resonances of the structure. Current paths on the structure are shown in Figure 2.4. Unit cell is divided into *m* rows, with the current path for each row shown with an arrow in Figure 2.4. Each row has different length of current path for the circled region. Therefore, to calculate an average path for the circled region, the length of each arrow in the circled region are added and divided by the number of rows, as shown in equation (2.2) for the structure. To achieve an excited wave which is continuous, the number of rows was assumed to be infinite as shown in equation (2.3). Equation (2.4) shows calculation of '*a*', which is the total current path in x-direction, derived from CPA-Method for the structure. For simplicity of calculation, it was assumed that *d1* is equal to *d2*, and both of them can be expressed as '*d*'. To calculate resonance frequencies for the one-dimensional periodic structure, '*a*' in (2.1) is replaced with (2.4). '*b*' in (2.1), which is the current path in y-direction, is replaced with 'ℓ' for the structure in Figure 2.3. For general structures where *d1* is not equal to *d2*, equation (2.4) can be expressed as equation (2.5).

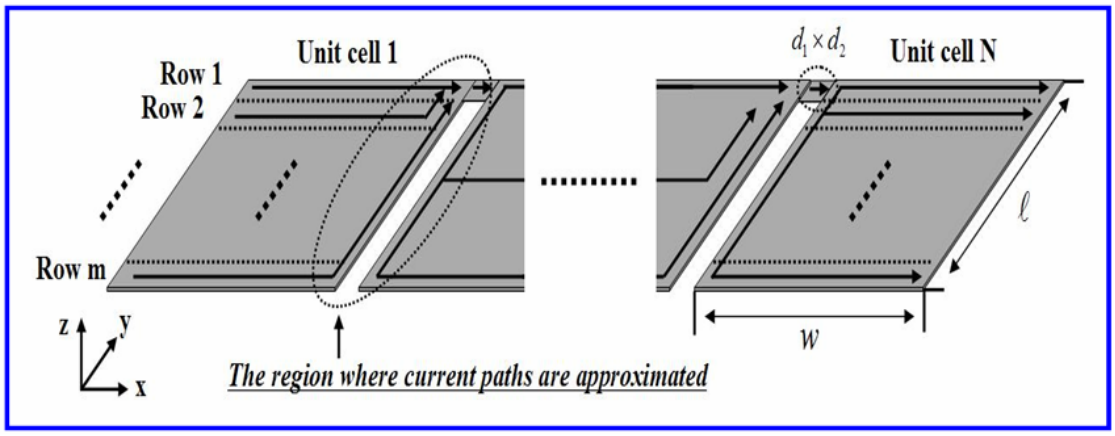


Figure 2.4: One-dimensional periodic structure and current paths on the structure.

$$length_{approximated} = \frac{\left(\frac{1}{m} + \frac{2}{m} \cdots + \frac{m-1}{m} + \frac{m}{m}\right) \times \ell}{m} = \frac{m(m+1)}{2m^2} \times \ell \tag{2.2}$$

$$\lim_{m \to \infty}\left(length_{approximated}\right) = \lim_{m \to \infty} \frac{m(m+1)}{2m^2} \ell \approx \frac{1}{2} \ell \tag{2.3}$$

$$a = w \times N + length_{approximated} \times 2(N-1) + d \times (N-1) = (w + \ell + d) \times N - (\ell + d) \tag{2.4}$$

$$a = (w + \ell + d_2) \times N - (\ell + d_2) + (d_2 - d_1) \times 2 \times (N-1) \tag{2.5}$$

where 'w' is the length of a unit cell along x-direction, 'N' is the number of unit cells, '$length_{approximated}$' is the length of the approximated current path on a unit cell along y-direction, and 'd' is the width and length of a branch (refer to Figure 2.3).

For the structure in Figure 2.3, the high frequency edge of stop band is determined by TM (0, 1) mode, and the low frequency edge of stop band is determined by TM (N-1, 0) mode.

2.2.2 Border to Border Radius (B2BR) Method

More patches provide better isolation. However, practically, the number of implementable patches for design of an EBG structure will be restricted by board size. Furthermore, in some cases EBG structure can be applied for a portion instead of the whole area. Therefore, an approach to achieve best performance within a given area, that is, a method which can guide what is the maximum number of patches implementable within a given area, is very important.

The definition of the size of an EBG structure is shown in Figure 2.5. If an aggressor chip is located on the first patch of the EBG structure, a victim chip which is highly sensitive to the power supply noise generated by the aggressor chip should be located on the farthest patch from the first patch to obtain the most effective isolation. Border to border radius (B2BR) is defined as the radius between the inner border of the aggressor chip and the outer border of the victim chip. By calculating the B2BR, we can predict the maximum size of the EBG structure and determine the maximum number of patches within a given board size. In Figure 2.6, the B2BR was expressed in terms of parameters making up an EBG structure such as 'ℓ', 'w', 'd', and 'N'.

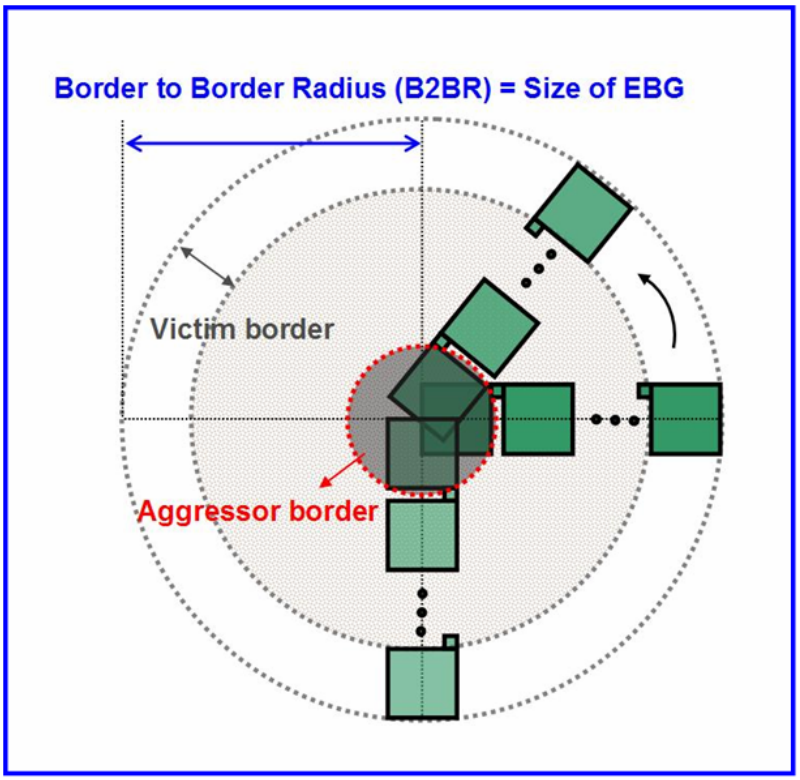


Figure 2.5: The size of an EBG structure is defined as the radius between the inner border of the aggressor chip and the outer border of the victim chip.

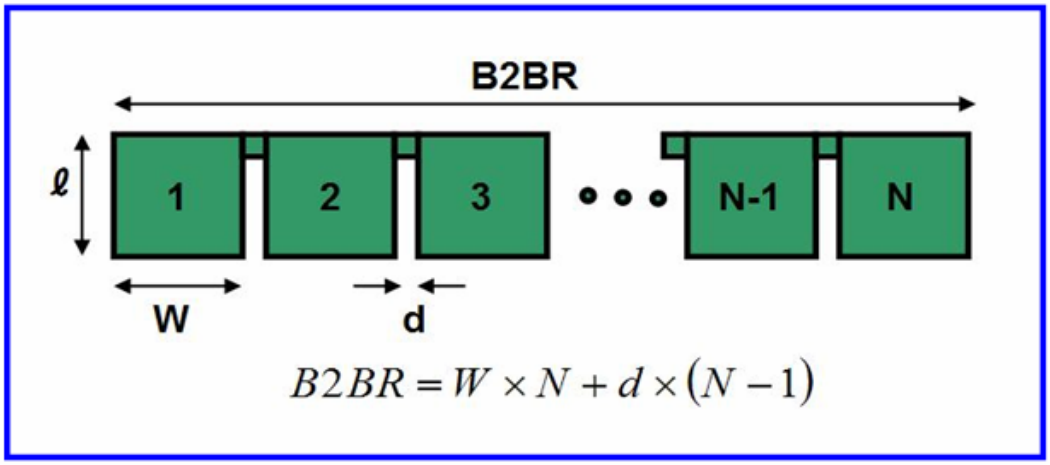


Figure 2.6: B2BR expressed in terms of parameters making up an EBG structure.

For the structure in Figure 2.3, since the high frequency edge (f_{high}) of stop band is determined by (0, 1) mode and the low frequency edge (f_{low}) of stop band is determined by (N-1, 0) mode, equation (2.6) and equation (2.7) can be obtained from equation (2.1).

$$f_{high} = f_{(0,1)} = \frac{1}{2}\frac{c}{\sqrt{\mu_r \varepsilon_r}}\frac{1}{\ell} \tag{2.6}$$

$$f_{low} = f_{(N-1,0)} = \frac{1}{2}\frac{c}{\sqrt{\mu_r \varepsilon_r}}\frac{(N-1)}{a} \tag{2.7}$$

Equation (2.7) can be transformed into equation (2.8), and '*a*' can also be expressed as equation (2.9) from equation (2.4) and Figure 2.5.

$$a = \frac{1}{2}\frac{c}{\sqrt{\mu_r \varepsilon_r}}\frac{(N-1)}{f_{low}} \tag{2.8}$$

$$a = B2BR + \ell \times (N-1) \tag{2.9}$$

Equation (2.10) can be obtained by combining (2.8) and (2.9), and (2.11) can be finally obtained by replacing 'ℓ' in (2.10) with (2.6).

$$B2BR = \left(\frac{1}{2}\frac{c}{\sqrt{\mu_r \varepsilon_r}}\frac{1}{f_{low}} - \ell\right) \times (N-1) \tag{2.10}$$

$$B2BR = \frac{1}{2}\frac{c}{\sqrt{\mu_r \varepsilon_r}} \times \left(\frac{1}{f_{low}} - \frac{1}{f_{high}}\right) \times (N-1) \tag{2.11}$$

This gives a linear equation between available design space (B2BR) and the number of patches (N). As shown in equation (2.11), for a given stop band ($f_{low} - f_{high}$), a linear line between B2BR and N shown in Figure 2.7 can be plotted. Therefore, if available design space for an EBG structure is given, the maximum number of patches implementable within that space can be decided.

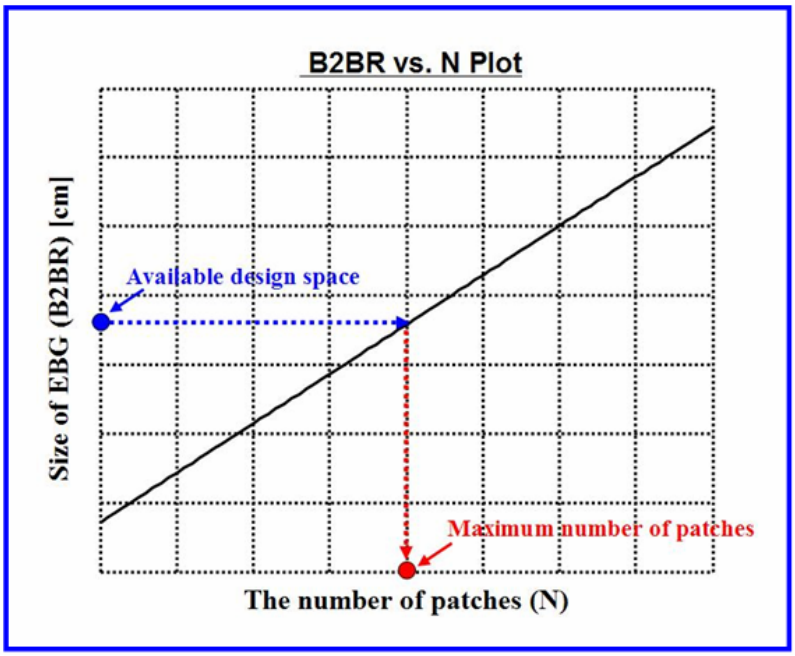


Figure 2.7: B2BR vs. N; Linear plot from (2.11) for a given stop band (f_{low} - f_{high}).

2.2.3 Power Loss Method (PLM)

Electromagnetic wave propagation is interrupted where it meets impedance mismatch. Electromagnetic band gap (EBG) structures are periodic structures, so the propagation of electromagnetic wave is interrupted and reflected when the wave goes through from the patch to a small branch and from a branch to a relatively large patch due to impedance mismatch. Less power will be transmitted at frequencies where more reflection occurs. Over those frequencies, stop band of the EBG structure occurs. Finally, if it is assumed that electromagnetic wave is fully reflected at impedance mismatches and radiation loss is relatively small compared to reflection loss, transmitted power can be calculated by subtracting reflected power from input power. The conceptual description of this concept is shown in Figure 2.8.

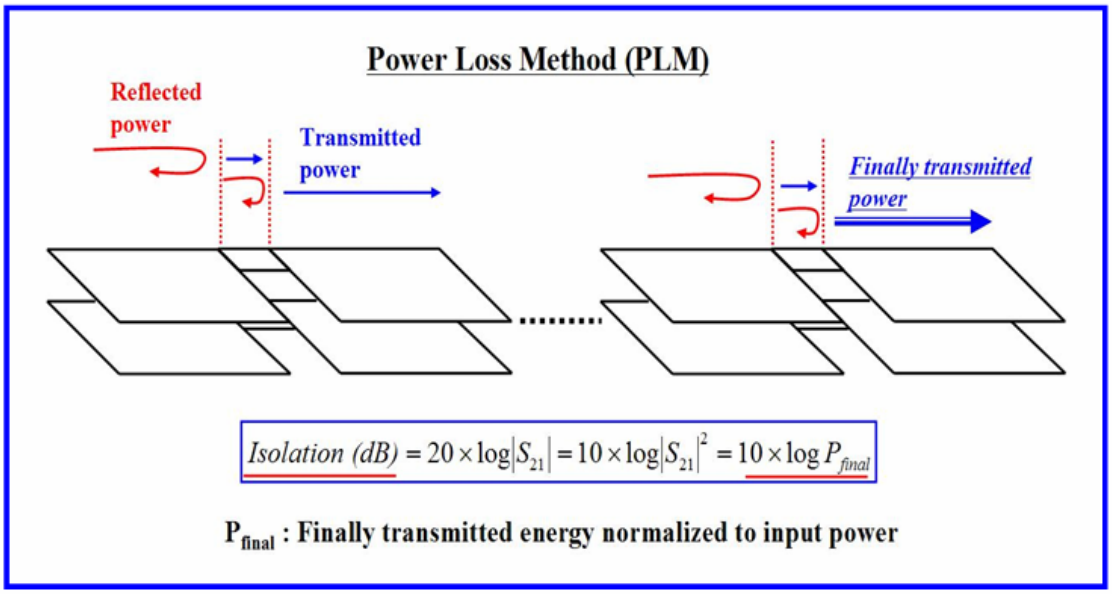


Figure 2.6: Conceptual description of power loss method (PLM).

The transmitted power through impedance mismatch can be calculated with reflection coefficient (Γ). For two lossless transmission lines having different characteristic impedances such as Z_O and Z_L, voltage and current waves according to the location z can be expressed as:

$$V(z) = V_0^+ \left[e^{-j\beta z} + \Gamma e^{j\beta z} \right] \tag{2.12}$$

$$I(z) = \frac{V_0^+}{Z_0} \left[e^{-j\beta z} - \Gamma e^{j\beta z} \right] \tag{2.13}$$

The time-average power flow along the line at the point z can be calculated as:

$$\begin{aligned} P_{av} &= \frac{1}{2} \mathrm{Re}\left[V(z) I(z)^* \right] \\ &= \frac{1}{2} \frac{\left| V_0^+ \right|^2}{Z_0} \mathrm{Re}\left\{ 1 - \Gamma^* e^{-2j\beta\beta} + \Gamma e^{2j\beta\beta} - \left| \Gamma \right|^2 \right\} \\ &= \frac{1}{2} \frac{\left| V_0^+ \right|^2}{Z_0} \left(1 - \left| \Gamma \right|^2 \right) \end{aligned} \tag{2.14}$$

If delivered power is normalized to incident power, (2.14) can be simplified as:

$$p_{delivered\_normalized} = 1 - |\Gamma|^2 \tag{2.15}$$

To apply (2.15) to an EBG structure, the EBG structure is represented with a transmission line model including discontinuity model as shown in Figure 2.9 [28]. Equations to calculate equivalent circuit values for the discontinuity model are derived in [35].

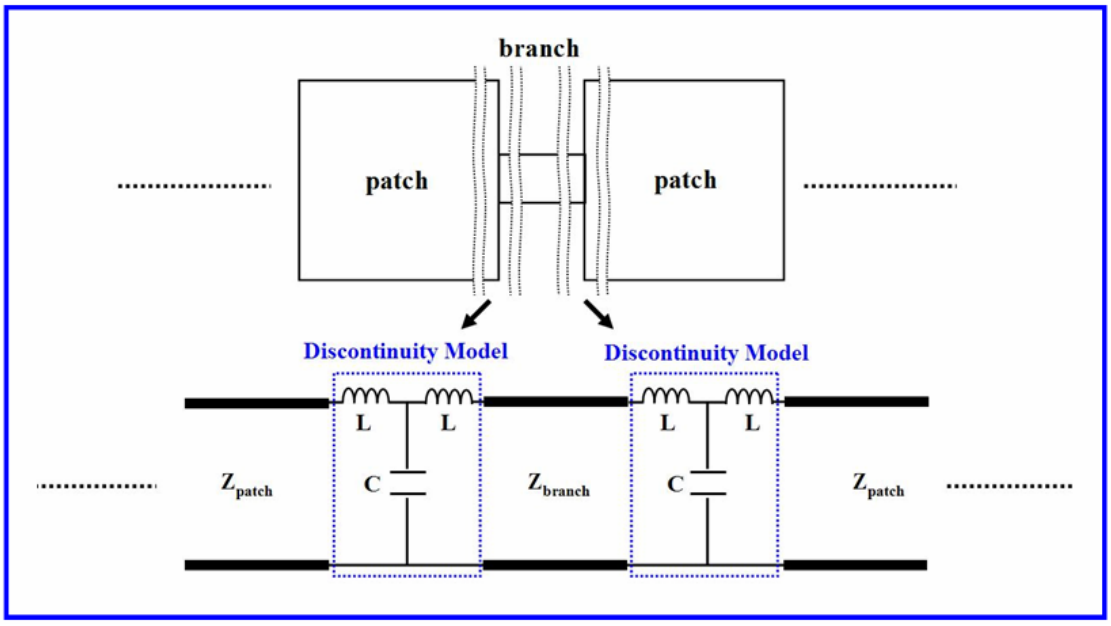
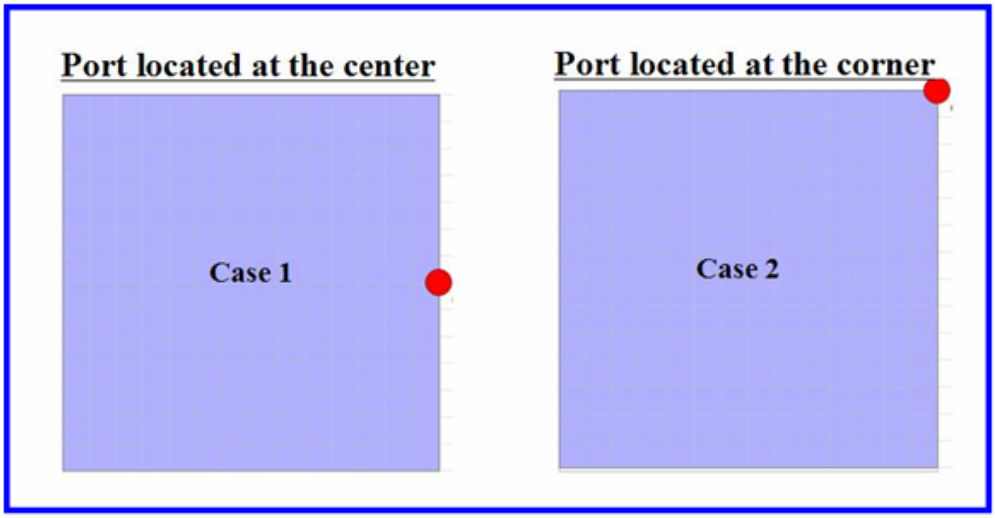


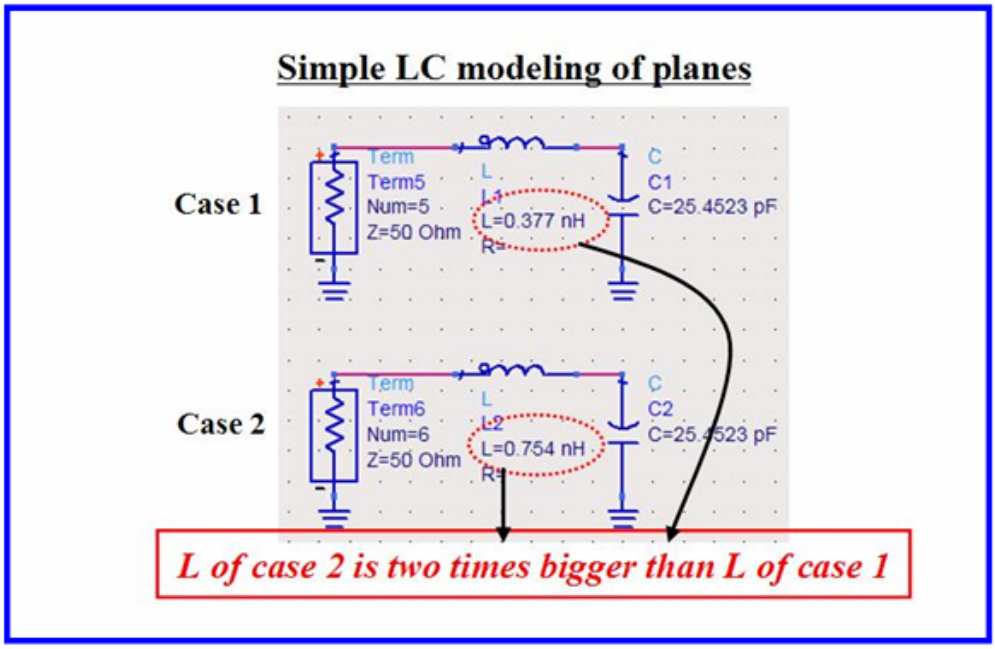
Figure 2.9: Transmission line modeling of an EBG structure including discontinuity model [28].

In this model, the branch was located at the center of patch. However, if a branch is located at the corner of a patch like an EBG structure shown in Figure 2.3, path inductance of power/ground plane will be two times bigger than that for the case that a branch is located at the center of a patch. This can be easily verified with one-port power/ground plane simulation. Figure 2.10(a) shows simulation setup with transmission matrix method (TMM) [36]. In case 1, a port is located at the center of a plane, and in case 2, a port is located at the corner of the plane. Power/ground plane was modeled with simple LC network as shown in Figure 2.10(b) to figure out inductance (L) and capacitance (C) values for two cases. As shown in Figure 2.10(b), the value of

capacitance is same regardless of port locations since the size of power/ground plane is same. However, the value of inductance depends on the port locations even though the size of power/ground plane is same. This can be also verified with CPA-Method. As shown in Figure 2.11, when CPA-Method was applied to the structure having a branch at the center of a patch, the approximated current path as calculated in (2.17) will be two times shorter than that in (2.3).

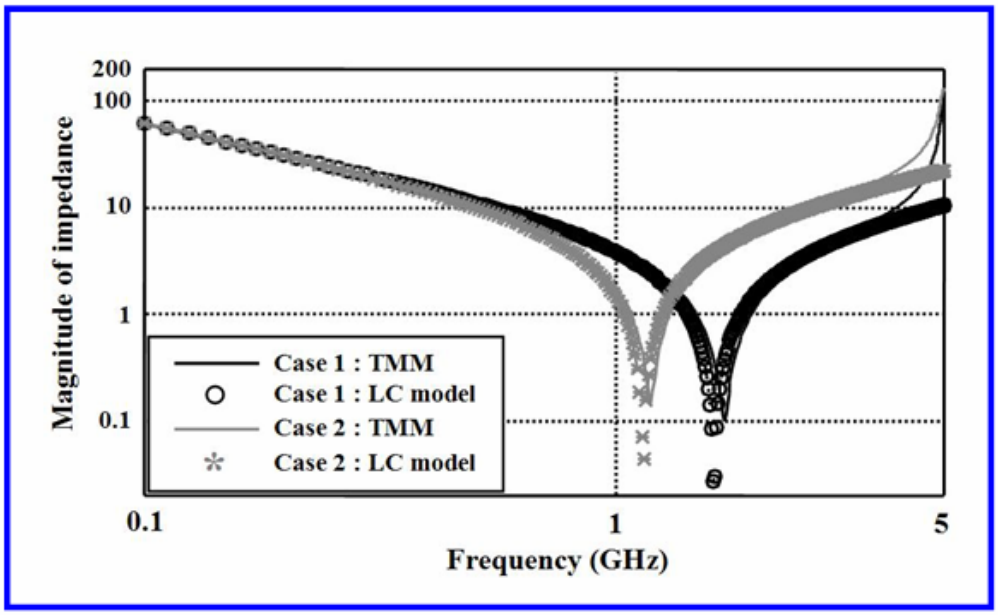


(a)



(b)

Figure 2.10: (a) Transmission matrix method (TMM) simulation setup for two cases, (b) simple LC modeling for each case, and (c) overlapped plots for the two cases.



(c)

Figure 2.10: Continued.

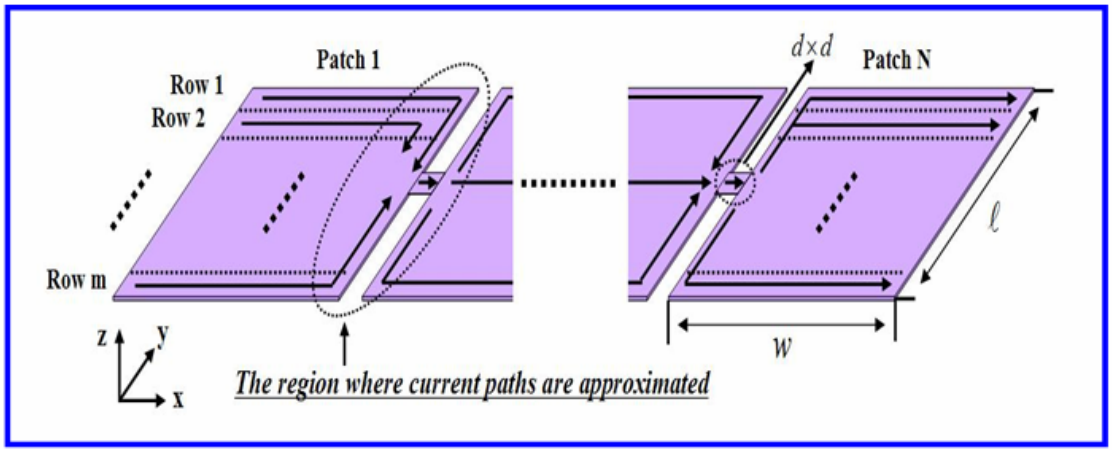


Figure 2.11: One-dimensional periodic structure having a branch at the center of a patch and current paths on the structure.

$$length_{approximated} = \frac{2\times\left(\frac{1}{m}+\frac{2}{m}\cdots+\frac{\frac{m}{2}}{m}\right)\times\ell}{m} = \frac{\frac{m}{2}\left(\frac{m}{2}+1\right)}{m^2}\times\ell \tag{2.16}$$

$$\lim_{m\to\infty}\left(length_{approximated}\right) = \lim_{m\to\infty}\frac{\frac{m}{2}\left(\frac{m}{2}+1\right)}{m^2}\ell \approx \frac{1}{4}\ell \tag{2.17}$$

Finally, for the EBG structure shown in Figure 2.3, the value of L for the transmission line model shown in Figure 2.9 will be twice compared to the periodic structure shown in Figure 2.11. Figure 2.12 shows a general equation for isolation calculation derived using PLM method.

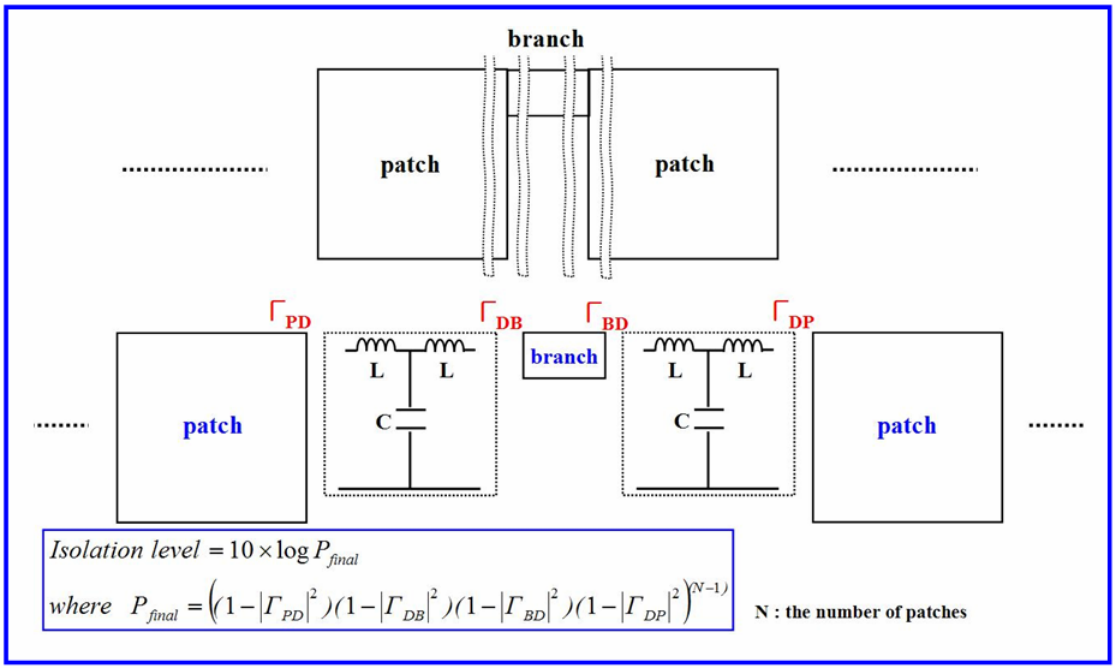


Figure 2.12: PLM method to calculate isolation level for the EBG structure.

2.3 Synthesis of EBG Structure with Proposed Approaches

In this section, synthesis of an EBG structure for a desired specification with the proposed approaches will be explained. The overall flow chart for the synthesis method is shown in Figure 2.13.

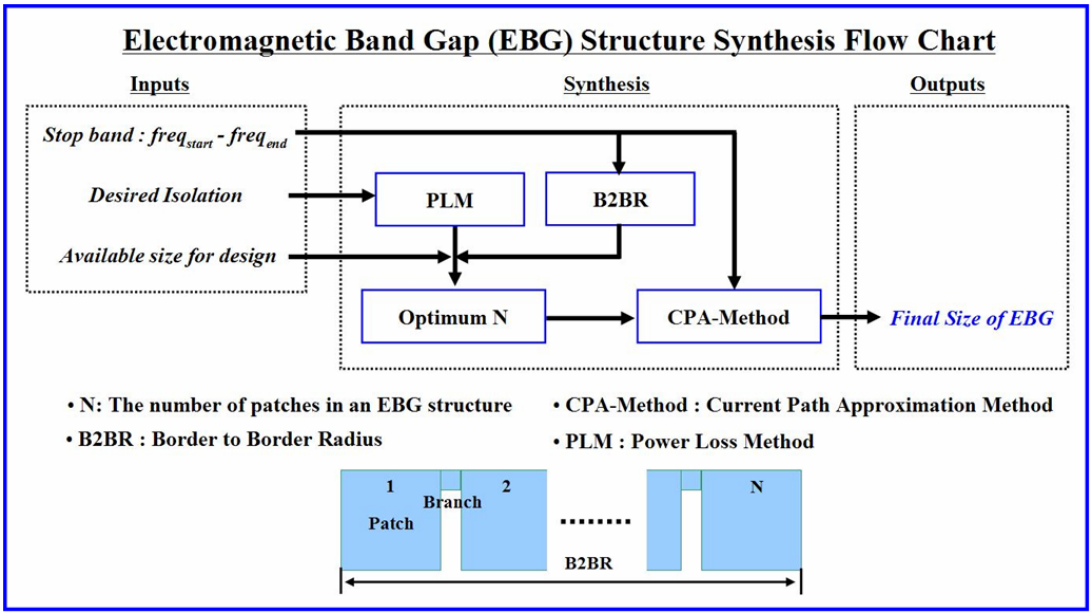


Figure 2.13: Electromagnetic band gap (EBG) structure synthesis flow chart: 1) Current Path Approximation Method (CPA-Method) is used to determine the size of a patch and a branch of an EBG structure for a desired stop band frequency, 2) Border to Border Radius (B2BR) determines the maximum number of patches that can be implemented within given available size, and 3) Power Loss Method (PLM) calculates isolation level in dB.

Assume that a noise source on a mixed signal system ranges from 3GHz to 5GHz and available board space for design of EBG structure is 50mm. An EBG structure is designed for a band gap from 2.5GHz to 5.5GHz.

First, the maximum number of patches implementable within a given design space, which is 50mm in this case, can be determined by (2.11). Figure 2.14 shows B2BR vs. N plot from (2.11) for f_{low}=2.5GHz and f_{high}=5.5GHz. According to the plot, N=4 is the maximum number of patches implementable within the given 50mm length space.

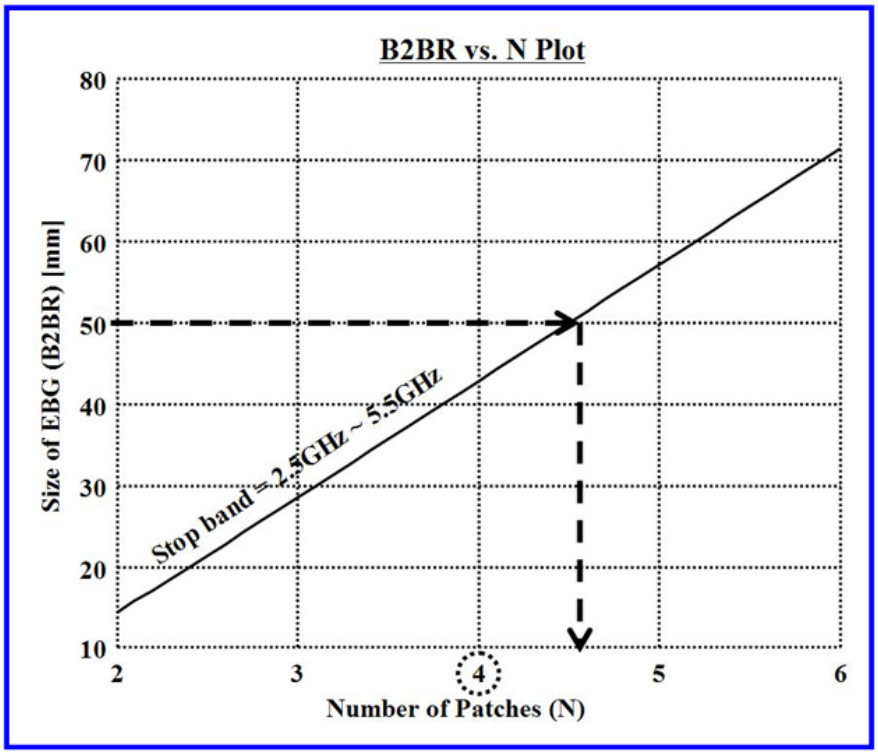


Figure 2.14: B2BR vs. N plot from (2.11) with stop band (2.5GHz ~ 5.5GHz).

After N is determined by B2BR, other parameters will be determined using the CPA-Method. As mentioned in the previous section, the low frequency edge of stop band, which is 2.5GHz in this case, is determined by (N-1, 0) mode, and the high frequency edge of stop band, which is 5.5GHz in this case, is determined by (0,1) mode. To calculate dimensions of the structure from given mode frequencies, equation (2.1) can be transformed into '*a*' and '*b*' equations with other parameters as shown in equations (2.18) and (2.19).

$$a = \frac{1}{2}\frac{c}{\sqrt{\mu_r \varepsilon_r}}\frac{m}{f_{m0}} \tag{2.18}$$

where *n* is zero because (N-1,0) mode determines the low frequency edge of stop band.

$$b = \frac{1}{2}\frac{c}{\sqrt{\mu_r \varepsilon_r}}\frac{n}{f_{0n}} \tag{2.19}$$

where *m* is zero because (0,1) mode determines the high frequency edge of stop band.

Figure 2.15 shows a flow chart to determine other parameters for an EBG structure meeting a desired band gap with equations derived above. In the design phase, these values will be rounded off to ℓ=500mils, *w*=400mils, and *d1=d2*=40mils for design simplicity. For this structure, PLM method showed about -85dB isolation. For this structure, equivalent circuit values for the discontinuity models shown in Figure 2.9 are L=8.53e-18H, 9.54e-17H, 1.19e-14H, 1.07e-15H (from left to right) and C=1.84e-19F, 1.56e-19F (from left to right).

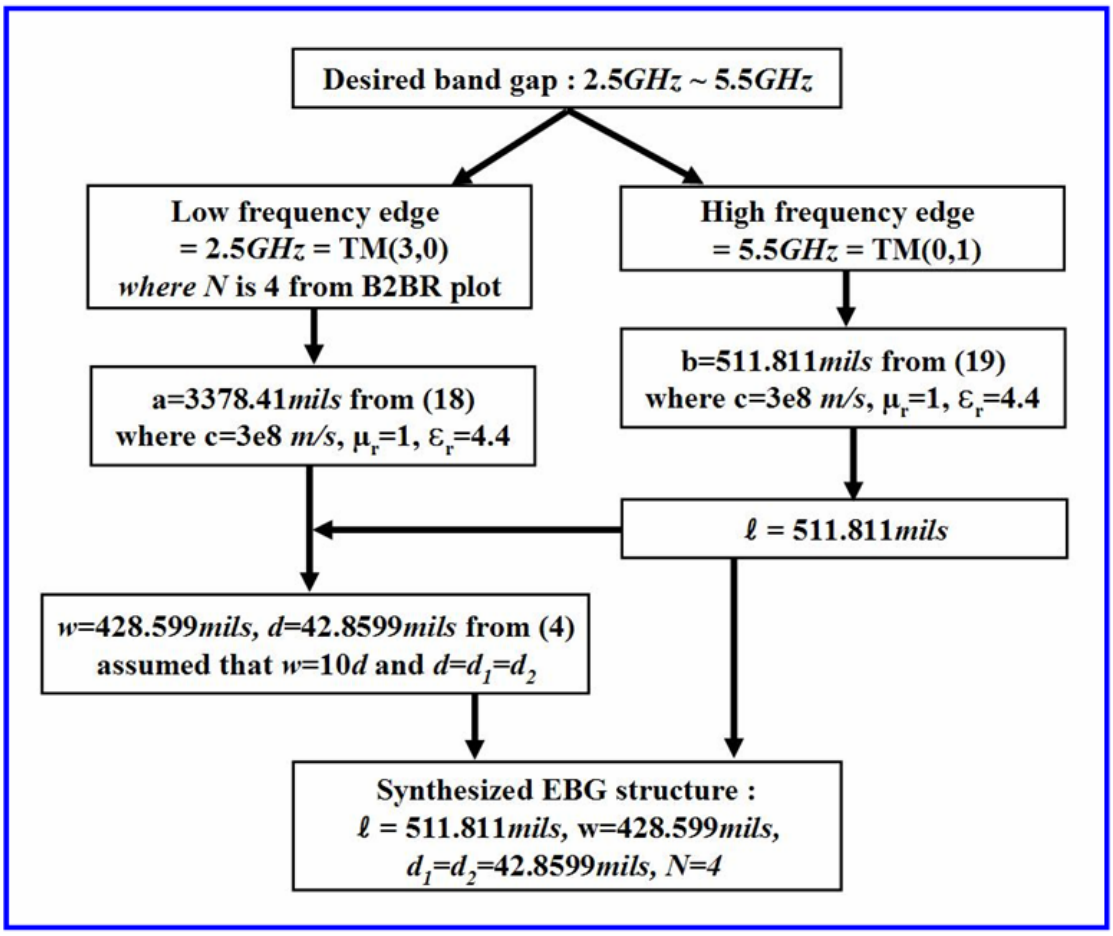


Figure 2.15: Flow chart to synthesize an EBG structure.

As shown in this example, if a desired specification is given, dimensions of the EBG structure to meet the specifications can be easily synthesized using the proposed approaches.

2.4 Verification

In the previous section, an electromagnetic band gap (EBG) structure was synthesized with the proposed approaches for a desired band gap (2.5GHz – 5.5GHz) and a given design space (50mm). In this section, the synthesized EBG structure will be verified through EM simulation and measurement.

The synthesized EBG structure and ports for simulation and measurement are shown in Figure 2.16. First, the synthesized EBG structure was simulated with Sonnet which is a 3D planar full-wave EM simulation tool. Dashed line in Figure 2.17 is the simulated result. The simulated result shows that the synthesized EBG structure has a band gap approximately from 2.5GHz to 5.5GHz, which is the desired band gap.

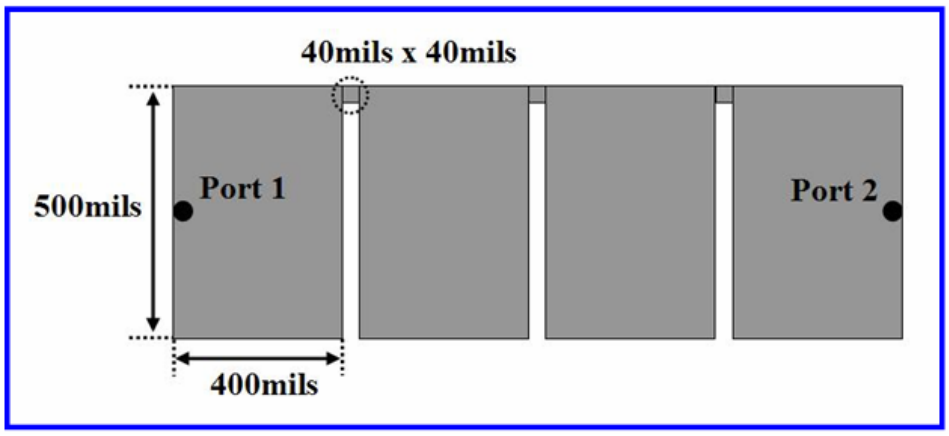


Figure 2.16: Synthesized EBG structure for a desired band gap (2.5GHz ~ 5.5GHz) and a given design space (50mm) with proposed approaches and port locations for simulation and measurement: for design simplicity, calculated values of EBG structure were rounded off.

The synthesized EBG structure was also fabricated using standard planar printed circuit board (PCB) process. The dielectric material is FR4, and the thickness of dielectric material is 5mils. The fabricated EBG structure was measured with an Agilent 8720ES vector network analyzer (VNA). Solid line in Figure 2.17 shows the measured result. The measured result shows not only that the synthesized EBG structure has a band gap approximately from 2.5GHz to 5.5GHz, which is the desired band gap, but also that isolation level is about -85dB which is calculated by PLM. The slight difference between desired band gap and band gap from the synthesized EBG structure in Figure 2.17 can be due to the rounded values of the synthesized EBG structure for design simplicity.

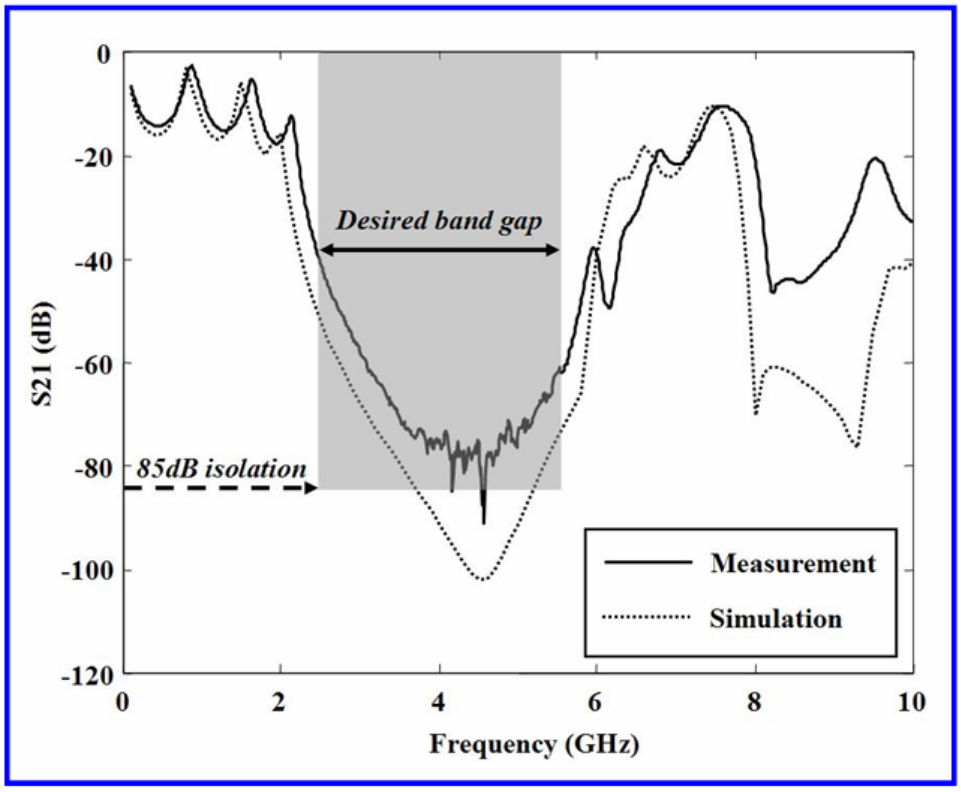


Figure 2.17: Simulated and measured transmission parameter (S21) for the synthesized EBG structure. The colored area is the desired band gap, and the dashed arrow is the calculated isolation level with PLM.

2.5 Summary

In this Chapter, a novel synthesis method consisting of the current path approximation method (CPA-Method), border to border radius (B2BR), and power loss method (PLM) was developed for one-dimensional periodic structures. An EBG structure was synthesized using these methods for a given design specification. The synthesized EBG structure was fabricated and verified with EM simulation and measurement. Stop band and isolation of the EBG structure showed good agreements with the design specification.

CHAPTER 3

EBG SYNTHESIS METHOD USING GENETIC ALGORITHMS

In this Chapter, a novel electromagnetic band gap (EBG) synthesis method using genetic algorithms is introduced for mixed signal applications. In this method, a genetic algorithm (GA) is utilized as a solution-searching technique. One of the main advantages of the proposed method is an automated design procedure for EBG structures that meet given design specifications. For this purpose, the GA method is combined with multilayer finite-difference method (M-FDM) [37] and dispersion diagram (DD) method [38]. The M-FDM is a circuit-based simulator for computing the Z-parameters of planar structures, while the DD method is a plot of the propagation constant versus frequency. The EBG synthesis method introduced in this paper consists of three main parts namely: a) GA, which generates populations of EBG structures and evaluates fitness functions using band gap response results from DD; b) M-FDM, which analyzes the EBG structures generated by the GA and links the analysis results to DD; c) DD, which calculates band gap frequencies using the EBG structure analysis results from the M-FDM and links the calculated stop band frequencies to the GA for fitness checks.

3.1 Design Flow for Electromagnetic Band Gap (EBG) Structures

Electromagnetic band gap (EBG) structures have been in the limelight recently for simultaneous switching noise (SSN) suppression in high-speed digital systems due to its passband and stopband characteristics. EBG structures are promising solutions for noise isolation, but despite the potential benefits of EBG structures, implementation of these structures can be costly and prohibitive. This is because the design of EBG

structures involves a manual process that is time consuming, computationally expensive, and often times unreliable. Therefore, in this section, drawbacks of the design flow being used today are presented along with a new design flow.

3.1.1 Current Design Flow

Figure 3.1 provides a block diagram of the current manual process for EBG structure design. The manual process involves devising a set of input specifications for an electromagnetic band gap structure. A prototype EBG structure is then created based on estimations in view of these input specifications. The prototype EBG structure is then analyzed with either a circuit simulator or electromagnetic (EM) simulator. The solved results of the prototype EBG structure are then compared with the input specifications to determine the validity of the EBG structure. If the EBG structure does not meet specifications, the prototype EBG structure is modified. Thereafter, the modified prototype EBG structure is analyzed and the results are compared again with the input specifications. The process of modifying, solving, and comparing are repeated until the EBG structure complies with the input specifications.

As expected, the current method of EBG structure design, shown in Figure 3.1, suffers from many drawbacks. For example, the number of iterations required for the manual method is often large. Therefore, numerous iterations are required to achieve a workable EBG structure. Furthermore, many input specification sets may have no solution. Therefore, a designer implementing the manual method may go through hundreds of iterations of the method without ever achieving a satisfactory EBG structure. Therefore, the manual method of EBG structure design is computationally expensive and often times time consuming. Another major problem with the current approach is the need for design expertise. A designer currently needs to have knowledge on EBG behavior before the structure can be designed. As the EBG structures become more main

stream, where such designs have to be embedded into Printed Circuit Boards, high level of design expertise cannot be expected. Thus a new design flow is required which is the focus of this chapter.

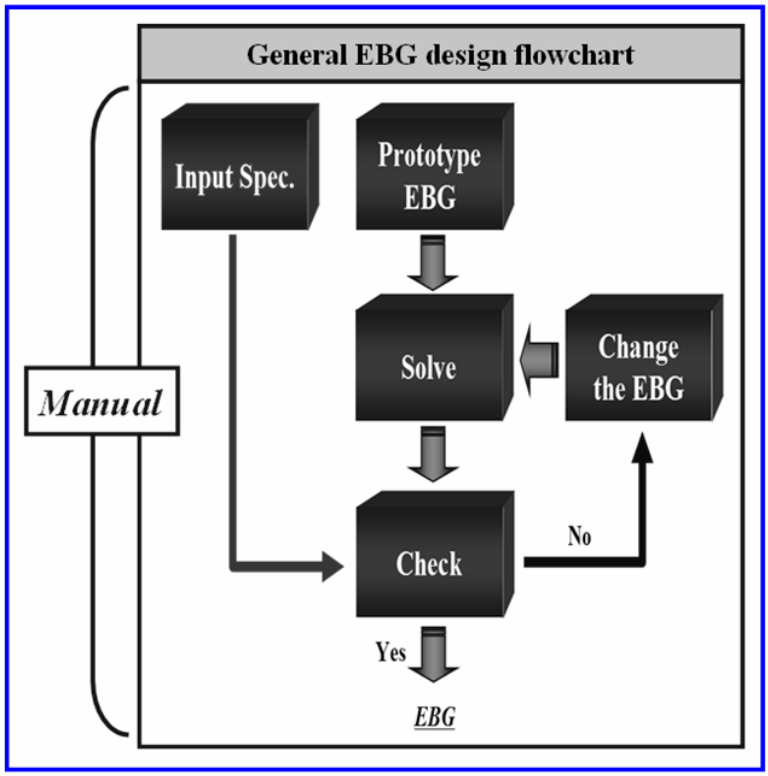


Figure 3.1: Current manual process for electromagnetic band gap structure design.

3.1.2 New Design Flow

In this research, a new design flow is suggested by focusing on an effective and completely automated synthesis of EBG structures. The new EBG design flow allows a user to provide a set of desired specifications for the EBG structure, including 1) on-set frequency of the band gap, 2) off-set frequency of the band gap, 3) isolation level, and 4) materials information such as conductor and dielectric properties, and receive, as the

output, the design of the EBG structure which meets the desired characteristics. In addition, the suggested flow aims at automatically determining when the synthesis of an EBG structure with a particular set of band gap parameters is not possible, that saves valuable time during the design process.

Figure 3.2 shows the overall block diagram for the suggested EBG design flow. As shown in Figure 3.2, the design flow consists of three main parts namely: a) genetic algorithm (GA), b) multilayer finite-difference method (M-FDM), and c) dispersion diagram (DD) analysis. Each part of the algorithm has the following functions:

1) The GA generates populations that represent EBG structures and evaluate fitness functions by using analysis results from DD analysis (for band gap frequency fitness check) and M-FDM (for isolation level fitness check).

2) The M-FDM solves the EBG structures generated by the GA and links the analysis results to DD (for calculating band gap frequencies) and the GA (for isolation level fitness check).

3) The dispersion diagram (DD) calculates band gap frequencies by using the EBG structure analysis results from the M-FDM and links the calculated band gap frequencies to the GA for fitness checks.

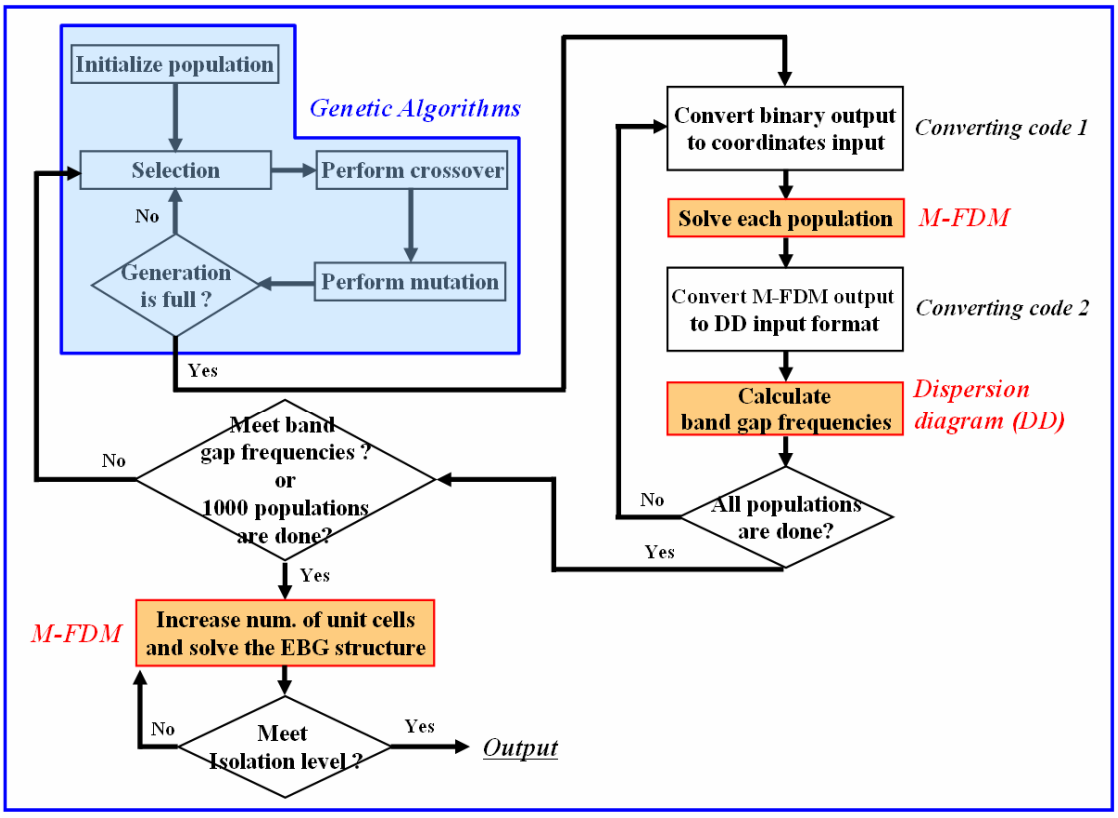


Figure 3.2: Overall block diagram of the suggested electromagnetic band gap synthesis method.

3.2 A Novel EBG Synthesis Method

As mentioned in Section 3.1, the suggested method consists of three parts namely, GA, M-FDM, and DD. In this Section, each technique is explained in detail, along with their inter-connectivity.

3.2.1 Genetic Algorithm (GA)

Genetic algorithm (GA) is an adaptive heuristic search algorithm. The GA represents an intelligent use of a random search within a defined search space to find a solution. More importantly, the GA is intrinsically parallel. Most other algorithms are serial and can only explore the solution space to a problem in one direction at a time, and

if the solution they discover turns out to be suboptimal, there is nothing to do but abandon all work previously completed and start over. However, since the GA has multiple offsprings, they can explore the solution space in multiple directions at once. If one path turns out to be a dead end, they can easily eliminate it and continue work on more promising avenues, giving them a greater chance of finding the optimal solution. Accordingly, the GA has been utilized as an intelligent and random search method to find a solution within a defined search space for the suggested EBG synthesis method.

To apply GA concepts to EBG synthesis, three problems need to be solved. First, to create a population, an EBG structure needs to be encoded as a string of genes. The EBG structure under consideration for the suggested EBG synthesis method is a two metal layer periodic structure consisting of identical metal patches in the vertical and horizontal directions, as shown in Figure 3.3. Dispersion diagram (DD) has been implemented for evaluating fitness values related to stop band frequencies. This diagram predicts stop band frequency responses for periodic structures by solving just a unit cell (or patch) that comprises the whole structure. As a result, a single patch making up an EBG structure is sufficient to predict the stop band frequencies of the EBG structure. Therefore, in the suggested method, a patch is encoded in terms of genes, as shown in Figure 3.3. Figure 3.3 shows an example of a patch discretized by 5x5 square cells. Each square cell is expressed with digital symbols according to whether it is a void or a solid cell. For a void cell, ‘0’ is assigned, and for a solid cell, ‘1’ is assigned. The square cells are numbered sequentially from left-bottom corner to right-top corner, as shown in Figure 3.3. The order of unit cells matches with the order of genes making up a population, as shown in Figure 3.3.

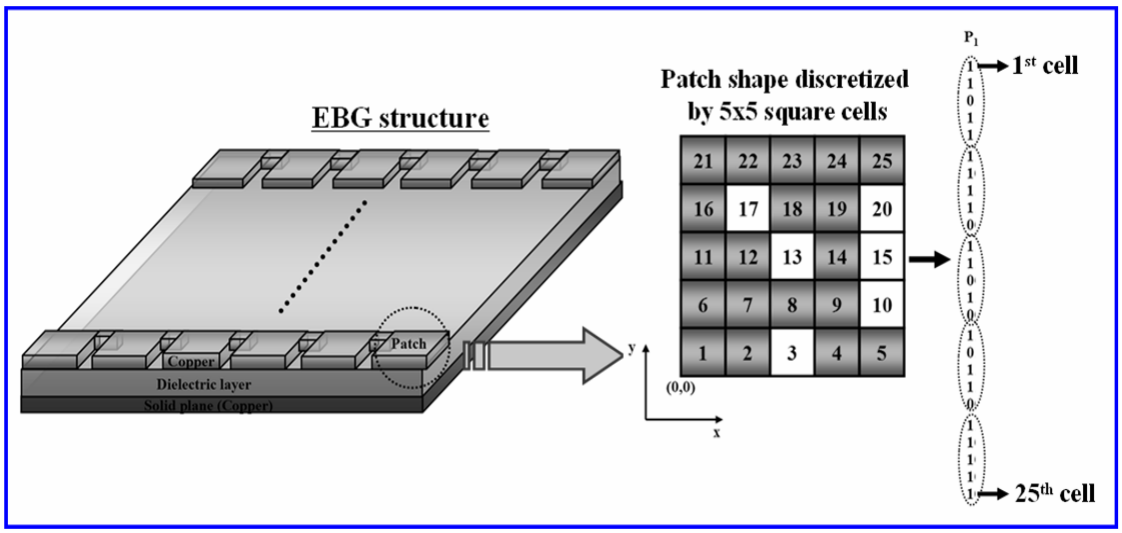


Figure 3.3: Encoding of an EBG structure in terms of genes to apply genetic algorithm concepts to EBG synthesis.

Second, when general GA concepts are applied to EBG synthesis, populations (which are patches in this application) with discontinuities in the current paths will slow down the convergence to the final solution. If initial populations are generated at random, there is a very high chance for the initial populations to have discontinuous current paths, as shown by the examples in Figure 3.4. The discontinuous parent populations tend to have more void cells than solid cells. Crossover and mutation are employed to obtain child populations from the parent populations. However, if the parent populations are discontinuous, the child populations have a very high possibility of also being discontinuous. Hence, almost every initial population should be ensured to have continuous current paths. To ensure this, the following method has been suggested in this chapter. Instead of creating initial populations at random, the suggested method starts from the most reliable population (a solid patch having no holes), and then chooses columns and rows that contain holes at random. It is important to make the number of columns and rows containing holes to be less than 50% of the total number of columns and rows. An increase in the percentage would increase the possibility of generating

discontinuous patch shapes. The basic idea behind the suggested method is to make each population have at least more than 50% solid cells.

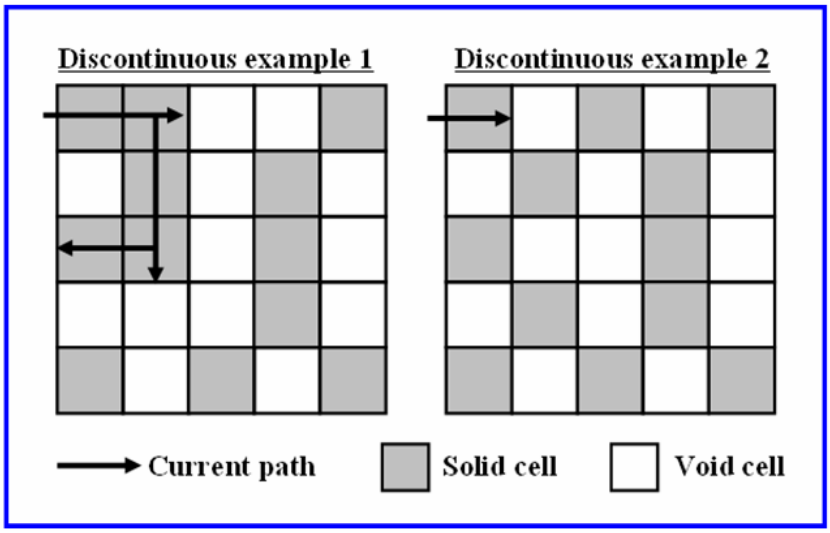


Figure 3.4: Examples of discontinuous populations in terms of current path.

The third problem has to do with connectivity between ports for each population in every generation. Ports are entities used to represent the system (patch) in terms of its terminal behavior. Such a representation captures the physics of the problem in a simplified manner. Four ports are needed to represent a patch in two-dimensional (2-D) EBG structure. These ports are then used to obtain a multiport impedance parameter (Z-parameter) representation of a patch. For this step, M-FDM is used. The four-port Z-matrix is later used by DD to predict stop band frequencies for each patch shape. While deriving the Z-parameter representation, it is important to make sure there is connectivity between ports: When a port is isolated at least from one of the other ports, this situation results in the loss of DC connection between at least two points in the power plane. Loss of DC connectivity should be avoided at all times. This means there should not be any isolated port in any population across different generations. The method, which was suggested to resolve the second problem in the previous paragraph, guarantees that there

are no isolated ports in any population in the first generation. However, due to crossover and mutation followed in the subsequent generations, such nonisolation of ports in a population cannot be guaranteed in subsequent generations. Therefore, the connectivity between ports has to be ensured even in the populations in the subsequent generations. The port connectivity is ensured in the following manner: Starting with a port, identify all square cells that are connected either directly to this port or indirectly through other cells to this port. If at least a neighboring cell of a port (other than the first port) is one among the cells connected to the initial port, then this port is also connected to the initial port. This process is repeated for all ports that are not the initial port. If for a particular port, the connectivity test has failed, then this port is not connected to at least one of the other ports. Therefore, the population containing such a port arrangement is discarded, and the test is started with a new population.

In this research, for GA parameters, ‘elitism’ as the selection method, two-point crossover, and modified adjustable mutation rate were used. The ‘elitism’ carries the best solutions across generations.

At the conclusion of each simulation step, the fitness of current generation is evaluated. The populations are ranked in order of fitness and the best 50% are chosen to form the next generation. Half of the next generation is created by performing crossover and mutation based on the populations selected from the current generation. The other half of the next generation is created by performing mutation on the same set of populations from the current generation. This technique allows good diversity of solutions to be maintained.

While the concept of elitism requires that the best solutions are carried unperturbed across generations, this procedure can lead to resimulation of the elite populations, which is wasteful. With the proposed technique, the next generation contains populations which have not been tested before, allowing for more trials of the search space. When the selection step of the next generation is being performed, once again, the

populations are ranked in order of fitness. This time, their fitness is compared with the elite from the previous generation. If the elite from the previous generation proves to be a better solution, they are chosen ahead of the best solution from the current generation.

Figure 3.5 illustrates the two-point crossover scheme with three populations. For populations consisting of equal to or less than 10 genes, a fixed mutation rate of 10% was used. For populations consisting of more than 10 genes, a mutation rate between 10% and 20% was used at random. By doing this, genetic diversity is maintained from one generation of populations to the next while preventing the GA from falling into local extremes.

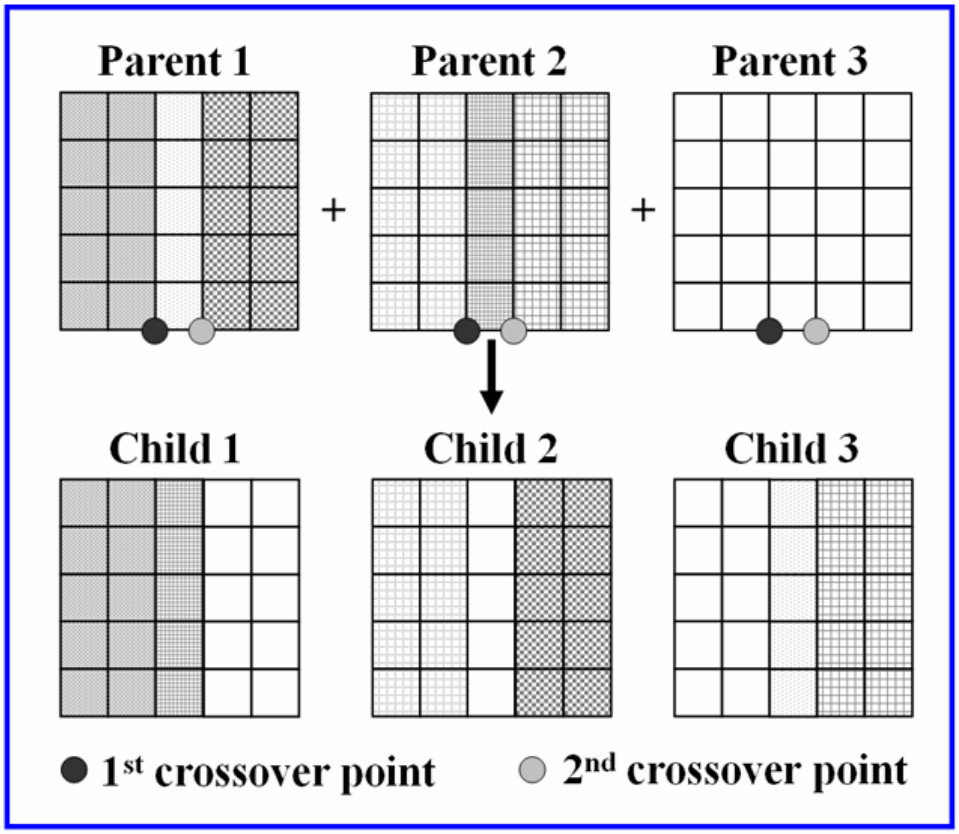


Figure 3.5: Illustration of two-point crossover scheme using three populations.

3.2.2 Dispersion Diagram (DD)

In the suggested method, dispersion diagram (DD) analysis was used to predict stop band frequency of the EBG structure. The main advantage of using DD is that the method only requires solving a unit cell of the periodic structure instead of the whole periodic structure to predict the stop band frequency.

Brillouin zone for two-dimensional (2-D) EBG structure with rectangular patches can be defined as shown in Figure 3.6. The behavior of the propagation vectors on the boundary of the Brillouin zone dictates the stopband and passband characteristic of the entire periodic structure. The importance of the Brillouin zone stems from the Bloch wave description of waves in a periodic medium, in which it is found that the solutions can be completely characterized by their behavior in a single Brillouin zone.

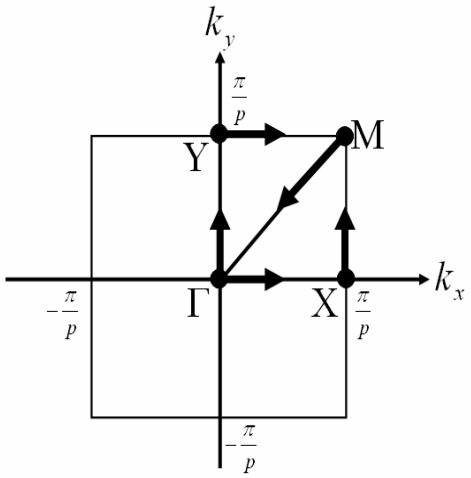


Figure 3.6: Brillouin zone for a square unit cell of size pxp mm^2.

For dispersion diagram analysis, an eigenvalue equation for two-dimensional (2-D) infinite periodic EBG structure was derived with a four-port network which is a unit cell of the 2-D infinite periodic structure [38]. Figure 3.7 shows port locations and the four-port network expressed by Z-parameter, which is calculated using M-FDM. When

input and output variables of the four-port network are defined as shown in Figure 3.7(b), the relationship between these variables can be written as:

$$\begin{pmatrix} \overline{V_I} \\ \overline{V_O} \end{pmatrix} = \begin{pmatrix} \overline{\overline{Z_{11}}} & \overline{\overline{Z_{12}}} \\ \overline{\overline{Z_{21}}} & \overline{\overline{Z_{22}}} \end{pmatrix} \begin{pmatrix} \overline{I_I} \\ \overline{I_O} \end{pmatrix} \tag{3.1}$$

where

$$\overline{\mathrm{V_I}} = \begin{pmatrix} \mathrm{V_1} \\ \mathrm{V_2} \end{pmatrix},\ \overline{\mathrm{V_O}} = \begin{pmatrix} \mathrm{V_3} \\ \mathrm{V_4} \end{pmatrix},\ \overline{\mathrm{I_I}} = \begin{pmatrix} \mathrm{I_1} \\ \mathrm{I_2} \end{pmatrix},\ \overline{\mathrm{I_O}} = \begin{pmatrix} \mathrm{I_3} \\ \mathrm{I_4} \end{pmatrix}. \tag{3.2}$$

The Z-matrix in Equation (3.1) can be converted to ABCD-matrix as

$$\begin{pmatrix} \overline{V_I} \\ \overline{I_I} \end{pmatrix} = \begin{pmatrix} \overline{\overline{A}} & \overline{\overline{B}} \\ \overline{\overline{C}} & \overline{\overline{D}} \end{pmatrix} \begin{pmatrix} \overline{V_O} \\ -\overline{I_O} \end{pmatrix} \tag{3.3}$$

where

$$\begin{pmatrix} \overline{\overline{A}} & \overline{\overline{B}} \\ \overline{\overline{C}} & \overline{\overline{D}} \end{pmatrix} = \begin{pmatrix} \overline{\overline{Z_{11}}} \cdot \overline{\overline{Z_{21}^{-1}}} & -\overline{\overline{Z_{12}}} + \overline{\overline{Z_{11}}} \cdot \overline{\overline{Z_{21}^{-1}}} \cdot \overline{\overline{Z_{22}}} \\ \overline{\overline{Z_{21}^{-1}}} & \overline{\overline{Z_{21}^{-1}}} \cdot \overline{\overline{Z_{22}}} \end{pmatrix} \tag{3.4}$$

By introducing the following vectors based on the direction of x and y,

$$\overline{\mathrm{X_I}} = \begin{pmatrix} \mathrm{V_1} \\ \mathrm{I_1} \end{pmatrix},\ \overline{\mathrm{X_O}} = \begin{pmatrix} \mathrm{V_3} \\ -\mathrm{I_3} \end{pmatrix},\ \overline{\mathrm{Y_I}} = \begin{pmatrix} \mathrm{V_2} \\ \mathrm{I_2} \end{pmatrix},\ \overline{\mathrm{Y_O}} = \begin{pmatrix} \mathrm{V_4} \\ -\mathrm{I_4} \end{pmatrix} \tag{3.5}$$

Equation (3.3) can be expressed as:

$$\begin{pmatrix} \overline{X_I} \\ \overline{Y_I} \end{pmatrix} = \begin{pmatrix} \overline{\overline{F_{11}}} & \overline{\overline{F_{12}}} \\ \overline{\overline{F_{21}}} & \overline{\overline{F_{22}}} \end{pmatrix} \begin{pmatrix} \overline{X_O} \\ \overline{Y_O} \end{pmatrix} \tag{3.6}$$

where

$$\overline{\overline{F_{ij}}} = \begin{pmatrix} \overline{\overline{A_{ij}}} & \overline{\overline{B_{ij}}} \\ \overline{\overline{C_{ij}}} & \overline{\overline{D_{ij}}} \end{pmatrix} \quad (i = 1,2,\ j = 1,2) \tag{3.7}$$

If the periodic structure is infinitely long, the voltages and currents at the output terminals of the unit cell should be different from the voltages and currents at the input terminals by only the propagation factor in the corresponding propagation direction. Therefore,

assuming the propagation factor $e^{-\gamma_x d_x}$ for the interval d_x in the +x direction and $e^{-\gamma_y d_y}$ for the interval d_y in the +y direction, we have

$$\left(\begin{pmatrix} \overline{\overline{F_{11}}} & \overline{\overline{F_{12}}} \\ \overline{\overline{F_{21}}} & \overline{\overline{F_{22}}} \end{pmatrix} - \begin{pmatrix} e^{\gamma_x d_x}\overline{\overline{I}} & 0 \\ 0 & e^{\gamma_y d_y}\overline{\overline{I}} \end{pmatrix}\right)\begin{pmatrix} \overline{X_O} \\ \overline{Y_O} \end{pmatrix} = 0 \tag{3.8}$$

where $\overline{\overline{I}}$ is a 2x2 unit matrix.

Equation (3.8) is a general eigenvalue equation for a 2-D infinite periodic EBG structure. A nontrivial solution for the output vectors exists only if the determinant of matrix in Equation (3.8) vanishes.

Once the network parameters in the eigenvalue equation are given, the equation can provide the relationship between phase constant (β) and frequency (*f*). The plot of β versus *f* is the dispersion diagram. The dispersion diagram shows stopband and passband characteristics of the EBG structure. Therefore, DD is used to predict stop band frequencies of EBG structures in the suggested method.

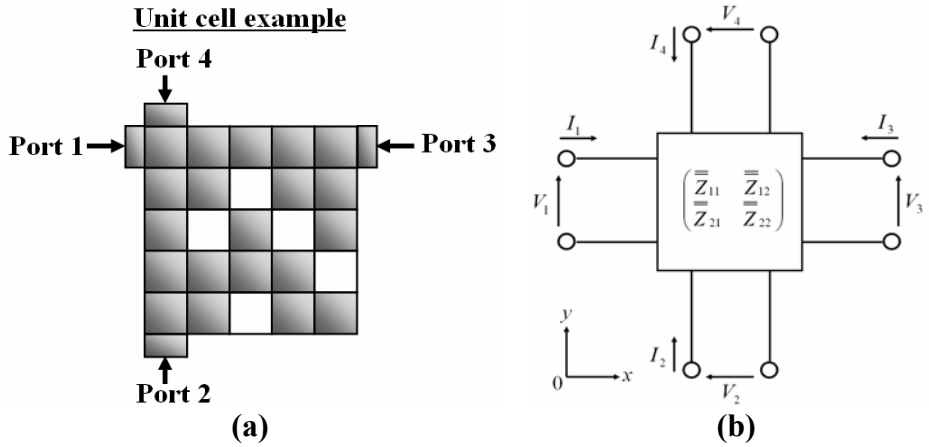


Figure 3.7: (a) Port locations for a unit cell and (b) Four-port network expressed by Z-matrix for the unit cell.

3.2.3 Multilayer Finite-Difference Method (M-FDM)

For Electromagnetic Band gap (EBG) structure synthesis, when populations expressed by binary sequences are generated by GA, the next step involves converting the binary sequences of patch shape outputs from the genetic algorithm into a set of coordinates for each patch shape member, as shown in Figure 3.8. Once converted, each patch shape of each population is solved with multilayer finite-difference method (M-FDM) [37].

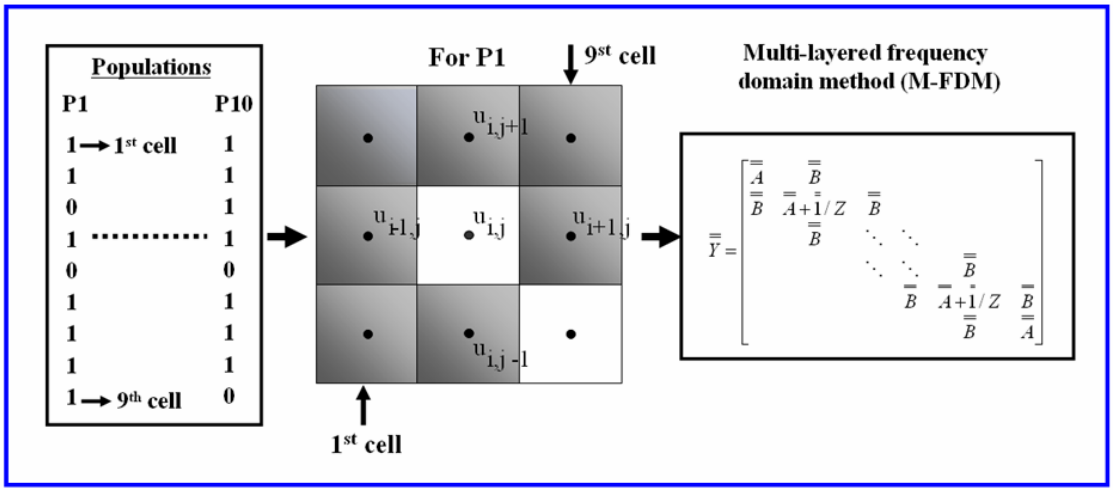


Figure 3.8: Illustration of the conversion of the binary sequences of populations into a set of coordinates for patch shapes for M-FDM solving.

M-FDM calculates the finite-difference solution of the Helmholtz equation. The underlying elliptic partial differential equation for the modeling of planes is a Helmholtz equation given by:

$$\left(\nabla_T^2 + k^2\right)u = -j\omega\mu d J_z \tag{3.9}$$

where ∇_T^2 is the transverse Laplace operator parallel to the planar structures, k is the wave number, u is the voltage, ω is the angular frequency, μ is the permeability, d is the distance between the planes, and J_z is the current density injected normally to the planes

[39]. Problem definition is completed by assigning homogenous Neumann boundary conditions, which correspond to assuming a magnetic wall, or an open circuit, on the periphery of the planes. The Helmholtz equation can be solved by applying the finite-difference scheme [37]. The finite-difference scheme can be represented by a finite-difference unit cell shown in Figure 3.9. The impedance (Z) and admittance (Y) for each of these unit cells can be expressed as

$$Z = R + j\omega L \tag{3.10}$$

$$Y = G + j\omega C \tag{3.11}$$

where the parameters can be calculated as

$$C = \frac{\varepsilon h^2}{d} \tag{3.12}$$

$$L = \mu d \tag{3.13}$$

$$R = \frac{2}{\sigma t} + 2\sqrt{\frac{j\omega\mu}{\sigma}} \tag{3.14}$$

$$G = \omega C \tan\delta \tag{3.15}$$

for a given permittivity ε, permeability μ, conductivity σ, conductor thickness *t*, loss tangent tanδ, and cell size *h*.

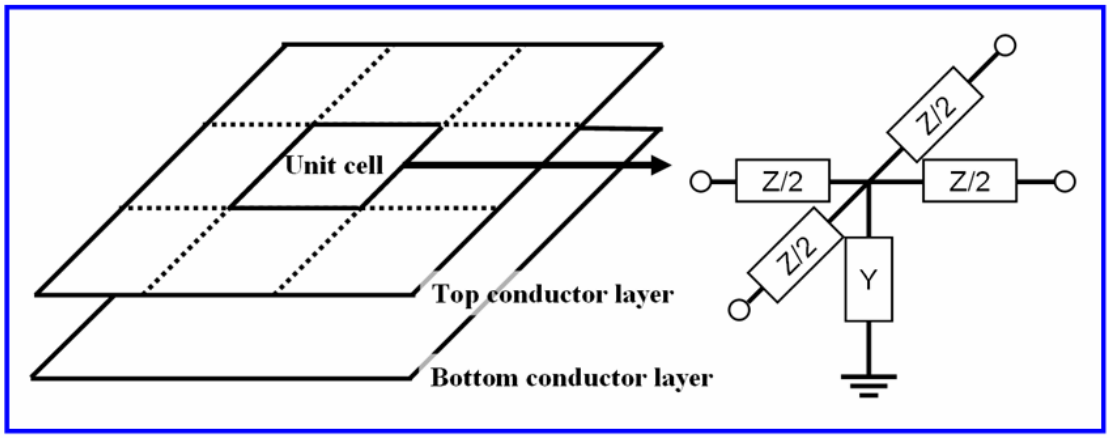


Figure 3.9: Finite-difference unit cell model for a single plane pair [37].

However, this formulation can be inaccurate for structures with narrow-width metal patches and slots in the metal plane, since fringe and gap fields are neglected.

Firstly, since branches connecting adjacent patches in EBG structures are narrow, these branches will be modeled inaccurately. In this case, the effect of fringing fields is significant compared to the parallel plate fields. Secondly, EBG structures typically contain a lot of gaps. The coupling between them is being neglected as formulated above. Therefore, fringe and gap models suggested in [40] were added to M-FDM to improve the accuracy of the suggested EBG synthesis method. These models are based on simple semi-empirical expressions and do not involve significant additional computational effort.

Finally, M-FDM is used to solve the following:

1) Each population, which is a unit cell, in terms of Z-parameters. The Z-parameters are linked to dispersion diagram (DD) to calculate stop band frequencies for the population.

2) An EBG structure being composed of the best unit cell in terms of Z-parameters. The Z-parameters are converted to S-parameters. The S-parameters are used to calculate isolation level over the stop band frequencies.

In this research, M-FDM is used; however any other computational method can also be used.

3.2.4 Generating the Total EBG Structure

When the best population (patch) meeting the input stop band specification is selected, the EBG structure is designed by arranging the patch in horizontal and vertical directions to find out the number of patches required to meet isolation level specification. At each step of increasing the number of patches, the EBG structure is solved in terms of Z-parameters with the M-FDM. The Z-parameters are converted to S-parameters. Transmission coefficient (S21) in dB is compared with the isolation level specification for the band gap frequencies. If the transmission coefficient of the EBG structure for the band gap frequencies is equal to or better than the isolation level specification, the

number of patches to meet the isolation level specification is determined for the final EBG structure.

In this research, the total number of populations is used to determine whether there is a solution for a given input specification or not. Even after a thousand populations, if a solution meeting the input design specification is not found, it is assumed that the input specification has no solution. The best population among the thousand populations will be a solution for the input design specification. To test the existence of a solution, a thousand populations have been used in this research. However, the number of populations for the test can be also defined by users.

3.3 Results

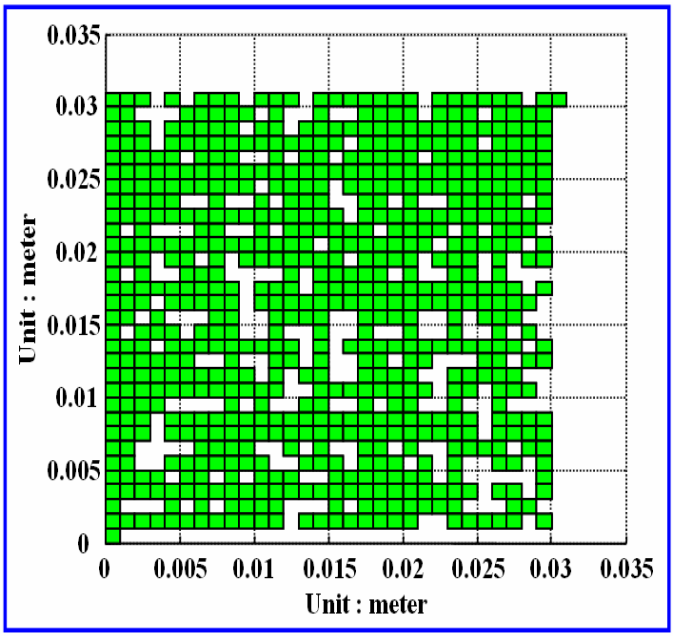
In order to verify the EBG synthesis method suggested in this Chapter, the suggested method has been implemented using MATLAB. EBG structures designed by the synthesizer have been modeled and simulated using multilayer finite-difference method (M-FDM). The EBG structures were also fabricated and measured for verification.

3.3.1 Simulation Results

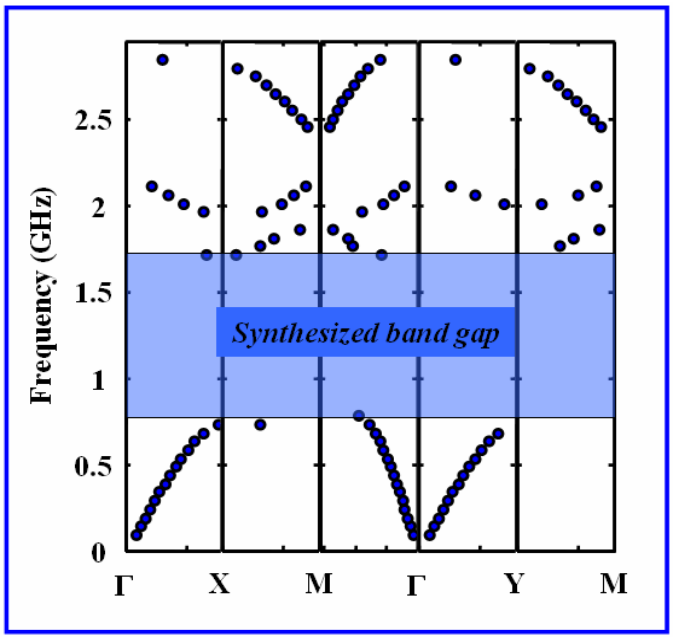
To verify the suggested method, three examples have been designed using the EBG synthesizer for three different input specifications: 1) EBG structure meeting a band gap specification (700MHz ~ 1.8GHz), 2) EBG structure satisfying band gap (2.2GHz ~ 3.6GHz) and isolation level (50dB) specification, and 3) EBG structure satisfying a wide band gap (4.5GHz ~ 9GHz) and high isolation (100dB) level.

1) Band gap (700MHz ~ 1.8GHz)

First, an EBG structure was designed for an on-set frequency of 700MHz and off-set frequency of 1.8GHz. The on-set frequency is the starting frequency of the band gap, and the off-set frequency is the ending frequency of the band gap. Tolerance of 200MHz was used for this design. The tolerance is used to determine how much deviation from the desired on-set frequency and off-set frequency are acceptable. For this target design, 300μm thick FR4 as dielectric material, 35μm thick copper as conductors, and a patch size of 30mm x 30 mm were used. The synthesized patch shape and dispersion diagram are shown in Figure 3.10(a) and 3.10(b) respectively. As shown in Figure 3.10(b), a band gap from 700MHz ~ 1.8GHz was achieved as per the initial design specification. The deviation from the desired stop band is less than 200MHz as per the initial tolerance. To verify the synthesized patch shape in frequency-domain, six patches shown in Figure 3.10(a) were arranged in a 2x3 array as shown in Figure 3.11. Figure 3.12 shows the modeled and simulated results of the EBG structure shown in Figure 3.11. Port locations for the simulation are shown in Figure 3.11. As shown in Figure 3.12, the modeled and simulated results of the EBG structure with M-FDM exhibit a band gap from 700MHz to 1.8GHz as per the initial EBG design specification. Figure 3.11 shows the voltage distribution for the EBG structure at a frequency (1.35GHz) within the band gap (700MHz ~ 1.8GHz) when port1 is excited. The voltage distribution is proportional to transfer impedance (Z_{21}) between port1 and other locations when port1 was excited with a current source of 1A. The transfer impedance is a measure of the amount of coupled noise from an aggressor (port1) to a victim. Higher level of voltage distribution means more noise coupling from the aggressor (port1) to the location. As shown in Figure 3.11, there is no coupling within the band gap, and the excited noise is confined within the patch. Finally, it proves that the EBG structure effectively isolates noise coupling within the band gap.



(a)



(b)

Figure 3.10: For on-set frequency of 700MHz and off-set frequency of 1.8GHz (a) the synthesized patch shape and (b) dispersion diagram plot of the synthesized patch shape in (a).

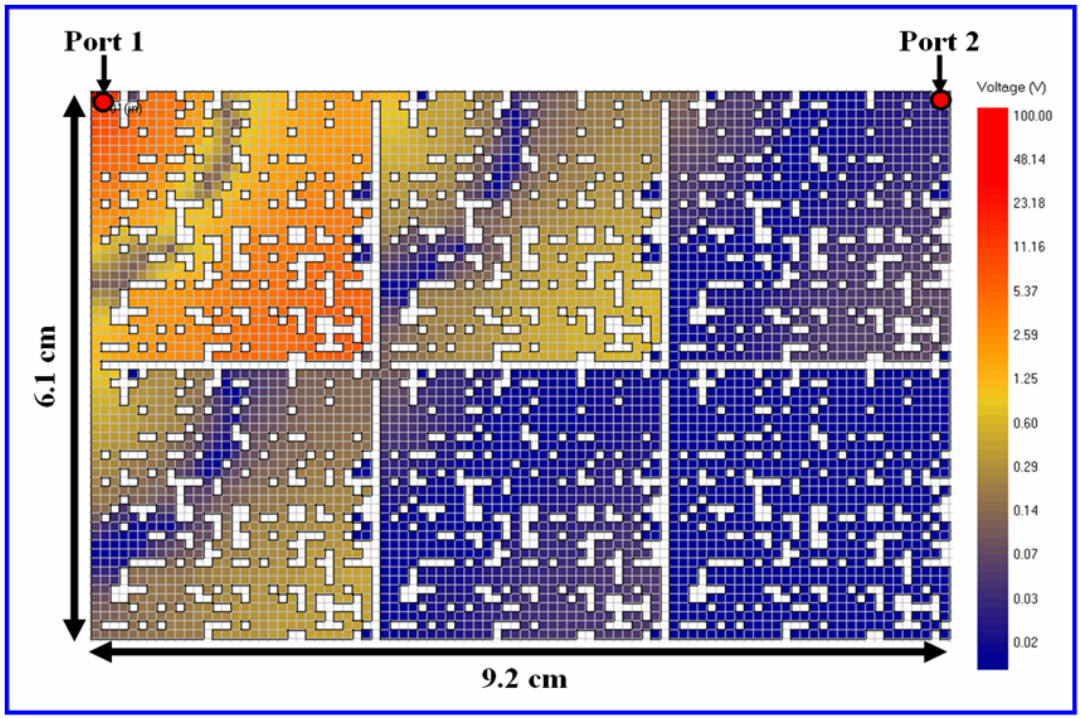


Figure 3.11: Voltage distribution at 1.35GHz for an EBG structure consisting of a 2x3 array of the synthesized patch shown in Figure 3.10(a) when port 1 was excited.

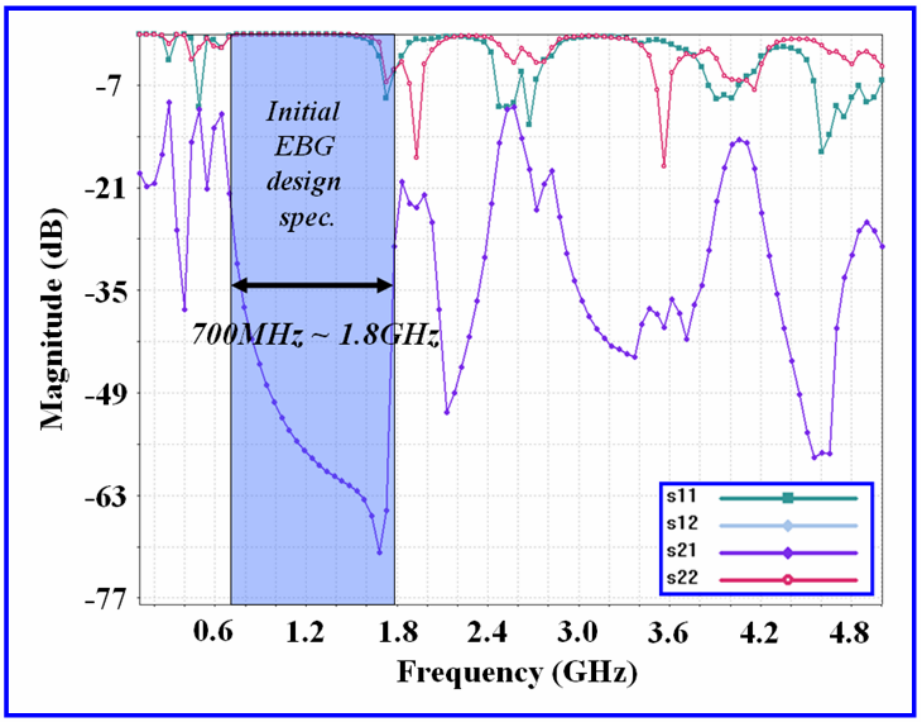
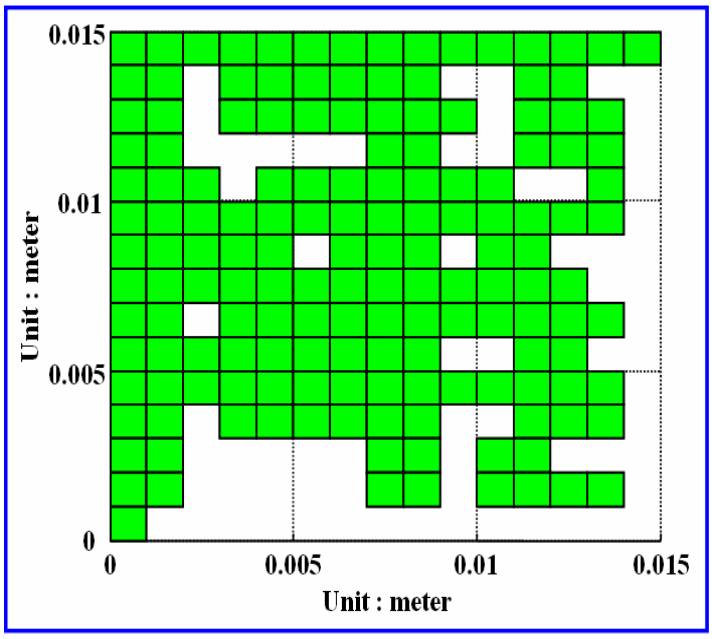


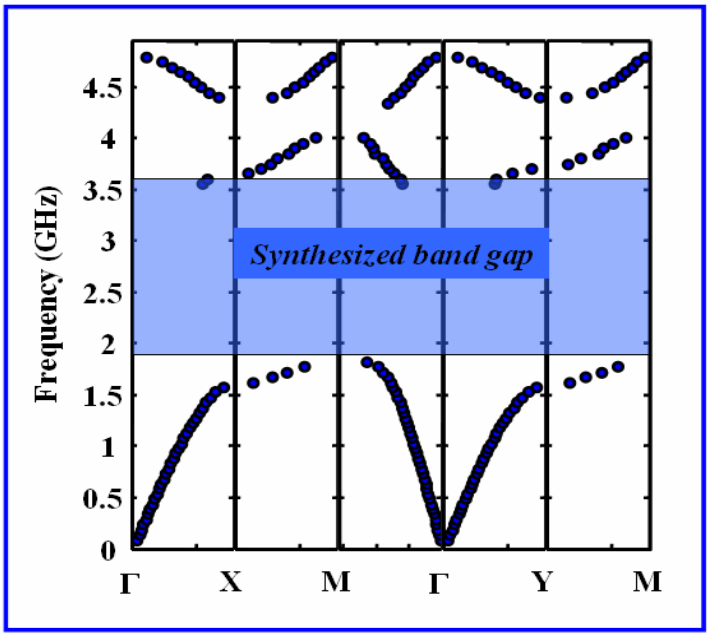
Figure 3.12: Modeled and simulated S-parameter results of the EBG structure in Figure 3.11 with M-FDM.

2) Band gap (2.2GHz ~ 3.6GHz) and Isolation Level (50dB)

Second, an EBG structure was designed for an on-set frequency of 2.2GHz, off-set frequency of 3.6GHz, and at least 50dB isolation over the stop band (2.2GHz ~ 3.6GHz). Tolerance of 300MHz was used for this design. The same conductor and dielectric material as the first design was used for this design. Like in the first design, 300μm thick FR4 as dielectric material and 35μm thick copper as conductor were used. For this design, a patch size of 14mm x 14mm was used. The synthesized patch shape and dispersion diagram are shown in Figure 3.13(a) and 3.13(b) respectively. As shown in Figure 3.13(b), a band gap from 2.2GHz ~ 3.6GHz was achieved as per the initial design specification. The deviation from the desired stop band is less than 300MHz as per the initial tolerance. Figure 3.13(c) shows the final EBG structure being made up of the synthesized patch shape shown in Figure 3.13(a). To achieve the initial isolation target which is at least 50dB over the band gap (2.2GHz ~ 3.6GHz), at least 5 unit cells are required in either horizontal or vertical direction depending on the direction along which the isolation is needed, as shown in Figure 3.13(c). Figure 3.13(d) shows the modeled and simulated results of the EBG structure shown in Figure 3.13(c) with M-FDM. For this simulation, two ports were placed as shown in Figure 3.14. As shown in Figure 3.13(d), the modeled and simulated results for the synthesized EBG structure with M-FDM shows that the synthesized EBG structure with the EBG synthesizer meets the EBG design specification. Figure 3.14 shows voltage plots for the EBG structure shown in Figure 3.13(c) at 3.1GHz when port1 was excited. As shown in Figure 3.14, no coupling exists within the band gap.

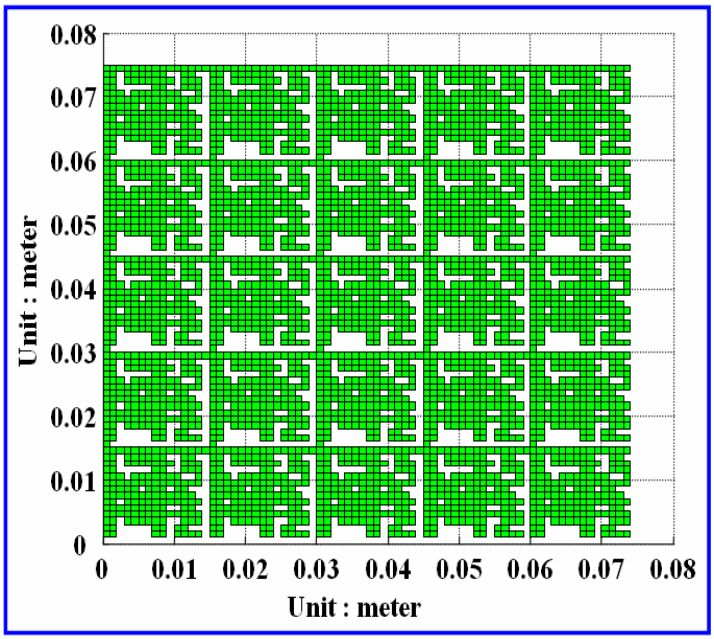


(a)

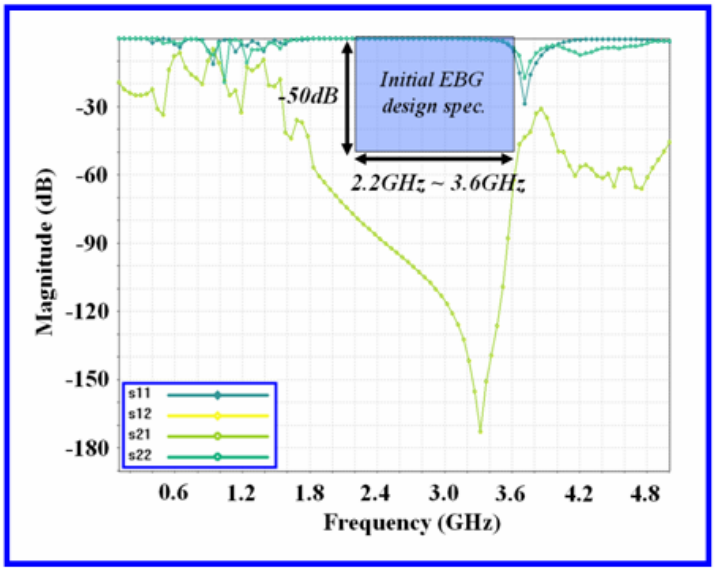


(b)

Figure 3.13: For on-set frequency of 2.2GHz, off-set frequency of 3.6GHz, and minimum isolation of 50dB (a) the synthesized patch shape, (b) dispersion diagram plot of the synthesized patch shape in (a), (c) the final EBG structure being made up of the synthesized patch shape in (a), and (d) modeling results of the final EBG structure in (c).



(c)



(d)

Figure 3.13: Continued.

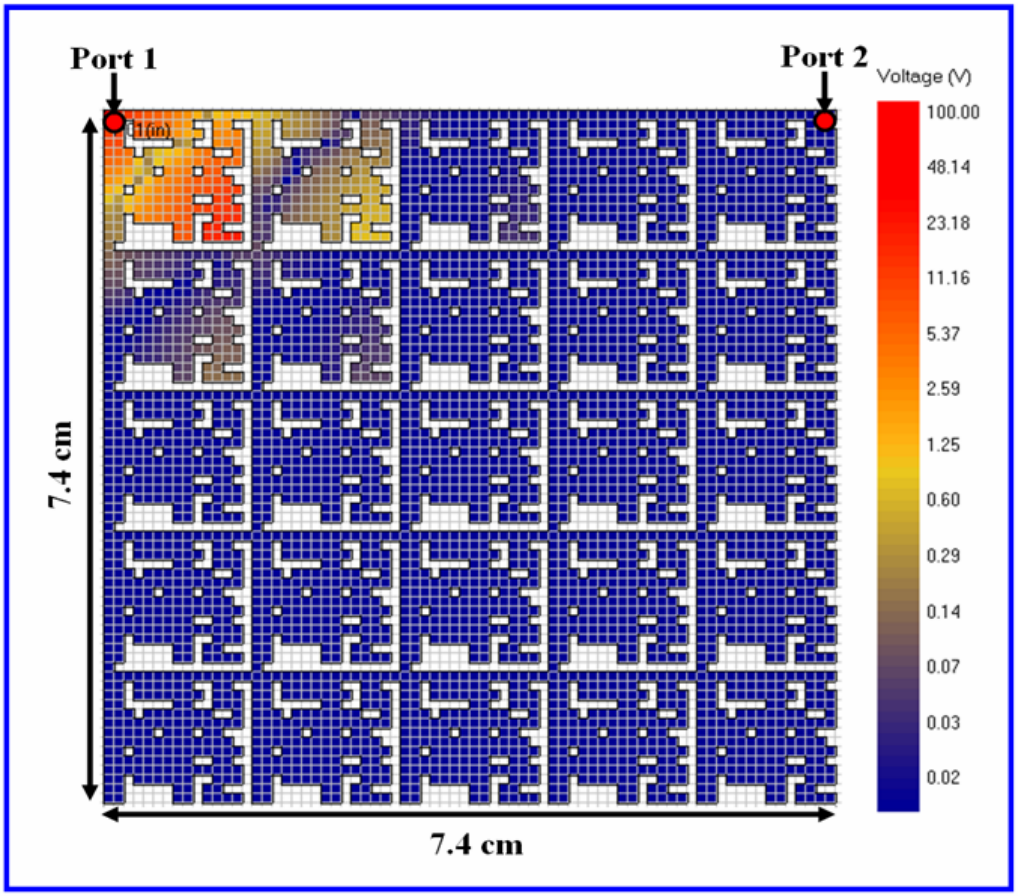


Figure 3.14: Voltage distribution at 3.1GHz when port 1 was excited for the EBG structure in Figure 3.13(c).

3) Band gap (4.5GHz ~ 9GHz) and Isolation Level (100dB)

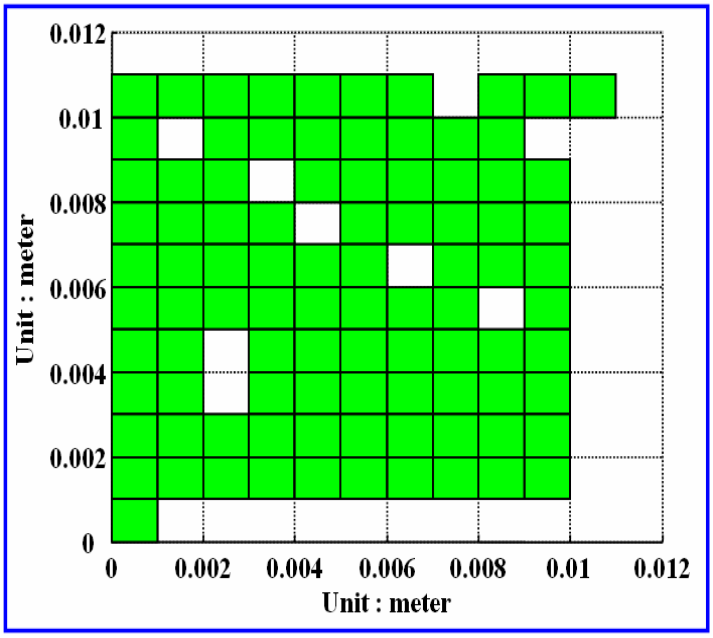
Third, a wide band gap and high isolation EBG structure was designed with the synthesizer tool. For the wide band gap and high isolation structure, copper was used as conductor like in the first and second design. A material (ECCOSTOCK LoK from EMERSON & CUMING MICROWAVE PRODUCTS) which has permittivity of 1.7, loss tangent of 0.004, and 100μm thick was used as a dielectric material. The EBG structure was designed for a stop band from 4.5GHz ~ 9GHz and 100dB isolation over the band gap. For the design, 500MHz was used for the tolerance. A patch size of 10mm

x 10mm was used for the design. Figure 3.15 shows the synthesized patch shape, dispersion diagram plot for the synthesized patch, and the final EBG structure. As shown in Figure 3.15(b), the synthesized patch shows a band gap from 4.5GHz ~ 9GHz as per the initial specification. Figure 3.15(d) and Figure 3.16 shows the modeled and simulated results for the EBG structure and voltage distribution at a frequency of 8.5GHz within the band gap respectively. Port locations for the simulation result in Figure 3.15(d) are shown in Figure 3.16. To achieve 100dB isolation over the band gap as per the input specification, seven unit cells are needed in the direction along which the isolation is required, as shown in Figure 3.15(c).

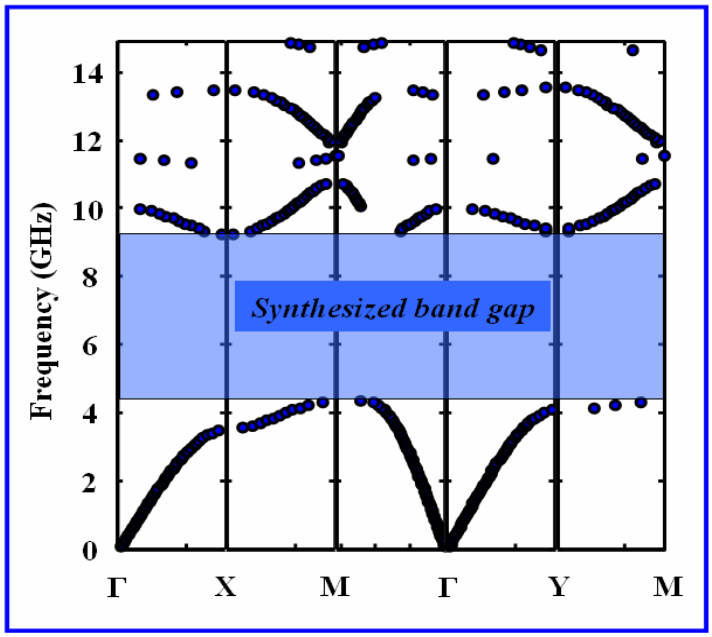
Table 1 summarizes the dielectric and conductor material information, EBG design specifications, and simulation time for the three design examples.

Table 3.1: Summary of material information, EBG design specifications, and simulation time for three design examples in Figure 3.10, 3.13, and 3.15.

		Example 1 (Figure 14)	Example 2 (Figure 17)	Example 3 (Figure 19)
Dielectric	tan δ	0.02	0.02	0.004
	ε_r	4.4	4.4	1.7
	t	300μm	300μm	100μm
Conductor	σ	5.8e7 S/m	5.8e7 S/m	5.8e7 S/m
	t	35μm	35μm	35μm
EBG design Spec.	band gap	700MHz ~ 1.8GHz	2.2GHz ~ 3.6GHz	4.5GHz ~ 9GHz
	isolation	N/A	50dB	100dB
	tolerance	200MHz	300MHz	500MHz
	patch size	30mm x 30mm	14mm x 14mm	10mm x10 mm
	branch size	1mm x 1mm	1mm x 1mm	1mm x 1mm
Time (sec)		6395	1048	2032

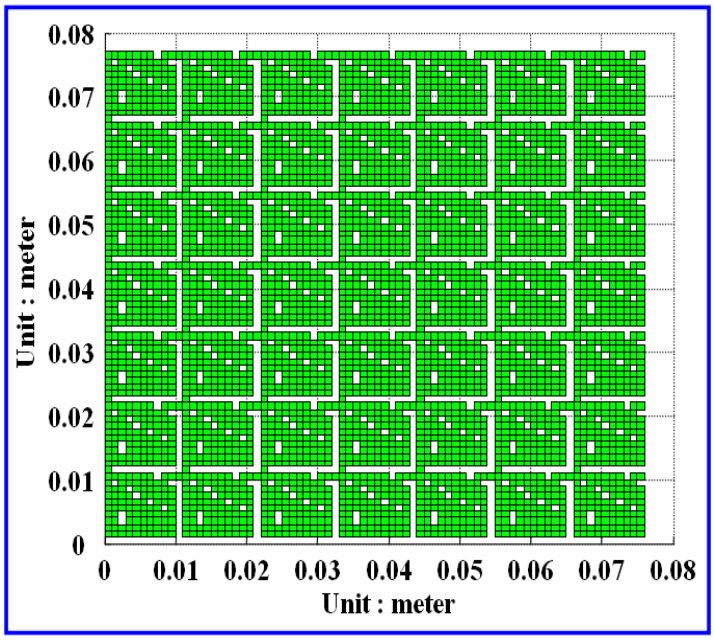


(a)

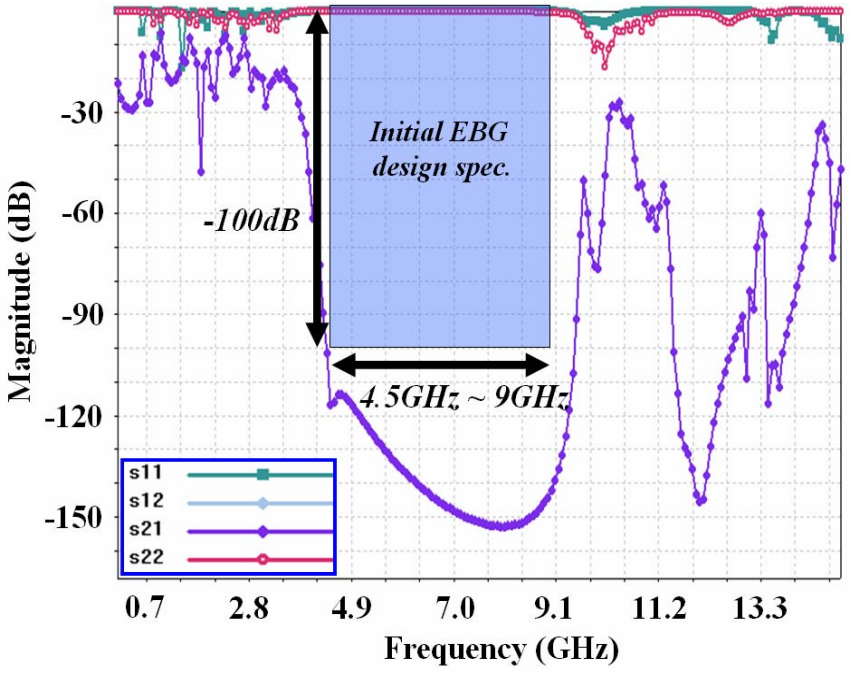


(b)

Figure 3.15: For on-set frequency of 4.5GHz, off-set frequency of 9GHz, and minimum isolation of 100dB (a) the synthesized patch shape, (b) dispersion diagram plot of the synthesized patch shape in (a), (c) the final EBG structure being made up of the synthesized patch shape in (a), and (d) modeling results of the final EBG structure in (c).



(c)



(d)

Figure 3.15: Continued.

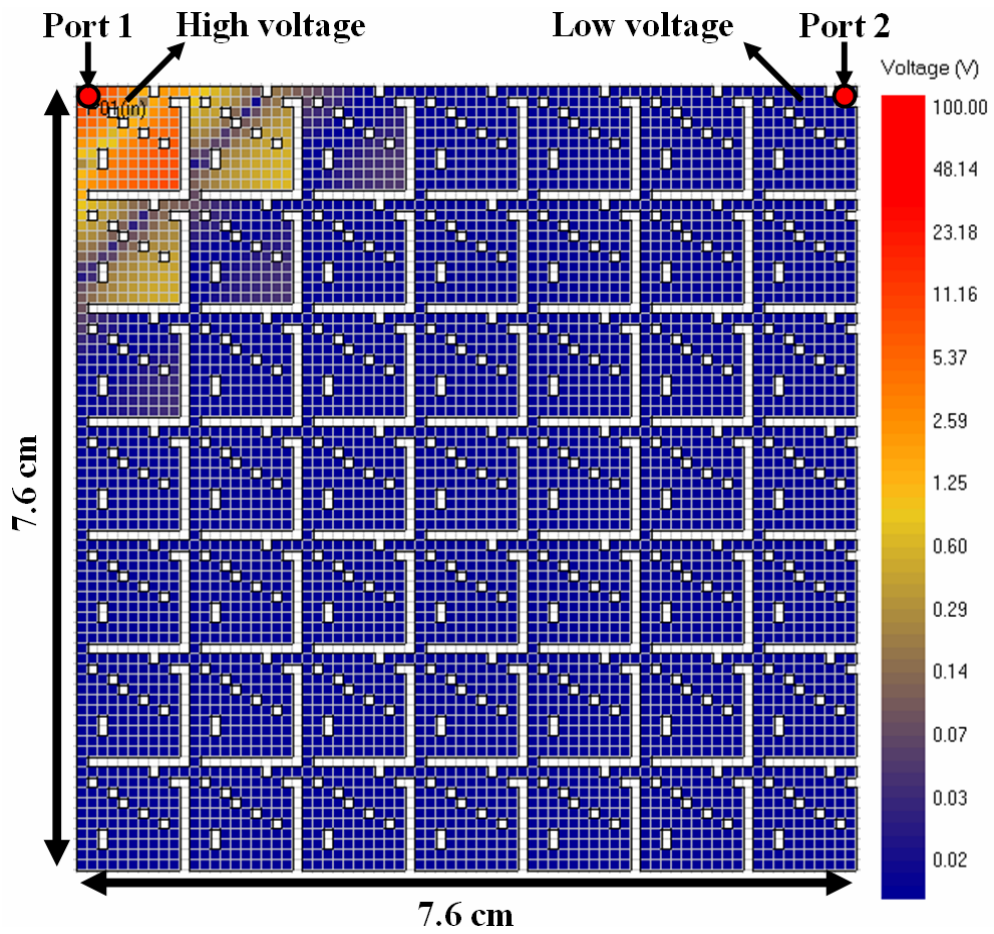


Figure 3.16: Voltage distribution at 8.5GHz when port 1 was excited for the EBG structure in Figure 3.15(c).

3.3.2 Model to Hardware Correlation

For verifying the designed EBG structures, EBG structures synthesized in Figures 3.10 and 3.13 were fabricated using standard FR4 processes. For the synthesized patch shape shown in Figure 3.10, six patches were arranged in a 2x3 array as shown in Figure 3.17. For the synthesized patch shape shown in Figure 3.13, twenty patches were arranged in a 4x5 array as shown in Figure 3.19. The photos of the fabricated EBG structures are shown in Figure 3.17 and 3.19. Two-port frequency domain measurements

were carried out for the fabricated EBG structures using a PNA Series Network Analyzer (E8363B) from Agilent Technologies. The locations of port 1 and port 2 for the measurements are shown in Figure 3.17 and 3.19. Figure 3.18 and 3.20 shows S-parameter results for the fabricated EBG structures shown in Figure 3.17 and 3.19. As shown in Figure 3.18 and 3.20, the frequency domain results of the fabricated EBG structures exhibit band gaps as per the design specifications shown in Table 3.1.

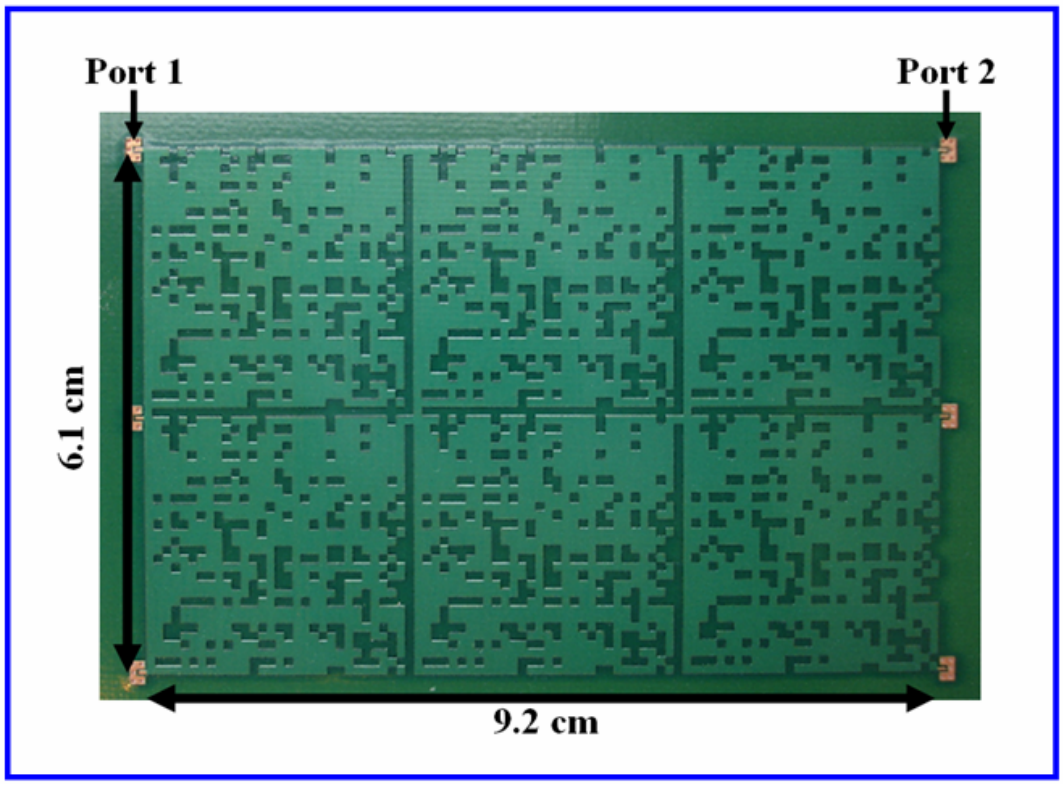


Figure 3.17: A photo of the fabricated EBG structure: six patches shown in Figure 3.10(a) are arranged in a 2x3 array.

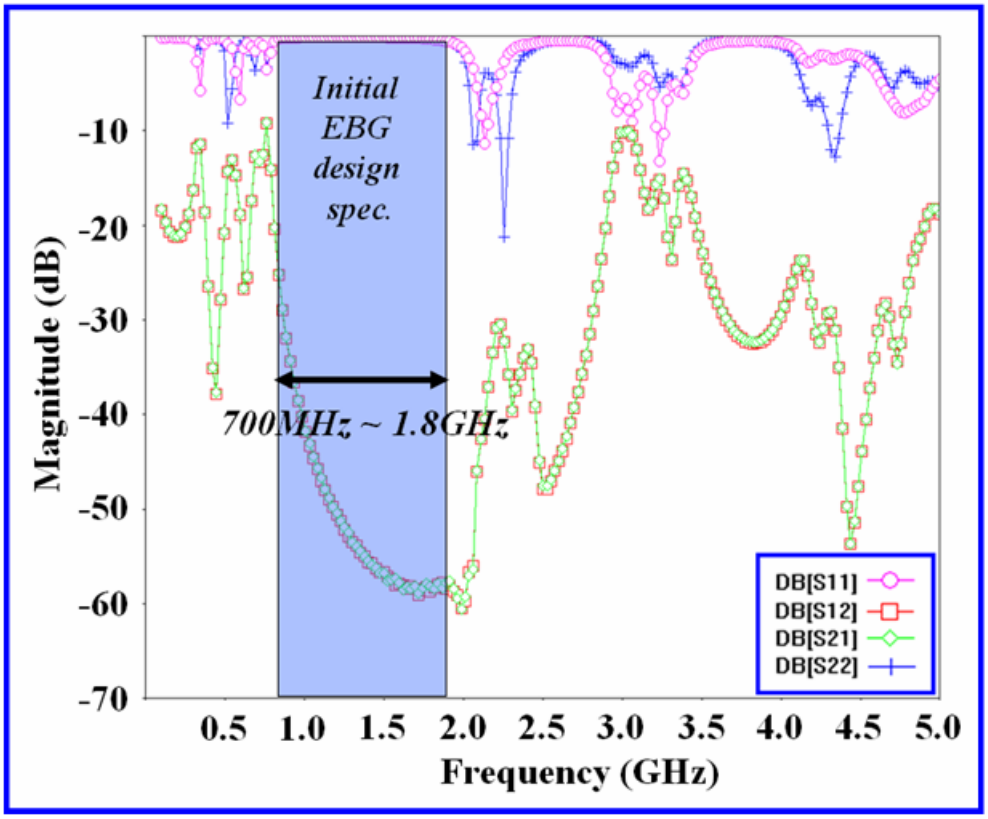


Figure 3.18: Measured S-parameter for the EBG structure shown in Figure 3.17.

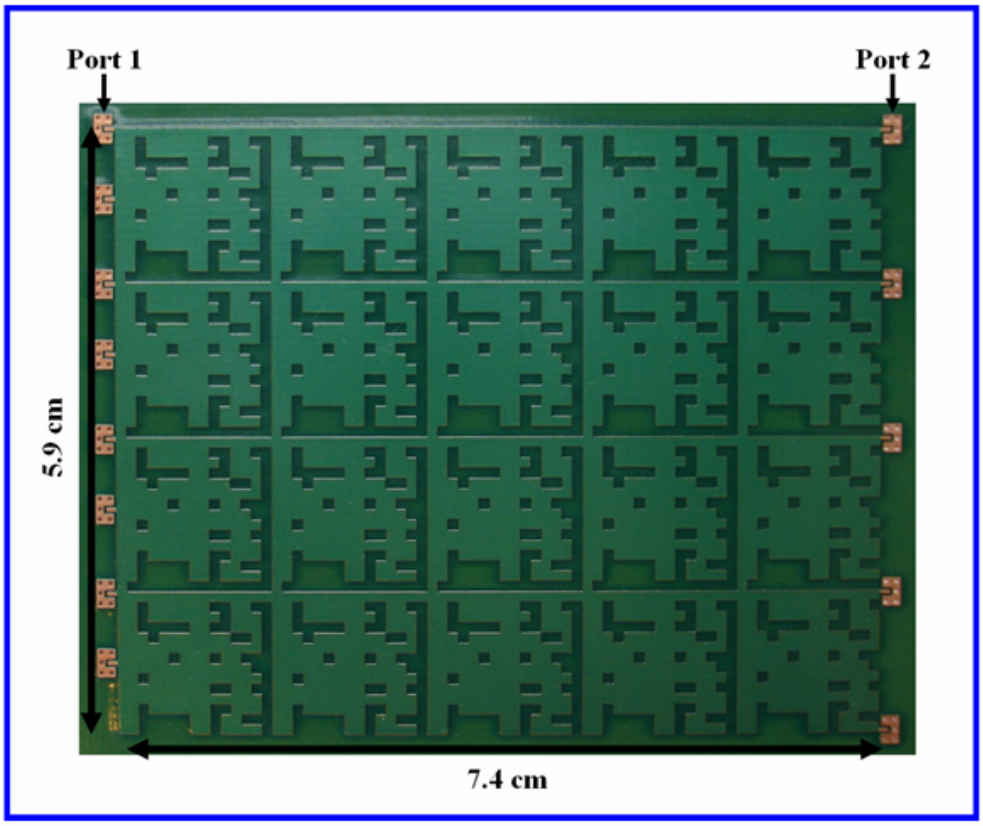


Figure 3.19: A photo of the fabricated EBG structure: twenty patches shown in Figure 3.13(a) are arranged in a 4x5 array.

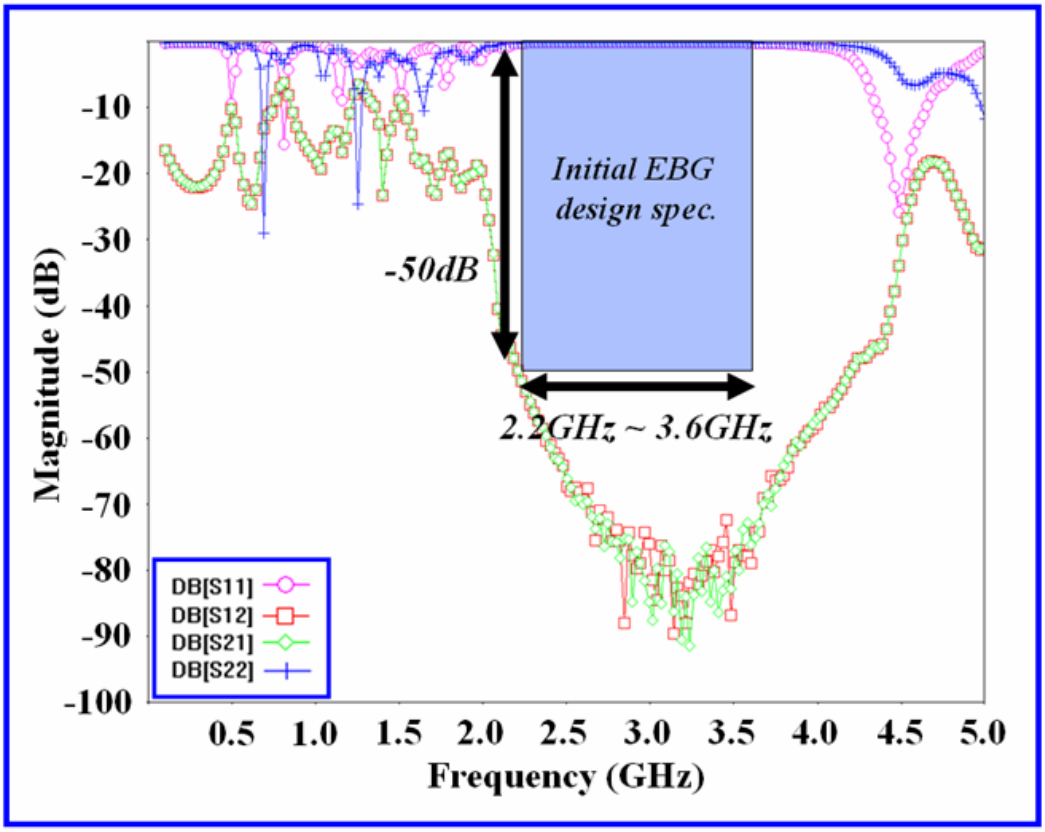


Figure 3.20: Measured S-parameter for the EBG structure shown in Figure 3.19.

3.4 Summary

With increasing clock frequencies and demand for low supply voltages, today's mixed signal systems are very sensitive to power/ground noise. In addition, with convergence toward mixed signal systems, supplying stable voltages to integrated circuits and blocking noise coupling are major bottlenecks. Therefore, better isolation techniques are required for today's mixed signal technology. Since electromagnetic band gap (EBG) structures act like filters, EBG structures are being used for noise isolation in mixed

signal systems. However, despite the potential benefits of EBG structures, there has been no synthesis tool for EBG structures proposed so far.

In this Chapter, a novel EBG synthesis method was introduced to design EBG structures for a given set of design specifications. The method took advantage of parallel solution-searching technique [47] in a huge solution space by utilizing a genetic algorithm (GA) as a problem-solving technique. By using modified GA, the method ensured continuity in the current paths and connectivity between ports. The method automated the synthesis process by combining genetic algorithm, multilayer finite-difference method, and dispersion diagram analysis method together. To verify the suggested method, an EBG synthesizer was implemented in MATLAB based on the suggested method. EBG structures were designed with the synthesizer for various EBG performance specifications. The designed EBG structures were simulated and measured in frequency domain. The simulated and measured frequency domain results exhibited band gaps as per the initial design specifications.

CHAPTER 4

SIMULTANEOUS SWITCHING NOISE (SSN) EFFECTS ON ANALOG-TO-DIGITAL CONVERTERS

Analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) are among the most ubiquitous and sensitive devices in mixed-signal systems. These data converters have been thought of as the central cores of wireless-infrastructure systems. Complex signals must be digitized upon reception and converted to analog signals for transmission. To meet the needs of present and future-generation wireless-infrastructure systems, ADCs and DACs must perform at RF rates and with outstanding linearity [41]. Therefore, the current trend for ADCs is toward obtaining high-speed and high-resolution. This trend makes ADCs more sensitive to noise because of the reduction in noise and timing margin. Hence, the characterization and testing of these devices require load boards with negligible path loss and noise. A load-board is used to interface a device under test to the automatic test equipment (ATE) while evaluating the device. It is an integral part of the test environment to accurately evaluate the device. Therefore, the design of these load boards becomes critical at gigahertz frequencies where high frequency electromagnetic effects can cause excessive path loss and noise because of the distributed behavior of the interconnections. Finally, for the accurate characterization and testing of current high-speed and high-resolution ADCs, the reduction of switching noise on the load board is very important. In this Chapter, simultaneous switching noise (SSN) effects on ADCs are discussed. Noise sources existing on the load board are studied.

4.1 Trend in Analog-to-Digital Converters (ADCs)

For over 20 years, the development of ADC technologies has always been driven by emerging applications. To meet the needs of present and future-generation wireless communication systems, high-speed and high-resolution ADCs have been required. To meet the requirements for high-speed and high resolution ADCs, a variety of ADC structures have been developed. Flash ADCs specialize in very high sampling rates but achieve poor linearity for high resolutions. On the other hand, sigma-delta ADCs enjoy much better linearity with high resolutions but suffer in their maximum effective sampling rate. Therefore, sigma-delta ADCs are desired for high resolution with low speeds, while flash ADCs are used for the exact opposite purpose. SAR, pipeline, and other structures fill in the midrange demands for speed (flash) and resolution (sigma-delta), achieving decent speeds and decent resolutions.

Historical [46] and current trends in sampling speed and number of bits (resolution) are shown in Figure 4.1. As shown in Figure 4.1, higher than 1Gsps and more than 20bits of ADCs are required in 2007. With the demand for higher speed and resolution, the characterization and testing of these devices require load boards with negligible loss and noise. The load-board is used to interface a device under test (DUT) to the automatic test equipment (ATE) while evaluating the DUT. It is an integral part of the test environment to accurately evaluate the DUT. Therefore, the design of load boards becomes a challenge to accurately evaluate high-speed and high-resolution ADCs.

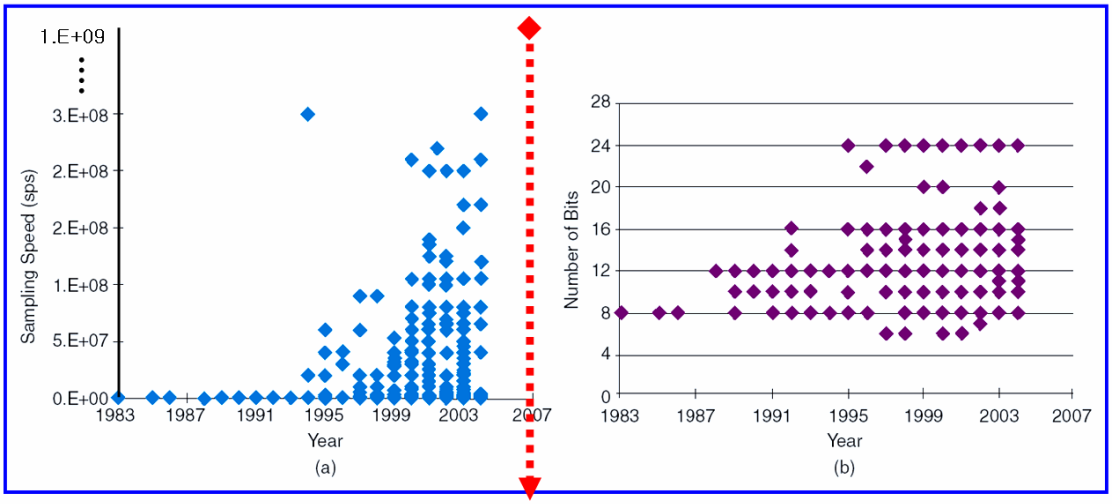
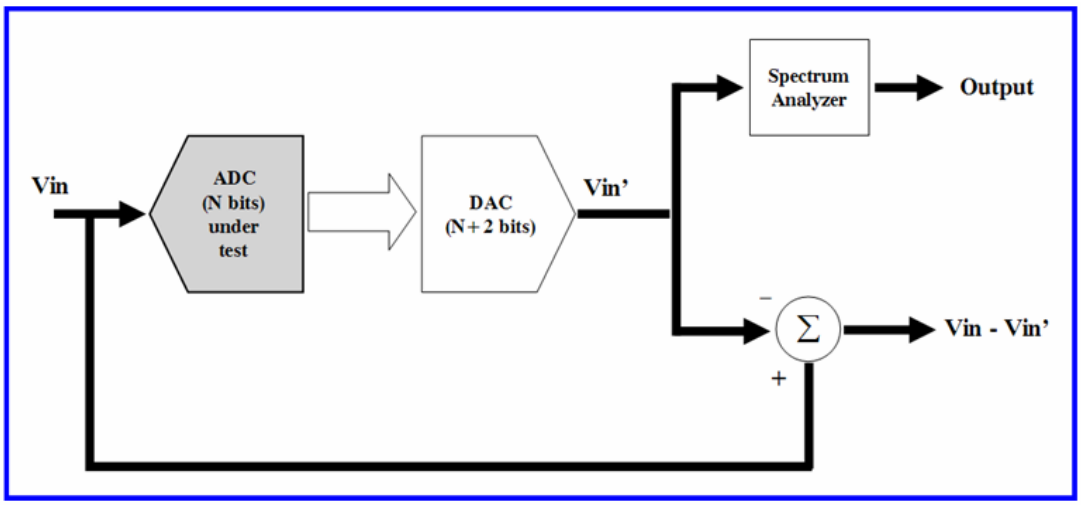


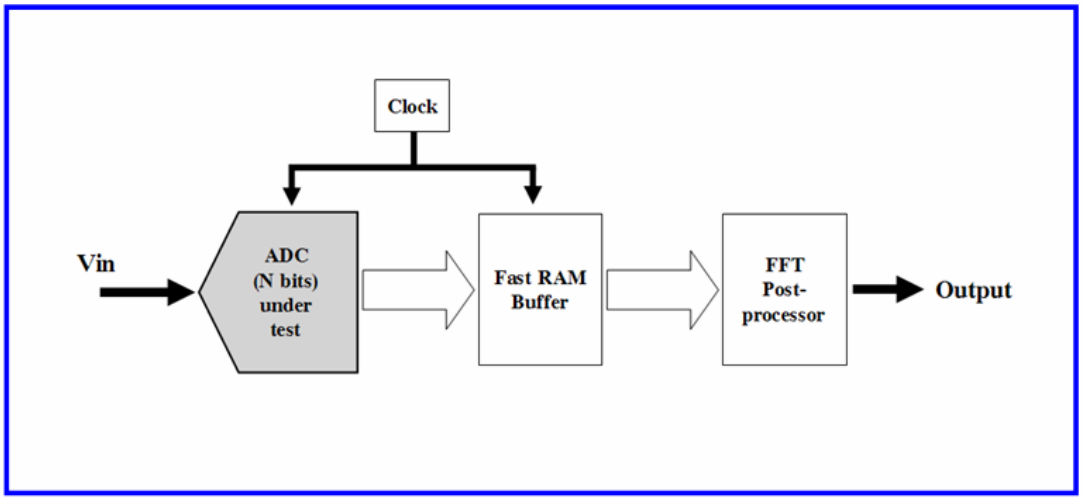
Figure 4.1: Historical and current trends in (a) sampling speed and (b) number of bits (resolution).

4.2 Switching Noise Sources Existing on an ADC Load Board

In ADC load boards, switching noise sources can be categorized into two sources: external noise source and internal noise source. There are two common ways to measure ADC characteristics. One is input-output testing and the other is fast fourier transform (FFT) based test, as shown in Figure 4.2 [42]. In the input-output test, an external clock generator is needed for ADC and DAC if the ADC and DAC use external clock inputs. Here, the clock generator can be considered as the external noise source. In the FFT-based testing, an external clock generator and large digital blocks are needed for storing and converting ADC output using the fast fourier transform. Here, the clock generator can be considered as the external noise source. In both cases, the digital part of the ADC can be considered as the internal noise source with an internal clock generator if the ADC used the internal clock generator instead of external one.



(a)



(b)

Figure 4.2: (a) Input-output test (b) fast fourier transform (FFT) based test.

Finally, there are two switching noise sources, such as internal noise sources and external noise sources, existing on the ADC load board, as shown in Figure 4.3. These can generate the switching noise on the test board, and the generated switching noise will affect the functionality of analog parts of the ADC. Therefore, both external and internal noise sources should be controlled carefully in high-speed and high-resolution ADC test boards.

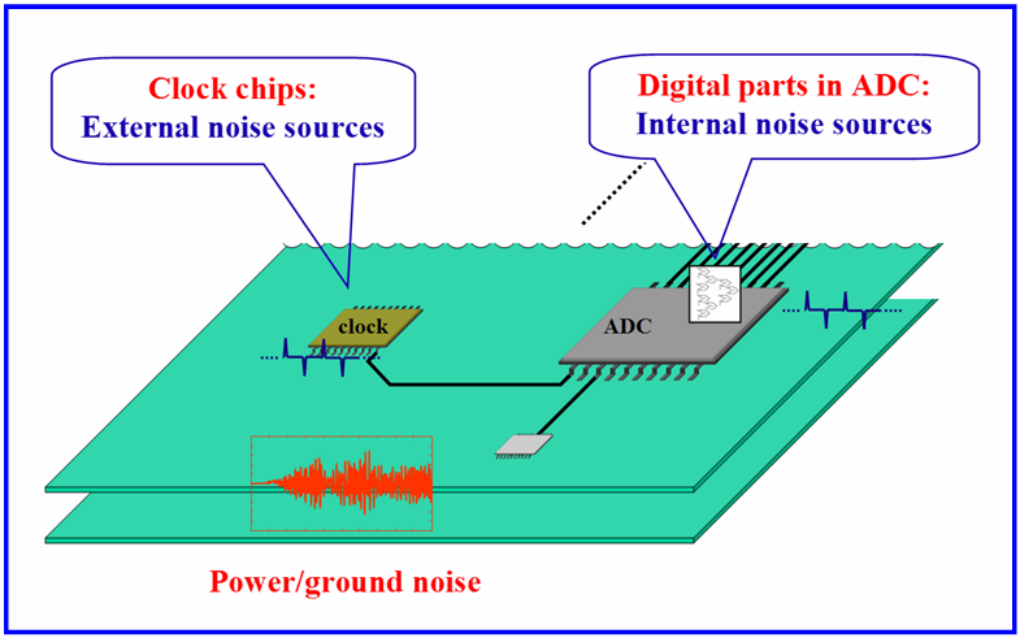


Figure 4.3: Sources for switching noise (power/ground noise) on a high-speed and high-resolution ADC load board.

4.3 Simultaneous Switching Noise Effects on ADC Performance

Figure 4.4 shows the switching noise effects on ADC performance. The switching noise can affect four main parts of ADCs: i) reference voltage, ii) input voltage, iii) sampling clock, and iv) comparator. The reference voltage defines the range of voltage inputs and therefore the size of the least significant bit (LSB). For an N-bit converter, the LSB is defined as

$$\frac{\text{Full} - \text{scale voltage}}{2^N} \tag{4.1}$$

The full-scale voltage range may not always be V_{REF}, depending on the particular ADC. But regardless of how the output codes are mapped, they are directly influenced by the value of V_{REF}. Needless to say, the outputs of ADC will be directly affected by the value of V_{IN}.

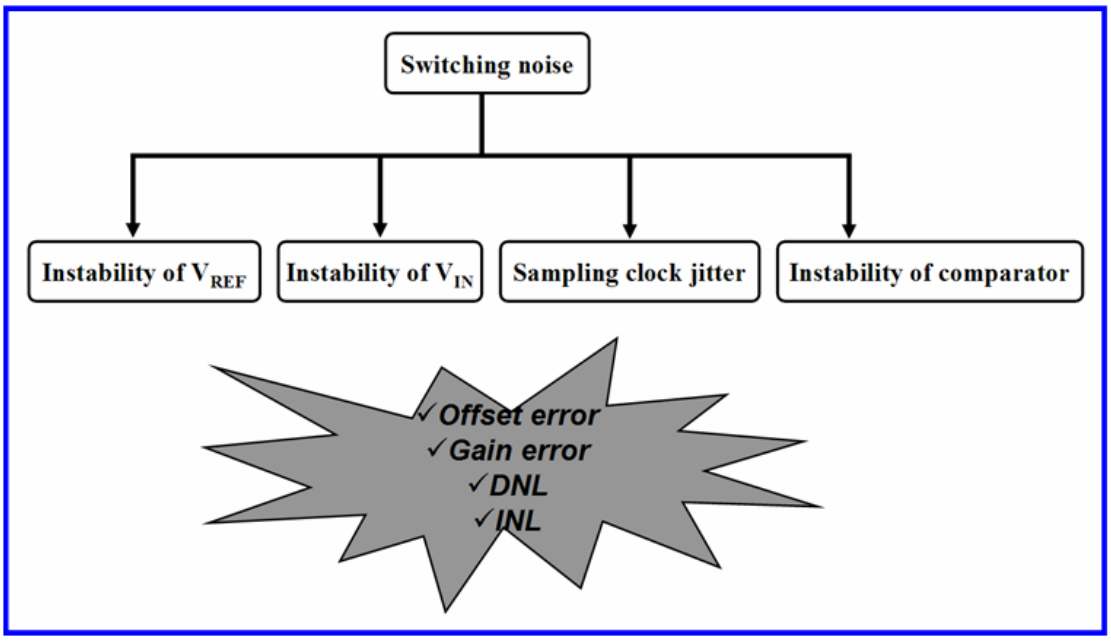


Figure 4.4: Switching noise effects on ADC performance.

If jitter resulting from the switching noise is present in the sampling clock of an ADC, the sample values are taken either a little too early or a little too late. Similarly, clock jitter in a DAC causes the sample values to be converted to analog signals at the wrong time. The result is the distortion of the waveform and the creation of spurious components related to the jitter frequency. The errorless operation of comparators can be guaranteed only under a noise-free environment.

Finally, the switching noise results in the instability of V_{REF}, the instability of V_{IN}, the sampling clock jitter, and the instability of comparator. These cause offset error, gain error, and nonlinearity on ADC. These also result in reduced signal-to-noise ratio (SNR) and effective number of bits (ENOB).

4.4 ADC Performance Modeling in the Presence of SSN

To simulate ADC performance in the presence of switching noise, a four-layer load board, which is 30 cm x 25 cm, was assumed. The test board consists of top signal, power plane, ground plane, and bottom signal. Copper with conductivity of 5.8×10^7 S/m was used for power and ground planes. FR4 with relative permittivity of 4.5 was used as a dielectric material. The height of the dielectric between the power and ground plane is 4.8 mils. Vias connecting ADC pins to the power/ground plane are assumed as short circuit for simplicity. Port1 and port2 were located at (5 cm, 10 cm) and at (25 cm, 15 cm) respectively, as shown in Figure 4.5. Here, the origin of the coordinate is the left-bottom corner. Two-port impedance data of the power/ground plane was extracted using the method suggested in [43]. In [43], the impedance matrix is computed using analytical equations and then equivalent circuits for two ports on plane pairs were constructed using resonator models. Impedance data previously generated was converted into an S-parameter file for simulation in Advanced Design System (ADS). A switching source in ADC was modeled as a voltage clock in series with an output resistance. It was assumed that the ADC under test is at port1. Switching current in ADC modeled as a voltage clock in series with an output resistance generates switching noise when it meets self-impedance of the power/ground plane at port1. Figure 4.5 shows the modeling of switching noise in a load board. Shown in Figure 4.6 is the self-impedance (Z_{11}) plot of the test board as a function of frequency. Switching sources having three different kinds of frequencies are used, as shown in Figure 4.6.

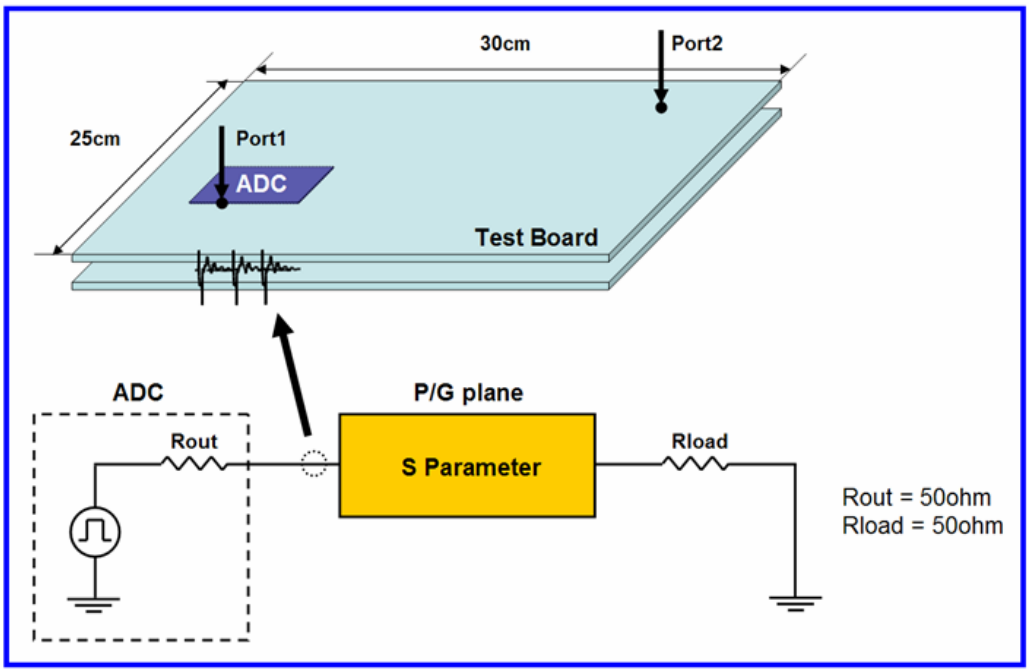


Figure 4.5: Switching noise modeling in a load board.

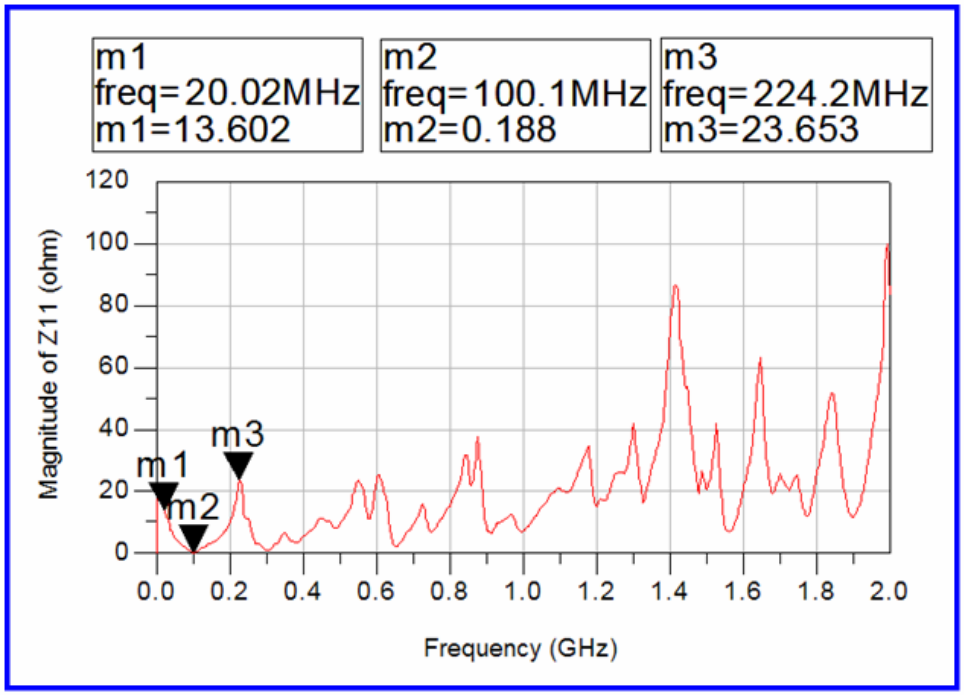


Figure 4.6: Self-impedance (Z_{11}) plot of a load board. Switching noises were generated at three different frequencies indicated by m1, m2, and m3.

To simulate the effects of switching noise on ADC performance, the switching noise generated in Figure 4.5 were inserted into the ground of V_{REF} and V_{IN} of ADC, as shown in Figure 4.7. First, static characteristics of the ADC were simulated with a ramp input, which is a 2.5 us period, as shown in Figure 4.8. The top schematic in Figure 4.8 is an ADC without noise, and the bottom schematic is an ADC with noise.

Figure 4.9 shows switching noise generated by the switching sources for ADC performance simulations in Figure 4.8 with three frequencies in Figure 4.6. Shown in Figure 4.10 is ADC outputs for the switching noise in Figure 4.9. Full scale range (FSR) of 3 V and 4-bit resolution ADC has approximately 180 mV range for LSB. As shown in Figure 4.10, the generated switching noises are so large that ADC cannot operate correctly.

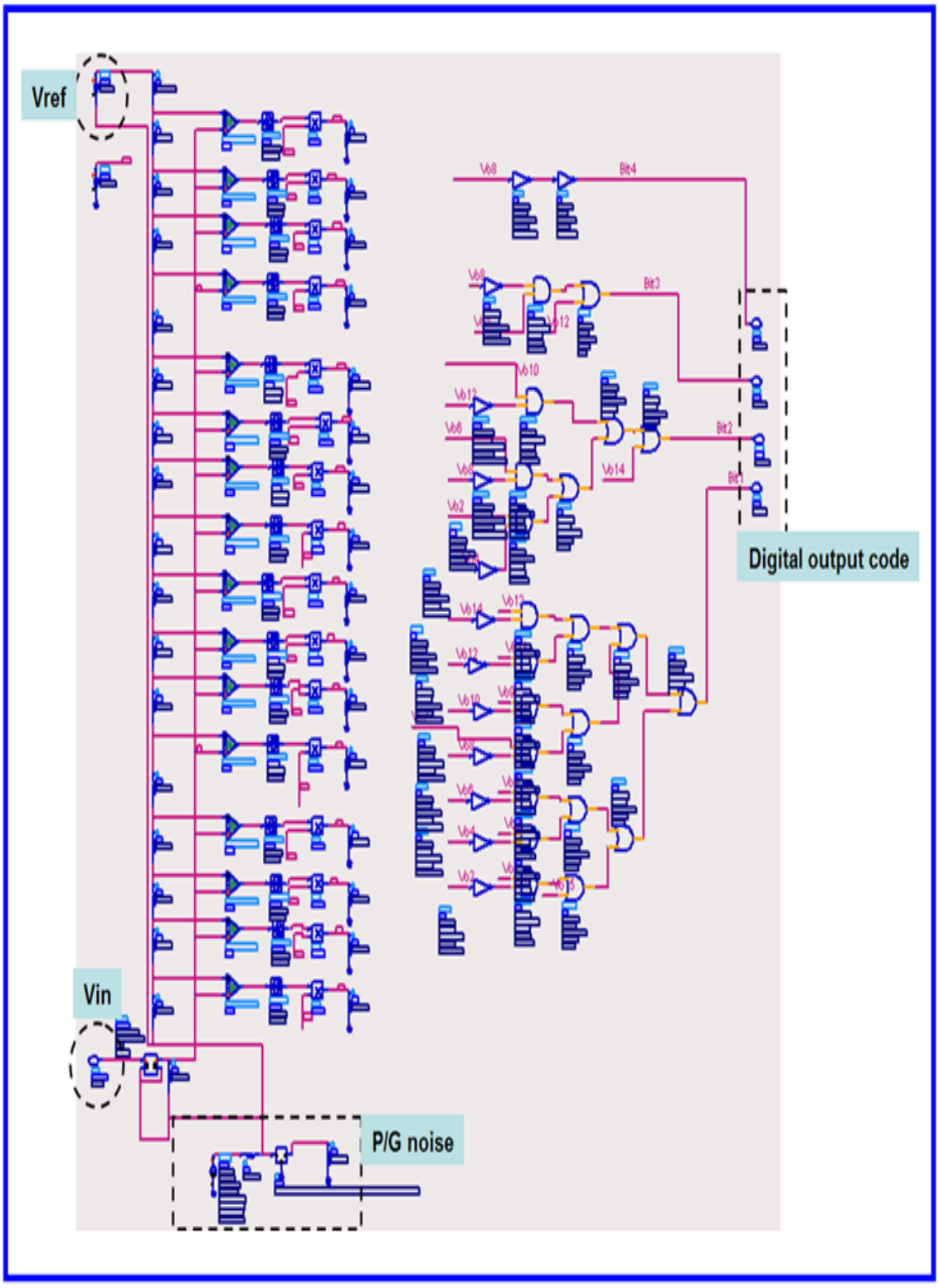


Figure 4.7: Four-bit flash ADC model in ADS from Agilent excited by the switching noise modeled in Figure 4.5.

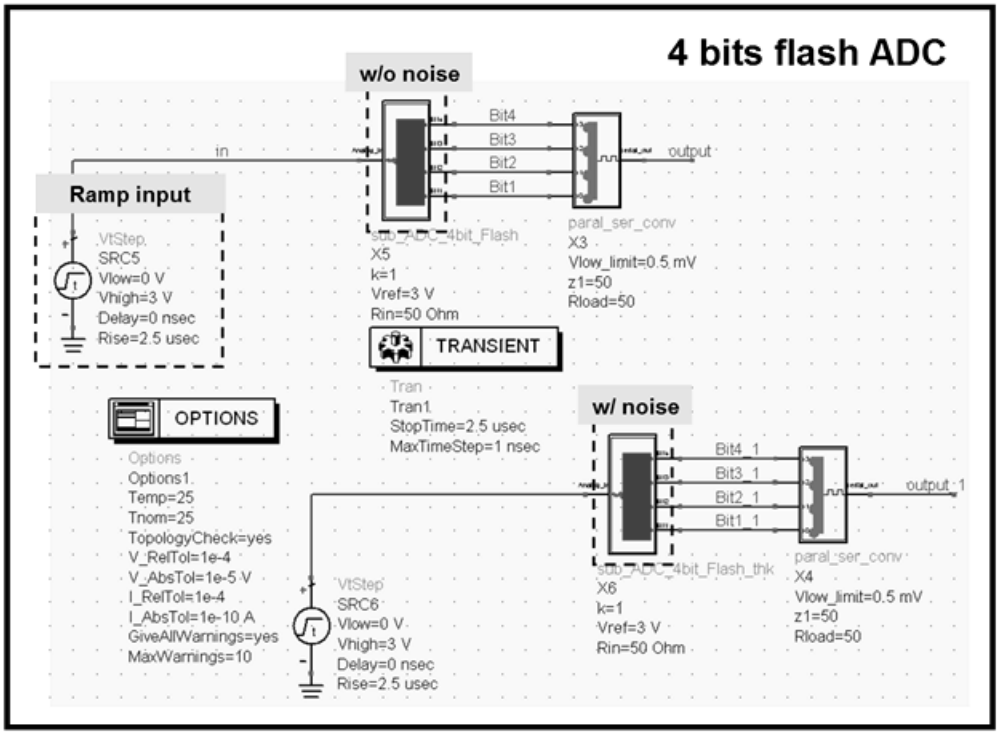
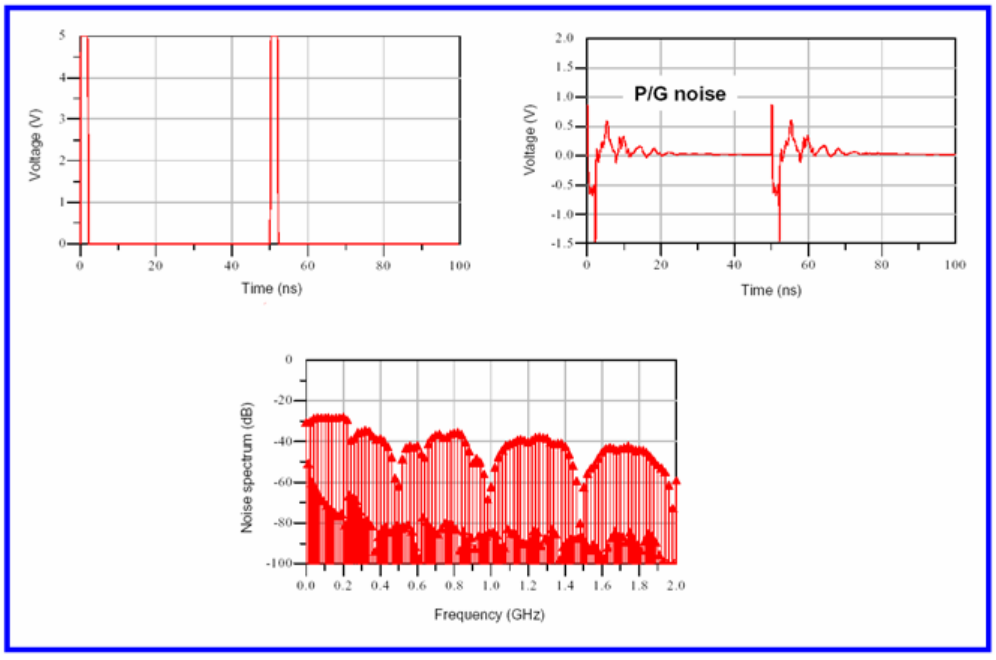
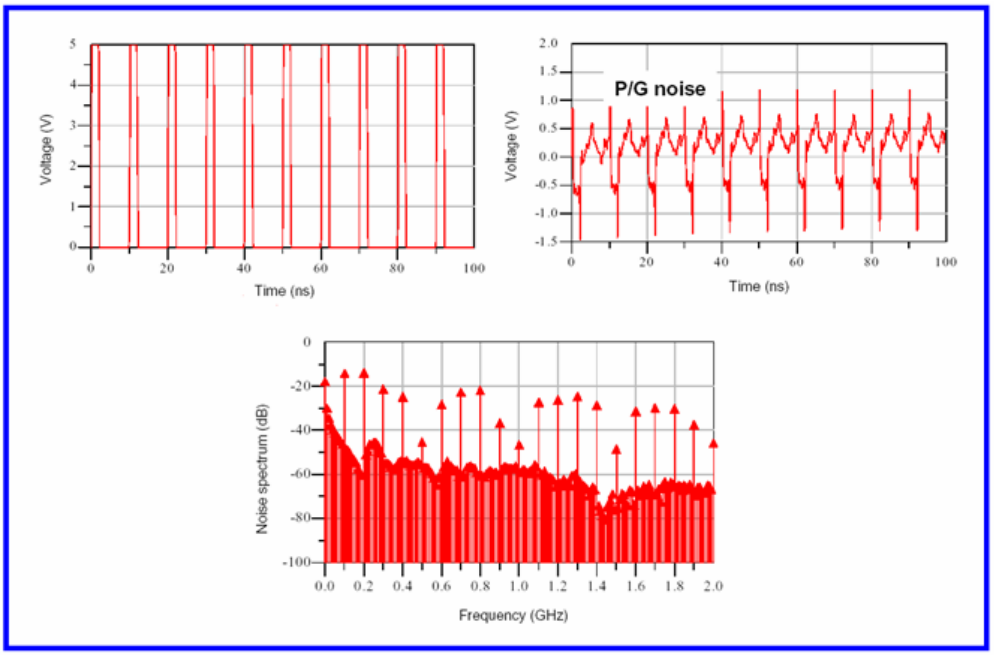


Figure 4.8: Simulation schematics for static characteristics of ADC with ADS.

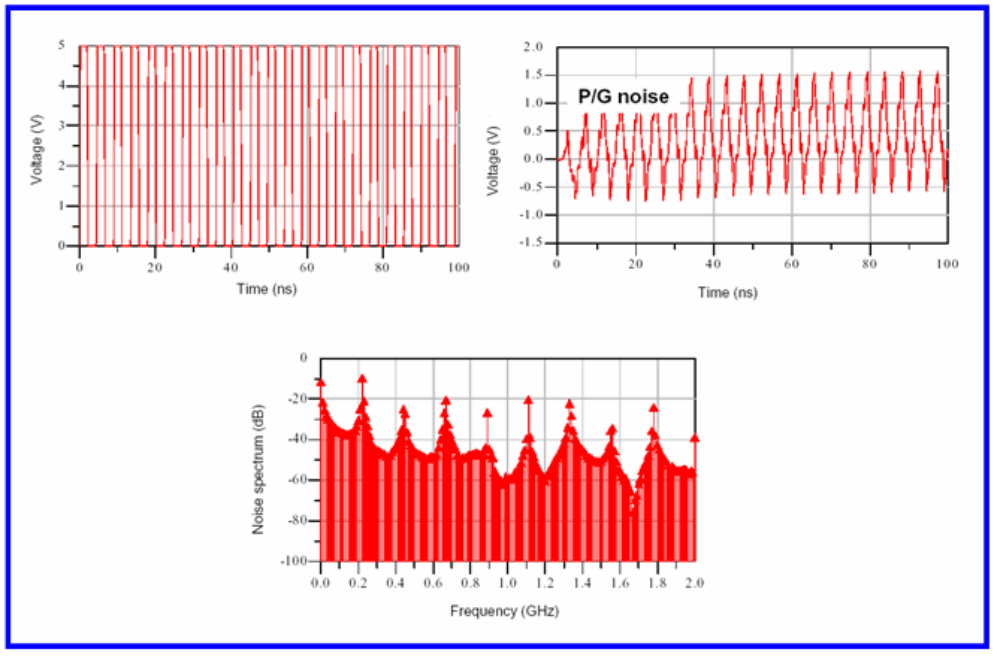


(a)

Figure 4.9: Voltage sources used in Figure 4.5 to generate switching noises, the switching noises generated with the voltage sources, and spectrums for the switching noises for (a) a voltage source (20MHz and 5Vp-p), (b) a voltage source (100MHz and 5Vp-p), and (c) a voltage source (224MHz and 5Vp-p) .



(b)



(c)

Figure 4.9: Continued.

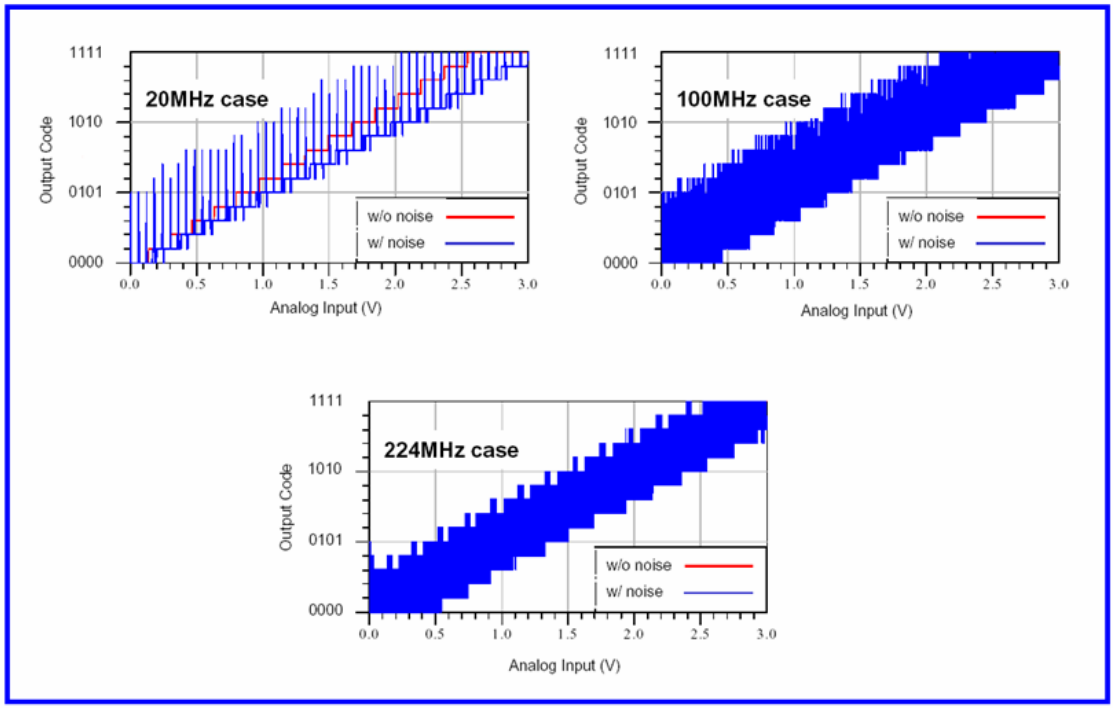


Figure 4.10: ADC outputs for the switching noises in Figure 4.9.

To reduce the switching noise, a decoupling capacitor (10nF) was connected to port1, as shown in Figure 4.11. Since the switching noise is proportional to plane impedance and the amount of switching current, the reduction of plane impedance with a decoupling capacitor resulted in reduced switching noise, as shown in Figure 4.12. As shown in Figure 4.12, the switching noise is reduced by almost 7 times. However, as shown in Figure 4.13, ADC outputs still have some errors although ADC shows better performance than what was shown in Figure 4.10. Finally, the switching noise has to be reduced below 0.5 LSB for ADC to operate correctly.

Also, simulations for signal to noise ratio (SNR) and effective number of bits (ENOB) were conducted. As shown in Figure 4.14, a 100 MHz sinusoidal input was used for the simulation of dynamic characteristic of ADC. Figure 4.15 shows simulation results for SNR and ENOB. As shown in Figure 4.15, the switching noise reduced SNR

by 6 dB and ENOB by 2 bits. The simulation results shown in Figure 4.15 (a) can be verified with theoretical equations. The signal-to-noise ratio of ADC can be expressed as

$$SNR_{\max}(dB) = 20\log_{10}\frac{V_{OUT(\max)}}{rms(quantization\ noise)} = 6.02NdB + 1.76dB \tag{4.2}$$

where

$$V_{OUT(\max)} = \frac{FSR}{2\sqrt{2}} \text{ for a sinusoidal waveform} \tag{4.3}$$

$$rms(quantization\ noise) = \frac{FSR}{2^N\sqrt{12}}. \tag{4.4}$$

The effective number of bits (ENOB) can be defined from (4.2) as

$$ENOB = \frac{SNR_{actual} - 1.76}{6.02}. \tag{4.5}$$

The sampling clock jitter effect on ADC performance was also simulated. Switching noise causes phase noise in VCO and delay in clock distribution network. This results in timing jitter. Figure 4.16 shows ADC performance errors in the presence of 10 % jitter.

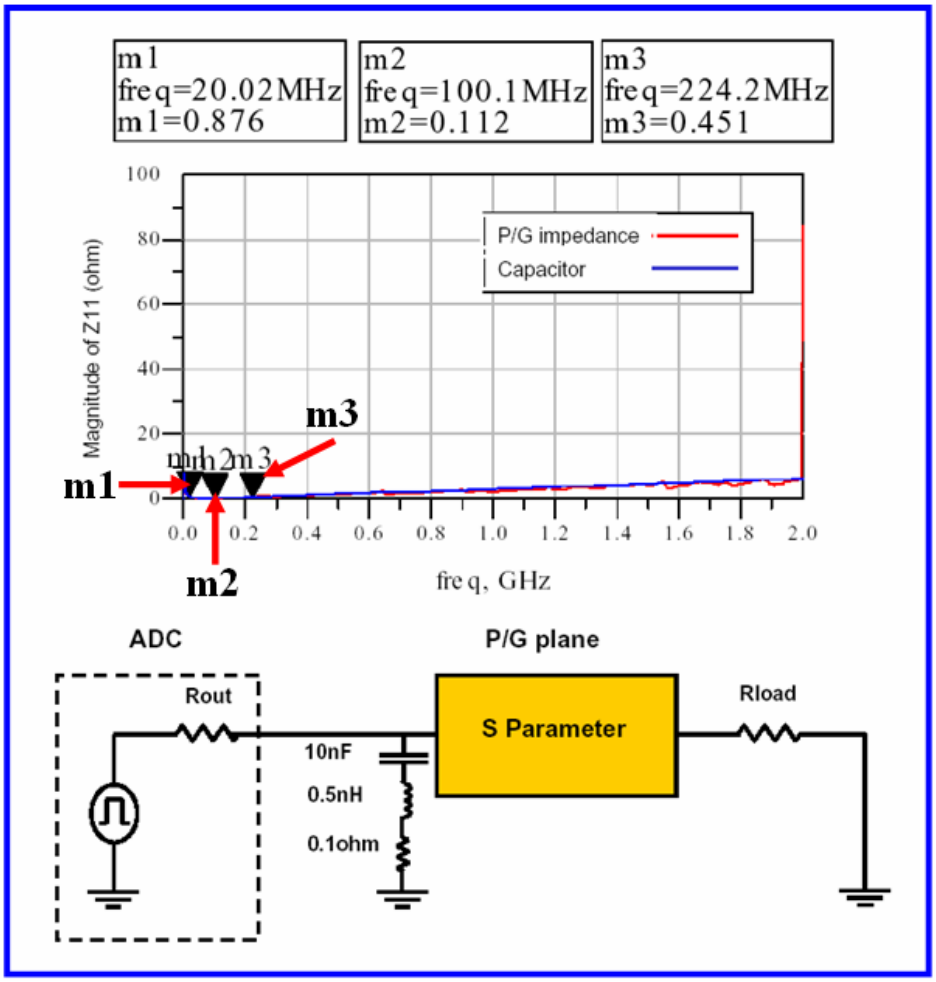


Figure 4.11: Self-impedance (Z_{11}) of the power distribution network (PDN) with a decoupling capacitor which is 10nF.

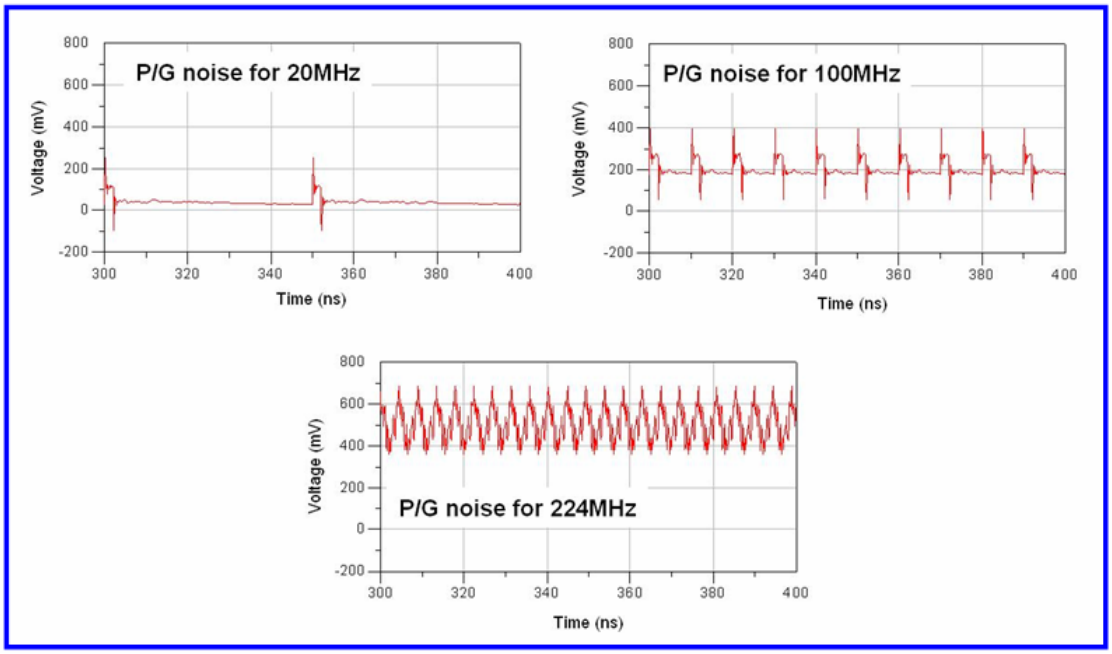


Figure 4.12: Switching noise generated when a decoupling capacitor (10nF) was connected.

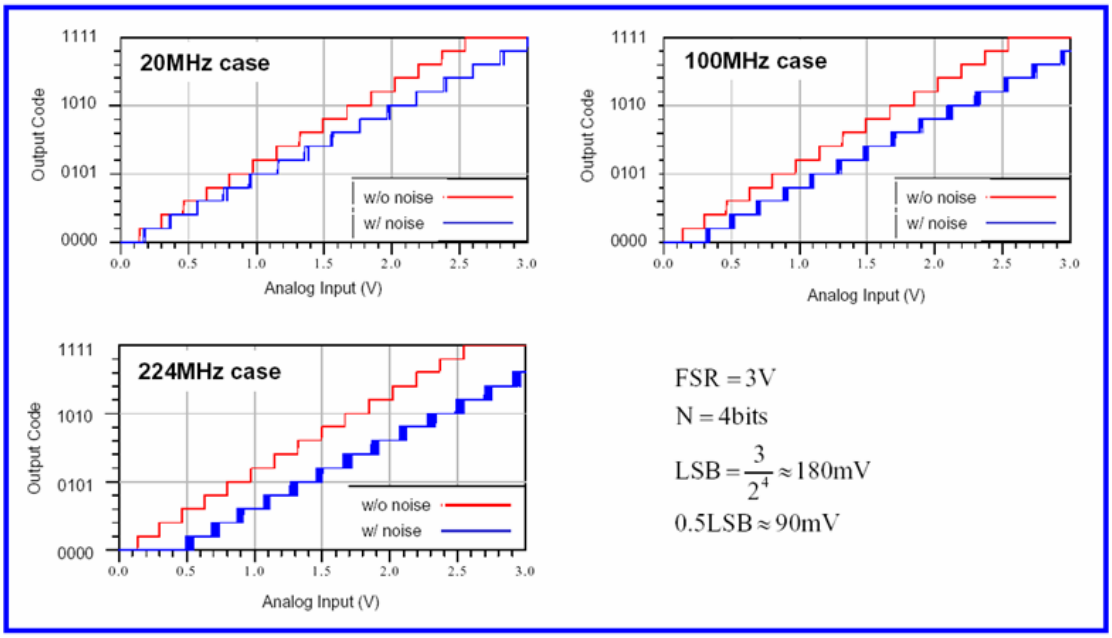


Figure 4.13: ADC outputs for the reduced noise in Figure 4.12.

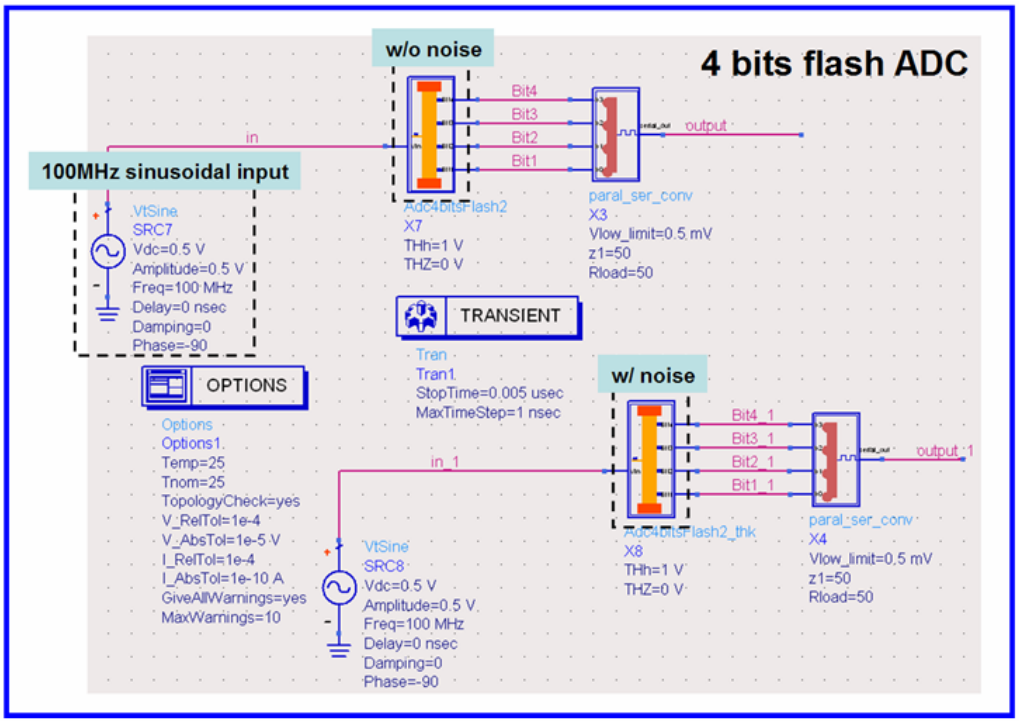
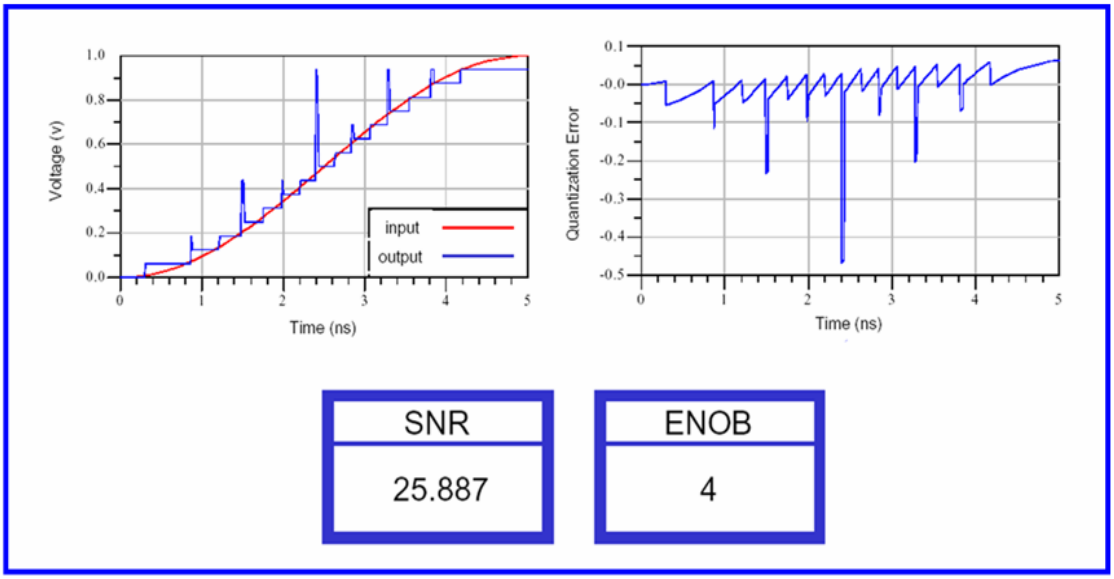
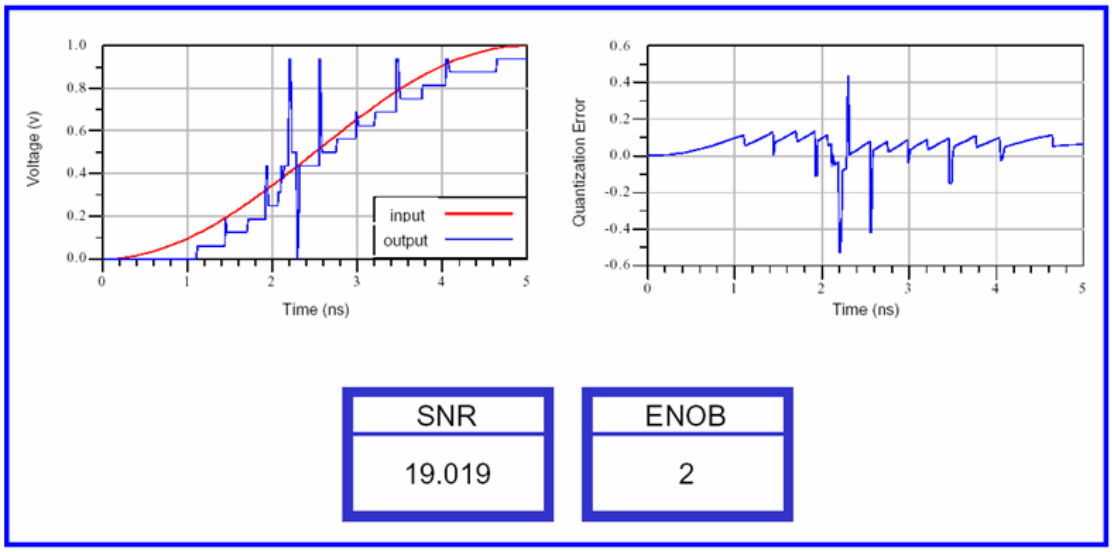


Figure 4.14: Simulation schematics for dynamic characteristics of ADC.



(a)

Figure 4.15: Signal to noise ratio (SNR) and effective number of bits (ENOB) for ADC (a) without switching noise and (b) with switching noise.



(b)

Figure 4.15: Continued.

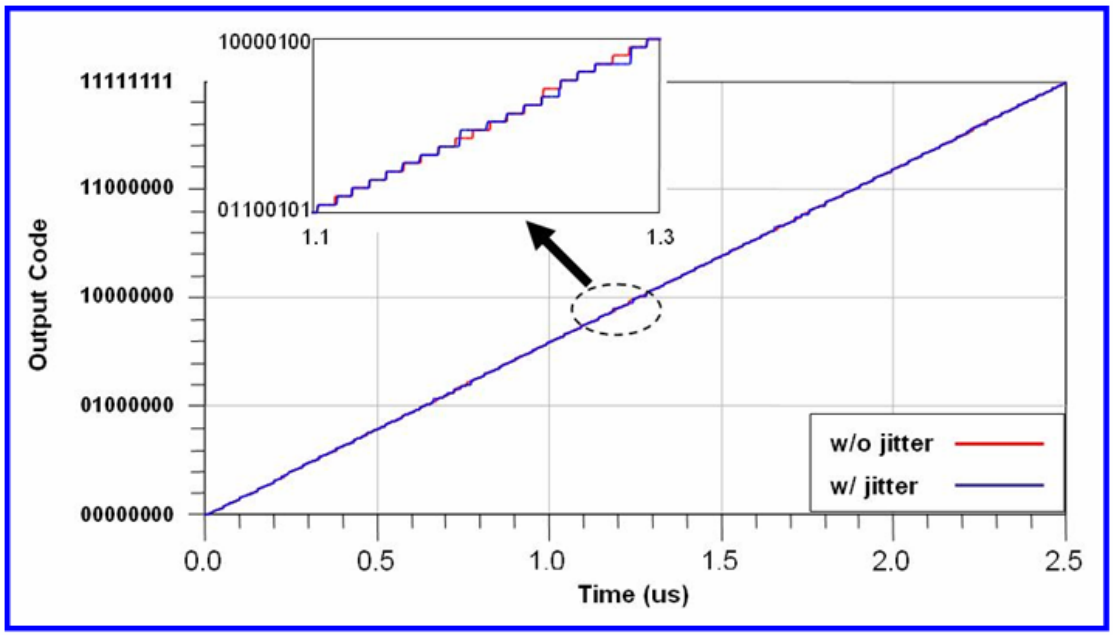


Figure 4.16: ADC performance in the presence of timing jitter.

4.5 Specification and Guidelines for ADC Load Board Design

In this Section, the target impedance of a power distribution network (PDN) is utilized to define specifications for ADC load board design. The target impedance is the maximum allowed impedance for the system to meet a specified noise level.

For example, consider a component operating at a voltage V_{DD} and dissipating an average of P watts. The average current is $I_{avg} = P / V_{DD}$. Assuming that the allowed ripple on the power supply is $V_{ripple} = xV_{DD,}$ where typical values for x are 5% to 10%, then the target impedance is

$$Z_{Target} = \frac{V_{ripple}}{I_{avg}}. \tag{4.6}$$

Finally, the power distribution system should be designed so that the impedance looking into the system at the site of the component is less than the target impedance over a specified bandwidth. The definition of target impedance is sketched in Figure 4.17.

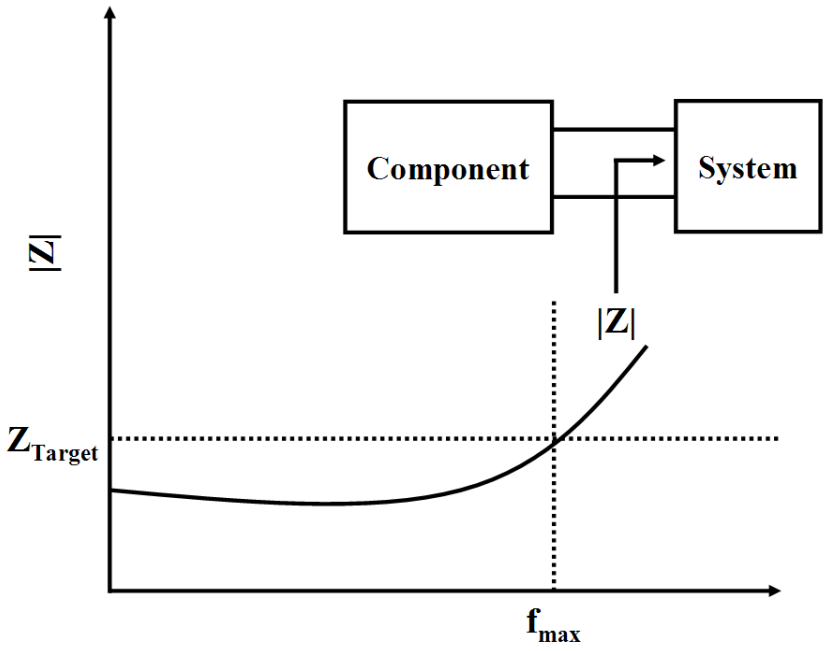


Figure 4.17: Target impedance sets the maximum impedance magnitude of the power distribution network as seen from the position of a component [17].

As mentioned before, the switching noise (the allowed ripple on the power supply : V_{ripple}) on the ADC load board should be below 0.5 LSB for ADC to operate correctly. Assuming that the transient current for ADC is $\triangle i$ (I_{avg}), then, Z_{Target}, the target impedance of the ADC load board power distribution network should be less than 0.5LSB/$\triangle i$.

Finally, the power distribution system of ADC load board should be designed so that the impedance looking into the system at the site of noise source on the load board is less than the target impedance over the bandwidth of critical signals on the load board.

4.6 Summary

In this Chapter, simultaneous switching noise (SSN) sources existing on the ADC load board and the SSN effects on ADCs were analyzed. It was shown that the SSN should be below 0.5 LSB for ADCs to operate correctly. The target impedance of ADC load board power distribution network was suggested for accurate characterization of ADCs.

CHAPTER 5

POWER/GROUND NOISE SUPPRESSION IN ADC LOAD BOARD USING EBG STRUCTURES

A load board is used to interface a device to be tested with automatic test equipment (ATE). The load board is an integral part of the test environment. For proper characterization and testing of current multi-gigahertz and high-resolution ADCs, suppression of the switching noise on the load board can be critical.

The current trend for analog-to-digital converters (ADCs) is towards multi-gigahertz sampling rate and high resolution (more than 20 bits) [45]. These ADCs are increasingly sensitive to noise due to the reduction in noise and timing margins. Characterization and test hardware for these devices can become problematic, since the required load boards must demonstrate negligible levels of path loss and introduced noise. Solutions become especially complicated at gigahertz frequencies, where high frequency electromagnetic effects can cause excessive path loss and noise due to the distributed behavior of the interconnections.

Electromagnetic band gap (EBG) structures have become very popular due to their suppression of unwanted electromagnetic mode transmission and radiation in the area of microwave. In the last few years, EBG structures have been proposed for the reduction of simultaneous switching noise (SSN) in high-speed digital systems [7] and in mixed-signal systems where digital circuits are combined with RF circuits [8].

In this Chapter, EBG structures are presented for an ADC load board design in which sensitive analog circuits coexist with digital circuits. As a real application, a prototype load board for 1.5Gbps and dual 8-bit ADCs is considered. The devices and

hardware were provided by National Semiconductor. The voltage range used for the test is 1.9 V +/- 200 mV.

5.1 Power/Ground Noise Analysis on ADC Load Board

For power/ground noise analysis on the load board, aggressors and victims were determined on the pre-modification board. Output drivers of the ADC chip are considered to be the aggressors and the analog power/ground pins of the ADC chip are considered to be the victims.

Figure 5.1 shows the locations of the PWR pins and GND pins of the ADC chip and the pads of the bypass capacitors. For power/ground noise analysis, the layer of the board including both the analog power plane and the digital power plane was imported and simulated by the multilayer, finite-difference method [37] as shown in Figure 5.2. As shown in Figure 5.2, a total of 18 bypass capacitors were placed at the same locations as shown in Figure 5.1. For P4 and P11 (Figure 5.1), a bypass capacitor that has a C of10 uF, an ESR of 311.91 mohm, and an ESL of 1.8 nH was installed. For P1 through P3, P5 through P10, and P12 through P16 (Figure 5.1), a bypass capacitor having a C of 0.1 uF, an ESR of 63.41 mohm, and an ESL of 1.94 nH was put in place.

First, the amount of switching noise (ΔV) generated by each output driver (P1 through P8) was simulated, assuming that the switching current (ΔI) of 20 mAp-p and 747 MHz is forced to flow by each output driver. For the simulations of the switching noise generated by each output driver, the 747 MHz switching current of 20 mAp-p was connected to P1 through P8 (Figure 5.1) one at a time, and the switching noise (ΔV) for each case was observed. Figure A.1 in Appendix A shows the switching noise generated at each output driver for the switching current.

As shown in Figure 5.3, a histogram was used to graphically summarize and display the distribution of the switching noise generated at each output driver. As the

histogram in Figure 5.3 shows, P1, P5, P7, and P8 generate relatively more switching noise than P2, P3, P4, and P6 for the same switching current. Therefore, it is necessary to reduce the impedance of the power distribution network (PDN) for P1, P5, P7, and P8. This is especially important in the case of P7.

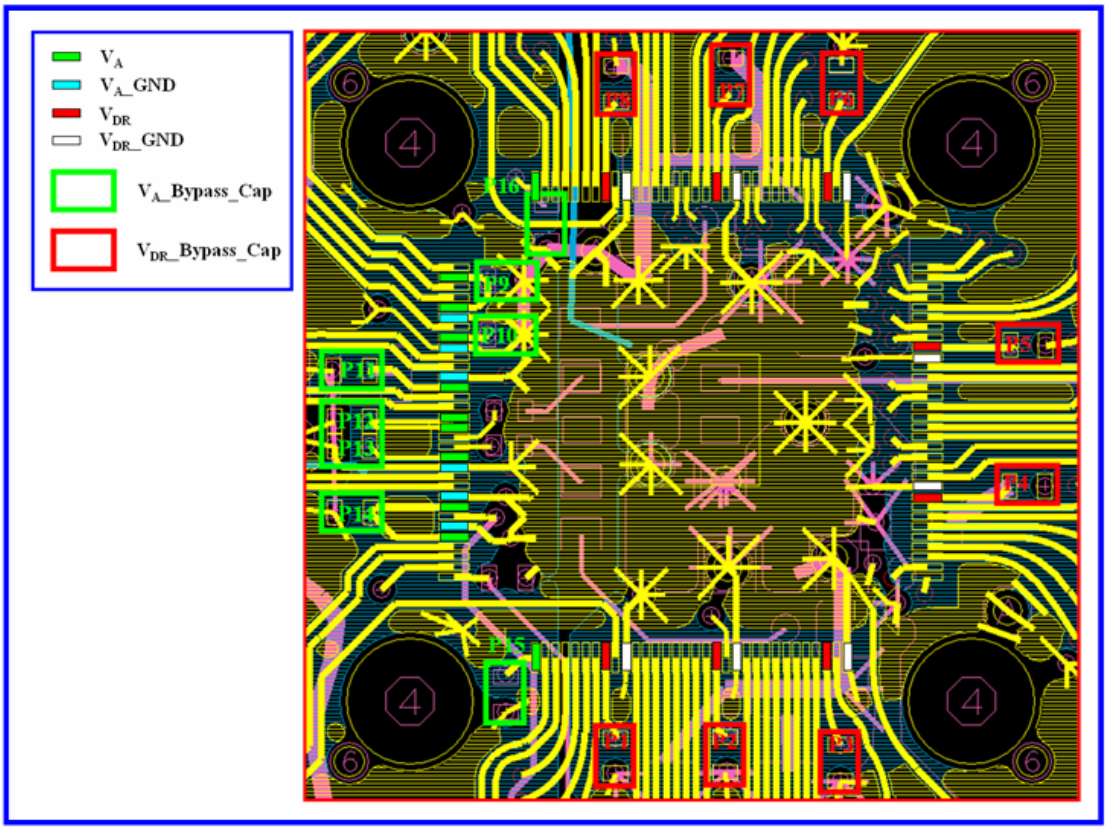


Figure 5.1: Locations of PWR pins and GND pins of ADC chip and the pads of the bypass capacitors: V_A is a power for analog parts, V_A_GND is an analog ground, V_{DR} is a power for digital parts, and V_{DR}_GND is a digital ground. V_A_Bypass_Cap is bypass capacitor for analog parts and V_{DR}_Bypass_Cap is a bypass capacitor for digital parts.

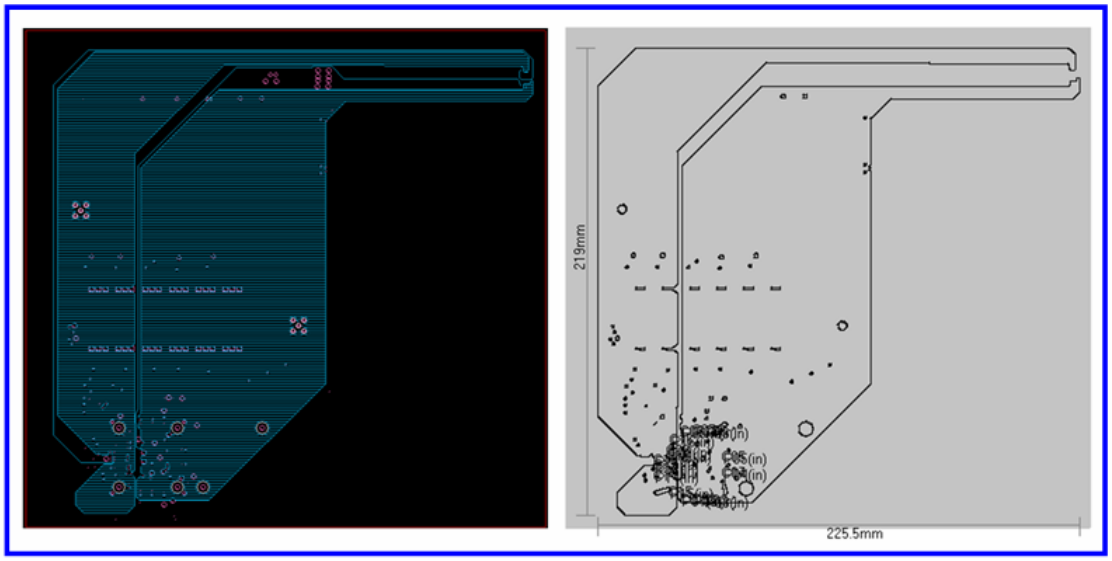


Figure 5.2: Layout of analog power plane and digital power plane (on the left) and the imported structure with multilayer finite-difference method (on the right).

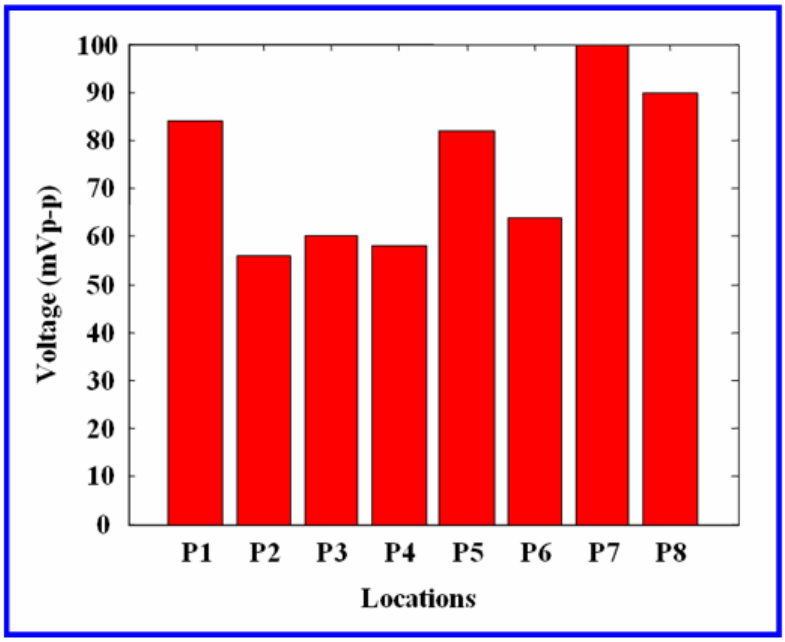


Figure 5.3: Histogram graphically summarizing and displaying the distribution of the switching noise generated at each output driver for the 747MHz switching current of 20mAp-p.

Next, the amount of coupled noise to P9 through P16 (Figure 5.1) was simulated when each output driver from P1 to P8 (Figure 5.1) was excited with the switching current of 20 mAp-p and 747 MHz. The simulated results are shown in Figure A.2 through Figure A.9 in Appendix A. Figure 5.4 shows a histogram that graphically summarizes and displays the distribution of the coupled switching noise. The histogram shown in Figure 5.4 consists of eight columns, each of which represents each aggressor from P1 to P8 (Figure 5.1). Each column includes eight bars, each of which is the amount of coupled noise from an aggressor representing the column to each victim (from the left-most bar to the most right bar: P9 ~ P16).

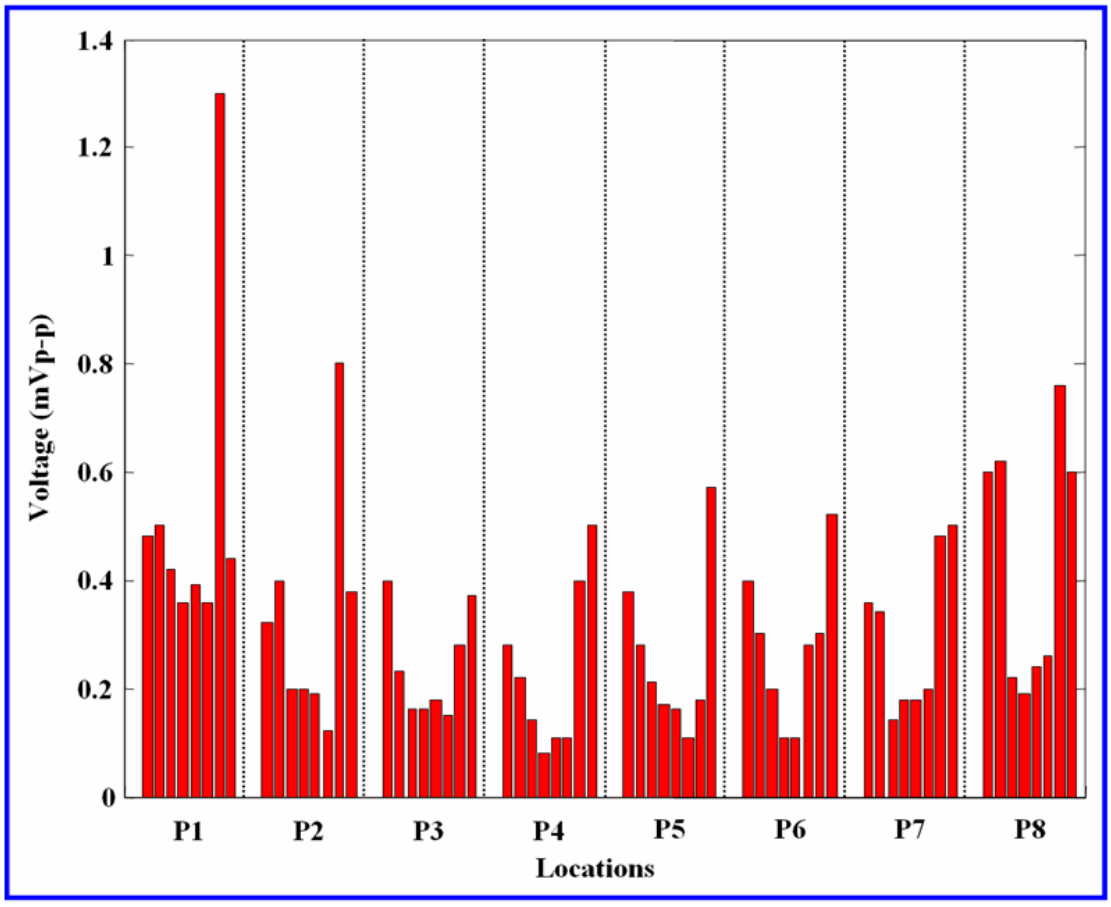


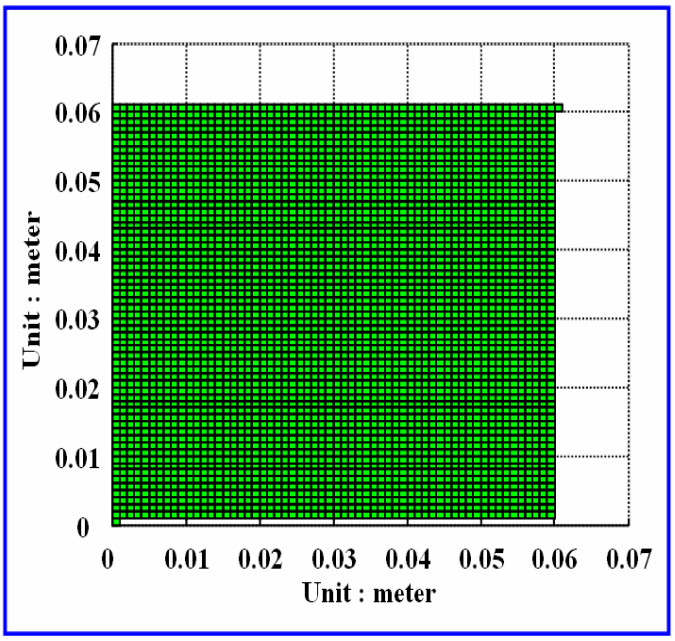
Figure 5.4: Histogram graphically summarizing and displaying the distribution of the coupled switching noise. This histogram consists of eight columns each of which represents each aggressor: P1 through P8. Each column includes eight bars each of which shows the amount of coupled noise from the aggressor representing the column to each victim (from the left-most bar to the right-most bar: P9~P16). Refer to Figure 5.1 for the locations.

As shown in the histogram in Figure 5.4, P1-P8 (digital PWR/GND pins which are aggressors on the ADC load board) show a large amount of noise coupling to P9-P16 (analog PWR/GND pins which are victims on the ADC load board). Therefore, it is necessary to minimize the coupling noise.

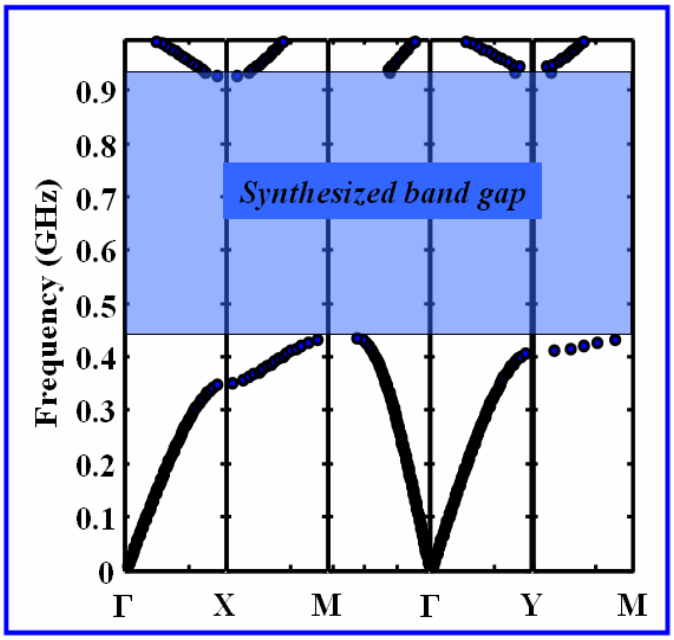
5.2 Synthesizing an EBG Structure

In order to suppress the power/ground noise on the ADC load board, an EBG structure was synthesized using the EBG synthesizer suggested in Chapter 3. The target noise is 747 MHz. The EBG structure was designed for an on-set frequency of 500 MHz and off-set frequency of 950 MHz. The on-set frequency is the starting frequency of the band gap, and the off-set frequency is the ending frequency of the band gap. Tolerance of 100 MHz was used for this design. The tolerance is used to determine how much deviation from the desired on-set frequency and off-set frequency are acceptable. For this target design, a material (FR4), which has permittivity of 4.5, loss tangent of 0.035, and 406.4 μm thick, was used as a dielectric material. 30 μm thick copper was used as conductor. A patch size of 60 mm x 60 mm was used. The synthesized patch shape and dispersion diagram are shown in Figure 5.5 (a) and 5.5 (b) respectively. As shown in Figure 5.5 (b), a band gap from 500 MHz – 950 MHz was achieved as per the initial design specification. The deviation from the desired stop band is less than 100 MHz as per the initial tolerance. To verify the synthesized patch shape in frequency-domain, six patches shown in Figure 5.5 (a) were arranged in a 2x3 array as shown in Figure 5.6. Figure 5.7 shows the modeled and simulated results of the EBG structure shown in Figure 5.6. Port locations for the simulation are shown in Figure 5.6. As shown in Figure 5.7, the modeled and simulated results of the EBG structure with M-FDM exhibit a band gap from 500 MHz to 950 MHz as per the initial EBG design specification. Figure 5.6 shows the voltage distribution for the EBG structure at a frequency (750 MHz) within the

band gap (500 MHz – 950 MHz) when port1 is excited with a current source of 1A. The voltage distribution is proportional to transfer impedance (Z_{21}) between port1 and other locations. The transfer impedance is a measure of the amount of coupled noise from an aggressor (port1) to a victim port. Higher level of voltage distribution (indicated by red) means more noise coupling from the aggressor (port1) to the victim location. As shown in Figure 5.6, there is no coupling within the band gap, and the excited noise is confined within the patch.



(a)



(b)

Figure 5.5: For on-set frequency of 500 MHz and off-set frequency of 950 MHz (a) the synthesized patch shape and (b) dispersion diagram plot of the synthesized patch shape in (a).

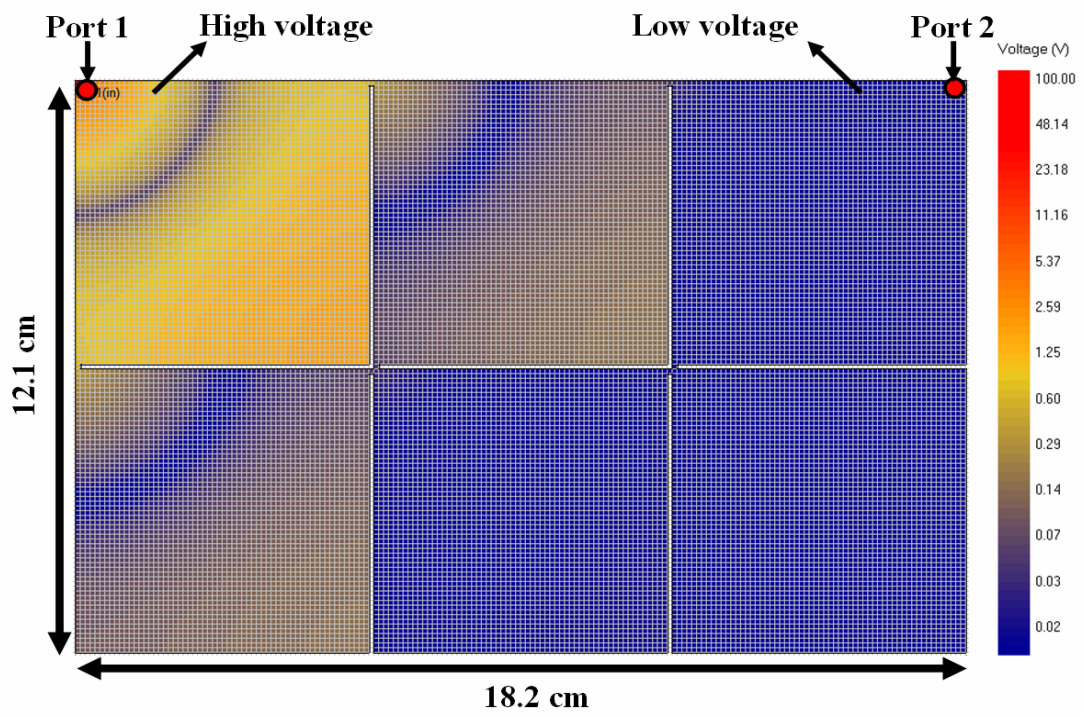


Figure 5.6: Voltage distribution at 750 MHz for an EBG structure consisting of a 2x3 array of the synthesized patch shown in Figure 5.5(a) when port 1 was excited.

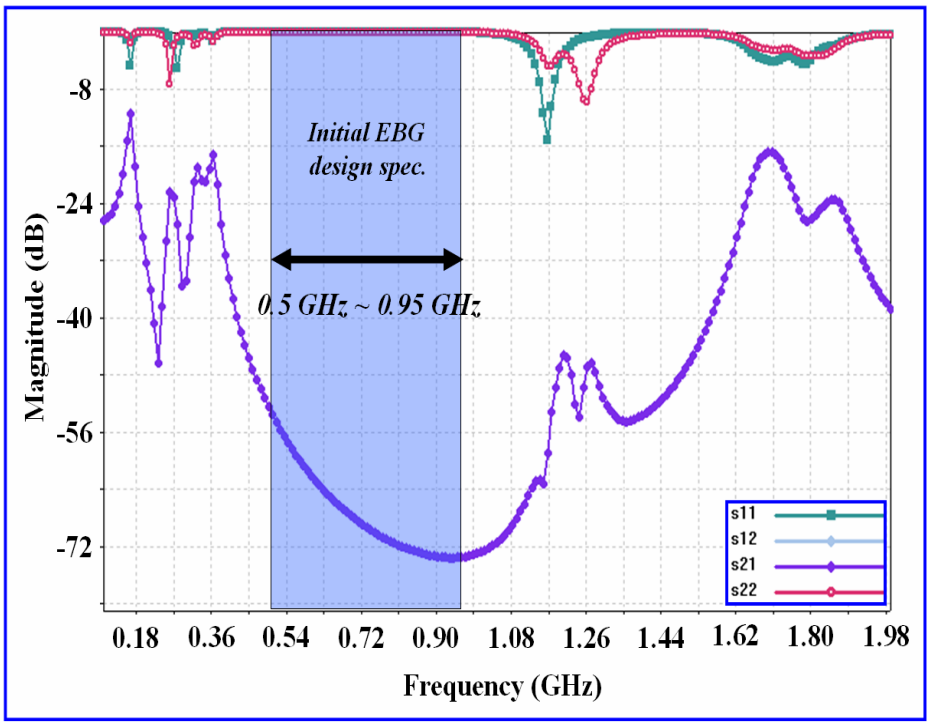


Figure 5.7: Modeled and simulated S-parameter results of the EBG structure in Figure 5.6 with M-FDM.

5.3 Modifying the ADC Load Board

Figure 5.8 shows the pre-modification board and the post-modification board. As shown in Figure 5.8, three major modifications were made to the pre-modification board. First, the gap between the analog power plane and the digital power plane on the pre-modification board was widened as long as the connections of all analog/digital PWR pins to the proper plane were not adversely affected. The expected effect from the modification is that the widened gap between aggressors (digital PWR/GND pins) and victims (analog PWR/GND pins) will minimize the chance of noise coupling from the aggressors to the victims. Second, the digital power plane on the pre-modification board was made larger on the post-modification board. Providing a larger power plane will increase the capacitance of the plane, and the increased capacitance will decrease the switching noise generated by the same amount of switching current. Third, an EBG structure, which was synthesized in the previous Section, was created on the digital power plane. When the EBG structure was created, two important factors were taken into account. The first factor was to confine all aggressors, which are digital PWR/GND pins in this target board, into a unit cell of the EBG structure. An EBG structure will prohibit the propagation of electromagnetic waves over the stop-band frequency. Therefore, the switching noise can be confined within the unit cell in which the noise is generated. The switching noise can be prevented from propagating from the unit cell in which the noise is generated to other unit cells over the stop-band frequency by placing all aggressors into a unit cell. This means that the only way that noise generated in the digital plane can couple to the analog plane is through the unit cell in which the aggressors are placed. If there is no EBG on the digital plane, the noise generated by the aggressors will couple to other areas of the digital plane, and the noise will then couple to the analog plane through the gap. Finally, the area of the gap by which noise can couple from the digital side to the analog side was minimized by creating the EBG structure. The second factor has something to do with how to implement the EBG structure into a limited area. First, a

unit cell of the EBG structure was placed so that it could include all aggressors. Then, the unit cell was extended in horizontal and vertical directions. While approaching the edge of the plane, there was not enough space to implement a whole unit cell. Therefore, a partial unit cell was used so that it would fit into the remaining space.

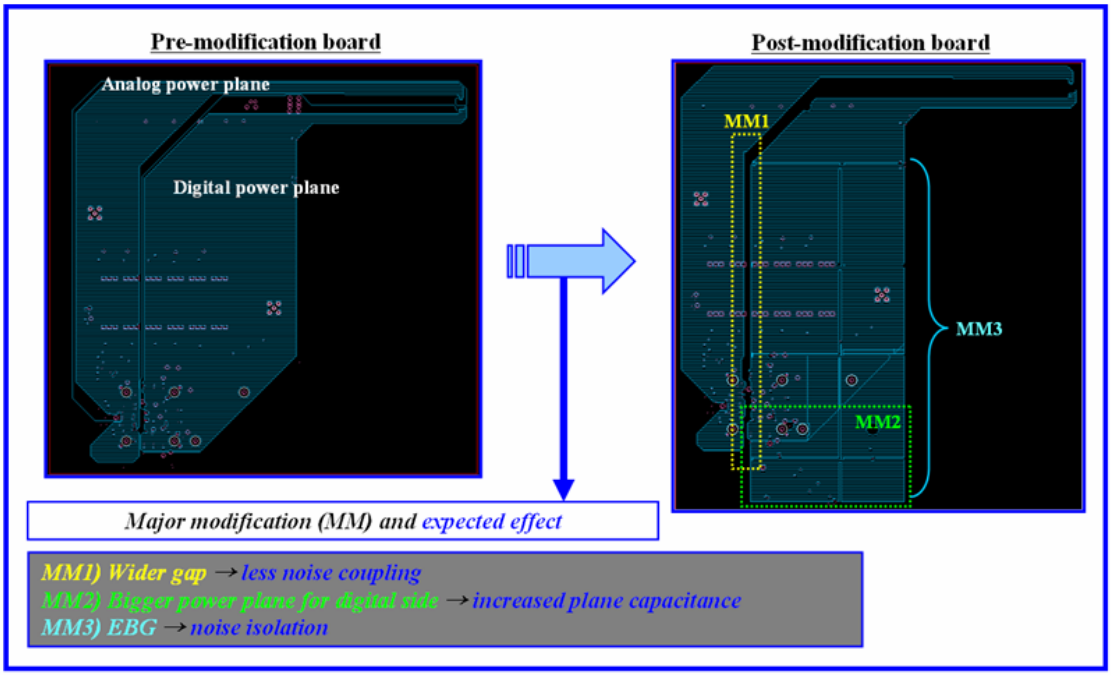
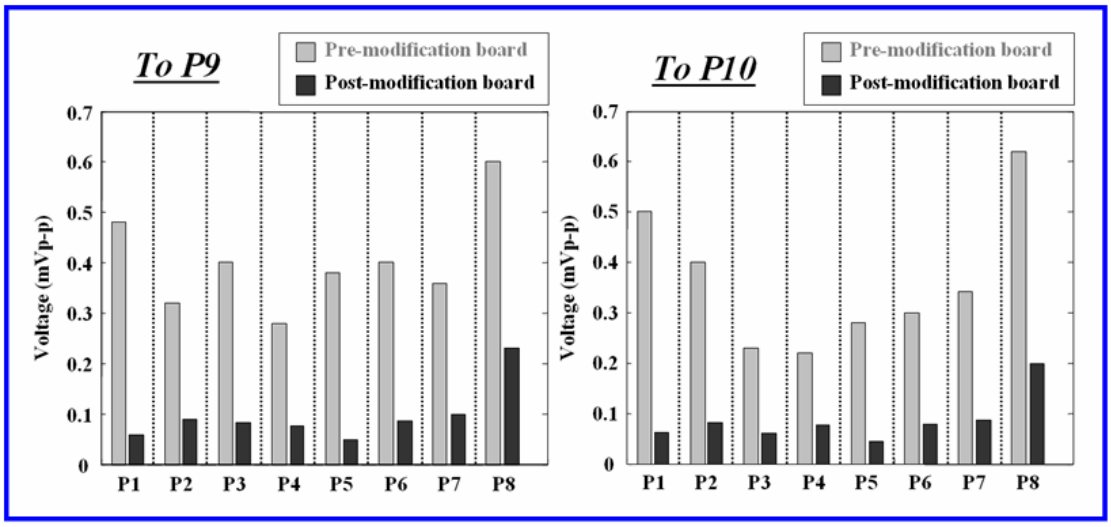


Figure 5.8: Pre-modification board vs. post-modification board.

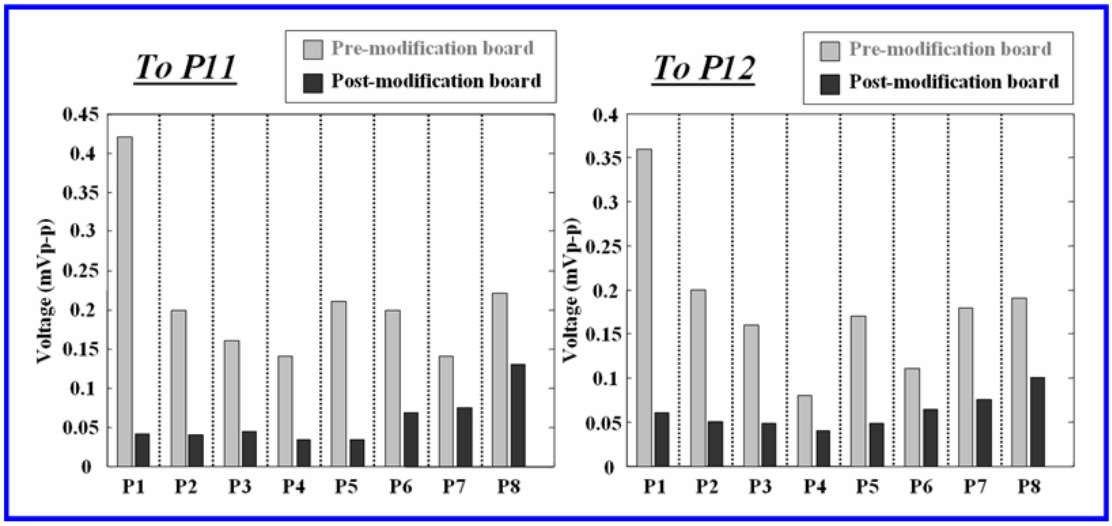
5.4 Time-Domain and Frequency-Domain Comparisons between the Pre-Modification and Post-Modification Boards

The post-modification board was compared with the pre-modification board using simulations. For the comparisons, the same simulations that were done for the pre-modification board in the previous section (Section 5.1) were conducted for the post-modification board. The time-domain simulation results are shown in Figures B.1 through B.9 in Appendix B. Figure 5.9 displays histograms that show the coupled noise comparisons between the pre-modification board and the post-modification board. There

are eight histograms in Figure 5.9. Each of the histograms has eight columns, each of which represents each aggressor (P1 through P8). Each column has two bars. These bars show the amount of coupled noise from the aggressor represented by the column to the victim represented by the title for the pre-modification and post-modification boards. As shown in Figure 5.9, the post-modification board shows reduced noise coupling from aggressors (P1 through P8) to victims (P9 through P16). For the frequency-domain comparison, the scattering parameter (Sij) was also compared. Sij is the transmission coefficient from port j (location j) to port i (location i). The comparison results are shown in Figures C.1 through C.8 in Appendix C. As shown in Figures C.1 through C.8, the post-modification board has a lower transmission coefficient (Sij), which represents less noise coupling from j (P1 - P8) to i (P9 - P16).

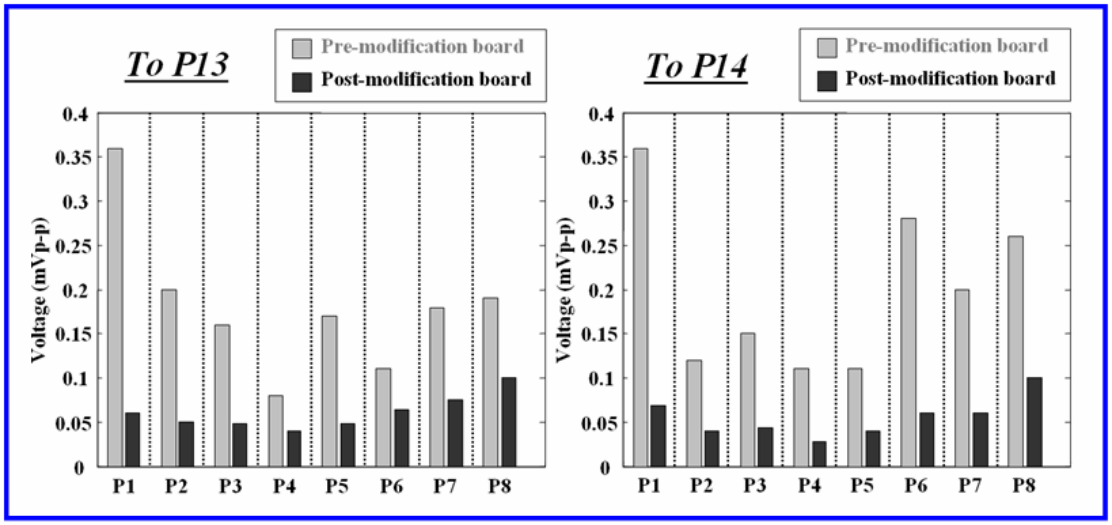


(a) (b)

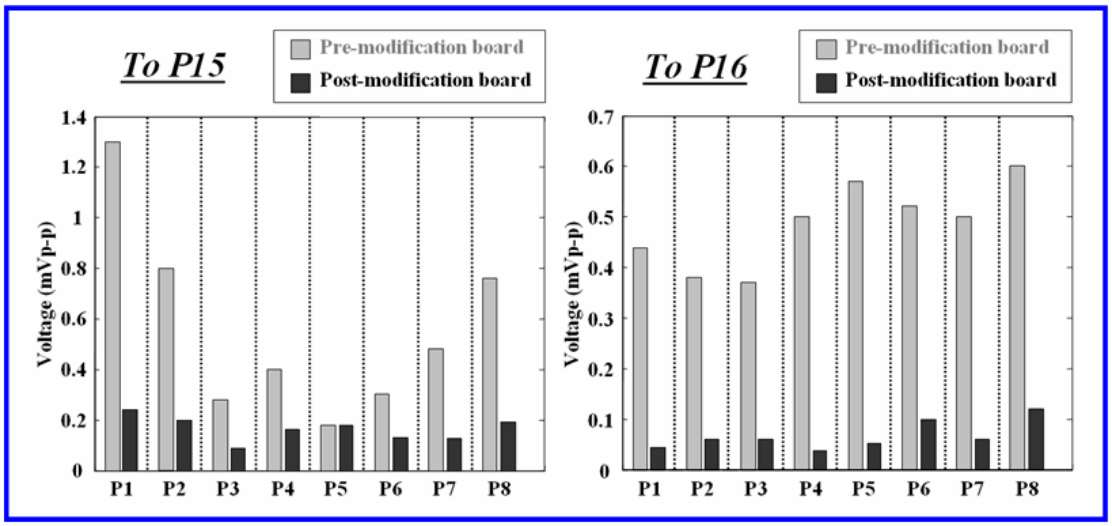


(c) (d)

Figure 5.9: Histograms comparing the coupled noise from P1 ~ P8 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16 between the pre-modification board (gray) and the post-modification board (black).



(e) **(f)**



(g) **(h)**

Figure 5.9: Continued.

Measurements were used to compare the post-modification board with the pre-modification board. For these comparisons, both the simultaneous switching noise (SSN) spectrum and ADC outputs were measured for both the pre-modification board and the post-modification board. The measurements were conducted at all PWR and GND pads of the bypass capacitors. While the tester was on, noise spectrum measurements were conducted with a spectrum analyzer (refer to Figure 5.1 for the locations of the PWR and GND pins of the ADC chip, as well as the pads of the bypass capacitors).

First, noise spectrums were measured for digital parts of the ADC chip. The measured results are shown in Figures D.1 through D.8 in Appendix D. In each Figure, the spectrum on the left side is the measured noise spectrum for the pre-modification board, and the spectrum on the right side is the measured noise spectrum for the post-modification board.

As shown in Figures D.2 through D.5, D.7, and D.8, the noise peaks that were observed at P2 through P5, P7, and P8 on the pre-modification board were more numerous and higher than those on the post-modification board. On the other hand, as shown in Figure D.6, for P6, the post-modification board shows the reduction of noise peaks for the frequency region around 750 MHz, but a noise peak, which was not observed for the pre-modification board, was measured at 1.5 GHz for the post-modification board. For P1, a mixed result was observed for the frequency region around 750 MHz as shown in Figure D.1. While the pre-modification board showed a lower noise peak at 747 MHz, the post-modification board showed reduced noise peaks at 800 MHz and 880 MHz.

The comparisons of the measured results for digital parts of the ADC chip are summarized in Table 5.1. In the right-most column in Table 5.1, the improvement achieved by the post-modification board is expressed as a percentage of the noise from the pre-modification board. In case that no noise peak was measured, the noise minimum, -96 dBm, was used to calculate the percentage. Figure 5.8 shows a histogram that

graphically summarizes and displays the distribution of the noise comparison results shown in Table 5.1.

Table 5.1: Noise spectrum comparisons for digital parts (P1-P8) of the ADC chip between the pre-modification board and the post-modification board.

	Noise peak	Pre-modification board (reference)	Post-modification board	Comparison result
P1	**747 MHz**	-86.27 dBm	-83.02 dBm	3.7 % deterioration
	800 MHz	-87.8 dBm	No noise peak (noise floor: -96dBm)	8.5 % improvement
	880 MHz	-80 dBm	-90 dBm	12.5 % improvement
P2	**747 MHz**	-91.8 dBm	No noise peak (noise floor: -96dBm)	4.6 % improvement
	880 MHz	-83 dBm	-86 dBm	3.6 % improvement
P3	**747 MHz**	-91.21 dBm	No noise peak (noise floor: -96dBm)	5.3 % improvement
	880 MHz	-84 dBm	-91 dBm	8.3 % improvement
P4	**747 MHz**	-92.05 dBm	No noise peak (noise floor: -96dBm)	4.3 % improvement
	880 MHz	-85 dBm	-89 dBm	4.7 % improvement
P5	**880 MHz**	-80 dBm	-91 dBm	13.75 % improvement
P6	**747 MHz**	-92.57 dBm	No noise peak (noise floor -96dBm)	3.7 % improvement
	880 MHz	-82 dBm	-84 dBm	2.4 % improvement
	1.5 GHz	No noise peak (noise floor -96 dBm)	-90 dBm	6.25 % deterioration
P7	**747 MHz**	-90.46 dBm	No noise peak (noise floor -96dBm)	6.1 % improvement
	880 MHz	-82 dBm	-83 dBm	1.2 % improvement
P8	**747 MHz**	-91 dBm	No noise peak (noise floor: -96dBm)	5.5 % improvement
	880 MHz	-80 dBm	-87 dBm	8.75 % improvement

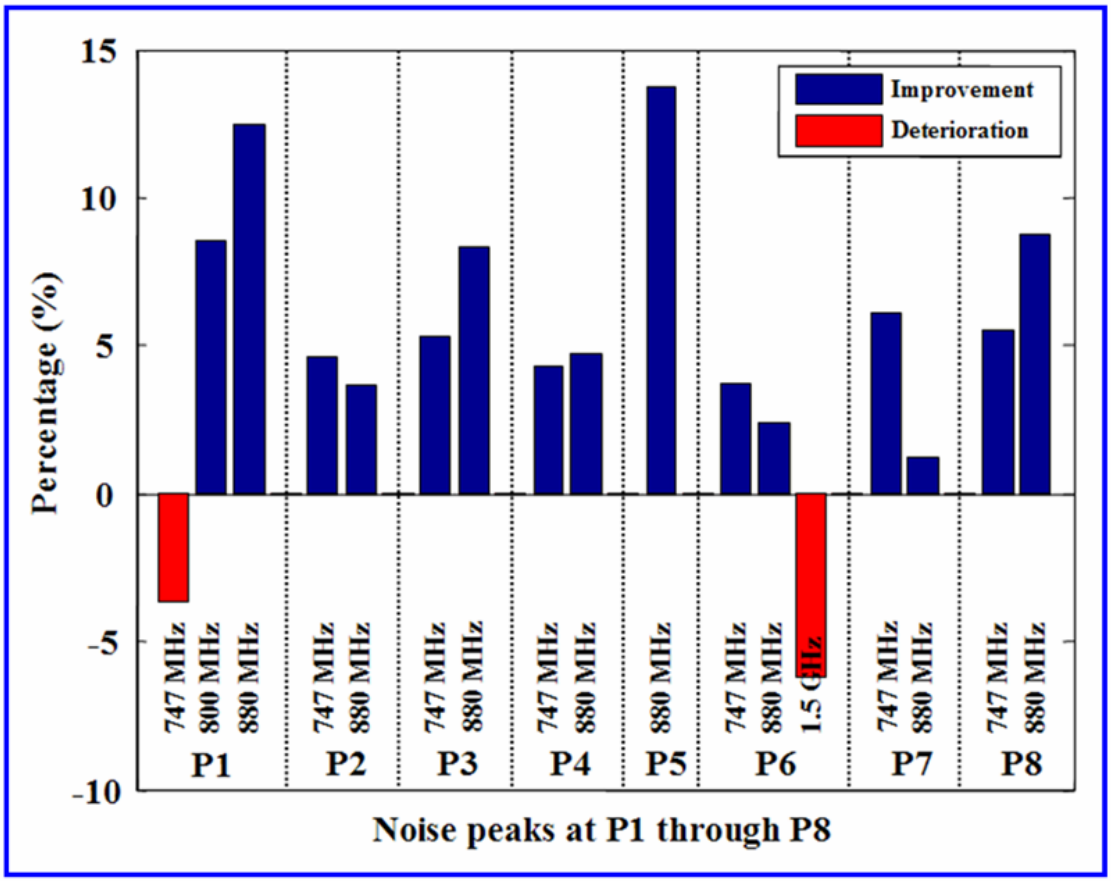


Figure 5.8: Histogram graphically summarizing and displaying the distribution of the noise comparison results shown in Table 5.1.

Noise spectra were also measured for analog parts of the ADC chip. The measured results are shown in Figures D.9 through D.15 in Appendix D. As in Figures D.1 through D.8, the measured noise spectrum for the pre-modification board and the measured noise spectrum for the post-modification board are located on the left side and on the right side in each figure, respectively.

As shown in Figures D.9 and D.11 through D.13, many fewer noise peaks were observed at P9 and P11 through P14 on the post-modification board than on the pre-modification board. On the other hand, as shown in Figure D.10, for P10, a noise peak, which was not observed for the pre-modification board, was observed at 1.5 GHz for the post-modification board. For P15 and P16, the same noise spectra were observed for both

the pre-modification board and the post-modification board, as shown in Figures D.14 and D.15.

Table 5.2 shows the comparisons between the two boards for P9 through P16 in terms of noise spectra. As in Table 5.1, in the right-most column in Table 5.2, the improvement achieved by the post-modification board is expressed as a percentage of the noise from the pre-modification board. In case no noise peak was measured, the minimum noise (-96 dBm) was used to calculate the percentage. Figure 5.9 shows a histogram graphically summarizing and displaying the distribution of the noise comparison results shown in Table 5.2.

Table 5.2: Noise spectrum comparisons for analog parts (P9-P16) of the ADC chip between the pre-modification board and the post-modification board.

	Noise peak	Pre-modification board (reference)	Post-modification board	Comparison result
P9	**880 MHz**	-86 dBm	-92 dBm	7 % improvement
	1.5 GHz	-91 dBm	No noise peak (noise floor: -96dBm)	5.5 % improvement
P10	**880 MHz**	-90 dBm	-90 dBm	No change (0 %)
	1.5 GHz	No noise peak (noise floor: -96dBm)	-82 dBm	6.25 % deterioration
P11	**747 MHz**	-89.88 dBm	-90.5 dBm	0.7 % improvement
	880 MHz	-80 dBm	-86.5 dBm	8.125 % improvement
	1.5 GHz	-92 dBm	No noise peak (noise floor: -96dBm)	4.3 % improvement
P12	**747 MHz**	-88 dBm	-91 dBm	3.4 % improvement
	880 MHz	-80 dBm	-89 dBm	11.25 % improvement
P13	**747 MHz**	-88 dBm	-91 dBm	3.4 % improvement
	880 MHz	-80 dBm	-89 dBm	11.25 % improvement
P14	**747 MHz**	-85 dBm	No noise peak (noise floor: -96dBm)	12.9 % improvement
	800 MHz	-85 dBm	No noise peak (noise floor: -96dBm)	12.9 % improvement
	880 MHz	-75 dBm	-75 dBm	No change (0 %)
	1.5 GHz	-88 dBm	No noise peak (noise floor: -96dBm)	9.1 % improvement
P15	**880 MHz**	-84 dBm	-84 dBm	No change (0 %)
	1.5 GHz	-77 dBm	-77 dBm	No change (0 %)
P16	**880 MHz**	-90 dBm	-90 dBm	No change (0 %)
	1.5 GHz	-70 dBm	-70 dBm	No change (0 %)

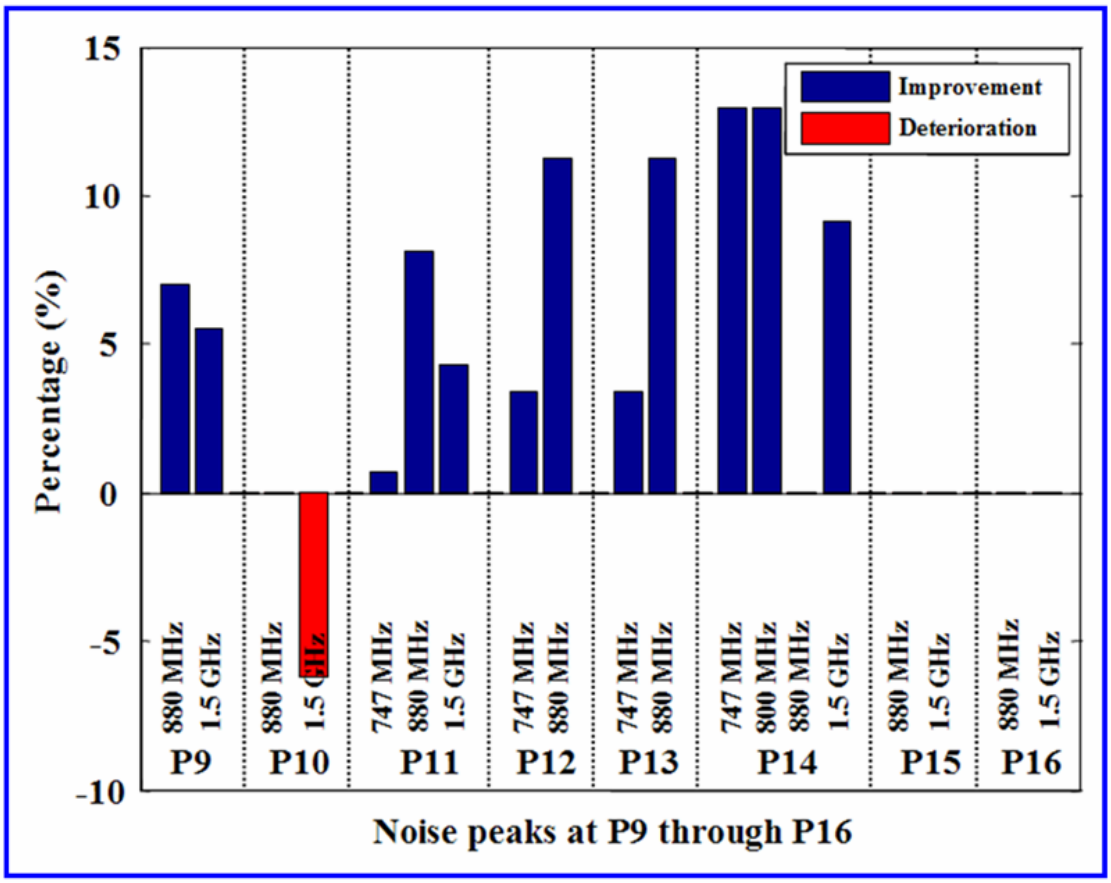
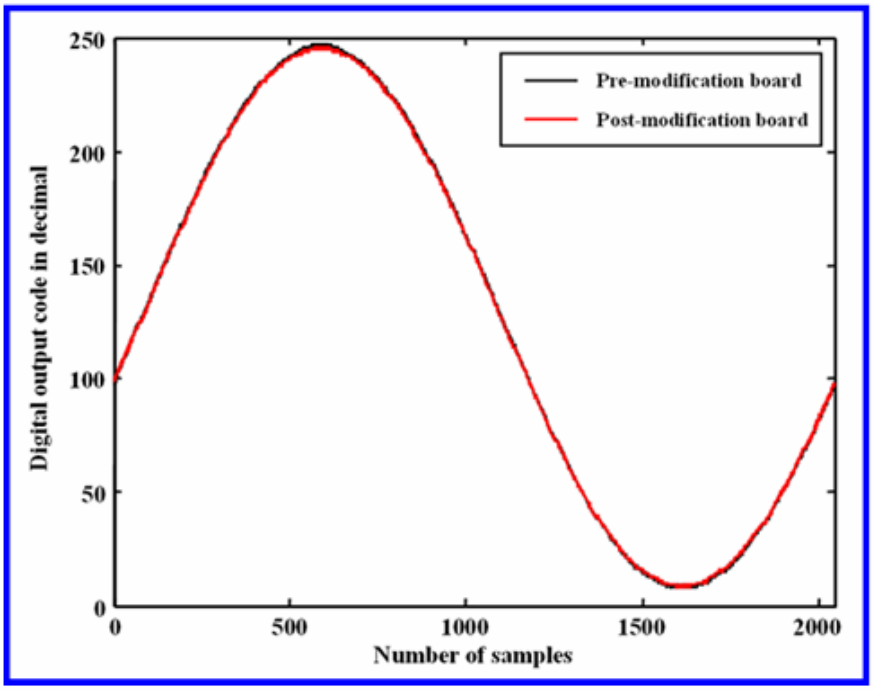


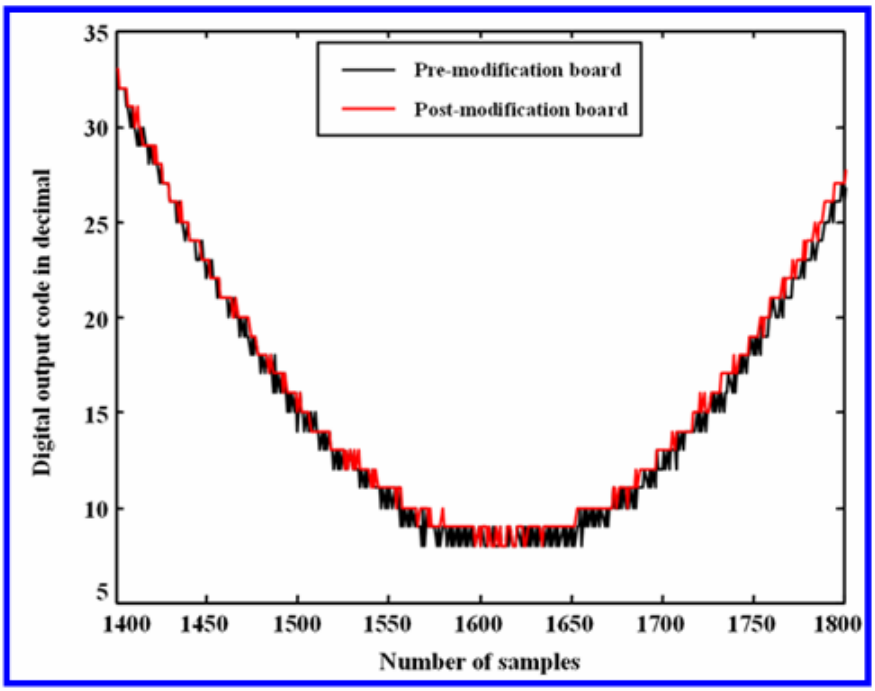
Figure 5.9: Histogram graphically summarizing and displaying the distribution of the noise comparison results shown in Table 5.2.

While the tester was on, ADC outputs were measured for both the pre-modification board and the post-modification board. For this measurement, a 747 MHz sinusoidal input was used. A single cycle of ADC output was captured to compare the ADC output between the pre-modification board and the post-modification board.

Figure 5.10 shows the ADC outputs. As shown in Figure 5.10 (b), the post-modification board showed fewer fluctuations, e.g., saw teeth for each step of digital output, than the pre-modification board.



(a)



(b)

Figure 5.10: (a) Single cycles of ADC outputs captured for a 747 MHz sinusoidal input and (b) a zoomed-in plot of the region from 1400th sample to 1800th sample in (a).

Finally, as shown in Figures 5.8 and 5.9, the post-modification board shows improvement in terms of noise spectra at 11 locations, while there was no change at 2 locations and deterioration at 1 location among the 16 locations from P1 to P16. A mixed result was shown at P1 and P6. The post-modification board shows fewer “saw-teeth” fluctuations, which usually result from noise, on each step of digital output.

5.5 Summary

In this Chapter, the electromagnetic band gap (EBG) structure was presented to suppress the power/ground noise on a 1.5Gbps and dual 8-bit ADC load board. The load board was successfully designed, fabricated, and measured. The post-modification board showed improvements in terms of noise spectra at 11 locations, while there was no change at 2 locations and deterioration at 1 location among the 16 locations from P1 to P16. A mixed result was shown at P1 and P6. The post-modification board also showed fewer saw-teeth fluctuations, which usually result from noise, on each step of digital output.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

With today's demand for devices having more functionality and reduced sizes, the integration of mixed signal modules into a tightly-designed system in which digital signals are combined with RF/analog signals is crucial. Noise isolation is a key to the success of high-performance mixed-signal modules. Electromagnetic band gap (EBG) structures are promising solutions for power/ground noise isolation in mixed signal systems. This is due to the characteristic that the periodicity of the EBG structures prohibits electromagnetic wave propagation over certain frequency bands called stop bands. Another advantage of the EBG structures is that the EBG structures can be easily implemented into a system requiring a single power supply without additional vias or layers, which can be expensive.

However, in spite of the fact that EBG structures have become important for switching noise (power/ground noise) management in mixed-signal systems, there has been no design method for the synthesis of EBG structures based on specifications. Therefore, this research focused on the development of EBG synthesis method for mixed signal applications.

6.1 Conclusions

Based on the work presented in Chapters 2 through 6, the contributions of this research can be listed as follows:

- The development of synthesis method for one-dimensional electromagnetic band gap (EBG) structures.

1. Three new approaches have been suggested: current patch approximation method (CPA-Method), border to border radius (B2BR), and power loss method (PLM). CPA-Method is based on the current flow on a periodically patterned power/ground plane. CPA-Method gives a final dimension of EBG structure for a desired stop band frequency. B2BR determines the maximum number of patches implementable within a given area. PLM calculates isolation level of an EBG structure based on the transmitted power.

2. The proposed approaches have been combined together to synthesize EBG structures for given specifications. The synthesized EBG structure with these approaches has been fabricated and verified with electromagnetic (EM) simulation and measurement.

- The development of electromagnetic band gap (EBG) synthesizer using genetic algorithm (GA).

1. GA concepts have been adopted for the development of the EBG synthesizer. A new method has been suggested to encode an EBG structure as genes and to create a string of genes to form a chromosome. A unit cell making up an EBG structure is discretized into square cells. Each square cell is expressed with digital symbols according to whether it is a void or a solid. For a void cell, '0' is assigned, and for a solid cell, '1' is assigned. Finally, a patch is expressed by a string of the digital symbols.

2. General GA has been modified to achieve faster and more efficient convergence to a final EBG design meeting design specifications. Two new methods have been introduced to ensure continuity in current paths and connectivity between ports. Randomly generated genes result in discontinuous patch shapes for EBG structures. These discontinuous patch shapes (populations) decrease the possibility of convergence to a final solution while going through

generations. Therefore, in this synthesizer, instead of creating initial populations at random, it starts with the most reliable population (a solid patch having no holes), and then chooses columns and rows which will be created in terms of genes at random. Also, with constraining the number of columns and rows having holes to be less than 50% of the total number of columns and rows, the synthesizer lowers the possibility of generating discontinuous patch shapes. The connectivity between ports is ensured in the following manner: Starting with a port, identify all square cells that are connected either directly to this port or indirectly through other cells to this port. If as least a neighbor cell of a port (other than the first port) is one among the cells connected to the initial port, then this port is also connected to the initial port. This process is repeated for all ports that are not the initial port. If for a particular port, the connectivity test has failed, then this port is not connected to at least one of the other ports. Therefore, the population containing such a port arrangement is discarded, and the test is started with a new population.

3. The EBG synthesizer using genetic algorithm (GA) has been fully automated by combining GA with multilayer finite-difference method (M-FDM) and dispersion diagram analysis method. Populations, which are patch shapes in this application, are generated by GA. M-FDM is used to solve the patch shapes (populations in a generation) in terms of Z-parameter, and the Z-parameter of each population is converted to S-parameter and is transferred to the dispersion diagram analysis part through a conversion code. The dispersion diagram calculates stop band frequencies with the results from M-FDM.

4. In addition to the automation, the synthesized EBG structure is a cost-effective solution because the EBG structure doesn't require blind vias and additional layer. In addition, since dispersion diagram has been implemented into the synthesizer

to calculate stop band frequencies, only a patch is required to be solved which makes the method computationally effective.

- Analyses of simultaneous switching noise effect on ADC and EBG effect on the noise reduction.

1. Analysis has been conducted on possible switching noise sources for high-speed and high-resolution ADC test boards. It has been found that digital parts of ADC could be an internal noise source, and clock chips and digital chips for data processing could be external noise sources.
2. The effects of the switching noise on ADC performance have been analyzed. It has been found that the switching noise could affect four main parts of ADC: i) reference voltage, ii) input voltage, iii) sampling clock, and iv) comparator.
3. ADC performance has been modeled in the presence of the switching noise. It has been observed that the switching noise should be kept at least below 0.5LSB for ADCs to operate correctly. Based on the result, design specifications and guidelines for high-speed and high-resolution ADC test board design have been suggested.
4. As a solution to reduce the switching noise, EBGs have been introduced. The effects of the EBGs have been researched with simulations and measurements in various noise environments. It has been verified that EBGs are very effective for periodic noise reduction. However, because of wide-spread spectrum characteristic of random noise, EBGs need very cautious application to random noise reduction.

- Low-noise load board design for gigahertz analog-to-digital converters with EBG structures.

1. As an application of EBG structures, a prototype load board for high-resolution and gigahertz ADC has been considered from National Semiconductor. Pre-modification board has been analyzed with simulations and measurements in both frequency-domain and time-domain.

2. Based on the pre-modification board analysis results, three major modifications have been made to the load board. First, the gap between analog power plane and digital power plane on the board has been widened as long as it doesn't hurt the connections of all pins to the proper plane to minimize the chance of noise coupling from the aggressors to the victims. Second, the digital power plane on the board has become bigger to decrease the switching noise generation by increasing the plane capacitance. Third, an EBG structure has been created on the digital power plane to minimize the area of the gap by which noise generated in digital plane can couple to analog plane.

3. Based on the modifications, post-modification board has been successfully simulated, designed, fabricated, and measured. The post-modification board has shown improvements at 11 locations, no change at two locations, and deterioration at one location among a total of 16 locations. In addition, the post-modification board has shown fewer fluctuations like saw teeth, which usually result from noise, on each step of digital output.

6.2 Future Work

The electromagnetic band gap (EBG) synthesis method in this dissertation has been developed for mixed signal applications.

As an extension to the work presented in this dissertation, the following areas of research could be of interest:

1. Synthesis of material characteristics of EBG structures

The suggested EBG synthesis method in this dissertation requires material information as input parameters. Then, based on the material information, the method synthesizes an EBG structure meeting given EBG design specifications such as an on-set frequency of band gap, an off-set frequency of band gap, and isolation level over the band gap. To implement that, an EBG structure is encoded as a string of genes in the suggested method. However, if conductor and dielectric material characteristics are encoded in terms of genes along with the EBG structure, the method will synthesize conductor and dielectric materials as well as the EBG structure.

2. Synthesis of EBG structures for a given area

The suggested EBG synthesis method in this dissertation designs an EBG structure based on given input parameters such as material characteristics, band gap frequencies, and isolation level. If the EBG structure, which is synthesized based on the given input parameters, is larger than a given area to implement the EBG structure, the EBG structure should be resynthesized with a different patch size. Therefore, if the design area can be used as a design constrain for EBG synthesis, tuning of the EBG structure will be much easier when the structure is applied to a real application.

6.3 Publications, Inventions, and Awards

[1] **Tae Hong Kim**, D. Chung, E. Engin, Y. Toyota, W. Yun and M. Swaminathan, "A Novel Synthesis Method for Designing Electromagnetic Band Gap (EBG) Structures in Packaged Mixed Signal Systems," *IEEE 56th The Electronic Components and Technology Conference,* pp. 1645-1651, May 2006. – **[Outstanding Poster Paper Award]**

[2] **Tae Hong Kim**, E. Engin, and M. Swaminathan, "Switching Noise Suppression in Mixed Signal System Applications Using Electromagnetic Band Gap (EBG) Synthesizer," *IEEE Electrical Performance of Electronic Packaging (EPEP) 2006*, pp. 47-50, Oct. 23-25, 2006.

[3] **Tae Hong Kim**, E. Engin, and M. Swaminathan, "Electromagnetic Band Gap (EBG) Structure Synthesizer Using Genetic Algorithm for Wireless System Applications," *IEEE Asia-Pacific Microwave Conference (APMC) 2006*, Yokohama Japan, Dec. 12-15, 2006.

[4] **Tae Hong Kim**, E. Engin, M. Swaminathan, and P. Yadav, "Automated Tool for Electromagnetic Band Gap (EBG) Synthesis in Mixed Sigal Applications," *IEEE Asia-Pacific Microwave Conference (APMC) 2007*, Bangkok, Thailand, Dec. 11-14, 2007.

[5] **Tae Hong Kim**, M. Swaminathan, E. Engin, and A. Tambawala, "Electromagnetic Bandgap Structures – Design, Modeling, and Integration in Mixed Signal Modules," *IMAPS 40th International Symposium on Microelectronics*, San Jose, CA, Nov. 11-15, 2007. – **[IMAPS 2007 Best of Session Award]**

[6] **Tae Hong Kim**, M. Swaminathan, E. Engin, and B. J. Yang, "Electromagnetic Band Gap Synthesis Using Genetic Algorithms for Mixed Signal Applications," submitted to *IEEE Transaction Advanced Packaging*, 2007.

[7] D. Chung, **Tae Hong Kim**, C. Ryu, E. Engin, M. Swaminathan, and J. Kim, "Effect of EBG Structures for Reducing Noise in Multi-Layer PCBs for Digital Systems," *IEEE Electrical Performance of Electronic Packaging (EPEP) 2006,* pp. 253-256, Oct. 23-25, 2006.

[8] Y. Toyota, A. Engin, **Tae Hong Kim**, and M. Swaminathan, "Stopband Analysis Using Dispersion Diagram for Two-dimensional Electromagnetic Bandgap Structures in Printed Circuit Boards," *IEEE Microwave and Wireless Components Letters,* vol. 16, pp. 645-647, Dec. 2006.

[9] T. Spencer, P. Joseph, **Tae Hong Kim**, M. Swaminathan and P. A. Kohl, "Air-gap transmission lines on organic substrates for low-loss interconnects," *IEEE Transactions on Microwave Theory and Techniques*, pp. 1919-1925, Sep. 2007.

[10] N. Altunyurt, **Tae Hong Kim**, and M. Swaminathan, "Printed Monopole Antennas with Increased Bandwidth and Gain for Wi-Fi Applications," *IEEE Antennas and Propagation Society 2007*, June 2007, Hawaii USA.

[11] Y. Toyota, A. Engin, **Tae Hong Kim**, M. Swaminathan, and K. Uriu, "Stopband Prediction with Dispersion Diagram for Electromagnetic Bandgap Structures in Printed Circuit Boards," *IEEE Electromagnetic Compatibility (EMC) Symposium,* Portland Oregon, vol. 3, pp. 807-811, Aug. 14-18, 2006.

[12] A. Engin, Y. Toyota, **Tae Hong Kim**, and M. Swaminathan, "Analysis and Design of Electromagnetic Bandgap (EBG) Structures for Power Plane Isolation Using 2D Dispersion Diagrams and Scalability," *IEEE 10th Workshop on Signal Propagation on Interconnects,* Germany, pp. 79-82, May 09-12, 2006.

[13] Y. Toyota, A. Engin, **Tae Hong Kim**, M. Swaminathan and S. Bhattacharya, "Size Reduction of Electromagnetic Bandgap (EBG) Structures with New Geometries and Materials," *IEEE 56th Electronic Components and Technology Conference*, pp. 1784-1789, May, 2006.

• Inventions and awards

- **Tae Hong Kim**, E. Engin and M. Swaminathan, "Electromagnetic Band Gap (EBG) Structure Synthesizer Using Genetic Algorithm (GA)," U.S. utility patent application filed for GTRC ID No. 3832 Date Filed Sep. 12, 2007.

- **Tae Hong Kim**, N. Altunyurt, M. Swaminathan, R. Tummala, M. Iyer, and D. Kimberly, "High Gain Antennas for MIMO Based Wireless Applications," provisional patent application for GTRC ID No. 3996 filed Nov. 3, 2006 in the USPTO.

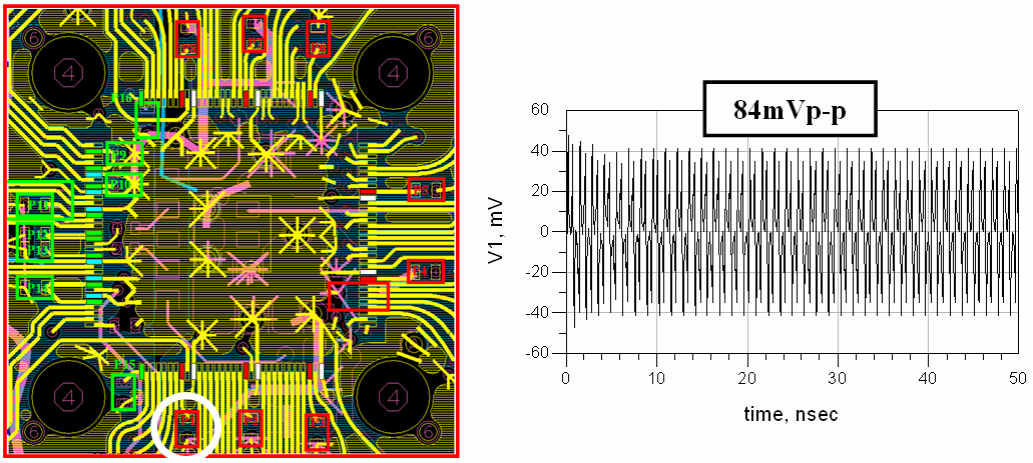
- Outstanding Poster Paper award for **the 56th Electronic Components and Technology Conference (ECTC)** in 2006.

- Best of Session award for **IMAPS 40th International Symposium on Microelectronics** in 2007, San Jose, California.

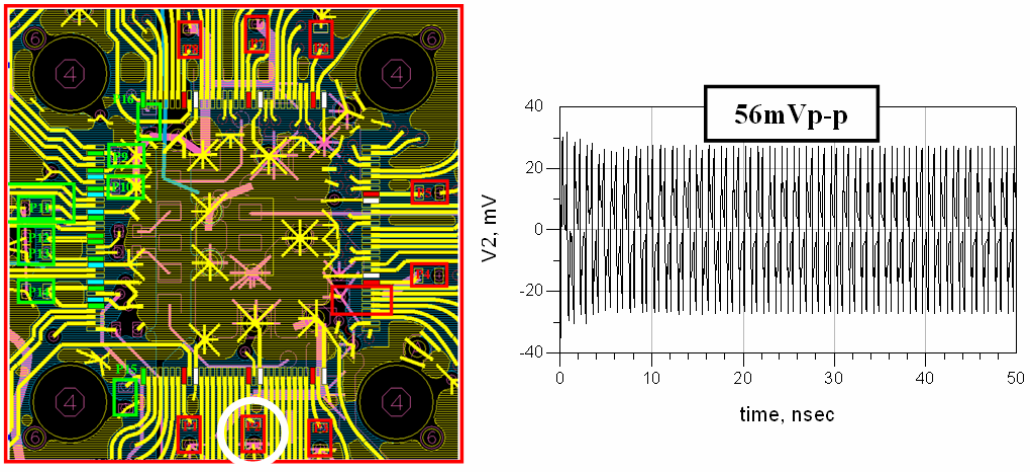
APPENDIX A

SIMULATION RESULTS FOR PRE-MODIFICATION BOARD

Simulation results for the pre-modification analysis are shown in this appendix.

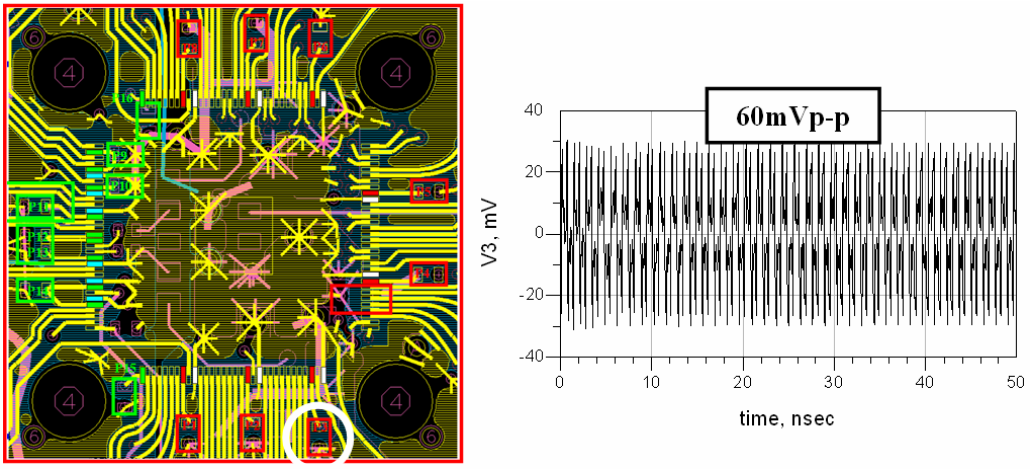


(a)

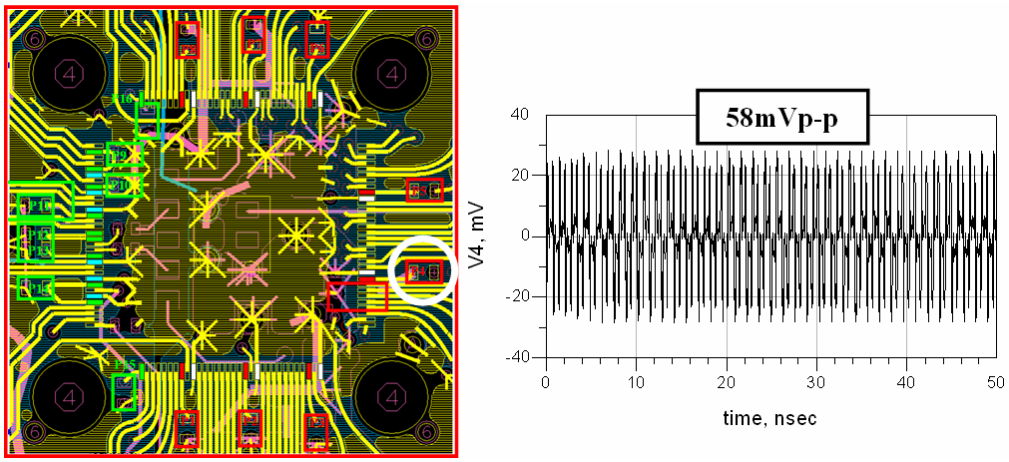


(b)

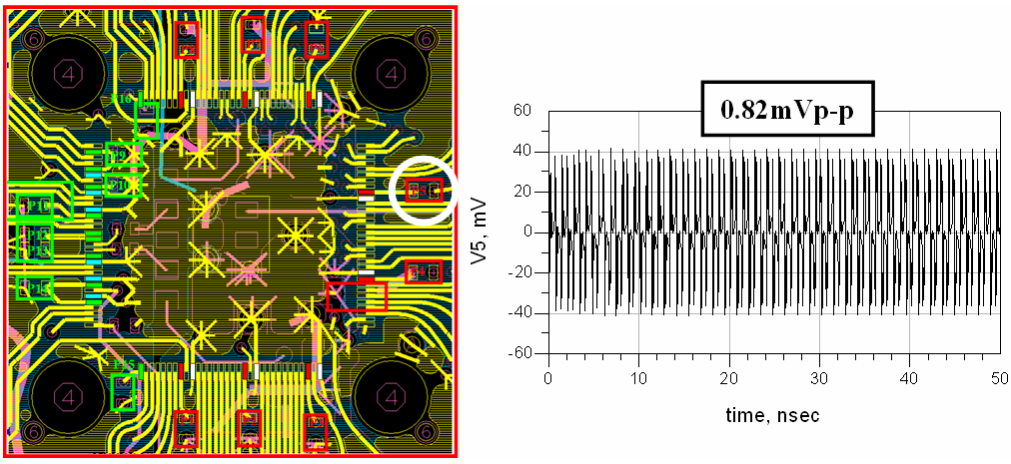
Figure A.1: The switching noise (ΔV) generated at (a) P1, (b) P2, (c) P3, (d) P4, (e) P5, (f) P6, (g) P7, and (h) P8 when each location from P1 to P8 was excited with the switching current (ΔI) of 20mAp-p and 748MHz one at a time. The white circle in the snap-shot of the board at (a) through (h) indicates locations for P1 through P8.



(c)

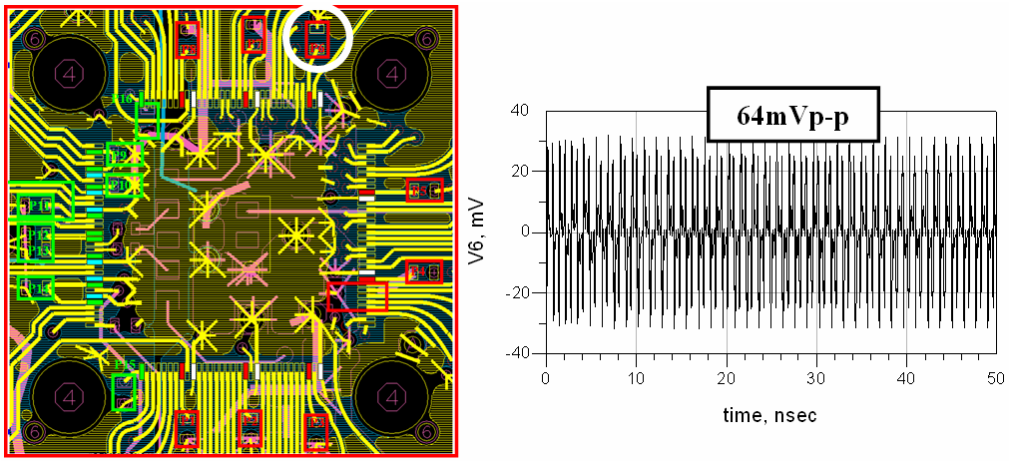


(d)



(e)

Figure A.1: Continued.



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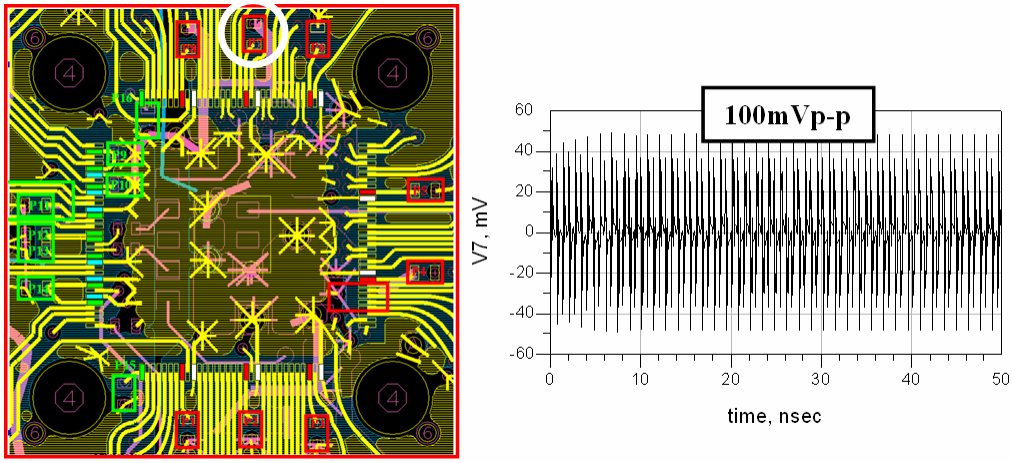
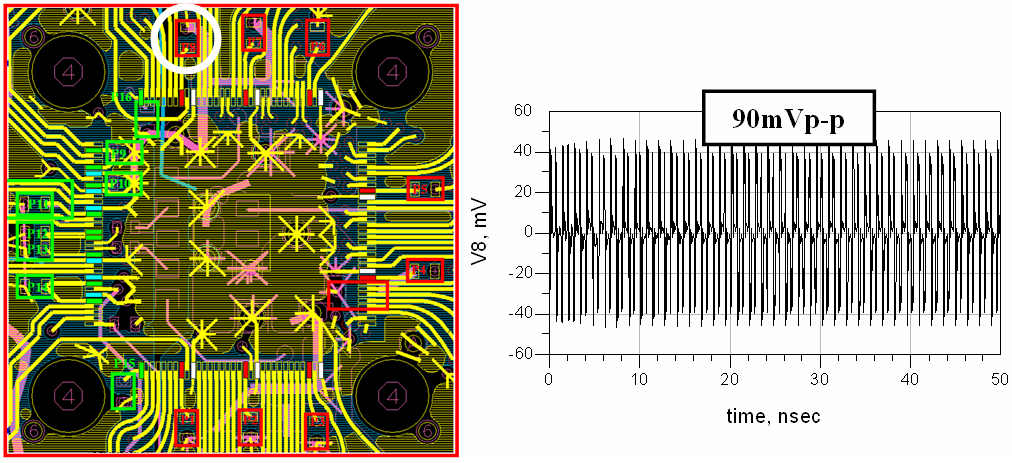
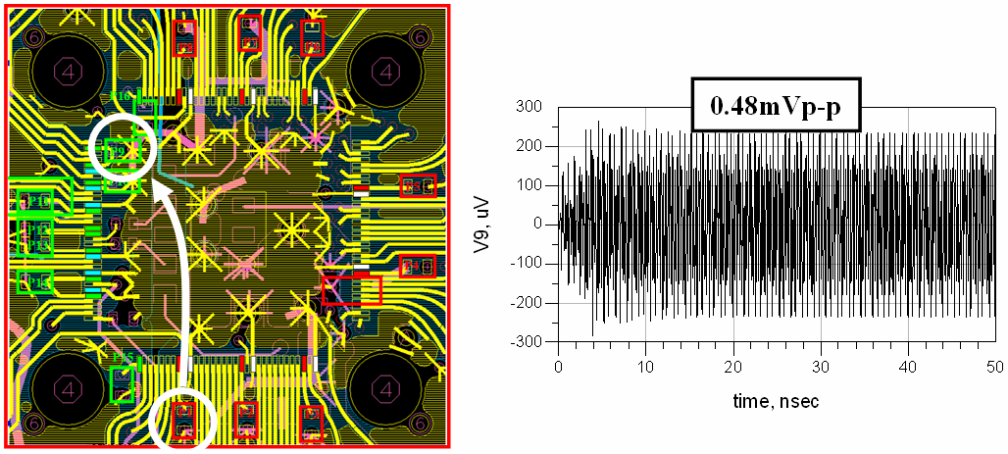


(g)



(h)

Figure A.1: Continued.



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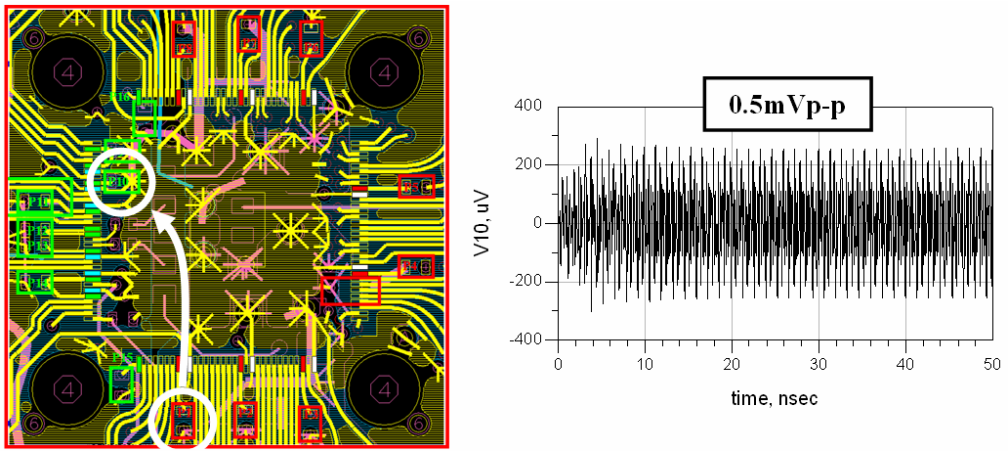
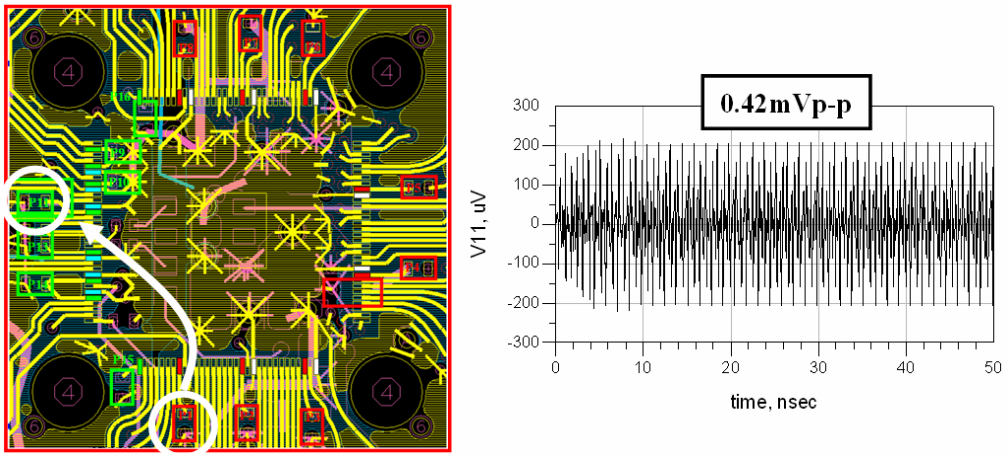
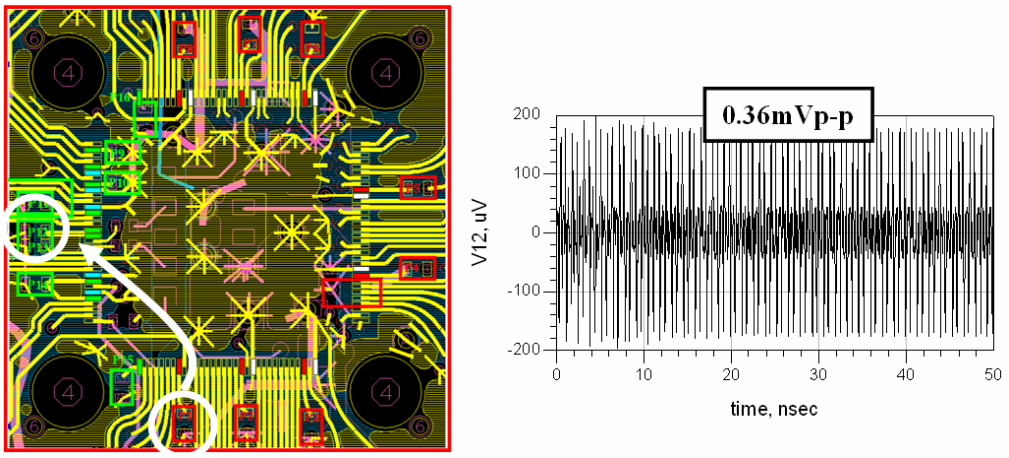


(b)



(c)

Figure A.2: The coupled noise from P1 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



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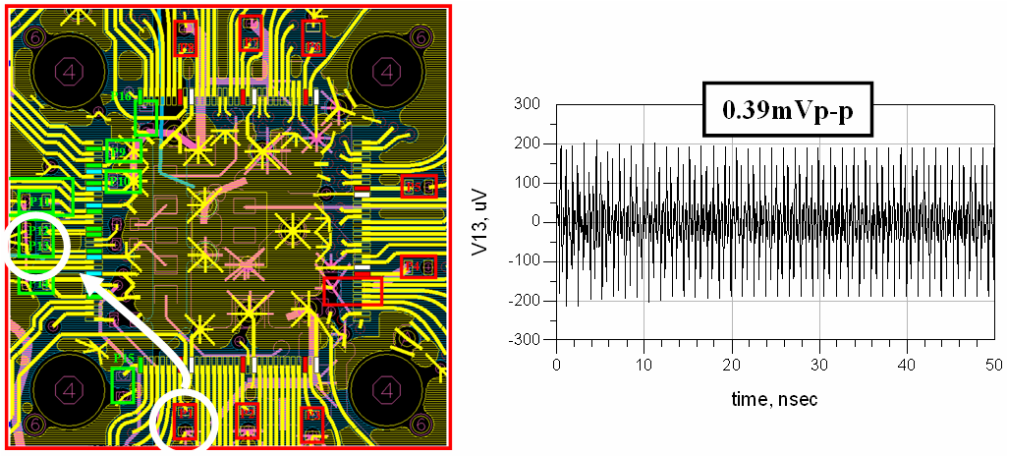

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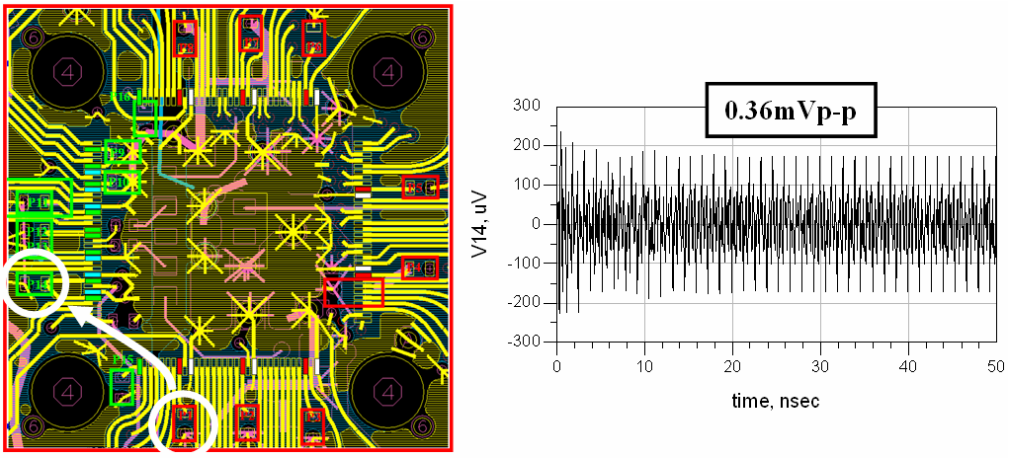

(f)

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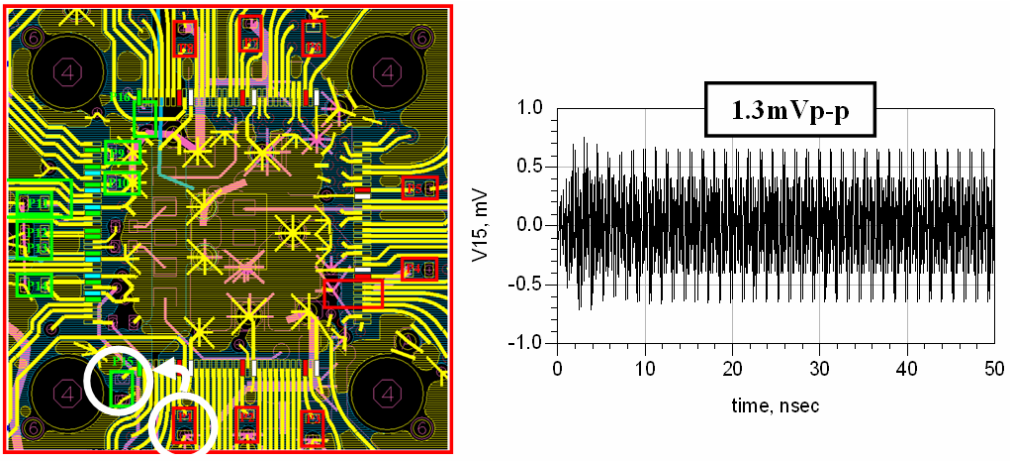

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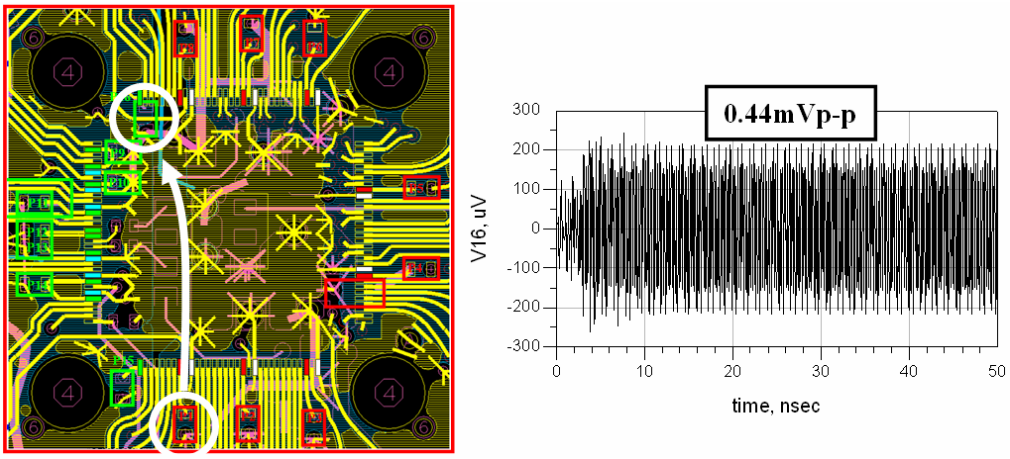

(h)

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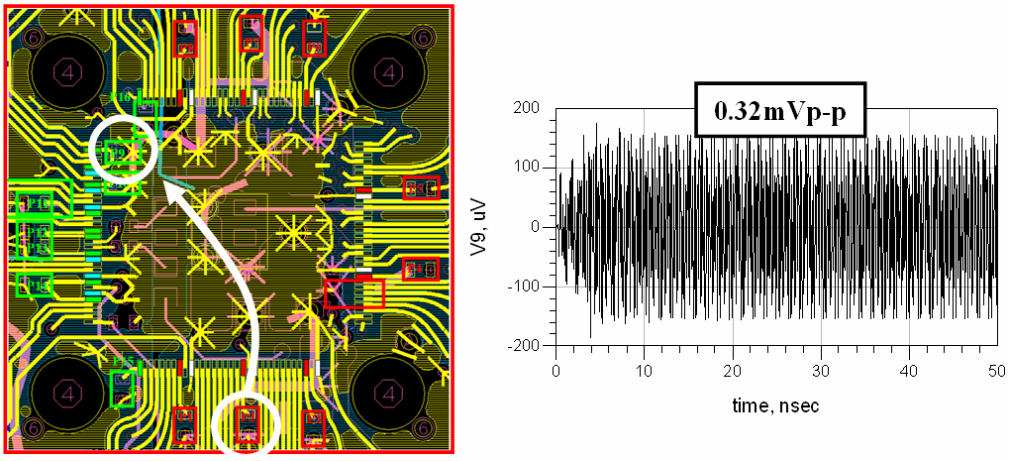

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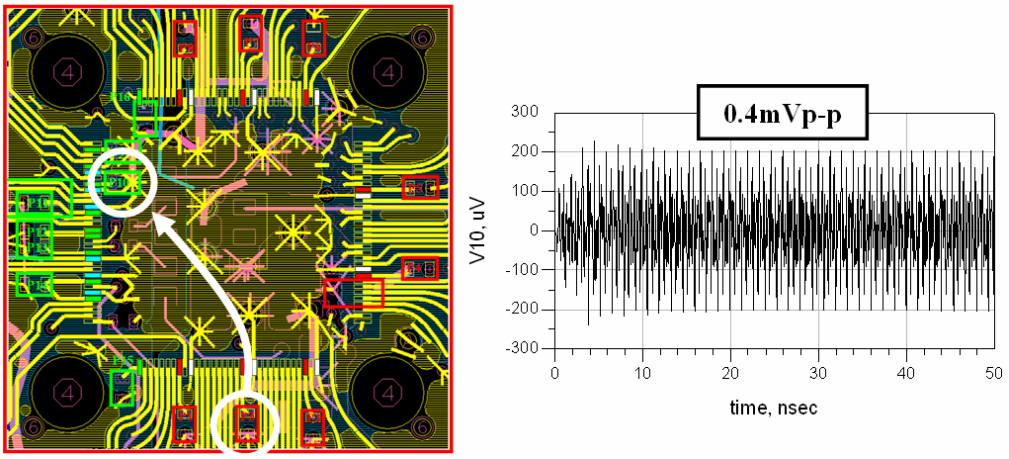

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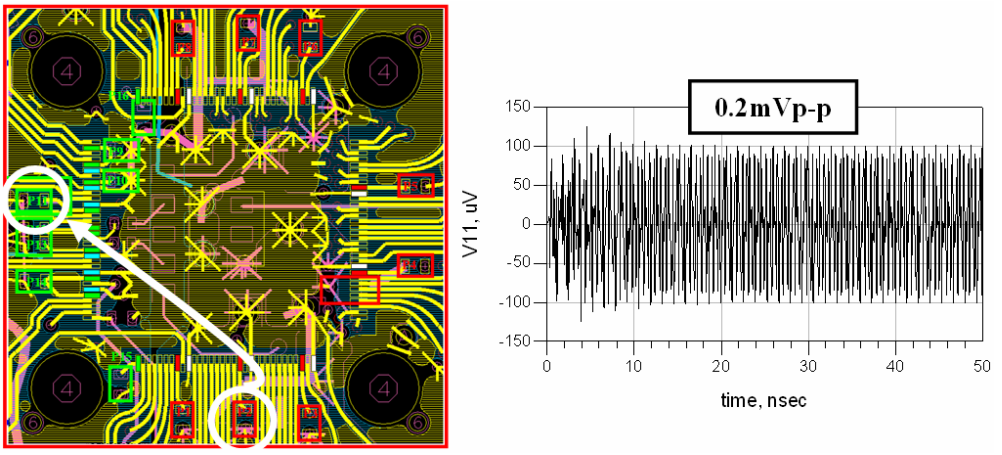
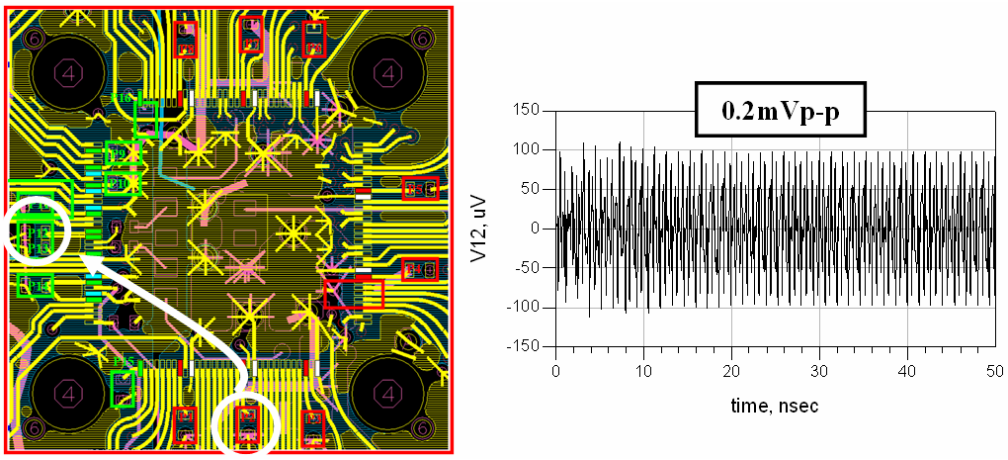


(c)

Figure A.3: The coupled noise from P2 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



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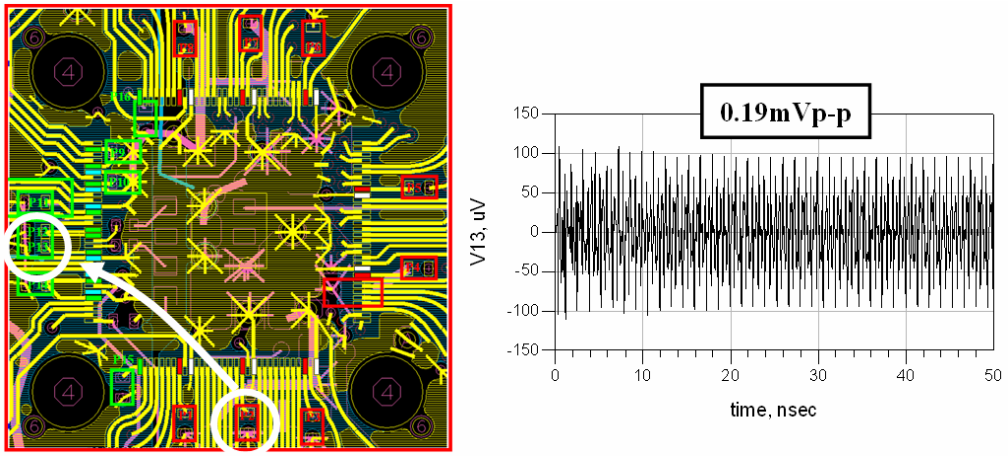

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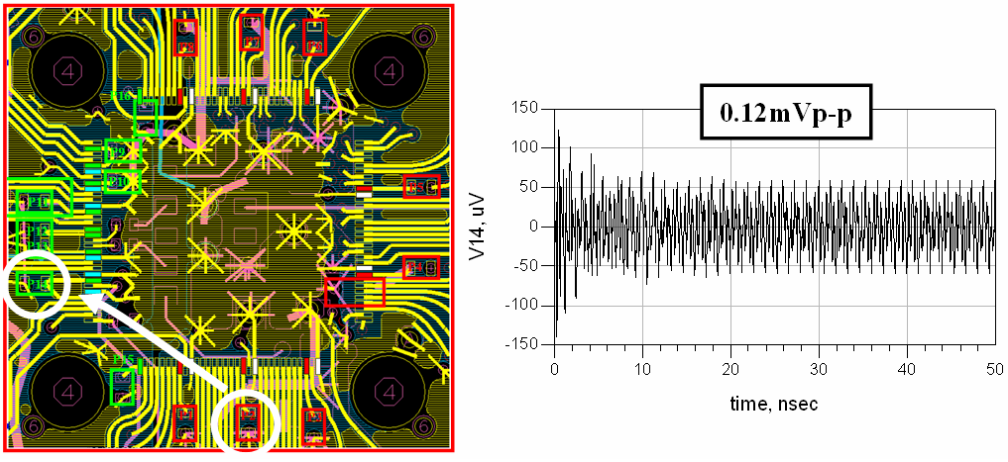

(f)

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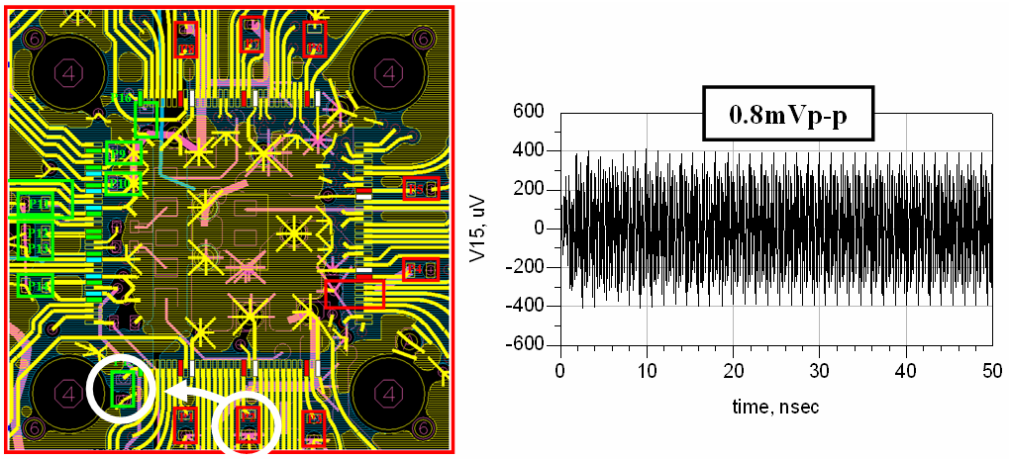

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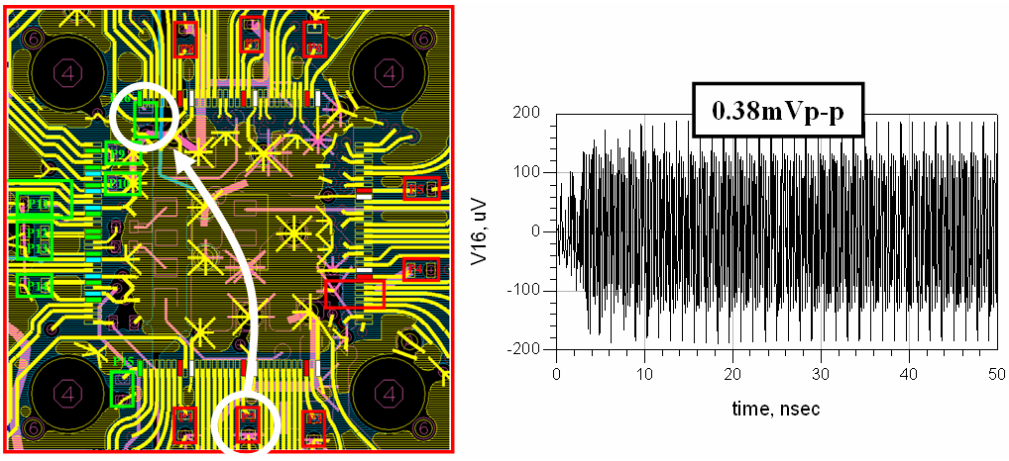

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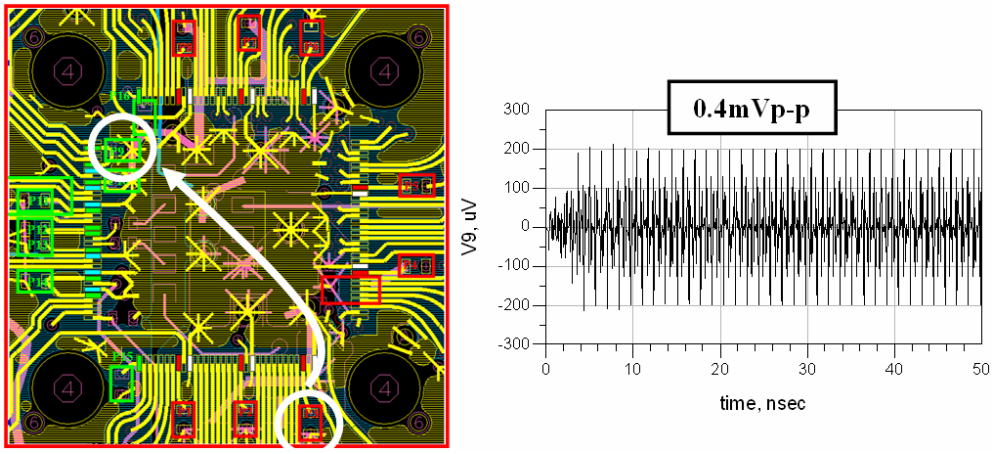
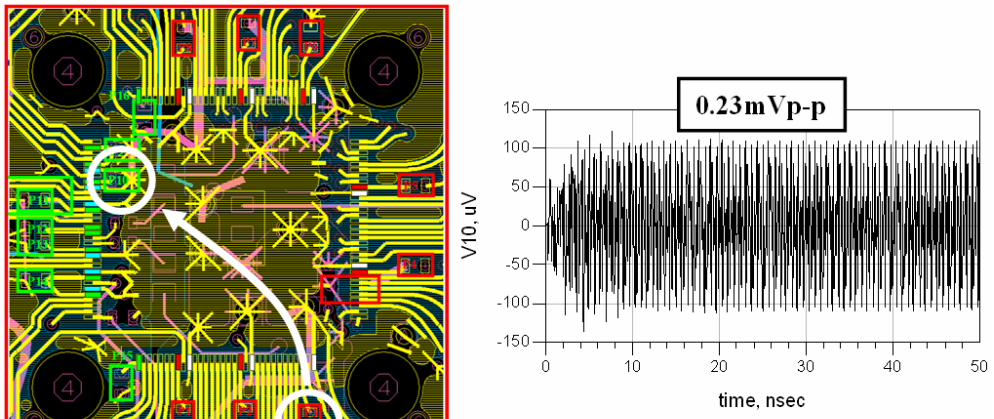


(a)



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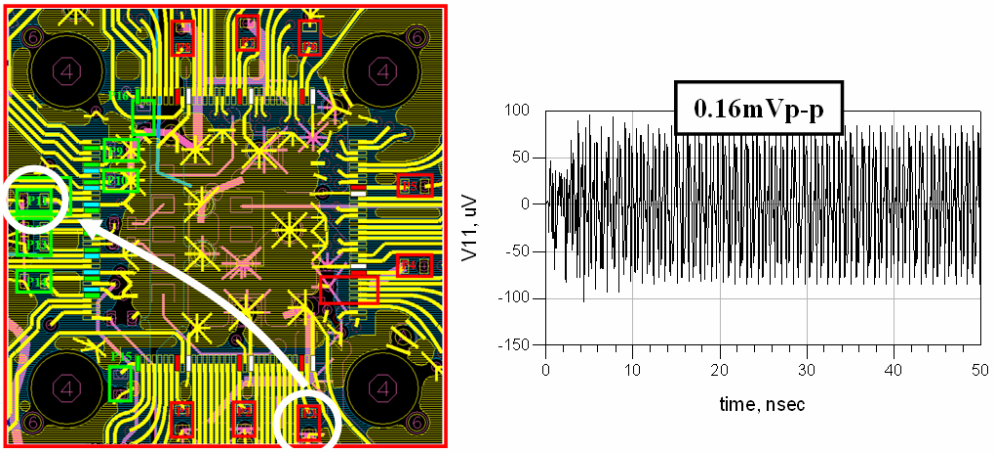
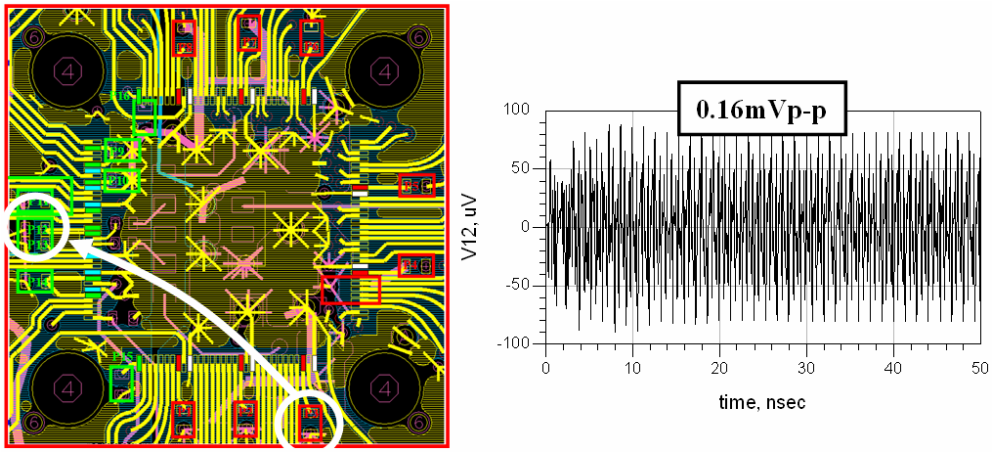


(c)

Figure A.4: The coupled noise from P3 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



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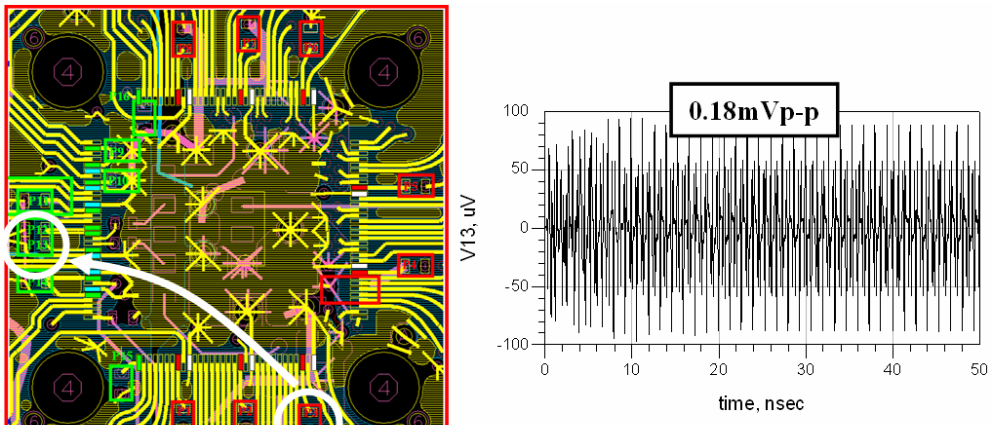
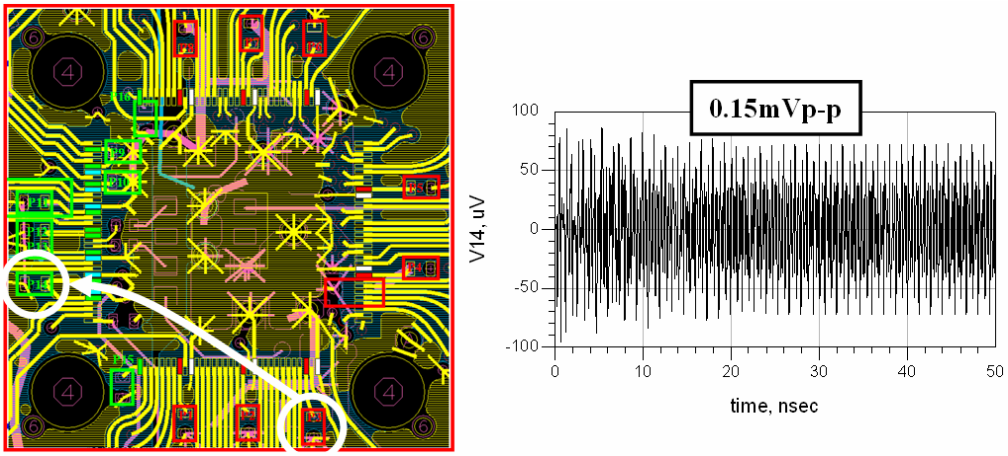


(e)



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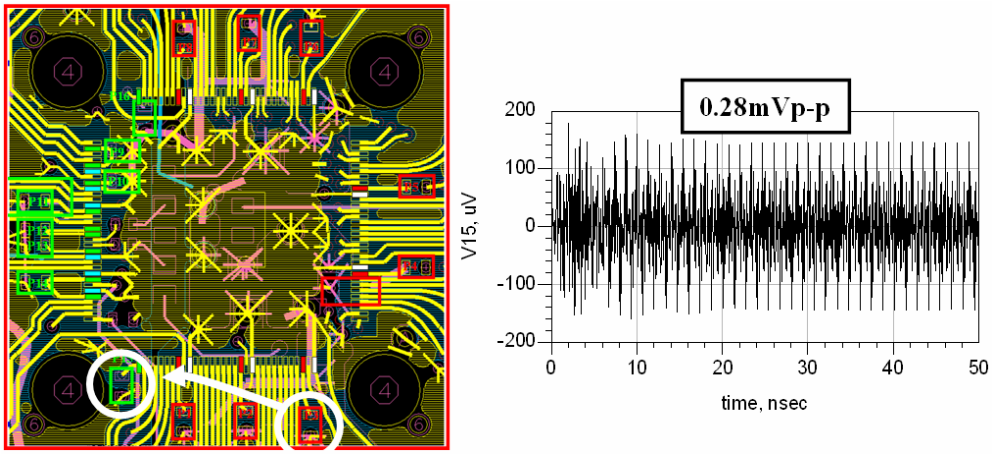

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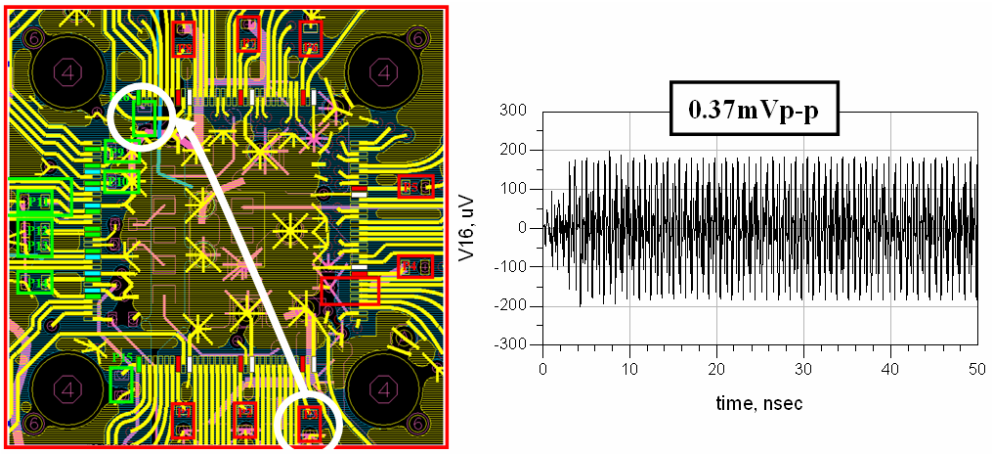

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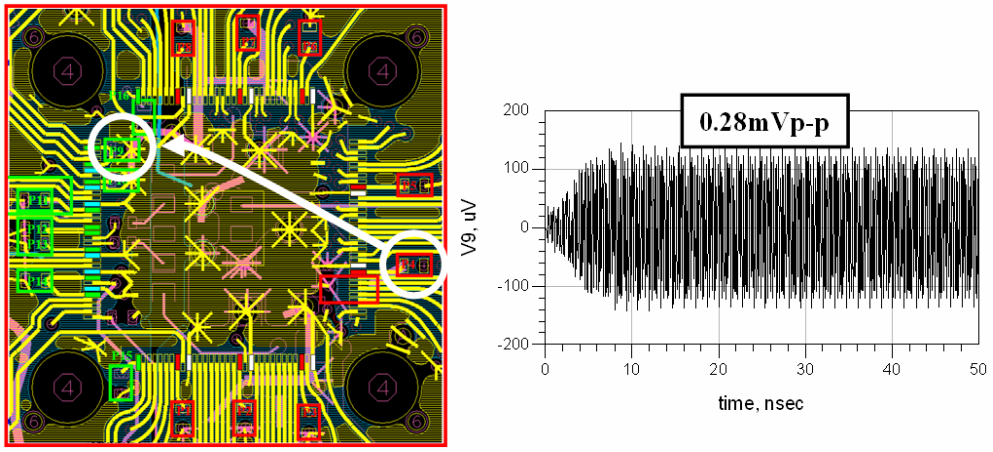

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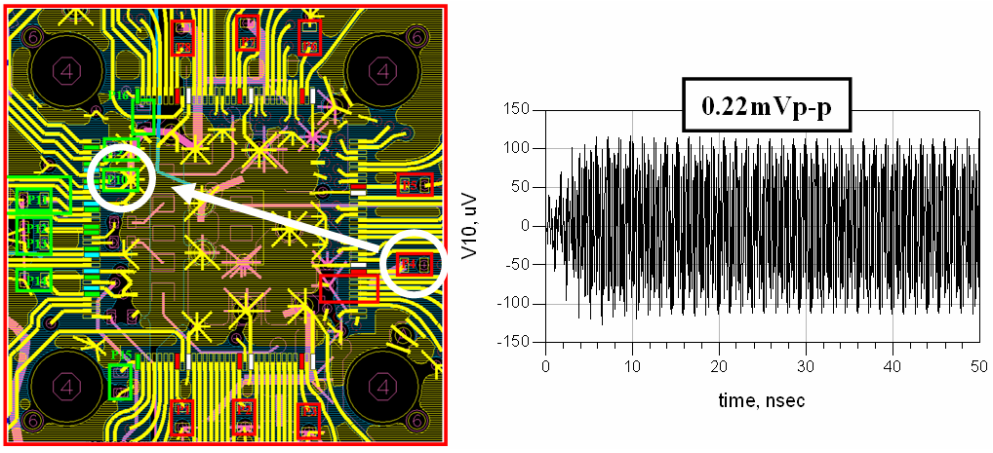

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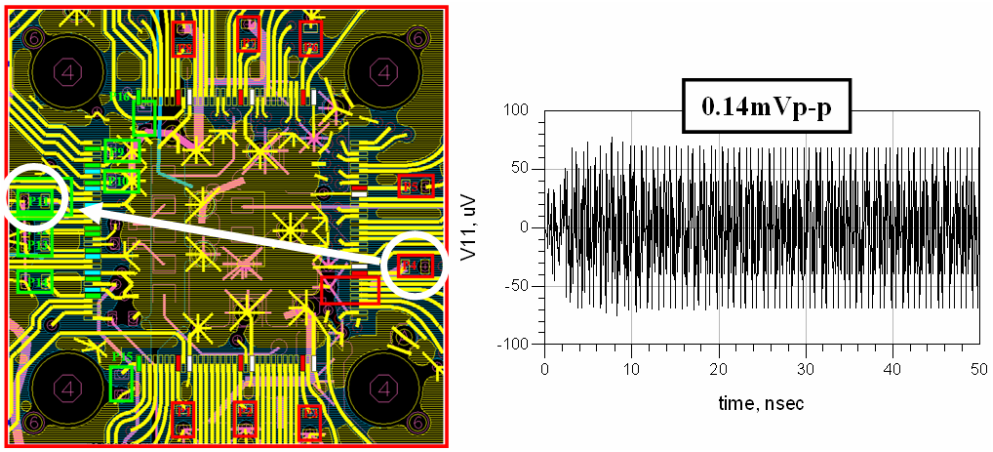
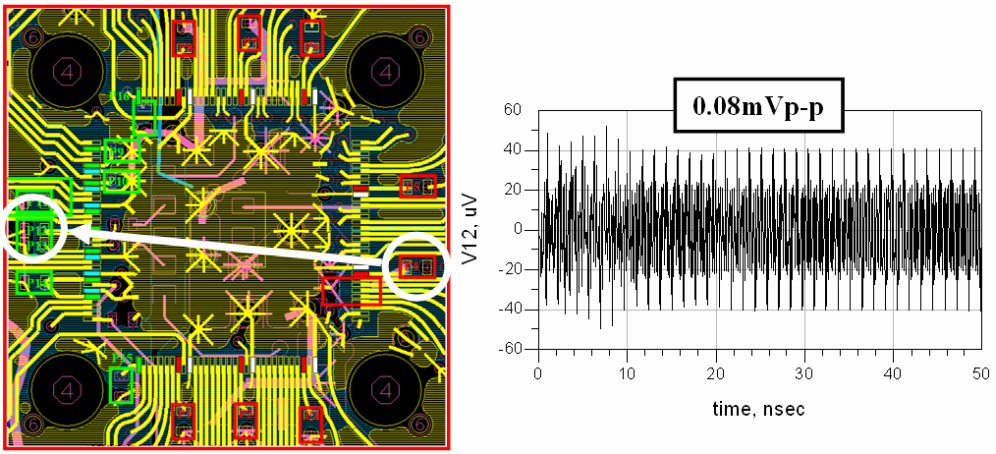


(c)

Figure A.5: The coupled noise from P4 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



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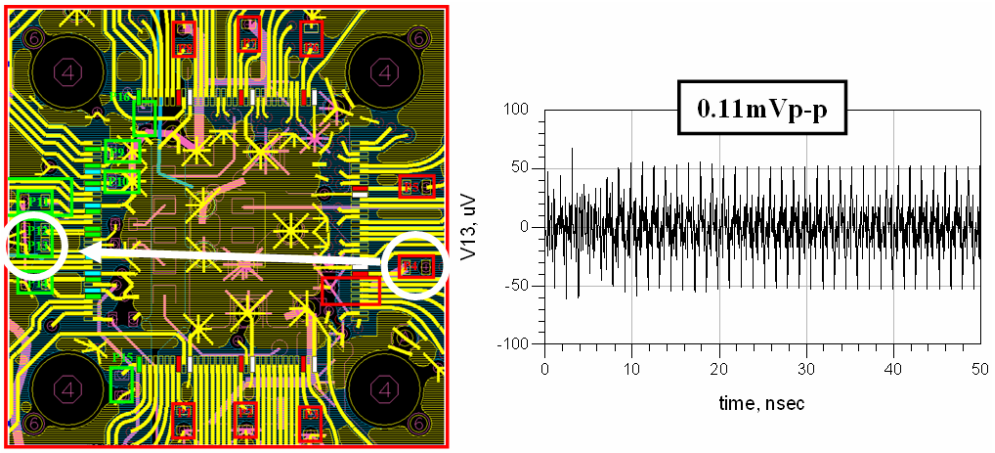

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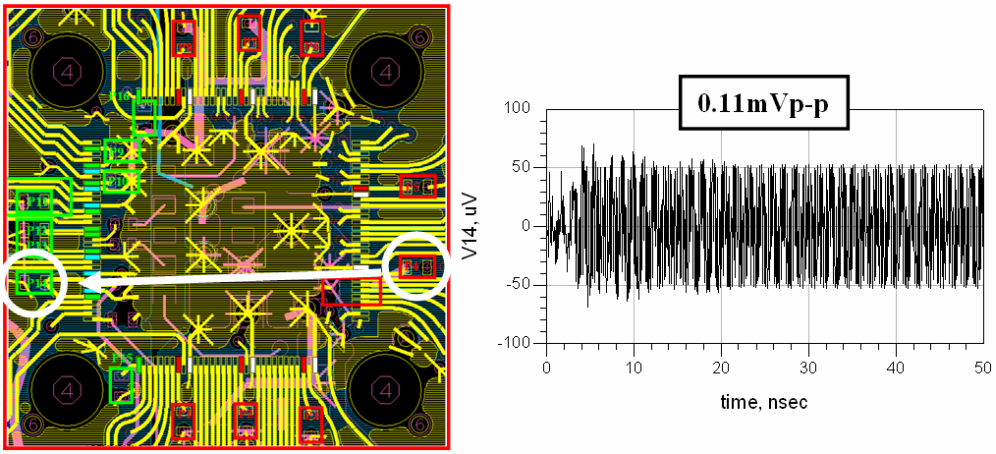

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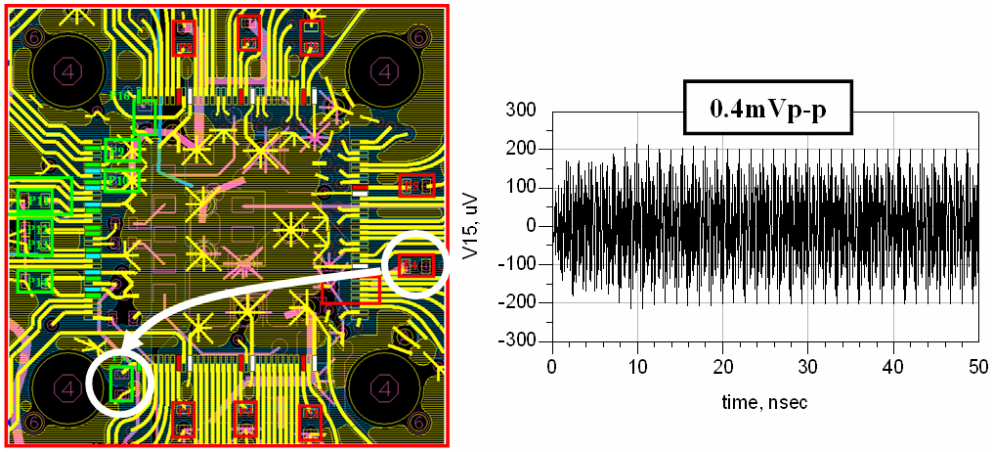
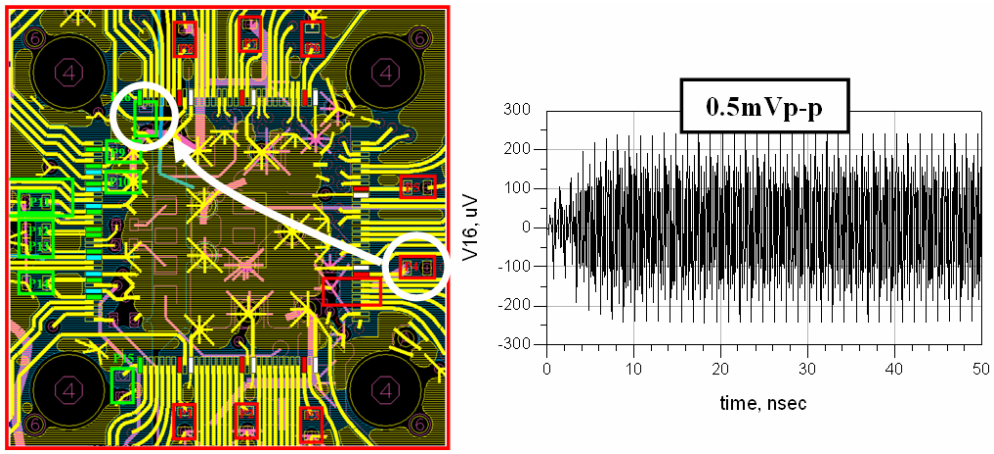
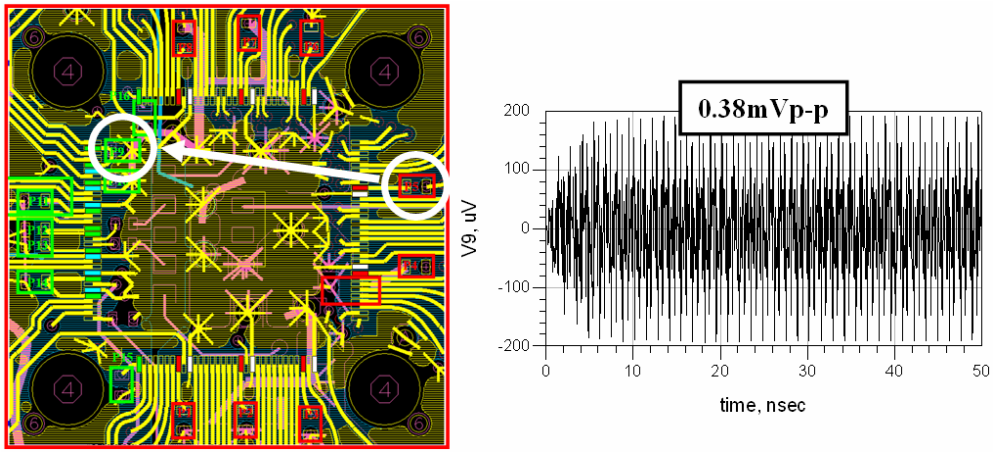


(g)

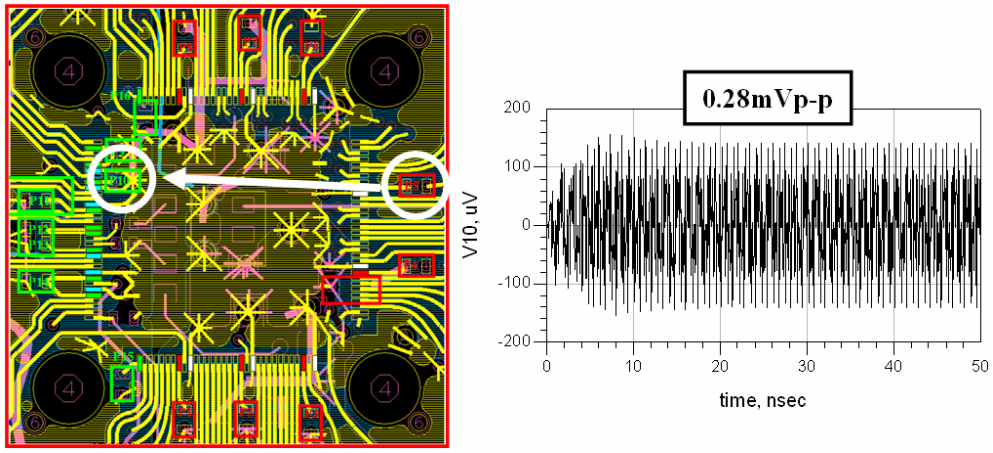


(h)

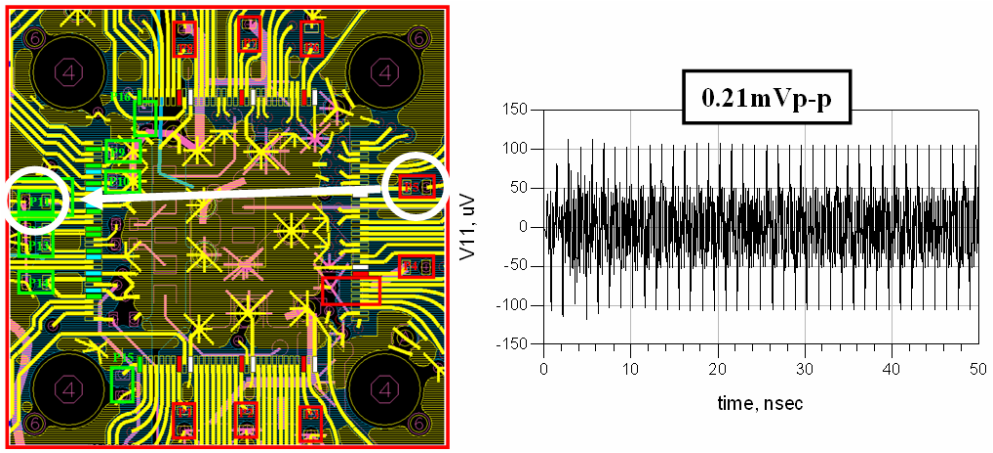
Figure A.5: Continued.



(a)

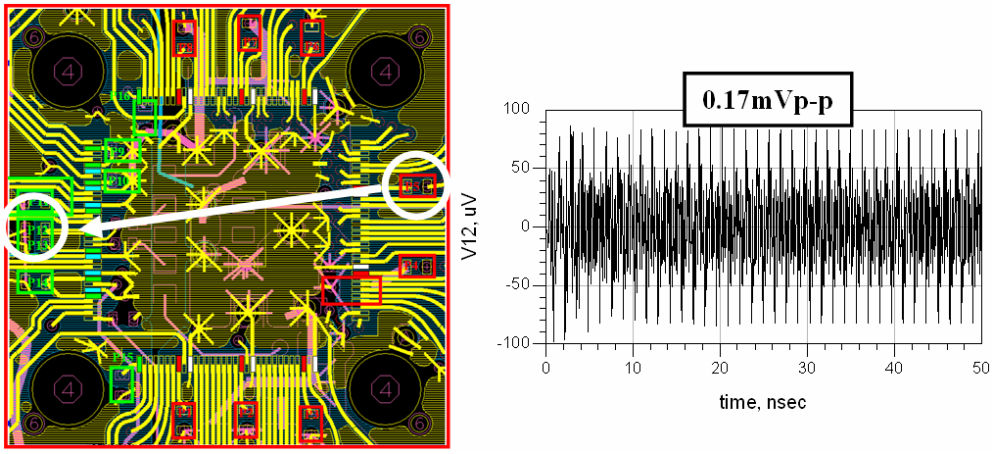


(b)

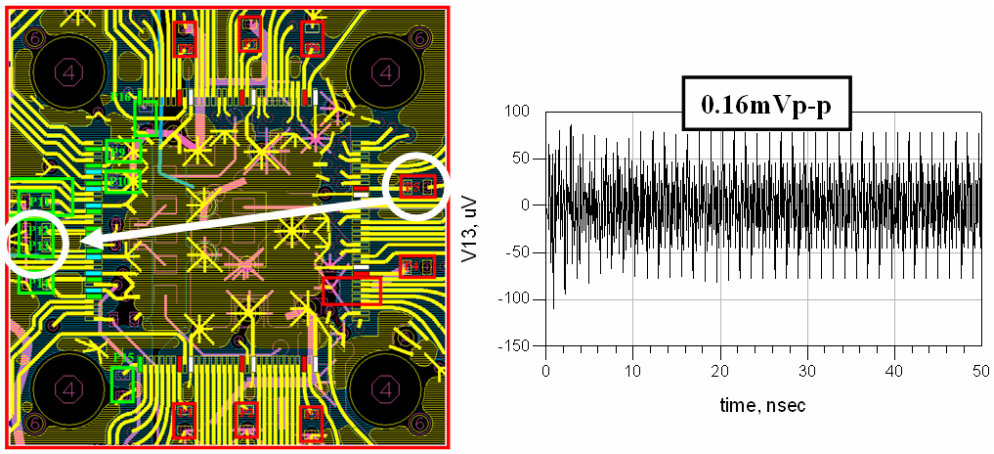


(c)

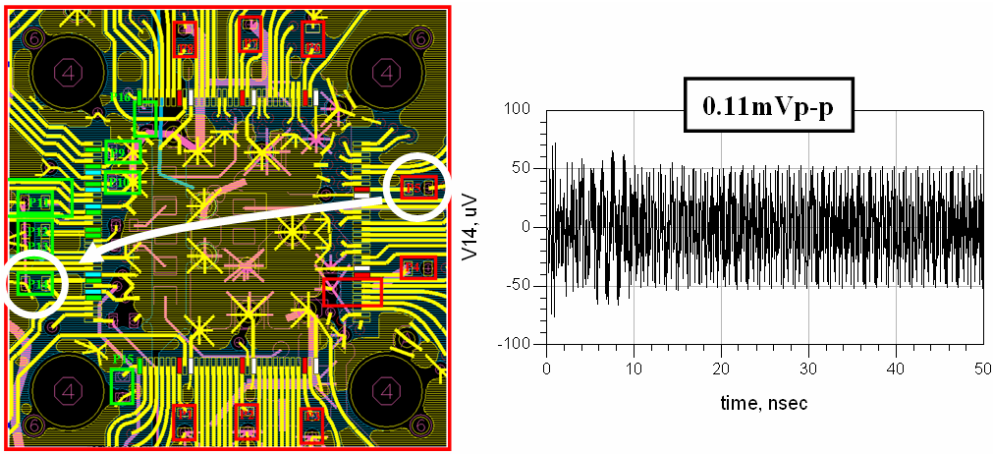
Figure A.6: The coupled noise from P5 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



(d)



(e)



(f)

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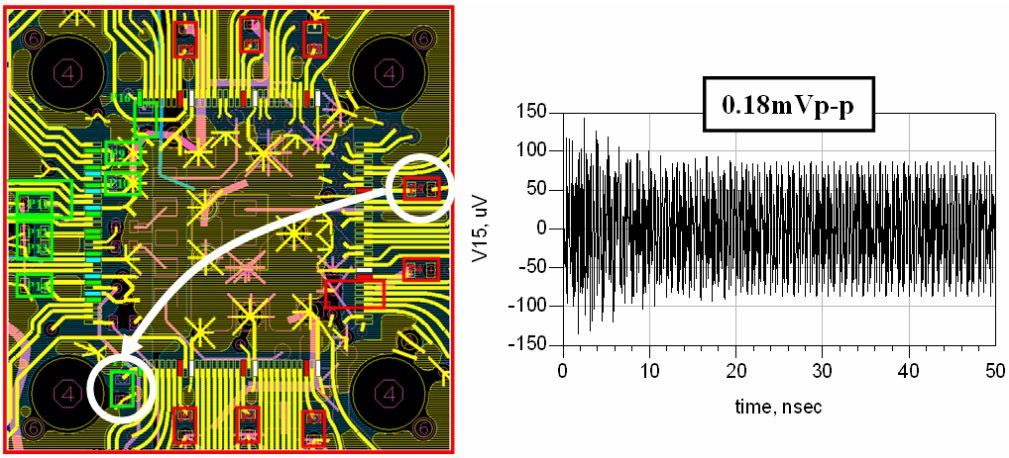
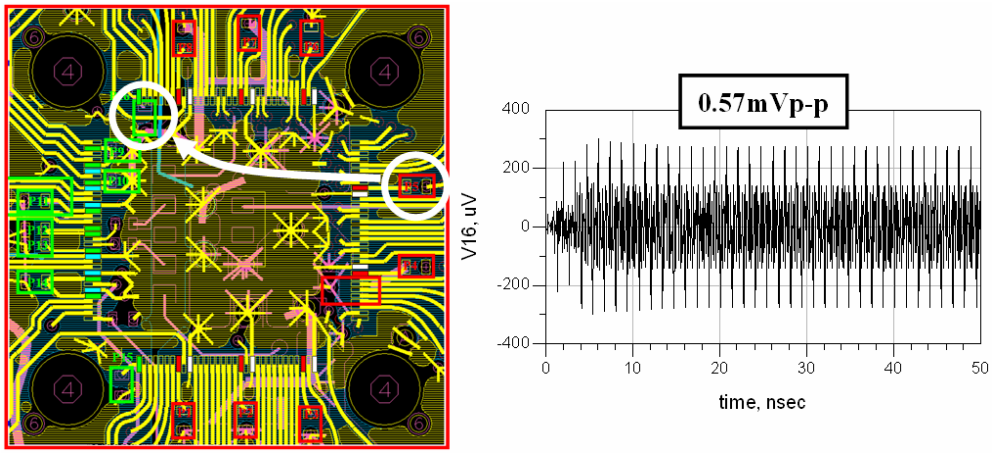
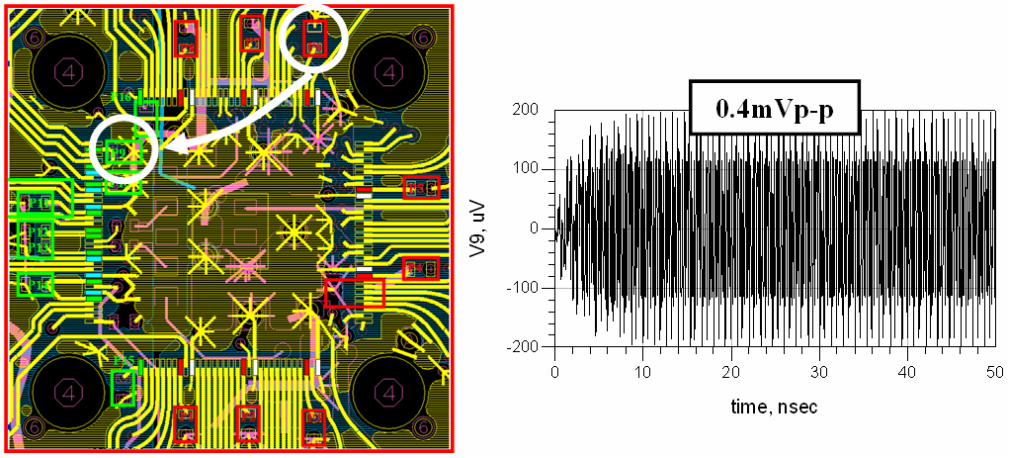


(g)

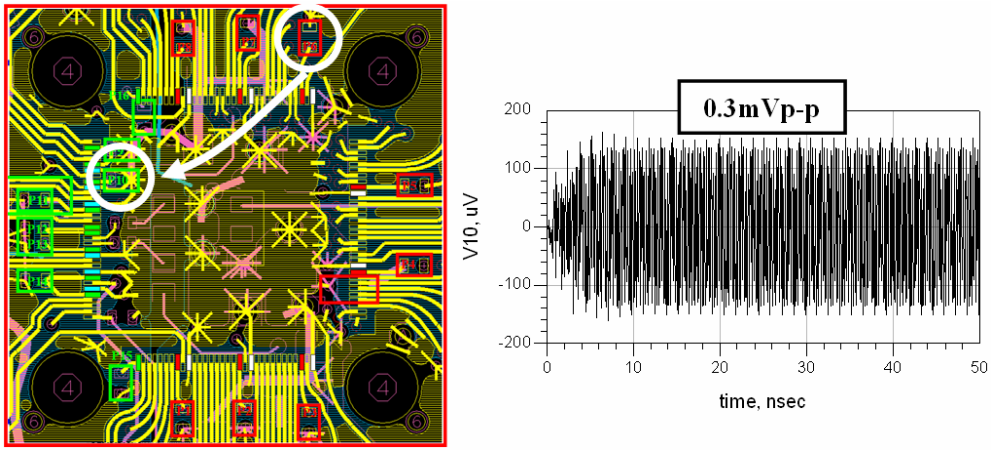


(h)

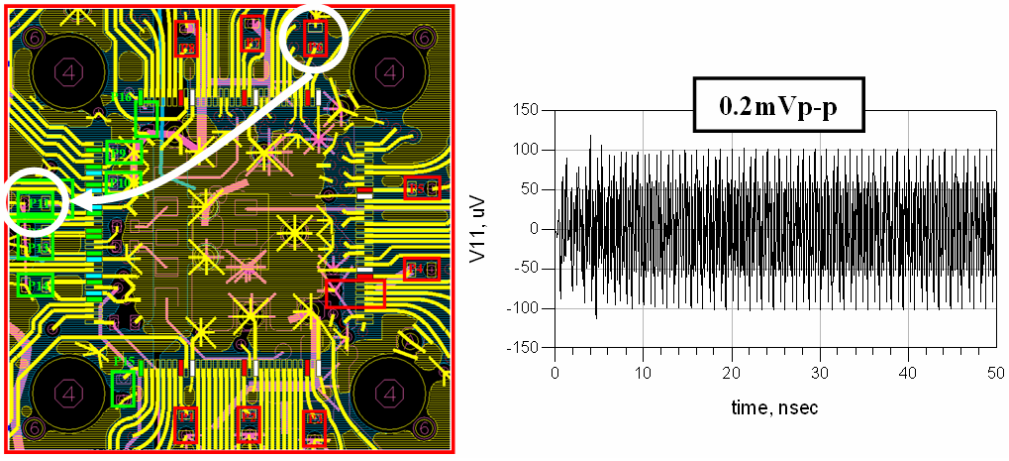
Figure A.6: Continued.



(a)

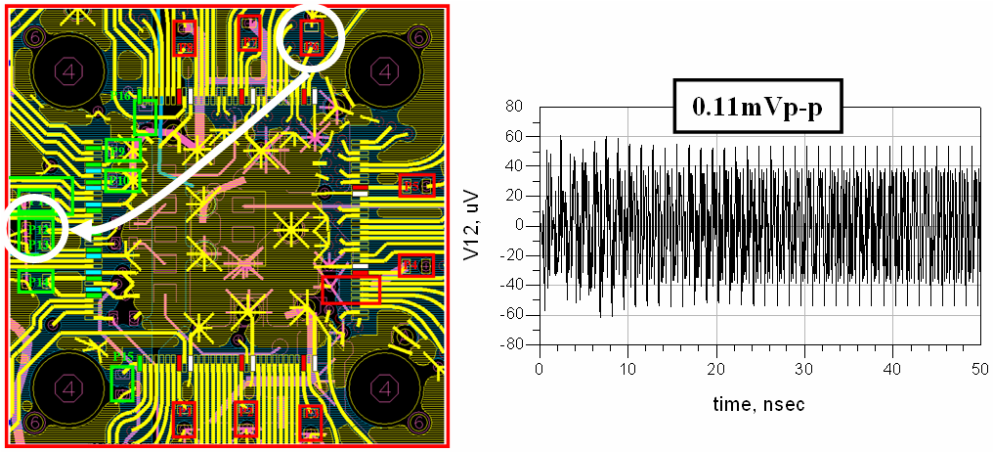


(b)

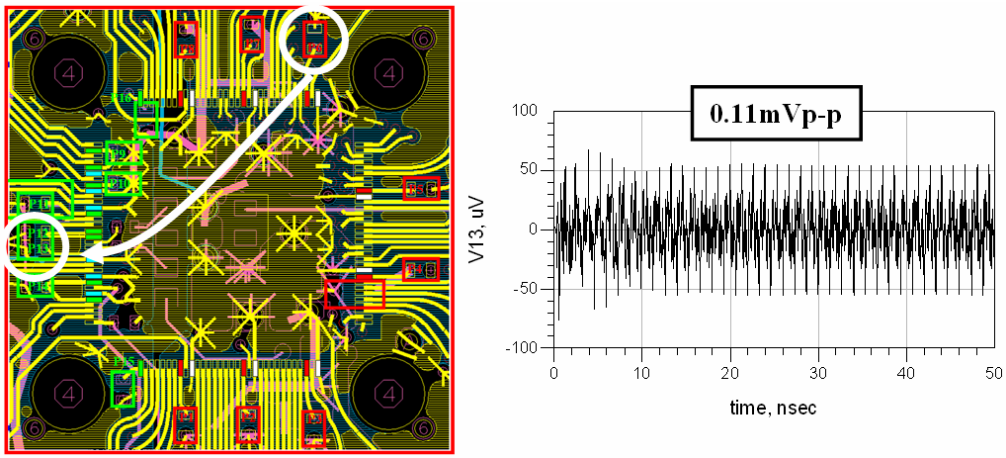


(c)

Figure A.7: The coupled noise from P6 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



(d)



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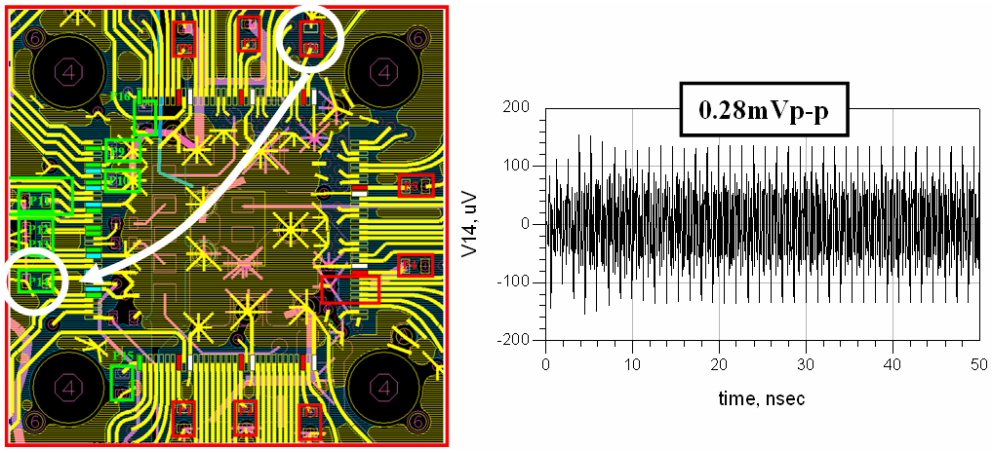
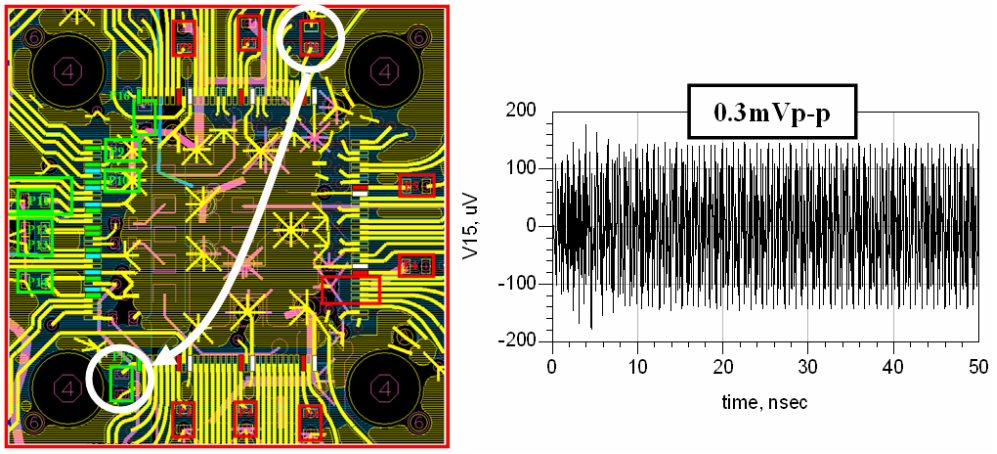
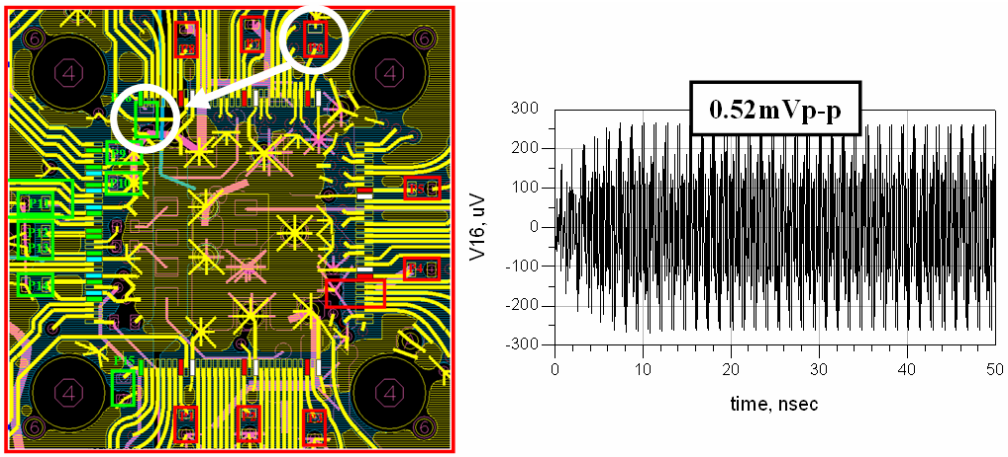


(f)

Figure A.7: Continued.

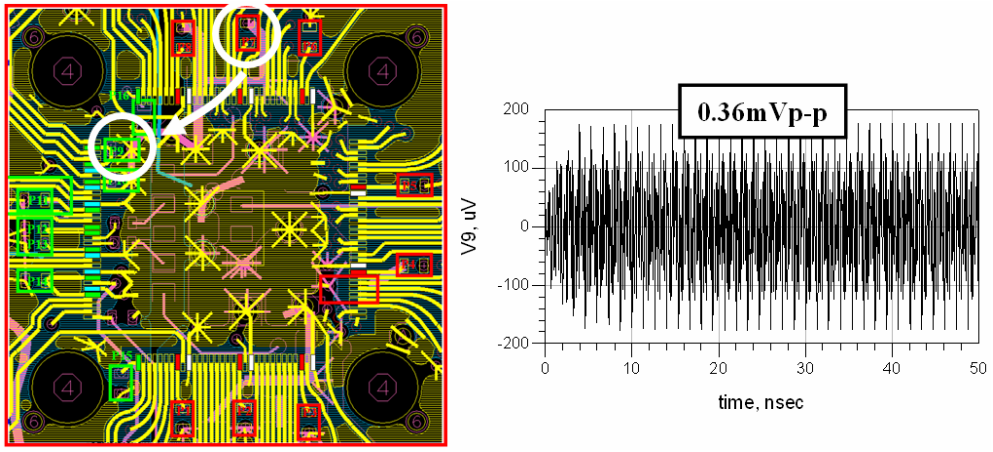


(g)

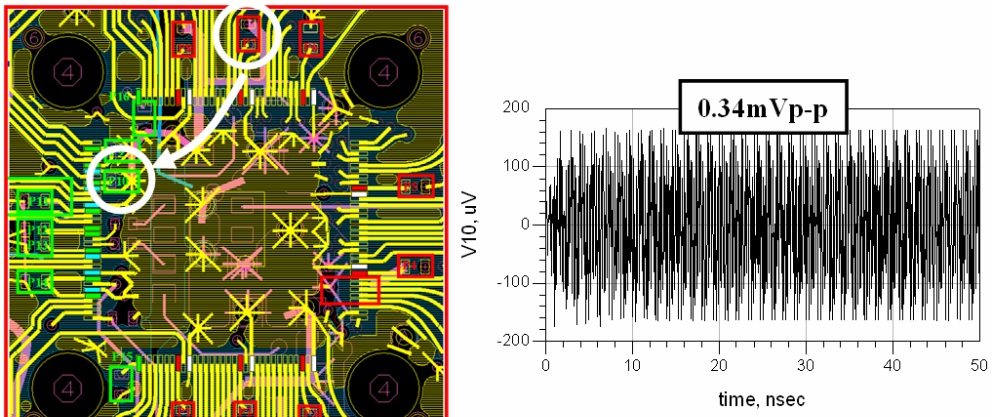


(h)

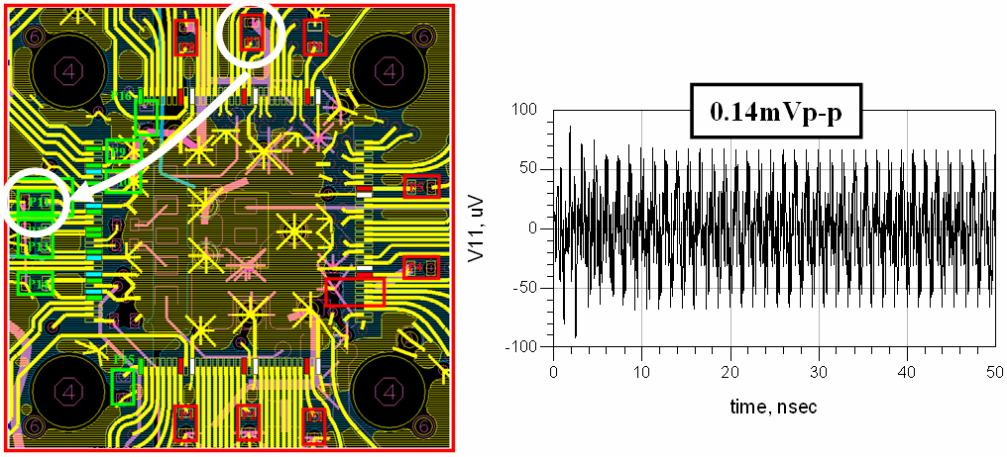
Figure A.7: Continued.



(a)

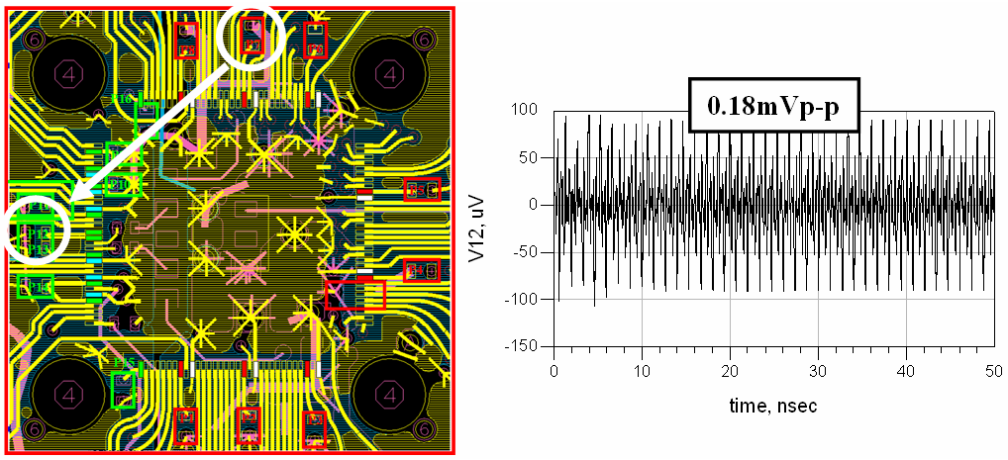


(b)



(c)

Figure A.8: The coupled noise from P7 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



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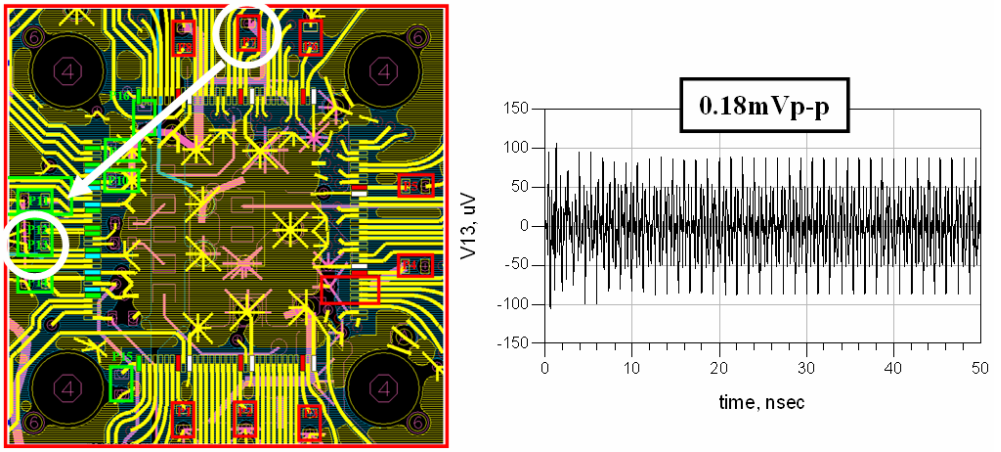
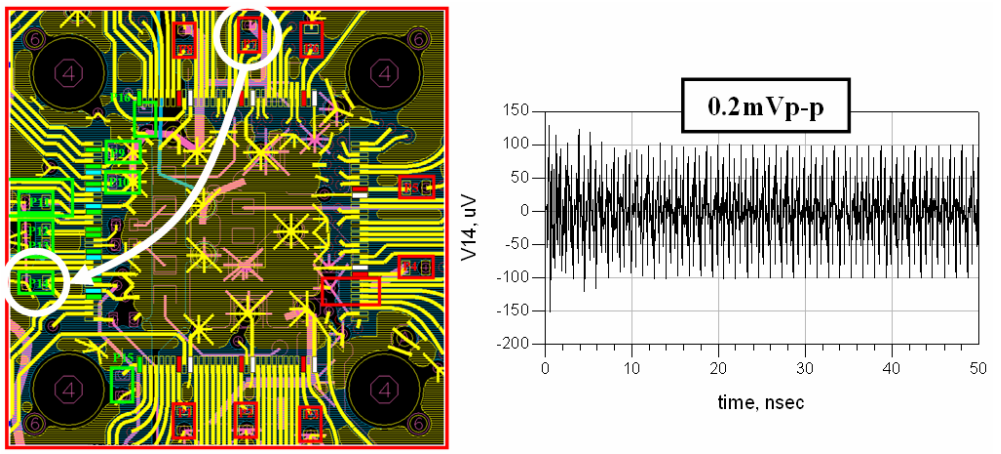
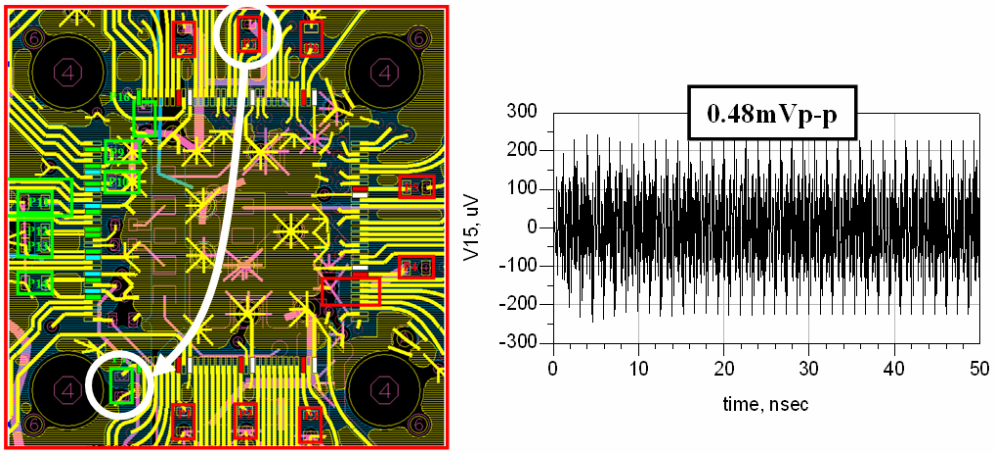


(e)

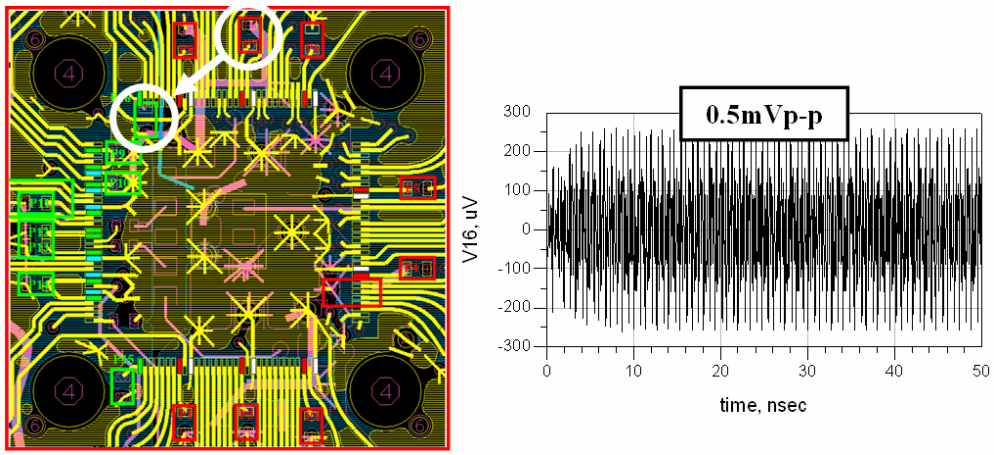


(f)

Figure A.8: Continued.

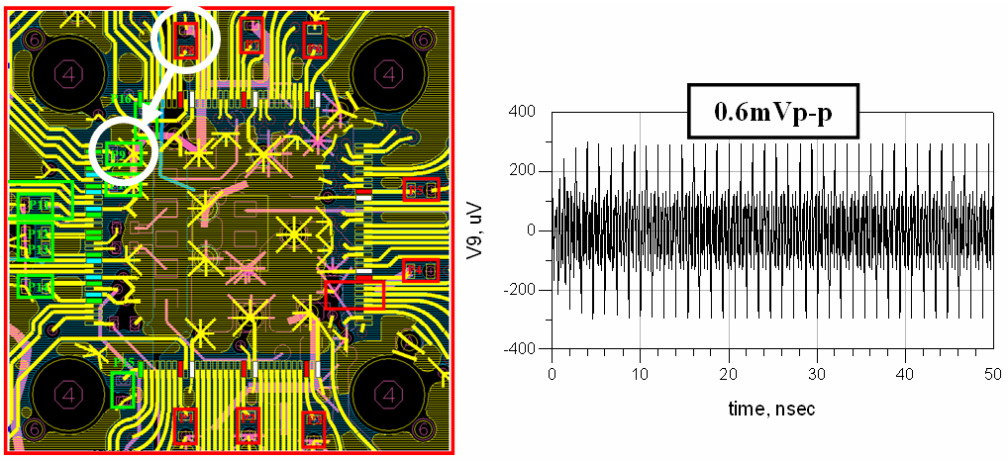


(g)

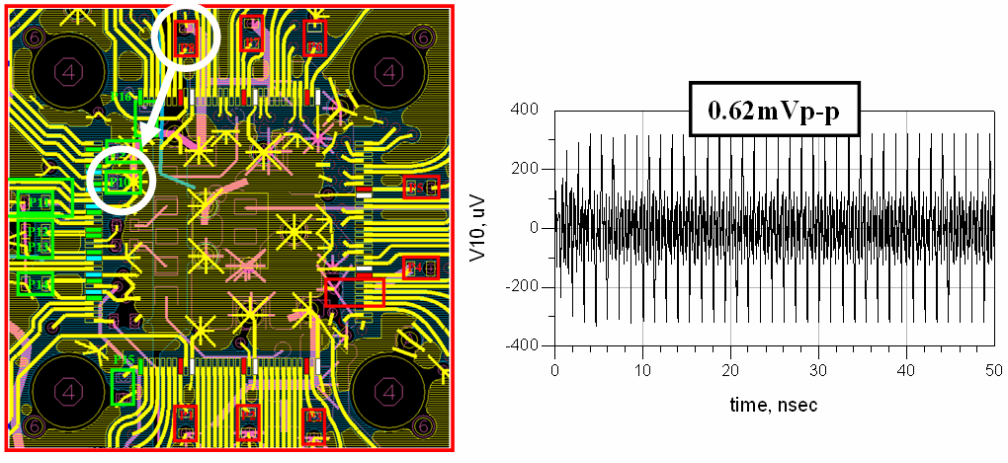


(h)

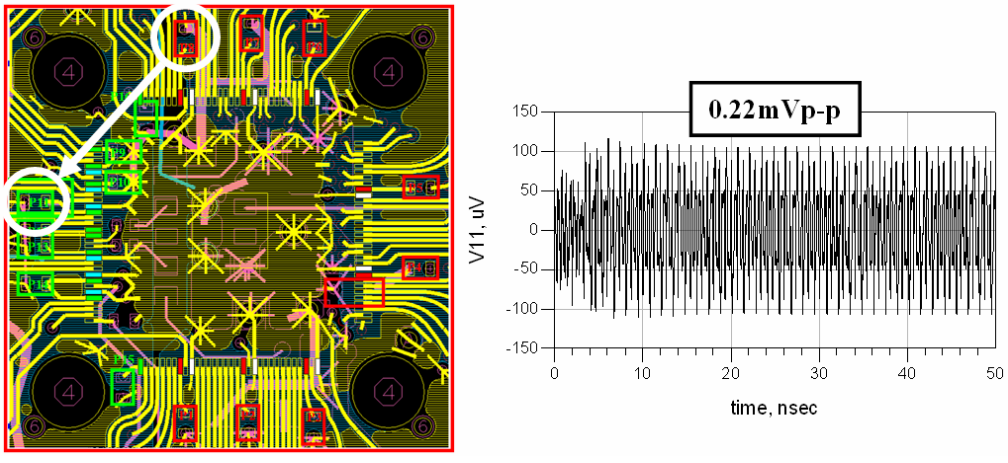
Figure A.8: Continued.



(a)

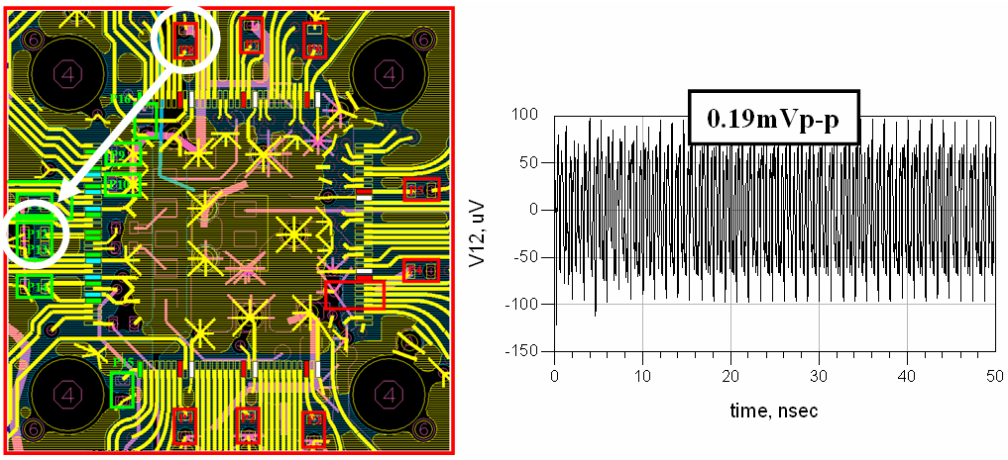


(b)



(c)

Figure A.9: The coupled noise from P8 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



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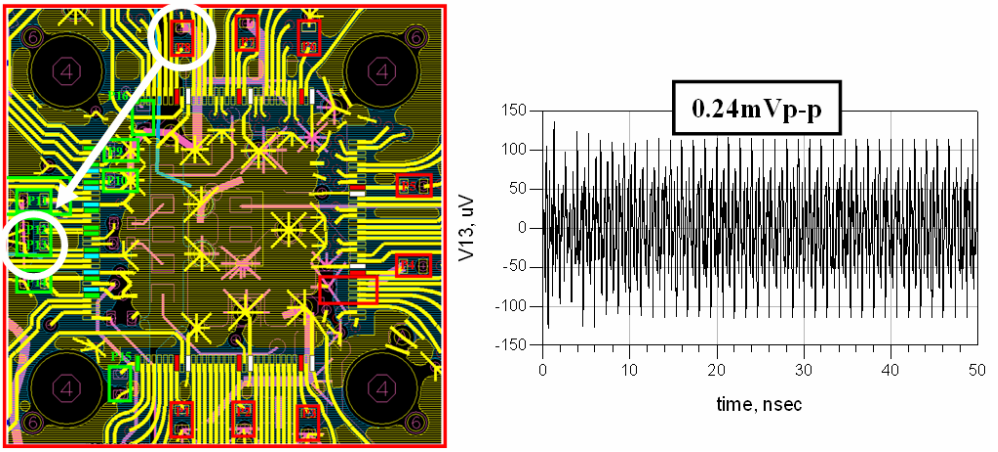
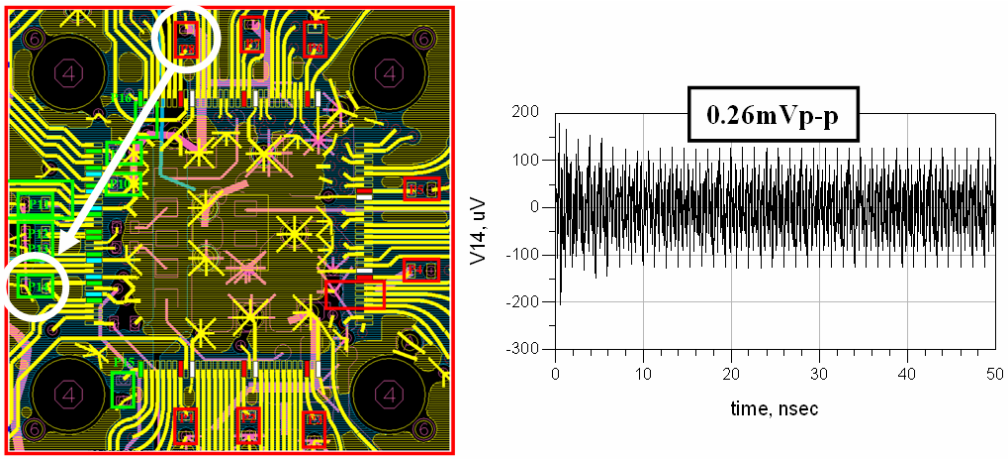
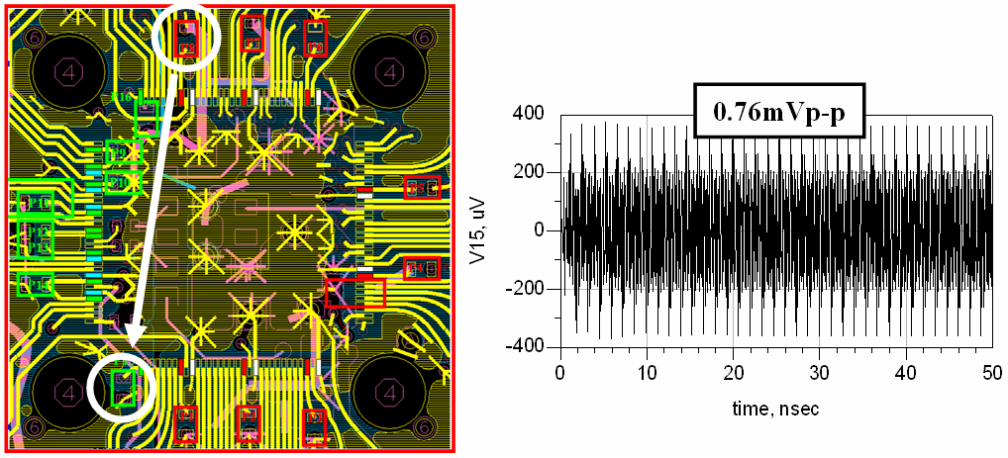


(e)

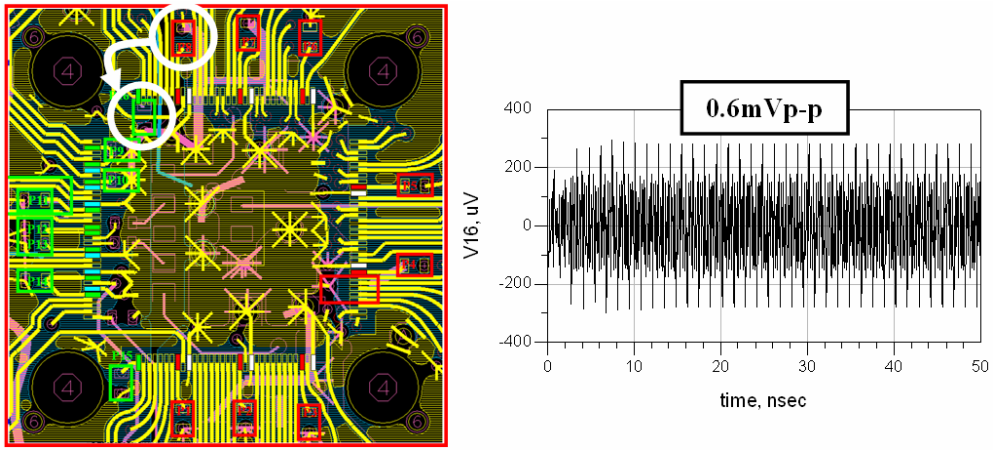


(f)

Figure A.9: Continued.



(g)



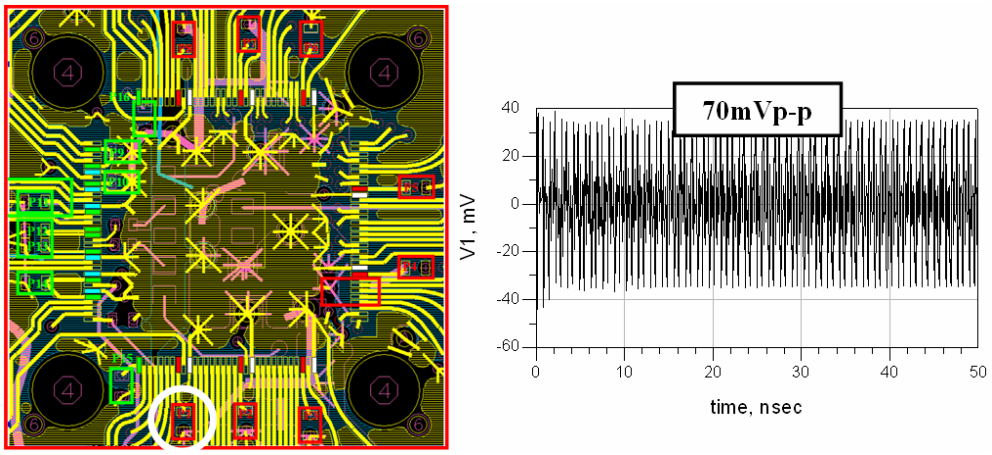
(h)

Figure A.9: Continued.

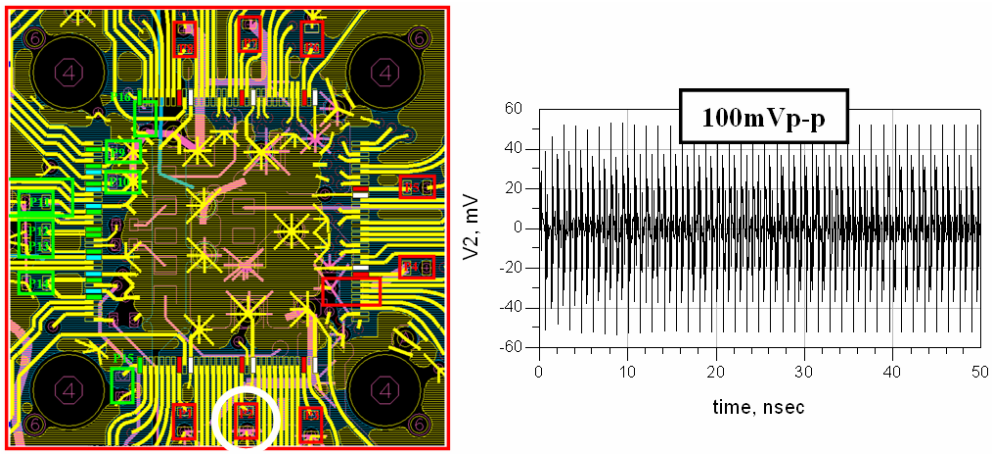
APPENDIX B

SIMULATION RESULTS FOR POST-MODIFICATION BOARD

Simulation results for the post-modification board are shown in this appendix.

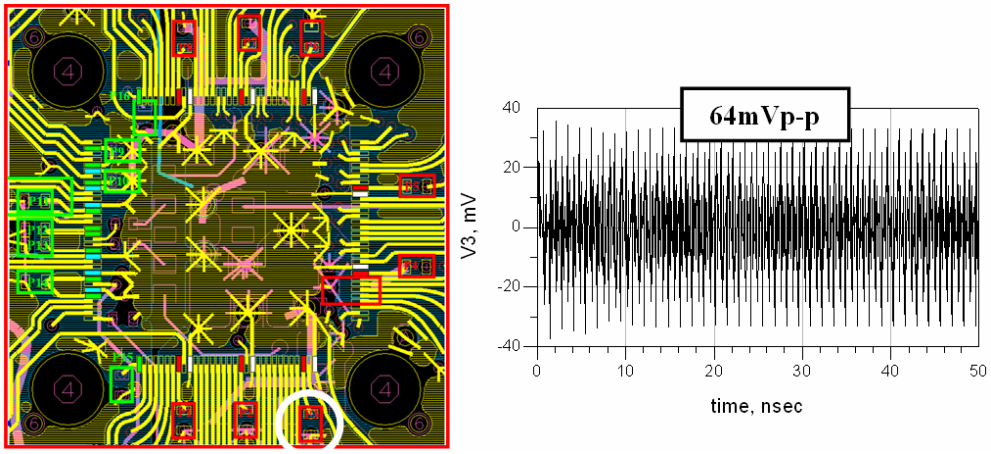


(a)

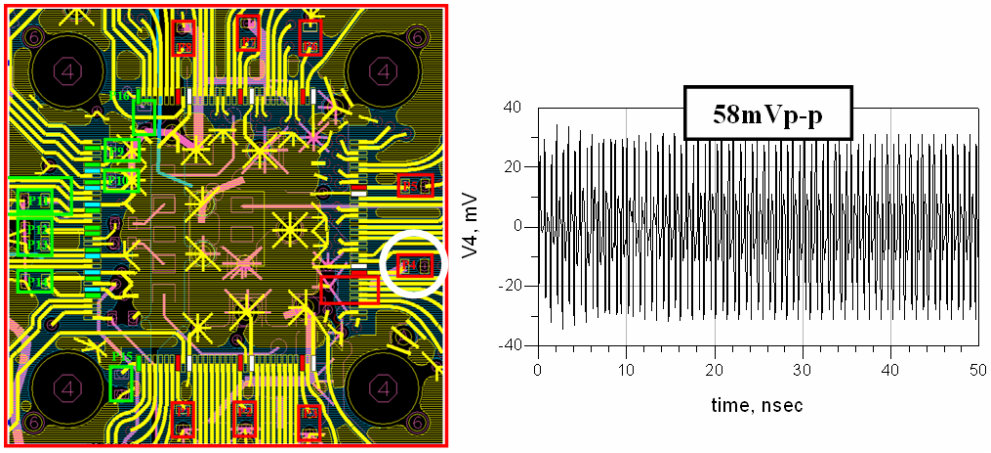


(b)

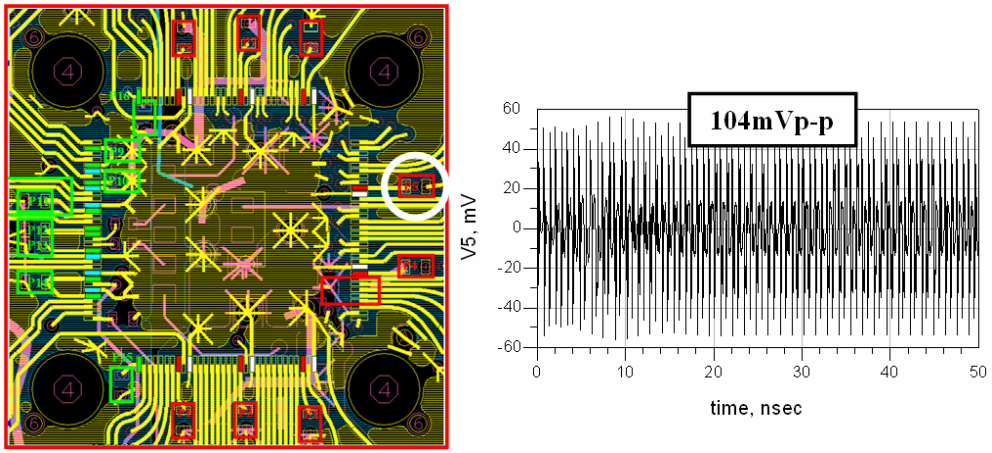
Figure B.1: The switching noise (ΔV) generated at (a) P1, (b) P2, (c) P3, (d) P4, (e) P5, (f) P6, (g) P7, and (h) P8 when each location from P1 to P8 was excited with the switching current (ΔI) of 20mAp-p and 748MHz one at a time. The white circle in the snap-shot of the board at (a) through (h) indicates locations for P1 through P8.



(c)

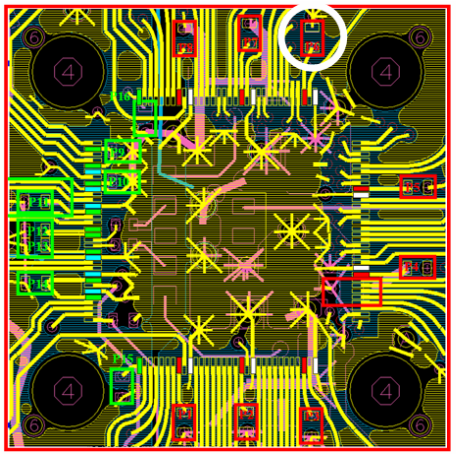


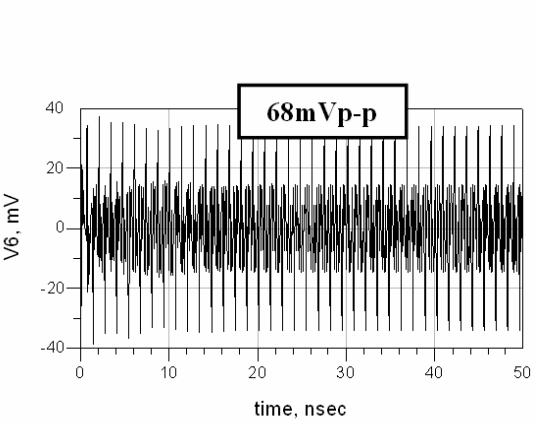
(d)



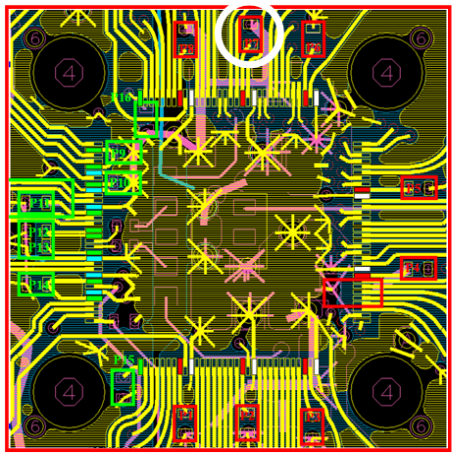
(e)

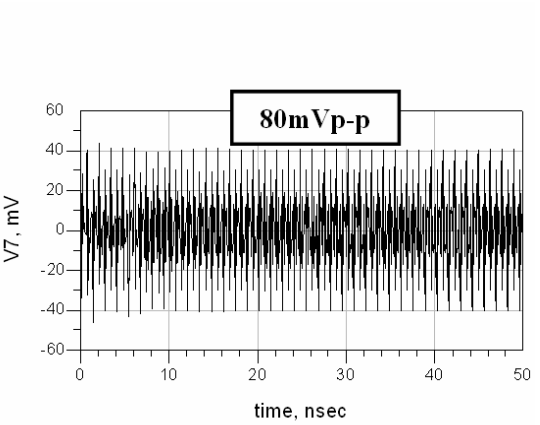
Figure B.1: Continued.



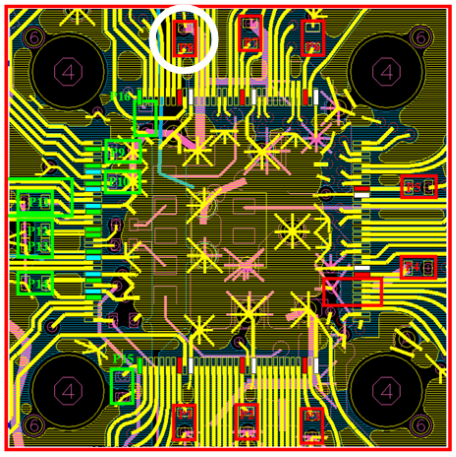


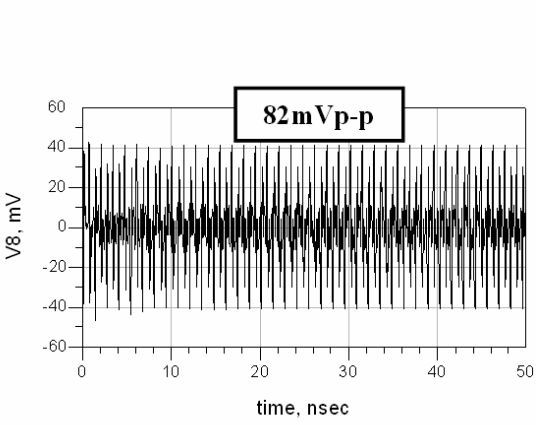
(f)





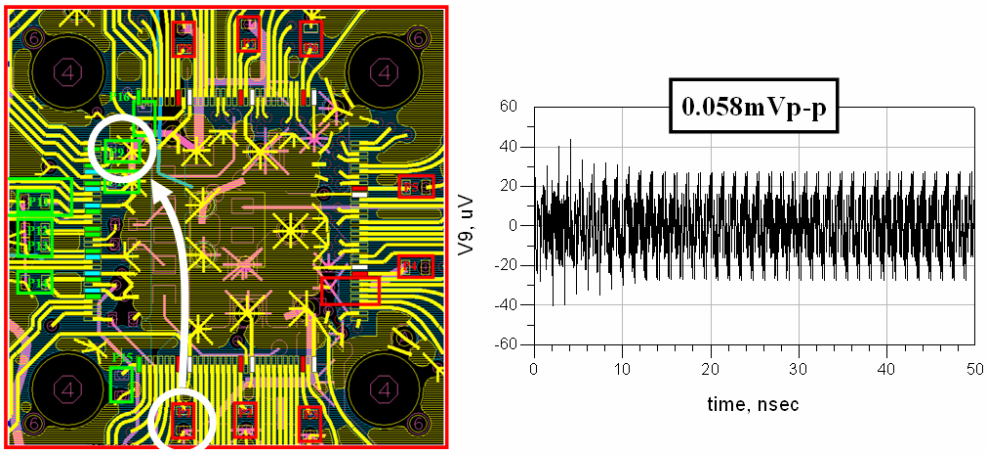
(g)



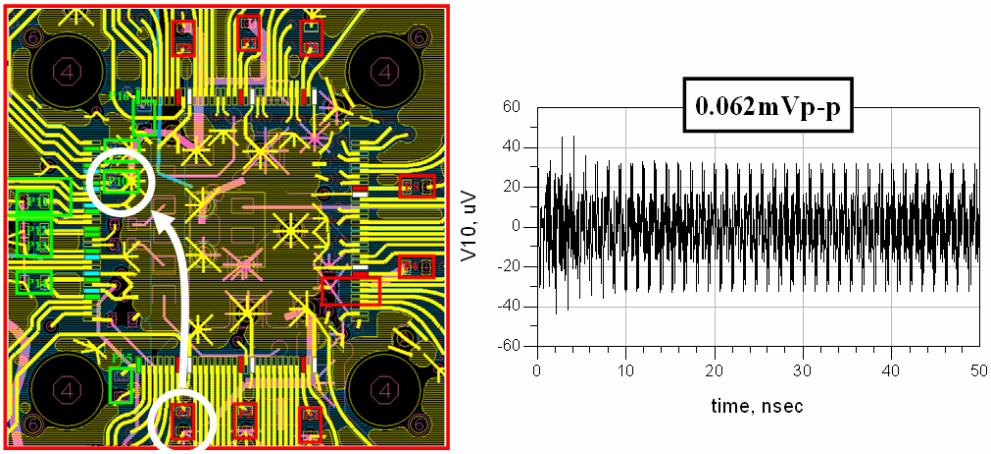


(h)

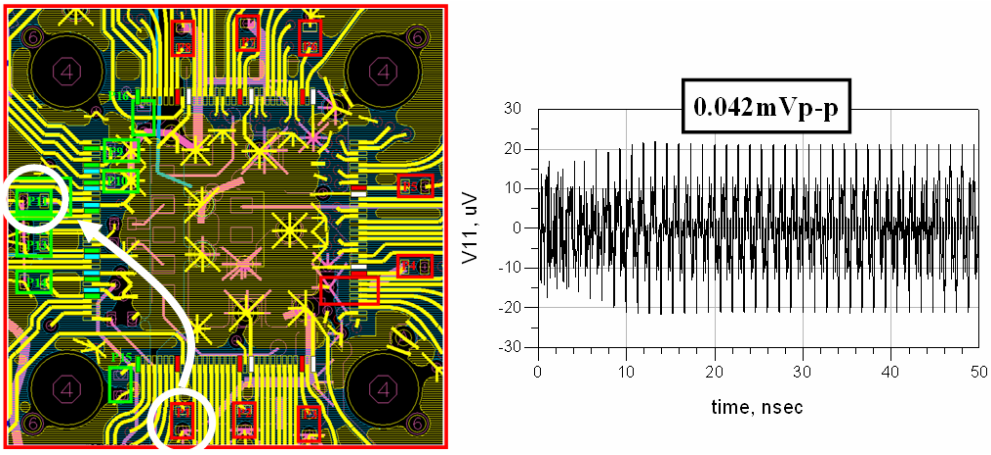
Figure B.1: Continued.



(a)

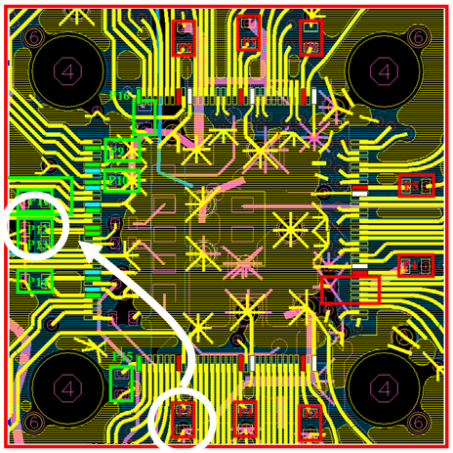


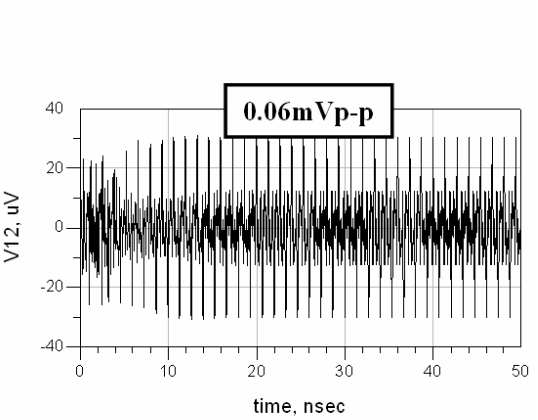
(b)



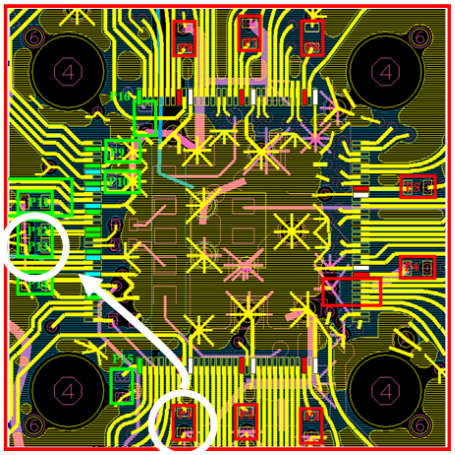
(c)

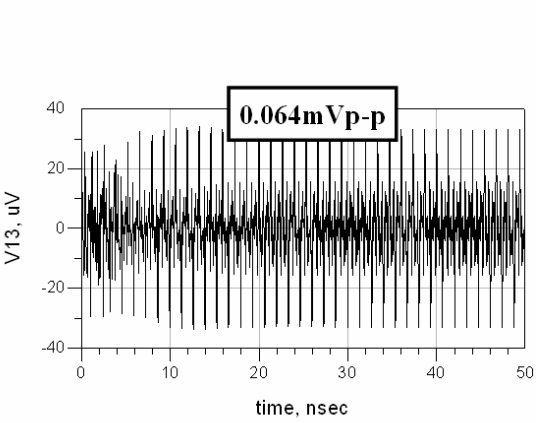
Figure B.2: The coupled noise from P1 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



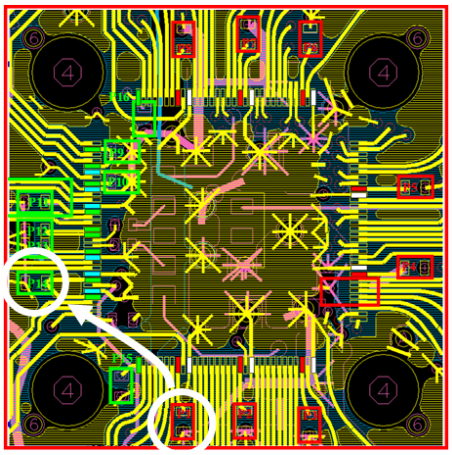


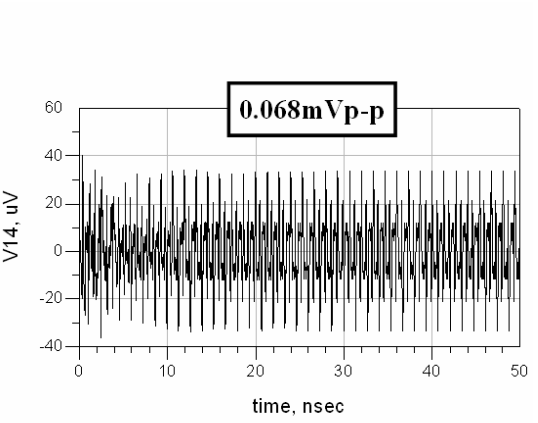
(d)





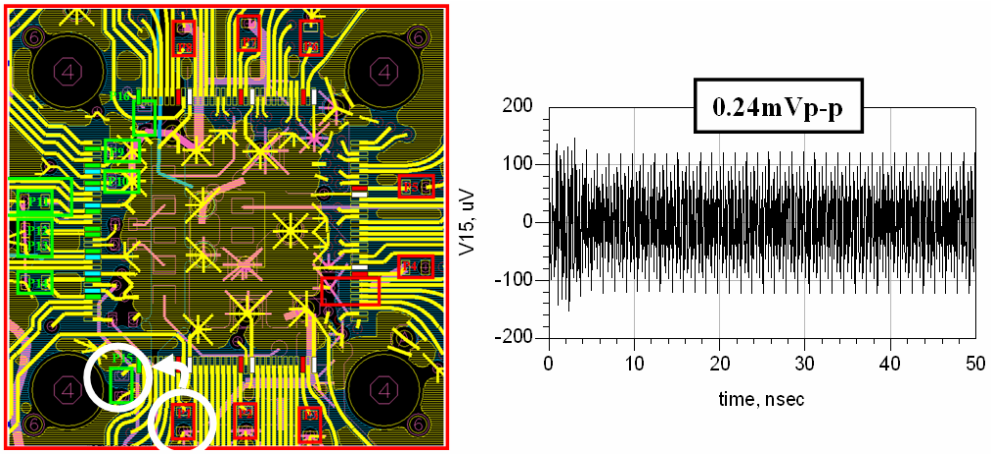
(e)



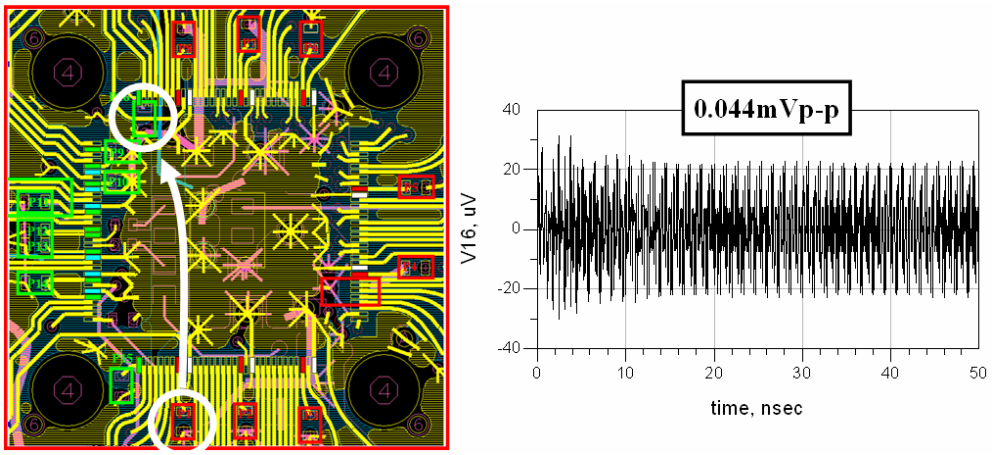


(f)

Figure B.2: Continued.

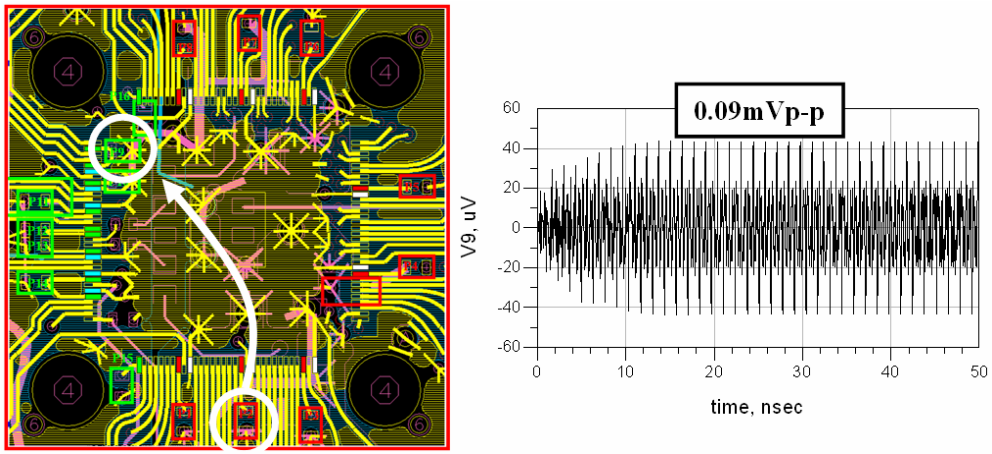


(g)

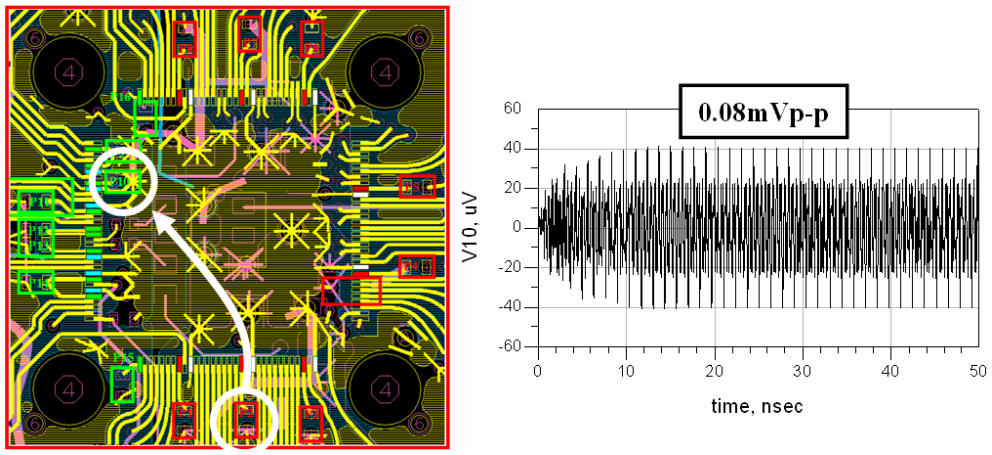


(h)

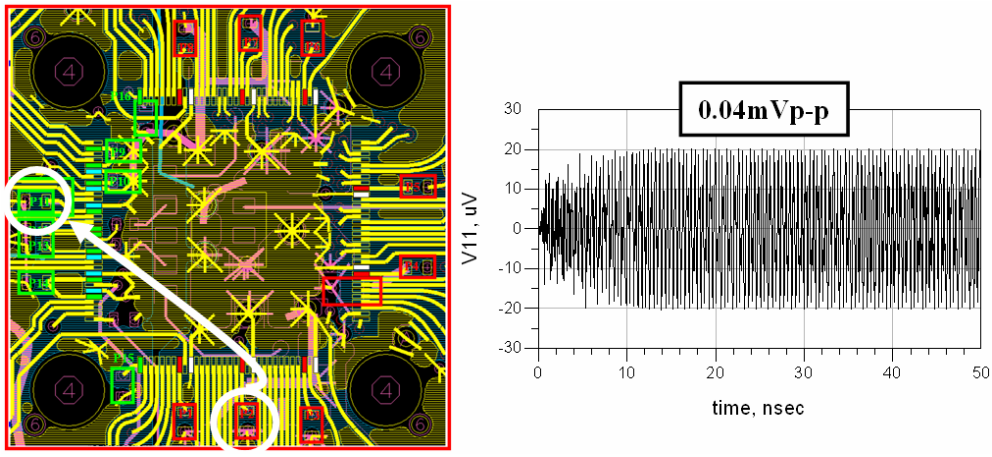
Figure B.2: Continued.



(a)

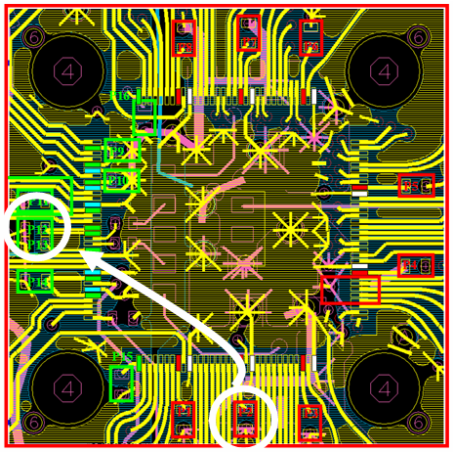


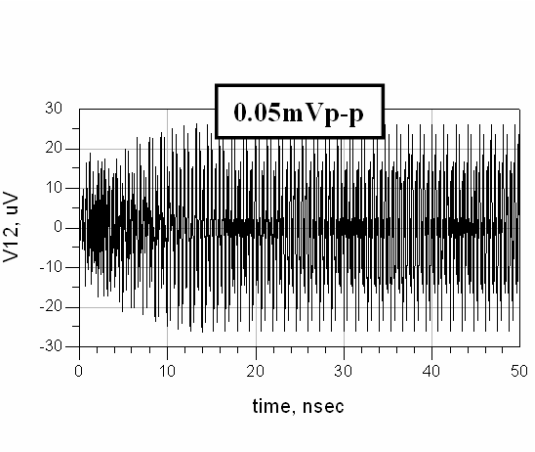
(b)



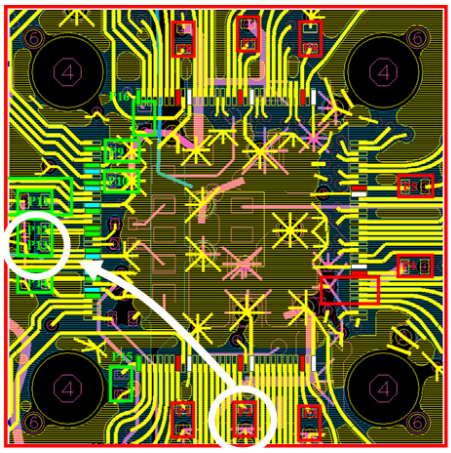
(c)

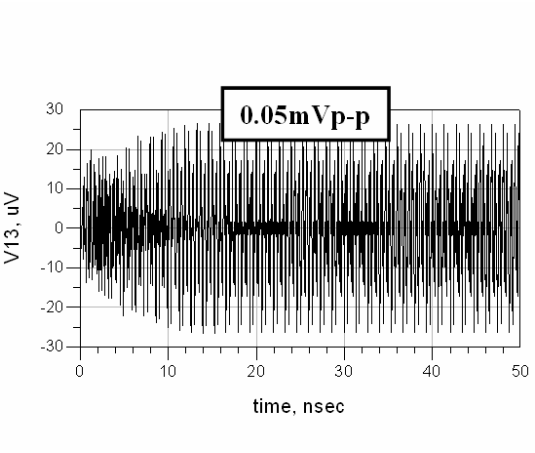
Figure B.3: The coupled noise from P2 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.





(d)





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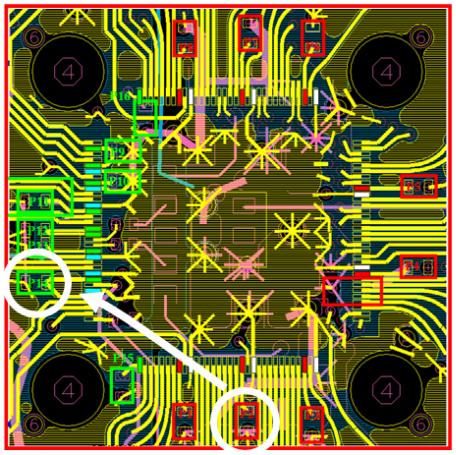
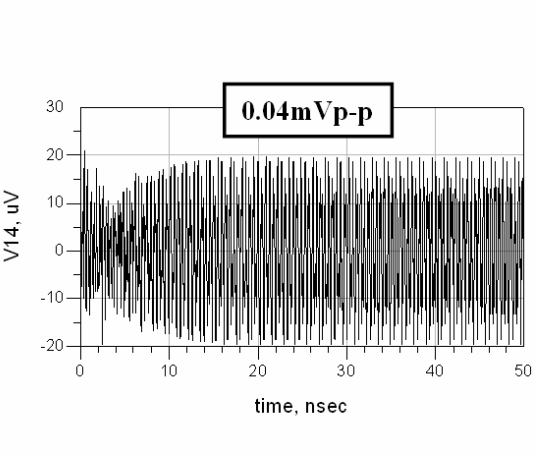
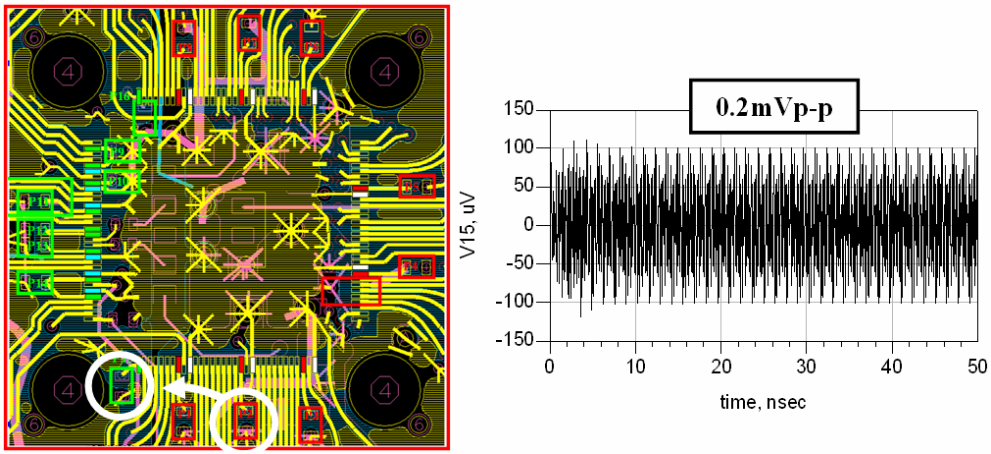


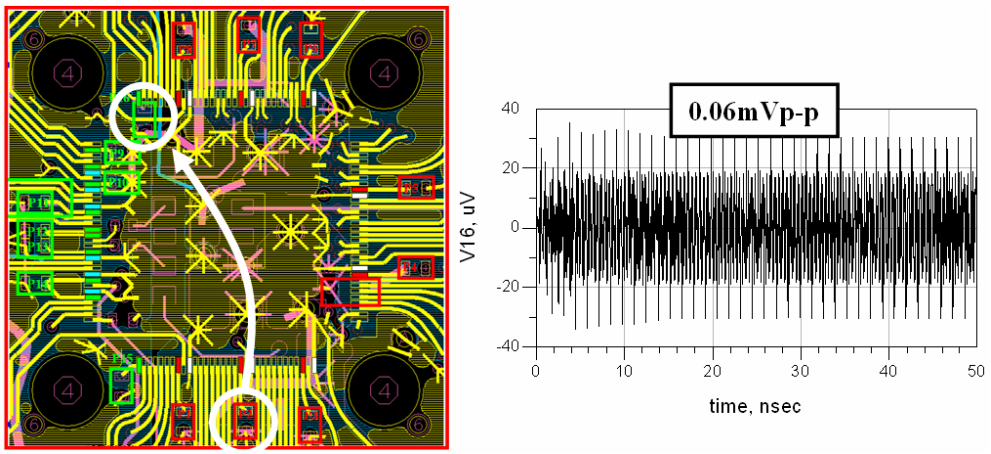


(f)

Figure B.3: Continued.

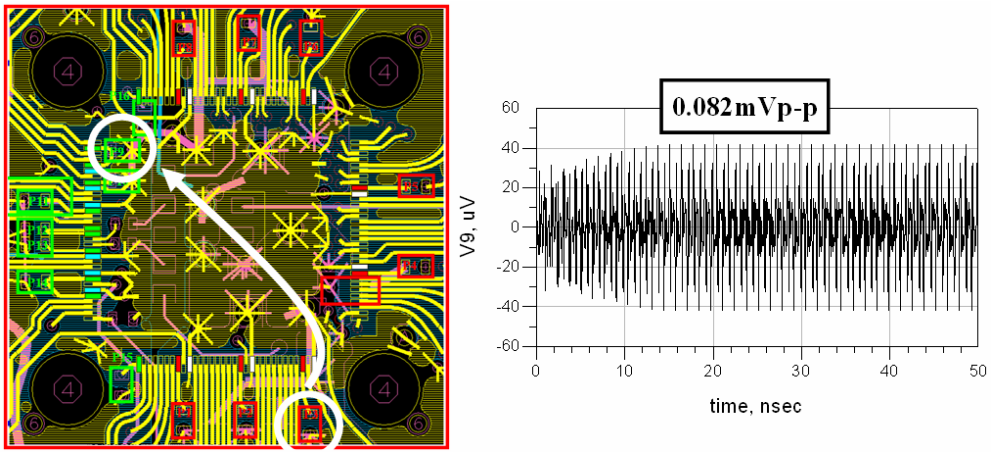


(g)

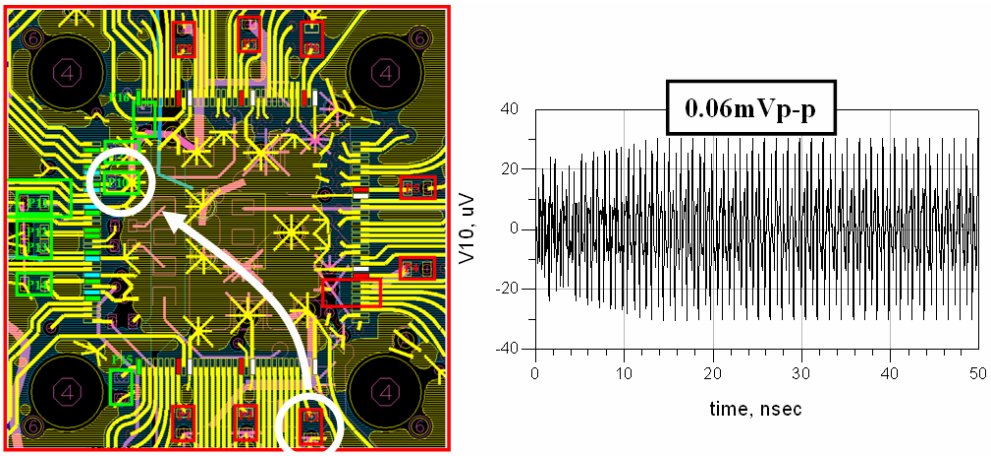


(h)

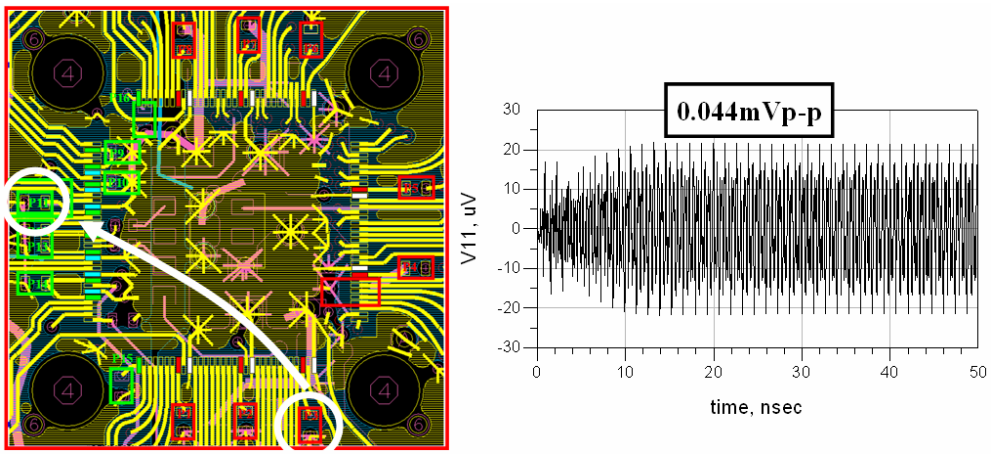
Figure B.3: Continued.



(a)

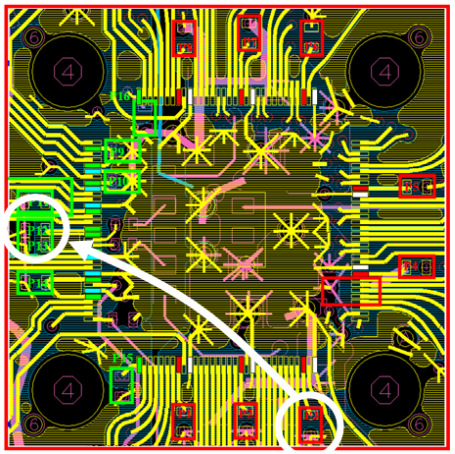


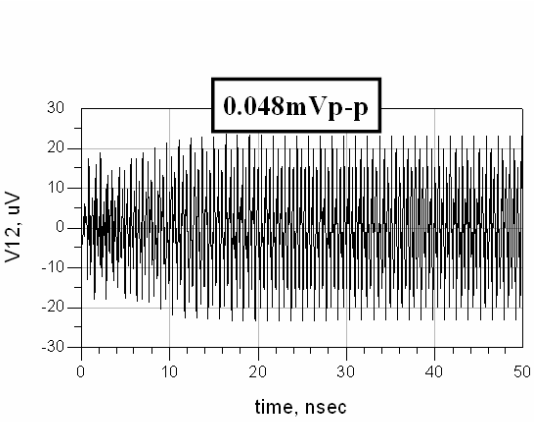
(b)



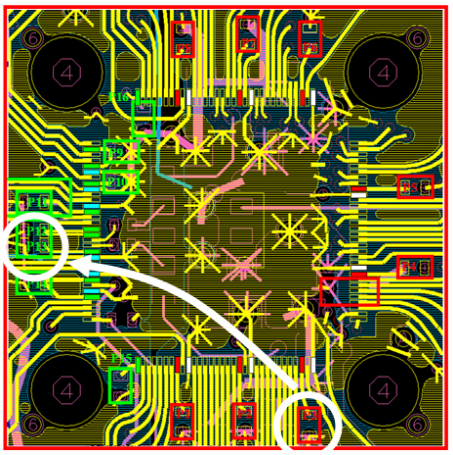
(c)

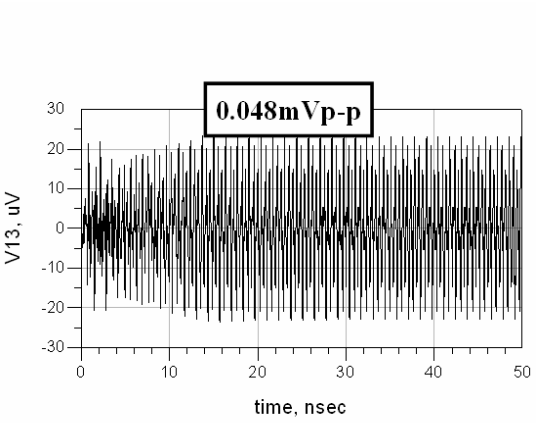
Figure B.4: The coupled noise from P3 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



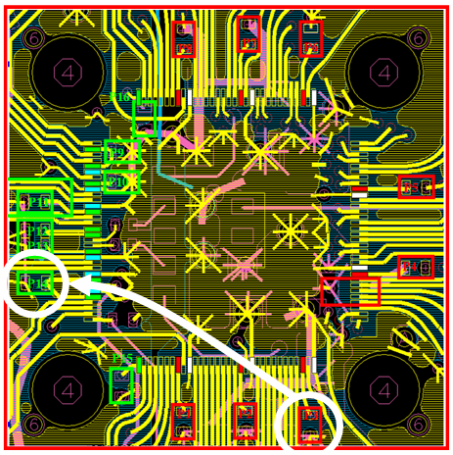


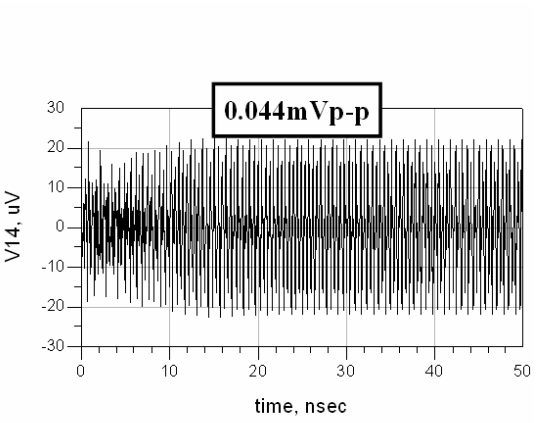
(d)





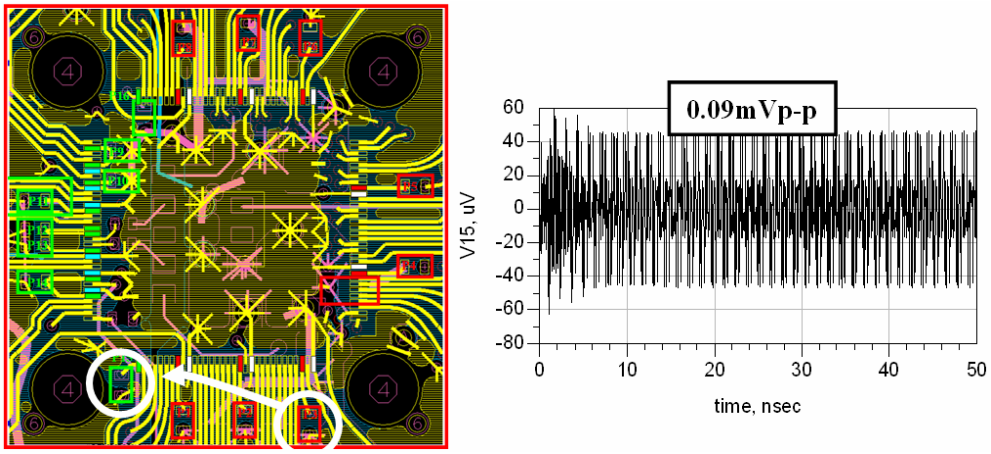
(e)



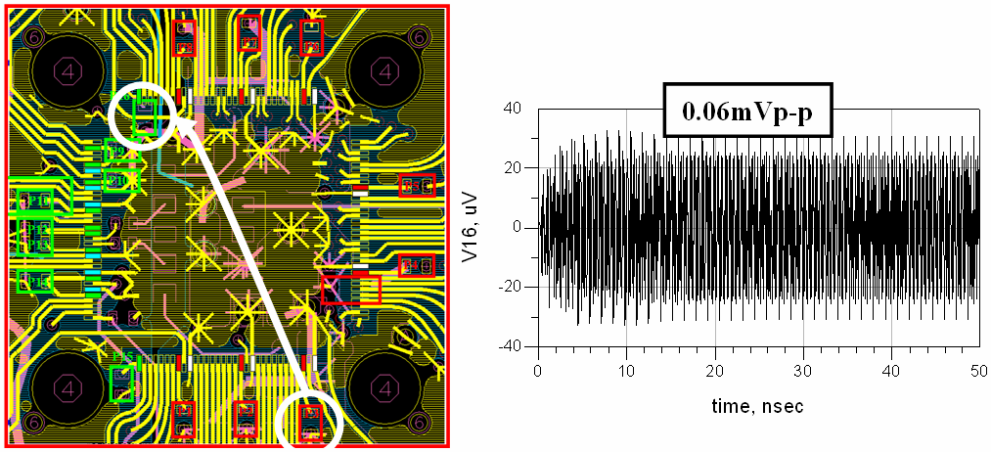


(f)

Figure B.4: Continued.

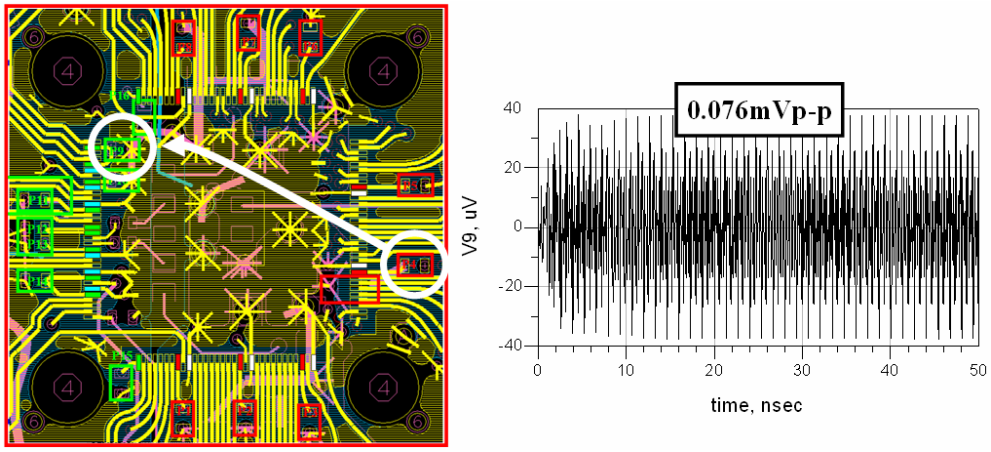


(g)

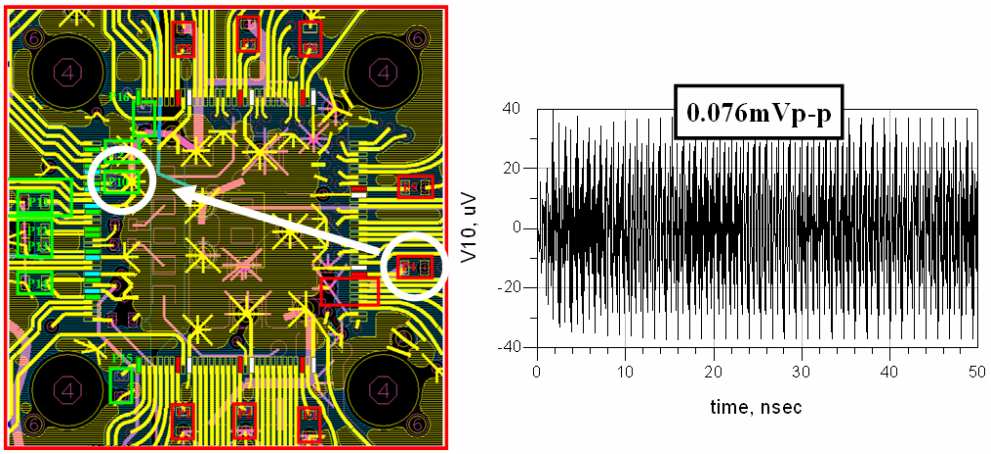


(h)

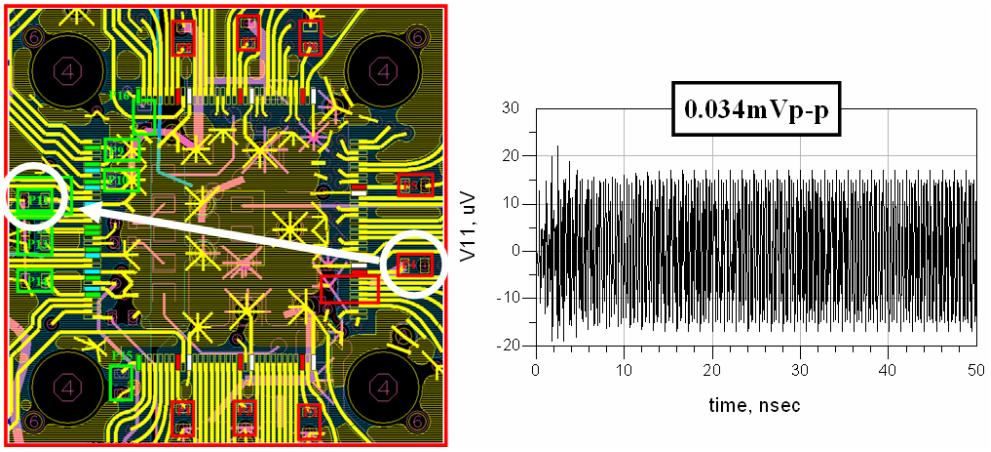
Figure B.4: Continued.



(a)

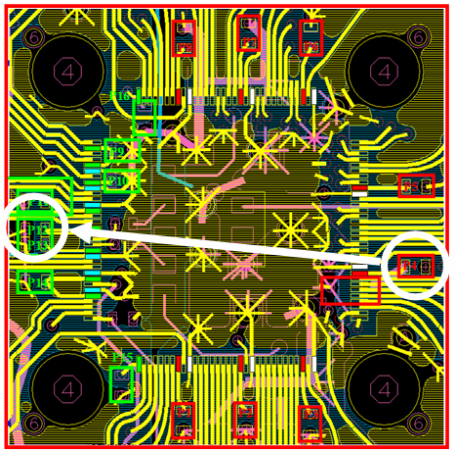


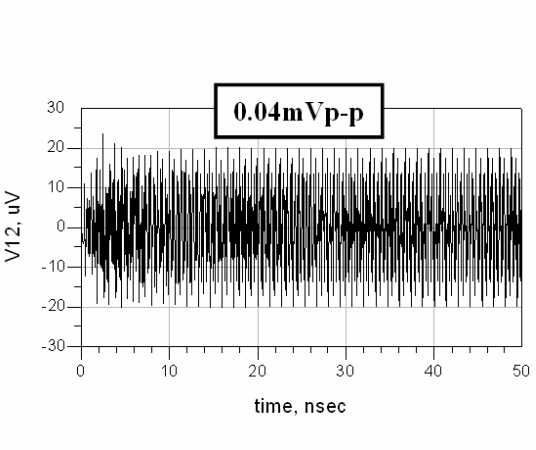
(b)



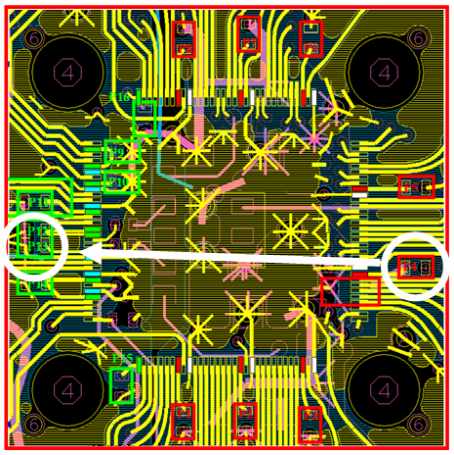
(c)

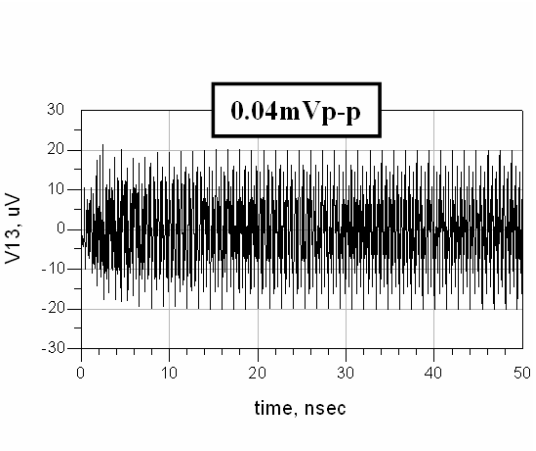
Figure B.5: The coupled noise from P4 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



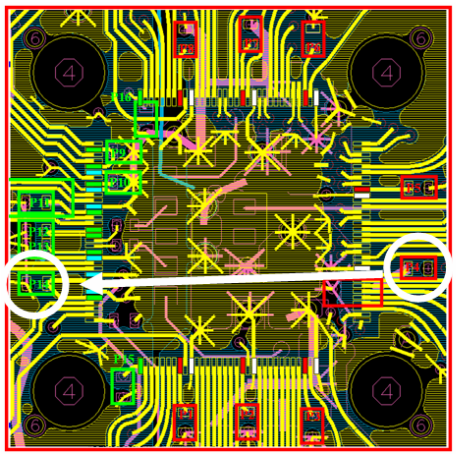


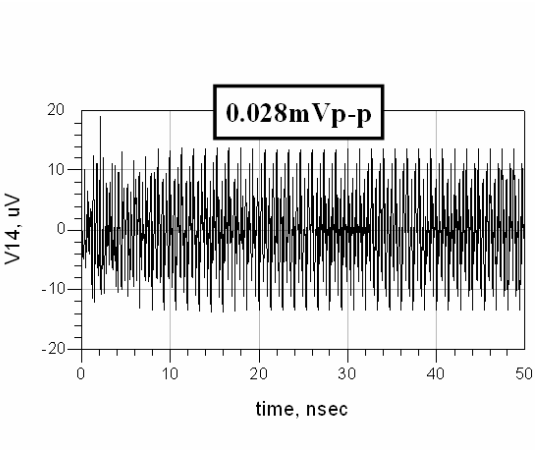
(d)





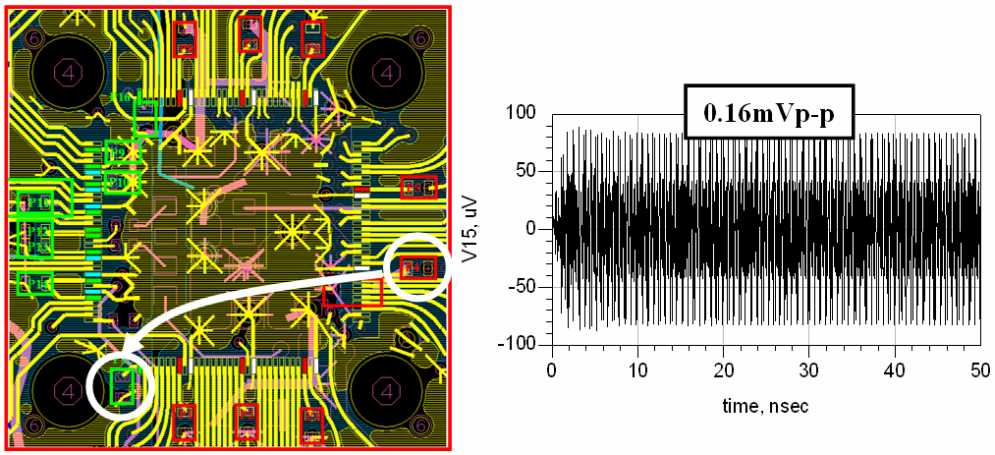
(e)



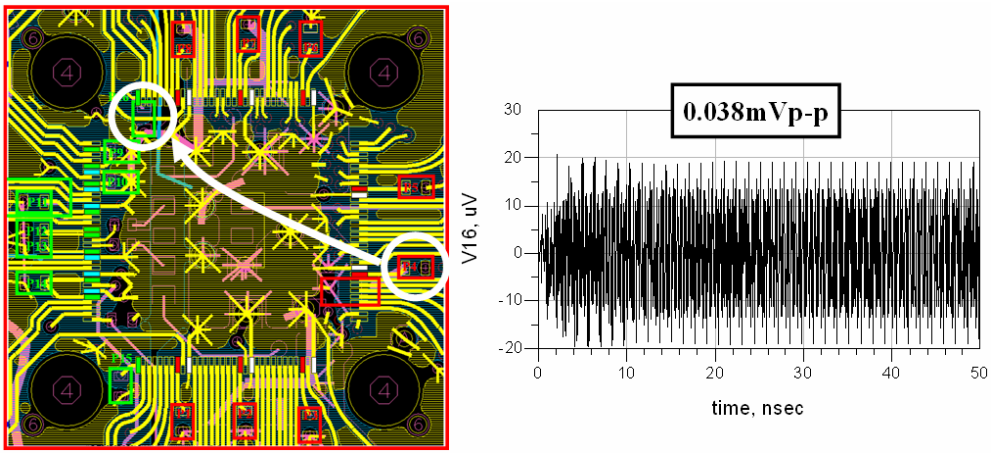


(f)

Figure B.5: Continued.

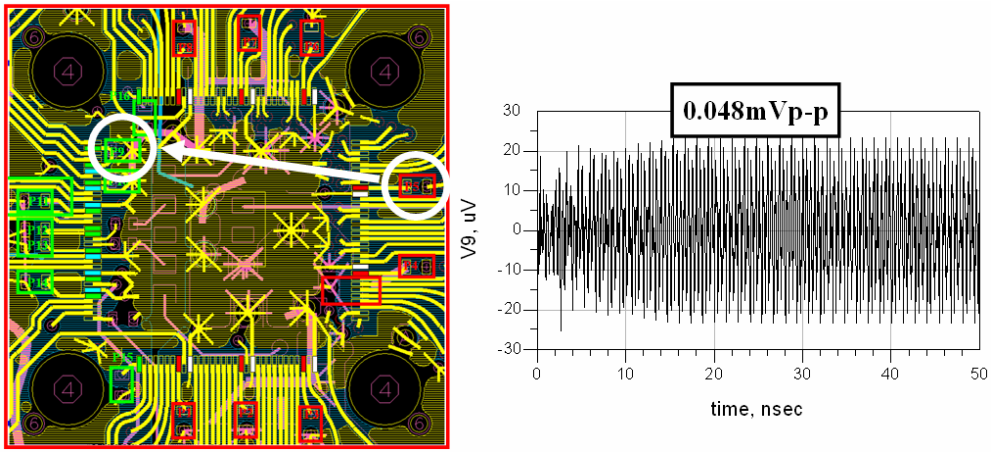


(g)

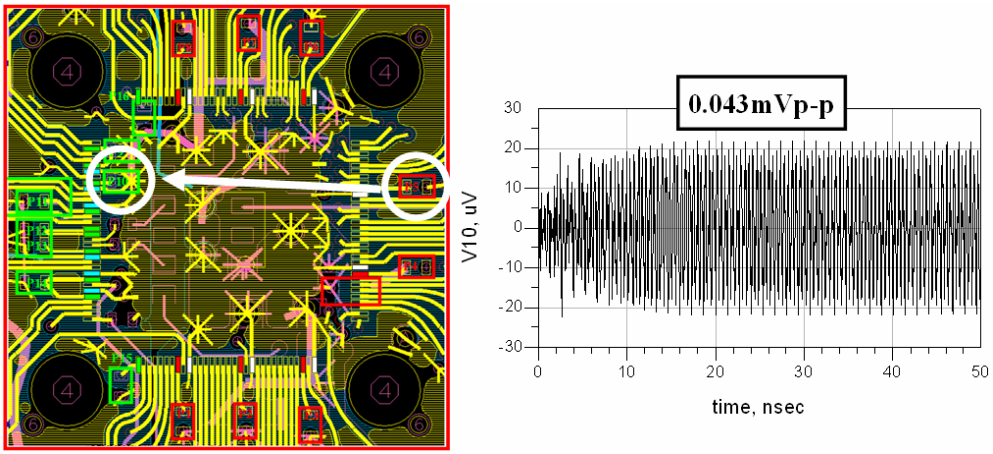


(h)

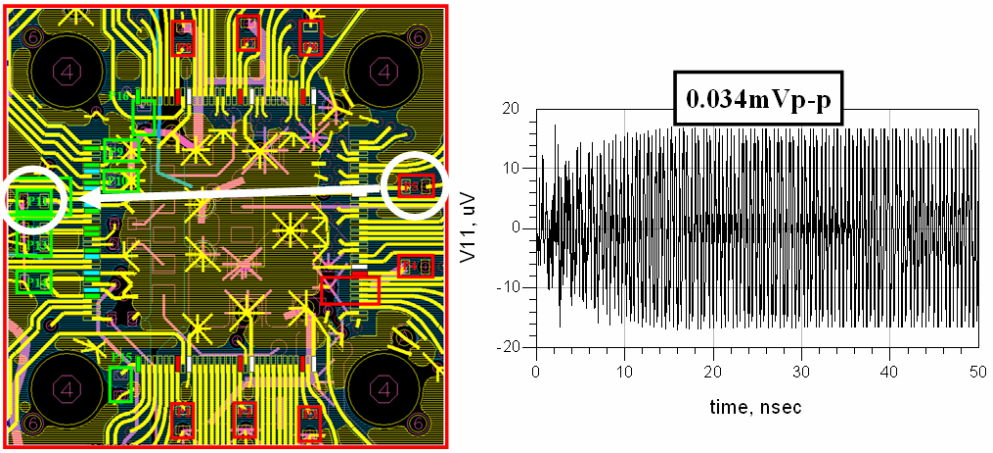
Figure B.5: Continued.



(a)

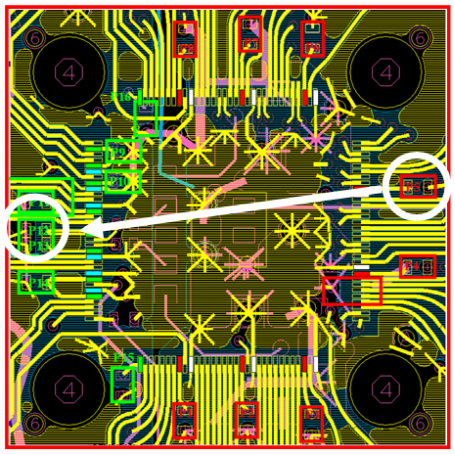


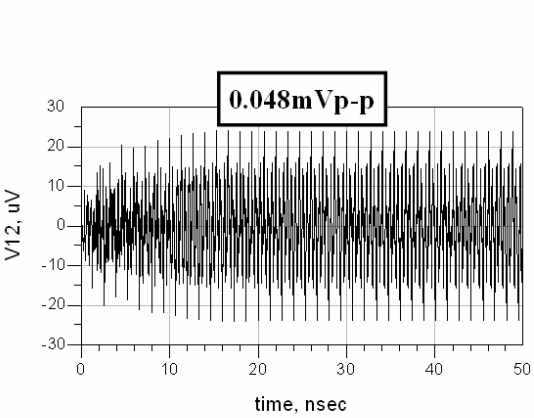
(b)



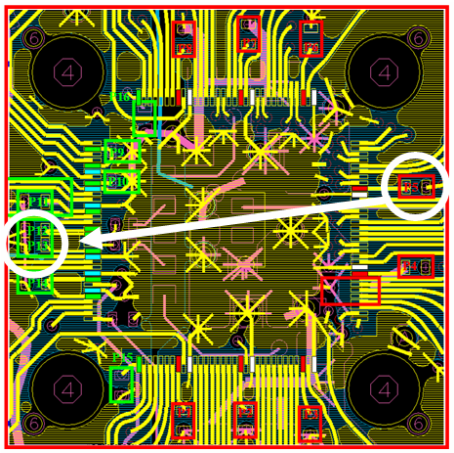
(c)

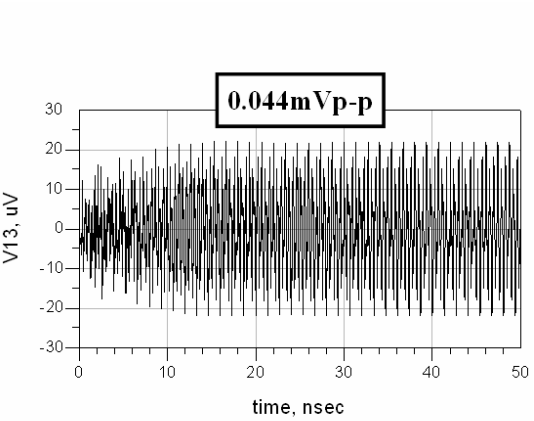
Figure B.6: The coupled noise from P5 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



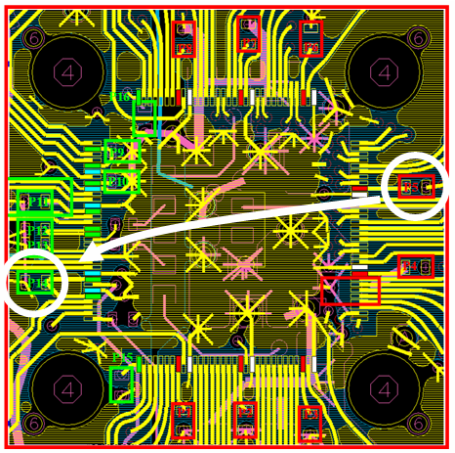


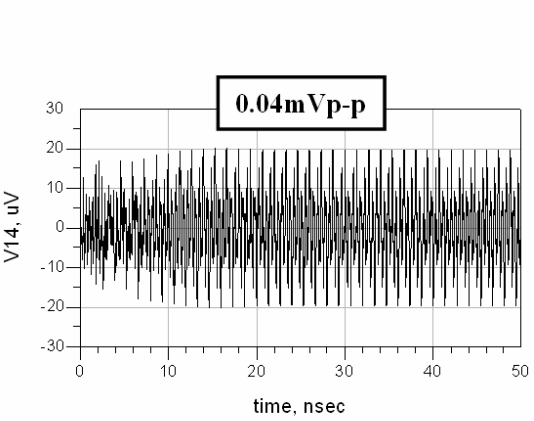
(d)





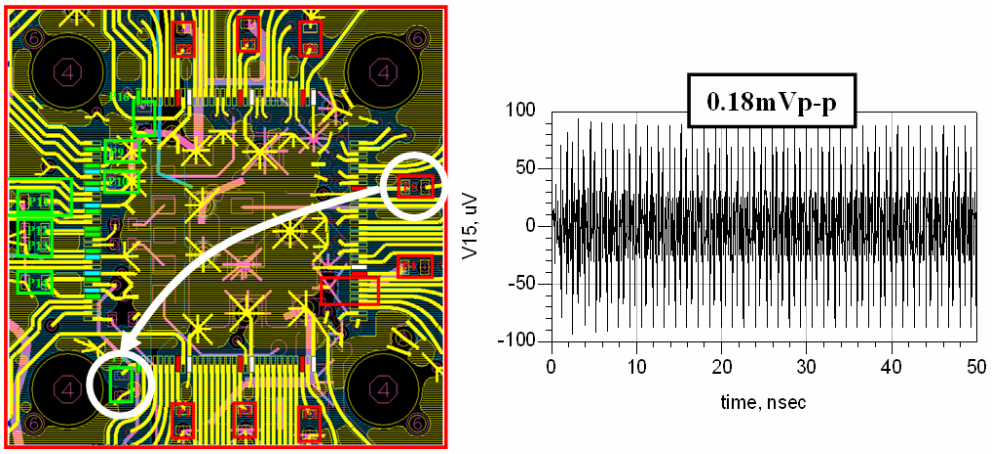
(e)



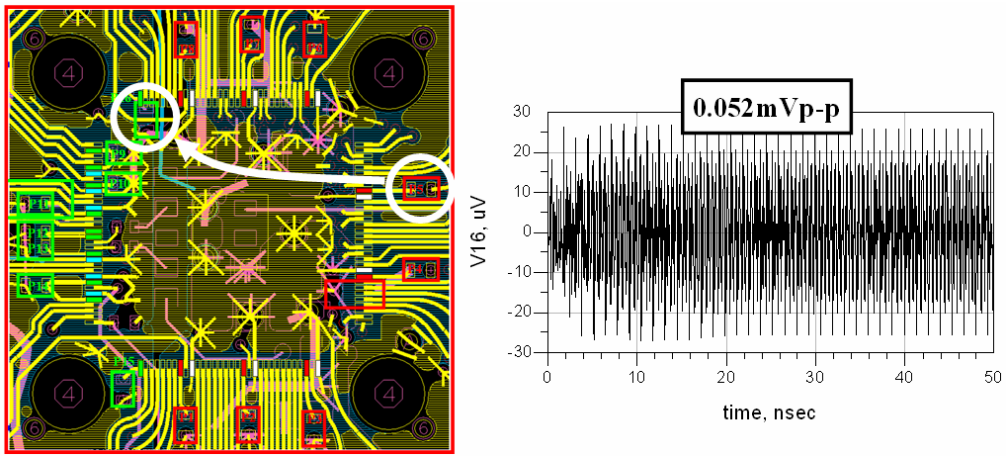


(f)

Figure B.6: Continued.

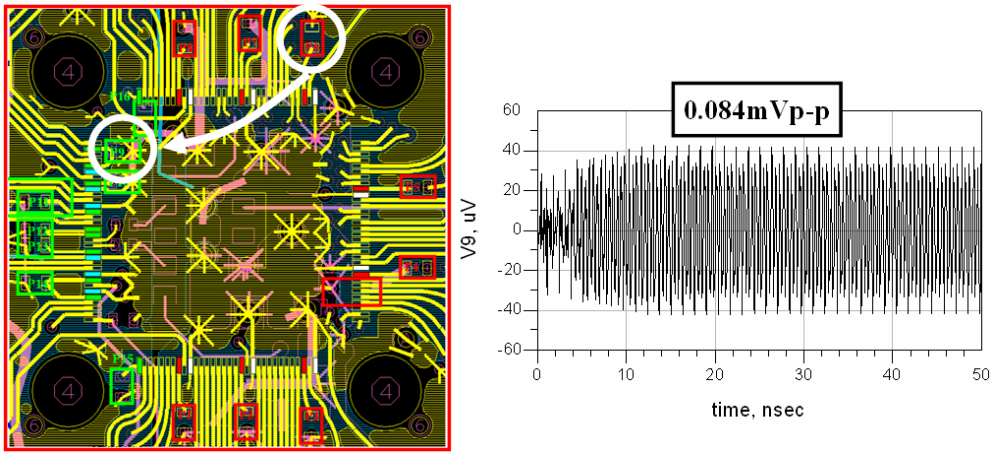


(g)

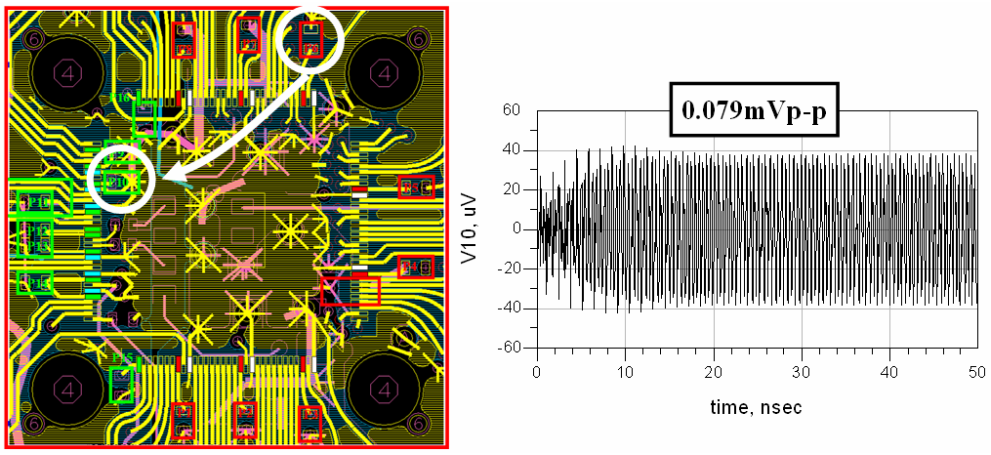


(h)

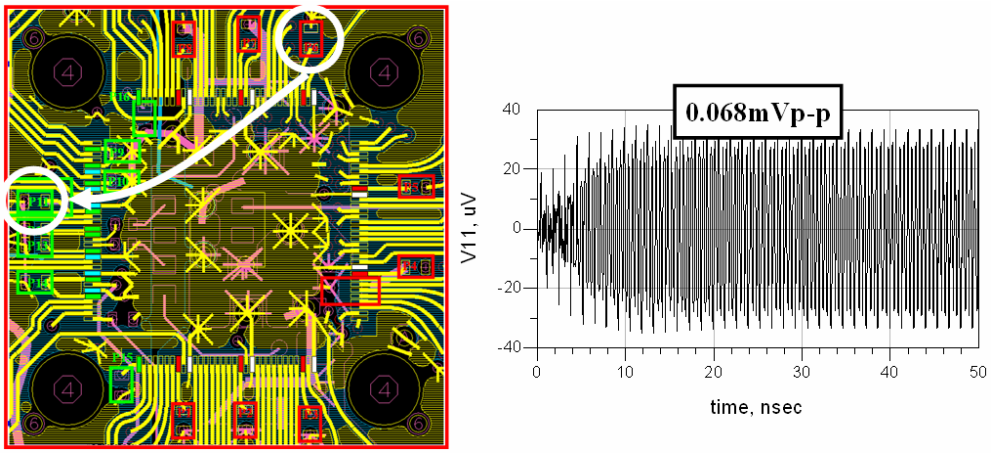
Figure B.6: Continued.



(a)

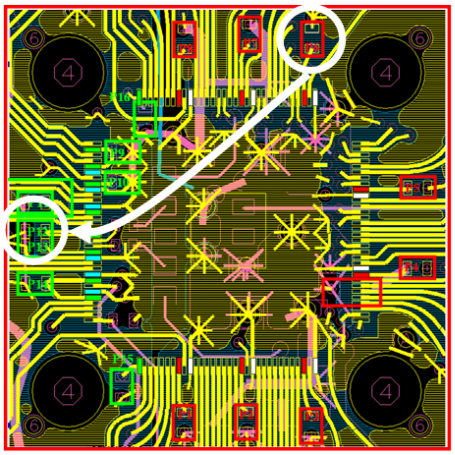


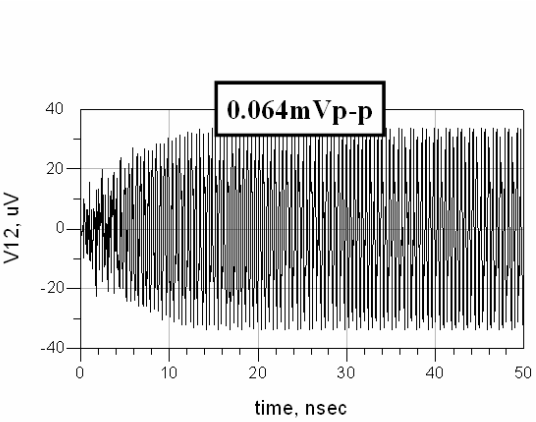
(b)



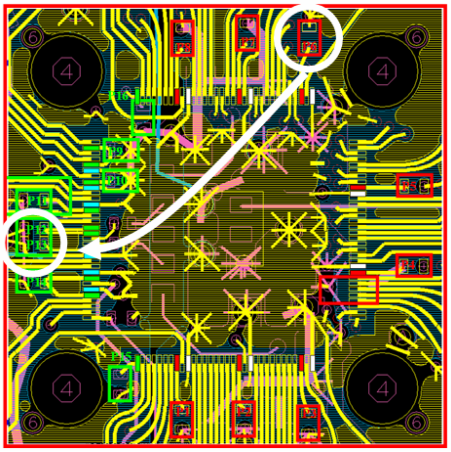
(c)

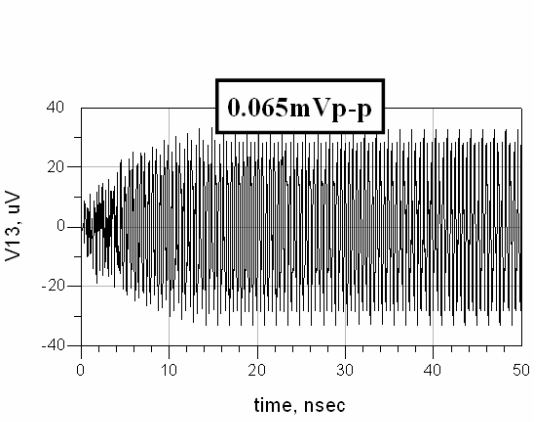
Figure B.7: The coupled noise from P6 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



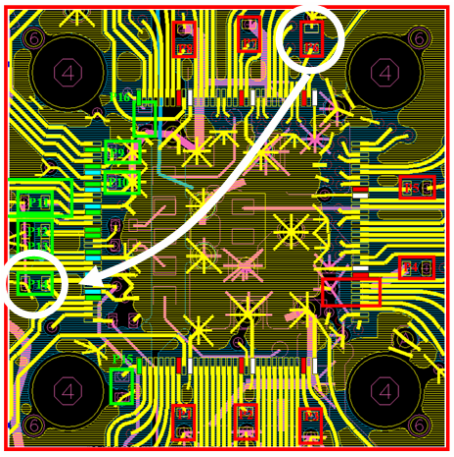


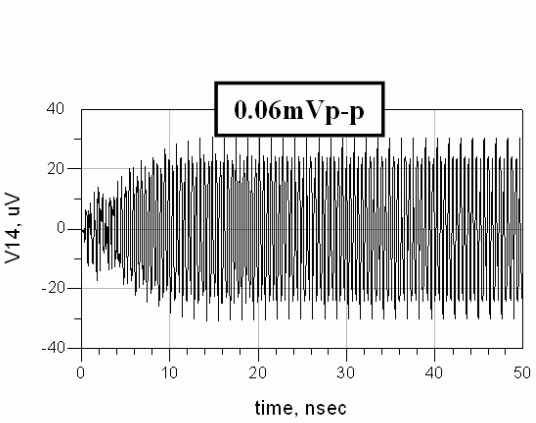
(d)





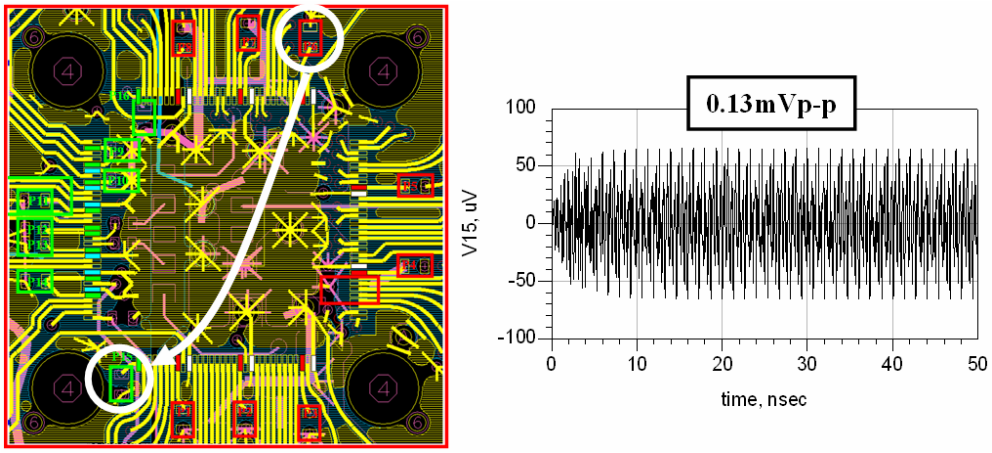
(e)



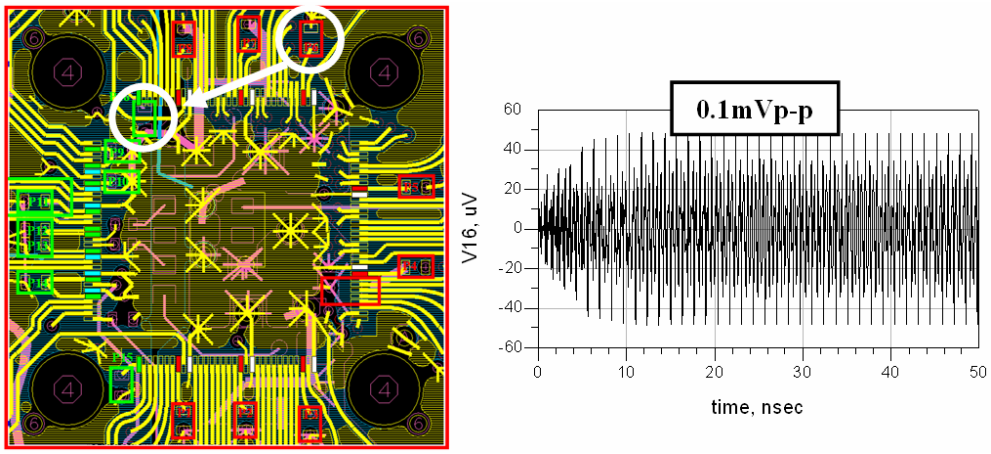


(f)

Figure B.7: Continued.

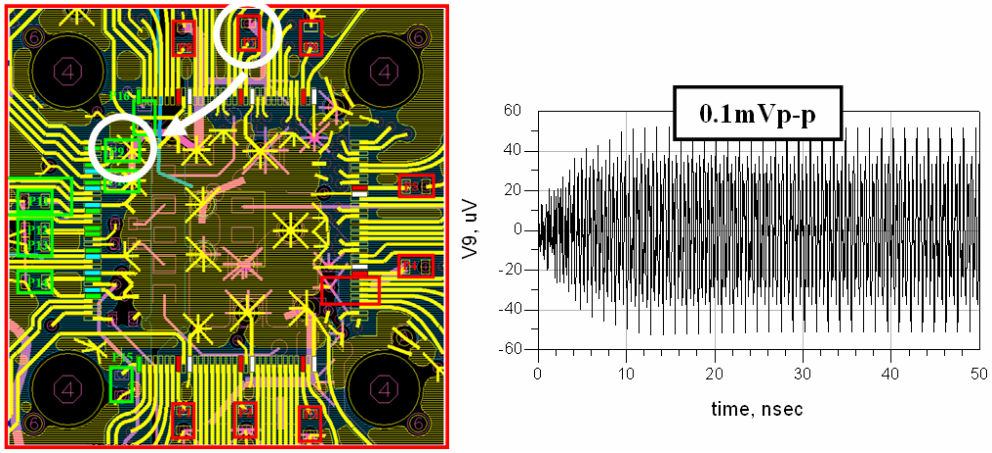


(g)

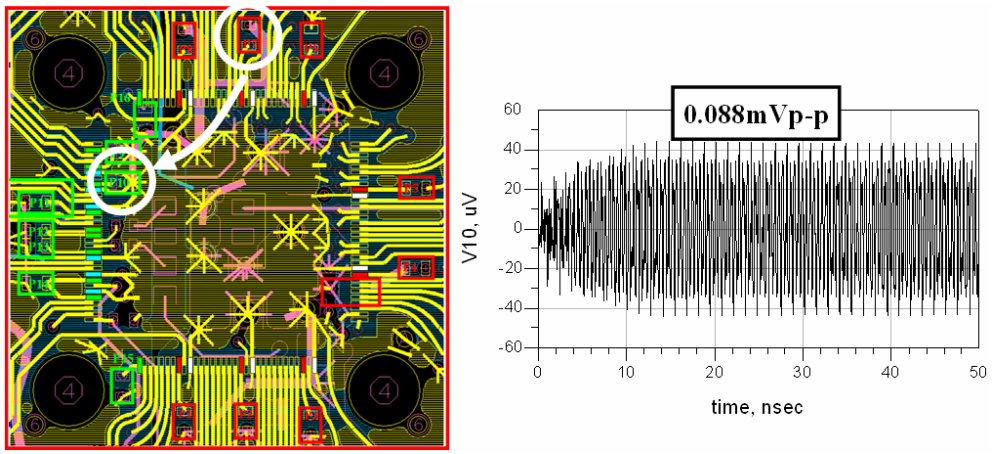


(h)

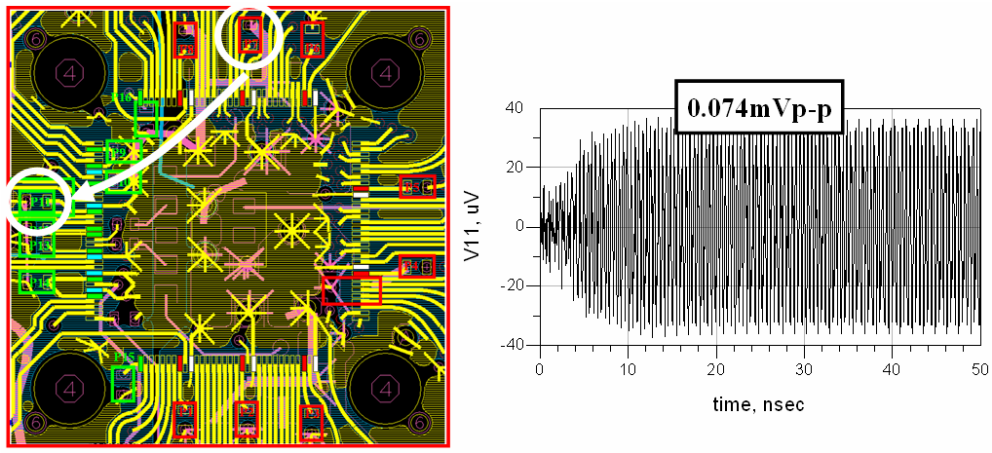
Figure B.7: Continued.



(a)

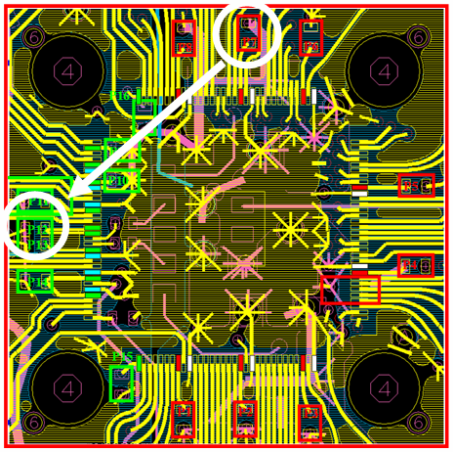


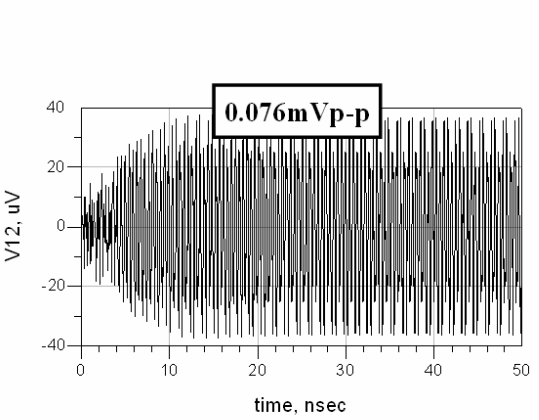
(b)



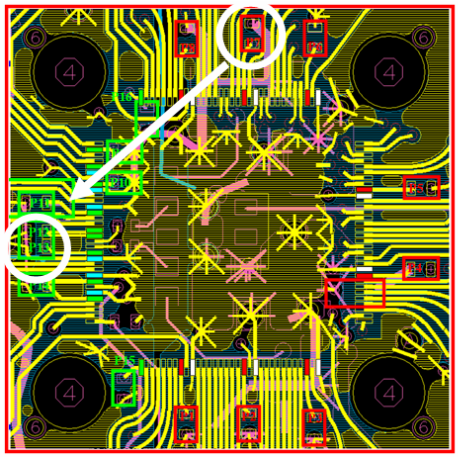
(c)

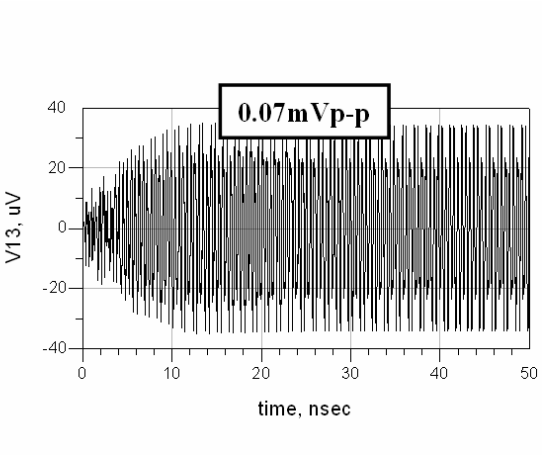
Figure B.8: The coupled noise from P7 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



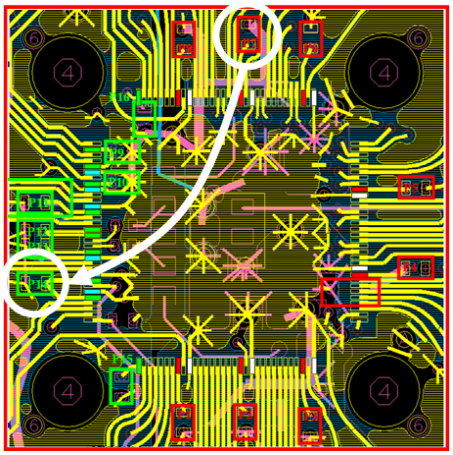


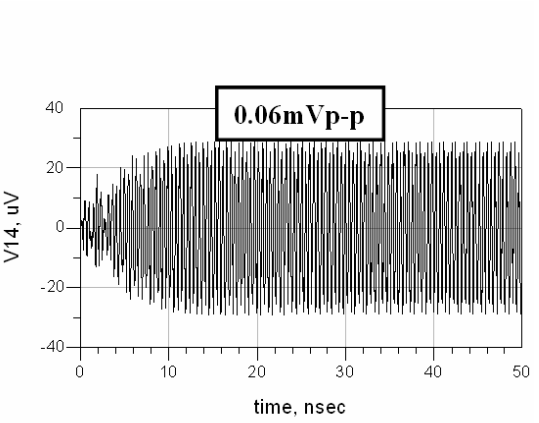
(d)





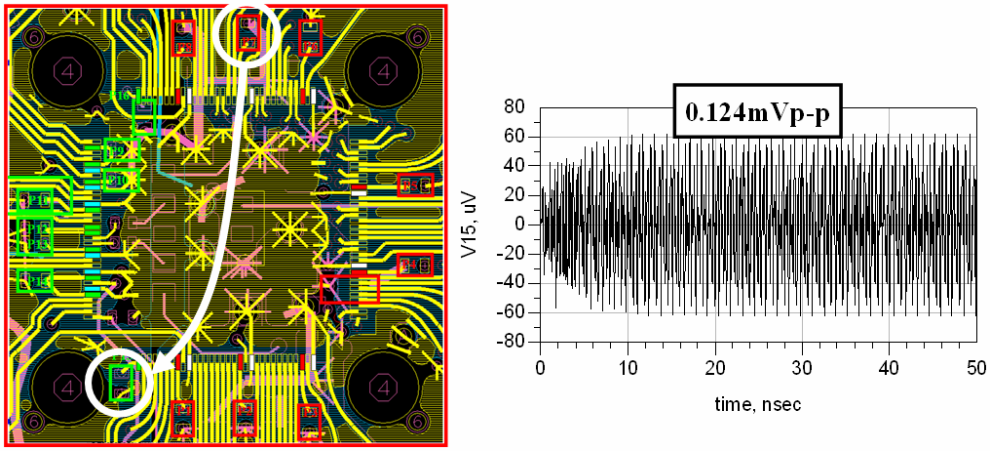
(e)



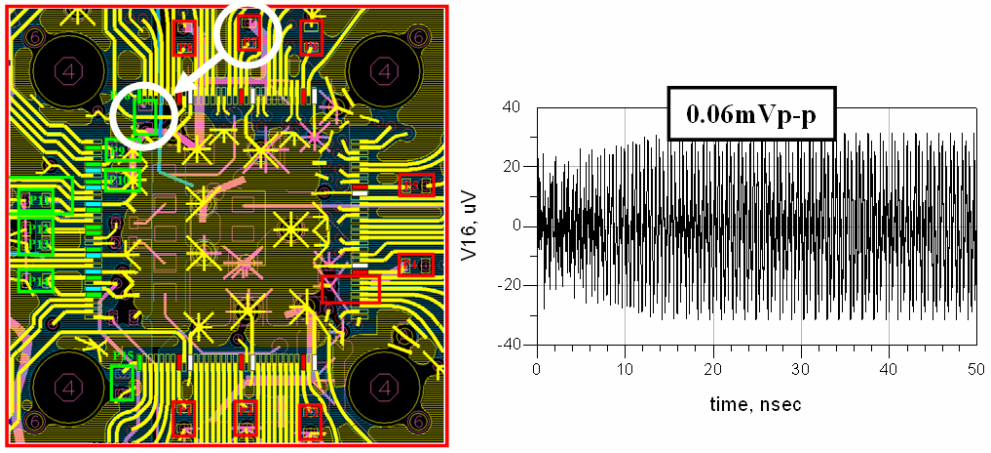


(f)

Figure B.8: Continued.

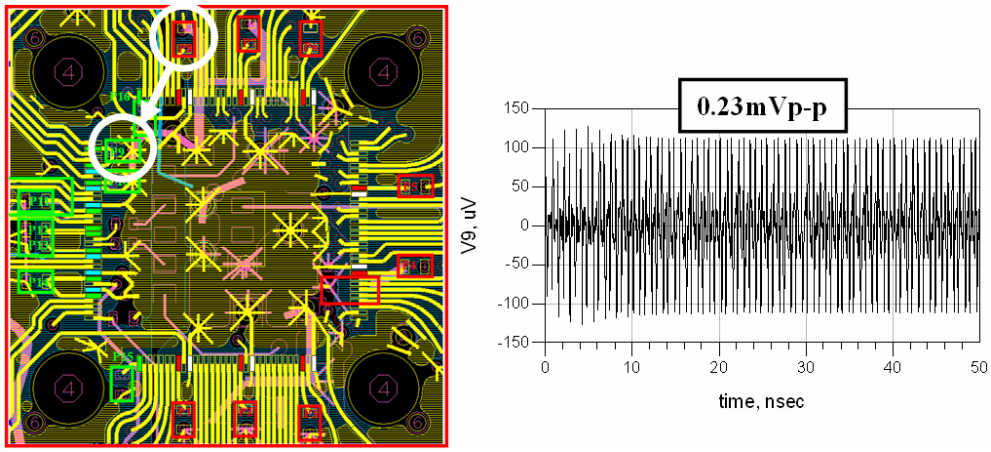


(g)

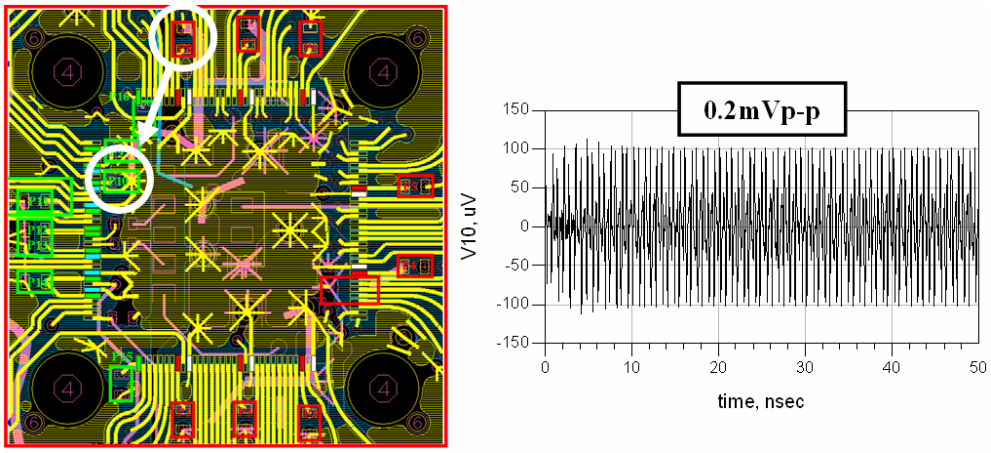


(h)

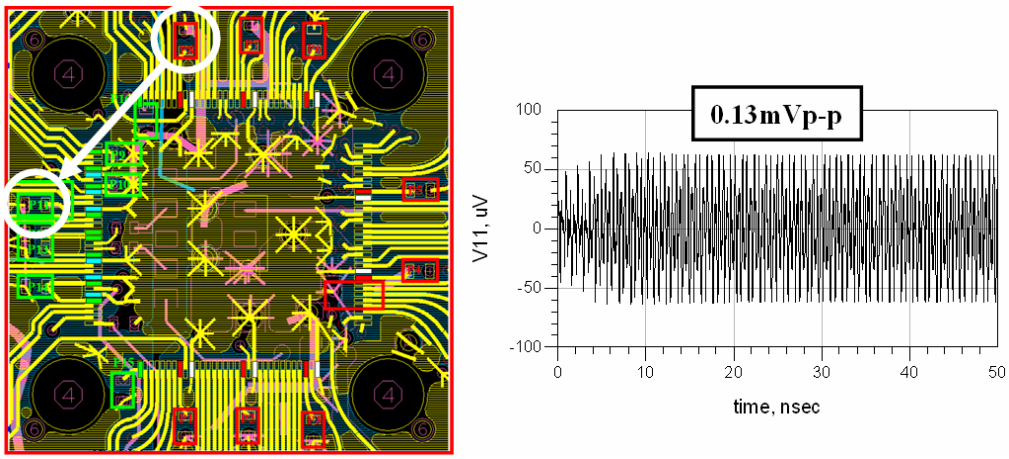
Figure B.8: Continued.



(a)

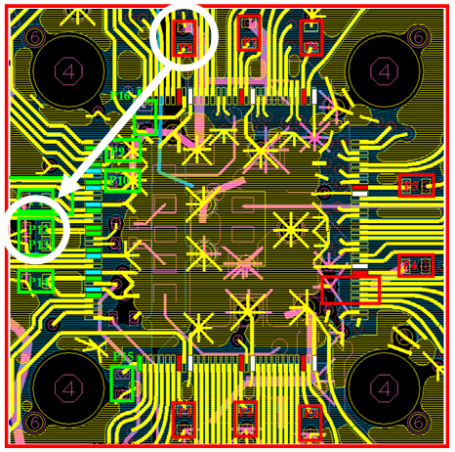


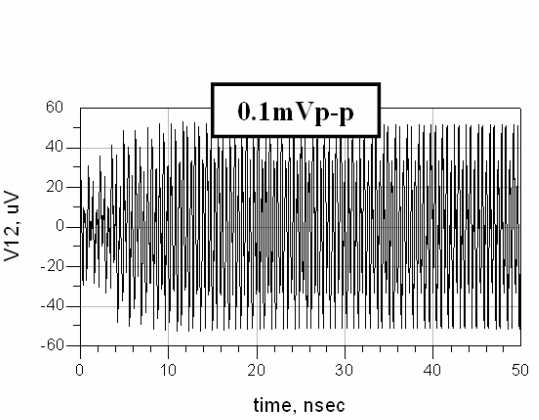
(b)



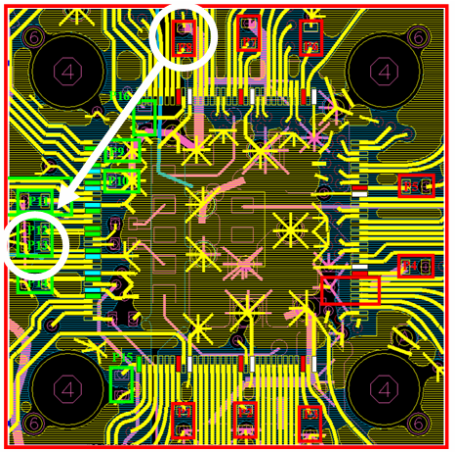
(c)

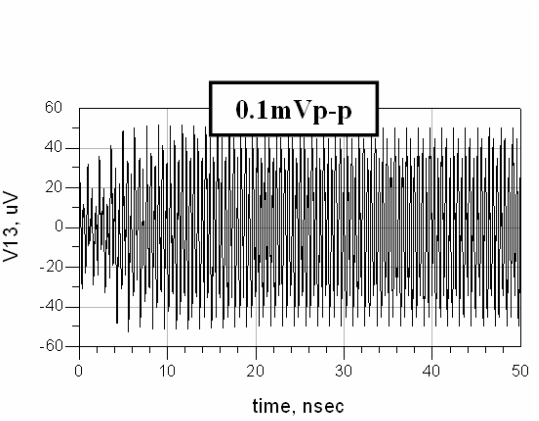
Figure B.9: The coupled noise from P8 to (a) P9, (b) P10, (c) P11, (d) P12, (e) P13, (f) P14, (g) P15, and (h) P16.



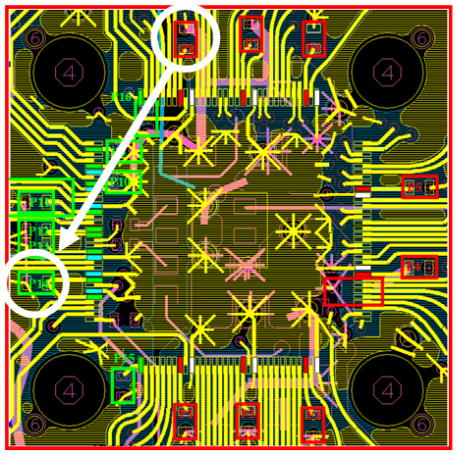


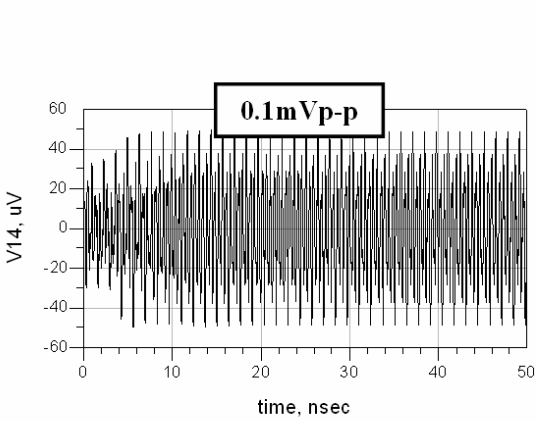
(d)





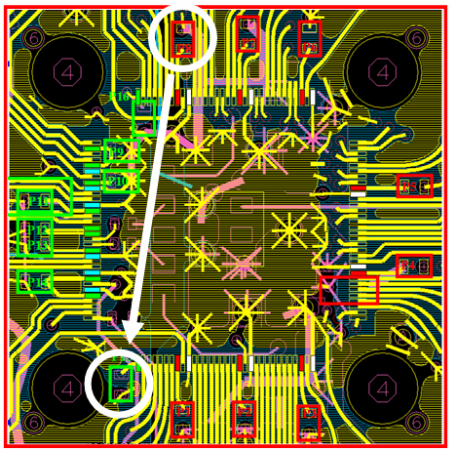
(e)

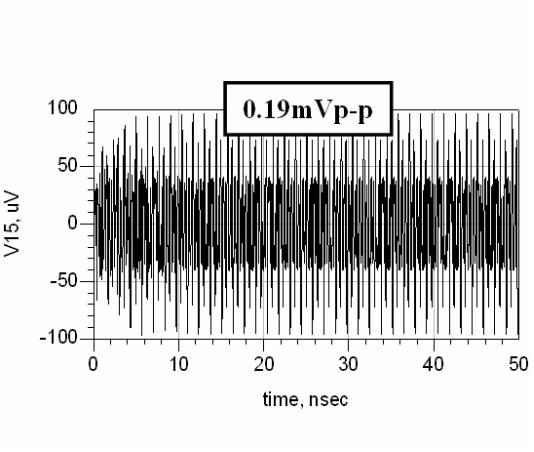




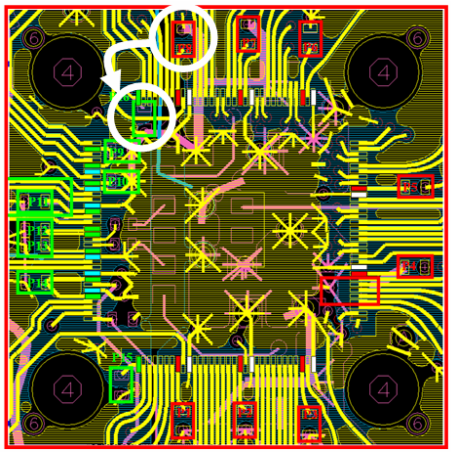
(f)

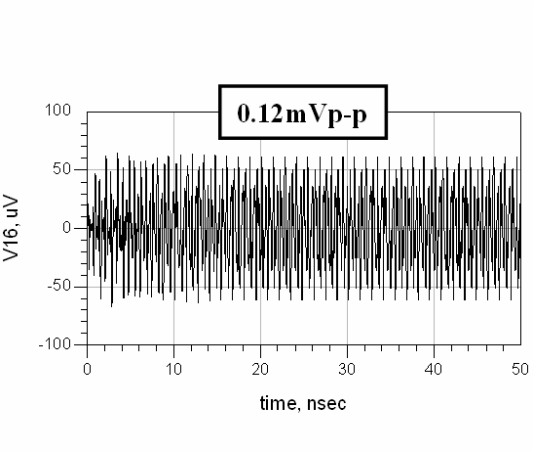
Figure B.9: Continued.





(g)





(h)

Figure B.9: Continued.

APPENDIX C

FREQUENCY-DOMAIN COMPARISONS BETWEEN PRE- AND POST-MODIFICATION BOARDS

Frequency-domain simulation results for the comparison between the pre-modification board and the post-modification board are shown in this appendix. For the comparison, used is scattering parameter (S_{ij}), which is equivalent to the transmission coefficient from port j (location j) to port i (location i). The i varies from 9 to 16 to represent P9 through P16, and the j varies from 1 to 8 to represent P1 through P8 (refer to Figure 6.1 for the locations).

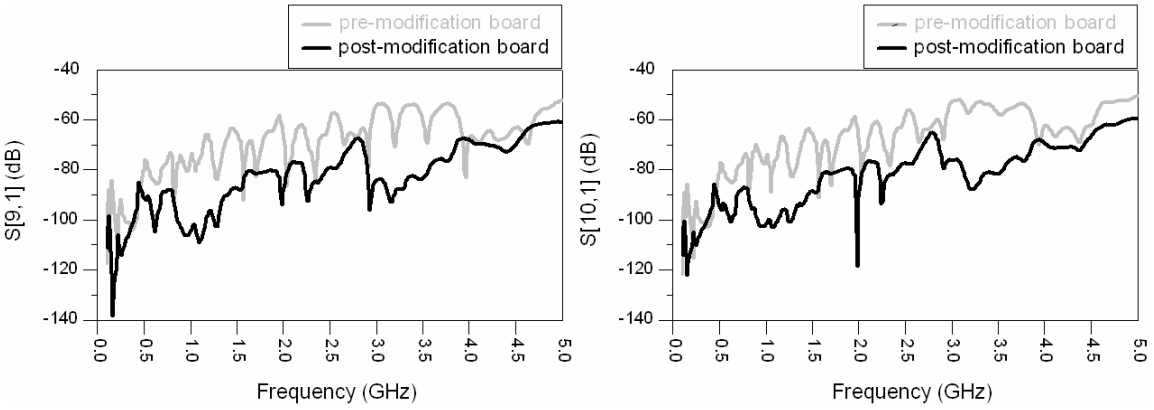
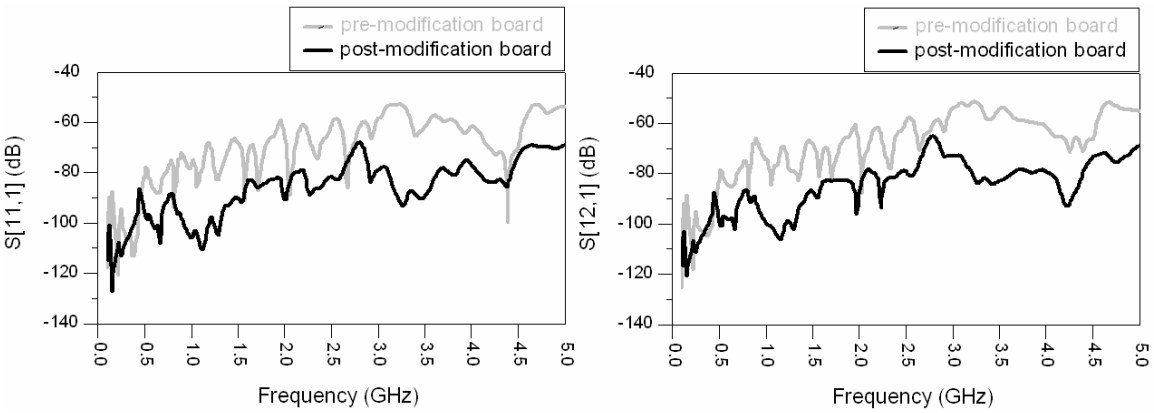
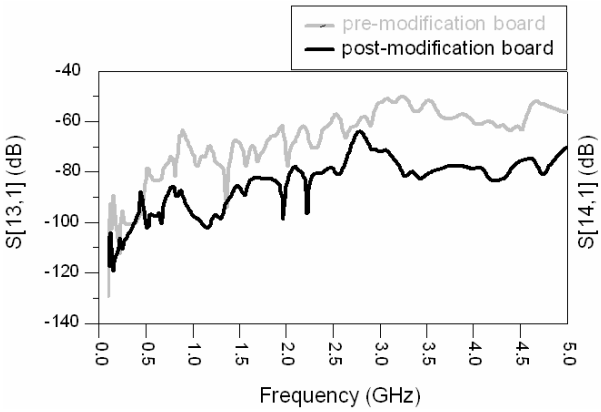


Figure C.1: Transmission coefficient in dB for the pre-modification board (gray) and the post-modification board (black): (a) S[9,1] from P1 to P9, (b) S[10,1] from P1 to P10, (c) S[11,1] from P1 to P11, (d) S[12,1] from P1 to P12, (e) S[13,1] from P1 to P13, (f) S[14,1] from P1 to P14, (g) S[15,1] from P1 to P15, and (h) S[16,1] from P1 to P16. Refer to Figure 1 for the locations.

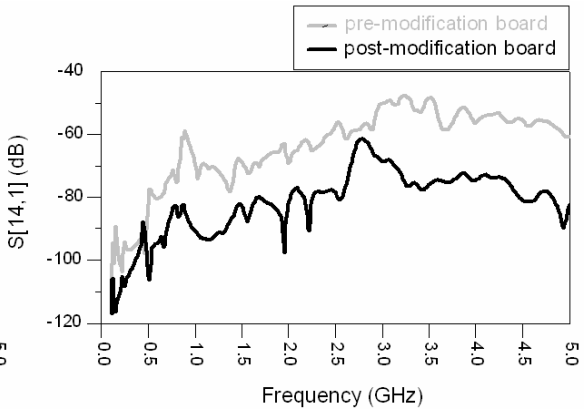


(c)

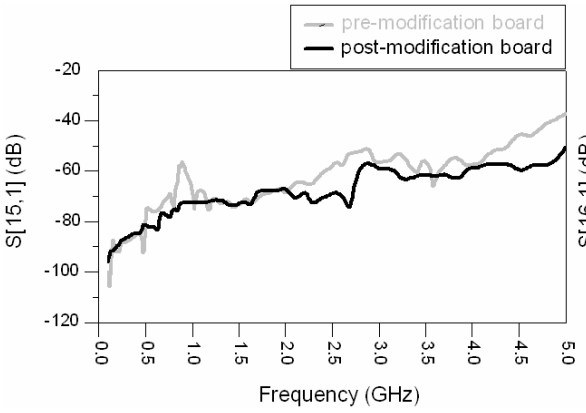
(d)



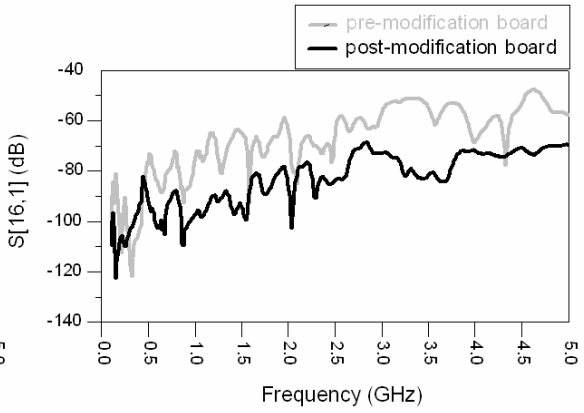
(e)



(f)



(g)



(h)

Figure C.1: Continued.

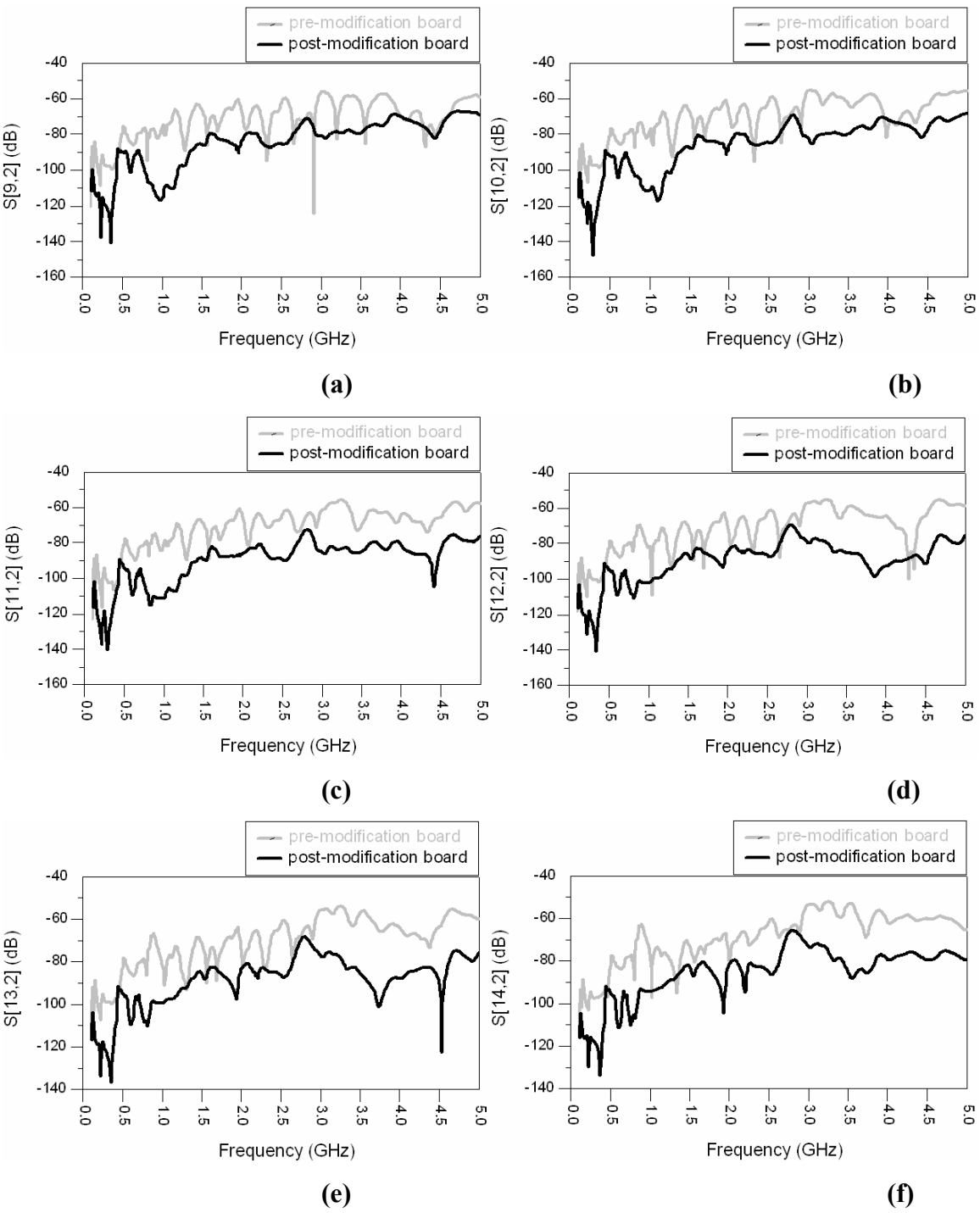
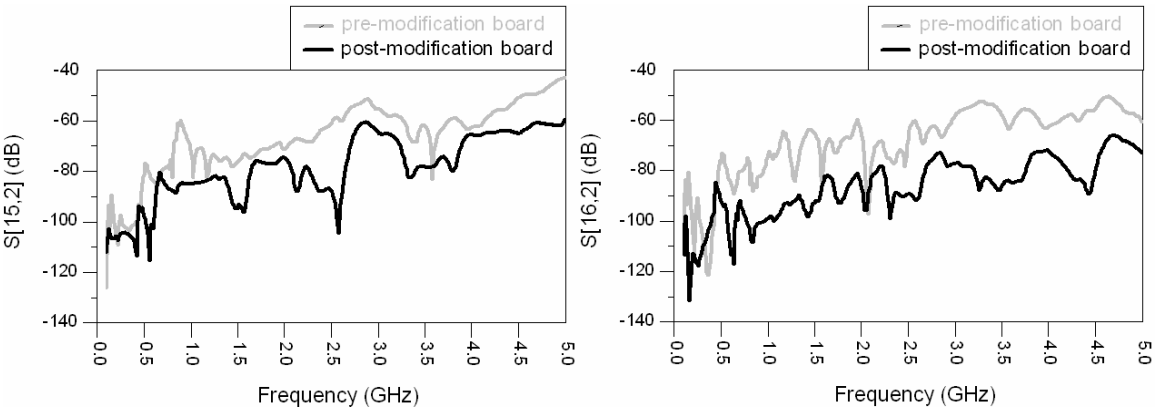


Figure C.2: Transmission coefficient in dB for the pre-modification board (gray) and the post-modification board (black): (a) S[9,2] from P2 to P9, (b) S[10,2] from P2 to P10, (c) S[11,2] from P2 to P11, (d) S[12,2] from P2 to P12, (e) S[13,2] from P2 to P13, (f) S[14,2] from P2 to P14, (g) S[15,2] from P2 to P15, and (h) S[16,2] from P2 to P16. Refer to Figure 1 for the locations.



(g) **(h)**

Figure C.2: Continued.

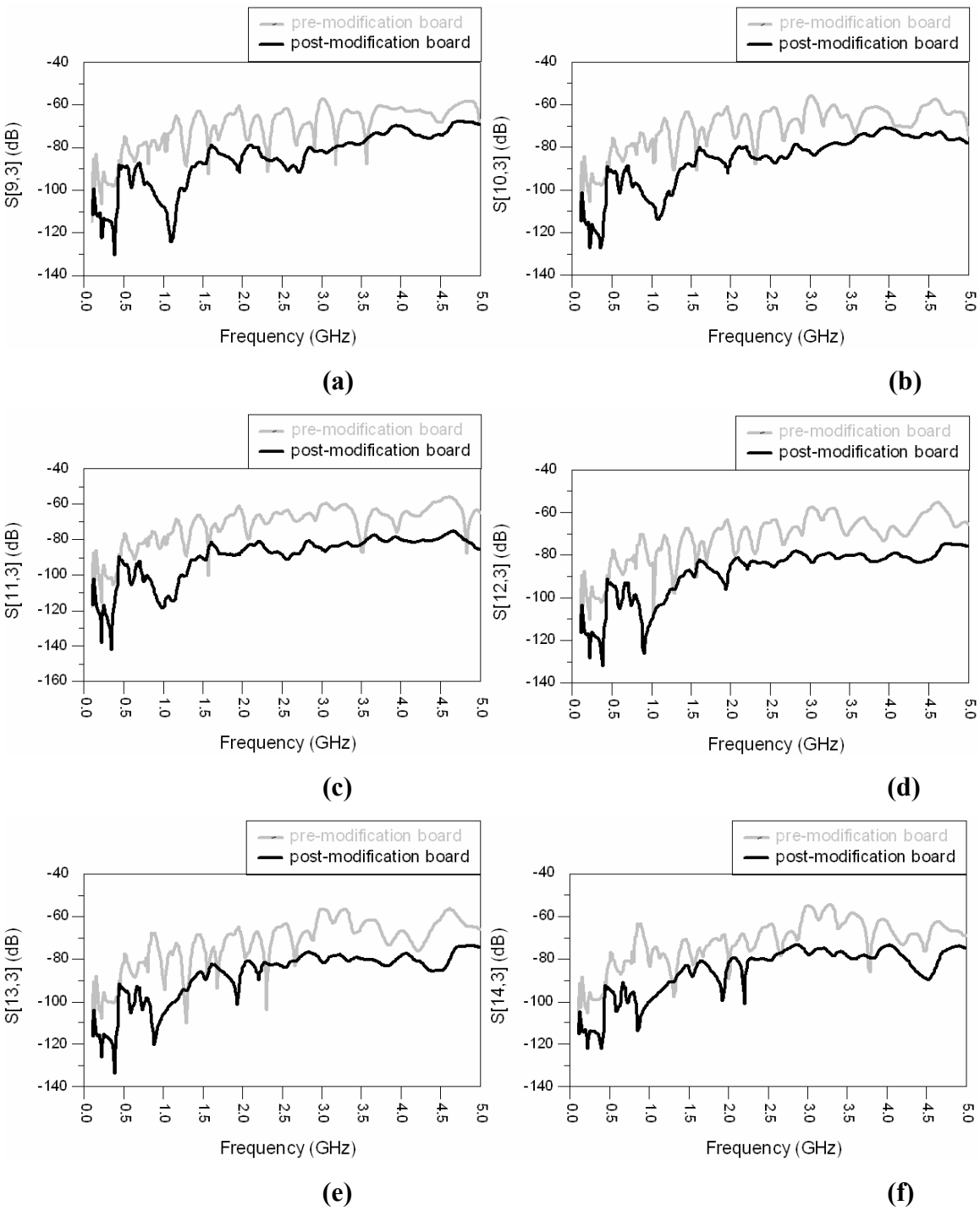
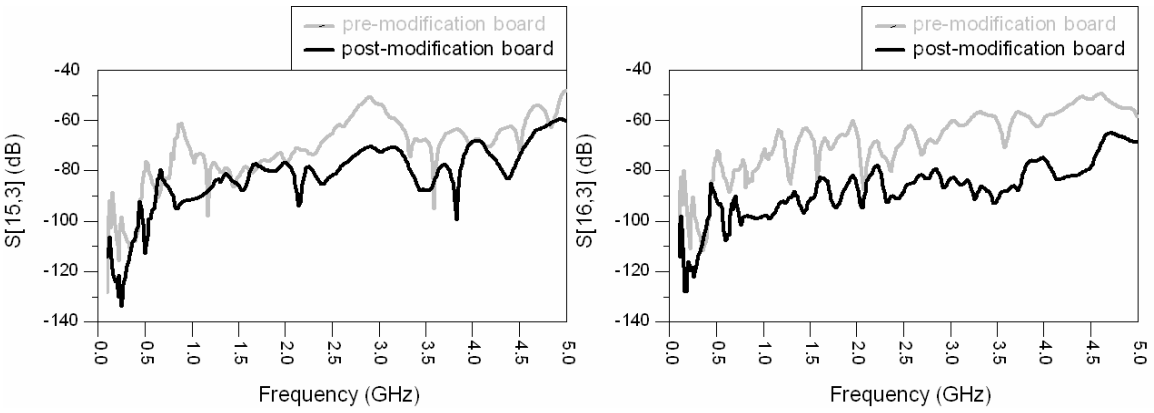


Figure C.3: Transmission coefficient in dB for the pre-modification board (gray) and the post-modification board (black): (a) S[9,3] from P3 to P9, (b) S[10,3] from P3 to P10, (c) S[11,3] from P3 to P11, (d) S[12,3] from P3 to P12, (e) S[13,3] from P3 to P13, (f) S[14,3] from P3 to P14, (g) S[15,3] from P3 to P15, and (h) S[16,3] from P3 to P16. Refer to Figure 1 for the locations.



(g) **(h)**

Figure C.3: Continued.

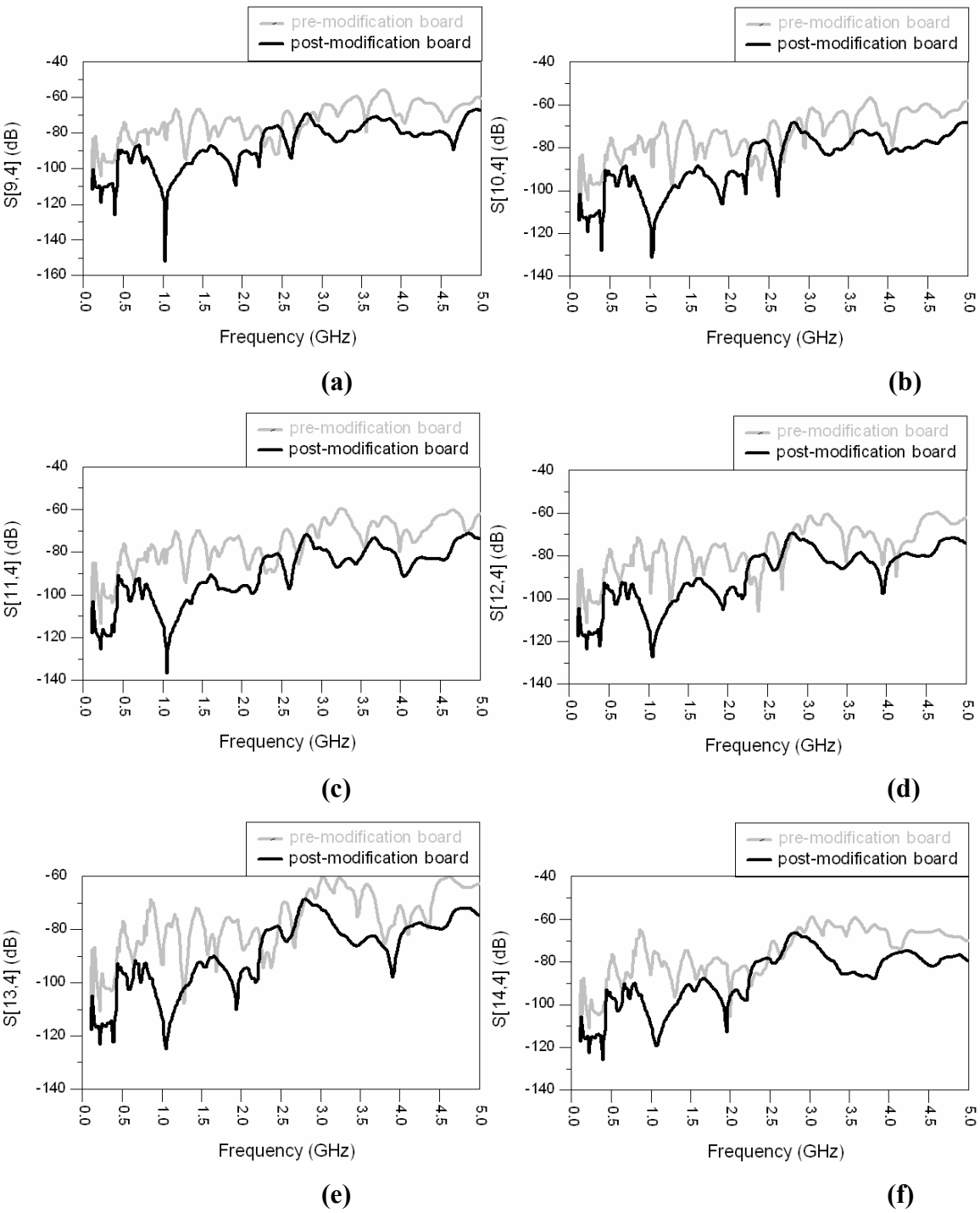
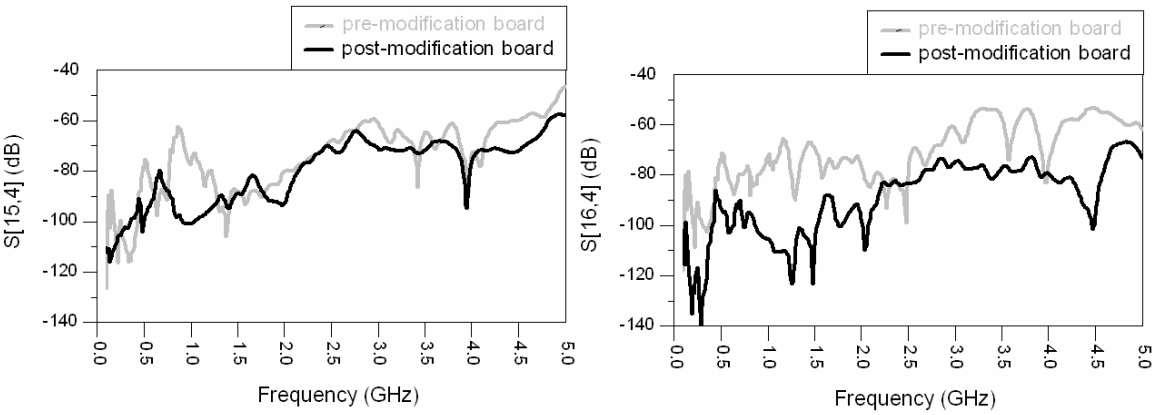


Figure C.4: Transmission coefficient in dB for the pre-modification board (gray) and the post-modification board (black): (a) S[9,4] from P4 to P9, (b) S[10,4] from P4 to P10, (c) S[11,4] from P4 to P11, (d) S[12,4] from P4 to P12, (e) S[13,4] from P4 to P13, (f) S[14,4] from P4 to P14, (g) S[15,4] from P4 to P15, and (h) S[16,4] from P4 to P16. Refer to Figure 1 for the locations.



(g) **(h)**

Figure C.4: Continued.

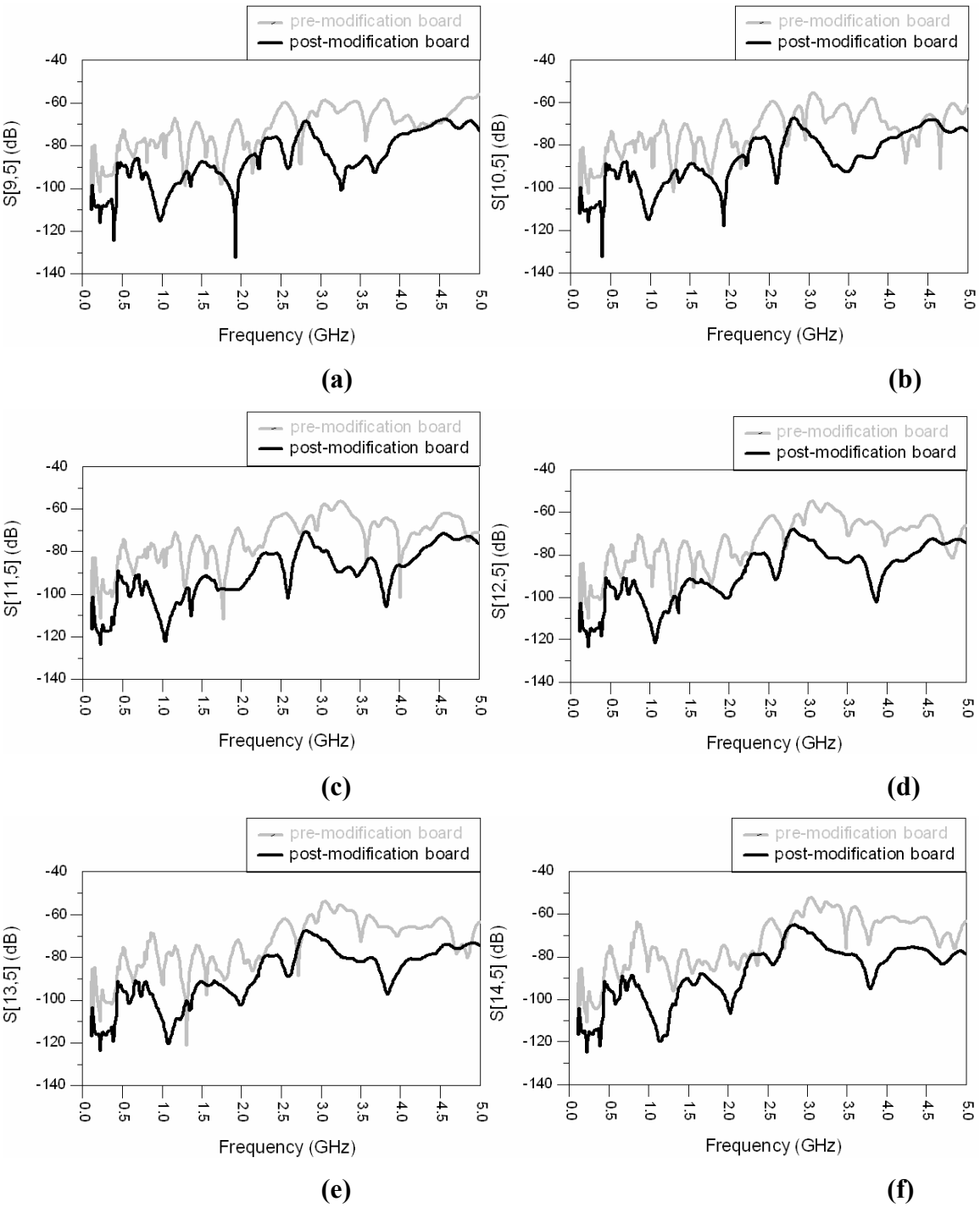
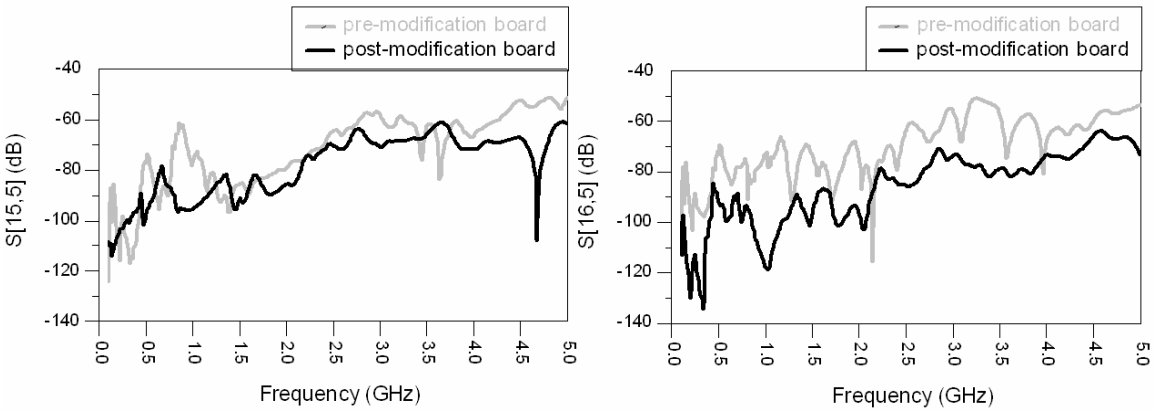


Figure C.5: Transmission coefficient in dB for the pre-modification board (gray) and the post-modification board (black): (a) S[9,5] from P5 to P9, (b) S[10,5] from P5 to P10, (c) S[11,5] from P5 to P11, (d) S[12,5] from P5 to P12, (e) S[13,5] from P5 to P13, (f) S[14,5] from P5 to P14, (g) S[15,5] from P5 to P15, and (h) S[16,5] from P5 to P16. Refer to Figure 1 for the locations.



(g) **(h)**

Figure C.5: Continued.

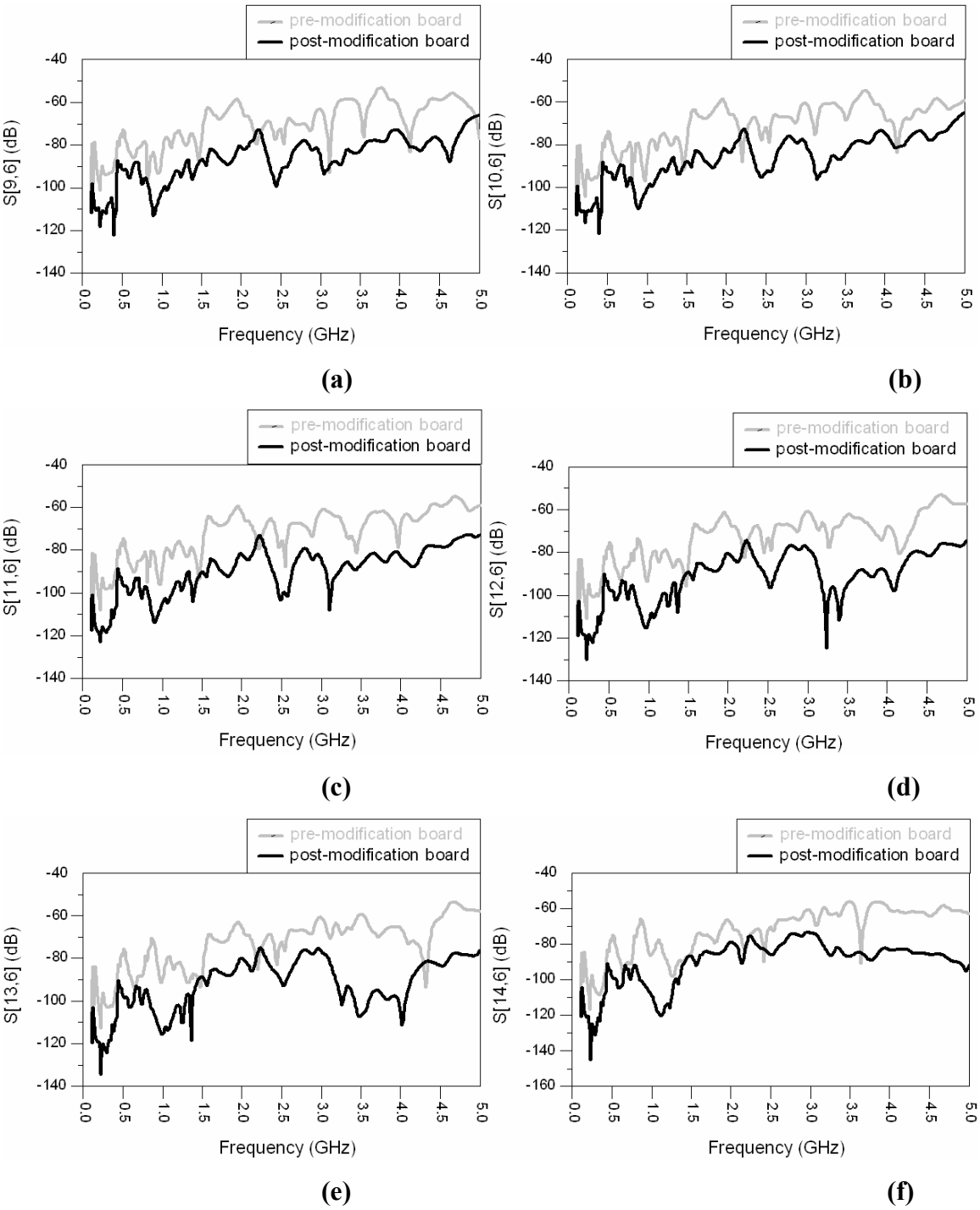
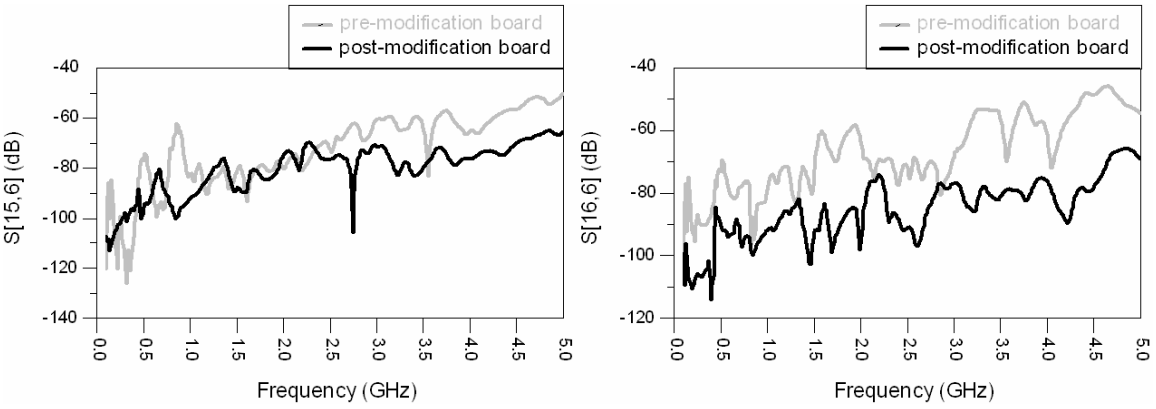


Figure C.6: Transmission coefficient in dB for the pre-modification board (gray) and the post-modification board (black): (a) S[9,6] from P6 to P9, (b) S[10,6] from P6 to P10, (c) S[11,6] from P6 to P11, (d) S[12,6] from P6 to P12, (e) S[13,6] from P6 to P13, (f) S[14,6] from P6 to P14, (g) S[15,6] from P6 to P15, and (h) S[16,6] from P6 to P16. Refer to Figure 1 for the locations.



(g) **(h)**

Figure C.6: Continued.

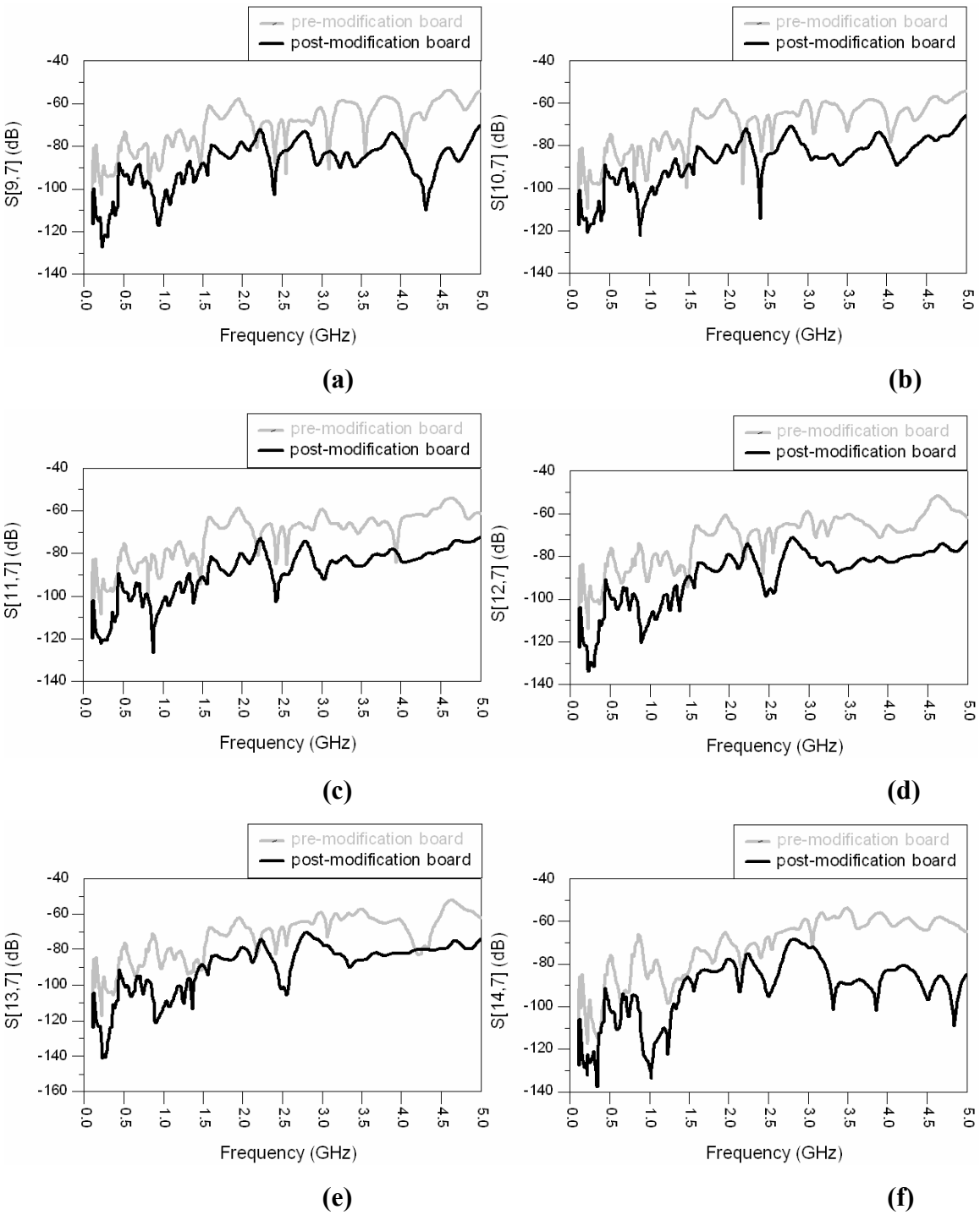
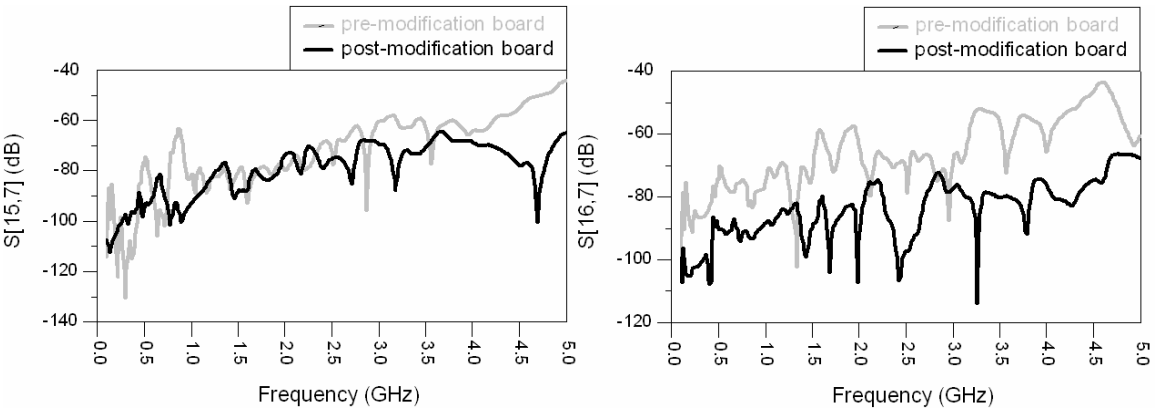


Figure C.7: Transmission coefficient in dB for the pre-modification board (gray) and the post-modification board (black): (a) S[9,7] from P7 to P9, (b) S[10,7] from P7 to P10, (c) S[11,7] from P7 to P11, (d) S[12,7] from P7 to P12, (e) S[13,7] from P7 to P13, (f) S[14,7] from P7 to P14, (g) S[15,7] from P7 to P15, and (h) S[16,7] from P7 to P16. Refer to Figure 1 for the locations.



(g) **(h)**

Figure C.7: Continued.

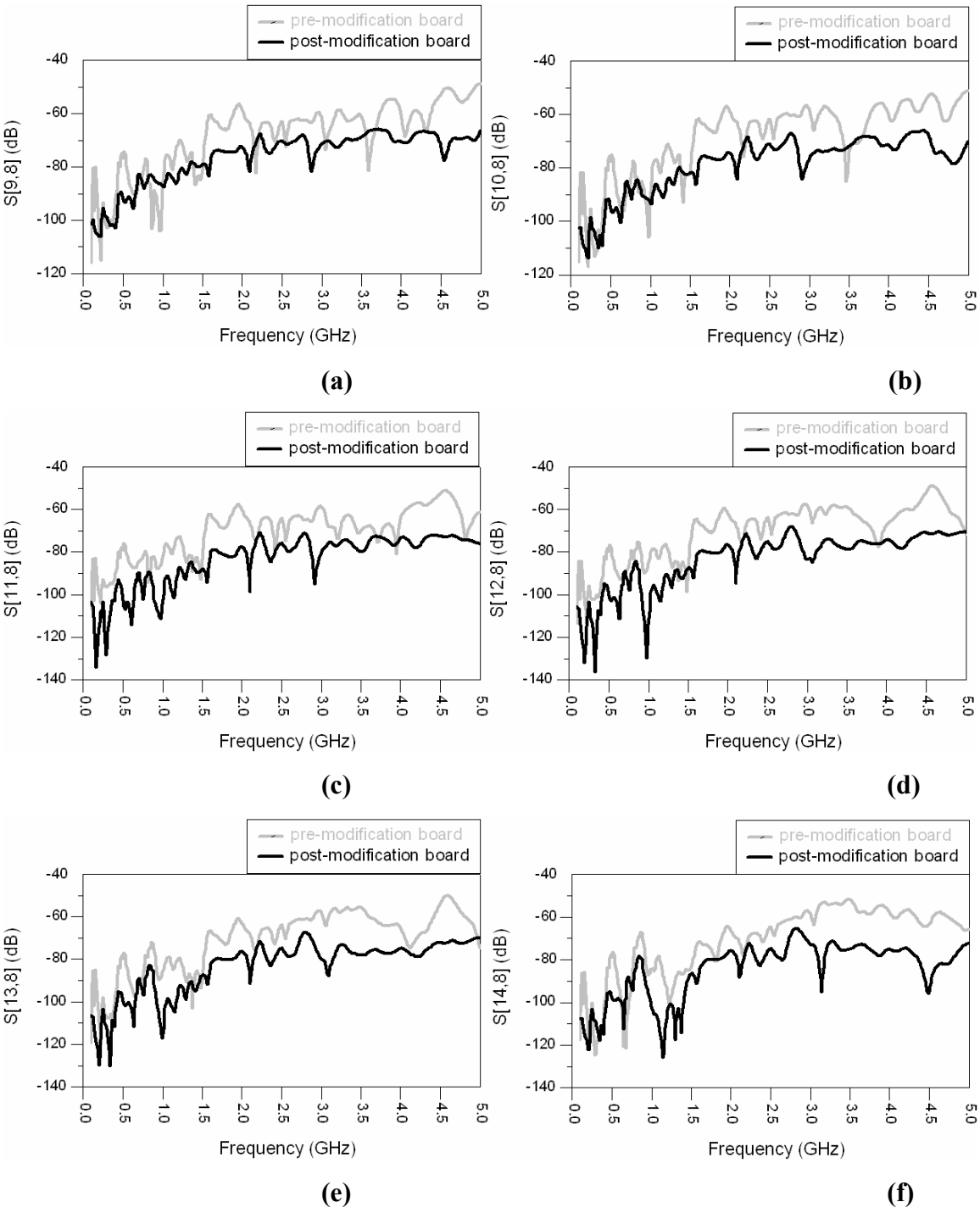
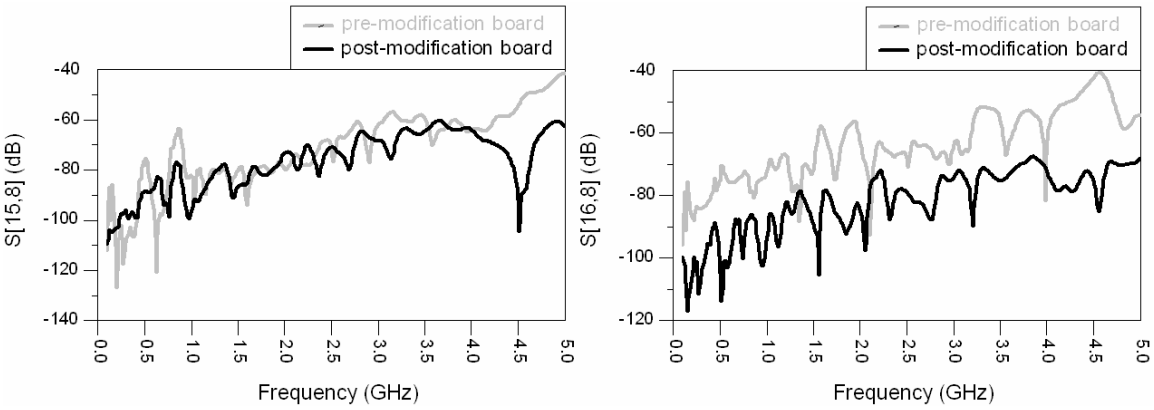


Figure C.8: Transmission coefficient in dB for the pre-modification board (gray) and the post-modification board (black): (a) S[9,8] from P8 to P9, (b) S[10,8] from P8 to P10, (c) S[11,8] from P8 to P11, (d) S[12,8] from P8 to P12, (e) S[13,8] from P8 to P13, (f) S[14,8] from P8 to P14, (g) S[15,8] from P8 to P15, and (h) S[16,8] from P8 to P16. Refer to Figure 1 for the locations.



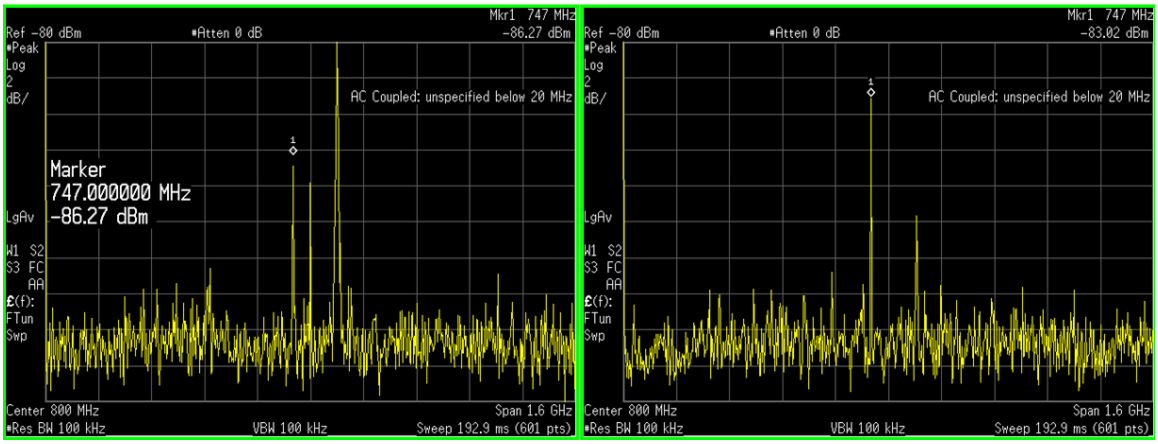
(g) **(h)**

Figure C.8: Continued

APPENDIX D

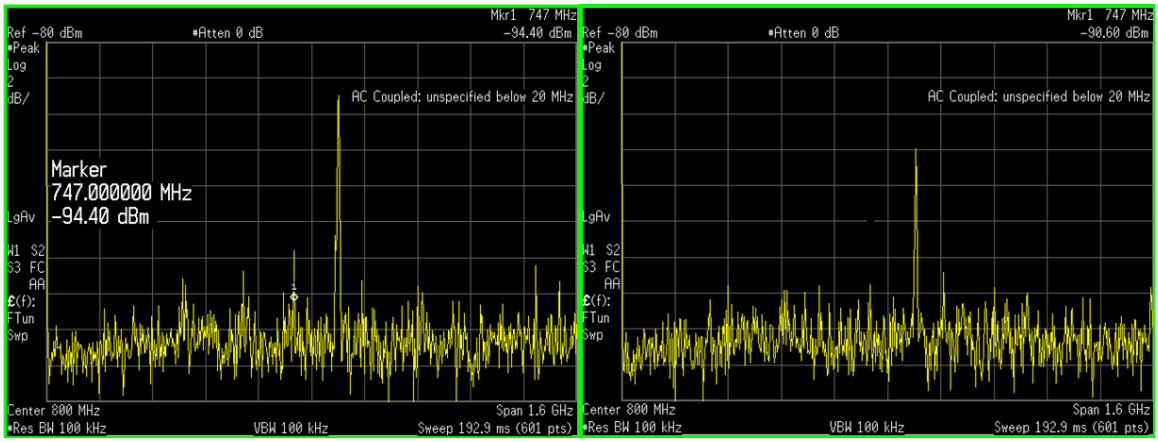
MEASUREMENT RESULTS FOR PRE- AND POST-MODIFICATION BOARDS

Measurement results for the pre-modification board and the post-modification board are shown in this appendix.



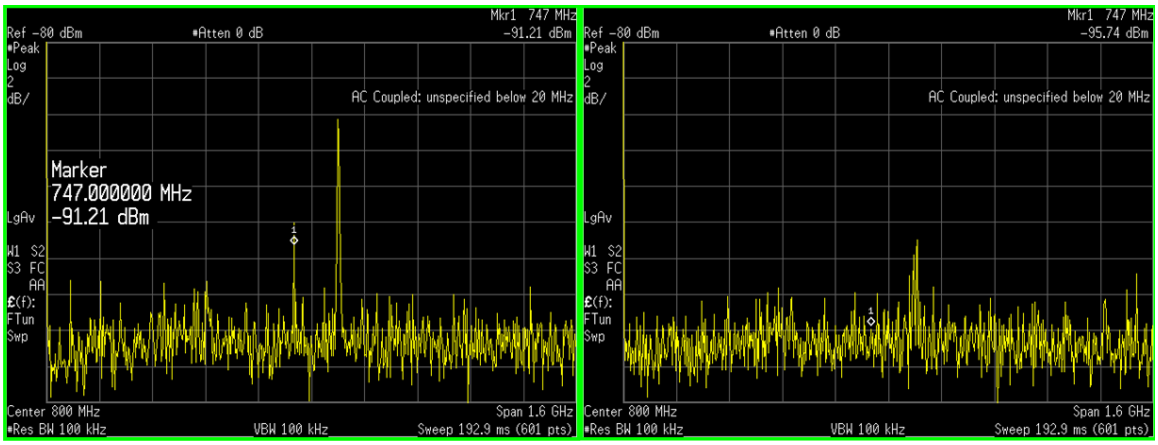
(a) **(b)**

Figure D.1: Noise spectrum measured at P1 (refer to Figure 1) (a) for the pre-modification board and (b) the post-modification board



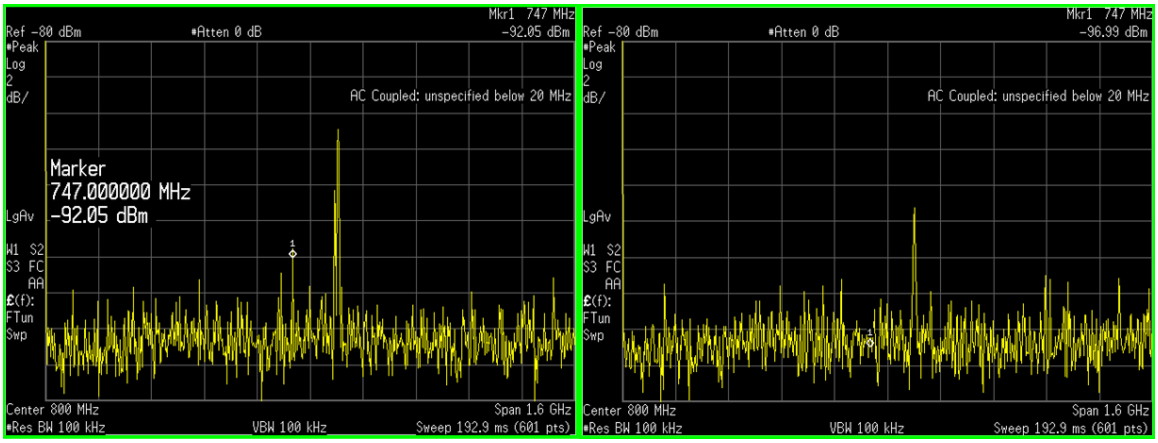
(a) **(b)**

Figure D.2: Noise spectrum measured at P2 (refer to Figure 1) (a) for the pre-modification board and (b) the post-modification board



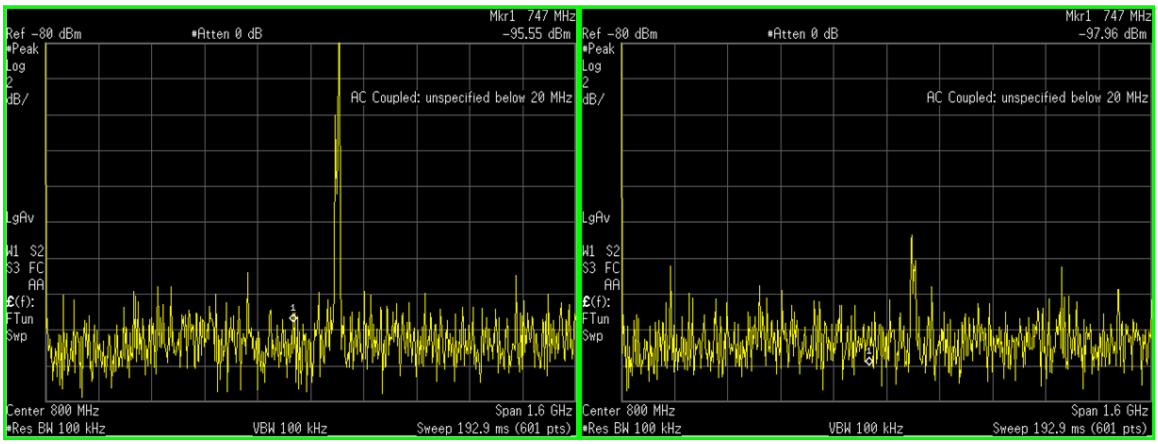
(a) **(b)**

Figure D.3: Noise spectrum measured at P3 (refer to Figure 1) (a) for the pre-modification board and (b) for the post-modification board



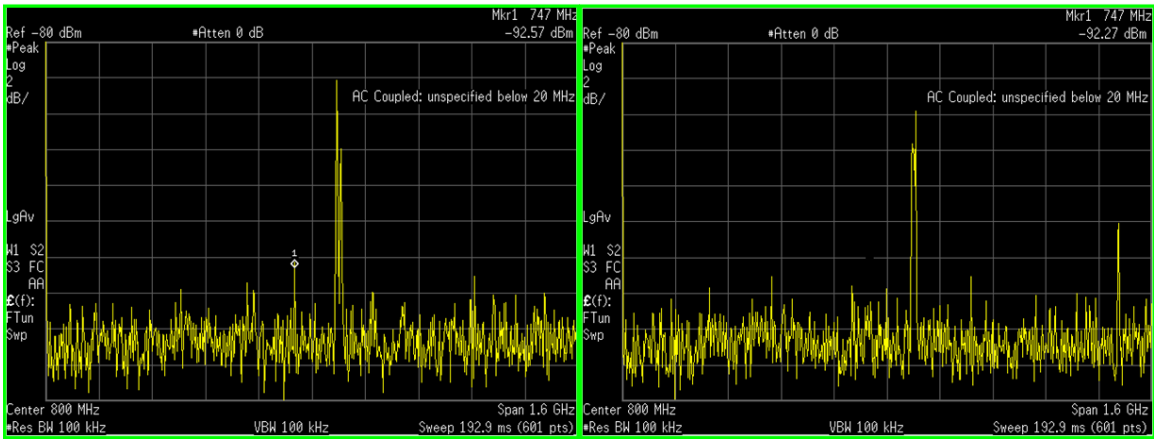
(a) **(b)**

Figure D.4: Noise spectrum measured at P4 (refer to Figure 1) (a) for the pre-modification board and (b) for the post-modification board



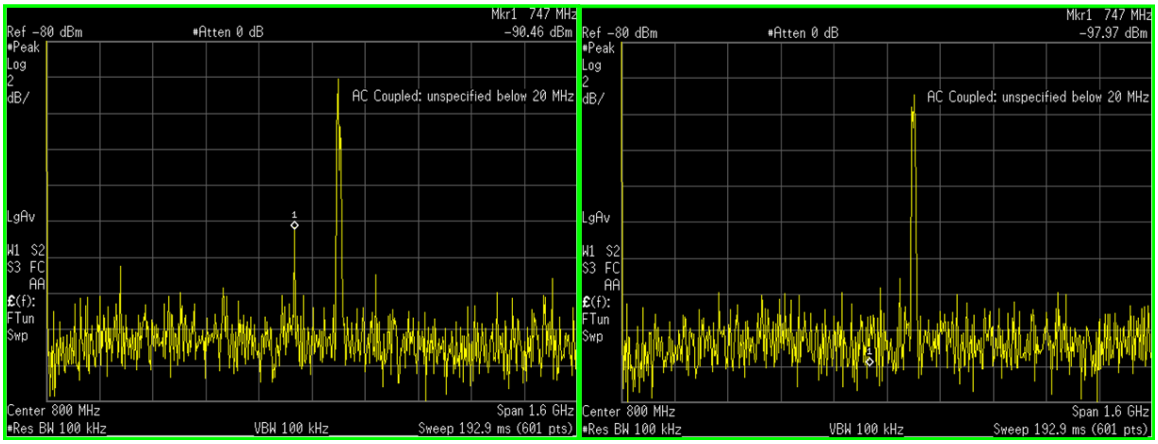
(a) **(b)**

Figure D.5: Noise spectrum measured at P5 (refer to Figure 1) (a) for the pre-modification board and (b) for the post-modification board



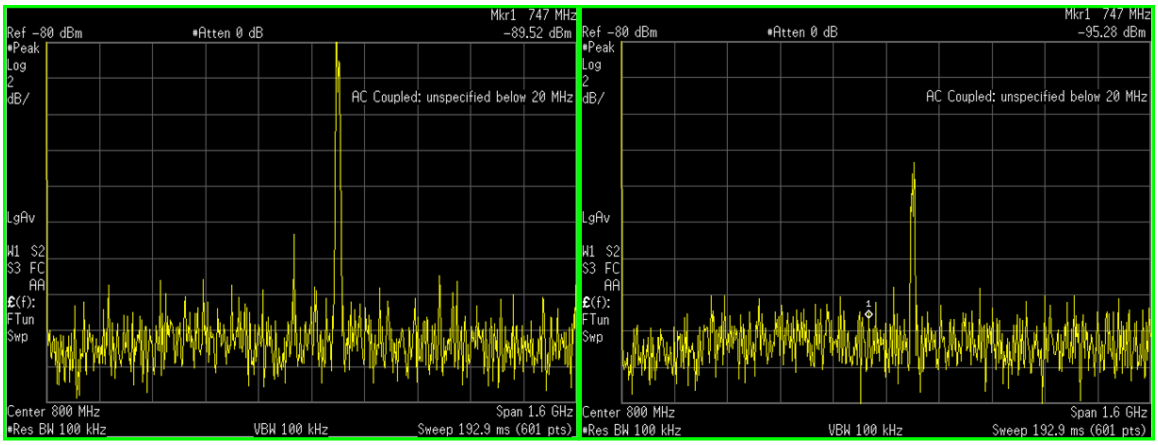
(a) **(b)**

Figure D.6: Noise spectrum measured at P6 (refer to Figure 1) (a) for the pre-modification board and (b) for the post-modification board



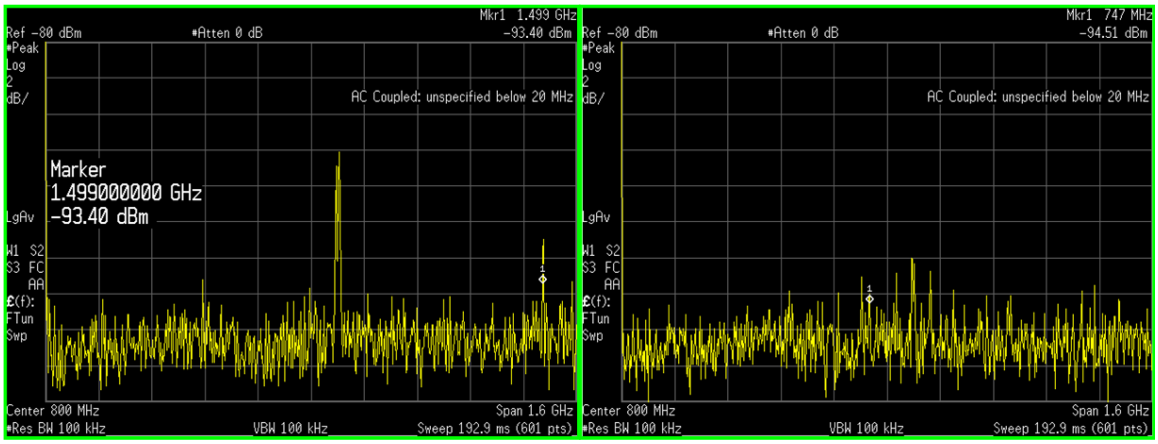
(a) **(b)**

Figure D.7: Noise spectrum measured at P7 (refer to Figure 1) (a) for the pre-modification board and (b) for the post-modification board



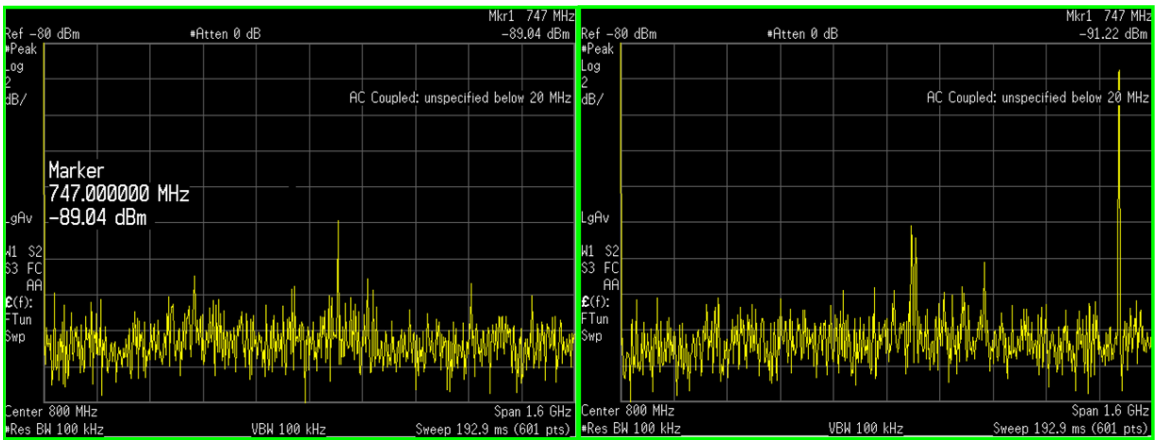
(a) **(b)**

Figure D.8: Noise spectrum measured at P8 (refer to Figure 1) (a) for the pre-modification board and (b) for the post-modification board



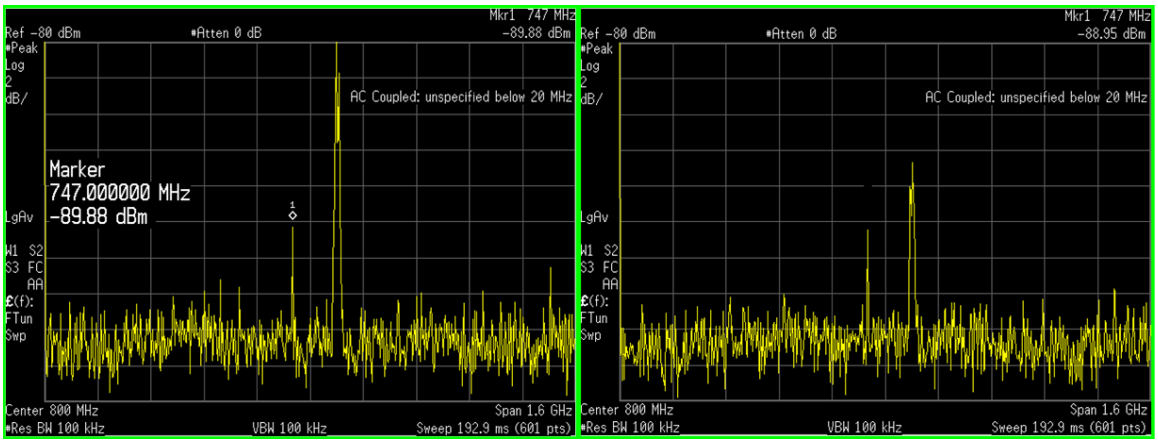
(a) **(b)**

Figure D.9: Noise spectrum measured at P9 (refer to Figure 1) (a) for the pre-modification board and (b) for the post-modification board



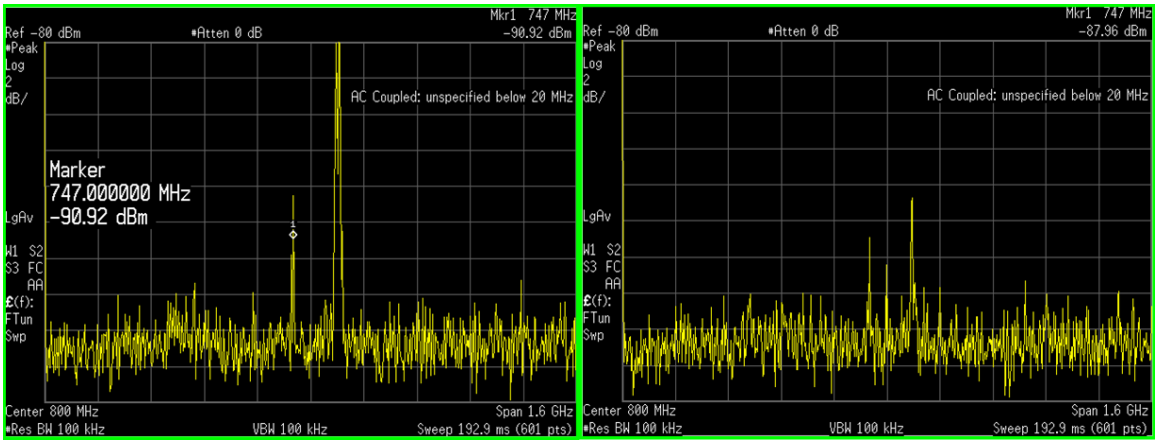
(a) **(b)**

Figure D.10: Noise spectrum measured at P10 (refer to Figure 1) (a) for the pre-modification board and (b) for the post-modification board



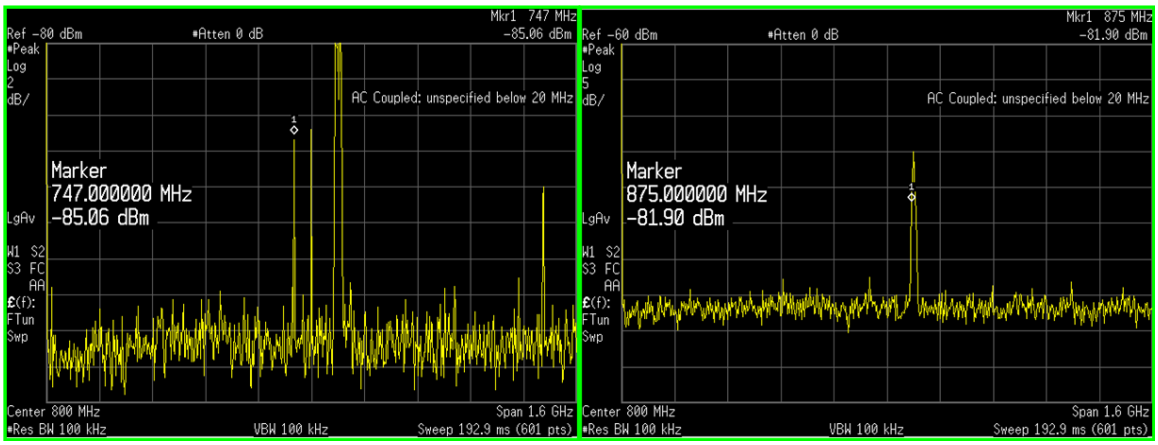
(a) **(b)**

Figure D.11: Noise spectrum measured at P11 (refer to Figure 1) (a) for the pre-modification board and (b) for the post-modification board



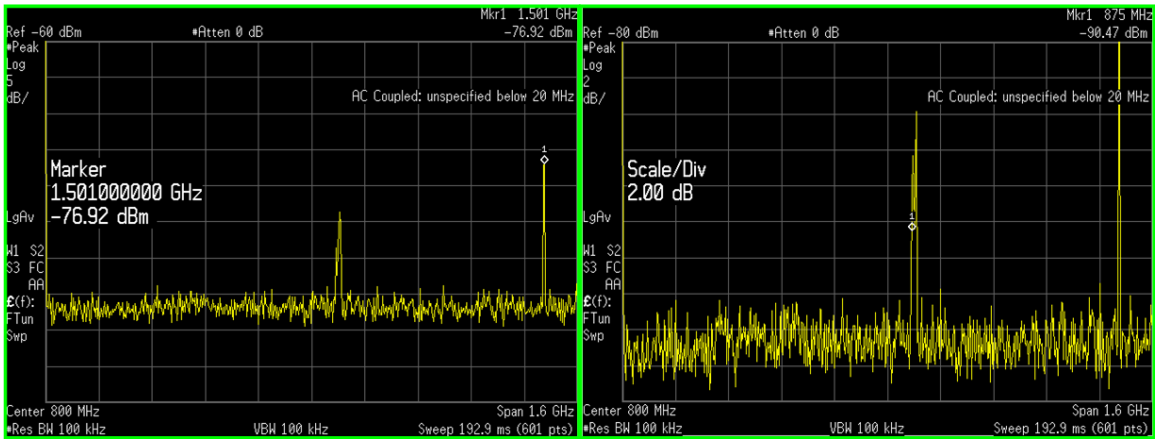
(a) **(b)**

Figure D.12: Noise spectrum measured at P12 and P13 (refer to Figure 1) (a) for the pre-modification board and (b) for the post-modification board



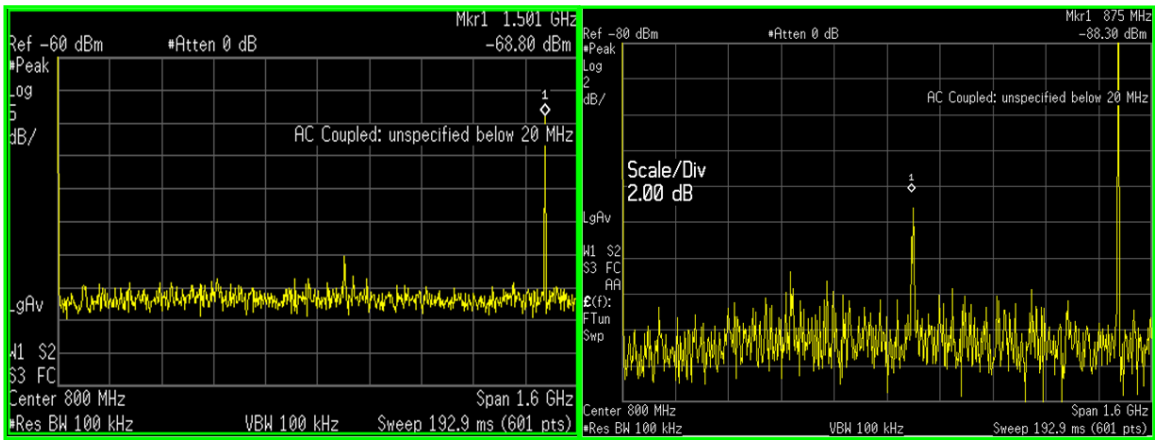
(a) **(b)**

Figure D.13: Noise spectrum measured at P14 (refer to Figure 1) (a) for the pre-modification board and (b) for the post-modification board



(a) **(b)**

Figure D.14: Noise spectrum measured at P15 (refer to Figure 1) (a) for the pre-modification board and (b) for the post-modification board



(a) **(b)**

Figure D.15: Noise spectrum measured at P16 (refer to Figure 1) (a) for the pre-modification board and (b) for the post-modification board

REFERENCES

[1] A. R. Djordjević and T. K. Sarkar, "An investigation of Delta-I Noise on Integrated Circuits," *IEEE Trans. Electromagnetic Compatibility*, vol. 35, pp. 134-147, May 1993.

[2] S. V. D. Berghe, F. Olyslager, D. D. Zutter, J. D. Moerloose, and W. Temmerman, "Study of the Ground Bounce Caused by Power Plane Resonances," *IEEE Trans. Electromagnetic Compatibility,* vol. 40, pp. 111-119, May 1998.

[3] H. Liaw and H. Merkelo, "Signal integrity issues at split ground and power planes," *Proceedings of Electronic Components and Technology Conference*, pp. 752-755, May 1996.

[4] T. Kim, J. Lee, H. Kim, P. J. Jun, and J. Kim, "The improvement of signal integrity according to the location of via in the vicinity of a slot in the reference plane," *Proc. of IEEE 6th Workshop on Signal Propagation on Interconnects*, 2002, pp. 185-188.

[5] T. Kim, J. Lee, H. Kim, and J. Kim, "3GHz Wide Frequency Model of Ferrite Bead for Power/Ground Noise Simulation of High-Speed PCB," *Proc. of IEEE 11th Topical Meeting on Electrical Performance of Electronic Packaging,* 2002, pp. 217-220.

[6] T. Kamgaing and O. Ramahi, "A novel power plane with integrated simultaneous switching noise mitigation capability using high impedance surface," *IEEE Microwave and Guided Wave Letters*, vol. 13, no. 1, January 2003.

[7] R. Abhari and G. V. Eleftheriades, "Metallo-dielectric electromagnetic bandgap structures for suppression and isolation of the parallel-plate noise in high-speed circuits," *IEEE Tran. Microwave Theory and Techniques*, vol. 51, no. 6, pp. 1629-1639, June 2003.

[8] J. Choi, V. Govind, M. Swaminathan, L. Wan, R. Doraiswami, "Isolation in mixed-signal systems using a novel electromagnetic bandgap (EBG) structure," *IEEE Electrical Performance of Electronic Packaging,* pp. 199-202, 2004.

[9] J. Choi, V. Govind, and M. Swaminathan, "A novel electromagnetic bandgap (EBG) structure for mixed-signal system applications," *IEEE Radio and Wireless Conference (RAWCON) 2004*, Atlanta, GA, pp. 243-246, September 2004.

[10] R. Gonzalo, P. Maagt, and M. Sorolla, "Enhanced patchantenna performance by suppressing surface wave using photonic-bandgap substrates," *IEEE Trans. Microwave Theory Tech.,* vol. 47, no. 11, pp. 2131-2138.

[11] R. Coccioli, F. R. Yang, K. P. Ma, and T. Itoh, "Aperture coupled patch antenna on UC-HIP substrate," *IEEE Trans. Microwave Theory Tech.,* vol. 47, no. 11, pp. 2123-2130, Nov. 1999.

[12] Y. Qian, R. Coccioli, D. Sievenpiper, V. Radisic, E. Yablonovitch, and T. Itoh, "A microstrip patch antenna using novel photonic bandgap structures," Microw. J., pp. 66-76, Jan. 1999.

[13] J. D. Shumpert, W. J. Chappell, L. P. B. Katehi, " Parallel-plate mode reduction in conductor-backed slots using electromagnetic bandgap substrates," IEEE Trans. Microw. Theory Tech., vol. 47, no. 11, pp. 2099-2104, Nov. 1999.

[14] M. Fallah-Rad, L. Shatai, "Enhanced performance of a microstrip patch antenna using a high impedance EBG structure," IEEE Antennas and Propagation Society International Symposium, vol. 3, pp. 982-985, June 2003.

[15] W. J. Chappell, M. P. Little, L. P. B. Katehi, "High Isolation, Planar Filters Using EBG Substrates," *IEEE Microwave and Wireless Components Letters,* vol. 11, pp. 246-248, June 2001.

[16] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection of modern CMOS technology," *IEEE Trans. Adv. Packag.*, vol. 22, no. 3, pp. 284-291, August 1999.

[17] B. Young, *Digital Signal Integrity Modeling and Simulation with Interconnects and Packages,* Prentice Hall, 2001.

[18] R. Dowing, P. Gebler, and G. A. Katopis, "Decoupling capacitance effects on switching noise," *IEEE Trans. Comp., Hybrids, Manufact. Technol.*, vol. 16, pp. 484-489, Aug. 1993.

[19] T. Takken, "Integral decoupling capacitors reduces multichip module ground bounce," *in Proc. IEEE Multichip Module*, pp. 79-84, March 1993.

[20] T. Chou, "Effect of on-package decoupling capacitors on the simultaneous switching noise," in Proc. 6th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 55-58, October 1997.

[21] G. W. H. S. H. Hall and J. A. McCall, *High-Speed Digital System Design*. JOHN WILEY and SONS, INC., 2000.

[22] T. Kamgaing and O. Ramahi, "High-impedance electromagnetic surface for parallel-plate mode suppression in high-speed digital systems," *in Proceeding of IEEE 11th Topical Meeting on Electrical and Performance of Electronic Packaging (EPEP),* pp. 279-282, October 2002.

[23] M. Swaminathan, J. Kim, I. Novak, and J. P. Libous, "Power distribution networks for system-on-package: status and challenges," IEEE Trans. Adv. Packag., vol. 27, no. 2, pp. 286-300, May 2004.

[24] T. H. Kim, D. Chung, E. Engin, W. Yoon, Y. Toyota, and M. Swaminathan, "A Novel Synthesis Method for Designing Electromagnetic Band Gap (EBG) Structures in Packaged Mixed Signal Systems," *IEEE Electronic Components and Technology Conference (ECTC)*, May 2006.

[25] V. Radisic, Y. Qian, R. Coccioli, and T. Itoh, "Novel 2-D photonic band gap structure for microstrip lines," *IEEE Microwave and Guide Wave Letters*, vol. 8, no. 2, pp. 69-71, February 1998.

[26] F. Yang, K. Ma, Y. Qian, and T. Itoh, "A uniplanar compact photonic bandgap (UC-PBG) structure and its applications for microwave circuits," *IEEE Trans. Microwave Theory and Techniques,* vol. 47, no. 8, August 1999.

[27] Z. N. Chen, N. Yang, Y. Y. Wang, and M. Y. W.Chia, "A novel electromagnetic bandgap structure and its application for antenna duplexer," *IEEE Radio and Wireless Conference*, pp. 71-74, September 2002.

[28] D. M. Pozar, *Microwave Engineering*, 2nd ed. New York: Wiley, 1998.

[29] J. Choi, V. Govind, and M. Swaminathan, "Noise suppression in ultra wide band (UWB) applications using alternating impedance electromagnetic bandgap (AI-EBG) structures," *Radar Conference 2005 EURAD European*, pp. 279-282, Oct. 2005.

[30] Y. Toyota, E. Engin, T. Kim, M. Swaminathan, and S. Bhattacharya, "Size Reduction of Electromagnetic Bandgap (EBG) Structures with New Geometries and Materials," *Electronic Components and Technology Conference*, pp. 1784-1789, 2006.

[31] T. Wu, C. Wang, Y. Lin, T. Wang, and G. Chang, "A Novel Power Plane with Supper-Wideband Elimination of Ground Bounce Noise on High Speed Circuits," *IEEE Microwave Wireless Components Lett.*, vol. 15, no. 3, pp. 174-176, March 2005.

[32] K. –P. Ma, K. Hirose, F. –R. Yang, Y. Qian, and T. Itoh, "Realisation of magnetic conducting surface using novel photonic bandgap structure," *Electronics Letters*, vol. 34, Iss. 21, pp. 2041-2042, October 1998.

[33] F. –R. Yang, K. –P. Ma, Y. Qian, and T. Itoh, "A Uniplanar Compact Photonic-Bandgap (UC-PBG) Structure and its Applications for Microwave Circuits," *IEEE Trans. Microwave Theory Tech.,* No. 8, pp. 1509-1514, 1999.

[34] T. E. Moran, K. L. Virga, G. Aguirre, and J. L. Prince, "Methods to reduce radiation from split ground planes in RF and mixed signal packaging structures," *IEEE Trans. Advanced Packaging*, vol. 25, no. 3, pp. 409-416, Aug. 2002.

[35] Y. Zhang, "Microstrip-Multilayer delay line on printed circuit board," University of Nebraska Lincoln, Technical Report, April 2003.

[36] J. Kim and M. Swaminathan, "Modeling of irregular shaped power distribution planes using transmission matrix method," *IEEE Trans. Advanced Packaging*, vol. 24, no. 3, pp. 334-346, 2001.

[37] A. E. Engin, M. Swaminathan, and Y. Toyota, "Finite difference modeling of multiple planes in packages," *in Proc. 17th Int. Zurich Symposium Electromagnetic Compatibility,* Singapore, pp. 549-552, March 2006.

[38] Y. Toyota, E. Engin, T. Kim, M. Swaminathan, K. Uriu, "Stopband Prediction with Dispersion Diagram for Electromagnetic Bandgap Structures in Printed Circuit Boards," *IEEE EMC Symposium*, Portland Oregon, Aug. 2006.

[39] T. Itoh, Ed., *Numerical Techniques for Microwave and Millimeter-Wave Passive Structures.* New York: Wiley, 1989.

[40] K. Bharath, E. Engin, M. Swaminathan, K. Uriu, and T. Yamada, "Efficient Modeling of Package Power Delivery Networks with Fringing Fields and Gap Coupling in Mixed Signal Systems," *IEEE Electrical Performance of Electronic Packaging*, pp. 59-62, 2006.

[41] J. Browne, "Fast data converters advance wireless systems," *Analog Devices. Inc.*, March 2005.

[42] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design, 2nd edition*. New York Oxford, Oxford University Press, 2002.

[43] N. Na, J. Choi, S. Chun, M. Swaminathan, and J. Srinivasan, "Modeling and transient simulation of planes in electronic packages," *Advanced Packaging, IEEE Transactions*, pp. 340-352, Aug. 2000.

[44] J. Park, H. Kim, J. S. Pak, Y. Jeong, S. Baek, J. Kim, and J. –J. Lee, "Noise coupling to signal trace and via from power/ground simultaneous switching noise in high speed double data rates memory module," *in IEEE EMC Symposium*, pp. 592-597, August 2004.

[45] T. Kim, E. Engin, and M. Swaminathan, "Switching noise suppression in mixed signal system applications using electromagnetic band gap (EBG) synthesizer," *in IEEE Electrical Performance of Electronic Packaging (EPEP) 2006*, pp. 47-50, October 2006.

[46] B. Le, T. W. Rondeau, J. H. Reed, and C. W. Bostian, "Analog-to-Digital Converters [A review of the past, present, and future]," *IEEE Signal Processing Magazine,* pp. 69-77, Nov. 2005.

[47] A. Marczyk, Genetic Algorithms and Evolutionary Computation Homepage, http://www.talkorigins.org/faqs/genalg/genalg.html.

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