LAYOUT-LEVEL CIRCUIT SIZING AND DESIGN-FOR-MANUFACTURABILITY METHODS FOR EMBEDDED PASSIVE RF CIRCUITS

A Dissertation
Presented to
The Academic Faculty

By

Souvik Mukherjee

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy
in
Electrical and Computer Engineering

School of Electrical and Computer Engineering
Georgia Institute of Technology
August 2007

Copyright © 2007 by Souvik Mukherjee

LAYOUT-LEVEL CIRCUIT SIZING AND DESIGN-FOR-MANUFACTURABILITY METHODS FOR EMBEDDED PASSIVE RF CIRCUITS

Approved by:

Dr. Madhavan Swaminathan, Advisor
Professor, School of ECE
Georgia Institute of Technology

Dr. Manos Tentzeris
Associate Professor, School of ECE
Georgia Institute of Technology

Dr. Sung Kyu Lim
Associate Professor, School of ECE
Georgia Institute of Technology

Dr. Mervyn Fathianathan
Asst. Professor, School of ECE
Georgia Institute of Technology

Dr. Andrew Peterson
Professor, School of ECE
Georgia Institute of Technology

Date Approved: June 2007

This thesis is dedicated to my uncle Late Prasanta Mukherjee, for his love, inspiration and encouragement.

ACKNOWLEDGMENTS

The last five years at Georgia Tech has been the the most valuable and cherished experience of my life. During this time, I have been helped and guided by numerous people, without whom this effort would not have been a reality. To pen down the magnitude of appreciation and gratitude, I owe to these people, is an impossible task. This is an effort to acknowledge most of, if not all, the people who helped me shape my career at Georgia Tech.

Firstly, I would like to thank my academic advisor, Professor Madhavan Swaminathan, for his continuous academic insight, valuable discussions, enthusiasm and encouragement. I am forever grateful to him for his guidance during my research. As an advisor, he has guided me in difficult times of my student career, and as a guardian and friend, in my personal life. I shall always remember the way he offered to help me when I first approached him to become a graduate researcher under his guidance. I am indebted to all my reading and oral committee members, Professor Worai Wardi, Professor Sung Kyu Lim, Professor Andrew F. Peterson, Professor Manos Tentzeris, and Professor Mervyn Fathianathan, for sitting through my presentations, providing thesis corrections and giving me excellent technical feedback. I would also like to thank my former advisor Professor Sung Kyu Lim for providing me the opportunity to begin my graduate studies at Georgia Tech. I would like to thank late Prof. John Uyemura for all his help and guidance when I applied for graduate studies at Tech.

I express my sincere gratitude to a lot of people who have helped me in my work. Special thanks to my friends and colleagues, especially Dr.Sidharth Dalmia, Dr.Bhyrav Mutnury, Dr.Erdem Matoglu, Dr.Vinu Govind, Dr.Rohan Mandrekar, Dr.Jifeng Mao and Dr.Jinwoo Choi for their friendship and their guidance in my research. I would also like to thank Mr.Venky Sundaram for helping me with the board fabrication, despite his hectic schedules. My sincere thanks to all the Epsilon

group members for providing me with a family at work, far away from my home and family. The times that I have spent with them, both academic and social, will always be some of the most valuable and cherished days of my life. Thanks go to: Subramanian N. Lalgudi, Krishna Bharath, Wansuk Yun, Tae Hong Kim, Nevin Altunyurt, Prathap Muthana, Abdemanaf Tambawala, KiJin Han, Marie-Solange Milleron, Janani Chandrashekhar, Abhilash Goyal and Pradeep Yadav. In particular, I would like acknowledge the help of Subramanian Lalgudi towards the end of my research work, Krishna during my dissertation writing, and Nevin for helping me immensely with all the correspondences and paperwork when I was out of town. Also, during these years, I was also fortunate to find friends who have helped me immensely in different ways, during my stay at Georgia Tech. Special thanks go to Ganesh, Vidya, Raj, Vishwa, Shalab, Maryam, Soumendu, Vivek, Bhaskar, Winston, Tippi, Jacob, Rajarshi, Mrinmoy, Bevin, Arup and Saikat. I share very good memories with all these people.

I would also like to thank Dr.Amit Bavisi and Mr.Aditya Makharia for their selfless friendship and immense help throughout my stay at Georgia Tech. The days that I have spent with them will always be memorable and irreplaceable in my life.

Finally, I would like to mention the people whose selfless love, blessings, inspiration, guidance and continuing sacrifices have defined my life; my parents Mrs. Shyamali Mukherjee and Mr. Prabir Mukherjee, my sister Jayoti, my brother Sanmoy, my sister-in-laws Papiya and Sanchita, my brother-in-law Rahul, my uncles and aunts, my loving nephew Sashwa, and my newborn and beautiful niece Rai. I would never forget the days when everybody in my family, in spite of all the hardships, would make sure that nothing impedes my studies and opportunities for a better career. I would also like to thank my in-laws Mrs. Kalpana Majumder and Dr. Paritosh Majumder for their love and immense faith in me, and letting me decide on my opportunities abroad, away from home. I derive great strength from the sacrifices of

these people. I would like to pay my tribute and respect to my uncle, Late Prasanta Mukherjee, whose love, inspiration and care was unparalleled. I carry all his memories and words to achieve all my goals in life. I also have received the care and affection of my beloved grandmother, without whose blessings, this effort would not have been successful. Also, a special thanks to the all the other members of the Mukherjee, Ganguly , Chatterjee and Majumder families for all the great times, fun, encouragement, appreciation, love and support. Lastly, but not the least, I would also like to thank my wife Mrs. Moumita Mukherjee, who deserves more praise than I can put down in words. As the best friend, she has loved me, encouraged me, inspired me, and believed in me for years before we got married. As a wife, she has spent more sleepless nights than myself, both at the lab and at home, helping me in everyday work, during the last days of my research. Her love and sacrifice are the some of the biggest gifts in my life.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

The objective of this research is the development of circuit sizing and statistical design-for-manufacturability methodologies for embedded, passive radio-frequency (RF) circuits.

With the revolutionary development in wireless communications technology, the need is continuously increasing for RF front-end modules that combine low cost, small size and high performance. At the same time, with the convergence of multiple wireless communications standards, the design constraints and manufacturing issues for RF modules are greater than ever. Two factors account for most of these difficulties. The first is the increased complexity of current cellular/wireless devices because of the increase in circuit functionality. Moreover, RF designers must deal simultaneously with multiple design constraints while also meeting several performance specifications across multiple frequency bands. Manual iterations in circuit solvers and field solvers are typically used in design flows to meet such design goals. These design iterations, however, can become computationally prohibitive. Consequently, time-efficient design closure is becoming increasingly difficult in the design of modern communications systems.

Secondly, system on package (SOP)-based technologies have emerged as strong candidates for the integration platform of next-generation, multi-functional communications devices [1], [2], [3]. Unlike a system on chip (SOC) in which the package exists solely for the thermal and mechanical protection of the ICs, SOP provides for an increase in the functionality of the integrated circuit (IC) package by supporting multiple dice and embedded passives. SOP can be viewed as a multichip module (MCM) [4], [5] that has more than one IC but has a better system-level perspective and hence is a more sophisticated packaging technique. A conceptual representation

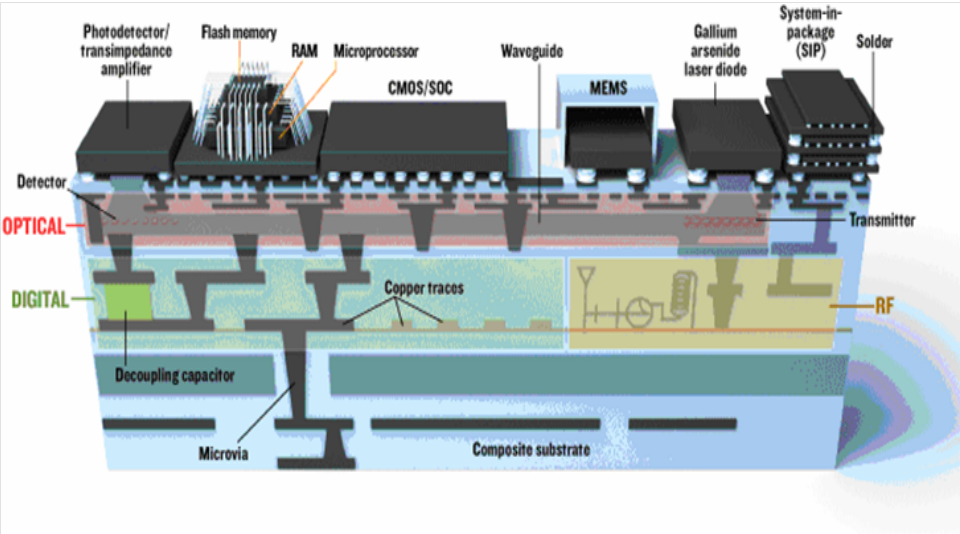

Figure 1. Illustration of an SOP test bed that combines: an optical circuitwith waveguide and detector just beneath the surface; RF thin-film components embedded within the package; and digital thin-film components at the bottom.

of a SOP test-bed is shown in Figure 1 [6].

However, the current design flow for the SOP-based systems is not as efficiently modularized into multiple levels of physical and logical abstraction as its SOC counterpart [7]. In addition, the new technologies have not been well-characterized because of the absence of adequate technological data. As a result, design optimization does not translate into manufacturing yield optimization.

The design of wireless components/modules, operating at very high frequencies and narrow bandwidths, is challenging [8], [9]. For example, high performance RF filters should exhibit low insertion loss, sharp roll-offs for filtering and channel selection, and preferably have low cost [10]. If RF circuit design is to be cost efficient, the design-cycle time must be reduced. The need for fast design closure for SOP-based RF circuits is best explained with the help of a flow chart, shown in Figure 2, of the stages in RF circuit design.

The flow is applied to the design of an RF bandpass filter with quasi-lumped embedded inductors and capacitors in multi-layer substrate. The layout of the filter (including probe-pads, signal vias and thruholes) is shown in Figure 3.

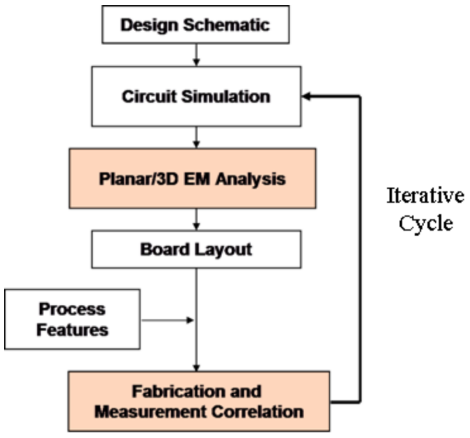

Figure 2. Typical design flow for RF circuits; grey represents time/memory bottleneck in the design flow.

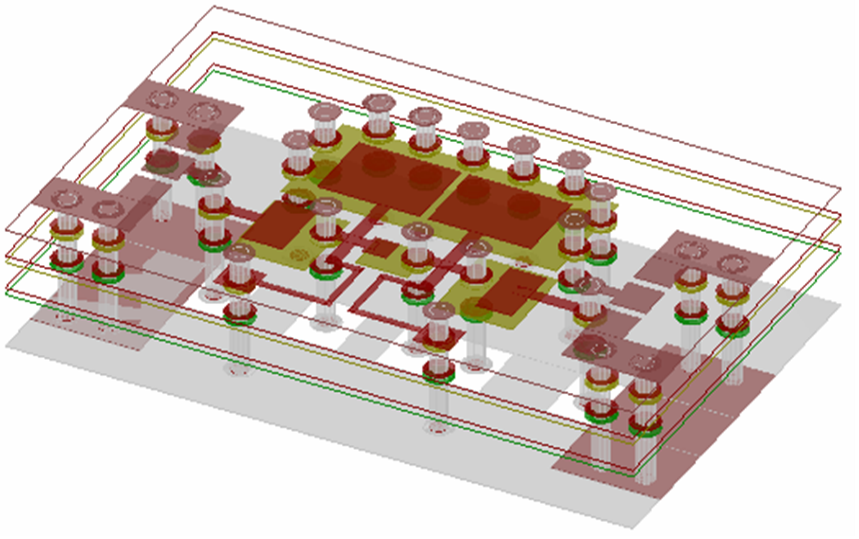

Figure 3. Layout of a bandpass filter in SONNET EM solver.

In Figure 2, the design flow begins with an ideal schematic in a circuit simulator. Design values derived from firsthand calculations are used to quickly arrive at rough estimates of the performance specifications. The optimized design values are then used to extract the layouts of the corresponding circuit components (Ls, Cs, Rs).

Typically, the layouts of the components are chosen from predesigned libraries. In many cases, the design values of the circuit components and library components are not exact matches. In such cases, the component with the closet value is chosen and its geometries are varied so that the required component specs are met. Full-wave electromagnetic (EM) solvers are typically used to tune layouts. EM solvers are computationally expensive but accurate. They capture the physical effects of layout, e.g. the parasitics and the EM coupling. However, multiple iterations are required to obtain the convergence necessary for accurate component values. Furthermore, when the layout components are connected via interconnects at a later stage of the design flow, these interconnects add to the inductance, resistance and parasitic capacitance of the overall circuit [9]. Consequently, the circuit response is modified and manual EM iterations are required again to restore the design specifications for the overall layout.

After fabrication of the design, measurements are performed to verify whether the specifications are met. For designs that deviate significantly from the specifications, the corresponding layouts are manually perturbed via EM simulations to meet the specifications. Clearly, as shown in Figure 2, the iterative cycle continues till the specifications are met and the design is ready to be delivered to the market. **In the absence of a robust computer-aided design(CAD) framework, the amount of manual intervention required for design tuning increases exponentially with design size, thereby increasing design cost and time.**

The limitations/challenges in this flow are as follows:

(a) EM simulations of complete layouts (which are time and memory intensive) are

a part of the iterative cycle instead of being a part of final verification.

(b) Design optimization does not ensure high volume manufacturability.

(c) Design flow lacks diagnosis. Diagnosis is the process of efficiently detecting and correcting faults in design (due to process variations). Commercial circuit simulator (e.g. Agilent's Advanced Design System (ADS) [11]) does circuit-level design of experiments (DOE) for statistical analysis, but it does not have diagnostic capability that can reduce the test time.

The statistical analyses of RF circuits that are solely based on circuit simulators provide fast but inaccurate results. The conventional method used to study the effect of component variations on system performance is to perform Monte Carlo (MC) analysis [12]. The MC analysis with full layout EM simulations is accurate but can be prohibitively time and/or memory-intensive.

1.1 The SOP paradigm for RF circuits

Developments in packaging technology have led to potentially cost-effective alternatives for systems integration, namely the system-on-package (SOP) approach [6],[13],[14]. A SOP module permits high levels of functional density by incorporating combinations of wirebond, flip-chip, stacked devices, embedded devices, MEMS, and package-on-package [15]. Moreover, SOP technology requires less power and generates less noise at the interconnect level, allows flexibility in mixing IC technologies, and reduction of board size and cost through inclusion of passive components [9]. Furthermore, compared with existing solutions based on SOC, SOP modules can be developed quicker.

From a designer's perspective, the use of SOP technology provides for design flexibility as well. For example, the noise figure of a low-noise amplifier is strongly dependent on the base/gate inductance of the active device [16]. On-chip solutions are

limited by the low quality factors (Qs) of the passives due to the high substrate losses [17], [18], [19]. In an SOP platform, the critical base inductance can be moved to the package, thereby increasing its Q, while the amplifier transistor can be integrated as a silicon die [16]. Therefore, a co-design approach can be achieved in an SOP design environment, thereby leading to better performance.

Despite the advantages, the use of embedded passive components for the design of RF circuits in SOP is considered bulky and risky. This can be attributed to the low tolerance for variations, the lower yield of the embedded components, and the increased cost of the substrate. The new SOP-based technologies are not yet optimized and well-characterized due to the absence of adequate technology data. Problematically, reference flows are lacking, concept feasibility is time-consuming and often inaccurate, and collaboration across the design chain is poor.

To improve time-to-market via design cycle reduction, SOP design has to move from an **expert methodology** to a **mainstream design methodology** - one that is **automated, integrated, reliable, and repeatable**.

For example, the return loss (S11) variations for a measured set of 50 samples of an embedded RF bandpass filter are shown in Figure 91. The bandpass filters were implemented using organic substrate with multi-layer LCP technology. The filter circuit was designed for a center frequency of 2.4 GHz,and 1 dB bandwidth of 100 MHz. From the figure, it can be seen that the narrow passband varies significantly in different samples due to manufacturing variations. Therefore, in volume manufacturing, it is critical to estimate and optimize the statistical metrics of the performance measures.

The aforementioned discussion summarizes the need for layout scaling techniques and statistical manufacturability analysis for fast design closure and high-volume manufacturability on emerging SOP-based packaging technologies. The focus of this dissertation is depicted by the shaded boxes in the Figure 5.

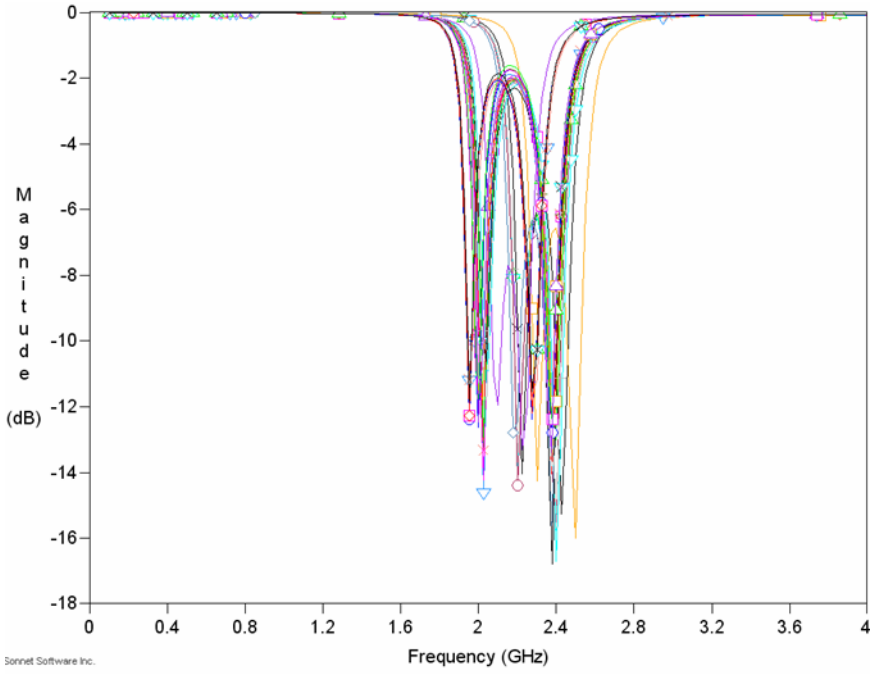

Figure 4. Return loss (S11) variations of an embedded RF bandpass filter.

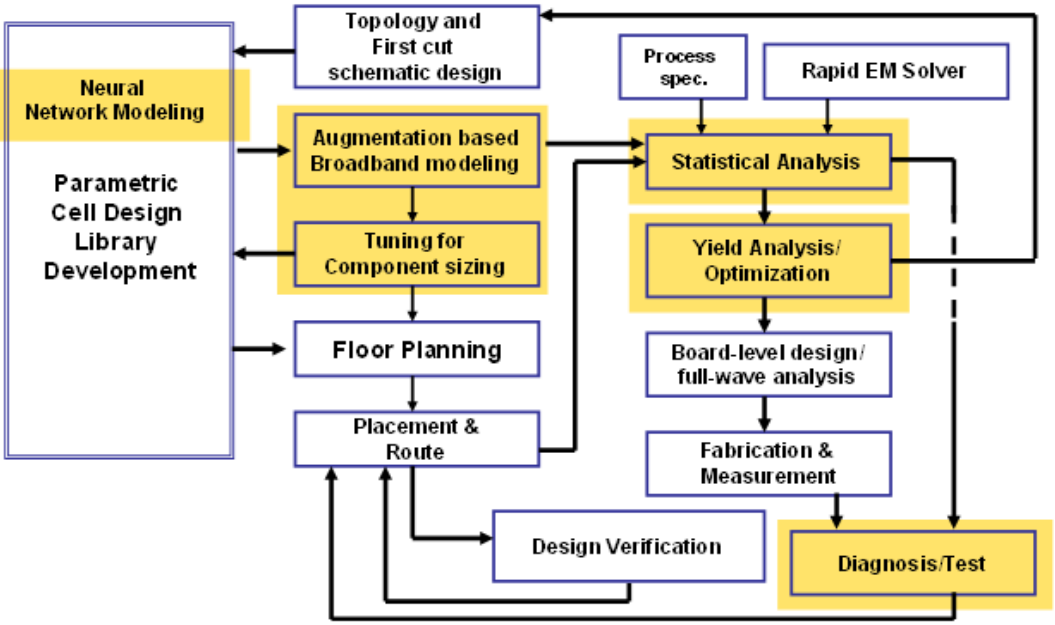

Figure 5. Design stages of an RF circuit; the focus areas of the dissertation have been shown by shaded boxes.

1.2 Need for Layout Scaling Methods in RF Design

Layout-level circuit scaling is the process of extracting network/layout-level parameters for a component/circuit from an existing set of different design specifications. It is common in digital designs and is being used increasingly in low-frequency analog circuits. Clearly, the key to fast design closure of digital ICs lies, partially, in the modular framework of the SoC CAD tools. A typical digital IC design flow proceeds from concept to cell-based logic design, cell-based logic synthesis, clock insertion, floorplanning, routing, design-for-manufacturability checking, design-rule checking and final tape-out [20]. Design changes in such a cell-based modular framework are time-efficient. The designer needs to specify the changes at a high/behavioral level of abstraction. The corresponding modifications in the low-level circuit blocks are realized through parameterized functional links between different design levels.

Current RF design tools, however, lack the capability of parametric cell approach implemented in a CAD framework. This can be attributed of the complexity of physical effects that needs to be considered while simulating a SOP-based RF module [9]. A few such critical parameters can be substrate coupling, near-field coupling, far-field coupling, component parasitics, large process tolerances and board warpage [9], [21]. Most of the aforementioned parameters are not encountered in silicon-based digital technologies, thereby facilitating a cell-based design flow.

The design emphasis of most wireless products is to provide the smallest form factor solution (hence, the cheapest solution) with the maximum functionality. SOP-based RF modules have emerged as a high-performance solution for designing multi-band wireless systems. Clearly, design cycle time must be reduced if cost-effective fabrication of RF modules on such technologies is to be achieved.

1.2.1 Simulation/optimization using circuit solvers

Standard circuit simulators use the description of a circuit in terms of lumped circuit elements and coupled (transmission) lines to account for distributed effects and/or

directly rely on S-parameter (or, equivalently Y or Z-parameter) descriptions of the different parts of the circuit. The circuit simulator approach, in general, relies on a divide-and-conquer technique in which the circuit is subdivided into separate parts for which models exist or can be calculated [22], [23], [24]. Kirchoff's current and/or voltage laws are then applied to obtain the overall circuit equations and solutions.

The advantages of the circuit simulator approach is clear; this approach is fast and, therefore, can be easily integrated with advanced network optimization techniques. However, for proper design of microwave, RF, and high-speed digital circuits, it is necessary to take into account the electromagnetic effects of the actual layout. When considering the more general class of microwave circuits, there is even less evidence of the need to distinguish between the circuit description and EM behavior because physical effects are often an integrated part of the desired circuit performance [25].

1.2.2 Simulation/optimization using EM solvers

Based on the reasoning in Section 1.2.1, more reliance on EM solvers for RF circuit design and optimization purposes would seem natural. This straightforward thought, however, has multiple disadvantages. Despite phenomenal progress in the development of field solvers and the availability of powerful computing systems, field solvers nevertheless continue to be slow in comparison with circuit solvers. This slowness is detrimental to their use for optimization, tuning, yield analysis, etc., which require a large number of circuit evaluations. Additionally, lumped-element values derived from EM analysis turn out to be quite sensitive to the parameters that control the EM simulation, in particular, the size of mesh cells [9]. For example, the layout of a second order bandpass filter with via pads and thruholes in SONNET is shown in Figure 3. To accurately capture the effects of the vias, the maximum size of the mesh cells can, at best, be a fraction of the via features. In case of uniform size of mesh cells in the layout, this can lead to a large number of mesh cells, and therefore, long simulation time.

EM solvers are based on different numerical approximation techniques for solving the Maxwell's equations to solve for fields, voltages and/or currents. Quite expectedly, such spatial/temporal discretization-based solution techniques are time and memory intensive. Unlike SoC design flows, SOP-based RF design involves significant amounts of EM simulations to analyze the physical effects of the layout. A full factorial MC analysis in a full-wave EM solver can, therefore, require impractical amounts of CPU time and memory resources for even simple structures.

In summary, the EM/circuit analysis and optimization tradeoff problem can be viewed as follows; EM field simulators offer highly accurate results, but this accuracy most often comes with high memory requirements and slow performance in terms of CPU time. On the other hand, conventional circuit simulators are fast and highly flexible but do not account for all the field effects, and their accuracy hinges strongly on the availability of models. **The question naturally arises as to how we can properly combine field analysis and circuit analysis in such a way that their respective advantages are optimally utilized in terms of reduced design cycle time in combination with acceptable performance and manufacturing yield.**

1.2.3 EM-circuit co-simulation

A wide array of literature exists on the combination of field and circuit analysis for optimization purposes [26], [27], [28]. An early contribution to the combination of field and circuit analysis can be found in [29]. Here, a time-domain simulator is based on a spatial network method (SNM). This work emphasizes on the inclusion on nonlinear elements but the focus is not design scaling of circuit layouts.

Optimization of silicon-based RF inductors based on geometric programming has been described by[30]. However, this method is limited by the use of analytical expressions for inductor parameters. This is because it is difficult to extract accurate, closed-form expressions for inductor parameters in multi-layer substrates. Mapping

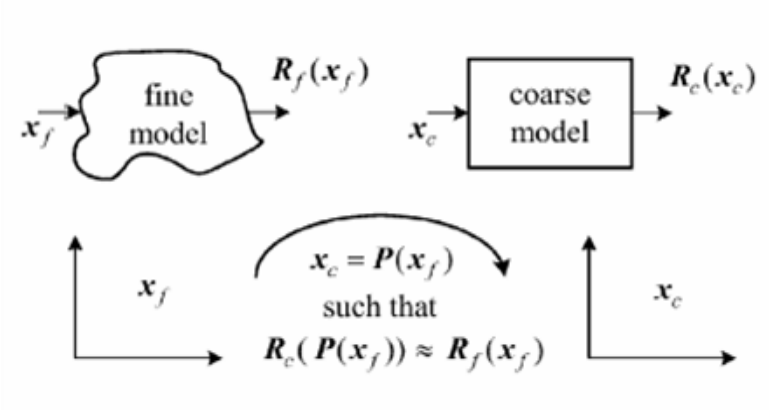

Figure 6. Illustration of the concept of space mapping.

of electrical parameters of inductors to layout parameters using polynomial functions have been shown in [31], [32]. The technique provides good interpolation for single or multiple parameter variations for weakly non-linear data. However, this method does not provide convergence to a unique solution in a multi-variable optimization environment.

Efficient EM optimization using space mapping (SM) is described in [33]. The SM-based algorithm is shown in Figure 6, where a linear mapping is developed between the parameter space of the coarse model and that of the fine model. The coarse model is obtained from extensive, circuit-based simulation data while the fine model is obtained from limited, time-consuming, but accurate EM simulation data. However, these methods are ideally suited for optimizing structures once it has been generated.

Artificial neural network (ANN) based modeling techniques have also been applied for the optimization of linear and nonlinear circuits [34], [35], [36]. Recent work has reported the application of ANN-based coarse models for design optimization of compact RF passive circuits on multi-layer substrates like low temperature co-fired ceramic (LTCC) technology [37], [38]. However, the focus of these works is on time-efficient layout optimization and not layout-level scaling.

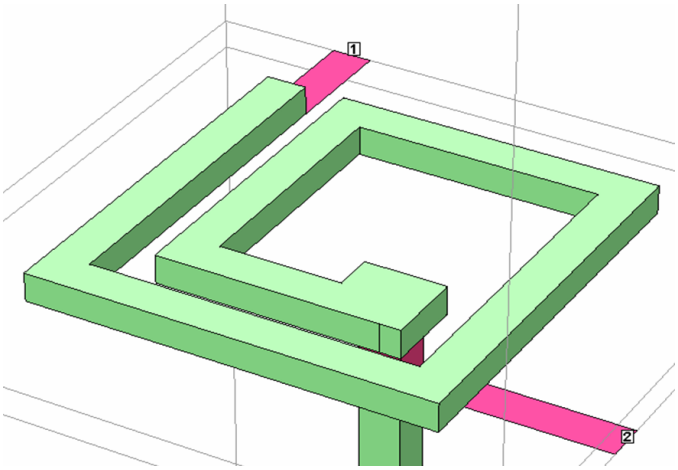

Figure 7. SONNET model of a spiral inductor in multi-layer substrate.

1.2.4 Circuit augmentation for broadband modeling and circuit tuning

As the RF system design complexity increases, it is imperative that the designer have access to accurate models for passive components and interconnects based on network analyzer measurement data or electromagnetic field solver results. Traditionally, an electrical model is created out of ideal circuit elements to fit the data [39].

Each element of the simple circuit model, if properly constructed, can represent meaningful electrical characteristics of the parameter being modeled. In other words, a "physics-based" model provides the designer with valuable insight into the object being modeled. However, this method has its set of disadvantages. It is very difficult and time-consuming to develop a physical model [40]; the task becomes increasingly difficult with frequency. Also, most of the physics-based modeling approaches provide "nominal" values for the model parameters, i.e. around the frequency where the model is extracted, and therefore, is unsuitable for accurate and broadband circuit-level optimization.

To illustrate the need for broadband modeling, a microstrip spiral inductor, shown in Figure 7, was simulated in SONNET EM solver. The values of the lumped circuit model parameters were extracted at a particular frequency. The circuit model for the inductor is shown in Figure 8. The difference in the frequency responses from

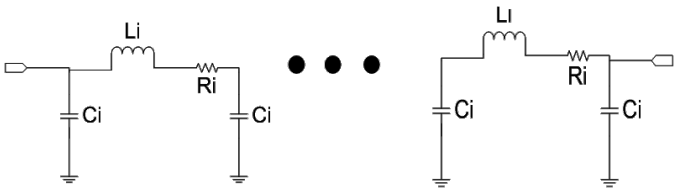

Figure 8. Multi-section lumped element model of a spiral inductor embedded in LCP substrate.

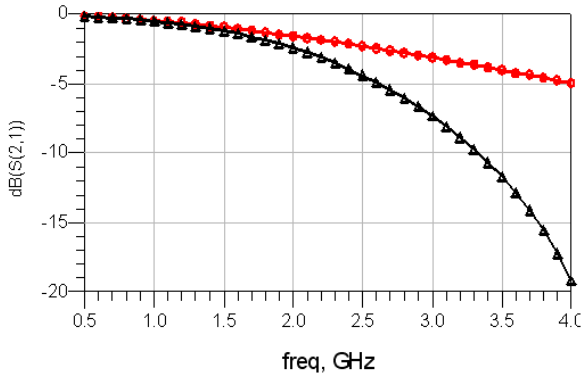

Figure 9. S-parameters from the EM model(black triangles) and the circuit model (red circles).

the EM simulation and that from the circuit model is shown in Figure 9. Clearly, the difference in the S-parameters needs to be minimized. Using ad-hoc modeling approaches, a large amount of trial and error may be required to find the location and value of the additional elements, rendering the procedure intractable for large ($n > 20$) number of components.

Over the last decade, there has been great interest in macromodeling techniques to fit frequency-domain data. The conceptual representation of the macromodeling approach is shown in Figure 10. The macromodeling technique aims to only match the terminal characteristics of the device. In common macromodeling approaches, the data is typically fit to a set of basis functions in the frequency domain [41], [42]. The methods vary as to how the locations of the basis functions are chosen and how their coefficients are determined. Usually, the methods implement some

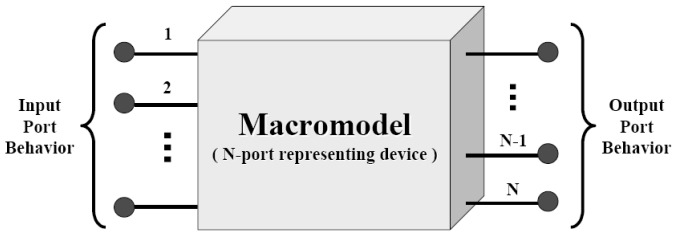

Figure 10. Black-box macromodel for an N-port device.

form of least-squares fitting of the coefficients of the data. From the perspective of broadband modeling for design optimization, these approaches have a number of disadvantages. Firstly, the non-physical nature of these models relegates the use of these approaches to applications that only require the terminal characteristics of the devices being modeled. In addition, the presence of controlled sources and non-physical values of passives in the macromodeled data cannot be utilized to correlate the model parameters with the layout parameters. Also, there are a number of constraints these "black-box" models must satisfy: passivity, stability and causality. Of these, passivity is most difficult to guarantee [43], [44], [45].

Clearly, it is necessary to develop an algorithm that can retain the physical nature of the circuit model while providing some augmenting network to minimize the error at higher frequencies. The algorithm in [46] considers such an approach where the circuit model is augmented with a black-box (or purely mathematical) model so as to match the y-parameters of the circuit model with the given measured parameters. It is based on finding a modified network by curve-fitting the difference between the measured parameters and that of an initial circuit model. One of the drawbacks of this approach is that the augmented network is restricted in its placement, only to the terminals of the circuit model. From the perspective of high-frequency/broadband matching, this may not necessarily be the optimum solution. Also, as with any black-box type model, it can become a challenge to ensure passivity. A modification of this approach has been proposed in [47]. However, this approach stills requires the use of

synthesis methods, such as vector-fitting, or other network generation techniques to develop SPICE-equivalent circuits for the augmented elements from their impedance profiles.

Therefore, an automated broadband circuit modeling technique without the drawbacks of "macromodeling" approaches is critical to the development of an efficient SOP-based RF CAD framework.

1.3 Need for DFM (Design-for-Manufacturability) methods in RF design

During manufacturing, process variations will inevitably cause design parameters, such as component values, to waver from their nominal values. As a result, the manufactured circuits may no longer meet some performance specifications, such the group delay, gain and bandwidth (in case of a filter, for e.g.), that it was designed to satisfy.

The procedure of design-for-manufacturability (DFM) attempts to select the nominal values of design parameters so as to ensure that the behavior of the circuit remains within specifications, with the greatest probability. In other words, the aim of design centering is to ensure that the manufacturing yield is maximized. This problem has been extensively researched in the domain of digital IC technology. For IC design flows, successful design verification translates to optimum design yield. This can be attributed to the presence of a mature design and manufacturing infrastructure for digital IC/SOC manufacturers. **The IC design infrastructure consists of predictive device models, complete digital CMOS characterization, statistical and scalable compact models that are hardware-verified, and a robust, parametric, and hierarchical design automation environment** [48],[49].

Previous approaches to solving the design centering problem have traditionally taken two routes:

1.3.1 The statistical approach

In electrical engineering, the drive for high yield and high performance have prompted researchers to develop many statistical methodologies. These studies were predominantly aimed for chip or component level yield estimation, and statistical circuit optimization. Although relevant contributions will be referred in the subsequent sections, it is suitable to categorize this effort into three main areas. In this section worst-case, Monte Carlo, and design of experiments (DOE) principles are discussed. Almost all statistical methods can be considered as improvements upon the combinations of these principles.

1.3.1.1 Worst case Analysis

The classical approach to account for process and functional uncertainties in a circuit/module is the worst-case analysis. After the worst-case combinations of the design parameters are verified, all products are expected to meet the specifications [50]. However, this conservative design approach has major limitations [51]. First, it requires an initial guess of the worst-case scenario. Full factorial simulations to find the worst-case point is inefficient. Furthermore, with a large number of performance measures, finding the worst-case parameter combination for each performance measure becomes very difficult. Also, the worst-case combination, where all design parameters are at their extremes, has very low probability of occurrence. Therefore, designs that are based on the worst-case analysis may underestimate the performance and increase the design effort.

1.3.1.2 Monte Carlo Analysis

The most prevalent methodology in the manufacturing community to estimate the parametric yield of a design is the Monte Carlo (MC) analysis [12]. This technique depends on simulating a large number of design parameter combinations for generating the performance statistics. The values of the design parameters are generated from random variables with associated probability distributions and correlations. Then,

the yield is approximated as the ratio of the number of acceptable instances to the total number of Monte Carlo runs. This can be mathematically formulated as

$$Y = \int_{-\infty}^{\infty} z(x) f(x) dx, \tag{1}$$

where $z(x)$=1 if all design values (x) satisfy the specifications, and $z(x)$=0 otherwise. In Equation 1, $f(x)$ is the joint probability density function of design parameters. Then the yield can be estimated as:

$$\hat{Y} = \frac{1}{N} \sum_{i=1}^{N} z(x_i), \tag{2}$$

and

$$\hat{Y} = \frac{1}{N} \sum_{i=1}^{N} z(x_i) \frac{f(x_i)}{h(x_i)}, \tag{3}$$

Depending on the complexity of the simulation model, and the number of process and operational variables, the "simulation space" of the the Monte Carlo method may become prohibitively large. This has led to the development of different sampling methods in the field of statistical analysis to optimize the error without exponentially increasing the number of simulations [52], [53], [54], [55]. An excellent survey of these sampling algorithms is provided in [56].

MC being a brute force method, is advantageous when the statistical parameter distributions and correlations between them are too complicated to represent as analytic functions [57]. This is the case in IC manufacturing, where the prime circuit parameters are highly correlated[58]. However, such simulations based on random parameter variations cannot reveal the methods for increasing yield. This dissertation focuses on optimizing the a set of design parameters and the yield for embedded RF passive circuits. Since the process parameters have been shown to be independent [56], more systematic design of experiment principles are used for the statistical analysis.

1.3.1.3 Design of experiments

Design of experiments method is a sequence of tests, where input parameters are varied in a planned manner [57], [59].

Using DOE, the circuit performance can be represented as empirical functions of the design parameters. To obtain the empirical functions, a series of planned experiments (simulations) can be performed with different levels of the input design parameters. Then, Monte Carlo instances can be applied to these surrogate functions to generate the performance statistics [54], [60].

In summary, DOE principles have emerged as a powerful alternative to worst case analysis and MC Analysis. Hence, the statistical analysis for embedded RF circuits are based on planned DOE arrays without resorting to MC type of simulations.

1.3.2 The geometrical approach

The procedure of design centering attempts to select the nominal values of design parameters so as to ensure, with the greatest probability, that the behavior of a manufactured circuit remains within the desired specifications. In this regards, the geometric approach aims at approximating the feasible region (where the specifications are satisfied) with the largest inscribed geometrical hypershape. The dimensions of the hypershape determines the nominal values of the design parameters. For example, the feasible region in the space of design parameters, can be approximated by a known geometrical body, such as a polytope or an ellipsoid. The center of this body is then approximated, and is taken to be the design center. Such approaches frequently assume that the feasible region is convex and bounded. For example, the ellipsoidal approximation of feasible design constraint region has been illustrated in Figure 11.

These methods commonly suffer from the following drawbacks:

(a) Limitations associated with the types of geometric bodies that are typically

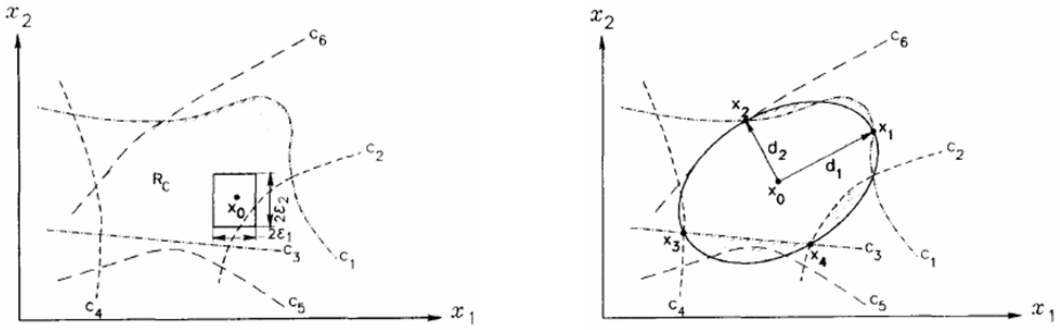

Figure 11. Ellipsoidal approximation of feasible design constraint region.

used to approximate the feasible region:

- In the case of ellipsoidal approximation as in [61], [62], certain nonsymmetric convex bodies cannot be approximated accurately. This is because an ellipsoid is symmetric about any hyperplane passing through its center, and is inherently incapable of producing a good approximation to a body that has a less symmetric structure.
- A polytope can provide a better approximation to a convex body than an ellipsoid, regardless of its symmetry. However, finding the center of a polytope is computationally complex [63], [64] and cannot be carried out in a reasonable time.

The simplicial approximation algorithm [65] attempts to inscribe the largest hypersphere in the polytope, and takes its center as the design center. However, as pointed out in [65] itself, in the case of elongated bodies, such as a rectangle with a highly skewed aspect ratio, it would be more appropriate to inscribe a ellipsoid rather than a hypersphere [65]. In any case, the simplicial approximation procedure essentially amounts to approximating the feasible region by a polytope, and then approximating the polytope by a hypersphere or ellipsoid. Hence, it suffers from the drawbacks of ellipsoidal approximation listed above.

(b) As pointed out above, the methods in [63],[65] essentially approximate the feasible region by means of an ellipsoid, and take the center of that ellipsoid to be the design center, *regardless* of the probability distributions that define the variations in the design parameters.

(c) Real feasible regions are seldom convex. While in many cases, they are "nearly convex", there are documented cases where the feasible region is not very well-behaved [66], [67],[68], leading to nonrealistic and poor yield numbers [69], [70].

1.3.3 Other conventional methods

Studies based on parametric sampling have been shown in [71]. This method permits the incorporation of realistic manufacturing constraints such as tuning, correlation, and end-of-life specifications. In this methodology, a database containing the results of a few hundred network analyses is first constructed. However, the method is limited by its initial requirement of this large database, which can be computationally prohibitive for RF designs on *emerging* technologies. Further, generation of large datasets of electromagnetic data (crucial for analysis of complex RF designs) can be time and memory-intensive, thereby relegating the use of this methodology to final verification.

Parasitic-aware, post-optimization design centering for RF integrated circuits based on simulated annealing (SA)[72] reduces iterations in design optimization. However, this work does not focus on diagnosis. In addition, SA has the limitation of local minima traps and numerous iterations are required to find a set of acceptable solutions.

Clearly, the focus of most of the prior work has been design centering using circuit parameters and not *layout-level* statistical analysis and diagnosis of RF designs.

1.4 Emerging technologies for SOP applications

Multi-layer packaging technologies have emerged as high performance alternatives to conventional substrate and surface-mount technologies for system integration of future multi-band wireless systems. **A step towards reducing design cycle time and improving design yields on such technologies would require efficient algorithms for the circuit scaling, diagnosis and yield optimization of embedded RF passive and active modules/components.**

In this dissertation, the researched layout sizing and DFM methodologies are validated on passive RF circuits with embedded inductors and capacitors in LCP dielectric material which is a laminate type, low-temperature, large-area and organic process. It should be noted, however, that the proposed methodology is generic to any mainstream packaging/manufacturing technology (capable of batch manufacturing RF circuits). LCP has been used in this work due to its excellent characteristics in terms of (a) circuit performance and (b) packaging cost/reliability, the two key requirements for cost-effective, high-performance SOP applications.

1.4.1 LCP-based organic substrate

In the recent past, laminate type organic processes have demonstrated LC passives with high Qs ($30 \sim 300$) that remain constant over a broad range of frequencies [9], [10]. High performance RF modules have been designed by selectively embedding high Q passives in the organic substrate, while using IC technologies for the design of active devices and biasing circuitry. In this thesis, LCP-based dielectric substrate has been used to validate the proposed layout scaling and DFM methodologies. LCP is a low-loss ($tan\delta = 0.002$), low temperature ($< 200°C$), laminate type organic thermoplastic that is compatible with PWB infrastructure. The advantages of using LCP substrate for radio frequency (RF) functionalities are as follows:

(1) The process technology allows the integration of high Q (100), high-density

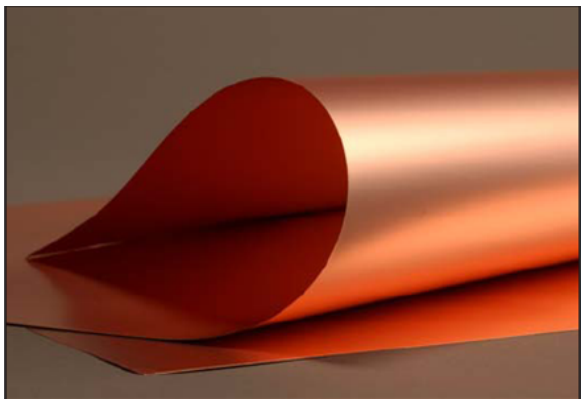

Figure 12. Copper cladded flexible sheet of LCP material.

lumped and distributed passive components [9].

(2) The material has low loss tangent ($tan\delta = 0.02$), enabling the design of passives with high quality factors [10].

(3) The quality factor of the passives can be scaled over a bandwidth of DC to 100 GHz thereby enabling broadband, low loss module designs [42], [45].

(4) LCP provides for large volume manufacturability, leading to low cost per component. This can be attributed to the large-area processing capability of LCP-based substrate panels (can be as large as 18 in X 24 in) [1], [73].

(5) In the absence of supporting package layers, LCP material, inherently, is a flexible material, making it ideally suited for conformal and/or flex circuit applications [74], [2].

(6) The organo-polymeric composition of the LCP material makes it suitable for low-temperature processing. In particular, the temperature cyles of LCP-based processing is compatible with printed wiring board (PWB) infrastructure.

(7) LCP has low coefficient of thermal expansion (CTE) that can be engineered to match metals or semiconductors.

1.5 Completed Research

The objective of this dissertation is the development of accurate and efficient methods for automated layout-level sizing/tuning, statistical modeling for parametric yield optimization, and layout-level diagnosis of RF passive circuits. Different methodologies have been developed to size RF circuits at the layout level without resorting to exhaustive iterations of EM simulations. A broadband modeling technique, and nonlinear mapping based on artificial neural networks (ANNs) for the generation of passive libraries have been demonstrated. In addition, a multi-domain design-for-manufacturability for embedded RF passive circuits have been developed. Broadly, the DFM methodology is based on design of experiments, statistical circuit modeling, parametric yield optimization and probabilistic diagnosis techniques. The methodologies have been correlated and verified with full-wave EM simulations and measurement results.

The following research has been completed in this dissertation:

(a) **Circuit augmentation for broadband modeling and tuning**

A circuit augmentation technique for broadband modeling of component libraries, consisting of embedded passive circuits has been demonstrated. The circuit augmentation technique is based on a previously developed circuit partitioning technique, a modified nodal analysis formulation and a linear optimization framework. The augmentation technique has been verified for broadband modeling of spiral inductors and planar capacitors.

(b) **Library development of RF components:**

A layout-level library developement technique for embedded inductors/capacitors in multi-layer substrate has been proposed. The methodology employs artificial neural networks to develop a neuro-model for the embedded passives. In addition, an adaptive sampling algorithm is implemented to reduce the size of

design library that is required for neural network training and validation. The results from the proposed methodology have been validated on measured and simulated frequency response data.

(c) **Layout-level scaling of RF circuits:**

A layout-level circuit scaling technique for RF passive circuits with quasi-lumped embedded inductors and capacitors has been proposed. The proposed approach is based on a combination of layout segmentation, augmentation, broadband lumped circuit modeling, nonlinear mapping, artificial neural network (ANN)-based methods, and circuit-level optimization. The methodology has been validated on measured and simulated frequency response data of RF bandpass filters. The circuit augmentation technique has also been applied for the tuning of bandpass filters. Comparisons have been performed with tuning using commercial circuit simulators, employing nonlinear optimization, to demonstrate the advantages of the proposed technique, that is based on a linear optimization framework.

(d) **A scaling-based approach for fault diagnosis:**

An extension of the circuit sizing technique to layout-level diagnosis of prototype circuits has been proposed. The fabricated designs require diagnosis of variations in performance metrics such as center frequency, bandwidth and transmission zeros that occurs due to process variations. The design scaling methodology was applied to map the variations in electrical parameters to component geometries. The results predict the possible variations in physical parameters that have been confirmed with measurements of the fabricated devices.

(e) **DFM methodology for RF passive circuits**

This dissertation presents a layout-level, multi-domain DFM methodology and yield optimization technique for embedded RF circuits for SOP-based wireless

applications. The passive portion of RF circuits is composed of quasi-lumped embedded inductors and capacitors in low loss, multi-layer substrate. The proposed methodology consists of stochastic circuit/EM modeling, layout-level statistical diagnosis and parametric yield optimization.

The proposed statistical diagnosis technique is based on layout segmentation, lumped element modeling, sensitivity analysis and extraction of probability density function using convolution methods. The statistical analysis takes into account the effect of the thermo-mechanical stress/warpage effects and the process variations that are incurred in batch fabrication. Yield enhancement methods based on joint probability distribution and constraint-based convex programming have also been presented. The results show good correlation with measurement and EM simulation data.

1.6 Dissertation Outline

The focus areas of this dissertation, in the perspective of an "yield-aware" efficient RF CAD framework has been shown in Figure 5. The rest of the dissertation is organized as follows. In Chapter 2, a circuit augmentation technique for broadband modeling of design libraries has been presented. Layout-level circuit sizing techniques for RF passive components and circuits with quasi-lumped embedded inductors and capacitors have been presented in Chapter 3. The augmentation methodology is extended to develop layout-level component sizing/tuning based on a linear optimization scheme. A multi-domain statistical analysis methodology to develop a stochastic DFM framework has been presented in Chapter 4. In Chapter 5, the DFM methodology with constraint-based yield optimization have been detailed. Finally, the conclusions and the scope of future work have been discussed in Chapter 6.

CHAPTER 2

BROADBAND MODEL DEVELOPMENT FOR EMBEDDED RF PASSIVES

As the design complexity of the RF system enhances, it is imperative that the designer have access to accurate models for passive components and interconnects based on network analyzer measurement data or EM simulations. As explained in Chapter 1, simplistic lumped element models matches measurement/EM data only across a narrow band of frequencies. Therefore, design optimizations depends on multiple iterations of EM simulations, as the simplistic circuit models do not take into account, the effect of parasitics and EM coupling. Fast design closure, therefore, is difficult to meet. The focus of this chapter, as shown in Figure 13 is the efficient and automatic generation of broadband models to aid in the development of passive models for component library development and circuit-level design scaling methodologies.

Current RF design flows undergo extensive manual interventions and multiple iterations of EM/circuit simulations to meet the design specifications. Such a design approach will satisfy realistic time-lines for small designs (for example, less than 10 passive components). **However, with the advent of multi-band architectures, manual RF front-end design is getting time-consuming, emphasizing the need for an automated CAD framework for broadband model generation, parameterized library development, and "performance-aware" layout optimization.** The reasons for such requirements for the CAD framework has been explained as follows.

Firstly, for example, the current approach to optimize an RF layout is to perform multiple EM simulations with multiple incremental modifications in the physical parameters to meet the specifications. Each of these simulations is expensive, both in time and memory. Furthermore, the designer cannot rely on simplistic circuit models

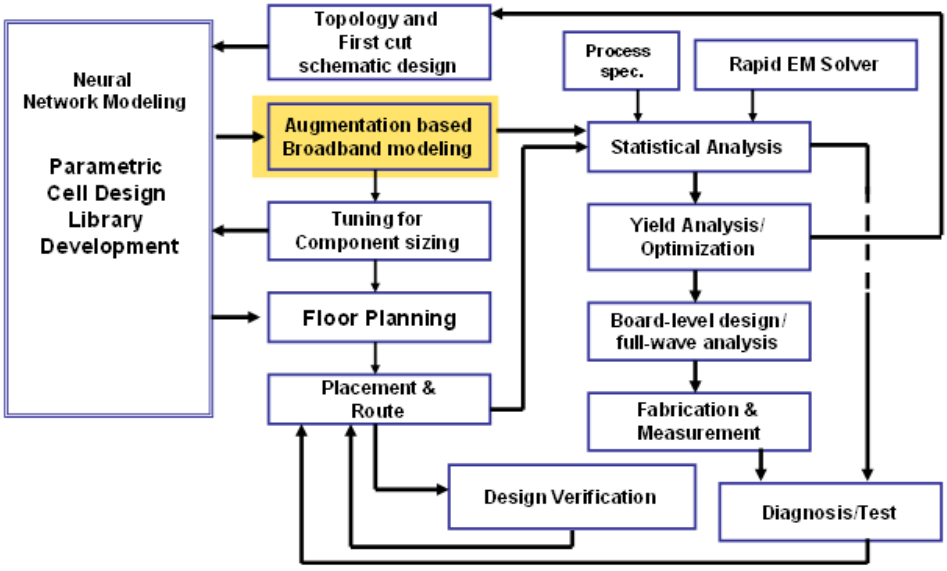

Figure 13. RF Design flow; the shaded box represents the focus of this chapter.

on this purpose, the former being inherently narrow-band in nature. Clearly, there is a need for a modeling technique that should meet two objectives:

(a) Broad-band accuracy of circuit-based models for parametric library development

(b) Optimization at user-defined frequencies for circuit-based component tuning

Secondly, the designer needs to tune the physical parameters of the individual passive components so that the S/Y/Z parameters of the components meet the specifications at the design frequencies. A hit-and-trial approach to this problem can lead to prohibitively large time for multi-band designs (for example, with more than 25 components). A parametric design library can help extract the layout parameters based on the S/Y/Z parameters of the components.

Thirdly, when a designer connects multiple Rs, Ls and Cs to form an entire layout, substantial deviation is seen in the response from the design specifications. This is due to the additional inductance and parasitic capacitance of the transmission lines used to connect the circuit components. Unlike the broadband modeling requirement

TECHNIQUE	Advantages	Disadvantages
Passive Macromodeling	Generic black box modeling	▪ Controlled sources not suitable for passive design optimization ▪ Passivity enforcement
Parametric EM Optimization	Full-wave analysis Accurate	Time/memory intensive
Vector Fitting	Efficient formulation	Model order not suitable for scalable layout synthesis
Genetic Algorithm	Efficient global optimization	Non-intuitive solution for design structures
This work	Broadband circuit modeling and component tuning	Current formulation suitable upto 10 GHz

Figure 14. Comparison with recent approaches to broad-band curve-fitting and parameterization.

for library development, the layout of the complete circuit needs to meet specifications, only at certain discrete and/or narrow band(s) of frequencies. An efficient, circuit-based tuning technique to optimize the response of the design at the desired frequencies will lead to fast design closure, prior to final EM simulation(s) for the purpose of verification. This chapter focusses on the development of circuit augmentation techniques for broadband modeling required for component library development and layout-lvele circuit scaling and sizing.

An efficient and automated algorithm has been presented in this chapter to identify an augmenting equivalent circuit for improving the accuracy of the simple circuit model at higher frequencies. Unlike the work presented in [47], this algorithm is not restricted in its placement of new circuit elements at the ports of the circuit model. On the other hand, it is possible to identify and insert frequency-dependent elements of both types, series and shunt, at any arbitrary location in the circuit model, based on the requirements of the data being modeled. To match the model's response to a measured set of y-parameters, a linear least-squares formulation was used to extract the values of the augmented elements. The algorithm, presented in this work does

not resort to nonlinear optimization. In addition, different augmentation elements that are tested for convergence with the EM/measurement data are chosen from a pre-designed SPICE circuit library. This is different from the approach presented in [47], where SPICE-equivalent circuits were synthesized from the frequency-dependent impedance profiles of the augmented elements. Therefore, in this work, passivity and causality check on the final circuit model is not required. The method is very fast as the optimum circuit elements are chosen using a linear least-squares optimization technique.

2.1 Experiment with BEMP macromodeling

The objective in this part of the dissertation is to develop a circuit model that captures the difference between the simple lumped circuit model and the measurement data over a wide frequency range. A straightforward approach is to use the macromdeling methodology to find the rational function approximations (which can be converted to SPICE-compatible netlists) of the augmented elements so that the overall model matches the measurement data. Mathematically, this problem can be formulated (with reference to Figure 16) as follows:

Some of the possible types of connections to the augmented network have been shown in Figure 15. To keep the test-case simple in topology, a parallel-only augmentation was chosen. To extract the difference in the Y-parameters (i.e. EM and circuit model), a macromodeling technique has been applied to the test case in this section, and the vector-fitting methodology in the following section. Let us consider the circuit model (CM) in Figure 16, and let an augmented model (AM) be connected in parallel, as shown in the figure.

The goal is to find the network representation of the AM such that the overall circuit in Figure 16 accurately matches the EM/measurement data. Mathematically,

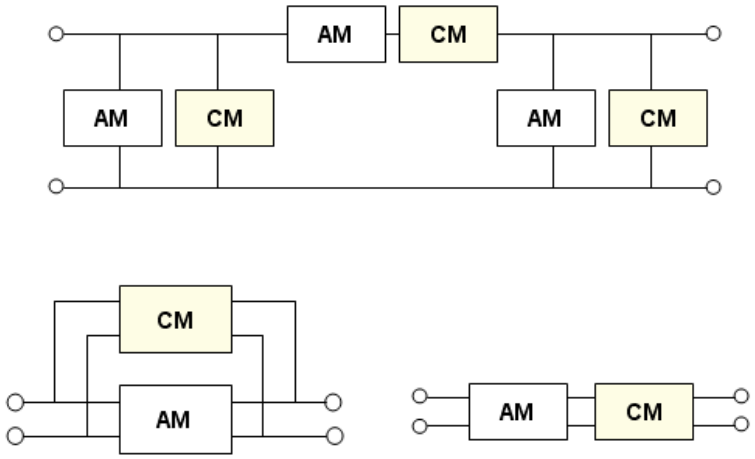

Figure 15. Different topologies for circuit augmentation.

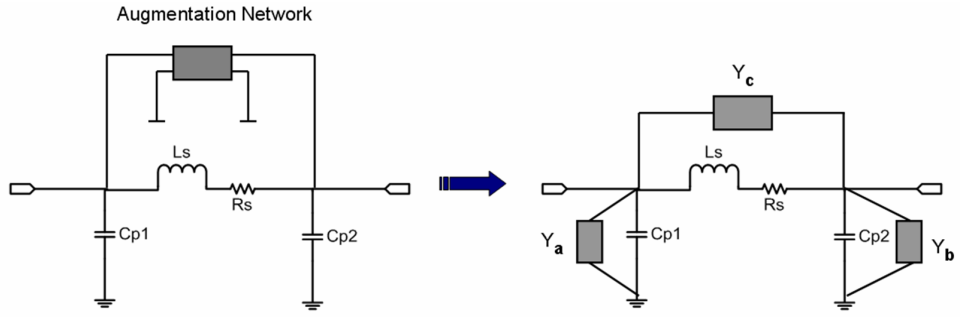

Figure 16. Shunt augmentation and its equivalent Π-model connection.

for the shunt topology, it is known that, for a particular frequency ω_n,

$$Y^{model}(\omega_n) + Y^{aug}(\omega_n) = Y^{meas}(\omega_n). \tag{4}$$

In addition, from the theory of network analysis, it is known that Y^{aug} can be represented as a Π-model shown in Figure 16. The corresponding Y-parameters of the Π-model is related to the Y^{aug} as shown

$$Y^{aug}(\omega_n) = \begin{bmatrix} Y_a(\omega_n) + Y_c(\omega_n) & -Y_c(\omega_n) \\ -Y_c(\omega_n) & Y_b(\omega_n) + Y_c(\omega_n) \end{bmatrix}. \tag{5}$$

Equation 4 can, therefore, be rewritten as

$$\begin{bmatrix} Y_{11}^{mod} & Y_{12}^{mod} \\ Y_{21}^{mod} & Y_{22}^{mod} \end{bmatrix}_{\omega_k} + \begin{bmatrix} Y_a + Y_c & -Y_c \\ -Y_c & Y_b + Y_c \end{bmatrix}_{\omega_k} = \begin{bmatrix} Y_{11}^{meas} & Y_{12}^{meas} \\ Y_{21}^{meas} & Y_{22}^{meas} \end{bmatrix}_{\omega_k}. \tag{6}$$

Here the relation has been shown for a discrete frequency point ω_k. The same relation holds at other frequencies as well. Equating (6), element-by-element, it can be shown that Y_a, Y_b, and Y_c can be solved, for each frequency point ω_k, as

$$Y_a(\omega_n) = [Y_{11}^{meas}(\omega_n) - Y_{11}^{mod}(\omega_n)] \quad + \quad [Y_{12}^{meas}(\omega_n) - Y_{12}^{mod}(\omega_n)], \tag{7}$$

$$Y_b(\omega_n) = [Y_{22}^{meas}(\omega_n) - Y_{22}^{mod}(\omega_n)] \quad + \quad [Y_{12}^{meas}(\omega_n) - Y_{12}^{mod}(\omega_n)], \tag{8}$$

$$Y_c(\omega_n) = [Y_{12}^{mod}(\omega_n) - Y_{12}^{meas}(\omega_n)]. \tag{9}$$

An efficient, broadband macromodeling tool BEMP [43] that was developed at Georgia Tech was used to macromodel the difference between the Y-parameters of the EM data and the model data, for the inductor test-case shown in Figure 17. The results of the macromodeling has been shown in Figure 18. A part of the synthesized SPICE netlist that accurately macromodels the difference between the EM data and the circuit data has been shown in Figure 19. It can be seen in Figure 19, that the total number of circuit elements is 82, that includes 52 RLGC-type elements, 20 controlled sources and 10 dummy elements. The initial, lumped-element, physical model, therefore, degenerates to a non-physical macromodel. Such a macromodel is not suitable

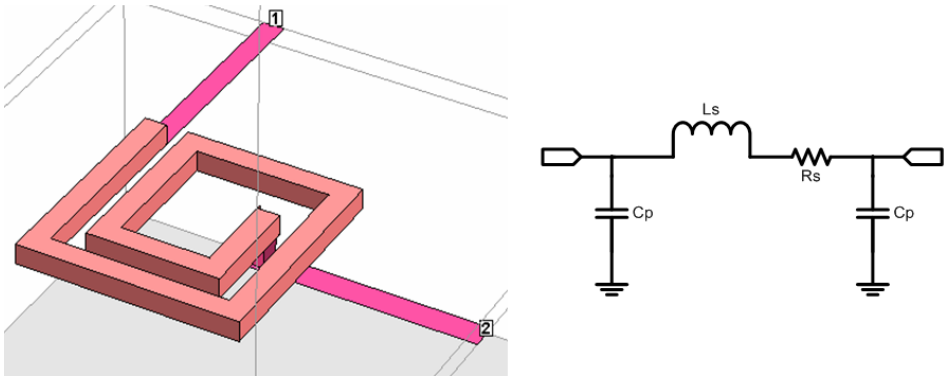

Figure 17. (Left):Layout of a spiral inductor in SONNET; (Right): Two-port lumped element model for the inductor.

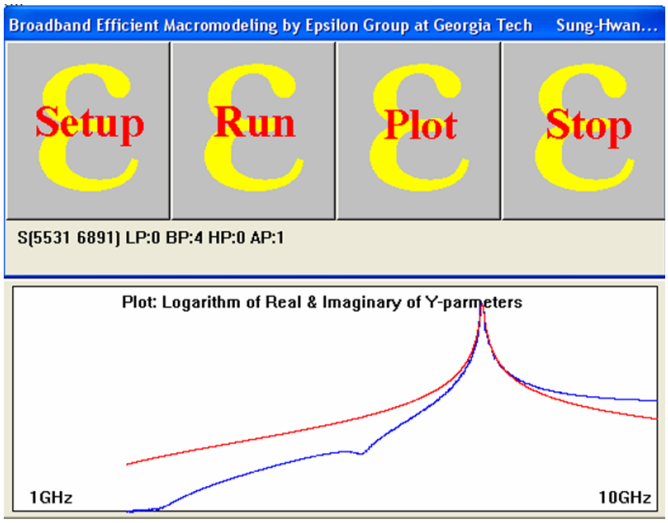

Figure 18. Results obtained from the BEMP macromodeling tool.

Figure 19. A portion of the SPICE netlist, generated by the BEMP macromodeling tool.

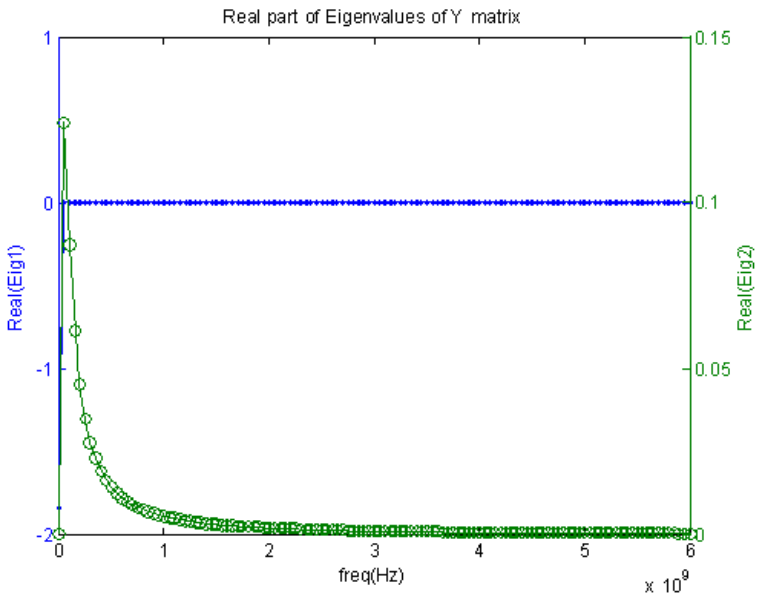

Figure 20. Real portion of the eigenvalues of the augmentation matrix.

for circuit-based component sizing. In addition, such a "black-box" approach has to deal with the problem of passivity. Passivity is one of the most difficult conditions to enforce, as its definition translates into complicated mathematical operations. By definition, a passive network cannot generate more energy than it absorbs, and thus, will be stable regardless of its terminations. In contrast, a stable but non-passive network may become unstable given particular terminations [41]. Using Y (or other immittance) parameters, a network is *passive* at a specific frequency $s = j\omega$ if [43]

$$eig\left(\frac{Y(s) + Y^H(s)}{2}\right) \geq 0, \tag{10}$$

where Y^H is the hermitian of Y. To illustrate the passivity problem, the eigenvalues of the macromodeled Y-parameters have been shown in Figure 20. For 2×2 matrices, passivity is guaranteed if $Re(eigenvalues) \geq 0$, where Re represents the real part. For the test-case in Figure 20, the violation of passivity around 50 MHz can be emphasized in Figure 21.

Therefore, an augmentation approach with purely physical components, will automatically guarantee passivity, with some possible tradeoff in accuracy. In addition,

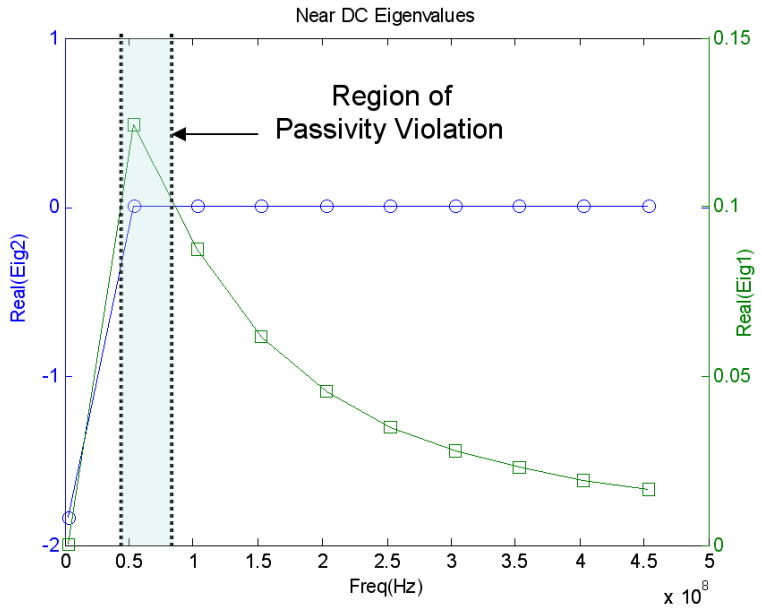

Figure 21. Violation of passivity (due to the positive eigenvalues) at near-DC frequencies, by the augmentation network.

stability and causality will also be satisfied with passive elements.

2.2 Experiment with vector fitting

Vector fitting is a powerful methodology for the fitting of measured or calculated frequency domain parameters [75]. The technique consists of replacing a set of starting poles with an improved set of poles via a scaling procedure [75]. To provide with a brief overview of the vector fitting technique, consider the rational function approximation

$$f(s) \approx \sum_{n=1}^{N} \frac{c_n}{s - a_n} + d + sh, \tag{11}$$

where the residues c_n, and the poles a_n are either real quantities or come in complex conjugate pairs, while d and h are real numbers. The underlying problem is to estimate all the coefficients in Equation 11 so that a least-squares estimation of $f(s)$ is obtained over a given frequency interval. It is to be noted that Equation 11 is a *nonlinear* equation in terms of the unknowns, because the unknowns a_n appear in the denominator. Vector fitting solves the problem in 11 sequentially, as a *linear*

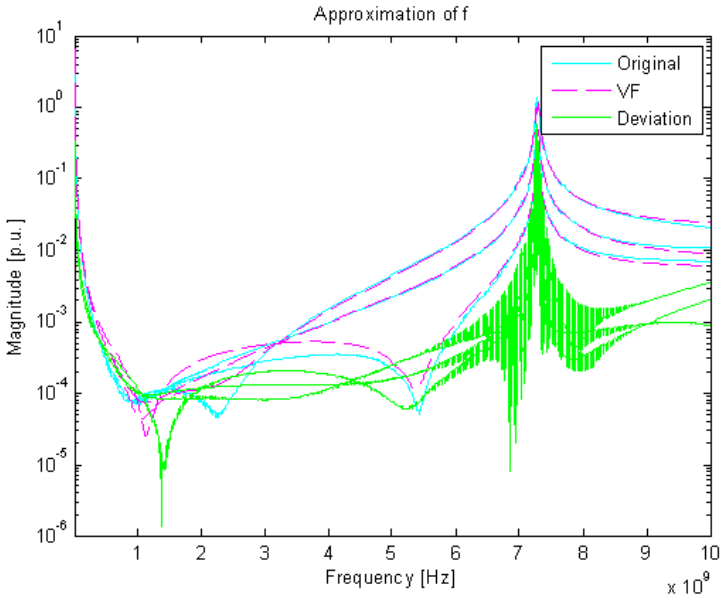

Figure 22. Magnitude correlation for Y_a, Y_b, and Y_c, between the difference of circuit-EM parameters, and that obtained from vector fitting (model order = 6).

problem in two stages, both times with known poles. The details of the pole and residue identification methodology have been detailed in Appendix C.

Vector-fitting technique was applied to each of Y_a, Y_b and Y_c, for the test case, discussed in the previous section. The purpose, as explained before, is to efficiently develop rational function approximation (and hence SPICE-equivalent circuits) for the augmented elements represent by the Π-network. The vector-fitting application is available as a free software [76]. The source code was appropriately modified and used in this work. The results (both magnitude and phase) of vector fitting for Y_a, Y_b and Y_c for different model orders (N=6,15,30) have been shown in Figures 22 through 27.

Clearly, it can be seen from the figures that with the increase in the model order, there is an increase in the accuracy of the vector fitting technique. This can be inferred from the improved correlation between the results of vector-fitting, and the difference between the EM and modeled data. However, such large values (N=15, 30) of the order of rational function translate to large number of residues and poles,

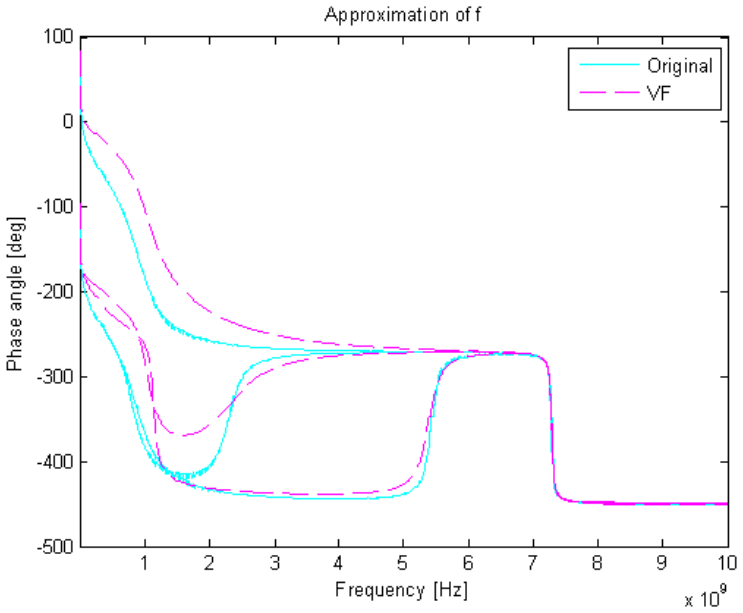

Figure 23. Phase correlation for Y_a, Y_b, and Y_c between the difference of circuit-EM parameters, and that obtained from vector fitting (model order = 6).

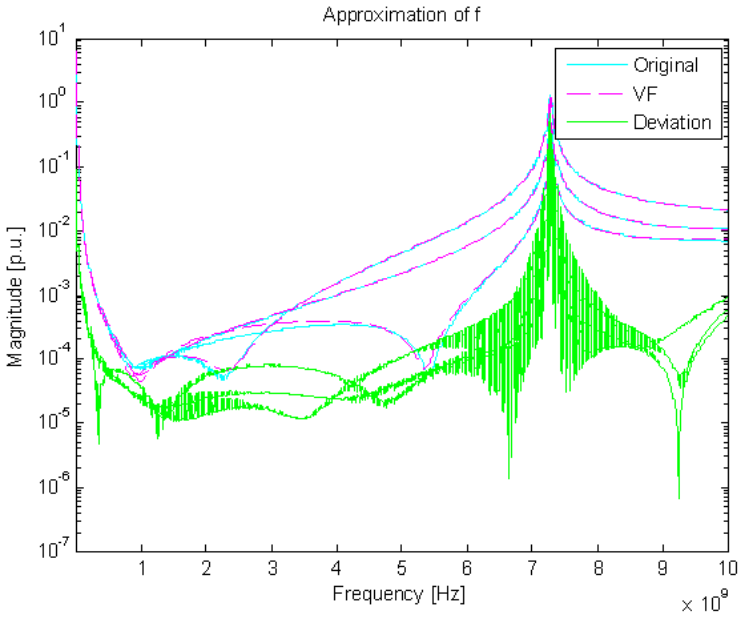

Figure 24. Magnitude correlation for Y_a, Y_b, and Y_c between the difference of circuit-EM parameters, and that obtained from vector fitting (model order = 15).

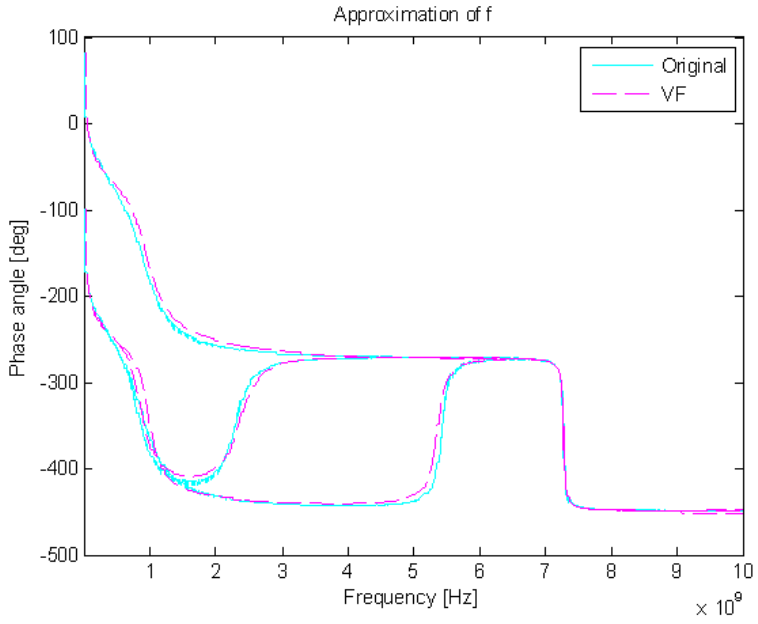

Figure 25. Phase correlation for Y_a, Y_b, and Y_c between the difference of circuit-EM parameters, and that obtained from vector fitting (model order = 15).

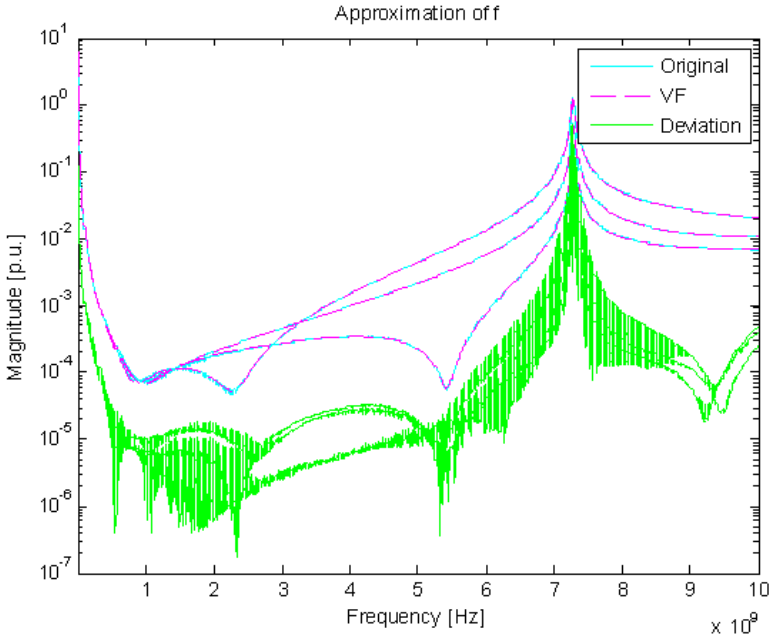

Figure 26. Magnitude correlation for Y_a, Y_b, and Y_c between the difference of circuit-EM parameters, and that obtained from vector fitting (model order = 30).

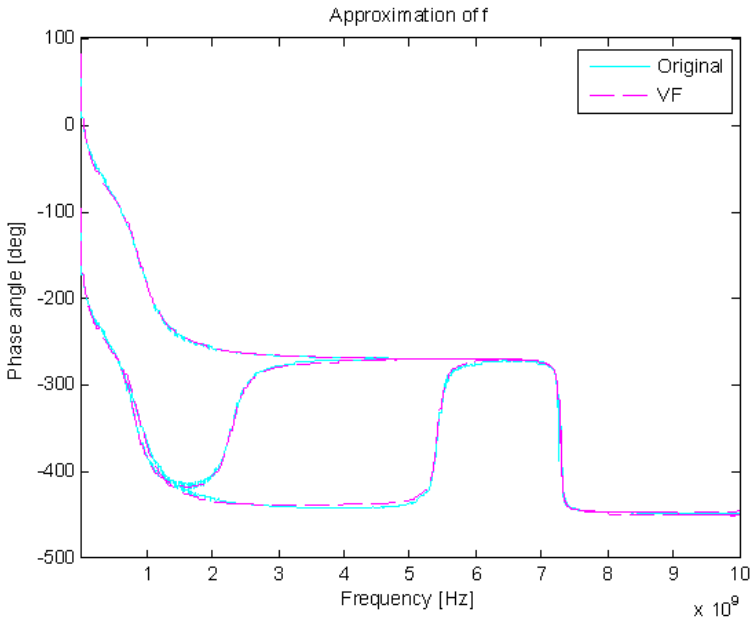

Figure 27. Phase correlation for Y_a, Y_b, and Y_c between the difference of circuit-EM parameters, and that obtained from vector fitting (model order = 30).

which, in turn, leads to the addition of large SPICE-equivalent circuits. Such an approach is not, therefore, suitable for physical model development and component sizing, since the physical intuition of the lumped element model is lost in the "black-box" curve-fitting process.

The disadvantages of BEMP-based macromodeling and vector-fitting, in the context of RF design, can be listed as follows:

(a) Lack of "physical intuition" into the circuit/component being modeled.

(b) Generation of large (greater than 50 elements) non-physical netlists, making mapping intractable.

(c) Strong dependence of accuracy on the model order.

(d) Requirement of additional processing for the conservation of passivity.

Clearly, there is a need for an efficient and accurate broadband modeling methodology for fast design closure of RF modules. The mathematical approach to the broadband

modeling methodology has been detailed in the following sections.

2.3 Mathematical formulation of the augmentation approach

The mathematical framework for the augmentation methodology has been presented in this section. The basic approach to circuit augmentation is similar to that shown in [47], [77]. However, the proposed method *differs* in the way the augmented elements are synthesized. To describe the methodology, it is important to recollect that simple lumped circuit models (S-LCMs) are generally available to approximate the multi-port behavior of a device or a network. The model parameters are extracted at a specified frequency. Therefore, quite expectedly, good correlation is shown by the S-LCM with the EM data over a certain range around the nominal frequency(the nominal frequency being the one where the parameter extraction was performed). However, in most cases, the frequency response of the S-LCM is not acceptable over broad ranges of frequencies. To improve the S-LCM, a set of frequency dependent impedances $z_{aug}(\omega)$, were added at arbitrary locations of the S-LCM. Here, there was no initial knowledge of the locations where these impedances need to be added. For an electrical network, the modified nodal analysis (MNA) relation, in its simplest form, is given by

$$Ax = Bv, \tag{12}$$

where $\mathbf{A}\epsilon\mathbb{C}^{N\times N}$ is the MNA matrix, $\mathbf{B}\epsilon\mathbb{R}^{N\times m}$ is a binary selector matrix which maps the port voltages into the MNA space, $v\epsilon\mathbb{C}^{N\times 1}$ contains the voltage sources connected to the terminals, and $x\epsilon\mathbb{C}^{N\times 1}$ is a vector containing the unknown variables of the MNA space. From this, the Y-parameters of the m-port equivalent circuit can be written as

$$Y = B^t A^{-1} B. \tag{13}$$

Let the measured y-parameters of the actual device be represented by Y_{meas}. The goal is to modify the S-LCM such that it the matches the measurement/EM data.

The augmenting elements are chosen from a *predesigned* library of shunt and series elements. Different elements are added in turn till the desired response is met. Even though, compared to [47], the iterations can be larger (but of the same order, stability and passivity of the final circuit is enforced by the use of constraint-based calculation of the values of the augmented elements. Such a constraint-driven calculation of impedances/admittances may, in principle, lead to slight inaccuracies in the network responses, due to additional conditions on the element values for overall error convergence of the updated network. But the focus in this work is the efficient development of first-cut broadband models in minimum computational steps that are encountered in traditional macromodeling techniques. Let an augmented element be represented by z_{aug}^{mn}, where m and n represent the nodes between which z_{aug} is connected. Let the corresponding new MNA matrix be $\hat{A}$ and the new y-parameters be $\hat{Y}$. The objective here is to find z_{aug}^{mn} so as to minimize the following error function

$$\varepsilon = \left\| Y_{meas} - \hat{Y} \right\| = \left\| Y_{meas} - B^T \hat{A} B \right\| \tag{14}$$

It is to be noted that the straightforward evaluation of Equation 14 leads to a nonlinear optimization problem. To overcome the nonlinearity of the optimization problem, a direct relation between the error ϵ and z_{aug}^{mn} is obtained [47]. The following sections describe the addition of series elements, shunt elements, and finally both type of elements.

2.3.1 Shunt augmentation

Let Δx be the change in the MNA space due to the addition of z_{aug}. For the rest of the discussion, the superscript mn will be omitted for the sake of simplicity of expression. Let ξ be an $N \times 1$ vector that maps the connecting nodes to the MNA space. In other words, if z_{aug} is added the nodes m and n, then the mth and the nth entries of ξ are set to '+1' and '-1',respectively and zeros everywhere else. The ξ

vector has been shown in Equation 15 as

$$\xi_{kl} \equiv [0 \ldots 0 \quad +1 \quad 0 \ldots 0 \quad -1 \quad 0 \ldots 0]^T . \tag{15}$$

In the case, where the shunt augmentation is between the kth node and ground, only of the kth entry is set to '+1' and zeros everywhere else. Let v_{oc} represent the open-circuit voltage and z_{TH} be the Thevenin equivalent impedance seen between the connecting nodes. As shown in [77], the effect of adding an arbitrary impedance between two nodes of a circuit is given by

$$\Delta x = -A^{-1}\xi \frac{\xi^T A^{-1} B v}{z_{aug} + \xi^T A^{-1} \xi}. \tag{16}$$

Consequently, the updated variable space of x is given by

$$\hat{x} = x + \Delta x. \tag{17}$$

Using Equations 12,13 and 16, Equation 17 can be rewritten as

$$\hat{x} = A^{-1}Bv - A^{-1}\xi \frac{\xi^T A^{-1} B v}{z_{aug} + \xi^T A^{-1} \xi}. \tag{18}$$

After a few mathematical manipulations, it is straightforward to show that

$$\Delta Y = B^T A^{-1} \xi (\xi^T A^{-1} B) \gamma_{aug}, \tag{19}$$

where γ_{aug} is defined to be

$$\gamma_{aug} = (z_{aug} + \xi^T A^{-1} \xi)^{-1} \tag{20}$$

Subsequently, the z_{aug} for a shunt connection is given by

$$z_{aug} = \gamma_{aug}^{-1} - \xi^T A^{-1} \xi \tag{21}$$

It is to be noted that the evaluation of (21) leads to a value of z_{aug} that minimizes the error function ϵ. In this work, we will be dealing with two-port networks. The number of simultaneous augmentations is limited by the rank of the system. For a

two-port system, the number of simultaneous augmentation is usually three. More can be added, but iterations become necessary. For example, the y-parameters of a two-port network is given by

$$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{22}$$

By the reciprocal property of passive networks, $Y_{21} = Y_{12}$. Therefore, theoretically, three unknown augmented elements can be solved, at a time, with the Y-parameters of a two-port network. For multiple simultaneous shunt augmentations, three variables are solved at one time. The linear matrix equation for three augmented variables is

$$\begin{aligned} \Delta Y = B^T A^{-1} \xi_1 (\xi_1^T A^{-1} B) \gamma_{aug}^1 \quad + \quad B^T A^{-1} \xi_2 (\xi_2^T A^{-1} B) \gamma_{aug}^2 \\ + B^T A^{-1} \xi_3 (\xi_3^T A^{-1} B) \gamma_{aug}^3 \end{aligned} \tag{23}$$

In this case, each of $B^T A^{-1} \xi_1 (\xi_1^T A^{-1} B)$ is a two-by-two matrix. In terms of the matrix elements, for each frequency point ω_n, Equation 23 can be rewritten as

$$\begin{aligned} \begin{bmatrix} \Delta Y_{11} & \Delta Y_{12} \\ \Delta Y_{21} & \Delta Y_{22} \end{bmatrix}_{\omega_k} = \begin{bmatrix} D_{11}^1 & D_{12}^1 \\ D_{21}^1 & D_{22}^1 \end{bmatrix}_{\omega_k} \gamma_{aug}^1(\omega_k) \quad + \quad \begin{bmatrix} D_{11}^2 & D_{12}^2 \\ D_{21}^2 & D_{22}^2 \end{bmatrix}_{\omega_k} \gamma_{aug}^2(\omega_k) \\ + \begin{bmatrix} D_{11}^3 & D_{12}^3 \\ D_{21}^3 & D_{22}^3 \end{bmatrix}_{\omega_k} \gamma_{aug}^3(\omega_k) \end{aligned} . \tag{24}$$

Simultaneous equations can, subsequently be formed by equating the coefficients of the matrices (or their linear combinations) as shown

$$\begin{bmatrix} \Delta Y_{11} \\ \Delta Y_{21} + \Delta Y_{21} \\ \Delta Y_{22} \end{bmatrix}_{\omega_k} = \begin{bmatrix} D_{11}^1 & D_{11}^2 & D_{11}^3 \\ D_{21}^1 + D_{12}^1 & D_{21}^2 + D_{12}^2 & D_{21}^3 + D_{12}^3 \\ D_{22}^1 & D_{22}^2 & D_{22}^3 \end{bmatrix}_{\omega_k} \begin{bmatrix} \gamma_{aug}^1 \\ \gamma_{aug}^2 \\ \gamma_{aug}^3 \end{bmatrix}_{\omega_k} \tag{25}$$

The system of simultaneous equations shown in Equation 25 is solved by linear least-squares technique as

$$\Gamma = (\mathbf{D}^T\mathbf{D})^{-1}\mathbf{D}^T\Delta\mathbf{Y}, \tag{26}$$

where, Γ is the γ vector in (25), $\mathbf{D}$ is the coefficient matrix in (25), and ΔY is the vector of ΔY parameters in (25). Since the linear formulation shown in Equation 23 is an approximate equation to obtain an optimum solution of a system using linear least-squares, a finite error is incurred. The error function for a set of augmented elements, cumulated over the frequency range is given by

$$\Phi(\mathbf{x}) = \left[\frac{1}{N_f}\sum_{k=1}^{N_f}\left[\sum_{i=1}^{N_p}\sum_{j=1}^{N_p}\left|Y_{i,j}^{meas}(\omega_k) - Y_{i,j}^{model}(\omega_k,\mathbf{x})\right|^2\right]^{1/2}\right] \tag{27}$$

It can be seen that the error function in Equation 27 is the average root-mean-square (rms) error, where N_p is the number ports, and N_f is the number of the frequency samples. Since a finite error is incurred in the linear formulation in (23), the y-parameters of the lumped element network do not match the measurement/EM data after a single iteration of the simultaneous solution of all the augmented variables. Instead, the values of the augmented elements are substituted in the lumped model to obtain the new updated y-parameters of the model and the error difference between the model and the measurement data is recalculated. This process of adding and updating the augmented networks is continued till the error difference between the y-parameters of the model and the measured data falls below a specified value. It should be noted, again, that the linear least-squares solution of the augmented variables is performed for each frequency point, since the error difference, shown in Equation 28 is the cumulative error over the frequency range as

$$\epsilon(j\omega) = \|Y_{meas}(j\omega) - Y(j\omega)\|. \tag{28}$$

2.3.2 Series augmentation

The discussion in the previous section considered the case where the augmented elements were added in parallel to the existing elements of the network. In terms of the network topology, a shunt augmentation do not add extra nodes to the existing network. Specifically, a shunt augmentation do not affect the size of the matrix A, B and the ξ vectors in Equation 23. This is because, the dimensions of these parameters (A, B and ξ) depend on the number of nodes present in the network.

However, in a series augmentation, the nodes of the network need to be updated during augmentation of a new element. Renumbering all the nodes in a large network can become cumbersome. In this work, the largest node number is searched and the corresponding value is incremented by unity and assigned to the new node that is being added during the augmentation. In this process, the numbers of the pre-existing nodes are preserved and need not be updated. The idea has been graphically depicted in Figure 28. The addition of a series element is performed along the lines of the tech-

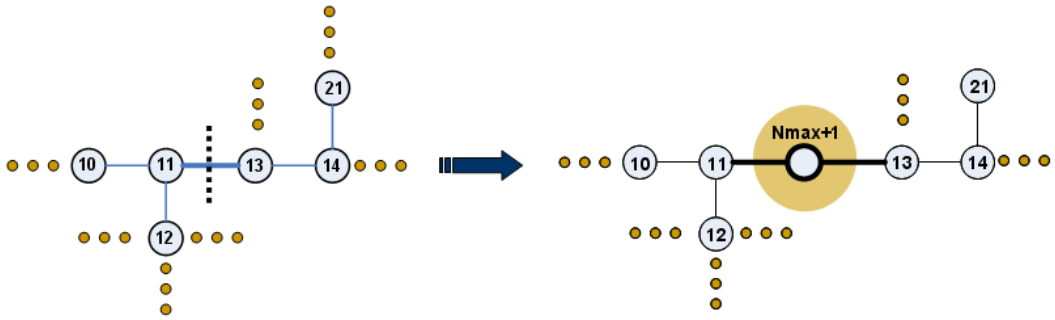

Figure 28. Graphical illustration of the node numbering technique, implemented in the series augmentation methodology.

nique shown in [78] (while adding inductor-type elements to the MNA matrix). Here, a new variable representing the unknown current through the augmented variable is added to the vector x in the MNA equation in (12). Further, if a series element is added at the k^{th} node, the ξ vector is a column vector with its k^{th} entry set to '+1' and zeros elsewhere. If the augmented variable is on the m^{th} row, the m^{th} diagonal

entry of A is set to $-z_{aug}$. Following the derivation in the previous section (for shunt augmentation), it is straightforward to obtain the augmented element z_{aug} as

$$-z_{aug}^{-1} = \gamma_{aug}^{-1} - \xi^T A^{-1} \xi. \tag{29}$$

2.3.3 Multiple simultaneous augmentation

In general, adding a series or parallel element one at a time, may not lead to fast convergence. Therefore, to analyze realistic test structures, the ability to add multiple series and/or shunt element simultaneously is imperative. Ordinarily, from a model optimization perspective, the effect of adding multiple elements simultaneously, to a network, is different from the effect of individually but separately adding the same elements. In addition, as mentioned before, the simultaneous addition of series and shunt elements allows the technique to handle realistic test structures and data, which requires a combination of series and shunt element addition to match the measured/EM effects. To accommodate both the series and shunt augmentation in the modeling framework, a verification stage (to identify the type of connection) is added to the existing series and shunt formulation. Based on the type of augmentation for each element, either of the series or shunt formulation is applied to arrive at the final network, when the error bound is satisfied. The flowchart for the series/shunt implementation is shown in Figure 29. As mentioned before, the number of simultaneous augmentations is limited to the rank of the system, which is usually three for a two-port network. More augmentations can be added but iterations becomes necessary.

2.4 Test cases

In this section, the validity, accuracy, and the efficiency of the proposed methodology is presented. The first test case under consideration is a spiral inductor embedded in multi-layer, LCP-based substrate. The layout of the inductor and the corresponding lumped element model (extracted at a particular frequency) is shown in Figure 17.

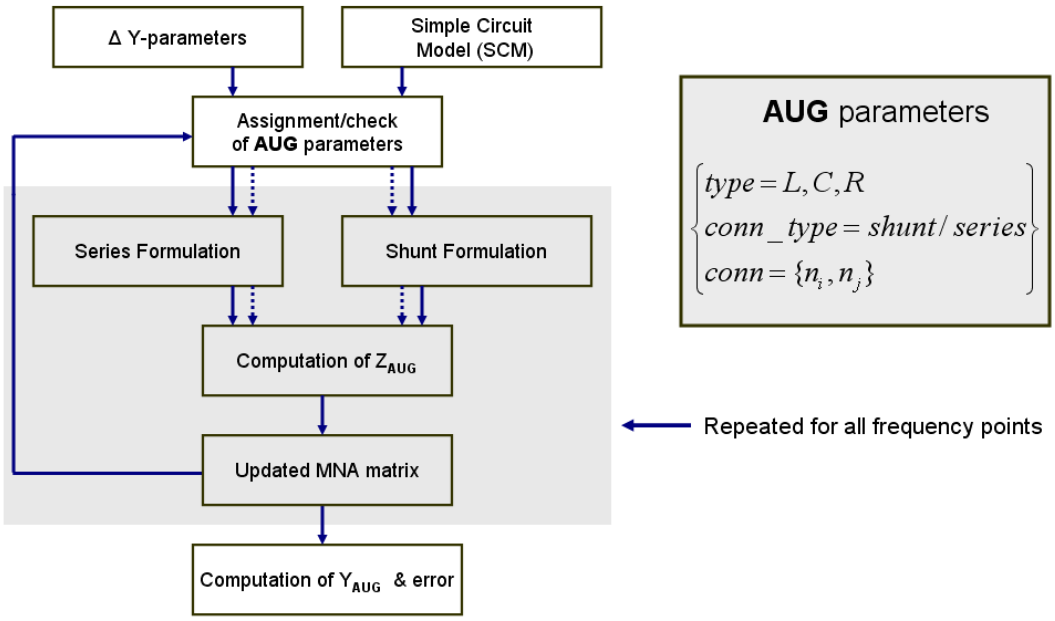

Figure 29. Flowchart for series and shunt augmentation.

The layout of the inductor, shown in Figure 17, was simulated in SONNET. The correlation between the unaugmented model and the EM data is shown in Figure 30. The augmentation technique was applied to the S-LCM of the inductor. The convergence took 13 iterations, for the solution passes of all the augmented network elements. At every pass of the iteration, three elements were either solved or updated. The augmented model has been depicted in Figure 44. The highlighted sections represent the augmentation to the S-LCM, two-port inductor. The augmented values are; Lsh2=6.8 nH, Csh1=1.2 pF, Rsh1=2.6 ohm, Csh2/3=0.22 pF, Rsh2/3=44 ohm.The results of augmentation has been depicted in Figure 31. Clearly, it can be seen in Figure 31 that the model response matches the EM data, quite expectedly, at the frequency where the parameters of the model were extracted. An example of the error convergence after multiple iterations of augmentation is shown in Figure 33.

The second test case under consideration is a planar embedded capacitor. The layout of the capacitor in SONNET and the corresponding S-LCM, are shown in Figures 34. The difference in the Y-parameters between the EM data and the S-

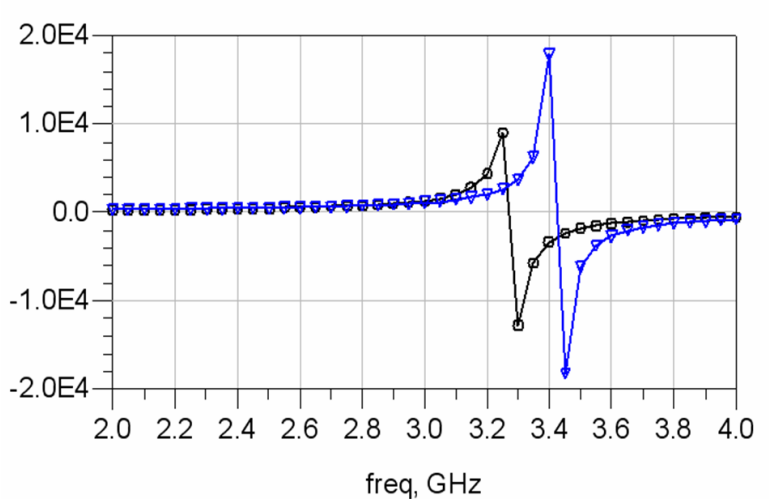

Figure 30. Comparison of the Z11-parameters of the EM simulation data with the unaugmented circuit model (S-LCM) of the inductor.

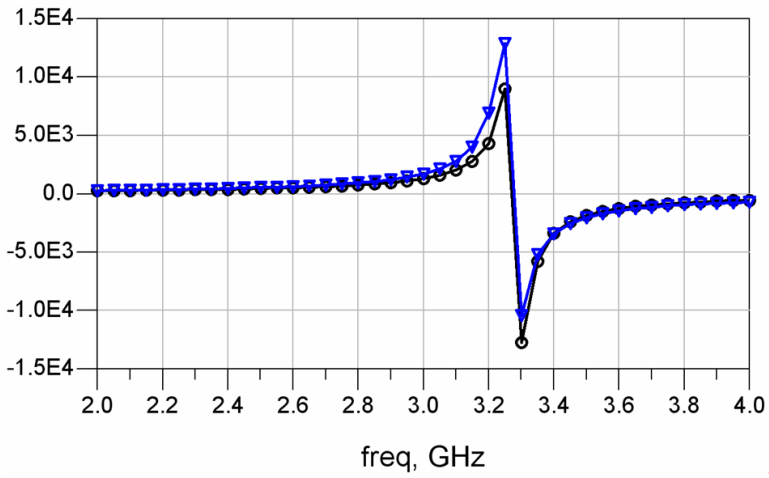

Figure 31. Comparison of the Z11-parameters of the augmented circuit model with the EM simulation data.

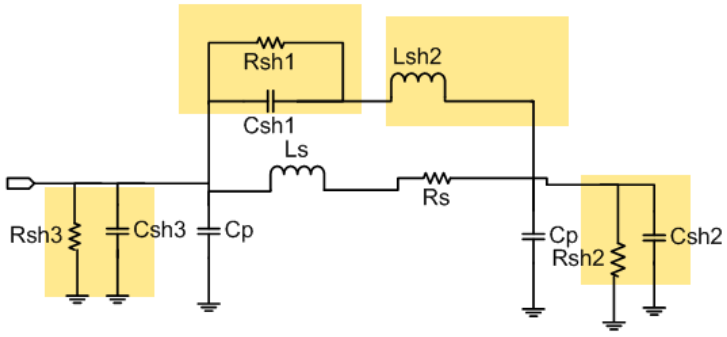

Figure 32. Augmented model of the spiral inductor; the augmentation elements are represented by the shaded boxes.

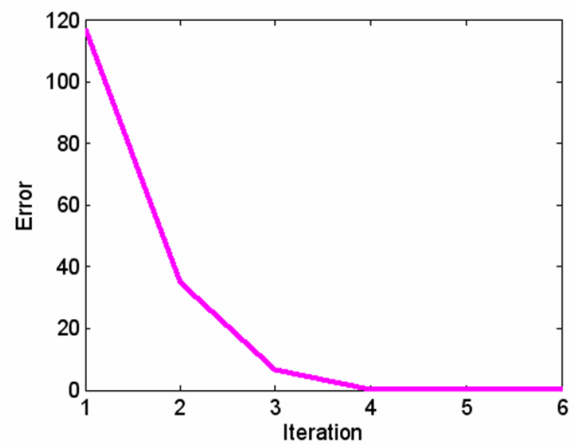

Figure 33. Augmentation error as a function of the number of iterations.

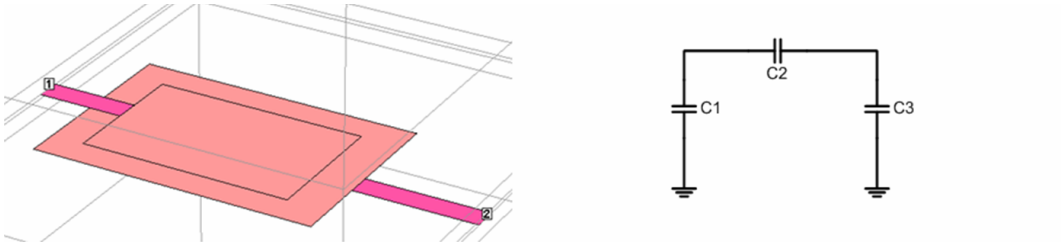

Figure 34. Layout of a planar capacitor (in SONNET).

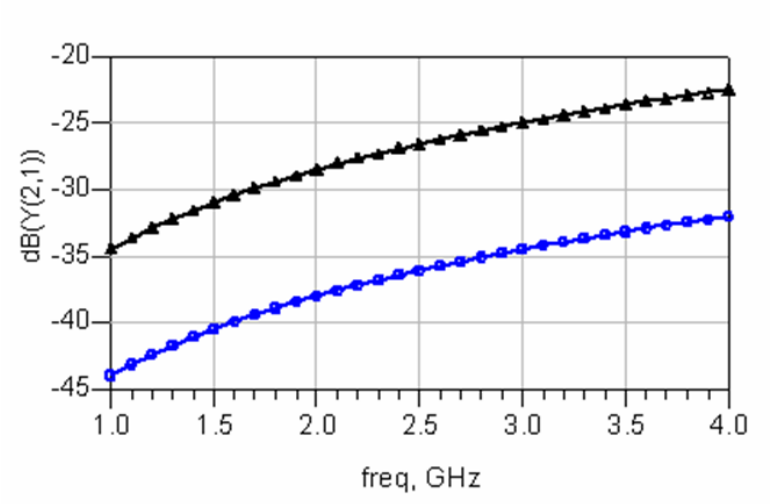

Figure 35. Comparison of the Y-parameters of the S-LCM of the capacitor, and that obtained from the EM simulation.

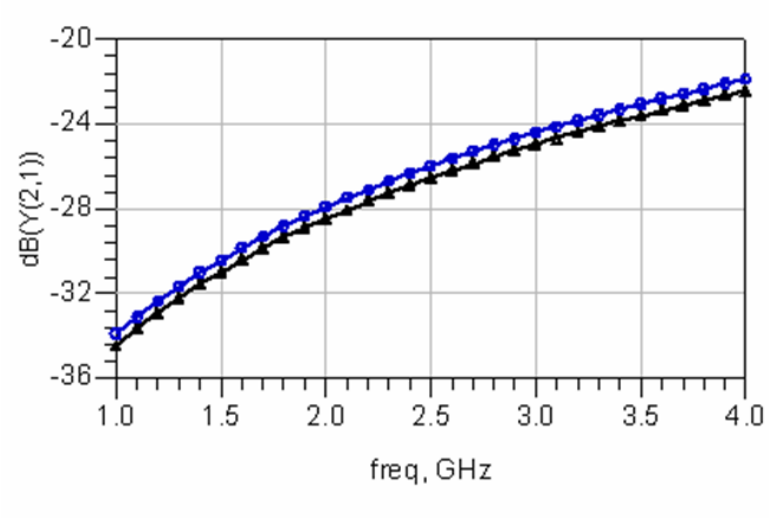

Figure 36. Comparison of the Y-parameters of the augmented model of the capacitor, and that obtained from the EM simulation.

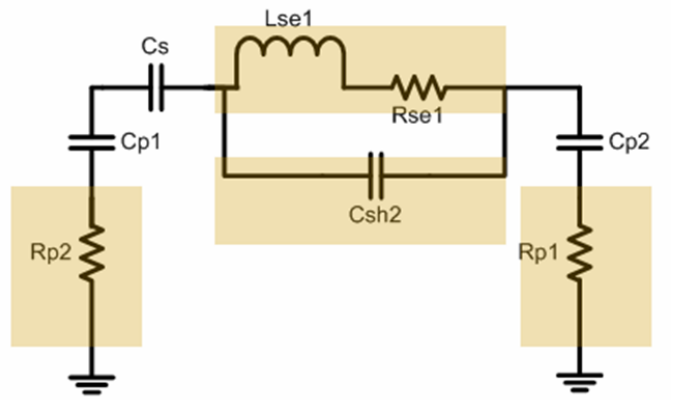

Figure 37. Augmented model for the capacitor; the augmented sections are represented by the shaded boxes.

LCM is shown in Figure 35. Clearly, there is a significant difference between the two results. The augmentation technique was applied to the S-LCM in order to simultaneously add series and shunt elements at different locations of the model. The final updated model and the results after convergence (within the specified error) are shown in Figures 37 and 36, respectively. The augmented values are; Lse1=0.4 nH, Rse1=1.2 ohm, Rp1=Rp2=4.6 ohm. As shown in Figure 36, the augmentation technique is useful for broadband matching of the passive component models with the EM/measurement data. In addition, the final, augmented model is stable and passive,

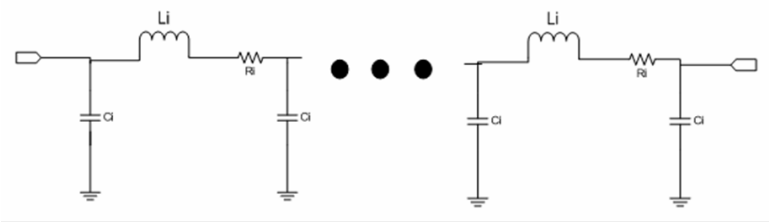

Figure 38. Multi-section model for the embedded RF inductor.

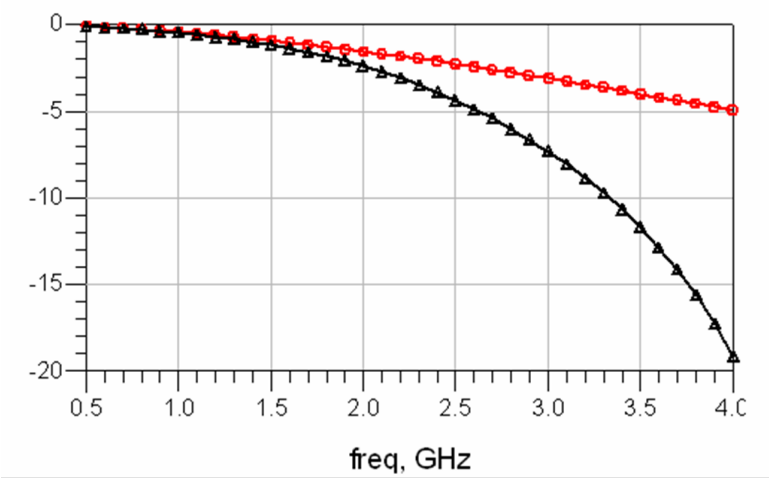

Figure 39. Comparison of the S-parameters of the S-LCM (circle) and that obtained from the EM solver (triangle).

due to the use of predesigned, physical element library and boundary conditions in the calculation of the impedance/admittance values.

In the third case, the goal was to develop a cascaded multi-section model for the embedded RF inductor shown in Figure 17. The multi-section S-LCM for an embedded inductor is shown in Figure 38. The difference between the S-parameters of the S-LCM and that obtained from the EM data is shown in Figure 39. Series and shunt augmentations were applied to the S-LCM to obtain a broadband multi-section model. The results of augmentation is shown in Figure 40. The multi-section augmented model is shown in Figure 41.

It took 20 s (DELL dualcore workstation, 2.8 GHz Pentium IV processor and 3 GB RAM) and 15 iterations for the convergence of all the augmented sections.

The fourth test case under consideration is another spiral inductor (with a value

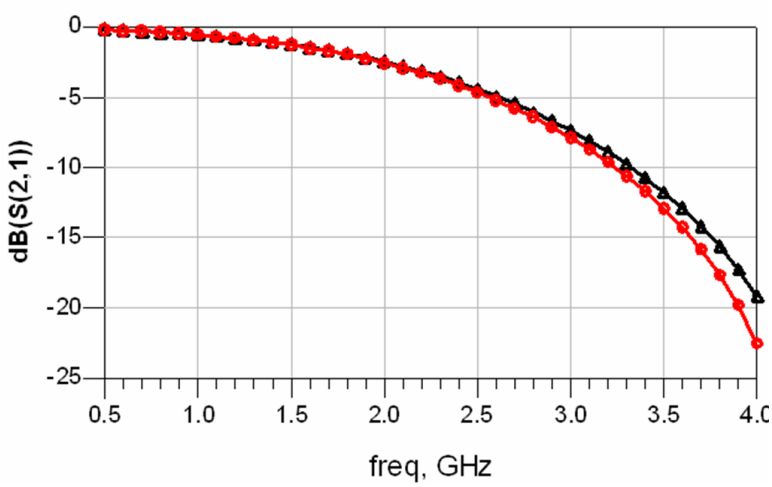

Figure 40. Correlation between the S-parameters of the augmented model (circle) and that obtained from the EM solver (triangle).

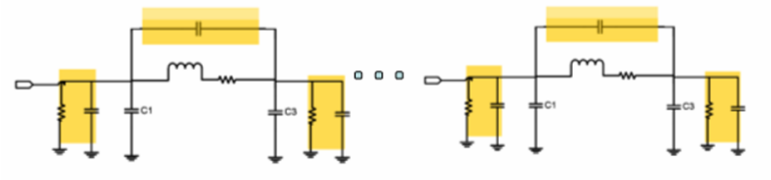

Figure 41. Multi-section augmented model for the embedded RF inductor; the shaded boxes represent the sections augmented to the core S-LCM.

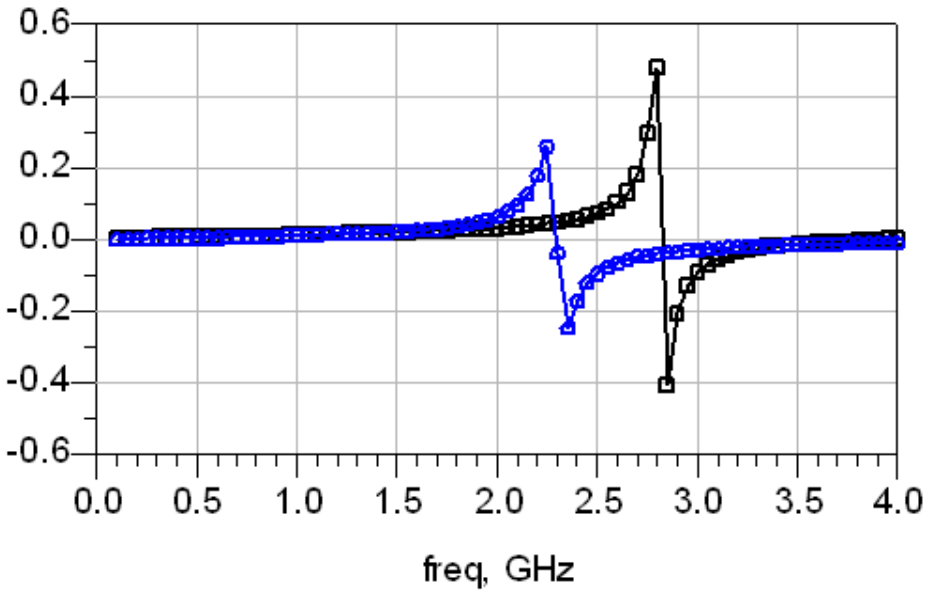

Figure 42. Comparison of the Y-parameters of the EM simulation data (data symbol:square) with the simple circuit model (S-LCM) of the inductor (data symbol:traingle).

different from that in test-case 1) embedded in multi-layer, LCP-based substrate. The layout topology of the inductor and the corresponding lumped element model (extracted at a particular frequency) is similar to that shown in Figure 17.

The layout of the inductor was simulated in SONNET. The correlation between the unaugmented model and the EM data is shown in Figure 42. The augmentation technique was applied to the S-LCM of the inductor. The convergence took 13 iterations, for the solution passes of all the augmented network elements. At every pass of the iteration, three elements were either solved or updated. The augmented model has been depicted in Figure 44. The highlighted sections represent the augmentation to the S-LCM, two-port inductor. The results of augmentation has been depicted in Figure 31. It can be seen in Figure 31 that the model response matches the EM data, quite expectedly, at the frequency where the parameters of the model were extracted, after 16 iterations (for all the augmentations). The augmented values are as follows: Cs=0.8 pF, Lp=0.2 nH, and Cp4=Cp5=0.45 pF.

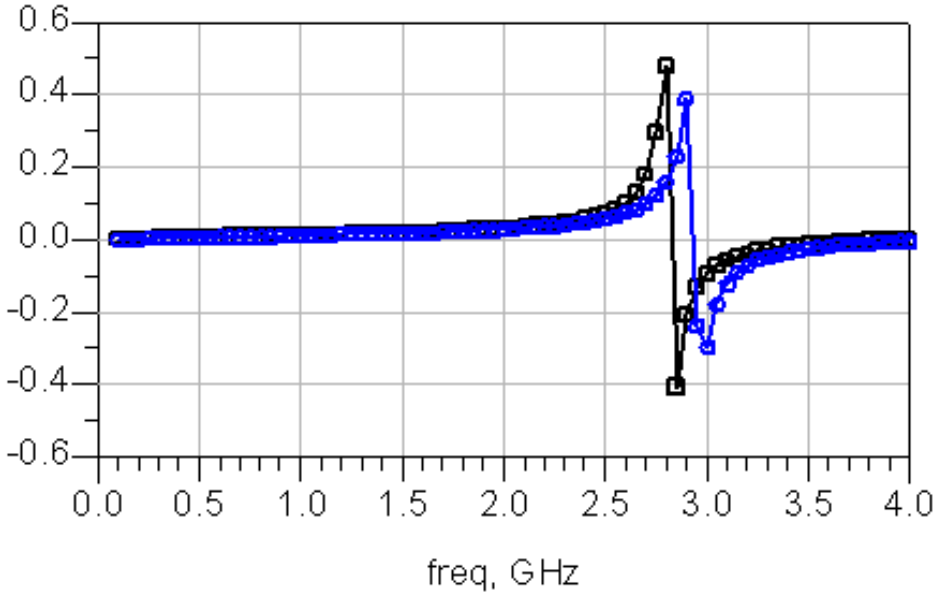

Figure 43. Comparison of the Y-parameters of the augmented circuit model (data symbol:circle) with the EM simulation data (data symbol:square).

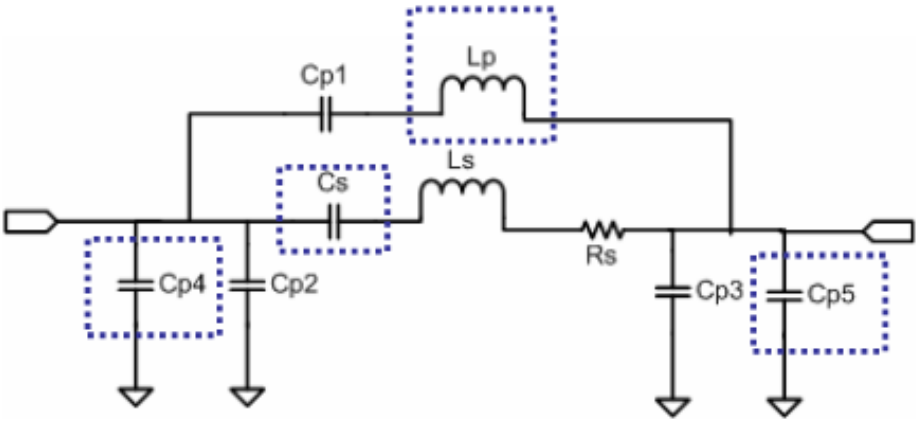

Figure 44. Augmented model of the spiral inductor; the augmentation elements are represented by the "dotted" boxes.

2.5 Summary

In this chapter, a circuit augmentation technique for broadband modeling of component libraries, and tuning of embedded passive circuits have been demonstrated. The circuit augmentation technique is based on a previously developed circuit partitioning technique, a modified nodal analysis formulation and a linear optimization framework. The circuit augmentation algorithm that has been implemented in this dissertation automatically ensures passivity and stability of the broadband model. The technique has been verified for broadband modeling of spiral inductors, planar capacitors. The circuit augmentation technique has also been applied for the tuning of bandpass filters. Comparisons have been performed with tuning using commercial circuit simulators, employing nonlinear optimization, to demonstrate the advantages of the proposed technique.

CHAPTER 3

EFFICIENT DEVELOPMENT OF DESIGN LIBRARY FOR LAYOUT-LEVEL SIZING OF RF CIRCUITS

In Chapter 1, it has been explained how the rapidly evolving telecommunications market has led to the need for advanced RF circuits. Accurate prediction, early in the design schedule, is difficult for complex multi-band/multi-mode RF circuits. In addition, time-to-market pressures require that design (circuit/electromagnetic)iterations be kept to a minimum. For integration in a SOP framework, there is a clear need for design cycle time reduction of passive and active RF modules. This is important because layout level electromagnetic (EM) optimization of RF circuits has been the major bottleneck for reduced design effort. Such bottlenecks are critical in design flows on emerging technologies, that lack of extensive component libraries. In Chapter 2, efficient techniques for the automatic development of passive, broadband circuit models from network analyzer/EM data have been explained. These techniques can then be applied for the development of design libraries and circuit sizing. As shown in Figure 45, the focus of this chapter is the efficient and accurate development of design libraries that enable the sizing of layouts, thereby significantly reducing the design cycle time.

In RF designs, the physical effects of layout such as the electromagnetic coupling and the parasitics affect the circuit performances. Furthermore, with the emergence of multiple frequency standards, the electrical specifications of the components have different constraints. For example, a voltage-controlled oscillator (VCO) operating at 2.45 GHz may require an inductor with a self-resonance frequency (SRF) of at least 5.5-6 GHz with high quality factor (Q). However, a 5.8 GHz VCO may require an inductor with a high SRF ($> 8 - 10$ GHz) and a reasonable Q. Design requirements of this kind can lead to very long EM simulation time. Since liquid crystalline

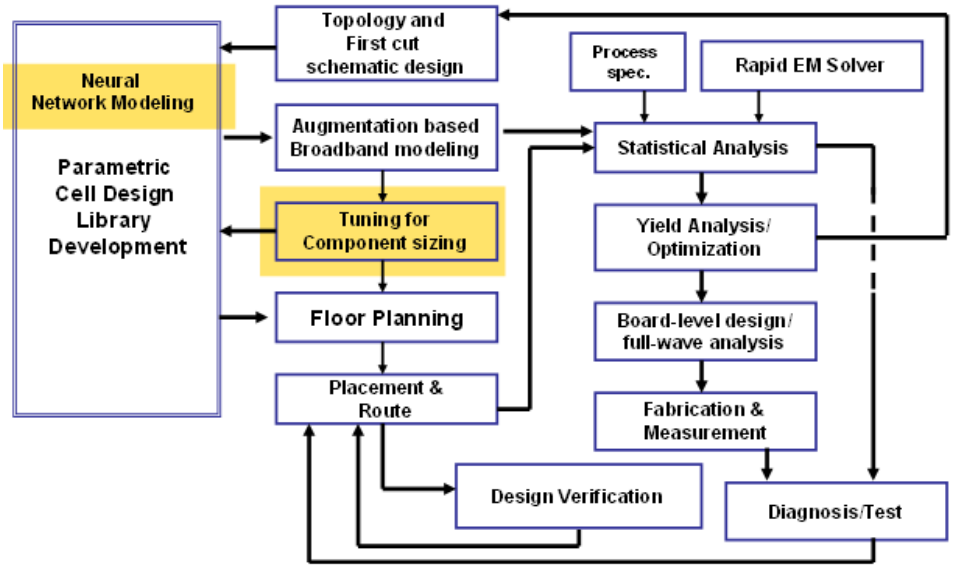

Figure 45. RF Design flowchart; the shaded boxes indicate the focus of Chapter III.

polymer (LCP) substrate provides design flexibility of RF circuits across a large frequency range (0.5-20 GHz) by embedding the passives in the substrate [9],[10],[16], a time-efficient, design constraint-based scaling and optimization technique can be useful. High performance, miniaturized filters, LNAs, VCOs, duplexers and baluns, functional from 500 MHz to 6 GHz, using embedded inductors and capacitors on multi-layer, organic laminate substrate with LCP have been reported in [10]. The fabricated inductors have Qs varying from 30-200 for an inductance range of 1-25 nH [16]. The capacitors with a capacitance density of 1 pF/mm^2 and Qs greater than 300 have also been demonstrated [16],[10]. In this chapter, a scaling method has been proposed and applied to the library development of embedded passives in LCP substrates. In Chapter 2, an augmentation methodology has been demonstrated for the development of broadband models of passive components. In this chapter, an ANN-based technique has been proposed to develop component libraries. The two techniques was then combined to perform tuning for layout-level sizing of passive devices (e.g. bandpass filters).

With increasing design complexity of multi-band RF front-end modules, along

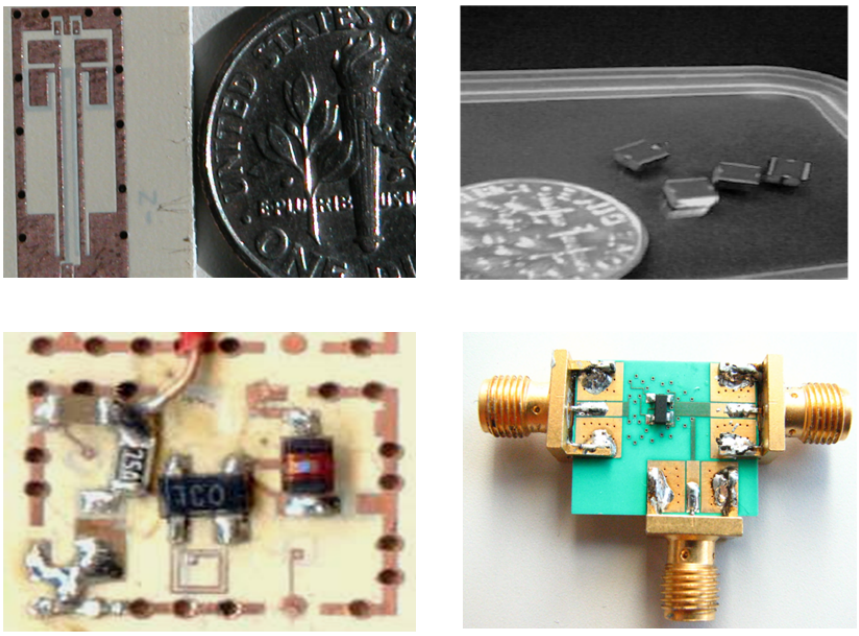

Figure 46. Fabricated RF front-end blocks in LCP-based substrates; baluns(top-left), bandpass filters(top-right), oscillators(bottom-left), and mixers(bottom-right).

with stringent performance specifications, the need for fast design closure is imperative. From Chapter 1, it is clear that the existing design methodologies for SOP-based RF circuits suffer from such major drawbacks as:

(a) Design flows are not scalable at the layout level and *completely new* set of EM/circuit simulations are required to generate the layout for a new set of design specifications

(b) Prototype circuits require multiple iterations of EM simulations for fault detection in fabricated circuits.

(c) Design flows lack "multi-domain" (electrical, mechanical parameters, to name a few) statistical diagnosis and yield enhancement techniques for batch-fabricated circuits on large panels.

In Chapter 1, the various methods adopted by the researchers to optimize RF circuits have been discussed. These include geometric programming [30], neural network

modeling [35], space mapping [33], aggressive space mapping [79], and polynomial mapping [31]. In all of these methods, there is focus on optimization of a pre-designed layout, as opposed to design scaling to meet different performance specifications. For example, the space mapping technique proposed by [33] provides a way for efficient optimization once the structure is generated. This is performed through the coarse and fine mapping implemented in the space mapping algorithm. Inherently, design scaling requires a perturbation of a larger "design space" as opposed to nominal design optimization. Furthermore, methods such as neural network-based modeling, convex optimization [63], and geometric programming depends on the analytical expressions of the electrical/process parameters of the circuit/module component being modeled. Therefore, these techniques will be limited by the analytical complexity of the multi-layer models for circuits that have a large number (> 25) of active and passive components embedded in different layers of the multi-layer substrate. Additionally, the focus of prior works is on time-efficient layout optimization of RF circuits and not synthesis/efficient library development. Accurate and efficient generation of component and circuit libraries, required for new design as well as design scaling, therefore, is the subject of this chapter.

For proof-of-concept validation, the library development and the design scaling methodologies have been demonstrated on a multi-layer, organic substrate with LCP dielectric material (ϵ_r=2.95, $tan\delta$=0.002). The electrical characteristics of the LCP material have been discussed in Chapter 1. It should be noted, however, that the method is generic and can be applied to designs on any multi-layer packaging technology. The method presented in this chapter enables the layout-level scalability of inductors and filters based on the constraints imposed by design specifications. The technique is based on nonlinear mapping of inductor and filter geometries and its electrical specifications using ANNs and polynomial functions with limited data

generated from EM solver. The design scaling methodology is based on layout segmentation, broadband model mapping and nonlinear/linear circuit-level optimization. The aforementioned methodologies have the following advantages:

(1) It enables global tradeoff analysis between competing objectives such as area, Q and SRF for planar inductors and capacitors.

(2) It uses a small dataset for neural model training by using adaptive interpolation.

(3) It enables component and device layout scalability across the various topologies.

(4) It allows for the mapping between the electrical response and the physical parameters.

(5) It enables the scalability of the circuit layout over a range of +/-20% of the center frequency (CF).

(6) It allows bandwidth tunability of 0.5-5% of CF.

(7) It reduces the number of iterations for EM simulations performed on the layout to meet design specifications.

3.1 Layout-level scaling of RF Circuits: Concept

In RF designs, the physical effects of the layout such as electromagnetic coupling and parasitics affect the circuit performance. Furthermore, with the emergence of multiple frequency standards, the electrical specifications of components have different constraints. Since liquid crystalline polymer (LCP) substrate provides design flexibility of RF circuits across a large frequency range (0.5-20 GHz) by embedding the passives in the substrate, an efficient and scalable library development technique can be useful for fast design closure of RF circuits.

Layout-level scaling is the process of extracting network/layout level parameters for a component/circuit from an existing set of specifications. Traditionally, RF

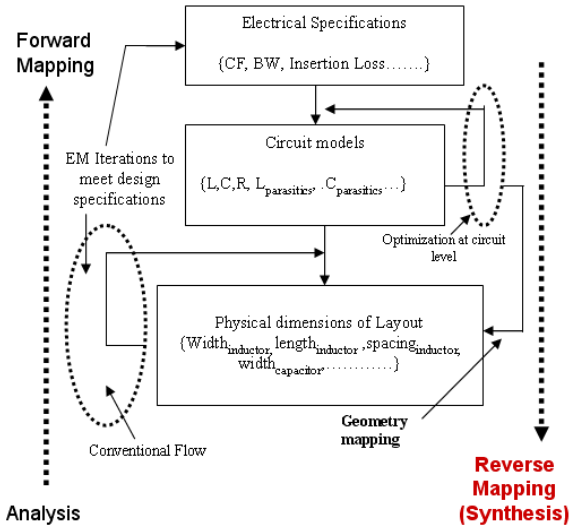

Figure 47. Flowchart for conventional design and layout-level circuit scaling; the iteration shown on the left is performed in forward mapping while that shown on the right is performed in design scaling.

design flows lack scalability due to the effects of layout level parasitics on circuit performance. The steps involved in developing a layout scaling methodology for RF circuits has been shown in Figure 47. A conventional design flow attempts to optimize the circuit performance at the layout level at the premium of time-consuming EM simulations for the full layouts. In contrast, a design scaling approach extracts physical dimensions of the layout from the electrical specifications by using some intermediate circuit level modeling and optimization. As shown in Figure 47, the scaling method develops a lumped circuit model with parasitics from a layout. To scale the model to a different frequency specification with minimum EM simulations, the proposed method performs optimization at the circuit level. After optimization, the physical dimensions of the layout are extracted using polynomial functions that map the physical parameters to their component values.

3.2 RF bandpass filters in LCP substrate

The bandpass filter is an important block in an RF front-end module. With the convergence of multiple frequency standards, the design of filters faces such design

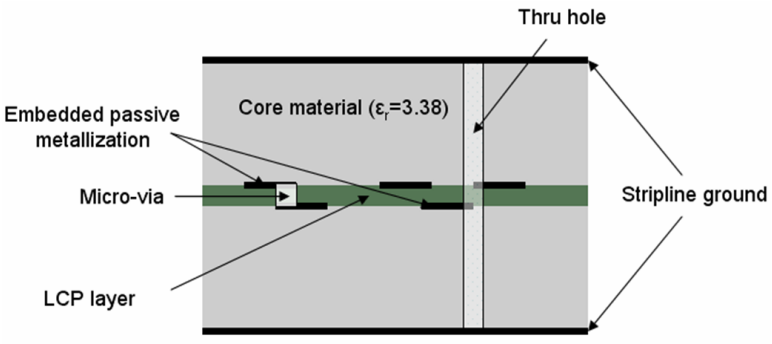

Figure 48. Cross-section of the dielectric stackup for the stripline configuration.

challenges as controllability of passband ripple, bandwidth, stopband attenuation, and harmonic rejection. High-performance, miniaturized filters have been designed in LCP-based substrate across different topologies to meet different frequency specifications. These include inductively coupled resonator filters, coupled line filters and capacitively coupled filters [10]. The filter designs are also based on hybrid topologies with a combination of coplanar waveguide (CPW) and stripline configurations to ensure volumetric reduction in multi-layer substrate. The filters are electromagnetically shielded with the use of top and bottom ground planes for reducing signal coupling from adjacent blocks.

Figure 46 illustrates the photograph of fabricated filters, with a size of 2mm X 2mm X 1.2 mm for Wi-Fi applications. The cross-section used for the filters is shown in Figure 48. The stackup consists of a 4-metal layer stackup with top and bottom ground planes. The core dielectric material ($\epsilon_r = 3.35$) on either side of the LCP layer has low loss and has a thickness of 36 mils. The laminated LCP and the metal layers are 1 mil and 0.5 mils thick, respectively. The passives are designed in the middle two metal layers. The entire cross sectional thickness of 1.8 mm (can be as low as 0.9 mm, in current processes) was fixed in the designs that have been used for validation in this dissertation.

In addition to the layout sizing of bandpass filters, details on inductor synthesis have also been described. This is because, for a fixed cross section, the capacitance is a

function of the width and the length and its Q value is only limited by the loss tangent ($tan\delta$) of the dielectric material [10]. However, inductors have multiple geometrical parameters such as the side-length, line width, line spacing and the number of turns. Furthermore the Q values of the inductors are comparatively lower than that of the capacitors. The need for high-Q inductors, coupled with the difficulty of achieving it, make the geometry optimization of inductors, an indispensable part of RF circuit design.

3.3 Efficient library development for embedded passives

In the absence of extensive design libraries of embedded passives in LCP-based substrates, synthesis techniques for inductors/capacitors, based on multiple design constraints, is important. Methods for optimization of inductor geometries in a multi-variable design environment have been reported by [30],[31]. In contrast, this section provides a layout-level synthesis technique for planar inductors that is used in RF front-end modules.

3.3.1 Multi-variable nonlinear mapping using ANNs

In the design of inductors, a nonlinear relationship exists between electrical parameters like inductance (L), Q and SRF; and the geometrical design variables such as the side-length, line-width, line-spacing and the number of turns. Artificial neural networks have emerged as a powerful alternative to numerical and analytical modeling techniques for capturing such nonlinear mapping of parameters.

ANNs are preferred due to their asymptotic properties, and because they exhibit smooth results for approximating multi-dimensional discrete data. A multi-layer, perceptron-based neural network structure is shown in Figure 49. During forward mapping, (from the inductor geometries to the electrical parameters), the input neurons $[x_1, x_2, ..., x_n]$ represent the inductor geometries, and the output neurons $[y_1, y_2, ..., y_m]$ produces L, SRF and Q as the output. Here n and m being the number

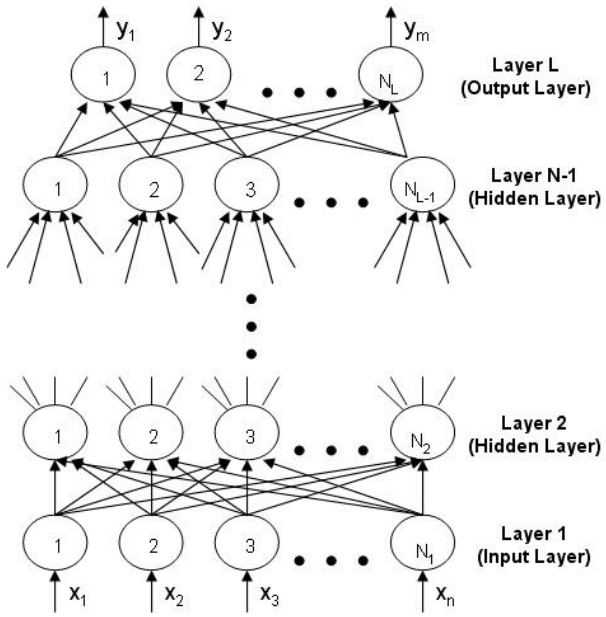

Figure 49. Multi-layer perceptron-based neural network structure.

of inputs and outputs in a general ANN structure. The datasets get reversed during reverse mapping. A single layer of hidden neurons has been used in this work. The outputs from all the processing units are summed through weights (w_{ij}) to form the output, as shown in Equation 30. This output passes through the activation function given by

$$\gamma_i^l = \sum_{j=0}^{N_l - 1} w_{ij}^l z_j^{l-1} \tag{30}$$

$$\sigma(\gamma) = \frac{(e^{\gamma} - e^{\gamma})}{(e^{\gamma} + e^{-\gamma})} \tag{31}$$

The activation function shown in Equation 31 is a hyperbolic tangent function. After passing through the activation function, the output dataset is obtained as

$$\sigma(\gamma_i^L) = \gamma_i^L = \sum_{j=0}^{N_{L-1}} w_{ij}^L z_j^{L-1} \tag{32}$$

In this work, the Levenberg-Marquadt nonlinear optimization algorithm has been used to train the neural networks. The details of this optimization technique has been discussed in the following section.

3.3.2 Levenberg-Marquadt optimization

Levenberg-Marquardt optimization is a virtual standard in nonlinear optimization techniques. It significantly outperforms the gradient descent and conjugate gradient methods for medium-sized problems (number of weights less than 1000). It is a pseudo second-order method, meaning that it works with only function evaluations and gradient information but it estimates the Hessian matrix using the sum of outer products of the gradients. To improve the convergence time without the loss of accuracy, the algorithm combines the speed of steepest descent (for sharp slopes), and the curvature or second-order information (for gentle slopes) of the modeling function. The iterative equation for steepest descent is given by

$$w_{i+1} = w_i - \mu \mathbf{d} \tag{33}$$

where w represent the weights that are associated with the edges of the multi-layer perceptron graph as shown in Figure. Here, $\mathbf{d}$ stands for the derivative and is given by

$$\mathbf{d} = \left\langle (f(x; w_0) - y) \nabla f(x; w_0)^T \right\rangle \tag{34}$$

where $f(x; w)$ represents the general deterministic modeling function. The purpose of the model training is to develop an optimized set of weights such that the output of the neural model is the closest approximation to the measurement/EM data.

Let E be defined as the average squared error, the error being the absolute difference between the actual data and that predicted by the trained neural network. It is well-known from linear algebra that when we have a linear function model, then the error function E is of a simple quadratic form

$$E(w) = \left\langle (f(x; w) - y)^2 \right\rangle \tag{35}$$

where the angle brackets donate the mean over input output pairs. First, let us consider the general deterministic model $f(x; w)$. It is a function of both the data

x and its parameters w. When the model is used to predict the behavior of the unknown target function,we have fixed w and are more interested in f as a function of x. However, when we are *training* our model by optimizing the weights to reduce E, we are interested in f as a function of w (instead of x). For the following discussion, we will consider this second view of f, and all derivatives and gradients are with respect to w.

One way to approximate E as locally quadratic (in w) near a minimum is to approximate $f(x; w)$ as a linear function of w. Let us define $\hat{f}(x; w)$ which is a linear approximation of $f(x; w)$ in the neighborhood of a specific weight value w_0 as

$$\hat{f}(x; w) = f(x; w) + (w - w_0)^T \nabla f(x; w_0), \tag{36}$$

Assuming the model is $\hat{f}$, the expressions for $E(w)$ and $\nabla E(w)$, in terms of y, $\hat{f}(x; w)$ and $\nabla \hat{f}(x; w)$ are written as

$$\hat{E}(w) = \left\langle (\hat{f}(x; w) - y)^2 \right\rangle, \tag{37}$$

$$\nabla \hat{E}(w) = \left\langle 2(\hat{f}(x; w) - y) \nabla \hat{f}(x; w) \right\rangle. \tag{38}$$

After a few mathematical manipulations, it can be shown that

$$\nabla \hat{E}(w) = \left\langle 2(f(x; w_0) + (w - w_0)^T \nabla f(x; w_0) - y) \nabla f(x; w_0) \right\rangle. \tag{39}$$

Let

$$\mathbf{H} = \left\langle \nabla f(x; w_0) \nabla f(x; w_0)^T \right\rangle \tag{40}$$

where $\mathbf{H}$ stands for the *Hessian*. It should be noted that while $\mathbf{d}$ is exactly the average error gradient, $\mathbf{H}$ is not the true Hessian (matrix of mixed partials) of the function. In other words, $H_{ij} \neq \partial f / \partial x_i \partial y_j$. Instead, $\mathbf{H}$ is an *approximation* to the Hessian which is obtained by averaging the outer products of the first order derivatives (gradients). To complete the quadratic approximation, we have:

$$\nabla \hat{E}(w) = 2\mathbf{H}(w - w_0) + 2\mathbf{d} \tag{41}$$

$$\nabla \hat{E}(w) = 0 \Rightarrow 2\mathbf{H}(w_{opt} - w_0) + 2\mathbf{d} = 0 \tag{42}$$

$$w_{opt} = -\mathbf{H}^{-1}\mathbf{d} + w_0 \tag{43}$$

Based on these derivations, the iterative update of the weights by steepest descent is modified as

$$w_{i+1} = w_i - \mathbf{H}^{-1}\mathbf{d}. \tag{44}$$

Intuitively, the Levenberg-Marquadt algorithm employs a steepest descent type method until the function approaches a minimum. Upon approaching the minimum, the iterative updating gradually switches to the quadratic rule. It can also be checked as to how the function approaches the minimum by tracking the change in the error. The "blend" between the steepest descent and the quadratic approximation is denoted by λ. The update rule is therefore modified as

$$w_{i+1} = w_i - (\mathbf{H} + \lambda\mathbf{I})^{-1}\mathbf{d}. \tag{45}$$

Mathematically, as λ gets small, the update rule approaches the quadratic approximation. On the other hand, if λ is large, the rule approaches the steepest descent. The iterative relation is made better by addition of local curvature information as shown in the final Levenberg-Marquadt form

$$w_{i+1} = w_i - (\mathbf{H} + \lambda diag[\mathbf{H}])^{-1}\mathbf{d}. \tag{46}$$

The only drawback of this nonlinear optimization technique is that it requires a matrix inversion step as part of the update which scales as the N^3 where N is the number of weights. For medium-sized networks (for example, a few hundred weights) this method will be much faster than the gradient descent plus momentum. Fortunately, the training of neural networks for practical RF structures are generally medium-sized problems (in terms of weights), thereby proving conducive to this powerful optimization technique. The following section discusses the test cases for training and data sampling.

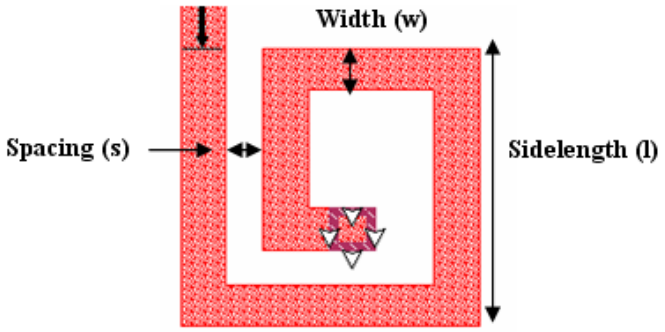

Figure 50. Layout of a spiral inductor in SONNET, depicting the different physical parameters.

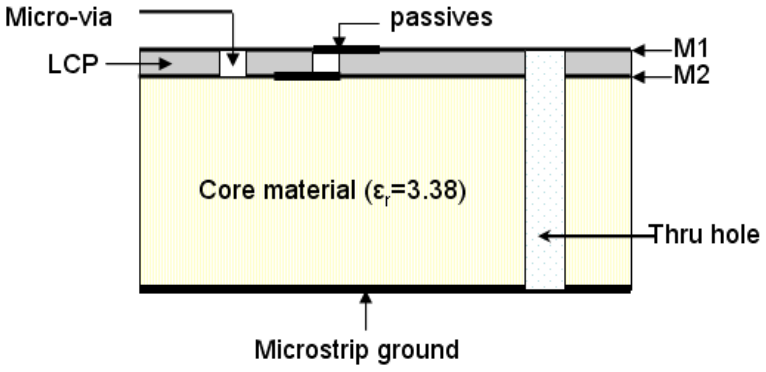

Figure 51. Cross-section used for the design of microstrip spiral inductors.

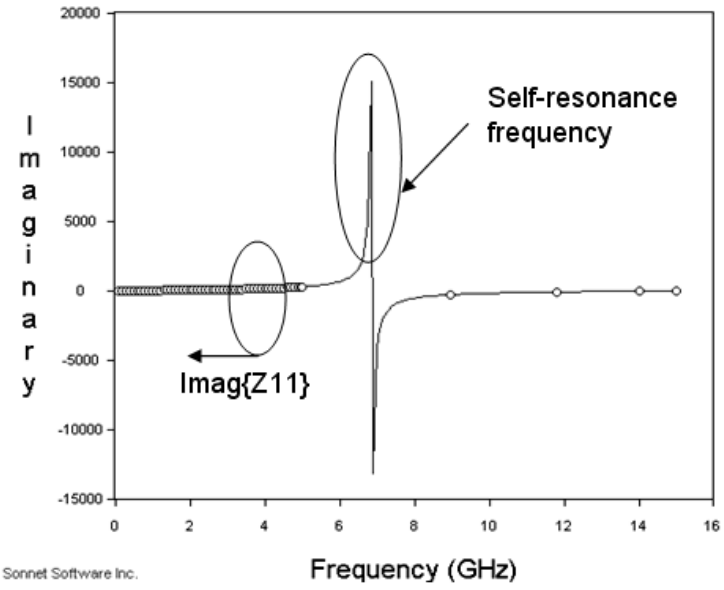

Figure 52. Depiction of the self-resonance frequency (SRF) of an inductor.

3.3.3 Adaptive data sampling

In this work, an initial library of 300 spiral and loop inductors, based on stripline and microstrip topology, respectively, were simulated using SONNET, a commercially available 2.5D full-wave method of moments (MoM)-based EM solver. The layout of an inductor in SONNET is shown in Figure 50. The cross-section used for microstrip design is shown in Figure 51, while the inductors with stripline topology have the cross-section shown in Figure 48. The inductance and quality factor were extracted from SONNET data as

$$L = \mathrm{Im}\{Z11\}/2\pi f, \tag{47}$$

and the quality factor (Q) is given by

$$Q = \mathrm{Im}\{Z11\}/\mathrm{Re}\{Z11\}. \tag{48}$$

The SRF was measured at the impedance transition frequency, as shown in Figure 53. For the training of the neural networks to "coarsely" map the input dataset to the output, eighty percent of the library was used. The remaining twenty percent of the inductor designs were used to test the neural networks. During testing, the mapping

accuracy was found to be worse than 10 percent. This is because, the number of data points (240) that was used for training the neurons was not sufficient to develop a mapping with the desired accuracy($< 3\%$). The inductor Q, area, L and SRF were represented as nonlinear functions of the inductor side-length, width and turns as shown below:

$$f = \sum_{k=1}^{M} b_{kj} g(\sum_{j=1}^{N} a_{ji} x_i + a_{oj}) + b_{ok}, \tag{49}$$

$$g(x) = (e^x + e^{-x})/(e^x - e^{-x}), \tag{50}$$

$$x = \{side\_length, width, turns, spacing\}$$

where, f represent Q, L, and SRF; b and a are the weights associated with the neural network, N represents the number of hidden neurons, M represents number of outputs and x is the regressor vector [80]. Practical ranges of design values (for wireless communication systems) were targeted during the library development. During the design of spiral inductor library from EM simulations, the number of turns varied from 0.75-1.75 in steps of 0.25. For each of these designs, the side-length was varied from 0.5-3.75 mm in steps of 0.25 mm and the width (w) from 0.075-0.225 mm in steps of 0.075 mm. It is to be noted that the orders of magnitude of various input and output parameter values of inductors are different. Therefore, a systematic preprocessing of training data called "scaling" is desirable for efficient neural-network training. The EM simulation data was normalized before being fed to the neural network. The data was scaled with respect to the maximum and minimum values of the data range for each electrical/geometrical parameter using a linear scaling technique as

$$x_{sc} = x^o_{\min} + [(x - x_{\min})(x^o_{\max} - x^o_{\min})]/(x_{\max} - x_{\min}), \tag{51}$$

where x_{sc}, x represent the normalized and denormalized values of the input data and $x^0_{max/min}$, $x_{max/min}$, represent the normalized and de-normalized maximum/minimum values of the data range for a particular parameter.

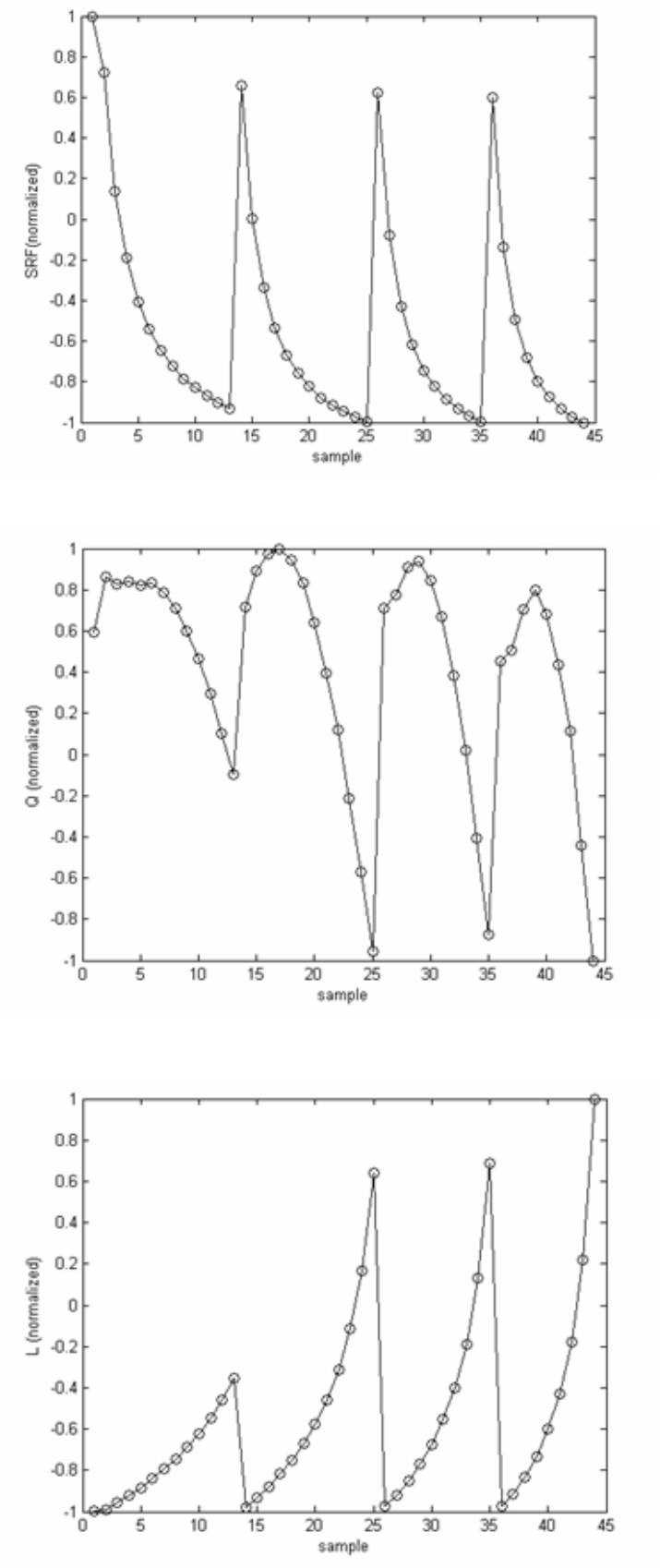

Figure 53. Correlation between modeled data and test data during forward mapping; (Top)-Inductance mapping, (Middle)-Quality factor mapping, and (Bottom)-SRF mapping.

The variations of the different electrical parameters for a section of the dataset are shown in Figure 53. There is a recurrent discontinuity in Figure 53. It should been seen that in Figure 53, there is *no* sample point in the region of discontinuity, rather sample points exist *only* in the smooth regions. The ANN-modeled plot for the training dataset looks the way it is because, the variation of parameters were taken for different widths of the inductor geometries. Every monotonic section of the curve represents geometry variations for a particular width.

During the training, the number of neurons in the hidden layers were manually adjusted so that the training error (the correlation between the neuro-modeled output and the training data) is neither too small (less than 2%), which hampers the generalization capability of the neuromodels nor too large (greater than 10%), which reduces mapping accuracy. As stated before, it was found that the size of the library was too small to provide an accuracy within 5% of the EM simulation data. Generation of the EM data, which is required for training of neural networks, is computationally expensive. Initially, MATLAB's inbuilt TrainLM neural network tool was used to train the neural models with limited EM data for forward mapping. The correlation between the EM data and the TrainLM-based neuromodel for 5 test data points is shown in Figure 54. Figure 54 show ANN-model to EM data correlation for two different training instants (with the same data). The large correlation error can be seen readily.

This problem was tackled by the following methods:

(a) EM modeling of pad and via structures

(b) Adaptive data sampling

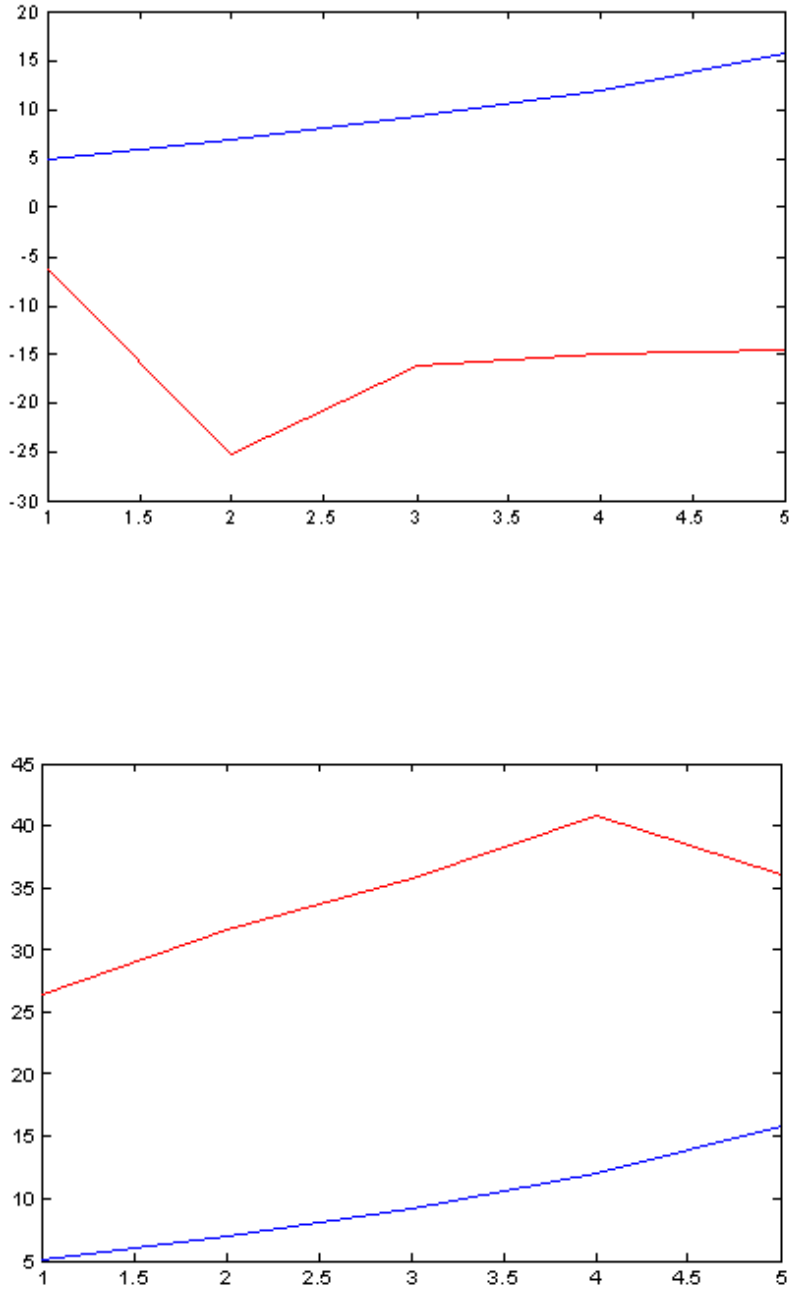

Figure 54. MATLAB TrainLM ANN-model to EM data correlation in forward mapping after training of ANN; Red graph is the TrainLM output for test data and Blue graph is the EM simulation result for test data. X- Axis is the test sample number; made continuous by interpolation. Figs (a),(b) represent two different training results for the same test data.

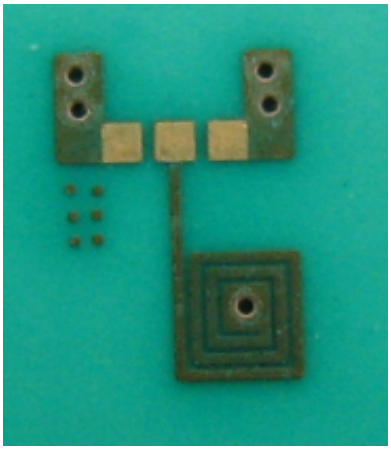

Figure 55. Photograph of the fabricated microstrip loop inductors.

3.3.3.1 EM modeling of probe-pads and vias

Significant discrepancies were observed between the inductance values obtained from the measurements and those obtained from the modeling results. A few such discrepancies in the inductance values have been listed in Table 1.

Table 1. Correlation between the measured data and neuromodeled data without including the effect of via and CPW pad models

Size (sq. mils)	Turns	L_meas(nH)	L_model(nH)	Freq(GHz)
30 × 22	1	1.49	1	1
54 × 30	1	3.18	2.5	4
45 × 45	2	4.86	5	1
60 × 62	3	12.77	15	1
39 × 12	1	1.63	1.1	4

The difference in the results was attributed, firstly, to the way in which the inductor/capacitor test samples were simulated in SONNET. An example simulation test structure (required for training data and test data) has been shown before in Figure 50. As shown in the figure, the EM simulations do not take into account, the effect of vias and probe pads. This is different from the fabricated test structures, as example of which is shown in Figure 55.

The test boards containing the inductors (and the filters) did not have de-embedding test structures. Therefore, the measurements took into account, the effect of vias and

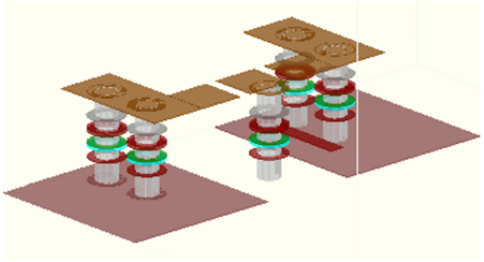

Figure 56. SONNET-based EM model for the CPW pads and thruhole vias for the microstrip inductor.

probe pads on the impedance/reactance profile of the inductors/capacitors. This problem was resolved by the development of separate models for the probe pads and the vias in SONNET. The EM models of the via pads and the thruhole structures has been illustrated in Figure 56.

The S-parameters of the model, shown in Figure 56, were augmented with the S-parameters of the inductors/capacitors. The improved hardware to model correlation has been tabulated in Table 2.

Table 2. Correlation between the measured data and the neuromodeled data after adding the EM models for vias and CPW pads of the spiral inductors

Size (sq. mils)	Turns	L_meas(nH)	L_model(nH)	Freq(GHz)
30 × 22	1	1.49	1.27	1
54 × 30	1	3.18	2.95	4
45 × 45	2	4.86	5.15	1
60 × 62	3	12.77	13.5	1
39 × 12	1	1.63	1.4	4

The difference in the modeling results (before and after EM modeling) in Table 1 and Table 2 underlines the need for via and probe-pad modeling.

3.3.3.2 Adaptive data sampling

To further improve the modeling accuracy of the neural networks, problem, the response surface analysis of the electrical parameters, as a function of geometry variations, was performed. For example, the response surface plots for inductance(L) and quality factor(Q) as a function of critical geometrical parameters are shown in Figure

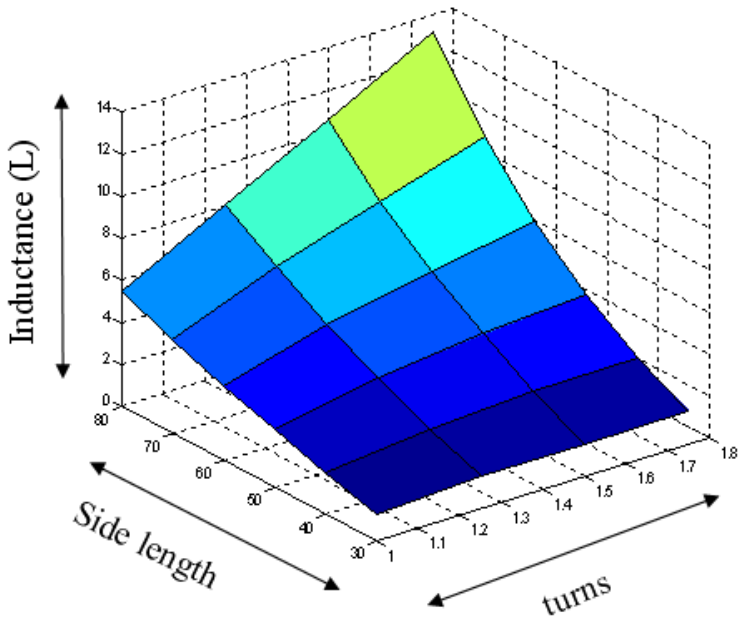

Figure 57. Response surface for the inductance(L) of the microstrip inductors.

57 and Figure 58, respectively.

It can be seen that the response surfaces are piecewise monotonic in nature. From the piecewise monotonicity, it can be inferred that more data points can be generated from the existing library based on separate interpolation of the "smooth" portions of the response surface. An adaptive sampling algorithm was implemented in the neural network structure and was used in conjunction with the training of the neural models. Based on the desired accuracy of the required Q, L, area and SRF (1-5%), the training dataset was sampled through interpolation to generate more data points (the final size of the library can be 10-15 times the size of the library developed from EM simulation). At each stage, the neural network was trained with the larger library size (than the previous stage) to improve mapping accuracy. For example, if a tolerance of 10% (around the desired value) is acceptable for a design, a step size of 0.30 turns (1.35 to 1.65) is sufficient, as tabulated in Table 3.

On the other hand, if a tolerance of 3% (around the desired value)is required for a design, a step size of 0.05 turns (1.55 to 1.6) is required, as tabulated in Table 4.

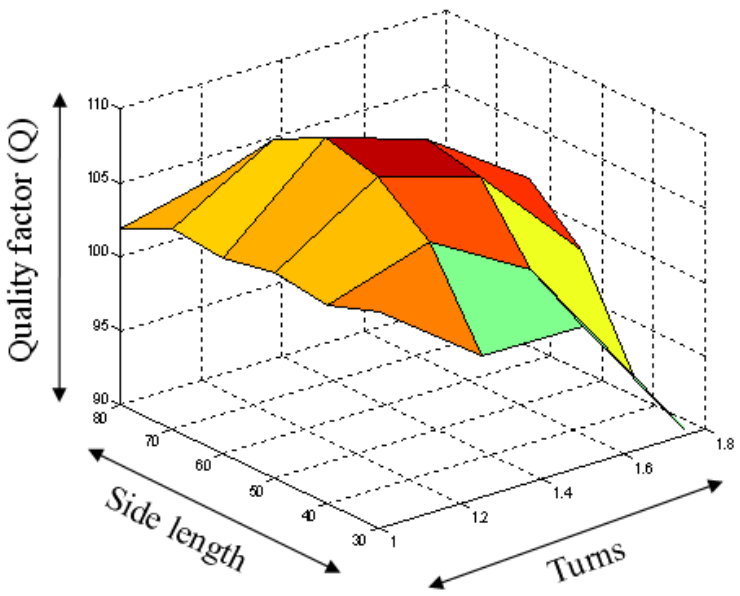

Figure 58. Response surface of the quality factor(Q) of the microstrip inductors.

Table 3. Variation in physical parameters for tolerance of 10% in Q

No. of turns	Side-length(mil)	Quality Factor	Inductance(nH)
1.35	91	99.23	11.88
1.35	92	98.65	12.17
1.65	79	99.56	11.79
1.65	80	98.69	12.14

Thirdly, if a 3% variation is required for both the inductance and quality factor is required, a step size of 0.05 and 1 is required for the number of turns and sidelengths, respectively. The results for forward mapping for 3% variation has been shown in Table 5.

The neuromodel was then used to forward map and reverse map between the electrical parameters and geometries. If the design-imposed accuracy of the component values was met, the training data interpolation was stopped. Otherwise, the training loop was iterated using interpolated data with smaller step size. The method works very well for monotonic variations of the data. The time-consuming part, however, was the generation of highly nonlinear data points. The neuromodels were then

Table 4. Variation in physical parameters for a tolerance of 3% in Q

No. of turns	Side-length(mil)	Quality Factor	Inductance(nH)
1.55	69	105.93	8.02
1.6	68	106.37	8.04
1.6	69	106.08	8.31
1.6	70	105.76	8.56

Table 5. Variation in the physical parameters for a 3% tolerance in Q and L

No. of turns	Side-length(mil)	Quality Factor	Inductance(nH)
1.35	94	97.07	12.75
1.35	95	96.06	13.06
1.35	96	94.86	13.36
1.4	91	96.86	12.67
1.4	92	96.84	12.97
1.4	93	96.65	13.27
1.5	87	93.32	12.83
1.55	85	93.33	12.79
1.6	83	95.68	12.66
1.6	84	94.51	13.02
1.6	85	93.29	13.29
1.65	82	96.76	12.87
1.65	83	95.71	13.24
1.7	80	95.73	12.77
1.7	81	94.89	13.05

checked for new test case values of side-lengths, line-widths and the number of turns for inductance calculations. The correlation between the modeled and EM data was within 5%. Figure 59 shows the correlation between the ANN-modeled data using the interpolation technique and EM simulation data for forward mapping using test data. The sampling technique allow for high mapping accuracy without resorting to extensive EM simulations. The nonlinear mapping approach is generic and can, therefore, be applied to different inductor topologies. The flowchart for the sampling algorithm is shown in Figure 60.

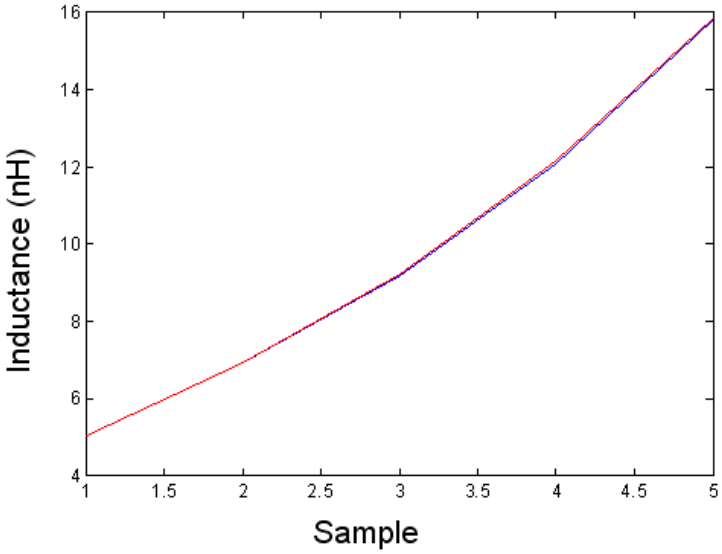

Figure 59. ANN-model to EM data correlation using interpolation for test data (same as that used in Figure 54); Red graph is the TrainLM output for test data and Blue graph is the EM simulation result for test data. X- Axis is the test sample number; made continuous by interpolation.

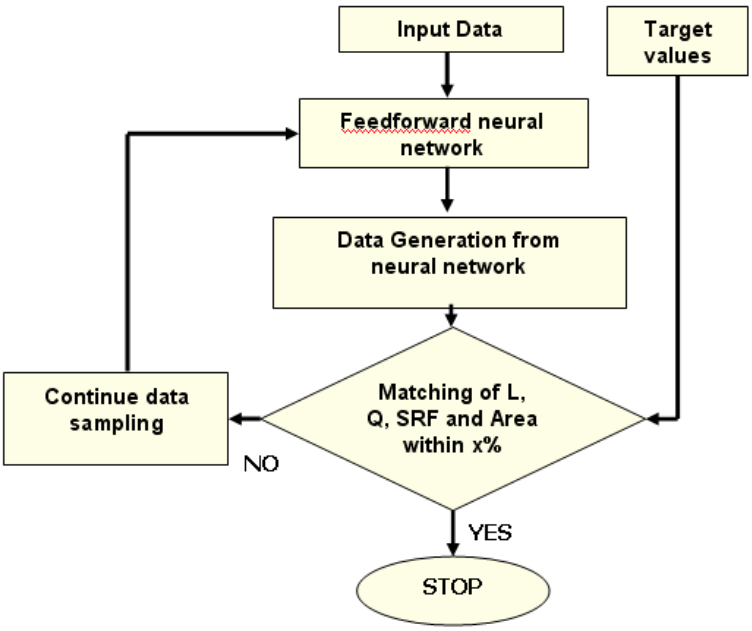

Figure 60. Flowchart for the adaptive data sampling algorithm.

3.3.4 Synthesis and design space exploration

Geometrical synthesis of inductors requires reverse mapping from the electrical specifications to geometries. The neuromodeled output provided multiple solutions of geometries for a given inductance and different values of Q and SRF. The concept is shown in Table 6. From a design perspective, the synthesized inductor geometry that meets the design specifications of SRF, area and L and has the maximum Q is the design that is to be selected. Mathematically, the optimization function can be written as:

$$Area < Area_{given}; SRF > SRF_{given}; maximize(Q)|_{L=L_0},$$

where $Area_{given}$ is the maximum area of the inductor allowed by a design and SRF_{given} is the minimum SRF required for the inductor in the design.

The design space exploration, leading to the synthesis of inductors, can be formulated as follows: Let the geometry dataset associated with the i^{th} inductor be

$$X^i = [x_1^i, x_2^i, ..., x_N^i]^T, \tag{52}$$

where N is the number of geometrical parameters associated with each inductor, and M is the number of inductors. The area of the inductor A^i can be obtained as a function of X^i as $A^i = \varphi(x^i)$ where $\varphi(\bullet)$ represents the geometrical mapping relationship. Let the dataset for Q, SRF, L and area (A) for the i^{th} inductor be given by

$$E^i = [Q^i, SRF^i, L,^i A^i]^T. \tag{53}$$

The neural network technique described earlier, has been used to develop weighted mapping functions to map X^i to E^i through the forward mapping procedure and E^i to X^i through the reverse mapping procedure. The algorithm for design space exploration can now be outlined as shown in Figure 61.

The geometries synthesized by reverse nonlinear mapping may not exactly be feasible for fabrication since the resolution of the process is 12.5 μm while the reversed

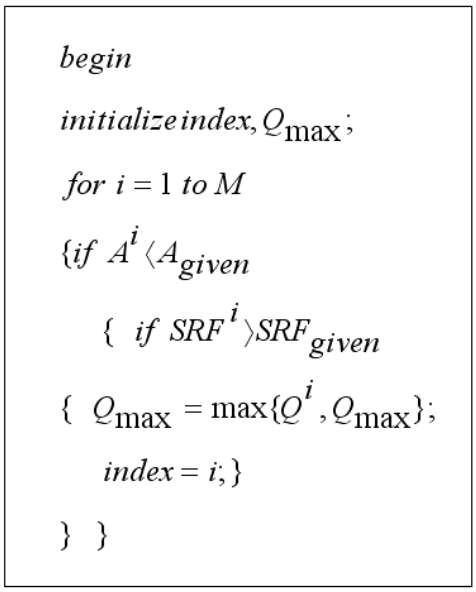

Figure 61. Algorithm for design space exploration.

mapped geometries can have higher decimal orders. In this case, the design values were rounded in accordance with the process rules with minimum error. For example, a current LCP-based fabrication process allows a minimum line width and line spacing of 75 μm. Synthesized designs gave 2-5 percent variation as compared to EM simulations. The Q and SRF variation with synthesized data for a 12.5 nH spiral microstrip inductor at 2.4 GHz is shown in Table 6.

Table 6. Synthesis results for a 12.5 nH (@2.4GHz) spiral inductor exhibiting Q, area and SRF tradeoffs (for a line spacing of 0.1 mm; 1mm=40 mils).

No.of turns	Side(mil)	Width(mil)	Q-value	L(nH)	SRF(GHz)
1.5	101	9	135	12.5	4.1
1.75	91	9	120	12.5	4.1
1.35	94	6	97	12.5	4.6
1.5	87	6	93	12.5	4.75
1	130	6	75	12.5	4.3
1.25	100	6	83	12.5	4.5
3.3	40	3	70	12.5	6.3
2.3	46	3	71	12.5	5.5
3.75	34	3	50	12.5	5.7

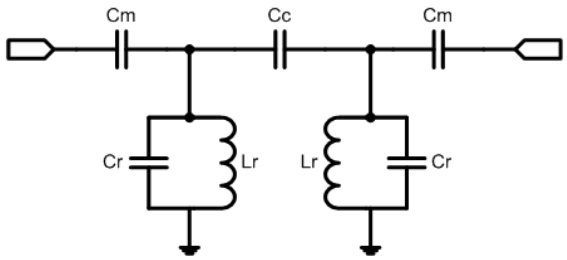

Figure 62. Ideal schematic for a second-order capacitively coupled bandpass filter.

The table clearly indicates the tradeoffs incurred in maximizing Q and minimizing area for the same inductance value of 12.5 nH (@ 2.4 GHz). Based on the design requirements, the designer can make a choice from multiple synthesized options that are shown in the table.

3.4 Layout-level sizing of RF bandpass filters

The development of library of embedded RF passives can also be extended to the scaling of RF circuits. Layout-level scaling of filters in the absence of extensive design templates to meet different frequency standards can significantly reduce the time required for EM simulations and redesign. Previous works have focused on efficient optimization techniques of a pre-designed layout. In contrast, this section of the chapter focuses on design reuse of filter layouts in LCP to enhance the circuit design libraries. In addition, the proposed methodology allows scalability of broadband circuit models for synthesizing layouts with different performance measures (bandwidth, center frequency, insertion loss etc.). The advantage lies in *minimizing* the number of layout template designed for a particular frequency specification and extracting layout-level parameters over a range of frequencies with *minimum* EM simulation data. The proposed technique described consists of multiple levels of abstraction and have been detailed in the following subsections.

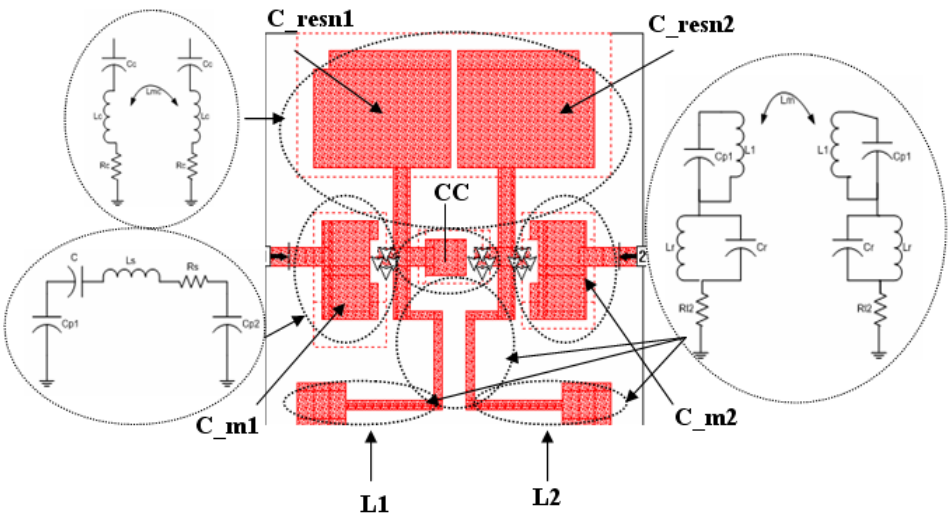

Figure 63. Lumped element modeling for segemented sections of the bandpass filter shown in Figure 62.

3.4.1 Lumped circuit modeling

The stages of the proposed layout-level sizing technique is best explained with the help of a circuit layout. A second-order, capacitively coupled, chebyshev bandpass filter was chosen as the topology to illustrate the underlying principle of design scaling. The ideal schematic of the filter is shown in Figure 62. It is a 3mm X 3mm X 1.5 mm 2-pole bandpass filter operating at a center frequency of 2.45 GHz and having a bandwidth of 300 MHz. The design stackup has two inner metal layers with top and bottom ground planes (not shown in the figure), which are 1.83 mm from each other. In Figure 63, the resonator capacitors C_{resn1}, C_{resn2} and L-resonator section L_{cp} have mutual coupling and was taken into account while segmenting the circuit. The layout was segmented into circuit sections which are isolated from each other without significant loss of accuracy. In Figure 63, the dotted lines represent the segmented sections. For example, the L-resonators were segmented into coupled section L_{cp}, and uncoupled sections L_1 and L_2. This segmentation approach allowed separate scaling and mapping of geometrical sections which have little electromagnetic interaction between them.

To develop *scalable* design libraries (Ls, Cs, filters etc.) using the neural networks, the development of broadband models for the library elements is imperative. In Chapter 2, an automatic, passive and broadband modeling technique, based on network augmentation, has been demonstrated. The methodology was validated by developing broadband, passive models for embedded RF spiral inductors and planar capacitors. This augmentation technique was then applied to the EM data of the layout segments to develop scalable broadband model for the entire filter layout. These broadband models were compared against the traditional narrowband 2-port and 1-port models of the passives (extracted in SONNET, at a particular frequency) to evaluate the computational effort for the broadband modeling. The advantage in using the augmentation technique is twofold

1 The augmented models for the segmented sections are broadband in nature, allowing for scalable design libraries

2 Large circuit layouts can be handled since time-consuming EM simulations for modeling the layout segments is minimized

The augmented lumped circuit models take into account the effect of parasitics and coupling. The schematics of the models for coupled L-resonator, matching capacitors C_{m1}, C_{m2}, center capacitor CC and coupled C_{resn1}, C_{resn2} are shown in Figure 63. The models showed very good correlation with EM simulation up to the second harmonic with a fundamental frequency of 2.45 GHz. Due to the use of segmented models, fast optimization at the circuit level was possible to meet the design specifications without losing the effects of physical layout on circuit performance.

The continuity of the reference ground plane in the circuit layout has a significant effect on the coupling between the resonator capacitors, which affects the bandwidth characteristics of the filter. In the layout, the lower plates of the two resonator capacitors were connected through a common ground plane. During lumped circuit

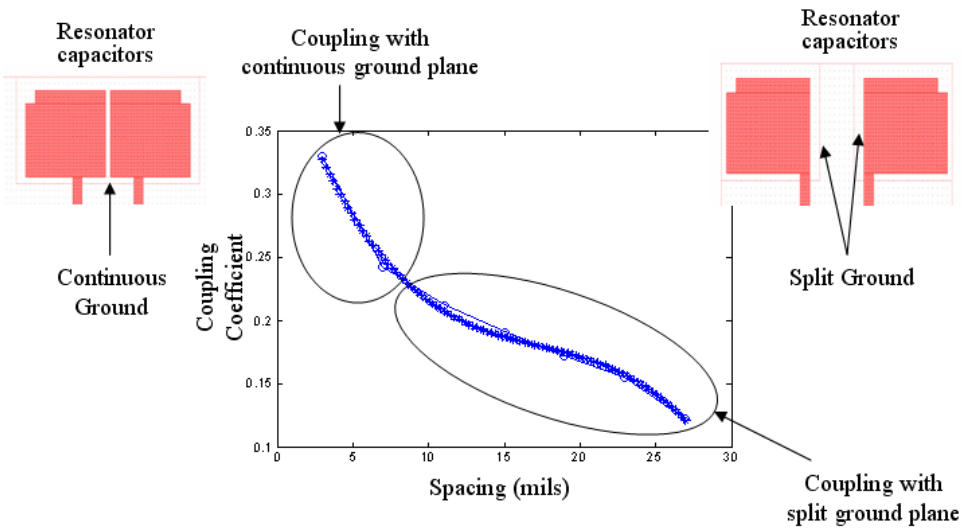

Figure 64. Mapping of reference ground plane of the resonator capacitors; separate polynomial functions are used for split and continuous ground plane coupling.

modeling, it was seen that the mutual coupling between the two resonator capacitors is not only a function of the size and spacing but also depends on the presence or absence of the ground plane. The difference in the coupling between the continuous and discontinuous ground planes is shown in Figure 64. In Figure 64, the spacing indicates the separation between the innerside edges of the top metal planes of the capacitors. Furthermore, the bottom plane has an overlay over the top plane to compensate for fringing capacitance. As a result, the bottom planes touch each other and become continuous at a point when the top planes are separated by a distance of 0.19 mm. Hence the coupling coefficient between the capacitors in the models will have different values based on continuous or split ground planes. This effect has been included in this work through piece-wise mapping of the coupling coefficients for continuous and discontinuous ground planes.

3.4.2 Sizing using model mapping

The broadband circuit models for the inductors and the capacitors were developed, using circuit augmentation. The circuit models, as explained in the previous sections take into account the effect of coupling, were developed based on the modeling

techniques developed by [10]. To allow scalability in the design libraries, models of the layout segments were made scalable, based on nonlinear polynomial mapping of the circuit model parameters to EM simulation data, using parametric simulations or ANNs.In its general form, the mapping can be mathematically formalized as follows:

Let the segmented component parameters (which include the parasitics) be represented by the vector as

$$\mathbf{C} = [C_1, C_2, ..., C_N]^T, \tag{54}$$

where N is the total number of model parameters. Here $\mathbf{C}$ consists of all the parameters in the circuit model which includes the ideal components and their parasitics. Let us assume that for a component $\mathbf{C}_j$, there exists a vector

$$\mathbf{g}_j = [g_{j1}, g_{j2}, ..., g_{jk}]^T, \tag{55}$$

where k is number of data points for which the solver was instructed to parameterize, for the particular parameter. Based on this data, nonlinear polynomial functions $\varphi_{ij}(\bullet)$ could be extracted for each of the geometrical sections to map to its corresponding component value in the model. This can be written as $\mathbf{C}_i = \varphi_{ij}(g_{ij})$. Therefore from the lumped circuit model component vector $[C_1, C_2, ..., C_k]^T$, the geometry mapping functions can be represented by

$$[\{\varphi_{1m}(g_{1m})\}, \{\varphi_{2m}(g_{2m})\}, ..., \{\varphi_{km}(g_{km})\}]^T, \tag{56}$$

where each vector $\varphi_{jm}(g_{jm})$ represents all the polynomial mapped geometries (equal to l^i) associated with the component $\mathbf{C}_i$ as

$$\overline{\varphi_i(g_i)} = [\{\varphi_{i1}(g_{i1})\}, \{\varphi_{i2}(g_{i2})\}, ..., \{\varphi_{il^i}(g_{il^i})\}]^T. \tag{57}$$

Here l^i is the number of geometrical parameters associated with $\mathbf{C}_i$. The circuit-level optimization parameters in the entire model is a subset of the entire model parameter $\mathbf{C}$ and is given by $[C_1, C_2, ..., C_s]^T$. All the optimization parameters in the

model, therefore, have mapping relations to its geometries given by

$$[\{\varphi_{1m}(g_{1m})\}, \{\varphi_{2m}(g_{2m})\}, ..., \{\varphi_{sm}(g_{sm})\}]^T, \tag{58}$$

In Equation 58, s is the number of variables selected for optimization. The next stage was to have mapping functions that correlate the component values to its *parasitics*. Let the mapping functions for this relation be given by $\phi_i(\bullet)$, where

$$C_i^p = \phi_i(C_i^c), \tag{59}$$

In Equation 59, C_i^p represents the parasitic associated with C_i^c and also,

$$C_i^p \bigcup C_i^c = \mathbf{C}, \tag{60}$$

where $\mathbf{C}$ is the entire model parameter vector, and $\bigcup$ represents the union operation. In conventional simulation methods, the component set $\mathbf{C}$ is the input, from which certain variables are selected for optimization. In this work, the vector $[C_s^c, \phi(C_s^c)]^T$ is used in the optimization routine where 's' is the number of parameters selected for optimization. At each step of the optimization of C_s^c, the parasitics also get updated through $\phi(C_s^c)$ in the simulation framework. As a result, the final optimized component values take into account, the associated parasitics. Mathematically, the j^{th} geometrical parameter of the i^{th} component value C_i could be extracted as shown

$$g_{i_{opt}}^* = \varphi_{im}^{-1}(C_{im}^*) \tag{61}$$

where $g_{i_{opt}}^*$ is the optimized m^{th} geometrical parameter corresponding to the optimized component C_i^* .

From the theory explained in this section, it is important to note that the reverse mapping was made under the premise that the mapping function $\varphi(\bullet)$ remains practically unchanged over the frequency range in which the reference layout was scaled. This holds true since the method described involves scaling of a reference layout within +/-20% of its center frequency with 0.5-5% tunability in bandwidth.

Three-dimensional EM simulations using Ansoft's HFSS and SONNET over the entire frequency range of scaling have verified that the mapping functions remain unchanged. The above methodology is best explained with the help of the layout of a bandpass filter, as shown in Figure 63. In Figure 63, the uncoupled inductor section in the lower half of the right lumped inductor model with shunt capacitor C_r and series resistance R_{12} were mapped to the inductor geometry as:

$$L_r = 0.0024(\Delta L)^3 + 0.0273(\Delta L)^2 + 0.0674(\Delta L) + 0.8104 \tag{62}$$

$$C_r = -0.0009(\Delta L)^3 + 0.0051(\Delta L)^2 - 0.0009(\Delta L) + 0.023 \tag{63}$$

$$R_{12} = 0.0007(\Delta L)^3 + 0.111(\Delta L)^2 + 0.1082(\Delta L) + 0.0942 \tag{64}$$

where ΔL is the increment in the inductor length of L_1 and L_2 for a fixed inductance of 0.8 nH. Similar mappings were obtained for all the other circuit models. The scalable models with parasitics were combined to perform filter circuit optimization using Agilent's Advanced Design System (ADS). The values of the components obtained from scaling and those obtained by simulating the designs in the EM solver (SONNET) are shown in Table 7.

Table 7. Comparison of the component values for three scaling test cases based on 2.45 GHz reference layout; correlation of EM simulation (Full-wave) data with the data obtained from the polynomial mapped model (poly).

Center Freq(GHz)		C_m1(pF)	CC(pF)	C_resn1(pF)	L_resn1(nH)
2.2	poly	0.451	0.11	1.80	1.76
full-wave		0.445	0.106	1.82	1.79
2.45	poly	0.50	0.16	1.80	1.64
full-wave		0.48	0.164	1.82	1.652
2.85	poly	0.355	0.065	1.06	1.06
full-wave		0.36	0.055	1.064	1.79

At each stage of the optimization process, the desired components were tuned and the corresponding polynomial-mapped geometries and parasitics were updated as well. For example, after optimization, the length (ΔL) and the spacing (ΔS) of

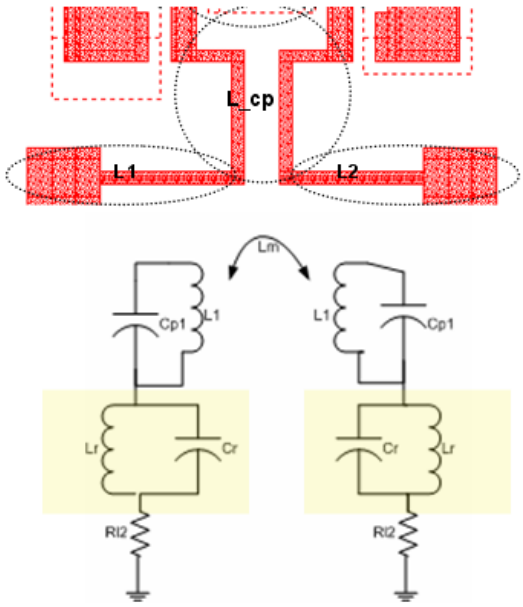

Figure 65. Scaling of segmented layout parameters from optimized lumped circuit models; an example has been shown for the coupled inductor section of the bandpass filter in Figure 63.

the inductors, as well as the width (ΔW) of the capacitors, illustrated in the previous example, was reverse mapped from the component parameters as shown

$$\Delta L = 0.039(L_r)^3 + 0.982(L_r)^2 - 0.0674(Lr) + 0.6104 \tag{65}$$

$$\Delta S = 0.0231(C_r)^3 + 0.051(C_r)^2 - 0.0012(C_r) + 0.032 \tag{66}$$

$$\Delta W = -0.0009(k)^3 + 0.351(k)^2 - 0.013(k) + 0.0123 \tag{67}$$

The scaling of the inductor section, explained before, has been illustrated in Figure 65. The values of the components obtained from scaling, and those obtained by simulating the designs in the EM solver are shown in Table 2. The flowchart for the optimization and scaling methodology is shown in Figure 66.

Table 2 shows that the component values obtained from optimization are within 2-5% of the EM simulation using the scaled geometries. The simulated results for the reference layout are shown in Figure 67. Based on different design specifications, the reference layout was scaled to a design at 2.2GHz with a bandwidth of 325 MHz and

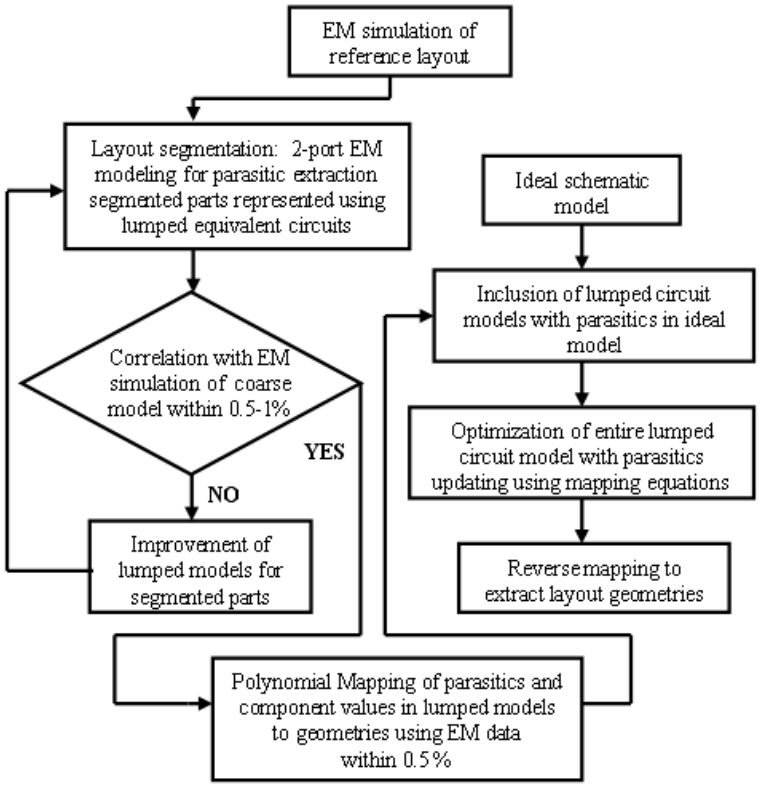

Figure 66. Flowchart for optimization and layout-level sizing methodology.

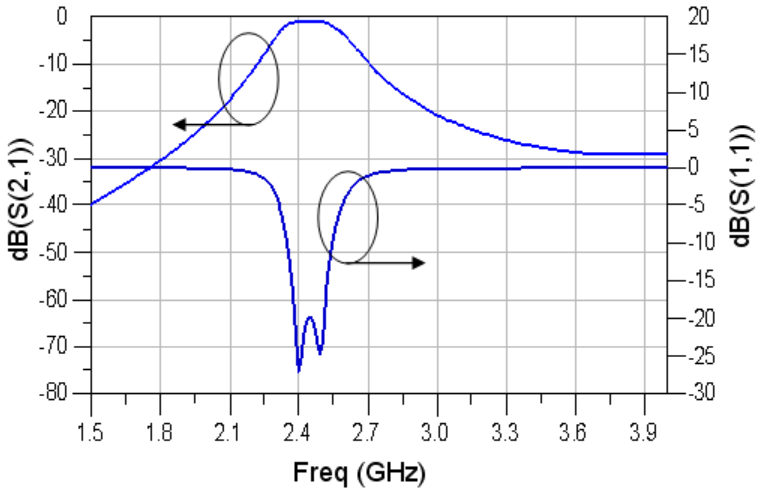

Figure 67. S-parameters of the reference design (2.45 GHz bandpass filter).

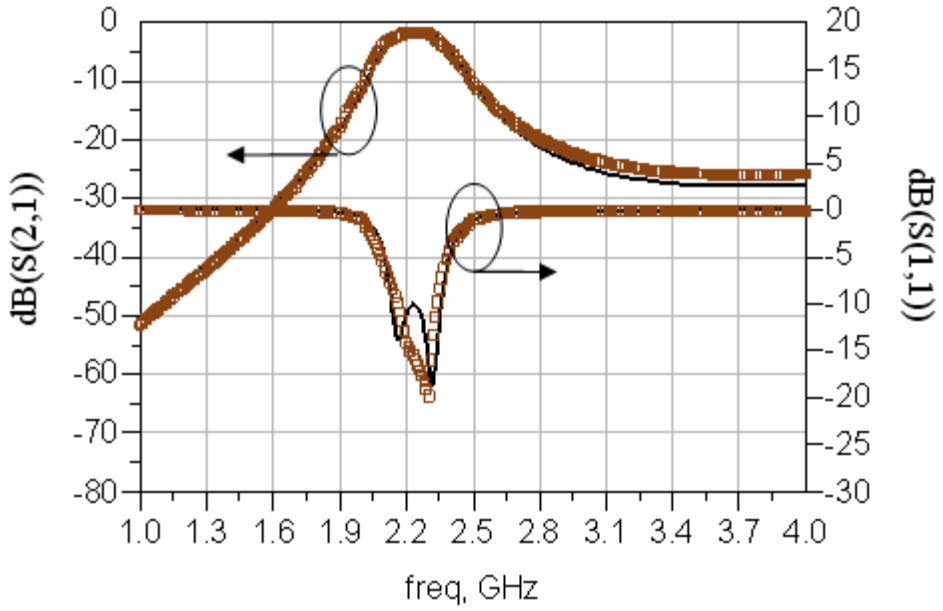

Figure 68. Correlation between full-wave data (sampled) and data from scaling methodology (solid) for a 2.2 GHz RF bandpass filter.

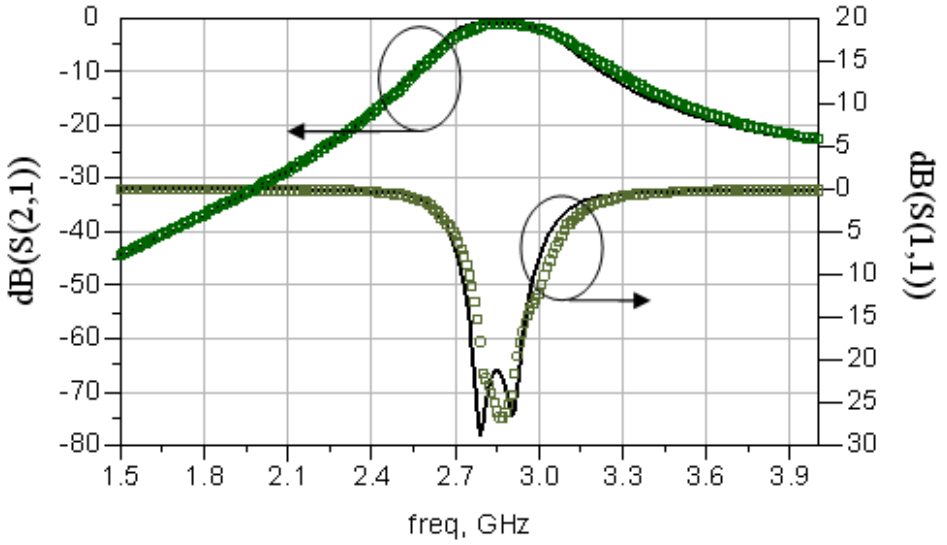

Figure 69. Correlation between full-wave data (sampled) and data from scaling methodology (solid) for a 2.8 GHz RF bandpass filter.

to another filter with a center frequency of 2.85 GHz and a bandwidth of 400 MHz. The S-parameters of the data from scaling techniqes, and that from the EM solver shows good correlation. Figure 68 shows the EM to model correlation for a scaled 2.2 GHz bandpass filter. Figure 69 shows the EM to model correlation for a scaled 2.8 GHz bandpass filter.

3.4.3 Correlation of scaled model with EM simulation

A detailed analysis of the S-parameters of the extensive lumped circuit models and that obtained from the EM data by using the scaled geometries (shown in Figures 67,68,69) showed that while S21 had very good correlation, the S11 results had some discrepancy. This can be explained as follows. The return loss characteristic (S11) is predominantly a function of the matching capacitors in the filter. It can be seen in the layout, that the segmented sections of these capacitors along with the central capacitors include the vias that were used in the design.

In other words, separate via models were not used as part of the design sizing. As a result, the mapping functions for the capacitor geometries and its component values required to be of higher order than what was used in the design for capturing the nonlinearities, introduced due to the vias. The argument is supported by the fact that no such discrepancies were seen in the S21 characteristic. This is because the resonator inductors and capacitors, which predominantly affect the passband characteristic, did not have any vias in their structures.

3.4.4 Additional test cases

The layout sizing method discussed was applied to bandpass filters across frequencies and topologies. Reference layouts of filters at different frequency bands and with transmission zeros were designed and scaled to different frequency specifications. The results of layout sizing have been discussed in the following subsections.

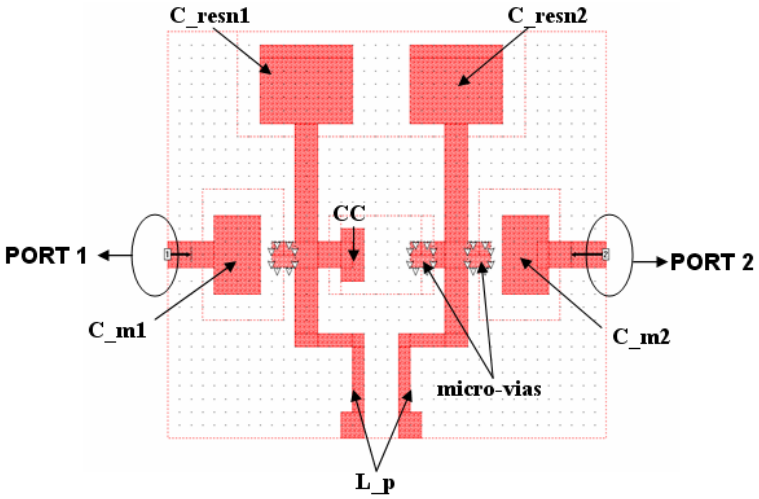

Figure 70. Layout of a second order, capacitively coupled 5.5 GHz bandpass filter in SONNET.

3.4.4.1 5.5 GHz bandpass filter scaling

The scaling methodology was applied to a capacitively coupled resonator bandpass filter with a center frequency of 5.5 GHz and a bandwidth of 750 MHz. The cross section of the layout is the same as that for the filter shown in Figure 63. The filter has a lateral dimension of 2.3 mm X 2.3 mm. The layout of the filter is shown in Figure 70. The filter has the same topology as the 2.45 GHz filter, shown in Figure 67. Consequently, a similar segmentation procedure was applied to the layout. For correcting the discrepancies due to via effects, which are prominent at higher frequencies, higher order mapping functions were used for the center as well as the matching capacitors. For example, the matching capacitor C_{m1} in the layout in Figure 63 with parameters C_{p1}, C_{p2} and C were mapped to its length increment of the capacitor plates from EM simulation data by 4^{th} order polynomial functions as

$$C_{p1} = 0.0079(W)^4 + 0.00691(W)^3 - 0.071(W)^2 - 0.069(W) + 0.0111 \quad (68)$$

$$C_{p2} = 0.0068(W)^4 + 0.0051(W)^3 - 0.056(W)^2 - 0.041(W) + 0.031 \quad (69)$$

$$C = 0.012(W)^4 + 0.0111(W)^3 - 0.0168(W)^2 + 0.061(w) + 0.0491 \quad (70)$$

The improvement can be clearly seen in the S-parameters shown in Figure 71.

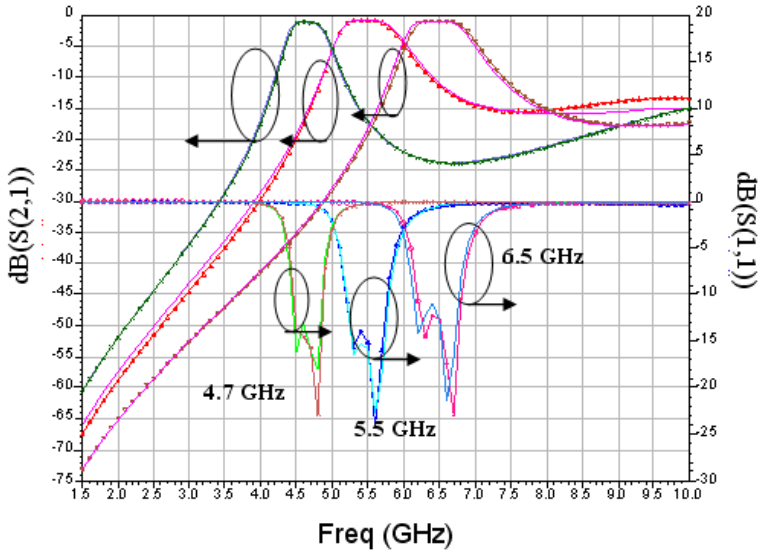

Figure 71. Correlation between full-wave data (triangular) and data from scaling (solid) for filters centered at 4.7 and 6.5 GHz based on coarse data of 5.5 GHz filter, shown in the middle.

From the figure, it is clear that S11 has a better correlation between the scaled models and the EM simulation due to the use of higher order polynomial fitting. The poles of the filter have also been captured in the scaled layout. The reference layout has been scaled to a filter at 4.7 GHz with a bandwidth of 550 MHz, and another filter at 6.5GHz with a bandwidth of 750 MHz. The component values are within 3-5% to that obtained from EM simulations. The circuit-level optimization took 5 minutes on DELL PC with 2.8 GHz Pentium IV processor and 1 GB RAM. EM simulations in SONNET of each segmented part with geometrical variation took on an average of 10 seconds per frequency point with a cell size of 3 mils $\times$ 3 mils. Table 8 shows the comparison of component values for three scaling test cases - between polynomial mapped model and full-wave EM simulation.

Results in Table 8 show that the use of fourth order models gave better correlation with EM data compared to the third order models in the first design.

Table 8. Comparison of component values for three scaling test cases; between polynomial mapped model (poly) and full-wave EM simulation (full-wave).

Center Freq(GHz)		C_m1(pF)	CC(pF)	C_resn1(pF)	L_p(nH)
4.7	poly	0.411	0.072	1.12	1.22
	full-wave	0.393	0.068	1.15	1.25
5.5	poly	0.350	0.061	0.98	0.96
	full-wave	0.371	0.057	1.06	1.04
6.5	poly	0.260	0.051	0.84	0.90
	full-wave	0.272	0.050	0.89	0.95

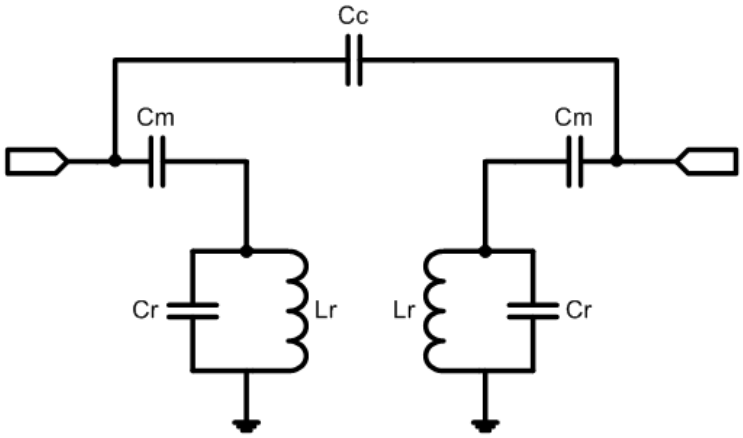

Figure 72. Ideal circuit schematic of the inductively coupled resonator filter.

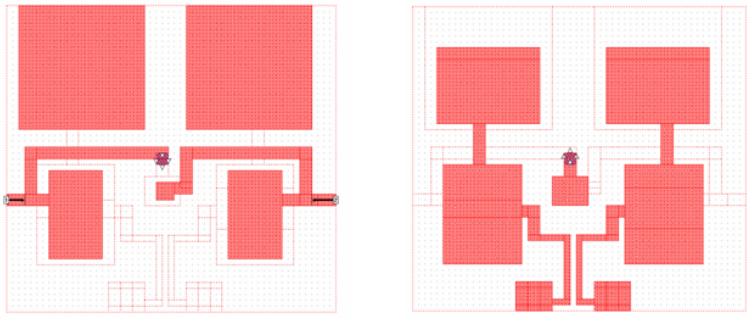

Figure 73. Layout of the filter (with transmission zeros) in multi-layer LCP-based substrate; (Top)-top plane, and (Bottom)- bottom plane of the filter structure.

3.4.4.2 Filter with transmission zeros

The scaling method was applied to a different filter topology. The filter shown in Figure 72 is an inductively coupled resonator bandpass filter. The feedback capacitor C_{12}, and the inductively coupled resonators provide multiple signal paths between the input and output, that are out of phase, resulting in the transmission zeros. The transmission zeros in the design allows controllability of the stopband attenuation and rejection at specific frequencies. The layout of the filter is shown in Figure 73. The layout has a lateral dimension of 3.9 mm $\times$ 4.1 mm. The cross section for the layout is same as that shown in Figure 48. The spacing between the inductors, which controls the inductive coupling in this design is an important design parameter. Further, during EM modeling, the inductive lines on the lower plane were also segmented. The top and bottom metal layers of the layout are shown in Figure 73. The EM simulation results from the scaled geometries is shown in Figure 74. The scaled model response was within 2-5 percent of EM simulations. It should be understood, however, that the segmented lumped element technique which was seen to work very well for 2 metal layer designs (considering the number of layers in which the passives are embedded), will have problems with multi-layer designs (no. of metal layers $>$ 3). This was realized in modeling the inductor coupling for the filter in Figure 73. This is due to the electromagnetic coupling between multiple metal layers which is not accurately captured by lumped models.

3.4.4.3 Dual-band filter

In the design of dual band filters, if the frequency bands are further away than the scalability of each frequency band, then separate mapping functions need to be used for the two filters. An ideal schematic of a dualband filter with operating center frequencies at 2.3 GHz and 4.25 GHz have been shown in Figure 75. Let the entire lumped circuit model vector for each of the two filters be defined by C^1 and C^2, where the vectors are similar to that in Equation 54. Let, for the components for

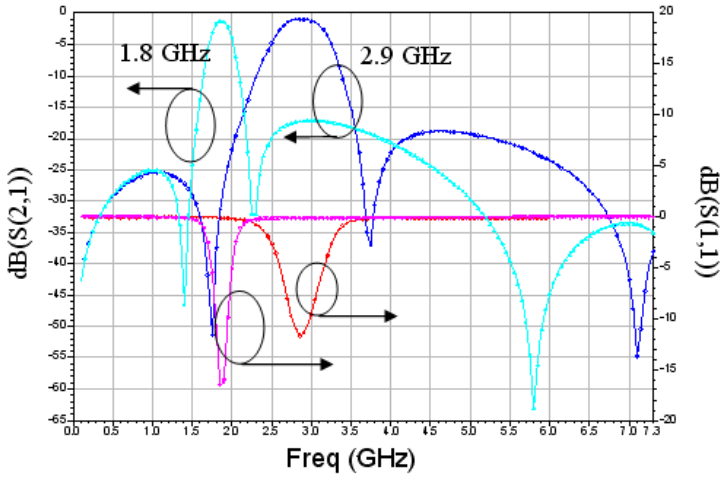

Figure 74. S-parameters of the reference and scaled filters; cyan represents the reference design (1.8 GHz) and blue represents the scaled design(2.9 GHz).

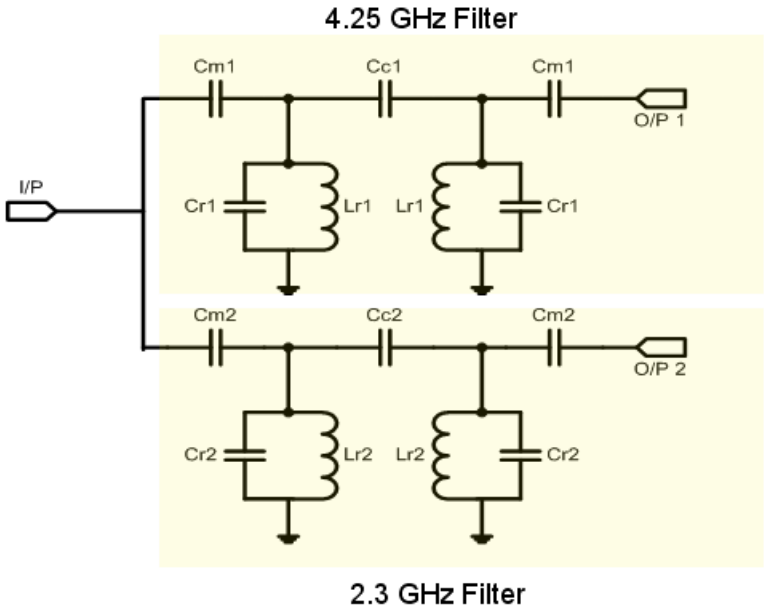

Figure 75. Ideal schematic of the 2.3 GHz and 4.25 GHz dual-band filter.

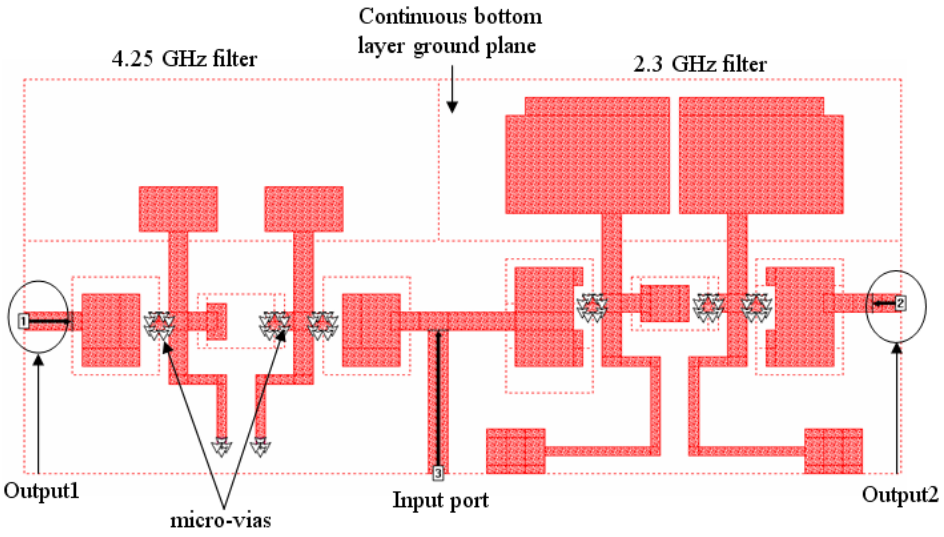

Figure 76. Layout of the 2.3 GHz and 4.25 GHz dual-band filter.

the first filter C^1, φ^1 represent the polynomials for mapping the model parameters to geometries, and ϕ^1 represent the mapping of the ideal component values to their parasitics. Similar relations hold for C^2 (in terms of φ^2 and ϕ^2). Therefore, in the circuit level optimization of a dual-band design, the vector of parameters that is optimized is given by

$$\mathbf{C}_{1,2} = [C_{s1}^{1c}, \phi^1(C_{s1}^{1c}), C_{s2}^{2c}, \phi^2(C_{s2}^{2c})]^T, \tag{71}$$

where $\mathbf{C}_{1,2}$ represents the components of the whole filter to be optimized; and '$s1$', '$s2$' are the number of components in each filter to be optimized. The geometries for the design are extracted, which is similar to Equation 61 for a single band design as

$$g_{1i_{opt}}^* = (\varphi^1)_{i1}^{-1}(C_i^{1*}), \tag{72}$$

$$g_{2i_{opt}}^* = (\varphi^2)_{i2}^{-1}(C_i^{2*}), \tag{73}$$

where g_{1i}^*, g_{2i}^*, represent the extracted geometries for the two bandpass filters.

The layout of the dual-band filter is shown in Figure 76. The design consists of two single band filters that were scaled from the 2.45 GHz and 5.5 GHz reference layouts. The circuit model of the dual band design was optimized to meet matching conditions

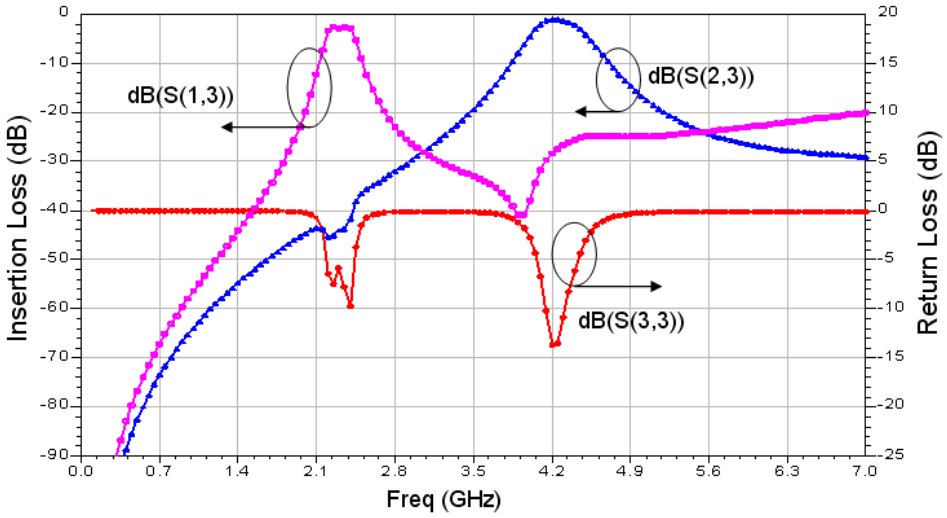

Figure 77. S-parameters of the dualband filter.

and reverse mapped to obtain the physical parameters of the dual-band filter layout. The design has a lateral dimension of 6.8 mm × 3.3mm with a cross section shown in Figure 48. The EM simulation results with the scaled geometries for the dual band filter are shown in Figure 77. It consists of two band pass responses centered at 2.3 GHz and 4.25 GHz with bandwidths of 250 MHz and 300 MHz respectively. Scaled design layout have a tunability of +/- 20 % with respect to center frequency with a bandwidth tunability of 0.5-5%. This was expected since the single band designs, from which the dual band filter is designed had similar scalability and tunability in terms of the center frequency and bandwidth.

3.5 Augmentation for model tuning

The optimization scheme employed in the previous sections for the scaling of bandpass filters is nonlinear in nature, and therefore more time-consuming. To improve the efficiency of the layout sizing scheme, a linear optimization-based tuning technique has been proposed in this section. This technique is based on the augmentation methodology explained in Chapter 2. As explained in Chapter 1, the layouts of the components are chosen from pre-designed libraries. In case of new designs, the

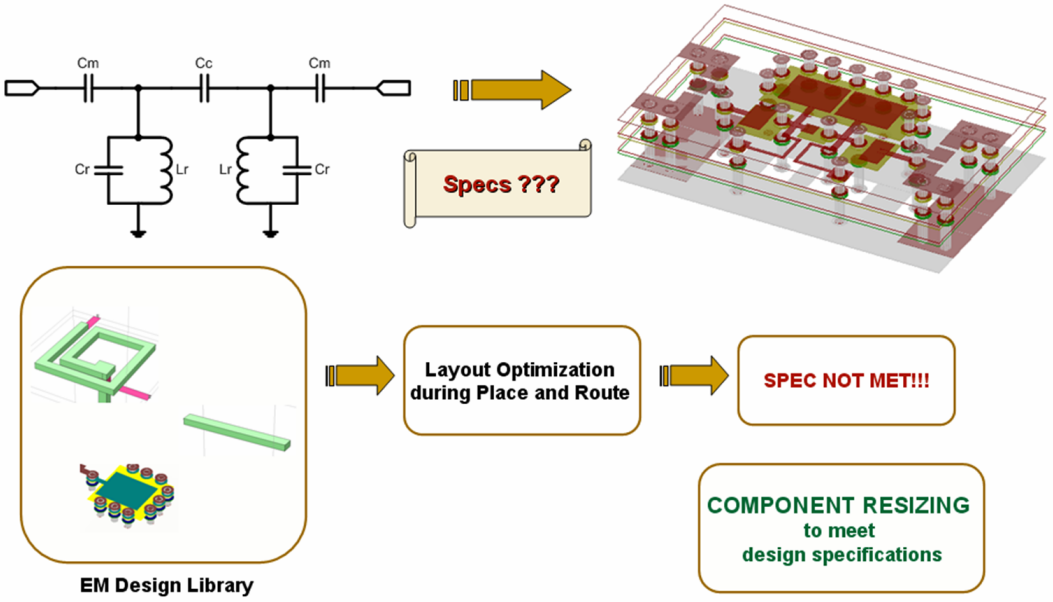

Figure 78. High-level description for the tuning requirement in RF circuits.

design flow usually begins by choosing individual components from the predesigned library. In many cases, the design values for the circuit components do not *exactly* match with that of the library components. In this case, the component with the closet value is chosen and its geometries are varied so that the required component specs are met. Full-wave EM solvers are typically employed for the tuning of layouts. Furthermore, when the layout components are connected via interconnects at a later stage of the design flow, the interconnects add to the inductance, resistance and parasitic capacitance of the overall circuit [9]. However, unlike broadband modeling of components, during circuit tuning, the circuit's frequency response needs to be satisfied at only discrete and/or narrow band(s) of frequencies. Conventionally, the circuit response is modified and manual EM iterations are required again to restore the design specifications at the overall layout level. The aforementioned problem is illustrated in Figure 78.

To address this sizing problem, the augmentation technique was applied to add *tuning* elements to the existing broadband models in the previous section. The broadband models for the components of the design library constitute the initial model for

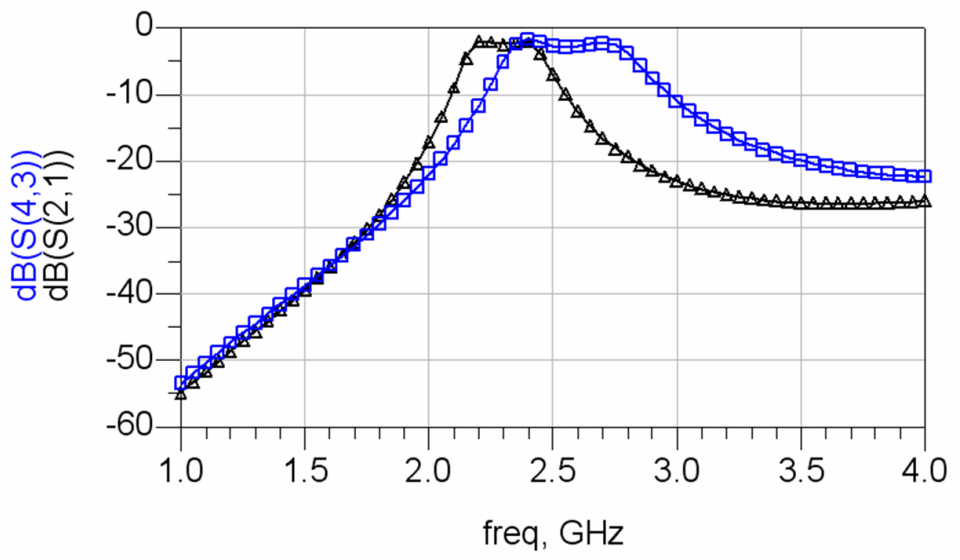

Figure 79. Comparison of the S-parameters obtained from the connected broadband model (data symbol:square), and that obtained from the EM simulation of the complete filter layout in SONNET (data symbol:traingle).

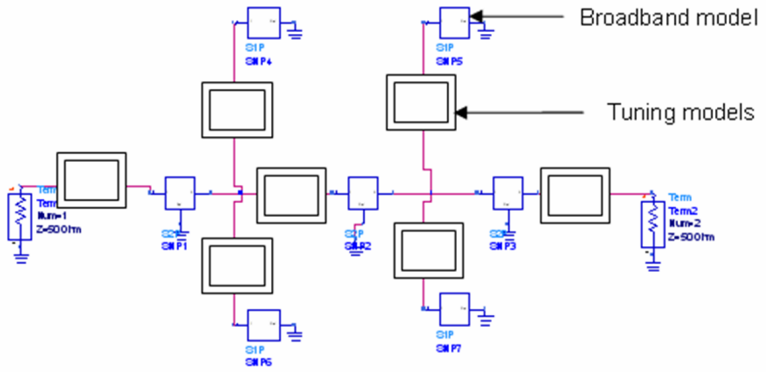

Figure 80. Simulation setup for the tuning of the bandpass filter.

the filter. However, as explained before, the response of the filter changes due to the addition of interconnects, required to physically connect the broadband models of the passive components. The goal is to meet the frequency response of an RF bandpass filter at specified frequency points. The difference in the S-parameters obtained, by appropriately connecting (through netlists, without any physical interconnects) the broadband models of the filter components, and the desired response is shown in Figure 79. The setup of the broadband models, with the tuning elements, for the entire filter has been depicted in Figure 80. The results after applying the augmentation

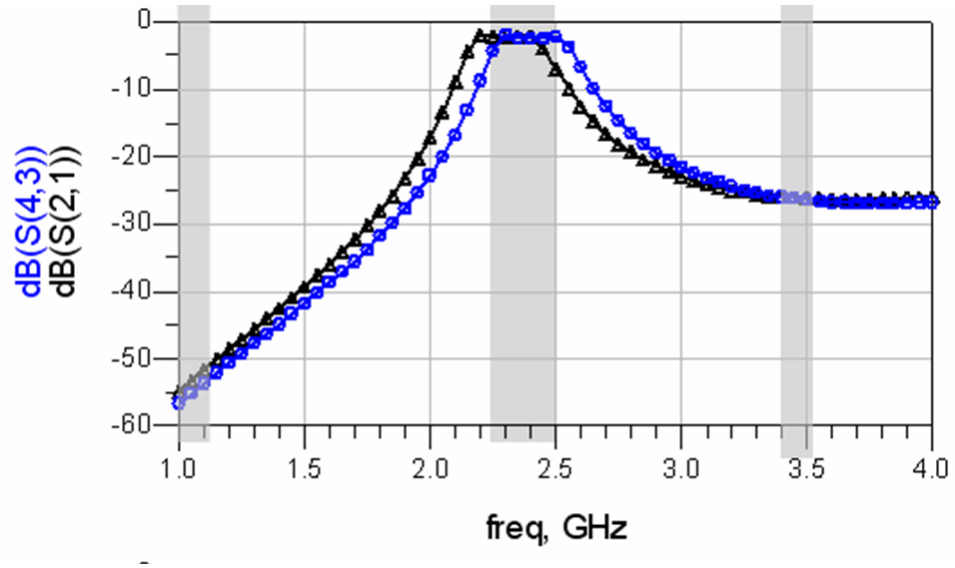

Figure 81. Comparison of the S-parameters obtained from the tunable broadband model, and that obtained from the EM simulation of the complete filter layout in SONNET; the frequency points where the specifications need to be satisfied are shaded in gray.

methodology, for tuning, are shown in Figure 81. The augmented models, after the addition of tuning elements, for inductors and matching, resonator and center capacitors, are shown in Figures 82 and 83, respectively. Since the two resonator capacitors and the two matching capacitors are identical, only one tuned augmented model has been shown for each of the same.

After adding the tuning elements, the port-to-port Z(or Y)-parameters can be obtained to find the equivalent inductance/capacitance, the resistive loss and the parasitic capacitance/inductance of the passive being modeled. At this stage, the designer can look into the ANN-based design library to obtain the component with the required electrical parameters (values of inductance, loss, parasitics etc.). Further, the tuned model can be added to the existing library of broadband models to increase the size of the model library, thereby reducing the number of iterations for future designs.

To compare the results with ADS (employing non-linear optimization schemes), the broadband model blocks in Figure 80 were replaced with S-parameter blocks,

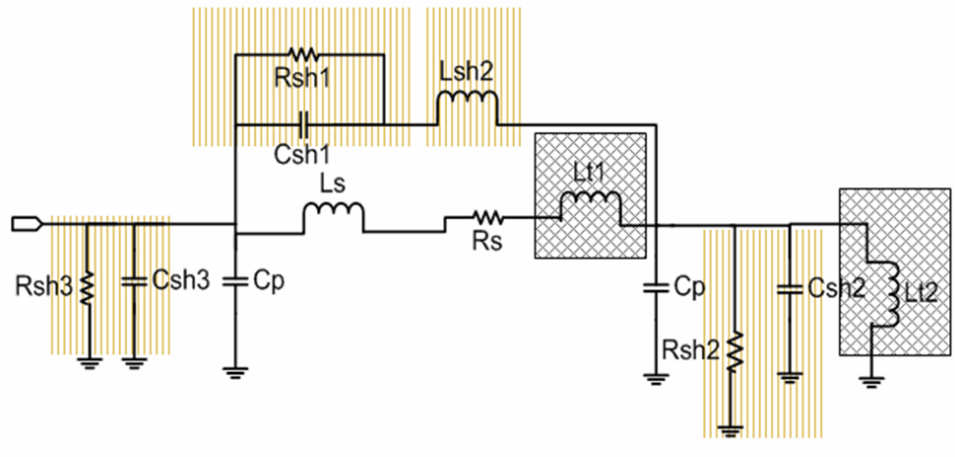

Figure 82. Tuned broadband model of the spiral inductor; the elements added during broadband modeling is shown by vertical-lined boxes, and the tuning elements have been shown by the hatch-lined boxes;Lsh2=6.8 nH, Csh1=1.2 pF, Rsh1=2.6 ohm, Csh2=Csh3=0.22 pF, Rsh2=Rsh3=44 ohm, Lt1=0.43 nH, Lt2=4.45 nH

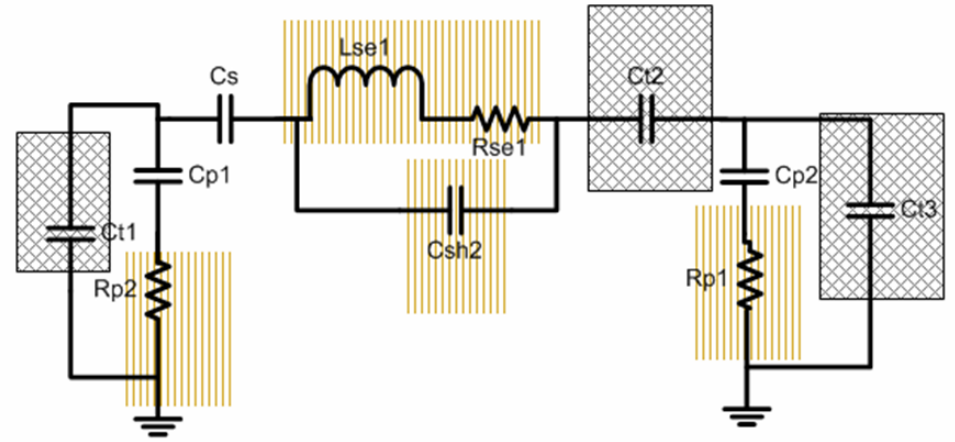

Figure 83. Tuned broadband model of the planar resonator capacitor; the elements added during broadband modeling is shown by vertical-lined boxes, and the tuning elements have been shown by the hatch-lined boxes; Lse1=0.4 nH, Rse1=1.2 ohm, Rp1=Rp2=4.6 ohm, Ct2=5.87 pF, Ct1=Ct3=0.78 pF

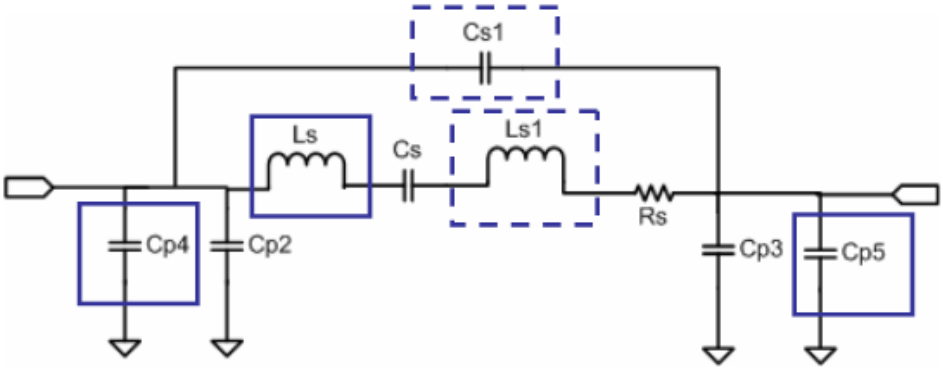

Figure 84. Tuned broadband model of the planar matching capacitors; the elements added during broadband modeling is shown by solid-lined boxes, and the tuning elements have been shown by the dotted-lined boxes; Cs1=0.49 pF, Ls=0.65 nH, Rs=2.3 ohm, Ls1=0.22 nH, Cp4=Cp5=0.85 pF

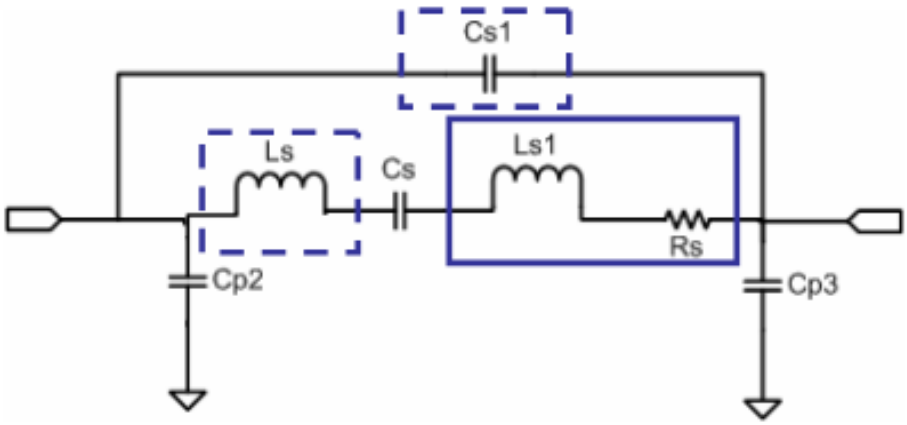

Figure 85. Tuned broadband model of the planar center capacitor; the elements added during broadband modeling is shown by solid-lined boxes, and the tuning elements have been shown by the dotted-lined boxes; Cs1=0.13 pF, Ls=0.2 nH, Ls1=0.31 nH, Rs=4.4 ohm

corresponding to the individual layout components. As before, shunt and series tuning elements were added to match the desired response. The comparison of the S-parameters after optimization of the tuning elements are shown in Figures 86 and 87. It should be noted, that the results are, to some extent, sensitive to the choice

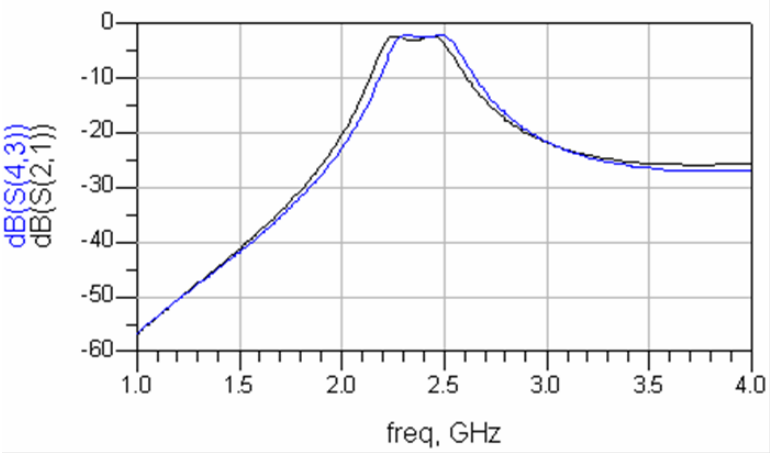

Figure 86. Comparison of the S21-parameters obtained from the augmentation-based technique(corresponds to the response that is shifted to the right) and that obtained from nonlinear, multi-variable optimization using ADS (corresponds to the response that is shifted to the left).

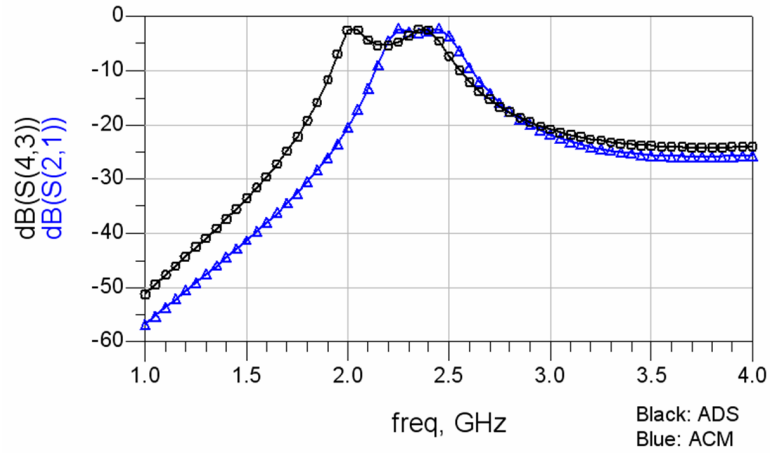

Figure 87. Comparison of the S21-parameters obtained from the augmentation-based technique (triangle) and that obtained from nonlinear, multi-variable optimization using ADS (circle).

of the nominal values of the tuning elements in the ADS. This is explained by the fact that the choice of nominal values of the tuning elements, leads to a better convergence in Figure 86, compared to Figure 87, that correspond to a different set of

nominal values of the tuning elements. However, the nonlinear optimization scheme employed in ADS has the advantage of solving all the unknown elements at the same time, unlike the proposed approach where the number of simultaneous variables is limited is determined by the rank of the augmentation coefficient matrix. However, as shown in Figures 86 and 87, the ADS-based simultaneous optimization has its own problem of choosing the nominal values for all the parameters. This problem of choosing the nominal value can become intractable when the number of variables is large (greater than 5-10). On the contrary, the augmentation scheme actually solves for the least-squares estimate of the values and do not require any nominal reference.

3.6 Summary

In this chapter, an efficient and accurate library development and layout-level circuit sizing methodology for the design of RF circuits in multi-layered organic substrate with LCP dielectric material is presented. The circuit sizing technique is based on layout segmentation, broadband modeling, polynomial mapping, and circuit-level optimization and tuning. An optimization technique based on ANNs and design space exploration has also been discussed for the synthesis of embedded inductors and capacitors. Synthesized results for components and circuits show accuracy that is within 5% of EM simulation results. A linear optimization-based circuit sizing methodology based on the augmentation technique has also been demonstrated. The tuning methodology is fast compared to nonlinear optimization using ADS. Design cycle time was significantly reduced since optimization were performed at the circuit level. Filter layout scaling was demonstrated across different frequency bands (single band as well as dual band), and circuit topologies. The mapping technique can be also applied to diagnostic analysis of circuit layouts in batch processing where geometrical variations affect the circuit performance.

CHAPTER 4

STATISTICAL ANALYSIS AND DIAGNOSIS METHODOLOGY FOR EMBEDDED RF PASSIVE CIRCUITS

The design of wireless circuits for RF frequencies requires precise values of passive components which is often not satisfied due to manufacturing variations, resulting in yield loss. In addition, RF design procedures in SOP-based technologies are migrating toward finer process features, that require tighter tolerances. Therefore, the circuit performance measures and yield are becoming increasingly sensitive to process fluctuations. These process fluctuations result from the buildup of variances at the different stages of the fabrication. To alleviate this problem, performance and yield figures for emerging technologies need to be analyzed during the design phase. However, fault detection and diagnosis for RF circuits after manufacturing is a time-consuming step in the design cycle. This is because multiple simulations of electromagnetic (EM) during incremental variations of structures are required while varying different layout parameters for correlation with the measured response. The focus of this chapter, as shown in Figure 88, is the application of statistical methods that enable accurate and efficient diagnosis of batch-fabricated RF circuits layouts. As demonstrated in Chapters 2 and 3, LCP-based packaging technology is a cost-effective approach to developing SOP-based RF circuits. As mentioned before, LCP material can be used to fabricate large panels (12" X 9"). For realistic yield estimation in batch fabrication, evaluation of the statistical analysis of performance measures is important. The picture of LCP panel with bandpass filers is shown in Figure 89.

The panel consists of 2,000 RF bandpass filters. The spread of the performance measures (S21 and S11) for 50 such functional filters from the panel are shown in Figures 111 and 91.

RF bandpass filter is one of most important blocks in an RF front-end. With

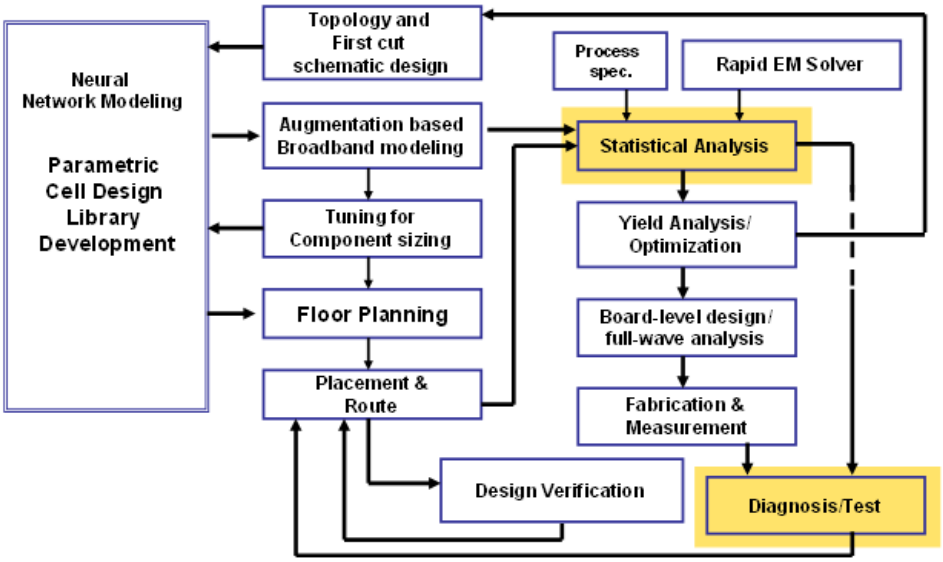

Figure 88. Focus of Chapter IV (shaded) in the perspective of an RF CAD framework

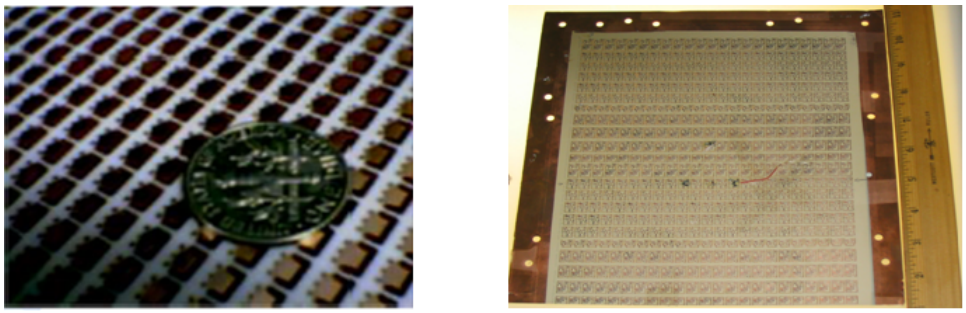

Figure 89. (Left) Visual comparison of the filter size and (right)photograph of an LCP panel.

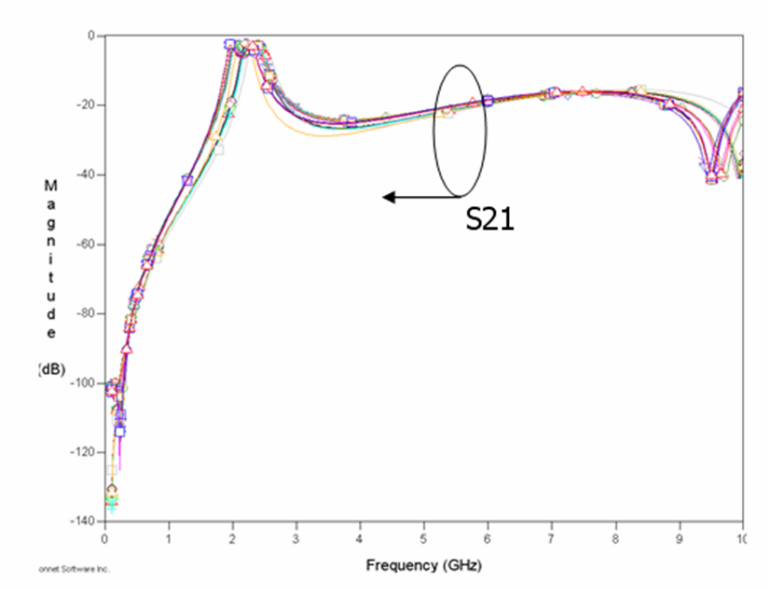

Figure 90. Measurement results of insertion loss (S21) for the fabricated filters.

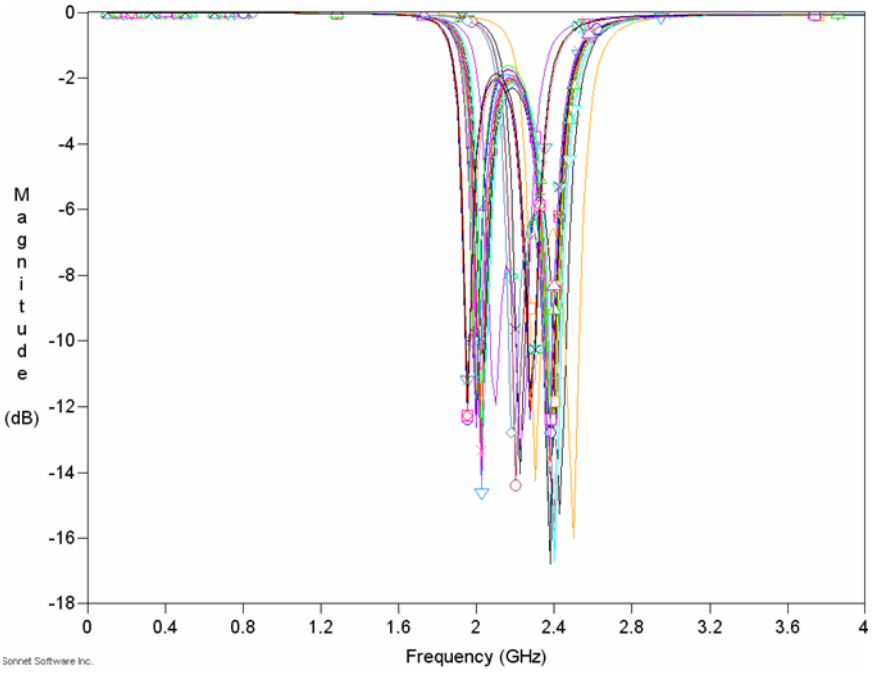

Figure 91. Measurement results of return loss (S11) variations of an embedded RF bandpass filter.

the convergence of multiple frequency standards, the design of filters requires precise controllability of the different performance measures. Due to the process variations, only a portion of the batch-fabricated filters meet the allowed range of specifications. The rest of the designs either depict functional failures (i.e. they do not possess filtering property), or they exhibit parametric failures (i.e. they show large variations in performance measures). As a result, prior estimation and optimization of yield in such emerging technologies is critical for cost-effective manufacturing. It should be noted, however, that the proposed statistical analysis and diagnosis approach is generic in nature and can be applied to any multi-layer packaging technology. LCP-based substrate was chosen as a proof of concept platform to validate the statistical analysis methodology.

In RF designs, the physical effects of the layout, such as electromagnetic coupling and parasitics affect circuit performance. The statistical analyses of RF circuits that are based on circuit simulators are fast, but they do not provide accurate results. In addition, the electrical characteristics of the embedded passive components (Ls, Cs, Rs), operating at RF frequencies, are highly dependent on the geometrical as well as the material properties. The conventional method to study the effect of component variations on system performance is to perform Monte Carlo (MC) analysis [12]. However, as discussed in Chapter 2, the MC technique for EM simulations can be time and memory-intensive. In addition, the MC analyses do not provide diagnosis or fault-detection capability, since it does not map the variations in the electrical parameters to the layout parameters.

The simulation time in general, for a method of moments (MoM)-based iterative solver increases as $O(n^2)$, where n is the number of cells in the layout. Parametric layout variations for sensitivity analysis (for example, optimetric analysis in Ansoft's HFSS) would require fine mesh setting of the test structures. Fine meshing is required to accommodate small increments in the geometrical parameters of the layout, the

stepwise increment process being typical in sensitivity analysis. Fine mesh settings translate to large number of cells, which, in turn, requires large amount of memory.

Furthermore, the cell size of the mesh varies inversely as the highest frequency of analysis. In other words, larger the highest simulation frequency, smaller is the cell size. Hence, EM simulations for the statistical analyses at high frequencies ($> 2GHz$), which require small cell size, is memory intensive. Classical worst-case analysis, in this case, is limited by the large number of input-output parameters and impractical simulation time. Clearly, there is a need for time-efficient, layout-level diagnosis methodology of RF circuits in prototype designs, as well as in batch fabrication.

4.1 Statistical design and modeling

With a particular performance measure of an RF circuit, such as insertion loss (for a bandpass filter), for a population of samples, a histogram such as the one shown in Figure 93 can be obtained. The spread in performance, illustrated in the figure, is due to inherent fluctuations in the manufacturing process. Local disturbances, caused by spot defects in the manufacturing process, are the primary causes of the catastrophic failures. Global disturbances, caused by process tolerances, are the primary causes of the parametric variations. Statistical design refers to the study that attempts to investigate and incorporate the effect of process variations on the circuit performance for a realistic estimate of performance and yield [81]. This study requires statistical circuit models that accurately reflect the process variations.

Statistical modeling for performance analysis/optimization is a new paradigm for embedded RF circuits. Therefore, it is useful to follow the research and development of statistical design and parametric yield optimization methods in digital IC design flows. Based on the studies, the different approaches to generating statistical parameters can be categorized as follows (as shown in Figure 92):

(a) Simulation based statistical modeling

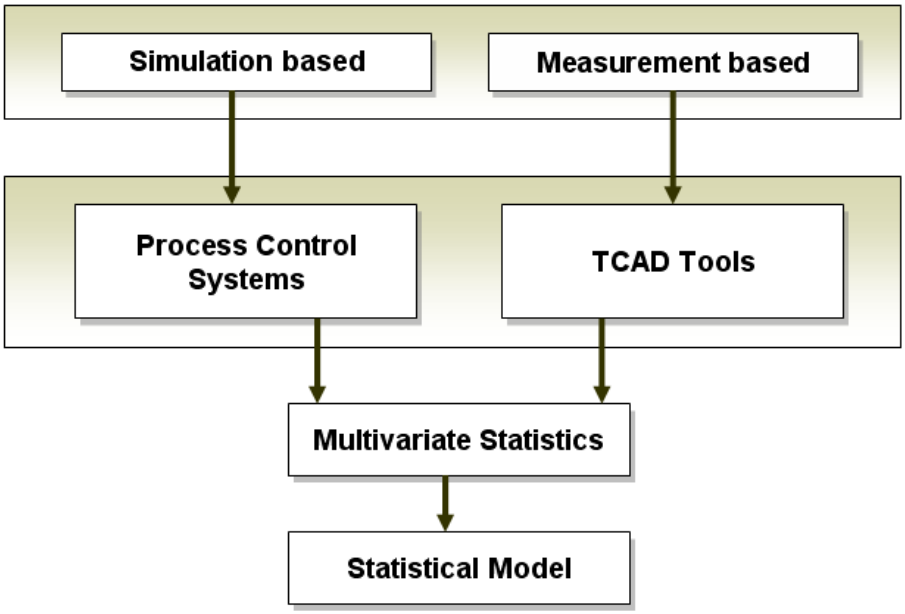

Figure 92. High-level methodology for statistical design.

(b) Measurement based statistical modeling

4.1.1 Simulation based techniques

Simulation-based statistical modeling is a "virtual" methodology that uses process and circuit simulators as the sources of statistical data. Such techniques are useful in the intial stages of process development, when test structures are unavailable. Such a methodology is also useful when the existing parameters of a low-yield process is incrementally improved.

The limitation of this approach, however, is that the inputs feeding the process simulators, such as dielectric variations, board warpage, and other material properties are not easily and efficiently characterizable in a fabrication line. Furthermore, the large number of models in a process simulator creates an additional challenge for calibration of the process simulator.

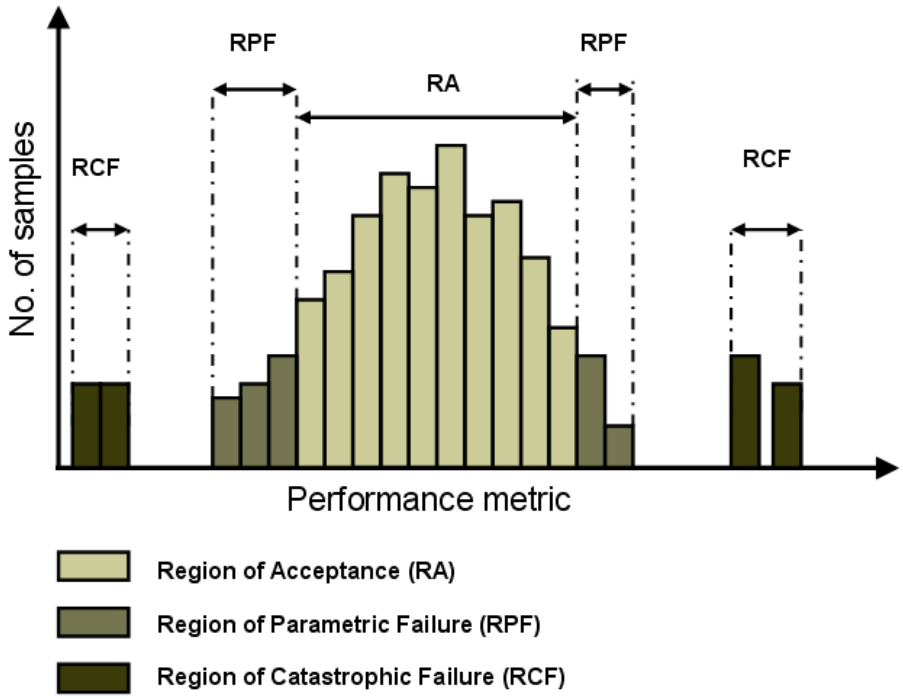

Figure 93. Statistical distribution of a performance metric, illustrating the region of acceptance, the region of parametric failure, and the region of catastrophic failure.

4.1.2 Measurement-based techniques

Measurement-based statistical modeling methods are practised in process-centric digital IC manufacturing. Measurement-based methods utilize high-speed, parametric testers and process control monitors (PCMs) to capture process variations. The practical advantage of the measurement based approach is that the pertinent device and process characteristics are measurable, electrically. Therefore, it is possible to develop a realistic model in a timely manner. The limitations of the measurement-based methods, however, are in the techniques for data analysis and data reduction. In addition, the correlation between the model parameters are not considered in this type of modeling technique. Several researchers have recently addressed these issues with more advanced statistical techniques for data analysis and generation of the statistical models.

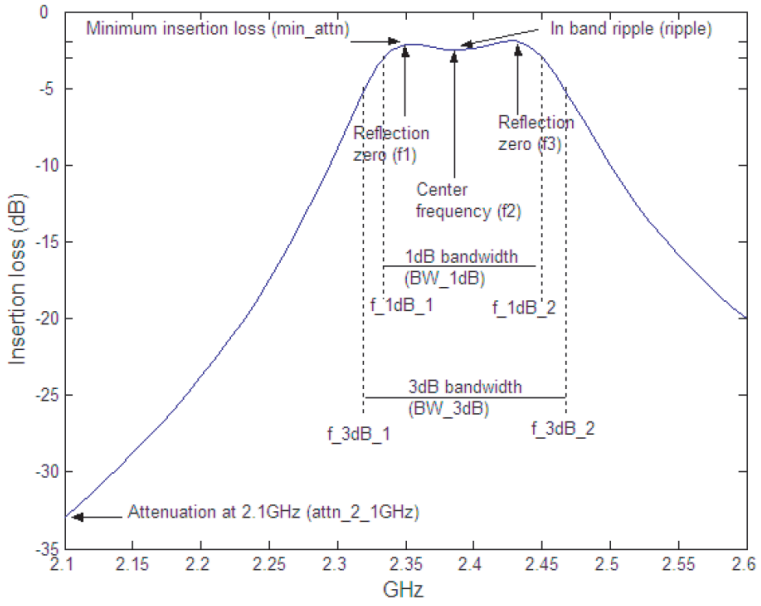

Figure 94. Typical variation of a performance metric (S21) for a bandpass filter for wireless applications.

4.2 Performance variations in RF bandpass filters

The RF bandpass filter is an important block in the design of an RF front end. With the convergence of multiple frequency standards, the design of filters requires precise controllability of passband ripple, bandwidth, stopband attenuation and harmonic rejection. An example of the different performance measures for an RF bandpass filter is shown in Figure 94 [56].

High performance, miniaturized bandpass filters have been designed on LCP across different topologies to meet the different frequency specifications. These designs include inductively coupled resonator filters, coupled line filters and capacitively coupled filter [9],[10]. Some of these designs are also based on hybrid topologies with a combination of coplanar waveguide (CPW) and stripline configurations to ensure volumetric compaction in multi-layer organic substrate. The filters are electromagnetically shielded with top and bottom ground planes for reducing signal coupling from the adjacent blocks. As mentioned in Chapter 1, the dimensional and the electrical stability of LCP material allow RF electronic devices to be manufactured in laminate

technologies. However, LCP-based processes may require strict process control for RF passive components.

Data sheets for the LCP material are commercially available in [82]. In the data sheet, thickness variation of 10%, and moisture absorbtion (at 23◦ C) of 0.04% has been reported. The changes in the values of the capacitors of the filters can be attributed to the change in the dielectric thickness. In addition, the capacitance values are also affected by variations in the dielectric constant value, the latter being affected by moisture absorption. Furthermore, in the manufacturing process, copper etching is conventionally assumed to have 10% line width variation for the minimum width lines. Based on these variations, the statistical analysis should be performed to estimate the yield of a particular design.

Dielectric constant variation can be attributed to the water absorbtion of the dielectric material. Since water has high dielectric constant ($\epsilon_r = 76.7$) and loss tangent ($tan\delta = 0.157$), water absorption can change the electrical properties of the material and degrade filter performance. Literature survey in the material characteristics of LCP and FR4 core material has shown the validity (for all practical purposes) of a linear change in the dielectric constant due to the water absorption. The following relation can be written for the effective dielectric constant:

$$\epsilon_{r_{eff}} = \epsilon_{r_{water}}(\%water) + \epsilon_{r_{lcp}}(1 - \%water), \tag{74}$$

where %water is the percentage of water absorbtion. Dielectric constant values for water and LCP material are $\epsilon_{r_{water}} = 76.7$ and $\epsilon_{r_{lcp}}$=2.9, respectively. Applying the maximum water absorbtion of 0.04% in Equation 82 resulted in 1% change in the dielectric constant. Although, this variation is very small for most high-speed electronic design and packaging applications, it proves critical, and, therefore, should be considered for RF front-end analysis. It is important to note that though Equation 82 is an approximation, the methodology presented is transparent to this approximation.

The manufacturing variations for the organic bandpass filter have been listed in

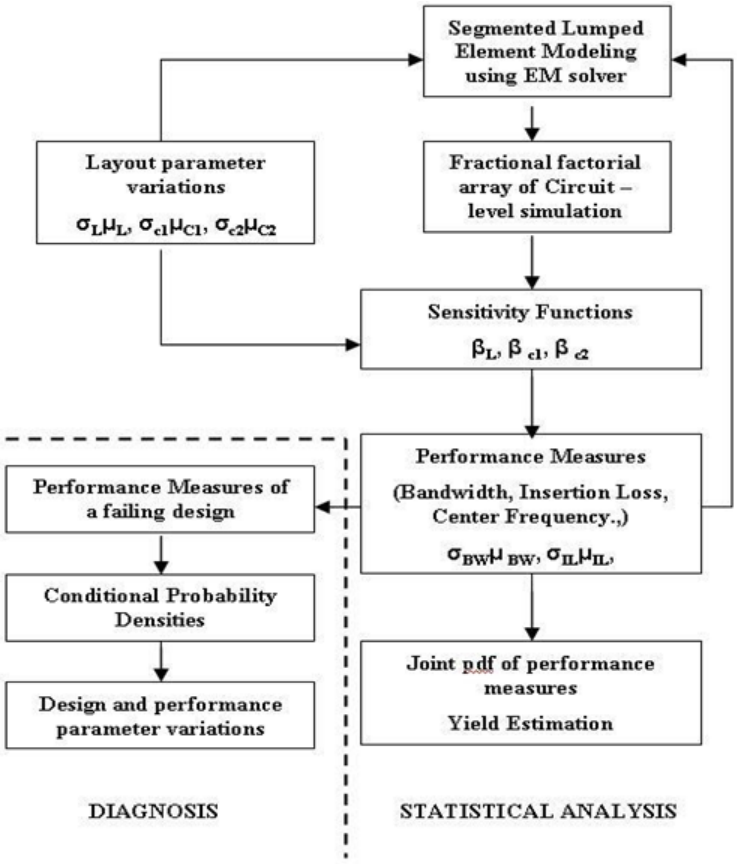

Figure 95. Flowchart of the statistical modeling and diagnosis methodology.

[56]. These manufacturing variations are assumed to have normal distribution with their mean (μ) and standard deviation (σ) presented in the table.

4.3 Statistical modeling methodology for embedded RF circuits

A design of experiments (DOE)-based statistical modeling methodology was employed in [56] for stochastic analysis and diagnosis of high-speed digital systems. In this dissertation, a similar DOE-based simulation setup to efficiently characterize the statistical disturbance space has been implemented. Furthermore, the relation between performance and design variations have been used for developing a parametric diagnosis methodology. The flowchart of the statistical analysis and diagnosis methodology is shown in Figure 95.

The process begins by identifying the key performance measures, significant parameters, and the statistical distributions of these parameters. After constructing an accurate model of the system, the performance measures were approximated as sensitivity functions of the design parameters through planned simulations. In this dissertation, the stochastic modeling is multi-domain in nature. It takes into account, the effect of electrical and mechanical parameter variations on the performance metrics of the devices being modeled. For example, to account for the thermo-mechanical stress effects incurred in the large panels, the warpage model of the board was included in the sensitivity analysis.

Linear and piecewise-linear (pwl) regression equations was used to map the multiple performance measures to the physical parameters. Linear and pwl regression techniques are not suitable for obtaining response functions over wide ranges of parameters, they can be used for fast characterization in small (around 5% to 10% of the nominal values) statistical variation space, which is the case for diagnosis. Yield and performance analysis was performed after computing the joint probability distribution (jpdf) of the analyzed performance measures. Parametric causes of the unacceptable performances of an individual system was searched by using the information acquired from the statistical analysis, thereby performing layout-level diagnosis.

Instead of catastrophic failures (Figure 92), this dissertation focusses on parametric failures, which occurs due to the variances of the component and the process parameters.

4.3.1 Segmented lumped element modeling and simulation

Segmented lumped element modeling of circuits have been formally explained and validated in Chapter 3. The lumped circuit models of the layout segments have been shown in Chapter 3, and were combined to extract the filter performance measures in the circuit simulator (Agilent's HP-ADS). The layouts of the segmented components were simulated in SONNET EM solver to extract the values of the circuit model

parameters. This is because simulation of the entire filter layout, using a DOE scheme in an EM solver, is computationally expensive.

As explained in [56], the design parameters were varied only within the statistical variation ranges. Therefore, with due consideratation to practical error bounds, third and higher order effects were ignored. The quadratic model for n design parameters is given by

$$y = \beta_0 + \sum_{i=1}^{n} \beta_i x_i + \sum_{i=1}^{n} \sum_{j=1}^{n} \beta_{ij} x_i x_j + \varepsilon, \tag{75}$$

where y is the approximated response, x's are the design parameters, β_0 is the intercept term, β_is are the coefficients of the first-order effects, β_{ij} are the coefficients of the second-order effects and ϵ is the approximation error. If $i \neq j$, then β_{ij} is called the interaction coefficient. One way to plan the experiments is to simulate all combinations of the design factors at all levels. This is called the full-factorial experimentation. If m is the level of the experiment plan and n is the number of design parameters, a full-factorial experiment results in m^n simulations. For a large number of parameters in RF designs, a full-factorial experiment plan is prohibitively time-consuming, especially for the requirement of the large number (m^n) of full-wave EM simulations. A 3-level, full-factorial plan, with n parameters and 3^n experiments, contains information on higher order interactions such as, linear and quadratic ($x_i x_j^2$) and bi-quadratic ($x_i^2 x_j^2$). These interactions are usually insignificant and are often ignored. Therefore, in such cases, the number of simulations can be reduced without incurring significant error, and fractional factorial experiment plans are obtained.

The number of simulations in the fractional factorial experiment plan is defined as m^{n-p}, where p is the fraction element. For example 3^{4-1} plan simulates four factors in 27 simulations. The plan is 1/3 fraction of the 3^4 full factorial plan. Table 96 shows a 3^{4-1} array, where 0's, 1's, and 2's correspond to different levels of factors A, B, C and D. The elements of the simulation matrix were coded values of the manufacturing variations, where 1's represent their mean, 0 and 2 are $\mu - 3\sigma$ and $\mu + 3\sigma$ respectively.

Here, μ is the mean and σ is the standard deviation. The component values in the table were obtained from SONNET EM simulations. Using the component values in each row, ADS circuit simulations were performed to obtain the filter performance.

A second table was generated with the results for the filter performance measures. Each row represented a different simulation condition. The filter performance was therefore, related to layout parameters.

4.3.2 Sensitivity analysis

The effects of the parameters was plotted by averaging the response at each level. For example, Figure 96 shows the sensitivities of certain performance measures with respect to layout parameters, the slopes being the measure of sensitivity. For example, C_{mid} is important for bandwidth, while C_{resn1}/Res_L is important for insertion loss (min_attn or S21). Based on the linearity and piecewise linearity of the plots, the performance measures can be represented as first-order linear approximations. For example, a performance measure P^i can be linearly approximated as a regression equation [56] as

$$P^i = \beta_{i0} + \beta_{i1}X^1 + \beta_{i2}X^2 + ... + \beta_{in}X^n + \varepsilon, \tag{76}$$

where n is the number of layout parameters, βs are the sensitivity coefficients and X^i s are the layout parameters converted to the standard normal by $(x - \mu_x)/\sigma_x$. Regression errors are given by ϵ_i. For example, the sensitivity equations for the filter for 1 dB bandwidth (BW_1dB), and attenuation at 2.1 GHz (attn_2_1_GHz) against the layout parameters, such as, the width of the center capacitor (C_{mid}), the width of the resonator capacitor ($C_{resn1/2}$), the width of the resonator inductor (Res_L), the matching capacitor width (C_{match}), and the dielectric constant of substrate (ϵ_r) are given by

$$\begin{aligned}\text{BW\_1\_dB} = {} & 0.1131 - 0.0426(\text{C\_mid}) + 0.0023(\text{C\_resn1}) + 0.002(\text{Resn\_L})\text{U}(\text{Resn\_L}) + \\ & -0.004(\varepsilon_r)\end{aligned} \tag{77}$$

Table 9. Array showing the fractional factorial plan

Experiment	A	B	C	D=AB^2C^2
1	0	0	0	0
2	1	0	0	1
3	2	0	0	2
4	0	1	0	2
5	1	1	0	0
6	2	1	0	1
7	0	2	0	1
8	1	2	0	2
9	2	2	0	0
10	0	0	1	2
11	1	0	1	0
12	2	0	1	1
13	0	1	1	1
14	1	1	1	2
15	2	1	1	0
16	0	2	1	0
17	1	2	1	1
18	2	2	1	2
19	0	0	2	1
20	1	0	2	2
21	2	0	2	0
22	0	1	2	0
23	1	1	2	1
24	2	1	2	2
25	0	2	2	2
26	1	2	2	0
27	2	2	2	1

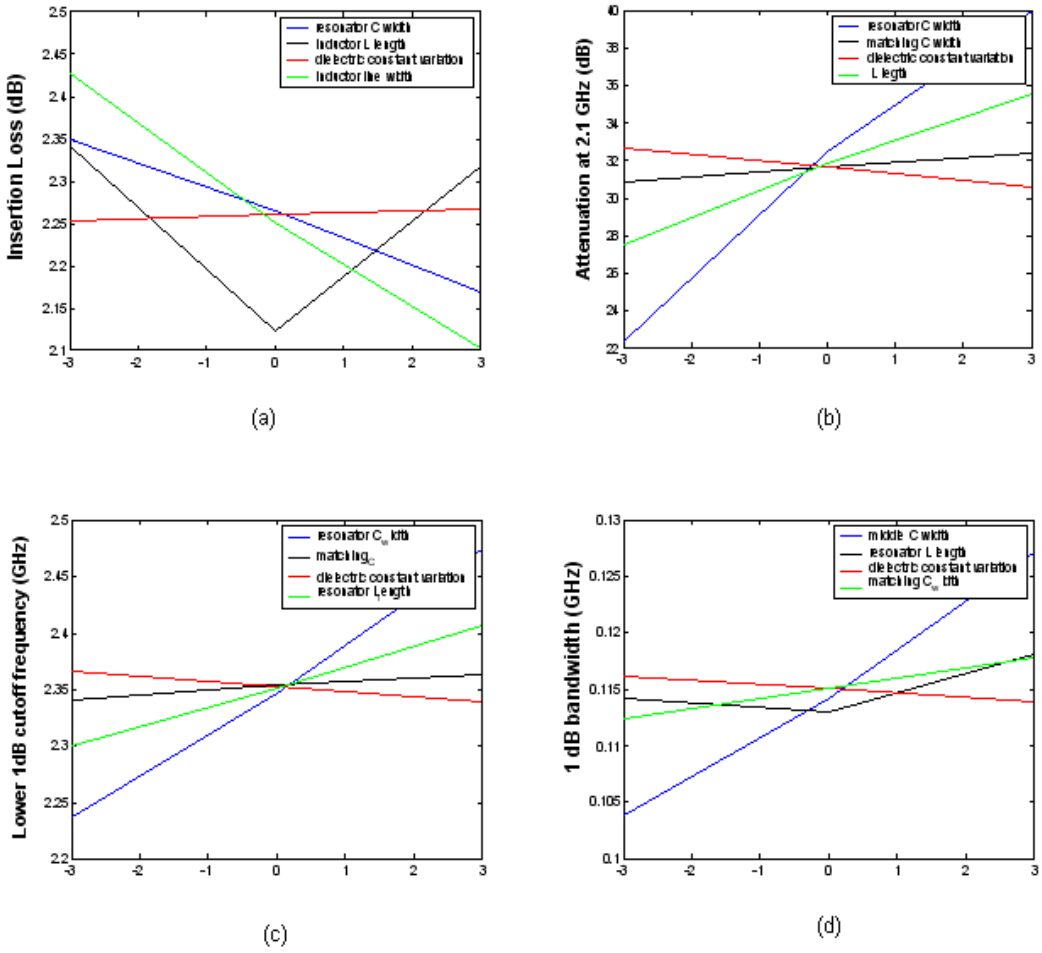

Figure 96. Sensitivity plots for the filter performance measures against layout parameters; The layout parameters has been converted to standard normal by $(x - \mu_x)/\sigma_x$; Sensitivity plots have been shown for (a)insertion Loss, (b)attenuation at 2.1 GHz, (c)lower 1 dB cutoff frequency, and (d)1 dB bandwidth.

$$\begin{aligned}\text{attn\_2\_1\_GHz} = 31.6096 + 1.3361(\text{Resn\_L}) + 0.2644(\text{C\_resn1}) - 0.3356(\varepsilon_{\text{r}}) \\ +2.9389(\text{C\_match})\end{aligned} \tag{78}$$

Here R^2 represents the regression coefficients, a measure of model fitness [56], and is computed as

$$R^2 = 1 - \frac{\sum_{1}^{27} [\varepsilon_i]^2}{\sum_{1}^{27} [P^i - \bar{P}^i]^2}, \tag{79}$$

and U is the unit step function. R^2 values close to 1 indicate good predictive capability of the regression equations. The simulation matrix was a resolution four $L_{27}(3^4)$ fractional factorial plan. As explained before, the $L_{27}(3^4)$ matrix does not confound single factor effects into two factor interactions. To show that the interaction effects are negligible, the simulation plan and the filter performance were applied to response surface regression (RSREG) procedures in SAS software [21]. It was seen that the R^2 values of the cross products (e.g. 0.0007, 0.0021, 0.0005, and 0.0005) were very small compared to the corresponding R^2 values of the linear terms (e.g. 0.7052, 0.8892, 0.9977, 0.9978). For min_attn, ripple, BW_1dB and BW_3dB, the R^2 values of the quadratic effects are significant, therefore, these performance measures were approximated by piecewise linear equations, the variables being insertion loss, ripple, 1 dB and 3 dB bandwidths respectively. The sensitivity coefficients were obtained with least-squares approximation as discussed before. For example, the coefficients for BW_1dB and attn_2_1_GHz were obtained as

$$[\beta_{BW\_1dB}] = ([E]^T[E])^{-1}[E]^T[bW\_1dB], \tag{80}$$

$$[\beta_{attn\_2\_1\_GHz}] = ([E]^T[E])^{-1}[E]^T[attn\_2\_1\_GHz], \tag{81}$$

where E is the simulation matrix (explained in Sec. IV A) , while [BW_1dB] and [attn_2_1_GHz] are the simulation results from the Table generated using design of experiments. In Equations 80, 81 the approximation error ϵ_i for the performance

measure P^i can be calculated as

$$[\varepsilon^i]_{27X1} = P^i - [E](([E]^T[E])^{-1}[E]^T)[P^i], \tag{82}$$

4.3.3 Extraction of probability density functions (pdfs) of performance measures

Using the regression equations of the performance measures and the pdfs of the process variations, the pdfs of the performance measures can be computed. The statistical variations of the layout parameters of components are independent of each other. This provides a significant advantage in computing the filter performance based on their variations. In general, let y be a random variable defined as

$$y = y_0 + h_1(x_1) + h_2(x_2) + h_3(x_3) + ... + h_n(x_n), \tag{83}$$

where $h_1, h_2, ..., h_n$ are functions of the independent random variables $x_1, x_2, ..., x_n$. Then *pdf* of y is defined as

$$f_y(y) = \delta(y - y_0) \otimes f_{h1}(h_1(x_1)) \otimes f_{h2}(h_2(x_2)) \otimes ... \otimes f_{hn}(h_n(x_n)), \tag{84}$$

where δ is the delta function, $\otimes$ is the convolution operator and $f_{h1}(h_1(x_1)), ..., f_{hn}(h_n(x_n))$ are the *pdfs* of $h_1(x_1), ..., h_n(x_n)$ respectively . Given the *pdf* of a random variable x_k, $f_{xk}(x_k)$, and a function $h_k(x_k)$, the *pdf* of the random variable h_k can be computed as

$$f_{hk}(h_k) = \frac{f_{xk}(x_{k1})}{\left|\dot{h}_k(x_{k1})\right|} + \frac{f_{xk}(x_{k2})}{\left|\dot{h}_k(x_{k2})\right|} + ... + \frac{f_{xk}(x_{kn})}{\left|\dot{h}_k(x_{kn})\right|}, \tag{85}$$

where $x_{k1}, x_{k2}, ..., x_{kn}$ are solutions to the equation $h_k - \dot{h}_k(x_k) = 0$ for a specific value of h_k, and $\dot{h}_k$ is the derivative of h_k. For cases in (2), (3), where β_k is the coefficient from the regression equation. Then we have

$$f_{hk}(h_k) = \frac{f_{xk}(h_k/\beta_k)}{|\beta_k|}. \tag{86}$$

Therefore, the *pdfs* of the performance measures can be computed by convolving the *pdfs* of the summation terms in (76) as

$$f_{P^i}(P^i) = \delta(P^i - \beta_{i0}) \otimes f(\beta_{i1}X1) \otimes f(\beta_{i2}X2) \otimes ... \otimes f(\beta_{in}Xn). \tag{87}$$

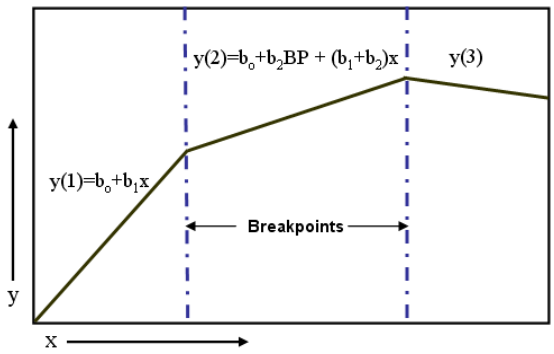

Figure 97. Piecewise linear function approximation for the estimation of weakly nonlinear sensitivities.

It can be seen that some of the sensitivity plots in Figure 96 are piecewise linear. In other words, a nonlinear sensitivity function can be approximated (with a practical degree of accuracy) with piecewise linear functions. A three section piecewise linear model has been illustrated in Figure 97.

A piecewise linear (pwl) relation between a variable x and a parameter y can be written (for example, with the first two stages of the pwl function in Figure 97) as

$$y = \beta_0 + \beta_1 x + \beta_2 (x - BP) U(x - BP) + \varepsilon, \tag{88}$$

where $\beta_{0,1,2}$ are the regression coefficients, BP is the breakpoint, ϵ is the regression error, and U is the unit step function defined as $U(x) = 1$, if $x \geq 0$ and $U(x) = 0$, otherwise. Equation (12) can be rewritten as

$$y = \left\{ \begin{array}{ll} \beta_0 + \beta_1 x + \varepsilon, & if x < BP \\ (\beta_0 - \beta_2 BP) + (\beta_1 + \beta_2) x + \varepsilon & if x \geq BP \end{array} \right\}. \tag{89}$$

The coefficients β_0, β_1, and β_2 in (12) were obtained by the least-squares approximation of y with the parameters x and $xU(x - BP)$[20]. The *pdfs* of the performance measures with linear and pwl terms can be written, as an example for P^i, as

$$f_{P^i}(P^i) = \delta(P^i - \beta_{i0}) \otimes f(\beta_{i1} X1) \otimes f(\beta_{i2a} X2 \otimes \beta_{i2b} X2U(X2)) \otimes ... \otimes f(\beta_{in} Xn) \tag{90}$$

Here $X2$ is a pwl term. The *pdf* for the piecewise linear terms in Equation 88 is

computed as [83]

$$f_y(y) = \left\{ \begin{array}{lll} \frac{f_x(y/\beta_1)}{|\beta_1|} & if & y/\beta_1 \leq 0 \\ \frac{f_x(y/(\beta_1+\beta_2))}{|\beta_1+\beta_2|} & if & y/(\beta_1+\beta_2) > 0 \end{array} \right\}. \tag{91}$$

The *pdf* of pwl terms in Equation 88 in general for positive and negative βs can be computed as

$$f(y) = \frac{f_x(y/\beta_1)}{|\beta_1|} U(y/(-\beta_1)) + \frac{f_x(y/((\beta_1+\beta_2))}{|\beta_1+\beta_2|} \times U(y/(\beta_1+\beta_2)), \tag{92}$$

Since $f_x(x)$ is normally distributed with μ =0 and σ =1, $(f_x(y/\beta))/\mid \beta \mid$ is the normal distribution of y with μ =0 and $\sigma = \beta$. Therefore, for the piecewise linear terms $y = \beta_1 x + \beta_2 x U(x)$, the pdf of y can be computed as

$$f(y) = N(y, 0, |\beta_1|) U(y/(-\beta_1)) + N(y, 0, |\beta_1+\beta_2|) \times U(y/(\beta_1+\beta_2)), \tag{93}$$

where $N(r, \mu, \sigma)$ is the normal *pdf* of the random variable r, with mean 'μ' and standard deviation 'σ'. For first order linear approximated performance measures, the μ and σ values are computed as

$$\mu = \beta_0; \qquad \sigma = \sqrt{\sum_{i=1}^{4} \beta_i^2 \sigma_{x_i}^2}, \tag{94}$$

The mean (μ) and variance (σ) of the pwl function y are given by

$$\mu_y = \int_{-\infty}^{\infty} y f_y(y) dy = \beta_2/\sqrt{2\Pi}, \tag{95}$$

$$\sigma_y^2 = \int_{-\infty}^{\infty} y^2 f_y(y) dy - \mu_y^2 = (\beta_1+\beta_2)^2/2 + \beta_1^2/2 - \beta_2^2/2\Pi. \tag{96}$$

For piecewise linear approximated performance measures,the μ and σ values are computed as

$$\mu = \beta_o + \sum_{i=1}^{n} \beta_{i2}/\sqrt{2\Pi}, \tag{97}$$

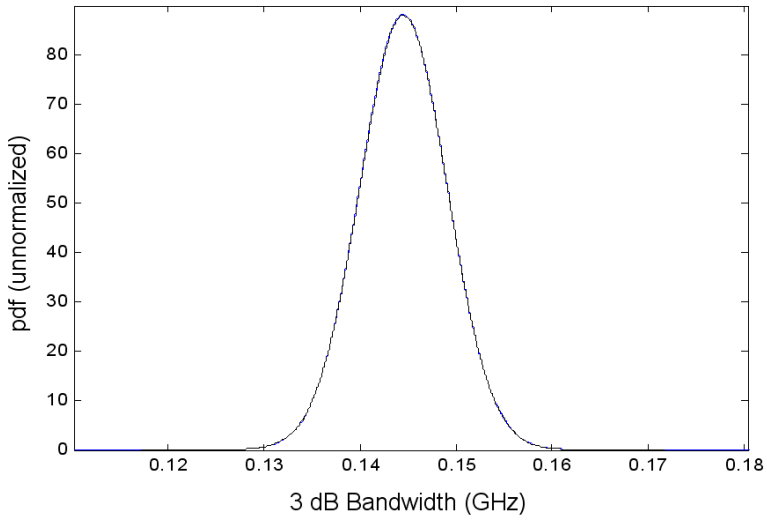

Figure 98. Probability density function for the 3 dB bandwidth.

$$\sigma = \sum_{i=1}^{n} \sqrt{\frac{(\beta_{i1} + \beta_{i2})^2}{2} + \frac{(\beta_{i1})^2}{2} - \frac{(\beta_{i2})^2}{2\Pi}}, \tag{98}$$

where β_{i1} and β_{i2} are the coefficients of x_i and $x_i U(x_i)$ terms. Similar analysis was performed on the individual components of the filter. Using similar sensitivity curves for the components and least square approximation, the values were approximated by first order linear equations. Due to the normally distributed nature of the manufacturing parameters, and first order linear equations, the components also have normal distributions. Figure 98 shows the pdf for the 3 dB bandwidth using convolution. Figure 99 shows the pdf for the minimum attenuation. The solid line is the convolution while the dotted line gives the normal distribution, which displays good agreement with the convolution results.

The convolution results have also been compared to the histogram of 100,000 random parameter instances applied to Equations 91 and 92. The convolution results were multiplied by a constant for visual comparison with the histogram. Figure 100 and Figure 101 show the results. Close agreement is observed between the results from the convolution technique and the histogram analysis, indicating that the convolution results accurately represent the probability density function.

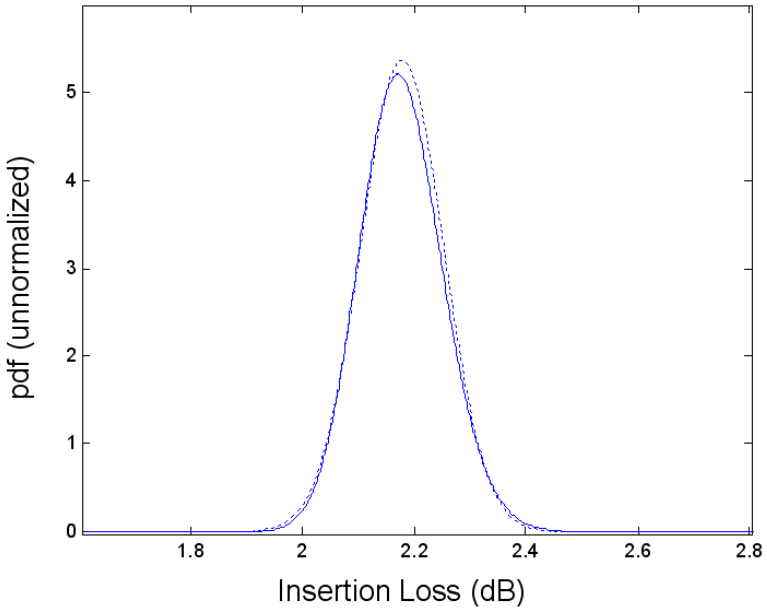

Figure 99. Comparison of probability density functions for minimum attenuation using convolution methodology(solid line) and normal approximation (dotted line).

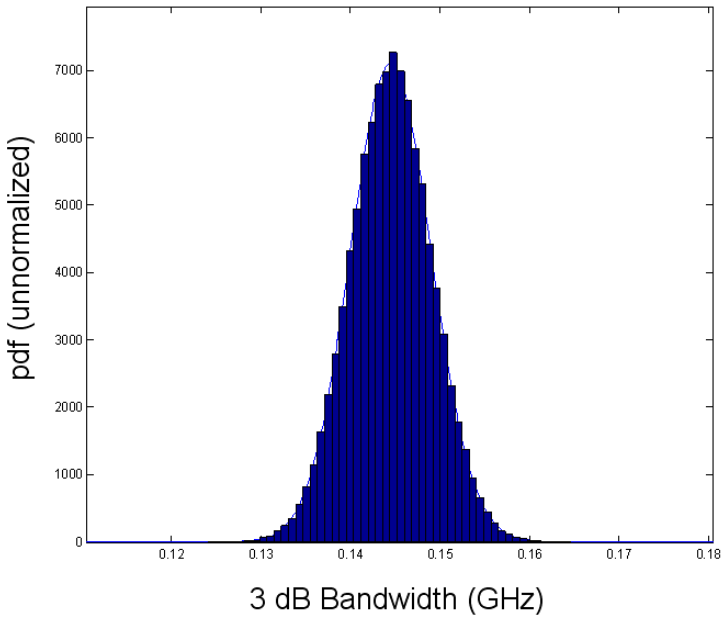

Figure 100. Comparison of probability distribution of 3dB bandwidth; Convolution (solid line) and random instances (histogram).

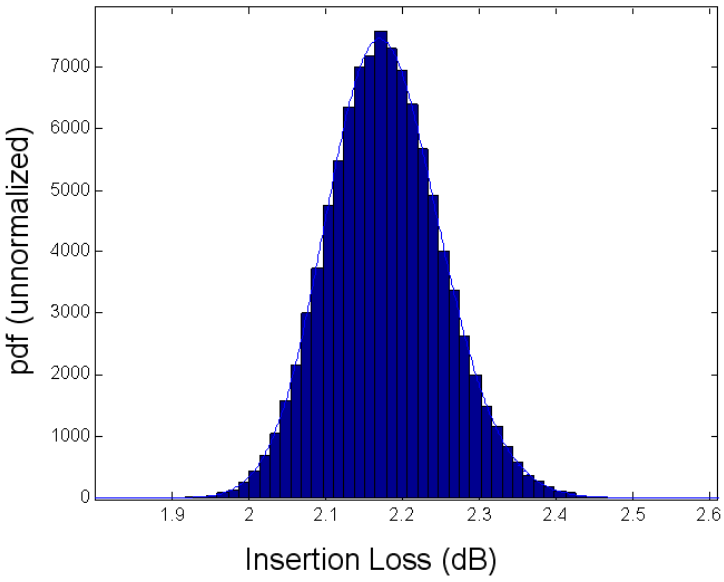

Figure 101. Comparison of probability distribution of insertion loss (S21); Convolution (solid line) and random instances (histogram).

In real-life applications, a few of the parameter distributions can be close to, but not ideally normal. Skewness and kurtosis are the measures of the deviation from normal distribution. They are defined as μ^3/σ^3 and μ^4/σ^4, respectively, where μ^3 and μ^4 are the third and fourth statistical moments and σ is the standard deviation. Clearly, the skewness and kurtosis for normal distribution are 0 and 3, respectively. For the random samples in Figure 99, the skewness and the kurtosis were computed as 0.1786 and 3.1112, indicating that they are distributed very close to normal. Similar analysis on the 3dB bandwidth (Figure 98) results in a skewness of 0.0086 and kurtosis of 3.0146. It is possible to compute yield with the exact convolution results shown in Figure 100. However, since the normal distribution is well defined in multivariate space, mean, variance, and covariance of the approximate normal distributions have been computed for the performance measures. The mean and variances of the approximate normal distribution of the performance measures were computed by adding the mean and variances of the linear and piecewise linear terms.

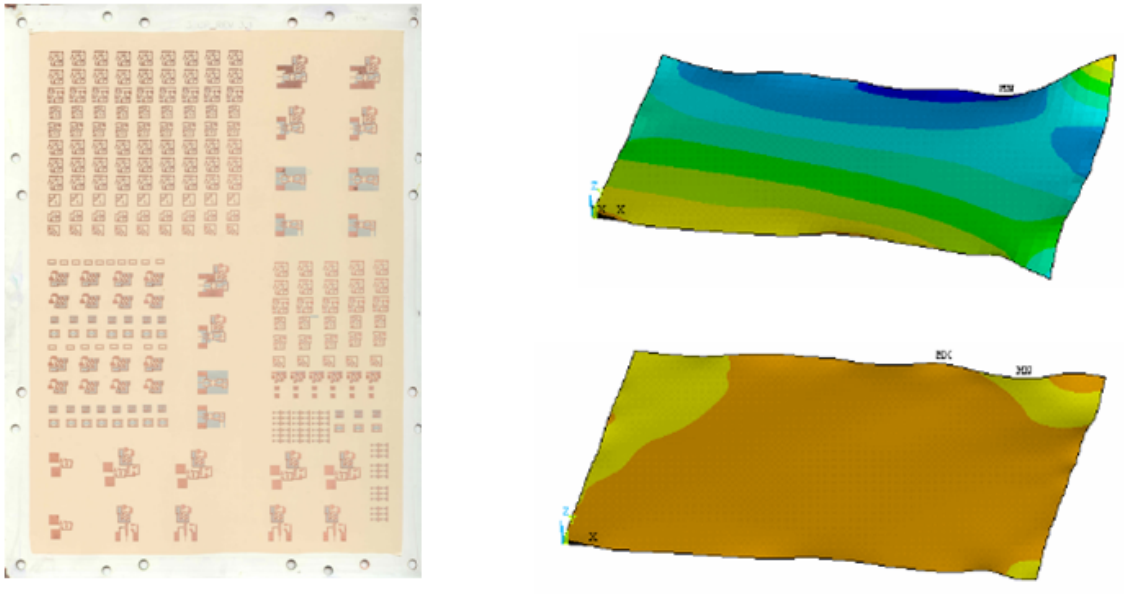

Figure 102. (Left) Photograph of a 12in × 9in LCP-based panel; (Right) Pictorial representation of the board warpage (figure not to scale).

4.3.4 Warpage modeling

Integration of embedded passives in RF circuits requires reliability estimation in order to maximize yield in batch fabrication. This subsection focusses on the effects of warpage on the performance variations of the embedded RF components. A conceptual representation of board warpage (not to scale) is shown in Figure 102, alongside a 9 in × 12 in LCP panel with embedded inductors and filters.

Warpage effects are critical in thin (∼30 mils) and large (18 in × 24 in) panels. The dependence of warpage on board thickness has been illustrated in Figure 104[21]. Recent studies have also reported the deformations (due to warpage) of panels that occur during thermal cycling with different substrates. The z-axis deformations for LTCC, LCP, FR4 and Teflon materials have been illustrated in Figure 103[21].

From Figure 104, it is evident that, for thin panels, inclusion of the effect of warpage on the performance variations is critical to realistic estimation of the manufacturing yield. This is because of thermo-mechanical effects that affect the electrical

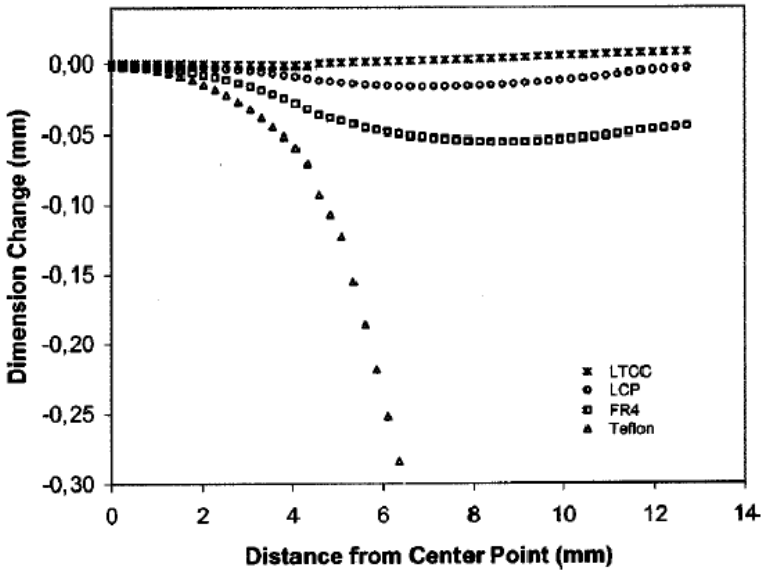

Figure 103. Out-of-plane displacement as a function of the distance from the center of the board; multiple plots correspond to different board-level RF packaging substrates.

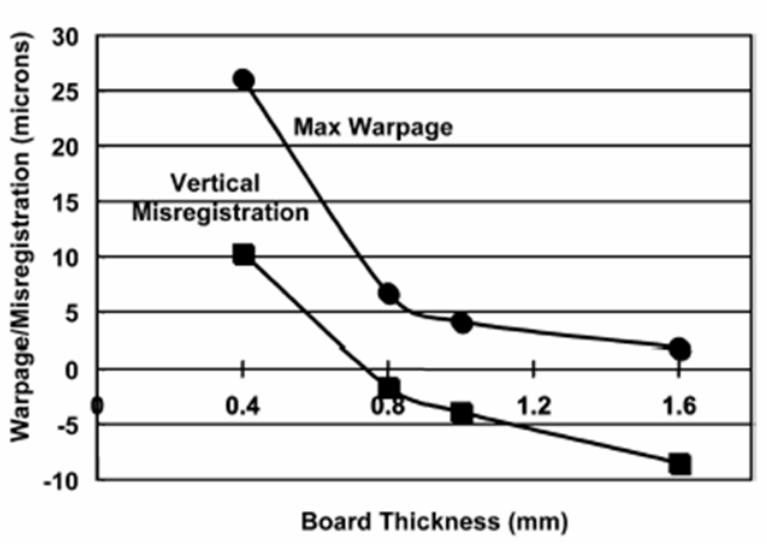

Figure 104. Board warpage as a function of board thickness.

characteristics of the fabricated devices, in addition to the process variations. Out-of-plane displacement (warpage) of the printed wiring board assemblies (PWBAs) has raised concerns on the assembly quality and their long-term reliability. Since the manufacturing of LCP-based panels is based on the PWB infrastructure, similar problems are being encountered in the batch fabrication of embedded LCP-based RF circuits.

Warpage of an organic PWB prevents surface-mount components from being aligned with the pads on the board during the placement process. After the leads are connected, the distances between the top surface of the PWB and the bottom surfaces of the components will vary due to warpage. Such variations will unevenly stress the interconnections and cause some of them and consequently (in some cases) the whole assembly, to fail. In addition, warpage-induced displacement affects the inline placement of the metallization layers of the embedded components (for e.g. capacitors and stacked inductors), thereby affecting their values. Warpage can also cause die cracks, via cracks, plated through hole (PTH) cracks, and delamination between different material layers during the assembly process. Many material, geometry, and process related parameters contribute to PWBA warpage.

From previous studies [21],[84],[85], the coefficient of thermal expansion (CTE) mismatch has been recognized as the dominant material factor for board warpage. From a geometric standpoint, the dimensions of the board and the components are critical to warpage [84]. Structures with larger aspect ratios (ratio of length to thickness) tend to generate larger warpage. In addition, the component layouts will affect the shape of the deformed PWB surface. During assembly and temperature cycling, PWBs and components experience a series of temperature variations. Large board panels experience considerable mechanical stresses during the thermal cycles due to mismatch in CTE (coefficient of thermal expansion) between the different layers, containing the supporting prepreg layers, the embedded LCP layers, and the copper

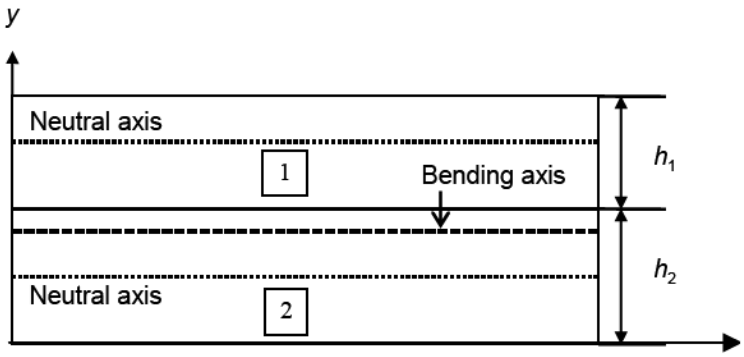

Figure 105. Two-plate model for the analytical calculation of board warpage.

metallization.

Large area (18 in × 24 in) processing which enables batch fabrication of devices using embedded passives in LCP substrate is a new technology that has been discussed in Chapter 1. The process enables the manufacturing of 2,000 - 10,000 devices on a single panel. Analysis of the variation of the electrical characteristics of the circuit components (e.g. inductance, capacitance) as a function of the spatial location of the circuit on the board is critical to realistic yield estimation for large panels. This is due to the reason that the statistical variance of performance measures, and the failure of the designs increase with increasing distance of the circuit locations from the center of the board.

The most straightforward model for thermo-mechanical stress analysis, for the multi-layer stackup shown in Chapter 2, is a two-layer analytical plate model [84]. The top layer is assumed to be LCP and the bottom layer as prepreg. The thickness of the LCP layer will be the combined thickness of all the individual LCP layers (in this case, 1) and similarly for the prepreg layers.

The analytical plate model considers only two layers of the substrate as shown in Figure 106. The assumptions are that the interface is mechanically well bonded, and the two layers have in-plane isotropy with Youngs moduli, E_1 and E_2, Poissons ratios, ν_1 and ν_2, and CTEs, α_1 and α_2. The first step is to get the curvature of the two-layer

stackup for a specified temperature loading. The plate bends with a curvature of κ_R, which is the inverse of the radius of bending (denoted as "R") is given by

$$\kappa_R = \frac{D_1}{C_4} 6h_1h_2\left(h_1 + h_2\right), \tag{99}$$

where h_1, h_2 denote the combined thicknesses of the LCP and prepreg layers respectively. Also,

$$C_1 = \overline{E_1^2}h_1^4\,; \qquad C_2 = \overline{E_2^2}h_2^4\,; \qquad C_3 = \overline{E_1E_2}h_1h_2. \tag{100}$$

The coefficient C_4 in Equation 99 can be obtained by combining the expressions for C_1, C_2, C_3 in Equation 100 as

$$C_4 = C_1 + C_2 + \left[C_3\left(4h_1^2 + 6h_1h_2 + 4h_2^2\right)\right]. \tag{101}$$

In Equation 99, D1 is given by

$$D_1 = \overline{E_1E_2}\left(\alpha_1 - \alpha_2\right)\Delta T, \tag{102}$$

where ΔT is the temperature loading for the process stage whose corresponding curvature is computed. Here the single layer of LCP is 1 mil in thickness which is much smaller compared to the combined thickness of the supporting dielectric layers (73 mils). Therefore, by using thin approximation [84], the curvature is given by

$$\kappa_R = 6\frac{\overline{E_1}}{\overline{E_2}}\frac{h_1}{h_2^2}\left(\alpha_1 - \alpha_2\right)\Delta T, \qquad h_1 << h_2, \tag{103}$$

The maximum warpage displacement is given by Equation 104, where the curvature κ_R is obtained from previous equations, as shown

$$W_L = L^2\kappa_R/8, \tag{104}$$

where L is the diagonal length from the center of the board. Therefore, the warpage of the board grows as the *square* of the distance from the point where it is held during curing.

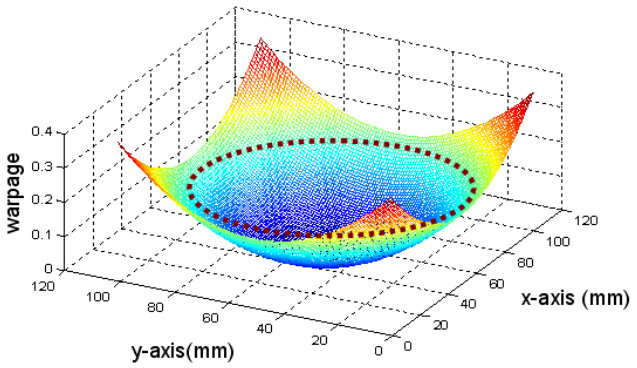

Figure 106. Board warpage distribution as a function of the distance from the center of the board (point of support during the thermal cycle.

Figure 106 shows the growth of the warpage as a function of the distance from the neutral point, which in this case, is the center of the board. The dotted line indicates the warpage levels within which the circuits statistically depict parametric variations in performance measures. For warpage levels beyond the dotted line, the statistical trend of circuits is functional failures instead of parametric variations. The iso-warpage (similar warpage level) contours are circular in nature due the isotropy of thermo-mechanical properties of the different layers in the stack-up. Accurate finite-element modeling of test structures of embedded passives using $ANSYS^{TM}$ in similar stackup has been shown by [86].

In this dissertation, the filters consist of planar spiral rectangular inductors. Therefore, the inductance does not undergo a significant change after deformation, since it does not have any turns in the z direction. Therefore, the effect of capacitance variations has been included in the sensitivity analysis. Linear regression analysis of the performance measures to extract the probability density functions (using convolution methods) has been shown in Section 4.3.3. Capacitance variations of around 5-8 % due to such warpage effects for similar stackup and thermal cycling conditions have been reported in [85]. The statistical analysis shown in this chapter is extended to also take into account, the mechanical parameters of large panel fabrication. In this

work, the design parameters are varied only within their statistical variation ranges. Therefore, the third and higher order effects were ignored. As explained before, the model parameters of the components are extracted from SONNET data and filter response is generated using HP-ADS. Each performance measure was approximated by linear and piecewise linear terms forming a regression equation. The statistical distribution of the performance measures is extracted by computing the mean and variance of individual components in the regression equation. The mechanical parameter variations are included in the regression equation for the components. For example, the regression equation for the resonator capacitor is given by

$$C_1 = 0.2125 + 0.07611(\varepsilon_r) - 0.0982(t) - 0.0231(w_r), \tag{105}$$

where ϵ_r, t and w_r stands for dielectric constant, line width and warpage level respectively. The regression equation is used to extract the mean and variance of the capacitance as

$$\mu_{C1} = 0.2125 + 0.07611\mu_{\varepsilon_r} - 0.0982\mu_t - 0.0231\mu_{w_r}, \tag{106}$$

$$\sigma^2_{C1} = (0.07611)^2\sigma^2_{\varepsilon_r} + (-0.0982)^2\sigma^2_t + (-0.0231)\sigma^2_{w_r}. \tag{107}$$

These multi-domain statistical parameters of the components are used to extract the *pdfs* of the performance measures. The *pdf* for the capacitance C_m1 and the insertion loss of the 2.3 GHz filter (with the warpage variations) have been shown in Figure 107 and Figure 108 respectively.

In order to test the spatial effect of warpage on performance failures, a test board was fabricated. The photograph of the LCP-based board has been shown in Figure 109. In Figure 109, it can be sen that the same filter designs (bunched as coupons) have been placed at different locations of the board. The measurement results for insertion loss (S21) and return loss (S11) for 50 filters on an LCP-based test board has been shown in Figure 111 and Figure 110, respectively. The measurement results, in

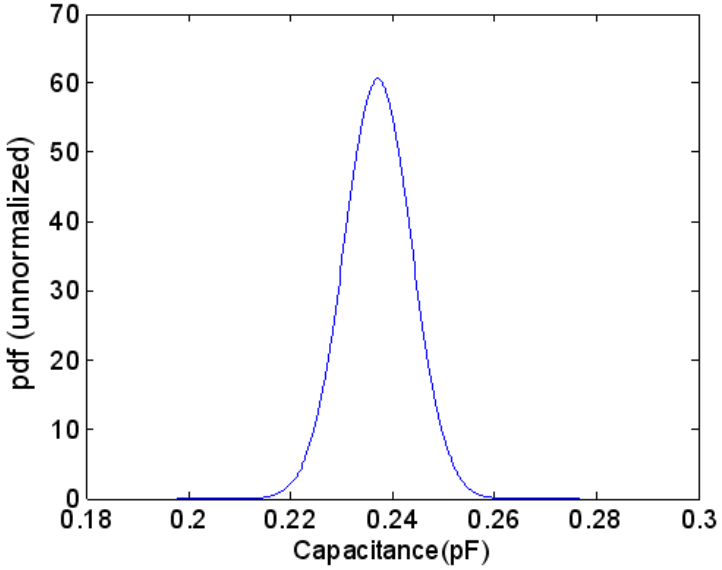

Figure 107. Probability density function of the capacitance for a capacitor after including the effect of warpage.

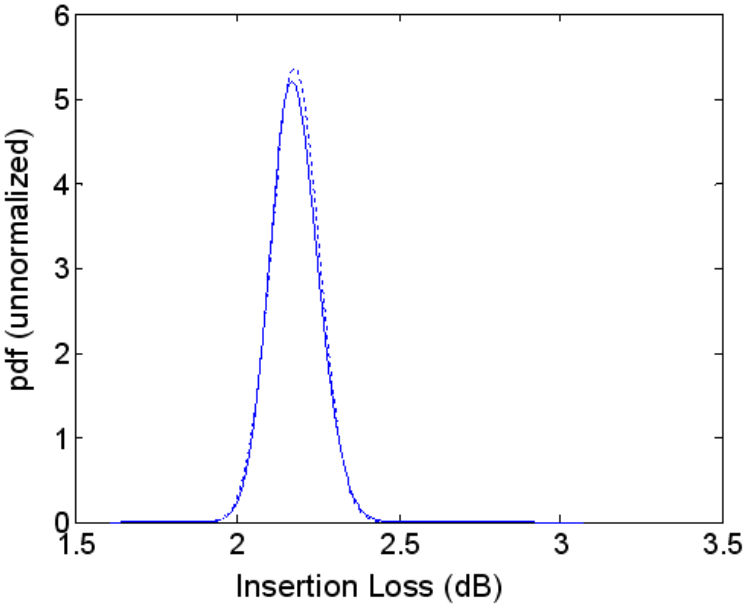

Figure 108. Probability density function of the insertion loss (S21) after including the effect of warpage.

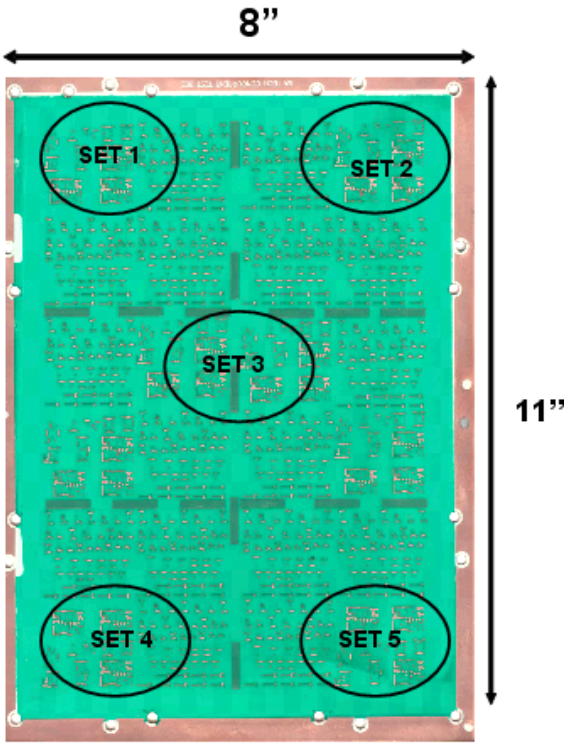

Figure 109. Fabricated panel of bandpass filters; The circles indicate different sets of filters distributed across the board to study performance variability.

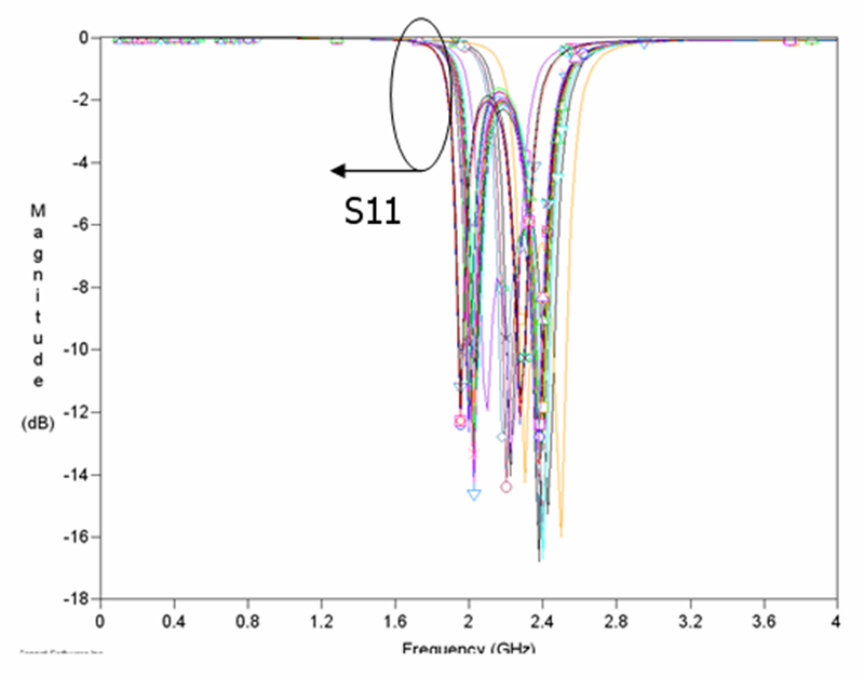

Figure 110. Measurement results of return loss (S11) for the fabricated filters.

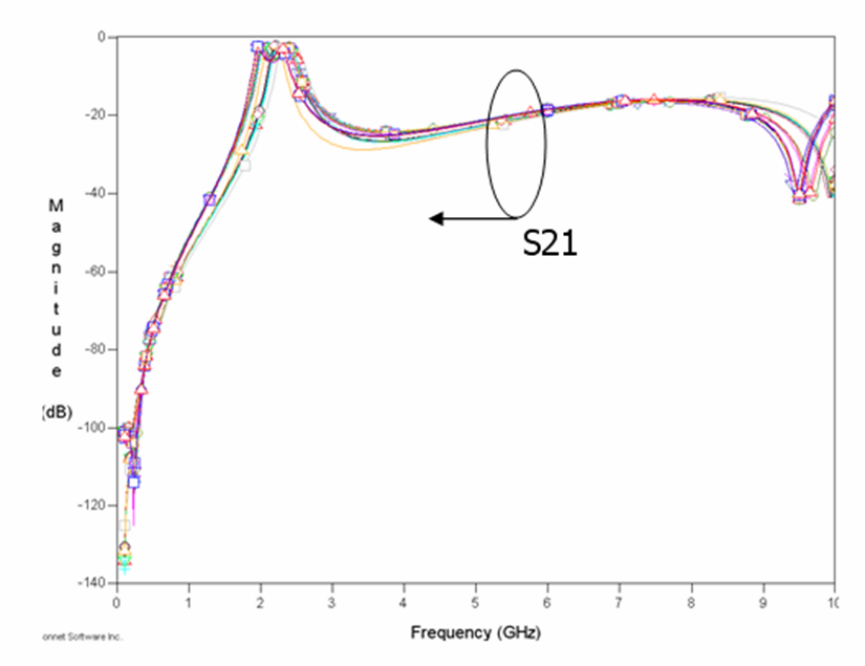

Figure 111. Measurement results of return loss (S11) for the fabricated filters.

Parameter	Variation (Set 1)	Variation (Set 2)	Variation (Set 3)	Variation (Set 4)
Center Frequency	~7%	~10%	~4%	~5%
Bandwidth	~11%	~8%	~6%	~5%
Attn@2.0 GHz	~3%	4%	~2%	~3%

Figure 112. Mean deviation of the measured results, from the design specifications, for different coupons.

terms of the coupons at different locations on the board, have been grouped in Figure 112 to demonstrate the effect of warpage. As predicted by the simulation results, the least variance in measurements for return loss (S11) was shown by the filters in coupon 3, located at the center. The model-to-hardware correlation for S11 variations have been depicted in Figure 113. From the correlation, it can be concluded that the modeling technique was able to capture the variations with sufficient accuracy.

Parameter	Variation Set 1 (measured)	Variation Set 1 (modeled)	Variation Set 3 (measured)	Variation Set 3 (modeled)
Center Frequency	~7%	~10%	~4%	~2%
Bandwidth	~11%	~8%	~6%	~5%
Attn@2.0 GHz	~3%	4%	~2%	~4%

Figure 113. Model-to-hardware correlation for average deviation of S11 from measurements and the simulations (shown for coupon 1 and 3.

4.4 Diagnosis based on design scaling

Diagnosis is the process of detecting faults in circuits after fabrication, thereby improving design yields. Fault diagnosis methodologies are prevalent in digital circuits. In RF designs, however, the physical effects of layout affect the circuit performance. In this part of the dissertation, diagnostic methods have been discussed for two scenarios: (a) discrete diagnosis to be applicable in the design of prototypes; and (b) probabilistic diagnosis based on statistical analysis for batch-fabricated designs, respectively.

In this part of the dissertation, the design scaling technique, discussed in Chapter 2, has been applied to the diagnosis of "prototype" designs. The variations in the measurement data from EM simulation were applied to the layout-level scaling flow to extract new layout geometries which are different from the origin layout parameters. The result was non-unique since multiple combinations of layout variations gave the same shift in frequency response characteristics. Certain designs met the process constraints and were selected for a cross-sectional analysis by which faulty designs could be detected. A flowchart of this prototype diagnosis methodology has been illustrated in Figure 114.

The mathematical formulation of the layout sizing methodology has been explained in Chapter 3. This analysis has been extended to demonstrate prototype diagnosis. To avoid confusion, the mathematical notations that were used in Chapter

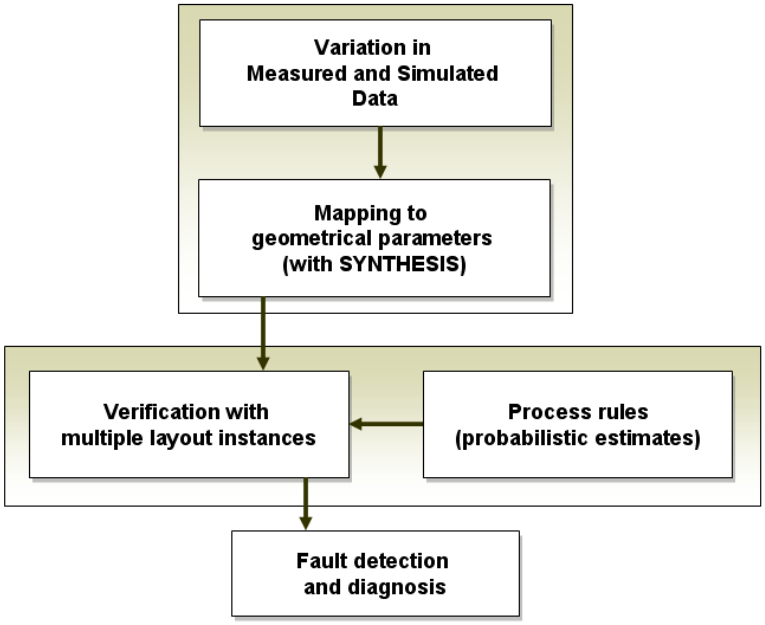

Figure 114. High-level methodology for the prototype diagnosis.

3 have been maintained in this section.

The measurement results of some of the fabricated filters show unacceptable variation from the desired frequency response. Multiple iterations of EM simulations of entire layouts with incremental variations in component geometries, to meet the measured response, can be time-consuming. A subset of the synthesized designs represents the possible defects in the fabrication, since some synthesized designs depict geometry changes that are not in accordance with the fabrication rules. Let the set of desired frequency characteristics of the filter (e.g. bandwidth, center frequency, insertion loss, transmission zero location) be given by the vector as shown

$$\lambda_T = [\lambda_1, \lambda_2, ..., \lambda_i]^T, \tag{108}$$

Let the frequency parameters for a device that show unacceptable variation of measurement data from simulation results is given by

$$\tilde{\lambda}_d = [\tilde{\lambda}_1, \tilde{\lambda}_2, ..., \tilde{\lambda}_j]^T, \tag{109}$$

where $\tilde{\lambda}_d$ is a subset of λ_T. $\tilde{\lambda}_d$ is used as the optimization goal in the circuit simulator

to tune the components in order the meet the measured frequency response. The solution, as stated before, is non-unique as different variations in component geometries lead to similar shift in frequency response. This is achieved by setting different sets of optimization variables in Agilent's ADS. Let the multiple synthesized component sets that meets $\tilde{\lambda}_d$ be given by

$$[C_1^1, C_2^1, .., C_{k^1}^1]^T, [C_1^2, C_2^2, .., C_{k^2}^2]^T, ..., [C_1^n, C_2^n, .., C_{k^n}^n]^T, \tag{110}$$

where n is the number of optimization variable sets and k^i is the number of variables in the i^{th} set. Using reverse polynomial mapping, as explained in Section 2.4.2, the modified geometry sets can be obtained as

$$g_m^i = \varphi_{im}^{-1}(C_m^i), \tag{111}$$

where C_m^i is the m^{th} component of the i^{th} synthesized set, and g_m^i is the corresponding geometrical parameter. The modified geometry sets for the optimized components of the synthesized layouts is given by the vector set

$$[g_1^1, g_2^1, .., g_{l^1}^1]^T, [g_1^2, g_2^2, .., g_{l^2}^2]^T, ..., [g_1^n, g_2^n, .., g_{l^n}^n]^T. \tag{112}$$

Here l^i is the number of layout parameters in the i^{th} synthesized layout. The initially synthesized dimensions, and those after tuning (to meet measured frequency characteristics) are related as

$$g_f^{syn} = g_i^{syn} + \delta, \tag{113}$$

where g_i^{syn}, g_f^{syn}, are the initial and final synthesized dimensions, respectively, and δ represent the change in geometry. This results in multiple sets of increment/decrement in component geometries for multiple instances of synthesized layout as

$$[\delta_1^1, \delta_2^1, .., \delta_{l^1}^1]^T, [\delta_1^2, \delta_2^2, .., \delta_{l^2}^2]^T, ..., [\delta_1^n, \delta_2^n, .., \delta_{l^n}^n]^T. \tag{114}$$

When δ is positive, g_f^{syn} is greater than g_i^{syn}. From a fabrication perspective, this means under-etching of metal lines. Similarly, a negative δ indicates over-etching of

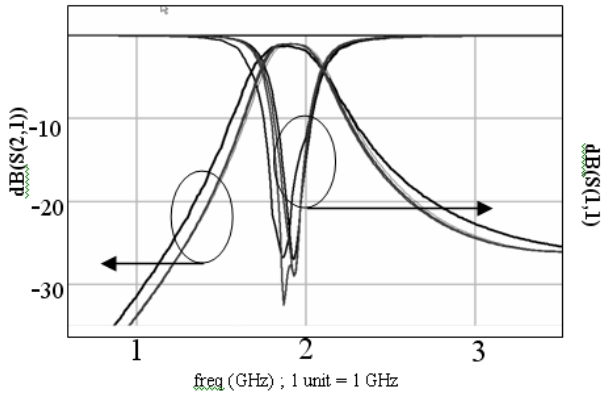

Figure 115. S11 and S21 of initial layout (S21 shifted to the left) and multiple instances of final synthesized layout (S21 shifted to the right and narrow bandwidth) that overlap with measurement data.

the lines. Statistical results of fabrication in this process show that the probability of over-etching is 80 % compared to under-etching. Therefore, the sets in Equation 114, that are predominant in negative δs (corresponding to over-etching), are selected. These sets are then compared with the fabricated designs to detect component faults. The frequency characteristic for the initial and final synthesized design (to correlate with measurement data) is shown in Figure 115. Figure 115 depicts the measurement for the fabricated prototypes for the filter design shown in Figure 32, in Chapter 2.

The measured response shows a change of 5.5 % in bandwidth and 1 % change in center frequency. Based on the synthesis technique outlined above and in Chapter 2 (Section 2.4.2), the variation in component geometries for different synthesized layouts is shown in Table 10. Based on the optimization variables that were selected,

Table 10. Variations(unit:mils) in the physical parameters in the synthesized filters, to exhibit similar frequency response as the fabricated prototype: Test case 1

Layout Instance	$\delta(C\_m1)$	$\delta(CC)$	$\delta(C\_resn1)$	$\delta(L1)$
1	-0.5	+0.6	X	-1.0
2	-0.7	+0.4	-0.7	X
3	-0.5	+0.75	-0.4	-0.7
4	X	+0.6	-0.3	-0.8

different sets of components have been scaled in different instances of the synthesis. An "X" in the table, indicates that the physical parameters of the corresponding component were not perturbed during the scaling procedure. In this example, all the sized instances have more number of decrement in geometries, and hence, all of these layouts were compared with the lateral cross section of the fabricated device for fault detection. The following inferences can be obtained from Table 10. The variations in instance 1 implied excessive etching for L, which, from process rules, is not accurate. Further, instances 3 and 4 implied high under-etching in CC and discrepancy in over-etching levels in C_resn1 and L1. Therefore, instance 2 bears highest resemblance with fabrication faults in resonator and matching capacitors. This was confirmed by measurements on multiple fabricated devices. This layout was then selected for redesign. The methodology did not require multiple time-consuming EM simulations of the whole layout with variations in different physical parameters for correlation with the measured response. The synthesis of each layout instance took 10 minutes on a 2.6 GHz Pentium(R) DELL PC with 1 GB RAM.

This includes the time for circuit optimization and polynomial mapping. In contrast, an EM simulation in SONNET, (on the same machine) for the entire filter, took 7.5 minutes for every frequency step of 0.1 GHz with a cell size of 1 mil X 1 mil. The simulation time in general for a MOM-based iterative solver increases as $O(n^2)$, where n is the number of cells in the layout. Hence, in diagnosis of RF circuits with small cell sizes to capture the etching effects, this approach can be very useful, compared to a full-blown EM analysis. This is specially important for batch fabrication. Diagnosis has also been applied to filters with one/two transmission zeros and have been confirmed through measurement data, as shown in the following test case.

4.4.1 Filter with transmission zeros

In this section, the test case under consideration is an embedded bandpass filter with transmission zeros. The layout of the filter is shown in Figure 116, while the

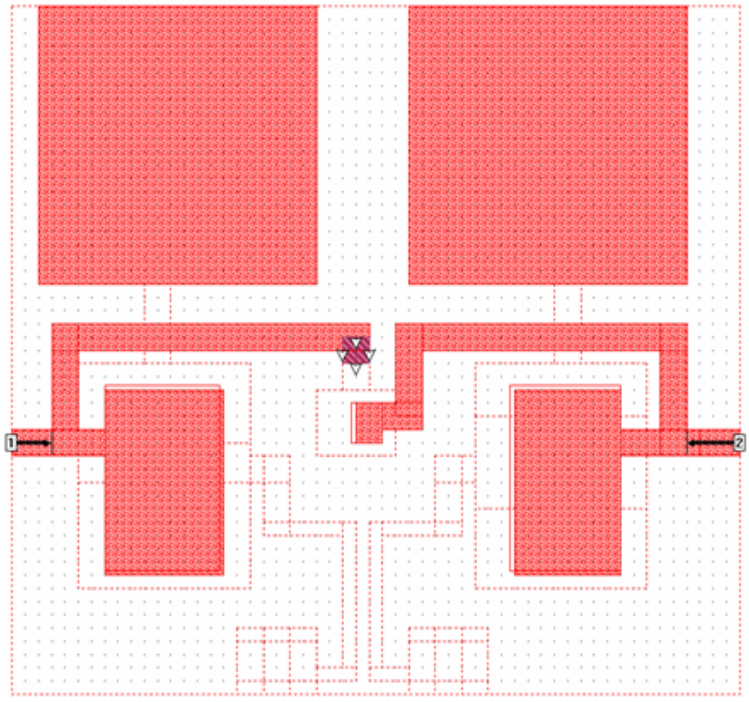

Figure 116. Prototype diagnosis for test case II; A second order bandpass filter with transmission zeros.

two EM simulation results with design variations are shown in Figure 117. The designs show variations in the center frequency, the bandwidth and the location of the transmission zeros. In contrast, no significant change in the insertion loss and the return loss characteristics were observed. The aim, as before, was to synthesize the variations in the geometries such that its frequency response bears resemblance with the fabricated prototype. Similar lumped element modeling and mapping, explained in the previous section and in Chapter 3 were used in circuit-level optimization to meet the response (which shows a shift to the right in Figure 117). As an example, the matching capacitors have polynomial based models of its components and parasitics as shown

$$Cp1 = 0.0079(W)^4 + 0.00691(W)^3 - 0.071(W)^2 - 0.069(W) + 0.011 \quad (115)$$

$$Cp2 = 0.0068(W)^4 + 0.0051(W)^3 - 0.056(W)^2 - 0.041(W) + 0.031 \quad (116)$$

$$C = 0.012(W)^4 + 0.012(W)^3 - 0.0168(W)^2 + 0.061(W) + 0.0491 \quad (117)$$

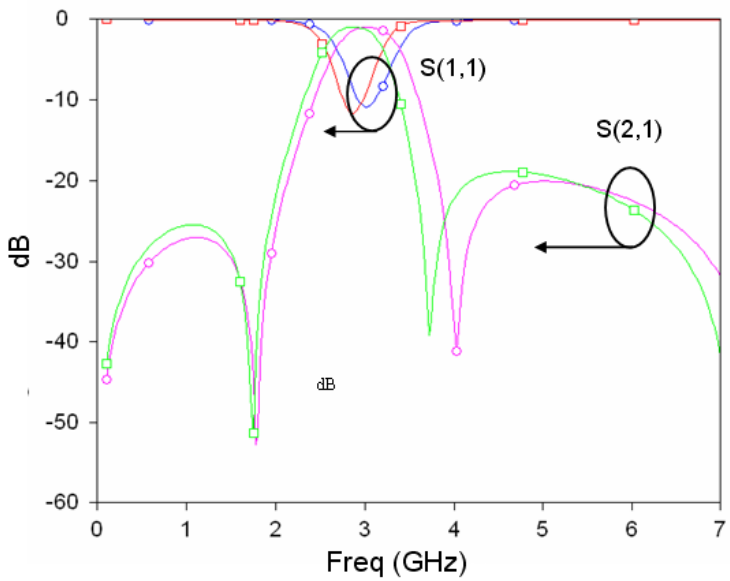

Figure 117. S-parameters for the faulty design(green) and the correct design(pink).

where W stands for the width of the capacitor plate. Similar polynomial-mapped models were derived for all the segmented sections. These models were used for lumped circuit optimization. The inverse of the polynomial curve-fits were used to extract the geometries from the optimized component values. The increment/decrement in component dimensions have been shown in Table 11.

Table 11. Variations(unit:mils) in the physical parameters in the synthesized filters, to exhibit similar frequency response as the fabricated prototype: Test case 2

Layout Instance	$\delta(C\_m1)$	$\delta(CC)$	$\delta(C\_resn1)$	$\delta(L1)$
1	X	+0.5	+1.5	-0.5
2	-0.5	+0.4	1	X
3	-1	+0.75	2	-0.75
4	X	+0.6	0.6	0.5

Measurement of the device cross-sections confirmed that the variations in the 2^{nd} layout instance correlated with the manufacturing fault. This clearly reduces the time for EM iterations to diagnose the layout defects in the fabricated designs.

4.5 Diagnosis based on statistical analysis

As mentioned before, LCP technology provides a platform for batch fabrication of RF circuits with embedded passives. As a result of the statistical variations in design and operational parameters, some circuits display unacceptable variations in performance measures. For example, for a bandpass filter, the variations can be in bandwidth, center frequency, return loss etc. For a functional design in this condition, the information extracted from the aforementioned statistical analysis can be utilized as a diagnosis tool.

Using the diagnosis methodology, the most probable layout parameters causing the unacceptable variations in performance measures can be systematically searched. The statistical framework, discussed in Chapter 4, can be employed to estimate the variations in the design and operational parameters for the measured variations in system performance. Here the analysis can be broken into two sections. When the number of performance measures in a design is *less* than the number of layout parameters, it suggests infinite number of solutions and therefore a probabilistic approach is used. When the number of performance measures is *more* than the number of physical parameters, it suggests a solution of linearly independent equations. A flowchart that depicts the high-level flow of statistical diagnosis is shown in Figure 118.

4.5.1 Number of performance measures less than number of physical parameters

For explaining the diagnosis approach, let $[X]$ and $[Y]$ be the random vectors for n layout parameters and m performance measures, respectively. The functional relation between $[X]$ and $[Y]$ is obtained by characteristic DOE-based simulations, as explained in the Chapter 4 (Section 4.3.2). If n is greater than m, then a unique solution of $[X]$ does not exist for a measured set of unacceptable performance metrics $[Y]$. Hence, the real parameter(s) causing the failure cannot be *accurately* decided.

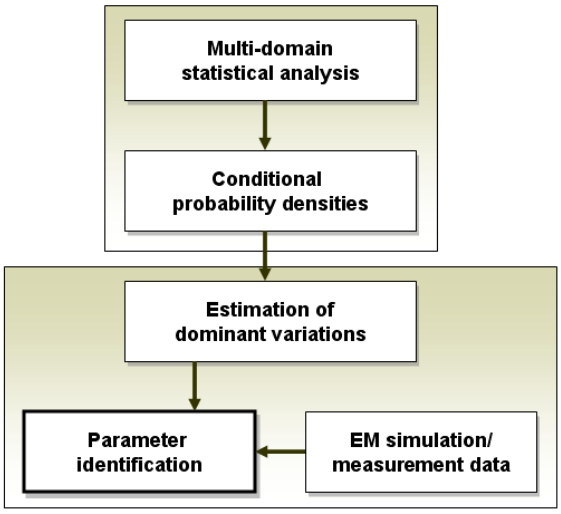

Figure 118. High-level flow for statistical diagnosis.

However since all design parameters are associated with *pdf*s, the most probable solution can be searched. The conditional *pdf* of the parameter vector $[X]$ for measured performance y is defined as [56]

$$f(X|Y=y) = \frac{f(X,Y)}{f(Y)}, \tag{118}$$

where $f(X,Y)$ is the joint *pdf* (*jpdf*) of the random vector of the design parameters and performance measures $[X^T Y^T]^T$. Then, the expected value of $f(X|Y=y)$ is the most probable parameter set causing the failure. Let $\tilde{Y} = [P^1, P^2, ..., P^m]^T$ be the set of unacceptable performance measures. Equations for the performance measures can be rewritten by subtracting the intercept terms $(\beta_{10}, \beta_{20}, ..., \beta_{n0})$ from $\tilde{Y}$ resulting in

$$Y = \beta X + \varepsilon, \tag{119}$$

where X is the parameter column, and Y,β and ϵ are defined as

$$Y = \begin{bmatrix} P^1 - \beta_{10} \\ P^2 - \beta_{20} \\ ..... \\ P^n - \beta_{n0} \end{bmatrix} \qquad \beta = \begin{bmatrix} \beta_{11}\beta_{12}.....\beta_{1k} \\ \beta_{21}\beta_{22}.....\beta_{2k} \\ ..... \\ \beta_{n1}\beta_{n2}.....\beta_{nk} \end{bmatrix} \qquad \varepsilon = \begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ ... \\ \varepsilon_n \end{bmatrix} \tag{120}$$

The error column ϵ is a gaussian random vector with a zero mean computed from the approximation errors. Since X and Y are gaussian random vectors, a new random vector Z can be defined as $Z_{n\times 1} = [X^T Y^T]^T$. Then, the *pdf* of Z is equivalent to the *jpdf* of X and Y, which can be computed as

$$f_Z(Z) = f_{X,Y}(X,Y) = \frac{Exp\{-1/2([Z]-E[Z])^T Cov(Z)^{-1}([Z]-E[Z])\}}{(2\pi)^2 \left|Cov(Z)\right|^{1/2}} \tag{121}$$

where $E[Z] = [\mu_X^T, \mu_Y^T]^T$, and $Cov(Z)_{n\times n}$ is a matrix composed of covariance matrices of X and Y vectors given by

$$Cov(Z) = \begin{bmatrix} Cov(X,X)Cov(X,Y) \\ Cov(Y,X)Cov(Y,Y) \end{bmatrix} \tag{122}$$

It is important to note that for independent design parameters, $Cov(X,X)$ is the diagonal matrix of the parameter variances. The expected value of the conditional *pdf* in Equation 118 can be computed as

$$E[X|Y=y] = \mu_X + Cov(X,Y)[Cov(Y,Y)]^{-1}(Y-\mu_Y) \tag{123}$$

Since X and Y are related through the linear regression operator, defined in Equation 119, as $Y = \beta X + \epsilon$, then

$$\mu_Y = \beta\mu_X, \tag{124}$$

$$Cov(X,Y) = Cov(X,X)\beta^T, \tag{125}$$

$$Cov(Y,Y) = \beta Cov(X,X)\beta^T + Cov(\varepsilon), \tag{126}$$

where $Cov(\epsilon)$ is the covariance matrix of the error vector in Equation 119. Substitution of Equations 124 through 126 results in

$$E[X|Y=y] = \mu_X + Cov(X,X)\beta^T[\beta Cov(X,X)\beta^T + Cov(\varepsilon)]^{-1}(Y-\beta\mu_X). \tag{127}$$

4.5.2 Number of performance measures more than number of physical parameters

Let $A_{n\times m}$ be the linear sensitivity matrix that relates n performance measures $Y_{n\times 1}$ to m physical parameters $X_{m\times 1}$, by

$$Y = Y_0 + AX + \varepsilon, \tag{128}$$

where Y_0 is a constant vector, and ϵ is the regression error vector. Provided that $(A^TA)^{-1}$ exists, for $n \geq m$, the least-squares solution is computed as shown

$$\hat{X} = (A^TA)^{-1}A^T(Y - Y_0). \tag{129}$$

The sensitivity equations of the matrix A, which correspond to its rows, should be linearly independent. Otherwise, the matrix $(A^TA)^{-1}$ is singular and not invertible. If two sensitivity equations in matrix A are linearly dependent, the corresponding performance measures are highly correlated. Therefore, such performance measures should not be included in the sensitivity matrix, simultaneously. Correlation coefficient among two performance measures $y1 \in Y$ and $y2 \in Y$, is defined as:

$$\rho_{y1,y2} = \frac{Cov(y1, y2)}{(\sigma_{y1})(\sigma_{y2})} \tag{130}$$

where $Cov(y1, y2)$ is the covariance, σ_{y1} and σ_{y2} are the standard deviations of $y1$ and $y2$, respectively. The correlation coefficient takes values between -1 and 1, where large values of $\mid \rho \mid$ indicate high correlation. The covariance values for the performance measures of the filter were computed as

$$Cov(y_m, y_n) = \sum_{i=1}^{4}\sum_{k=1}^{4}\left(\begin{array}{l}\frac{(\beta_{m-ia}\beta_{n-ka})}{2} \quad + \quad \frac{(\beta_{m-ia}+\beta_{m-ib})(\beta_{n-ka}+\beta_{n-kb})}{2} \\ - \quad \frac{(\beta_{m-ia}\beta_{n-ka})}{2\pi}\end{array}\right)\delta(i-k) \tag{131}$$

where β_{m-ia}, β_{m-ib} and β_{n-ka}, β_{n-kb} are pwl coefficients of the filter performance measures y_m and y_n, respectively. For the manufacturing parameters with linear sensitivity relations, $\beta_{m-ib} = 0$ and $\beta_{n-kb} = 0$. The covariance matrix can be computed

by using Equation 131 and the regression coefficients of the sensitivity equations. The standard deviations of the performance measures are shown in Table 12.

Table 12. Statistical parameters of the filter performance metrics: Test case I

Performance metric	Mean(μ)	Standard Deviation(σ)
min_attn(dB)	2.1714	0.0743
Ripple(dB)	0.4894	0.0613
f1(GHz)	2.3525	0.0437
f2(GHz)	2.4271	0.0474
BW_1dB(GHz)	0.114	0.0041
BW_3dB	0.135	0.0065

It was observed that many of the performance measures are highly correlated. Therefore, the sensitivity equations are linearly dependent. Amongst linearly dependent equations, only one equation and associated performance measure can be used for diagnosis. For example, in this case study, the center frequency was selected from the linearly dependent group. Then, the sensitivity functions of insertion loss (min_attn), inband ripple and the center frequency were considered for diagnosis as these parameters were linearly independent. It resulted in three equations to solve four manufacturing parameters. In this case, there is infinite number of solutions. However, for a measured unsatisfactory filter response, the most probable manufacturing parameter set can be searched. Therefore, probabilistic diagnosis was adopted for this filter. The most probable parameter vector can be written as

$$(X : f(X|Y = y)_{\max}) = \mu_X + Cov(X, Y)[Cov(Y, Y)]^{-1}(Y - \mu_Y), \tag{132}$$

where $(X : f(X|Y = y)_{\max})$ is the most probable layout parameter vector X for a measured filter performance y; μ_X and μ_Y are the expected values of X and Y; $Cov(Y, Y)$ is the covariance matrix of the performance measures; and $Cov(X, Y)$ is the covariance matrix of the layout parameters and the performance measures. The mean values of the performance measures were presented in Table 12.

For example, the faulty Y and μ_Y vector for min_attn, $ripple$ and $f2$ are defined as

$$Y = \begin{bmatrix} \min\_attn \\ ripple \\ f2 \end{bmatrix} \qquad \mu_Y = \begin{bmatrix} 2.1784(dB) \\ 0.5894(dB) \\ 2.3855(GHz) \end{bmatrix} \tag{133}$$

Covariance matrix of the performance measures $\mathrm{Cov}(Y, Y)$ was computed using Equation 131. Applying the regression coefficients results in

$$Cov(Y,Y) = \begin{bmatrix} 0.0055 & -0.0006 & -0.0022 \\ -0.0006 & 0.0038 & 0.0023 \\ -0.0022 & 0.0023 & 0.0021 \end{bmatrix} \tag{134}$$

Elements of the covariance matrix $\mathrm{Cov}(X, Y)$ is computed as [56]

$$Cov(x_i, y_n) = \frac{\beta_{n-ia}}{2} + \frac{\beta_{n-ia} + \beta_{n-ib}}{2}, \tag{135}$$

where β_{n-ia} and β_{n-ib} are the piecewise linear coefficients of filter performance measure y_n, for the layout parameter x_i. For parameters with linear sensitivities, $\beta_{n-ib} = 0$. Applying the regression to Equation 124 results in

$$Cov(X,Y) = \begin{bmatrix} -0.0297 & 0.0560 & 0.0414 \\ -0.0038 & 0.0123 & 0.0041 \\ 0.0023 & -0.0057 & -0.0046 \\ -0.0539 & -0.0045 & 0.0180 \end{bmatrix} \tag{136}$$

Then using Equation 132, the most probable vector of layout parameters for a measured set of performance can be computed. Multiple examples illustrate the accuracy of the diagnosis methodology.

4.5.2.1 Test case:I

The test case under consideration, for probabilistic diagnosis, is the the layout shown in Figure 32 (Chapter 2). From Table 12 as the 1^{st} example, a vector of layout parameters with random values was chosen according to the statistical distributions, and was

modeled and simulated. The resulting performance measures are min_attn=1.9933 dB, ripple=0.6513 dB and f2 (higher side of 1 dB frequency) =2.5342 GHz. For this filter, the center frequency has shifted to a higher frequency and hence does not pass the intended band. The performance results were applied to Equation 132. Table 13 shows the simulated and estimated manufacturing variations in the second and third columns.

Table 13. Comparison of the diagnosis results with measured variations: Case I

Layout parameter	Random input parameter	Estimated parameters	Least squares solution
Resn_L	$\mu + 2.29\sigma$	$\mu + 2.26\sigma$	$\mu + 1.52\sigma$
C_resn	$\mu + 1.34\sigma$	$\mu - 1.66\sigma$	$\mu - 3.95\sigma$
C_mid	$\mu + 0.71\sigma$	$\mu - 0.35\sigma$	$\mu - 6.64\sigma$
C_match	$\mu + 1.92\sigma$	$\mu + 2.47\sigma$	$\mu + 2.76\sigma$

It can be seen that most of the parameters are estimated close to their actual values. The fourth column in the table is the result obtained from the least square solution computed using (56). As explained before, the least-squares solution can be erroneous due to the ill-conditioned sensitivity matrix.

In the 2nd example, with non-random parameter variations, certain parameters like $Resn_L$ and $Resn_C$ had $+3\sigma$ variations from their mean values. The resulting performance measures where min_attn=2.4082 dB, ripple=0.4572 dB, and f2=2.253 GHz. Consequently, a shift is observed in the center frequency and change in the attenuation at 2.1 GHz. As a result, the filter violates the performance specifications. From Table 14, it can be seen that the estimated values captures the significant values, thereby enabling diagnosis.

In example 3, the other parameters were given 3σ variations. The resulting performance measures were min_attn=2.5107 dB, ripple=0.612 dB and f2=2.314 GHz. There has consequently been a shift in frequency and well as attenuation along with return loss. Estimated layout parameters are presented in Table 15.

Table 14. Comparison of the diagnosis results with measured variations: Case II

Layout Parameter	Input parameters	Estimated parameters
Resn_L	$\mu - 3\sigma$	$\mu - 2.65\sigma$
C_resn	$\mu - 3\sigma$	$\mu - 2.32\sigma$
C_match	μ	$\mu - 0.06\sigma$
C_mid	μ	$\mu - 0.79\sigma$

Table 15. Comparison of the diagnosis results with measured variations: Case III

Layout Parameter	Input parameters	Estimated parameters
Resn_L	μ	$\mu - 0.73\sigma$
C_resn	$\mu - 3\sigma$	$\mu - 3.17\sigma$
C_match	μ	$\mu - 0.46\sigma$
C_mid	$\mu - 3\sigma$	$\mu - 1.68\sigma$

As before, it is evident that estimated values capture significant variations. In addition, it is clear that the diagnosis technique do not give the exact statistical variation of the layout parameters in batch fabrication, but it captures the dominant variations. The results of statistical distributions show good correlation obtained from that using Monte Carlo methods. However, with the extensive lumped element model and having statistical distributions on all the model elements, Monte Carlo simulations took 36 hours on DELL PC with 2.4 GHz processor and 1 GB RAM. Clearly, layout-level statistical analysis using Monte Carlo methods is computationally prohibitive. Further, Monte Carlo cannot be used for layout-level diagnosis. The methodology shown in this chapter diagnoses parametric faults occurring due to manufacturing variations.

4.5.2.2 Test case:II

A second example for statistical analysis and diagnosis is the filter with transmission zeros shown in Figure 116. Using the regression analysis on the fractional factorial array of the design (consisting of 27 simulations), a subset of the sensitivity equations

has been shown

$$attn\_3\_7\_GHz = 40.489 + 0.025(C_{mid}) - 0.0083(resn_C) \\ -0.005(resn_L)U(resn_L) + 0.005(\varepsilon_r) \qquad (R^2 = 0.995) \tag{137}$$

$$f1 = 2.5213 - 0.029(resn_C) + 0.0056(C_{match}) \ - 0.0547(resn_L) - 0.0034(\varepsilon_r) \\ (R^2 = 0.980) \tag{138}$$

$$BW\_1dB = 0.4413 + 1.3361(C_{mid}) + 0.0644(resn_C) - 0.3356(\varepsilon_r) + 0.0389(C_{match}) \\ +0.0755(resn_L) \qquad (R^2 = 0.980) \tag{139}$$

The probability density functions of the performance measures were computed using the convolution methodology, explained in Chapter 4. The mean and standard deviation for the performance measures using has been shown in Table 16.

Table 16. Statistical parameters of the filter performance metrics: Test case II

Performance metric	Mean(μ)	Standard Deviation(σ)
min_attn(dB)	1.1714	0.0443
attn_3_7_GHz(dB)	40.589	0.0718
f1(GHz)	2.5213	0.0657
f2(GHz)	3.1871	0.0874
BW_1dB(GHz)	0.4413	0.0156
BW_3dB	0.6618	0.0082

Here $attn\_3\_7\_GHz$ is the transmission zero location at 3.7 GHz. The covariance of performance measures was computed to be

$$Cov(Y,Y) = \begin{bmatrix} 0.0075 & -0.0034 & 0.0049 \\ -0.0034 & 0.0017 & 0.0034 \\ 0.0049 & 0.0034 & -0.0049 \end{bmatrix} \tag{140}$$

Here the vector for the performance measure is given by

$$Y = \begin{bmatrix} attn\_3\_7\_GHz \\ BW\_3dB \\ \min\_attn \end{bmatrix} \qquad \mu_Y = \begin{bmatrix} 40.4894(dB) \\ 0.6618(GHz) \\ 1.1714(dB) \end{bmatrix} \tag{141}$$

For diagnosis, we needed to extract the covariance matrix between the performance measures and the physical parameters. This was calculated as [56] , and evaluated to be

$$Cov(X,Y) = \begin{bmatrix} -0.0458 & 0.0791 & 0.0624 \\ -0.0058 & 0.0325 & 0.0031 \\ 0.0021 & -0.0037 & -0.004 \\ -0.0439 & -0.0035 & 0.0280 \end{bmatrix} \tag{142}$$

For statistical diagnosis, the ideal design specifications were compared with the statistical variations of the design parameters. The information obtained for the statistical spread around the ideal specifications can be used, along with the covariance matrices, to obtain the feasible variation of the physical parameters. Table 17 shows the comparison between the observed and the estimated variations for a randomly selected design on the panel. Using the analysis and results obtained above, probabilistic diagnosis was performed. Clearly, the methodology closely estimates the major variations.

Table 17. Comparison of the diagnosis results with measured variations

Layout Parameter	Input parameters	Estimated parameters
Resn_L	$\mu - 0.25\sigma$	$\mu - 0.83\sigma$
C_resn	$\mu - 2.85\sigma$	$\mu - 3.17\sigma$
C_match	$\mu + 0.15\sigma$	$\mu - 0.34\sigma$
C_mid	$\mu - 3.23\sigma$	$\mu - 2.78\sigma$

4.6 Simulation with non-gaussian parameters

In statistical analysis of sensitivity data, many of the parameters are statistically related, thus requiring the use of the parameters' correlation coefficient matrix. Also, certain process distributions are not "purely" gaussian in nature. Since the methods for generating arbitrary sets of statistical parameter data are based on the concepts

of multivariate analysis, transformation of non-gaussian data to the gaussian/normal distribution domain is critical.

Appropriate transformation methods are necessary to convert non-gaussian raw data to the gaussian domain. With the input parameters represented in terms of gaussian distribution, the techniques from multivariate statistics (explained in the previous sections) can be used to generate the statistical metrics of performance parameters. The statistical methods that are employed for the extraction of the distribution of performance measures, requires the data to be in the Gaussian/normal domain. Typical Monte Carlo simulations in circuit analysis consist of applying random variations in the design parameters and performing SPICE simulations to extract the circuit response.

In Section 4.3.3, it was shown how convolution methods are used to extract distributions of performance measures from sensitivity data. In this part, the response surfaces are extracted from sensitivity data. For random variations of the design/process variables, the corresponding perturbed values of the performance measures can be obtained by using least-squares method to approximate the response surface. Figure 119 shows the unnormalized *pdf* of the insertion loss of the 2.3 GHz filter in the dualband design by using the response surface. Figure 120 represents the same distribution obtained from full-scale Monte Carlo analysis in ADS using lognormal design parameters. It can be seen that the response surface based method is in good agreement with the results obtained from the Monte Carlo analysis.

However, extraction of response surfaces with a large set (n>6) of critical, variational parameters becomes mathematically involved [14]. A simple but powerful alternative is to transform the non-gaussian raw data into the gaussian domain. By transformation, it is possible to view normal probability plots, run standard tests for normality, skewness and kurtosis. The square-root ($n = 1/2$), lognormal ($n = 0$), and

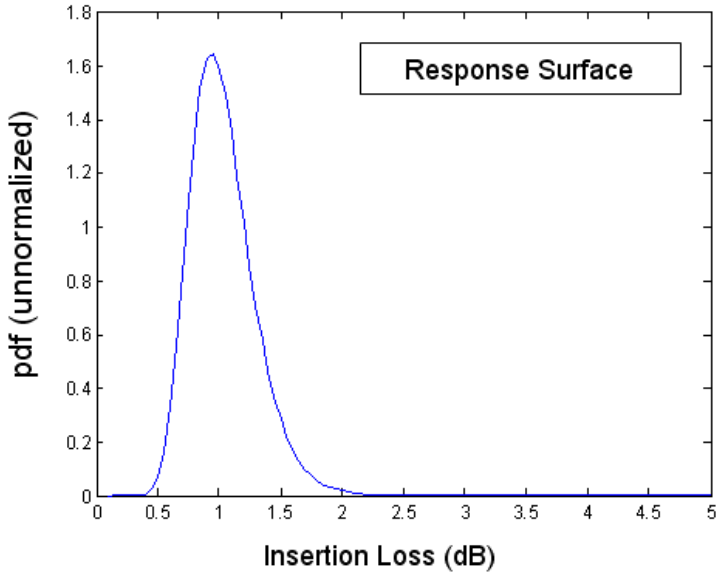

Figure 119. Probability density function of the Insertion Loss using the response surface methodology.

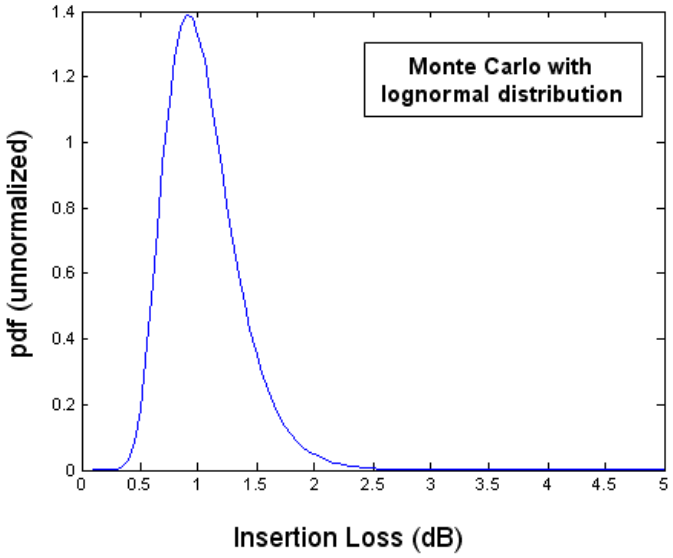

Figure 120. Probability density function of the Insertion Loss using Monte Carlo simulations in ADS with non-gaussian parameters.

reciprocal ($n = -1$) transform from literature [12] are generally sufficient to transform the "skewed" data into the gaussian domain. Let x be the original variable, and y its transformed value; then the following transform can be applied

$$y = a + c(x + b)^n \qquad for \quad n \neq 0 \tag{143}$$

$$y = a + c\log(x + b) \qquad for \quad n = 0 \tag{144}$$

If y is the transformed value of x by the function g, i.e. $y = g(x)$ then, as shown by [87]

$$f_x(x) = f_y(g(x)) \left| \frac{dg(x)}{dx} \right|, \tag{145}$$

where f denotes a density function. With this new non-gaussian density function $f_x(x)$ the first and second moments can be expressed as shown [87]

$$\mu_x = \int_{-\infty}^{\infty} x f_x(x) dx, \tag{146}$$

$$\sigma_x^2 = \int_{-\infty}^{\infty} x^2 f_x(x) dx. \tag{147}$$

An important set of transformations are those associated with lognormal distribution. With x lognormal distributed, so that $y = logx$ is distributed gaussian, the conversion from log-normal to the gaussian domain is given by

$$\mu_y = \log \mu_x - 1/2(\log(\frac{\sigma_x^2}{\mu_x^2} + 1)), \tag{148}$$

$$\sigma_y^2 = \log(\frac{\sigma_x^2}{\mu_x^2} + 1). \tag{149}$$

With the aid of a few mathematical manipulations, it is straightforward to show that the inverse transformation (gaussian domain to log-normal domain)is given by

$$\mu_x = \exp[(\mu_y + 0.5\sigma_y^2)], \tag{150}$$

$$\sigma_x^2 = (e^{\sigma_y^2} - 1) \exp[(2(\mu_y + 0.5\sigma_y^2)]. \tag{151}$$

The transformation of a lognormal technology variable to gaussian data form and applying to the aforementioned statistical framework for the calculation of the *pdf* of the insertion loss , as shown in Figure 121 and Figure 122.

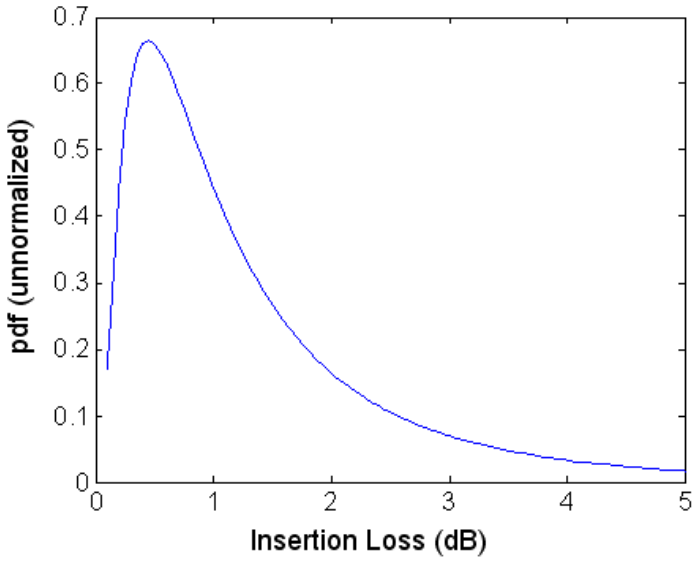

Figure 121. Lognormal distribution of the Insertion Loss.

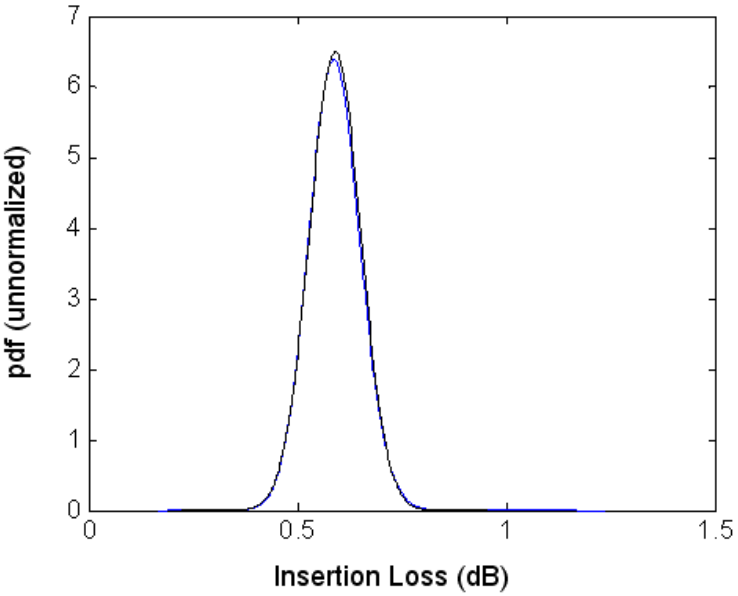

Figure 122. Probability density function of the Insertion Loss after conversion from the lognormal distribution to the gaussian distribution.

4.7 Summary

In this chapter, an efficient, multi-domain statistical analysis and diagnosis framework for RF passive circuit layouts such as bandpass filters is presented. The circuits are composed of quasi-lumped embedded inductors and capacitors in multi-layer, laminate-type, organic substrate like liquid crystalline polymer (LCP). The statistical methodology includes modeling of board warpage and dielectric variations that are critical for large panel fabrication. In this approach, the statistical variations of the layout parameters are mapped to performance measures through circuit and EM simulations, based on fractional factorial arrays. The stochastic analysis framework was utilized as a diagnosis tool to estimate the variations of RF circuit layouts for measured performance variations. The concept has been validated by the design and fabrication of embedded RF bandpass filters. The results of statistical analysis and diagnosis show good correlation with measurement/EM data. Finally, appropriate transformation techniques for analysis with non-gaussian distributed parameters have also been discussed.

CHAPTER 5

YIELD OPTIMIZATION OF RF PASSIVE CIRCUITS

In the fast paced competitive market of electronic products, the time-to-market and cost hold the key to economic survival. High manufacturability of electronic product designs minimizes lead time and costs. Design and manufacturing are key activities in the realization of electronic products. Due to the surge in the consumer wireless industry, the process of electronic product realization has assumed multidisciplinary proportions, and hence, design and manufacturing activities are no longer independent ventures. There is a need for electronic product designers to collaborate with manufacturers, gain essential knowledge regarding the manufacturing facilities and the processes, and apply this knowledge during the design process. The domain that addresses these issues is called "design for manufacturability"(DFM). The focus of this chapter, as shown in Figure 123 is the application of a optimization framework to improve the manufacturing yield of the embedded RF passive circuits. From an IC perspective, the underlying problems that have led to the development of DFM methods has been depicted in Figure 124 [88]. As shown in Figure 124, the features (structures) on the silicon chip are now smaller than the wavelength of the light used to create them. In order words, if we assume that the green geometric shape shown in Figure 124 is the ideal (desired) form, then this is the shape that would be created in the initial GDSII file generated by the physical design tools. The problem is that if this shape is subsequently created as-is in the photomask, then the corresponding form appearing on the silicon would drift progressively from the ideal, as feature sizes associated with the newer technology nodes decrease. A state-of-the-art, DFM-aware design flow for CMOS integrated circuits, by Magma Design Automation, as recently as 2006. The design flow for the DFM methodology for digital ICs has been depicted in Figure 125.

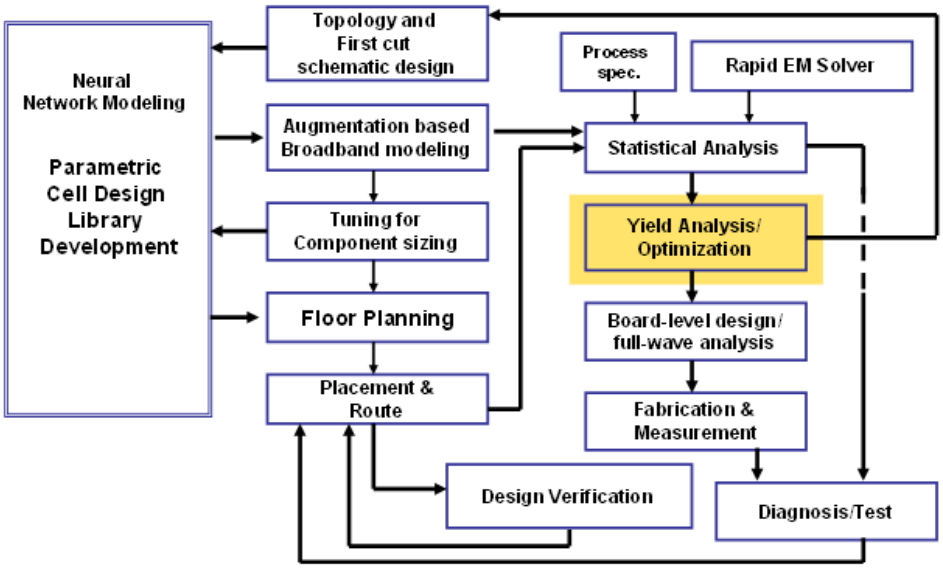

Figure 123. Focus of Chapter V (shaded) in the perspective of an RF CAD framework

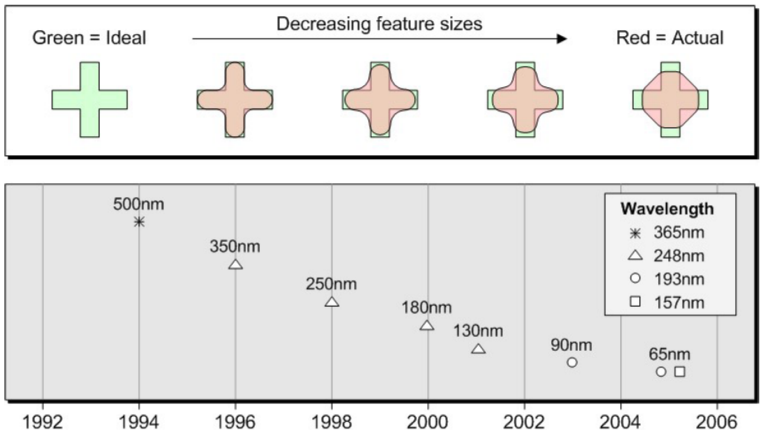

Figure 124. Effect of feature shrinkage on IC interconnect manufacturability.

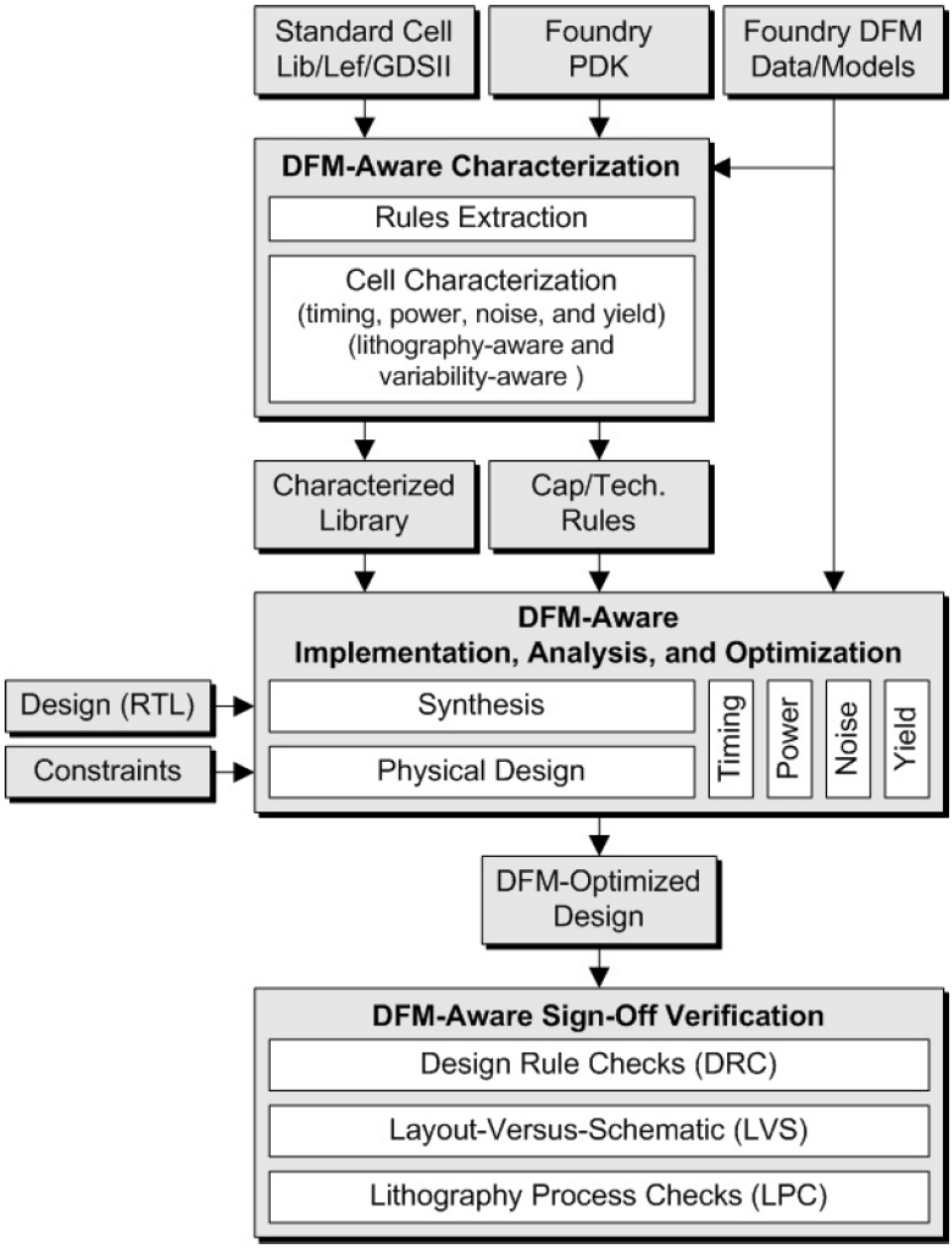

Figure 125. A DFM-aware design flow; from characterization to sign-off verification (Courtesy: Magma Design Automation, Inc.).

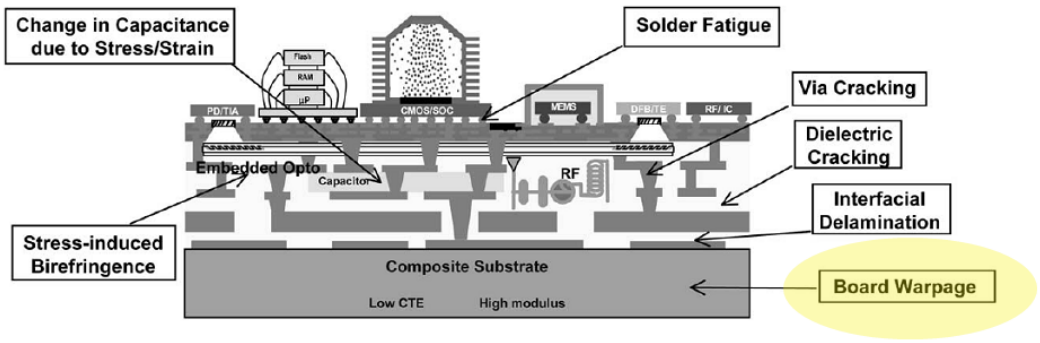

Figure 126. Potential failure mechanisms demonstrated on a conceptual SOP module.

The design of SOP modules is encountering a somewhat different, but equally difficult challenge in the face of faster time-to-market schedules and low cost. In order to highlight the manufacturability concerns of SOP-based systems, the multiple potential mechanisms in the manufacturing of a SOP module has been shown in Figure 126

In addition, with the possibility of large-area manufacturing with LCP, LTCC devices, the need for statistical diagnosis and design centering methods are imperative. A "multi-domain" statistical framework that takes into account the electrical as well as the mechanical parameters for the estimation of performance variations and parametric yield has been detailed in Chapter 4. The application of statistical methods for yield optimization is the focus of this chapter.

5.1 Parametric yield

The performance metrics of mass-produced circuits varies from one to another as a result of the variations of the manufacturing parameters. In addition, there are statistical variations in component values due to the environmental factors such as temperature and humidity. Such variances gives rise to a number of questions concerned with minimizing the undesired effect of component tolerances. Among them, yield maximization (or design centering) problem is of primary importance, simply because yield is a direct measure of profit.

From a designer's perspective, the objective of "high-yield" circuit design is usually:

(1) To fulfill some lower S_j^L and upper S_j^U constraints or (specifications) imposed on the circuit performance functions $y_j(e)$, $j = 1, , m$ such as insertion loss at different frequencies, bandwidth, transmission zero locations, etc. dependent on the vector of circuit elements and parameters.

(2) To realize, as accurately as possible, some of the most desirable (or "best") "target" design specifications (TDS's), S_j^T where

$$S_j^L < S_j^T < S_j^U. \tag{152}$$

Parametric yield is defined as the percentage of the functional components satisfying the performance specifications. Here multiple constraints need to be met e.g. bandwidth, ripple, center frequency. However, due to the manufacturing variations, certain parameters get shifted in the frequency/amplitude spectrum. In such cases, the joint probability density functions of the performance measures was approximated using multi-variate normal distribution [18], which is defined as

$$f_Y(Y) = \frac{\exp\{-1/2([Y] - \mu_Y)^T [Cov(Y,Y)]^{-1}([Y] - \mu_Y)\}}{(2\pi)^2 \left|Cov(Y,Y)\right|^{1/2}}, \tag{153}$$

where Y is the vector of performance measures, and μ_Y is the expected value for the vector Y. As an example, the vector Y and μ_Y vector are defined as:

$$Y = \begin{bmatrix} f\_1dB\_1 \\ f\_1dB\_2 \\ \min\_attn \\ attn\_2\_1GHz \end{bmatrix} \qquad \mu_Y = \begin{bmatrix} 2.3348(GHz) \\ 2.4499(GHz) \\ 2.1714(dB) \\ 31.6096(dB) \end{bmatrix} \tag{154}$$

Covariance of performance measures was computed as [53]

$$Cov(y_m, y_n) = \sum_{i=1}^{4}\sum_{i=1}^{4}\left(\begin{array}{l}\frac{(\beta_{m-ia}\beta_{n-ka})}{2} \\ +\frac{(\beta_{m-ia}+\beta_{m-ib})(\beta_{n-ka}+\beta_{n-kb})}{2} \\ -\frac{(\beta_{m-ia}\beta_{n-ka})}{2\pi}\end{array}\right)\delta(i-k) \qquad (155)$$

where $\beta_{m-ia}, \beta_{m-ib}$, and $\beta_{n-ka}, \beta_{n-kb}$ are pwl coefficients of filter performance measures y_m and y_n respectively and $\delta(i-k)$ is the impulse function. For the manufacturing parameters with linear sensitivity relations, $\beta_{m-ib} = 0$ and $\beta_{n-kb} = 0$. The yield was computed as the integral of Equation 153 over the acceptable region of performance. The yield constraints of a filter design were 1 dB bandwidth cutoff frequencies f_1dB_1 and f_1dB_2, min_attn and $attn\_2\_1GHz$, the attenuation at 2.1 GHz. The constraints included bandwidth of at least 2.35 to 2.45 GHz, maximum attenuation of 2.8 dB and minimum attenuation of 30 dB at 2.1 GHz. The yield is calculated as shown

$$\int_{-\infty}^{2.35}\int_{2.45}^{\infty}\int_{-\infty}^{2.8}\int_{30}^{\infty} f_Y(Y)d_{f\_1dB\_1}d_{f\_1dB\_2}d_{\min\_attn}d_{attn\_2\_1GHz} = 45.7\% \qquad (156)$$

5.2 Yield enhancement and optimization

Further, using the joint probability distribution of performance measures and computing the acceptability function, it can be inferred whether simultaneous constraints on a pair of performance measures is physical or not. This has been shown in Figure 127 and Figure 128. In the figures, the acceptability function (z-axis) has not been normalized. From Figure 127, it can be inferred that, by just the two spikes (indicating design acceptability), simultaneous constraints on the attenuation at 2.1 GHz and the lower 1 dB cutoff frequency leads to a nonphysical result. This means that certain design constraints cannot be met simultaneously and will result in very low yield. On the other hand, the distribution of the acceptability function in Figure 128 implies that it is reasonable to place simultaneous constraints on inband ripple and lower side frequency of the 1 dB bandwidth.

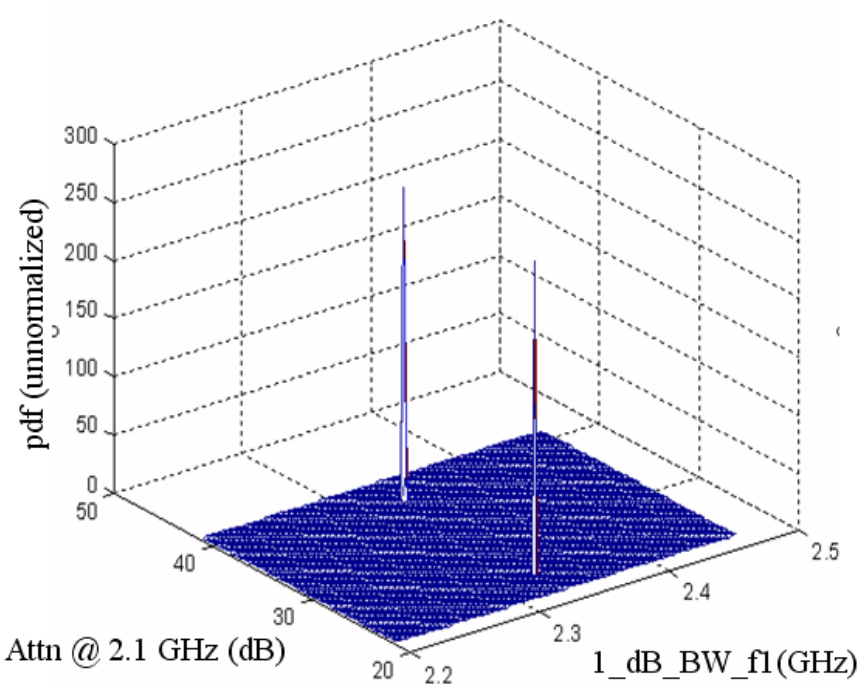

Figure 127. Distribution of design acceptability function using simultaneous constraints on Attenuation @ 2.1 GHz and lower-cutoff frequency of 1 dB bandwidth: isolated spikes indicate that such constraints lead to low yield.

This suggests that the yield of a design can be improved by identifying the parameters on which to place design constraints simultaneously. Here acceptibility function implies whether a device has met the design criteria. The function is positive when they are met. Further, it is clear that the yield of the bandpass filter can be improved by reducing the manufacturing variations. It was also observed that the yield does not increase unless additional performance tolerance was provided. Using figures of joint distributions and yield variations with design tolerance, yield targets can be achieved by the most feasible design and manufacturing changes.

The probability density functions that represent the variations in design parameters are typically gaussian in nature. The design yield, which is computed as an integral of the joint probability density, can therefore be posed as a convex programming problem. A function $f : \mathbf{R}^n \rightarrow \mathbf{R}$ is *convex* if $\mathbf{dom}\, f$ is a convex set and if for

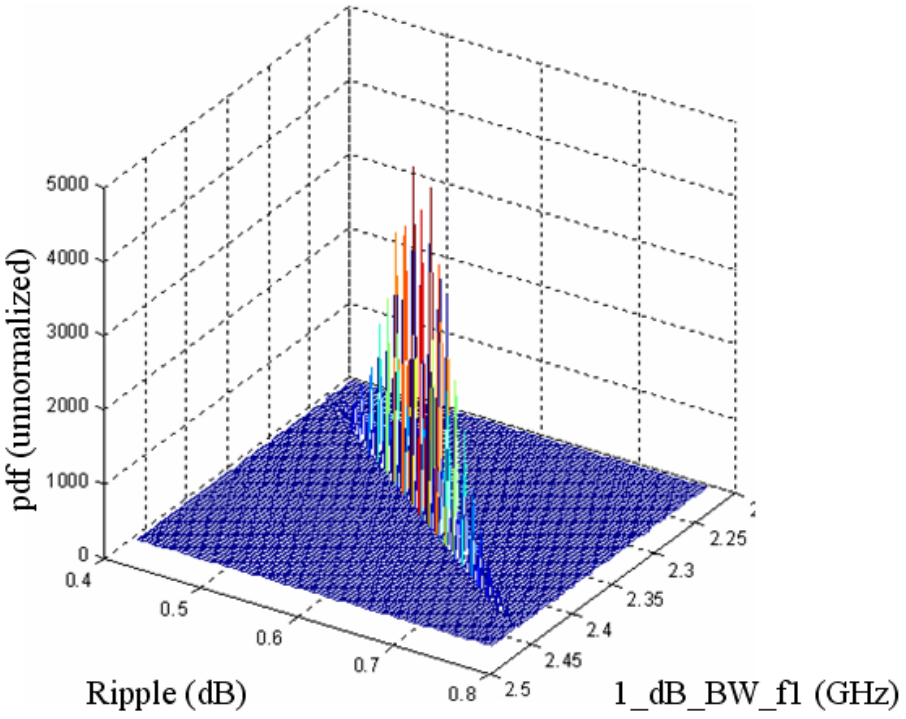

Figure 128. Computation of design acceptability function using simultaneous constraints on inband ripple and lower-cutoff frequency of 1 dB bandwidth: distribution shows that such constraints lead to realizable yield.

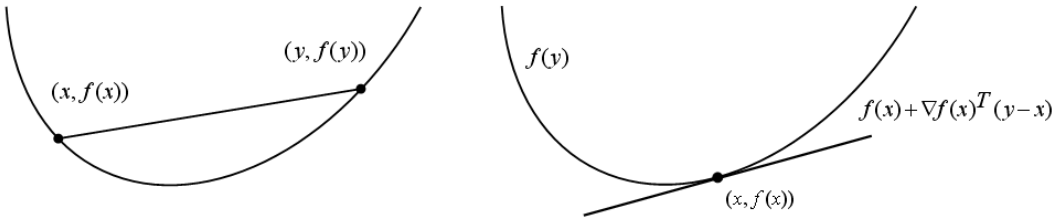

Figure 129. (Left):Graph of a convex function; the chord between *any* two points on the graph lies above the graph. (Right): Graphical illustration of the first-order condition for convexity.

all x, $y \in \mathbf{dom}\, f$, and θ with $0 \leq \theta \leq 1$, we have

$$f(\theta x + (1-\theta)y) \leq \theta f(x) + (1-\theta)f(y) \tag{157}$$

Geometrically, this inequality implies that the line segment between $(x,\ f(x))$ and $(y,\ f(y))$, which is the chord from x to y, lies above the graph of f as shown on the left, in Figure 129. In addition, for first-order conditions, suppose f is differentiable (i.e., its gradient ∇f exists at each point in $dom\, f$, which is open). Then f is convex if and only if $dom\, f$ is convex and

$$f(y) \geq f(x) + \nabla f(x)^T (y-x) \tag{158}$$

holds for all x, $y \in \mathbf{dom}\, f$. This inequality is graphically illustrated on the right, in Figure 129. A conceptual representation of a 3-dimensional convex function is shown in Figure 130.

The joint gaussian *pdf* of n random independent variables $y = (y_1, \cdots, y_n)$,where y_i has a mean x_i and a variance of σ_i^2, is given by [16]

$$\Phi_x(y) = \frac{1}{(2\pi)^{n/2}\sigma_1\sigma_2...\sigma_n} \exp\left[\sum_{i=0}^{n} -\frac{(y_i - x_i)^2}{2\sigma_i^2}\right] \tag{159}$$

where $x = (x_1, \cdots, x_n)$. The above joint distribution is known to be a log-concave function of x and y. Further, arbitrary covariance matrices can be handled, since a symmetric matrix can be converted to the diagonal form by use of orthogonal transformation. The optimization problem is formulated as

$$\text{maximize}\, Y(x) = \int_P \Phi_x(y)dy \tag{160}$$

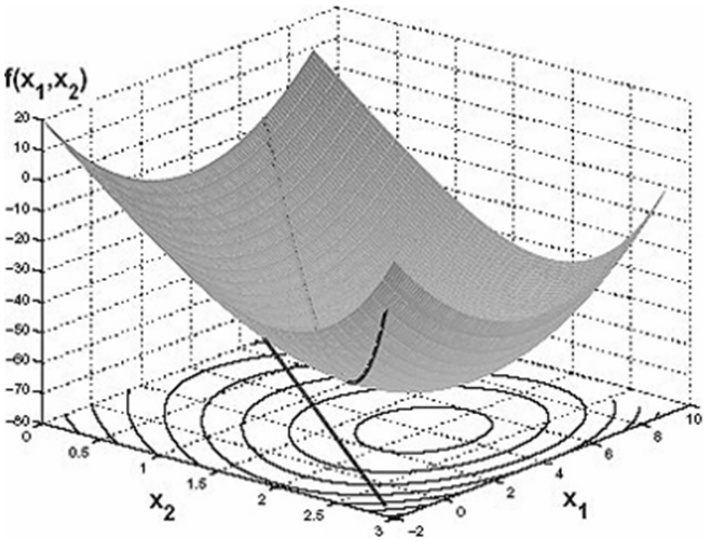

Figure 130. Graphical representation of a convex surface.

such that $x \epsilon P$, where P is the approximation to the feasible region. Since the integral of a log-concave function is also a log-concave function, the problem reduces to maximization of a log-concave function over a convex set. Hence, this can be transformed into a convex programming problem, with the corresponding property that any local minimum of the solution is also the global minimum. This is a desirable criterion in the formulation of the design centering problem. It should be noted that the yield function remain convex as long as $\Phi_{\mathrm{x}}(\mathrm{y})$ is a concave function of x and y. For example, this approach would also be valid for an exponential probability density function. The algorithm proposed in [16] provides an efficient technique for solving a convex programming problem. The algorithm consists of iteratively finding centers of approximated "polytopes" which constitute the feasible region. Let the feasible set be defined as

$$S = x \epsilon \mathbf{R}^n | x \epsilon \mathcal{P} \tag{161}$$

and let x_c be the solution to Equation 160. Initially, a region $\mathcal{Q} = \mathcal{P}$ that contain x_c

is chosen. The region $\mathcal{Q}$ is given by

$$Q = x|\hat{A}z \geq \hat{b}, \hat{A}\,\epsilon\,\mathbf{R}^{p\times n}, \hat{b}\,\epsilon\,\mathbf{R}^{n}. \tag{162}$$

The algorithm proceeds iteratively as follows. First a center z_c , inside the current region $\mathcal{Q}$ is found by minimizing the log-barrier function as

$$F(z) = -\sum_{i=1}^{p} \log(\hat{a}_i^T z - \hat{b}_i), \tag{163}$$

where $\hat{a}_i^T$ is the i^{th} row of matrix $\hat{A}$, and $\hat{b}_i$ is the i^{th} element of $\hat{\mathrm{b}}$. There exists a hyperplane that divides the polytope into two parts such that x_c is contained in one of them, satisfying the constraint

$$c^T z \geq c^T z_c \tag{164}$$

$$\text{with}\, c = -[\nabla Y(x)]^T, \tag{165}$$

being the negative of the gradient of the yield (objective) function. Since the yield function is not available in an explicit form, the gradient is estimated using yield gradient approximation methods. This is computationally much cheaper than repeated circuit/EM simulations with new sets of parameter values. This yield estimator works with the polytope approximation of the feasible region and requires no simulations. A point is considered to be feasible if it lies within the approximating polytope; this leads to a substantial savings in computation, since it is much cheaper to find out whether a point lies within a polytope than to simulate the circuit with a new set of parameter values. In practice, the yield gradient is approximate, and possibly erroneous, as it is based on Monte Carlo simulations. To offset this problem, the new hyperplane is taken as

$$c^T z \geq c^T z_c - \delta \left| c^T z_c \right|, \tag{166}$$

where δ is a small positive number (typically 0.1 or 0.2), representing the fact that the plane is moved away by a certain fraction towards the boundary of the current polytope.

The constraint in (166) is added to the current polytope to give a new region, $\mathcal{Q}$, that has roughly half the original volume. The process is repeated until the polytope is sufficiently small, and the final center z, is taken to be the computed *design center*. The yield function can be written as,

$$Y(x) = \int ... \int h(z)\Phi(z)dz \tag{167}$$

where $h(z) = 0$ if z is not $\in \mathcal{F}$, and $h(z) = 1$ if $z \in \mathcal{F}$. In this method, since we have a polytope approximation, $\mathcal{P}$, to the feasible region, $\mathcal{F}$, we can take an approximation to the yield as

$$Y_{approx}(x) = \int ... \int_F g(z)\Phi(z)dz \tag{168}$$

where $g(z) = 0$ if z is not $\in \mathcal{P}$, and $g(z) = 1$ if $z \in \mathcal{P}$. Thus, the computation of $g(z_k)$ is simply a matter of checking whether the point lies within the polytope or not, which is a computationally cheap operation and does not require an actual circuit simulation. Therefore, the gradient estimate can be written as

$$\begin{aligned} \frac{\partial Y_{approx}}{\partial x_i} &= \int ... \int_P g(z)\frac{\partial \Phi_x(z)}{x_i}dz \\ &= \int ... \int_P \left[\frac{g(z)}{\Phi_x(z)}\frac{\partial \Phi_x(z)}{\partial x_i}\right]\Phi_x(z)dz. \end{aligned} \tag{169}$$

An approximate estimate (based on a sample of N points) for yield gradient, based on the gradient function as

$$\frac{\partial \hat{Y}}{\partial x_i} = \frac{1}{N}\sum_{k=0}^{N}\frac{g(z_k)}{\Phi_x(z_k)}\frac{\partial \Phi_x(z_k)}{\partial x_i} \tag{170}$$

where $g(z) = 0$ when z is not $\in P$ and $g(z) = 1$ when $z \in P$.

The formulation was applied to multiple test cases, for bandpass filters with different design specifications. The first test case has a nominal set of design parameters

as shown in the initial estimate column. The optimized parameters have been depicted in the other column (optimized estimate). The results of optimization have been shown in Table 18.

Table 18. Test case I: Performance measures before and after convex optimization

Perf. metric mean	Initial estimate	Optimized estimate
μ IL (dB)	2.03	2.18
μ BW (GHz)	0.225	0.242
μ attn @ 3.5 GHz (dB)	35	30
μ fc2 (GHz)	2.45	2.43

The table shows the change in the mean of the performance measures as a result of the optimization of the design parameters. A yield improvement of 14% has been observed based on the aforementioned analysis. Further, it is to be noted that the performance variations were allowed within the acceptable region of variations, such that the optimized estimates of the performance measures fall within the valid region of design specifications.

For the second test case, again with a bandpass filter, the initial design parameters of the filter have been shown in Table 19. The optimized parameters have been shown in next column (optimized estimate). The yield improvement, after the optimization of the performance measures, was seen to be around $\sim$ 5%. As explained in the

Table 19. Test case II: Performance measures before and after convex optimization

Perf. metric mean	Initial estimate	Optimized estimate
μ IL (dB)	1.8	2.0
μ BW (GHz)	0.150	0.142
μ attn @ 4.2 GHz (dB)	43	35
μ fc2 (GHz)	2.15	2.11

previous test case, the variations were allowed within the acceptable region of the performance measures.

For the third test case, the initial and the optimized performance measures of the filter have been shown in Table 20. The convex programming formulation, using polytopal approximation and the yield gradient estimation, were applied to the feasible region of performance measures. As before, the inequality constraints for the yield cost function were provided by the allowable region of the performance measures. The yield improvement, after the optimization of the performance measures, was seen to be around $\sim 6.6\%$. As explained in the previous test case, the variations

Table 20. Test case III: Performance measures before and after convex optimization

Perf. metric mean	Initial estimate	Optimized estimate
μ IL (dB)	2.3	1.9
μ BW (GHz)	0.330	0.319
μ attn @ 5.8 GHz (dB)	50	43
μ fc2 (GHz)	1.9	1.93

were allowed within the acceptable region of the performance measures.

5.3 Summary

The rapidly evolving telecommunications market has led to the need for advanced RF circuits. Complex multi-band/multi-mode RF designs require accurate prediction early in the design schedule and time-to-market pressures require that design (circuit/electromagnetic) iterations be kept to a minimum. In this chapter, a layout-level, yield optimization technique for embedded RF circuits for SOP-based wireless applications have been presented. The passive portion of the RF circuits is composed of embedded inductors and capacitors in low loss, multi-layer substrate. The statistical analysis takes into account the effect of the thermo-mechanical stress effects and the process variations that are incurred in batch fabrication. Yield enhancement methods based on joint probability distribution and constraint-based convex programming has also been presented. The results show good correlation with measurement/electromagnetic (EM) data.

CHAPTER 6
CONCLUSIONS AND FUTURE WORK

The emergence of multi-band communications standards, and the fast pace of the consumer electronics market for wireless/cellular applications emphasize the need for fast design closure. In addition, there is a need for electronic product designers to collaborate with manufacturers, gain essential knowledge regarding the manufacturing facilities and the processes, and apply this knowledge during the design process. In this dissertation, efficient layout-level circuit sizing techniques, and methodologies for design-for-manufacturability have been investigated.

Firstly, design complexity increases due to the increase in circuit functionality of current celular/wireless devices. In addition, the RF designers have to deal with multiple design constraints to meet several performance specifications across multiple frequency bands, simultaneously. Manual iterations in circuit solvers and field solvers are typically employed in design flows to meet such design goals. These design iterations, however, can become computationally prohibitive. Consequently, time-efficient design closure is becoming increasingly difficult in the design of modern communications systems.

Secondly, system-on-package (SOP)-based technologies have emerged as strong candidates for the integration platform of next-generation, multi-functionality communications devices. However, the current design flow for the SOP-based systems is not as efficiently modularized into multiple levels of physical and logical abstraction as its SOC counterpart. Specifically, optimum design metrics do not translate to optimum manufacturing metrics. Therefore, design-for-manufacturability methods are imperative. Previous work have focussed on circuit-level and layout-level optimization, but not on design scaling methodologies. Also, extensive research, in the field of DFM, has been conducted for submicron technology nodes for digital ICs, but little

work, to the best of the author's knowledge, have been performed on statistical design and yield optimization of packaged RF circuits.

With the proposed circuit/component sizing approach, RF layouts can be modified to meet different frequency specifications, with minimum iterations of EM simulations. In particular, a layout segmentation, modeling, and mapping technique has been developed for the scaling of embedded RF components, such as, quasi-lumped, embedded inductors, and bandpass filters. Further, a circuit augmentation technique has been proposed; to perform broadband modeling for library model development, and circuit-based tuning of performance measures. Finally, diagnosis of prototype RF filters have been demonstrated, based on the aforementioned circuit scaling methodology.

Furthermore, with the proposed statistical framework, probabilistic diagnosis could be performed on batch-fabricated designs. In the statistical analysis, the effects of electrical, as well as mechanical parameters to assess the effect of micro parameters, such as line-width, dielectric thickness variations, and macro parameters, such as board warpage, have been investigated. The statistical analysis framework was combined with a constraint-based convex optimization scheme to perform yield optimization of embedded RF circuits.

6.1 Conclusions

Based on the work presented in Chapters 2 through 5, the contributions of this research can be listed as follows:

(a) A circuit augmentation technique for broadband modeling of components, required for library development and circuit sizing. The circuit augmentation technique is based on a previously developed circuit partitioning technique, a

modified nodal analysis formulation and a linear optimization framework. Physical design constraints in the circuit augmentation algorithm that has been implemented in this work ensures passivity and stability of the broadband model. The technique has been verified for broadband modeling of spiral inductors, planar capacitors. The circuit augmentation technique has also been applied for the tuning of bandpass filters. Comparisons have been performed with tuning using commercial circuit simulators, employing nonlinear optimization, to demonstrate the advantages of the proposed technique.

(b) A library development technique for embedded inductors/capacitors in multilayer substrate has been presented. The methodology employs artificial neural networks to develop a neuro-model for the embedded passives. A fast weight optimization algorithm (Levenberg-Marquadt algorithm) was implemented for fast training of the neural networks. In addition, an adaptive sampling algorithm is implemented to reduce the size of design library that is required for neural network training and validation. The proposed modeling and library develpment methodology is ideally suitable for multi-layer structures with no more than four metallization layers.

(c) A layout-level circuit scaling technique for RF passive circuits with quasi-lumped embedded inductors and capacitors has been demonstrated. The proposed approach is based on a combination of segmented lumped circuit modeling, nonlinear mapping using polynomial functions, artificial neural network (ANN)-based methods, and circuit-level optimization. The methodology has been validated on measured and simulated frequency response data of RF bandpass filters, filters with transmission zeros, and dual-band filters. The circuit augmentation technique has also been applied for the tuning of bandpass filters.

Comparisons have been performed with tuning using commercial circuit simulators, employing nonlinear optimization, to demonstrate the advantages of the proposed technique, that is based on a linear optimization framework.

(d) An extension of the circuit scaling technique to layout-level diagnosis of prototype circuits has been proposed. The fabricated designs require diagnosis of variations in performance metrics such as center frequency, bandwidth and transmission zeros that occurs due to process variations. Synthesis methodology was applied to map the variations in electrical parameters to component geometries. The synthesized results predict the possible variations in physical parameters that have been confirmed with measurements of the fabricated devices.

(e) This dissertation presents a layout-level, multi-domain DFM methodology and yield optimization technique for embedded RF circuits for SOP-based wireless applications. The passive portion of RF circuits is composed of quasi-lumped embedded inductors and capacitors in low loss, multi-layer substrate. The proposed methodology consists of stochastic circuit/EM modeling, layout-level statistical diagnosis and parametric yield optimization.

The proposed statistical diagnosis technique is based on layout segmentation, lumped element modeling, sensitivity analysis and extraction of probability density function using convolution methods. The statistical analysis takes into account the effect of the thermo-mechanical stress/warpage effects and the process variations that are incurred in batch fabrication. Yield enhancement and optimization methods based on joint probability distribution and constraint-based convex programming has also been presented. The results show good correlation with measurement and EM simulation data for embedded, RF bandpass filters fabricated in LCP-based substrate.

6.2 Future work

Layout-level circuit sizing is an critical bottleneck in the design cycle of RF modules. For multi-band architectures, that require design of circuits with large number of passive components (greater than 30 in filter banks, for example), manual intervention through EM simulations is prohibitively time-consuming. An ideal layout-level circuit sizing methodology would require a broadband, quasi-physical physical modeling framework, and an efficient, multi-dimensional parameterizations technique. The parameterization technique should be able to map the S-parameters of the components to the physical parameters of the corresponding layout. The framework of the first stage of modeling has been demonstrated in this dissertation. Though several published works have researched on efficient parameterization techniques for digital interconnects, none of them addresses the need for developing a similar framework for efficient circuit sizing of RF circuits. Development of a parameterization methodology could be a good extension to the work accomplished in this dissertation. Another possible and useful area of development in this research is the analysis of coupling, and thereby include coupled structures in the broadband modeling technique. This is useful for the optimization of dense layout topologies, where the consideration of near-field EM coupling is critical to the accurate calculation of performance measures.

Another possible area of future work lies in the development of a computationally robust framework for the DFM methodology that has been presented in this dissertation. Computation of gradient information is a critical issue that needs to be addressed in optimization technique in large "variable space". A survey (and implementation, if required) of the different available optimization schemes need to be performed to develop a quantitative reference estimate of the appropriate scheme, to be applied to the DFM framework. Global and evolutionary algorithms such as genetic optimization can be a good starting point in this direction. In addition, inclusion of the package-level parameters in the scheme of statistical design centering

would result in a true, multi-domain DFM framework. Future work in this direction will have a significant impact on the economy of manufacturability for SOP-based RF circuits and systems.

6.3 Publications and Invention Disclosures

The following publications and invention disclosures have resulted during the course of the research

- **S. Mukherjee**, S. Dalmia, B. Mutnury and M. Swaminathan, "Layout-level synthesis of RF bandpass filter on organic substrates for Wi-Fi applications," in *Proc. IEEE European Microwave Conf.*, pp. 1324-1327, Oct. 2004, Amsterdam, Netherlands.

- **S. Mukherjee**, B. Mutnury, S. Dalmia and M. Swaminathan, "Synthesis and optimization of embedded inductors on organic substrate using knowledge-based artificial neural networks," in *Proc. IEEE Asia-Pacific Microwave Conf.*, pp. 501-504, Dec. 2004, New Delhi, India.

- **S. Mukherjee**, B. Mutnury, S. Dalmia and M. Swaminathan, "Layout-level synthesis of RF inductors and filters in LCP substrates for Wi-Fi applications," *IEEE Trans. Microwave Theory and Tech*, pp. 1212-1228, vol.6, no.52, June 2005.

- **S. Mukherjee**, M. Swaminathan and S. Dalmia, "Synthesis and diagnosis of RF filters in LCP substrates," *Proc. IEEE MTT-S Int. Microwave Symp.*, pp. 1412-1415, Long Beach, CA, June 2005.

- **S. Mukherjee**, M. Swaminathan and E. Matoglu, "Statistical analysis and diagnosis methodology for RF circuits in LCP substrates," *IEEE Trans. Microwave Theory and Tech.* Nov. 2005, vol.11, no. 52, pp. 3621-3630.

- **S. Mukherjee**, M. Swaminathan and E. Matoglu "Statistical diagnosis and parametric yield analysis of LCP based RF dualband filters," *Proc. IEEE 36th European Microwave Conf.*, pp. 74-77, Paris, France, Oct. 2005.

- **S. Mukherjee** and M. Swaminathan "Design-for-manufacturability methodology and yield analysis of embedded RF circuits for system-in-package (SiP) applications", *Proc. IEEE Asia Pacific Microwave Conf.*, vol.3, pp. 465-468, Yokohama, Japan, Dec. 2006.

- **S. Mukherjee**, M. Swaminathan and S.N. Lalgudi "Broadband modeling and tuning of multi-layer embedded RF circuits using a physical augmentation methodology", submitted for review to *Asia Pacific Microwave Conf.*, Bangkok, Thailand, Dec. 2007.

- S.Dalmia, A.Bavisi, **S. Mukherjee**, V. Govind, G. White, M. Swaminathan and V. Sundaram, "A multiple frequency signal generator for 802.11a/b/g VoWLAN type applications using organic packaging technology," Proc. of *IEEE Electron. Comp. and Technl. Conf*, pp. 1664-1670, June 2004.

- V. Govind, **S. Mukherjee**, S. Dalmia and M. Swaminathan, "Digitally tunable compact multiband low noise amplifiers (LNA) through passive re-use," *Georgia Tech Invention Disclosure no. 2893*, April 2003.

- **S. Mukherjee** and M. Swaminathan "Design-for-manufacturability (DFM) methodology and yield analysis for embedded RF passive circuits for system-in-package (SIP) applications," *Georgia Tech Invention Disclosure no. 3866*, October 2006.

APPENDIX A
CIRCUIT PARTITIONING

The mathematical details of the circuit partitioning technique have been dscribed in this appendix. The effect on the circuit node voltages of the addition of an impedance z between the two nodes of a circuit k and l, has been explained. It is first assumed that an initial circuit has been solved by means of nodal analysis:

$$Yv = I \tag{171}$$

Therefore, the solution vector v is given by

$$v = Y^{-1}I \tag{172}$$

Here v is an $n\times1$ vector of nodal voltages, Y is an $n\times n$ nodal admittance matrix, and I is an $n\times1$ vector of (equivalent) source node currents. The effect of the augmentation of an impedance z between the nodes m and n is determined as follows. Firstly the connection vector, representing the augmentation between the two nodes m and n is given by

$$\xi_{kl} \equiv [0\ ...0\quad +1\quad 0...0\quad -1\quad 0...0]^T \tag{173}$$

where a "+1" is present in the mth row, a "-1" is present in the nth row, and zeros everywhere else. In other words, the connection vector, for an augmentation element, represents the incidence relation for the element that is being added between the two nodes. In the case where the augmentation is between a node and a ground, the element "-1" in the connector vector in Equation 173 is replaced by a "0"; the rest of the vector remains the same. Following Equation 173, the open-circuit voltage v_{oc} between the nodes m and n can be written as

$$v_{oc} = v_m - v_n = \xi_{mn}^T v = \xi_{mn}^T Y^{-1} I \tag{174}$$

where ξ_{mn}^T denotes the transpose of ξ_{mn}. Then, let all independent sources in the original circuit are set to zero and a one amp current source is connected between the nodes m and n. Then, the node equations are replaced with

$$Yv' = \xi_{mn}. \tag{175}$$

In this case, the nodal voltage vector is given by

$$v' = Y^{-1}\xi_{mn}. \tag{176}$$

The specific voltage between nodes m and n would be the Thevenin equivalent impedance is given by

$$z_{TH} = v'_m - v'_n = \xi_{mn}^T Y^{-1}\xi_{mn} \tag{177}$$

Therefore, the Thevenin loop current(in Figure) is given by

$$i_z = \frac{-v_{oc}}{z + z_{TH}}. \tag{178}$$

If, by linearity,$i_z = 1$, then, it implies

$$v' = Y^{-1}\xi_{mn} \tag{179}$$

for the node voltage vector, then

$$i_z = -\frac{v_{oc}}{z + z_{TH}} \tag{180}$$

implies

$$v'' = -\frac{v_{oc}}{z + z_{TH}} Y^{-1}\xi_{mn}, \tag{181}$$

for the nodal voltage vector. By superposition, the overall voltage $\hat{v}$ is given by

$$\hat{v} = v - \frac{v_{oc}}{z + z_{TH}} Y^{-1}\xi_{mn} \tag{182}$$

or

$$\hat{v} = Y^{-1}\left(I - \frac{\xi_{mn}^T Y^{-1} I}{z + \xi_{mn}^T Y^{-1}\xi_{mn}}\xi_{mn}\right). \tag{183}$$

APPENDIX B

DESIGN GUIDELINES FOR MANUFACTURING IN CURRENT LCP PROCESS

A mature manufacturing process is associated with a well-characterized set of design rules and guidelines. Some ground rules have to be strictly satisfied to avoid design rule check (DRC) errors. In addition, there are additional design practices to ensure that unwanted EM coupling, parasitics, and current crowding effects are *minimized* in the design process, prior to fabrication. Moreover, these design guidelines will prove useful to set up physical and electrical constraints in an automatic, "performance-aware", place-and-route tool, if developed for the floorplanning and layout optimization of RF circuit layouts. Some important design practices for the manufacturing of embedded circuits in the LCP process have been listed in this appendix.

The guidelines have been listed as follows:

(1) The minimum line-width is 3 mils, for all layers, except the top layer. The minimum line-width for the topmost metal layer is 4 mils. The minimum line-spacing, for all layers, is 3 mils.

(2) Line-to-line coupling can be neglected, if the separation between the lines is equal to, or more than 10 times the thickness of the LCP dielectric layer.

(3) The routing is performed (manually) by the designers based on its associated inductance and resistance and how much it affects the overall response of the circuit (the circuit models and the cost functions will be useful here).

(4) The length of interconnects is kept to a minimum (between components) so that extensive re-sizing of components is not required due to addition of inductance, loss and the parasitics of the interconnects.

(5) In accordance with the symmetric placement of similar sized components, the interconnects connecting the components are also placed symmetrically about the midline of the layout w.r.t i/p and o/p ports (unless coupling is desired between the lines).

(6) Routing of interconnects is generally avoided next to inductors to avoid in-line coupling; orthogonal orientation is usually preferred. However, this design practice has less weight if, due to such a placement, the interconnect length is increased excessively leading to significant change in performance (significant variation in cost function).

(7) Routing of interconnects parallel to capacitors do not pose similar extent of performance variations (with the current width of lines in our designs).

(8) Layer transitions of interconnects through micorvias/thruholes is kept to a minimum due to the inductive effects of vias.

(9) While routing on any layer with capacitors/inductors on layers above/below, overlap (effects of overlapping capacitance) is avoided.

APPENDIX C

VECTOR FITTING BY POLE RELOCATION

Consider the rational function approximation

$$f(s) \approx \sum_{n=1}^{N} \frac{c_n}{s - a_n} + d + sh, \tag{184}$$

where the residues c_n and the poles a_n are either real quantities or come in complex conjugate pairs, while d and h are real numbers. The underlying problem is to estimate all the coefficients in Equation 184 so that a least squares estimation of $f(s)$ is obtained over a given frequency interval. It is to be noted that Equation 184 is a *nonlinear* problem in terms of the unknowns, because the unknowns a_n appear in the denominator. Vector fitting solves the problem in 184 sequentially as a *linear* problem in two stages, both times with known poles.

C.1 Pole identification

A set of starting poles $\bar{a}_n$ is specified in 184, and $f(s)$ is multiplied with an unknown function $\sigma(s)$. In addition, a rational approximation for $\sigma(s)$ is introduced. Correspondingly, the augmented problem is given by

$$\begin{bmatrix} \sigma(s)f(s) \\ \sigma(s) \end{bmatrix} \approx \begin{bmatrix} \sum_{n=1}^{N} \frac{c_n}{s-\bar{a}_n} + d + sh \\ \sum_{n=1}^{N} \frac{\tilde{c}}{s-\bar{a}_n} + 1 \end{bmatrix}. \tag{185}$$

It can be seen that the rational approximation for $\sigma(s)$ has the same poles as $\sigma(s)f(s)$. Multiplying the second row in (185) with $f(s)$ yields

$$\left(\sum_{n=1}^{N} \frac{c_n}{s - a_n} + d + sh \right) \approx \left(\sum_{n=1}^{N} \frac{\tilde{c}_n}{s - \bar{a}_n} + 1 \right) f(s), \tag{186}$$

or

$$(\sigma f)_{fit}(s) \approx \sigma_{fit}(s) f(s). \tag{187}$$

Equation 186 is *linear* in its unknowns c_n, d, h, $\tilde{c}_n$. Writing (186) for several frequency points provides the overdetermined linear problem

$$Ax = b \tag{188}$$

A rational function approximation for $f(s)$ can be readily obtained from (186). This is clear when each sum of partial fractions in (186) is written as

$$(\sigma f)_{fit}(s) = h\frac{\prod_{n=1}^{N+1}(s - z_{n)}}{\prod_{n=1}^{N}(s - \bar{a}_n)}, \sigma_{fit}(s) = \frac{\prod_{n=1}^{N}(s - \tilde{z}_n)}{\prod_{n=1}^{N}(s - \bar{a}_n)} \tag{189}$$

From (189), we get

$$f(s) = \frac{(\sigma f)_{fit}(s)}{\sigma_{fit}(s)} = h\frac{\prod_{n=1}^{N+1}(s - z_n)}{\prod_{n=1}^{N}(s - \tilde{z}_n)}. \tag{190}$$

It can be seen in (190) that the poles of f(s) become equal to the zeros of $\sigma_{fit}(s)$. Thus, by calculating the zeros of $\sigma_{fit}(s)$, a good set of poles for fitting the original function $f(s)$ can be obtained.

VITA

Souvik Mukherjee was born in Kolkata, India on December 24, 1979. He received the B.Tech (Hons.) degree in electronics and electrical communication engineering in 2002 from the Indian Institute of Technology, Kharagpur, India, the M.S. degree in electrical and computer engineering in 2004 and the Ph.D. degree in 2007 from the Georgia Institute of Technology, Atlanta.

To pursue his Ph.D. in electrical and computer engineering, he began his research with Professor Madhavan Swaminathan in 2003 as a Graduate Research Assistant in Packaging Research Center, Georgia Institute of Technology. In the summer of 2005, he interned at Analog Devices Inc., Greensboro, NC, where he was involved with electromagnetic modeling and simulation of RF front-ends for wireless local area network (WLAN) applications. His research topic involves broadband modeling, simulation, synthesis and diagnosis of embedded RF passive circuits. He has contributed to several publications and a couple of invention disclosures in the fields of RF synthesis and statistical manufacturability analysis.

Souvik Mukherjee is currently working as an RF characterization engineer with Texas Instruments Inc., Dallas.

REFERENCES

[1] S. Dalmia, V. Sundaram, G. White, and M. Swaminathan, "Liquid crystalline polymer based RF/wireless components for multi-band applications," in *IEEE Proc. of Electronic Components and Technology Conference*, pp. 1866–1873, June 2004.

[2] V. Govind, S. Dalmia, V. Sundaram, G. White, and M. Swaminathan, "Design of multiband baluns on liquid crystalline polymer (LCP) based substrates," in *IEEE Proc. of Electronic Components and Technology Conference*, pp. 1812–1818, 2004.

[3] A. Sutono, A. H. Pham, J. Laskar, and W. R. SMith, "RF microwave characterization of multilayer ceramic-based MCM technology," *IEEE Trans. Advanced Packaging*, vol. 22, no. 3, pp. 326–331, Aug. 1999.

[4] G. Carchon, K. Vaesen, S. Brebels, W. D. Raedt, E. Beyne, and B. Nauwelaers, "Multilayer thin-film MCM-D for the integration of high-performance RF and microwave circuits," *IEEE Trans. Components and Packaging Technology*, vol. 24, no. 3, pp. 510–519, Sept. 2001.

[5] M. Samber, N. Pulsford, N. Delden, and R. Milson, "Low complexity MCM-D technology with integrated passives for high frequency applications," in *IEEE Proc. of International Conference on Multichip Modules and High Density Packaging*, pp. 285–290, 2004.

[6] R. R. Tummala, "Moore's law meets its match (system-on-package)," *IEEE Spectrum*, vol. 43, no. 1, July 2006.

[7] http://www.cadence.com/products/custom_ic/index.aspx, August 2006.

[8] W. Ryu, J. Kim, N. Kim, S. Ahn, S. Kim, H. Song, S. Lee, and J. Kim, "A low-cost high-density RF multi-chip module transceiver for 1.8 GHz personal communication service," in *IEEE Proc. of Electronic Components and Technology Conference*, pp. 193–197, 2000.

[9] A. Bavisi, *Integrated multi-mode oscillators and filters for multi-band radios using liquid crystalline polymer based packaging technology.* PhD thesis, Georgia Institute of Technology, 2006.

[10] S. Dalmia, *Design and Implementation of high Q passive devices for wireless applications using SOP based Organic technologies.* PhD thesis, Georgia Institute of Technology, 2002.

[11] http://eesof.tm.agilent.com/applications/sip-b.html, June 2003.

[12] J. M. Hammersley and D. C. Handscomb, *Monte Carlo methods*. New York: Chapman and Hall, 1983.

[13] R. R. Tummala and J. Laskar, "Gigabit wireless: system-on-a-package technology," *Proc. in IEEE*, vol. 92, pp. 376–387, Nov. 1992.

[14] R. R. Tummala, M. Swaminathan, M. Tentzeris, J. Laskar, G. K. Chang, S. Sitaraman, D. Keezer, D. Guidotti, Z. Huang, K. Lim, L. Wan, S. Bhattacharya, V. Sundaram, F. Liu, and P. M. Raj, "The SOP for miniaturized, mixed-signal computing, communication, and consumer systems of the next decade," *IEEE Trans. Advanced Packaging*, vol. 27, pp. 250 – 267, May 2004.

[15] V. Sundaram, F. Liu, S. Dalmia, G. White, and R. Tummala, "Process integration for low-cost system on a package (SOP) substrate," in *IEEE Proc. of Electronic Components and Technology Conference*, pp. 535–540, June 2001.

[16] V. Govind, *Design of baluns and low noise amplifiers in integrated mixed-signal organic substrates*. PhD thesis, Georgia Institute of Technology, 2005.

[17] K. O, "Estimation methods for quality factors of inductors fabricated in silicon integrated circuit process technologies," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 8, pp. 1249–1252, Aug. 1998.

[18] M. Park, S. Lee, C. S. Kim, H. K. Yu, J. G. Koo, and K. S. Nam, "The detailed analysis of high Q CMOS-compatible microwave spiral inductors in silicon technology," *IEEE Trans. Electron Devices*, vol. 33, no. 8, pp. 1249–1252, Aug. 1998.

[19] A. M. Niknejad and R. G. Meyer, "Analysis, design and optimization of spiral inductors and transformers for Si RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1470–1481, Oct. 1998.

[20] T. L. Brandon, B. F. Cockburn, and D. G. Elliott, "HDL2GDS: a fully automated ASIC digital design flow," in *IEEE Proc. of Canadian Conference in Electrical and Computer Engineering*, pp. 1535–1538, 2005.

[21] R. V. Pucha, S. Hegde, M. Damani, K. Tunga, A. Perkins, S. Mahalingam, G. Ramakrishna, G. C. Lo, K. Klein, J. Ahmad, and S. K. Sitaraman, "System-level reliability assessment of mixed-signal convergent microsystems," *IEEE Trans. Advanced Packaging*, vol. 27, no. 2, pp. 438–452, May 2004.

[22] G. Coen and D. D. Zutter, "Automatic derivation of equivalent circuits for general microstrip discontinuities," *IEEE Trans. Microwave Theory and Techniques*, vol. 43, no. 12, pp. 2536–2544, Dec. 1996.

[23] J. Sercu and F. Demuynck, "Electromagnetic/circuit co-optimization of lumped component and physical layout parameters using generalized layout components," in *IEEE Proc of MTT-S International Microwave Symposium*, pp. 2073–2076, June 2002.

[24] J. D. Geest, T. Dhaene, N. Fach, and D. D. Zutter, "Adaptive cad-model building algorithm for general planar microwave structures," *IEEE Trans. Microwave Theory and Techniques*, vol. 47, no. 11, pp. 1801–1809, Nov. 2002.

[25] D. Zutter, J. Sercu, T. Dhaene, J. D. Geest, F. J. Demuynck, S. Hammadi, and C. W. P. Huang, "Recent trends in the integration of circuit optimization and full-wave electromagnetic analysis," *IEEE Trans. Microwave Theory and Techniques*, vol. 52, no. 1, pp. 245–256, Jan. 2004.

[26] J. W. Bandler and S. A. Chen, "Circuit optimization: The state of the art," *IEEE Trans. Microwave Theory and Techniques*, vol. 36, no. 2, pp. 424–442, Feb. 1988.

[27] J. W. Bandler, "Optimization methods for computer-aided design," *IEEE Trans. Microwave Theory and Techniques*, vol. 17, no. 8, pp. 533–552, Aug. 1969.

[28] R. K. Brayton, G. D. Hachtel, and A. L. Sangiovanni-Vincentelli, "A survey of optimization techniques for integrated-circuit design," *Proc. in IEEE*, vol. 69, pp. 1334–1362, Oct. 1981.

[29] T. Shibata, "Circuit simulations combined with the electromagnetic field analysis," *IEEE Trans. Microwave Theory and Techniques*, vol. 39, no. 11, pp. 1862–1868, Nov. 1991.

[30] M. D. M. Hershenson, S. S. Mohan, S. P. Boyd, and T. H. Lee, "Optimization of inductor circuits via geometric programming," in *IEEE Proc. of Design Automation Coneference*, pp. 994–998, June 1999.

[31] R. C. Lee, G. A. Lee, and M. Megahed, "Design and analysis of embedded inductor on low cost multilayer laminate MCM technology," in *IEEE Proc. of Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 83–86, Oct. 2003.

[32] W. Pinello, A. Cangellaris, and A. Ruehli, "Hybrid electromagnetic modeling of noise interactions in packaged electronics based on the partial-element-equivalent-circuit formulation," *IEEE Trans. Microwave Theory and Techniques*, vol. 45, no. 2, pp. 1889–1896, Oct. 1997.

[33] J. W. Bandler, R. M. Biernacki, S. H. Chen, P. A. Grobelny, and R. H. Hemmers, "Space-mapping technique for electromagnetic optimization," *IEEE Trans. Microwave Theory and Techniques*, vol. 42, no. 12, pp. 2536–2544, Dec. 1994.

[34] Q. J. Zhang, K. C. Gupta, and V. K. Devabhaktuni, "Artificial neural networks for RF and microwave design-from theory to practice," *IEEE Trans. Microwave Theory and Techniques*, vol. 51, no. 4, pp. 1339–1349, Apr. 2003.

[35] V. K. Devabhaktuni, M. C. E. Yagoub, and Q. J. Zhang, "Artificial neural networks for RF and microwave design - from theory to practice," *IEEE Trans. Microwave Theory and Techniques*, vol. 49, no. 12, pp. 2282–2291, Dec. 2001.

[36] A. Suntives, M. S. Hossain, J. Ma, R. Mittra, and V. Veremey, "Application of artificial neural network models to linear and nonlinear RF circuit modeling," *IEEE International Journal RF Microwave Computer-Aided Engineering*, vol. 4, no. 5, pp. 231–247, July 2001.

[37] K. L. Wu, R. Zhang, M. Ehlert, and D. G. Fang, "An explicit knowledge-embedded space mapping and its application to optimization of LTCC RF circuits," *IEEE Trans. Components and Packaging Technology*, vol. 26, no. 2, pp. 399–406, June 2003.

[38] K. L. Wu, Y. J. Zhao, J. Wang, and M. Chen, "An effective dynamic coarse model for design optimization of LTCC RF circuits with aggressive space mapping," *IEEE Trans. Microwave Theory and Techniques*, vol. 52, no. 1, pp. 393–402, Jan. 2004.

[39] S. H. Min, *Automated Construction of Macromodels from Frequency Data for Simulation of Distributed Interconnect Networks*. PhD thesis, Georgia Institute of Technology, 2004.

[40] K. Lee, S. Mohammadi, P. K. Bhattacharya, and L. P. B. Katehi, "Scalable compact models for embedded passives," in *IEEE Proc. of 37th European Microwave Conference*, pp. 11–14, 2005.

[41] R. Achar and M. Nakhla, "Simulation of high-speed interconnects," *Proc. in IEEE*, vol. 89, no. 5, pp. 693–728, May 2001.

[42] M. Celik and A. C. Cangellaris, "Simulation of dispersive multiconductor transmission lines by Padé approximation via the Lancoz process," *IEEE Trans. Microwave Theory and Techniques*, vol. 44, no. 12, pp. 2525–2535, Dec. 1996.

[43] S. H. Min and M. Swaminathan, "Efficient construction of two-port passive macromodels for resonant networks," in *IEEE Proc. of 10th Topical Meeting of Electrical Performance of Electronic Packaging*, pp. 229–232, Oct. 2001.

[44] L. Daniel and J. Phillips, "Model order reduction for strictly passive and causal distributed systems," in *IEEE Proc. of Design Automation Conference*, pp. 46–51, June 2002.

[45] D. Saraswat, R. Achar, and M. S. Nakhla, "A fast algorithm and practical considerations for passive macromodeling of measured/simulated data," *IEEE Trans. Advanced Packaging*, vol. 27, no. 1, pp. 57–70, Feb. 2004.

[46] J. Kolstad, C. Blevins, J. M. Dunn, and A. Weisshaar, "A new modeling methodology for passive components based on black-box augmentation combined with equivalent circuit perturbation," in *IEEE Proc. of 10th Topical Meeting of Electrical Performance of Electronic Packaging*, pp. 259–262, Oct. 2004.

[47] J. Kolstad, C. Blevins, J. M. Dunn, and A. Weisshaar, "A new circuit augmentation method for modeling of interconnects and passive components," *IEEE Trans. Advanced Packaging*, vol. 29, no. 1, pp. 67–77, Feb. 2006.

[48] D. L. Harame, K. M. Newton, R. Singh, S. L. Sweeney, S. E. Strang, J. B. Johnson, S. M. Parker, C. E. Dickey, M. Erturk, G. J. Schulberg, D. L. Jordan, D. C. Sheridan, M. P. Keene, J. Boquet, R. A. Groves, M. Kumar, D. A. H. Jr, and B. S. Meyerson, "Design automation methodology and rf/analog modeling for rf CMOS and SiGe BiCMOS technologies," *IBM Journal of Researhc and Development*, vol. 47, pp. 139–175, May 2003.

[49] J. P. Spoto, W. T. Coston, and C. P. Hernandez, "Statistical integrated circuit design and characterization," *IEEE Trans. Computer-Aided Design*, vol. 10, no. 5, pp. 90–103, Oct. 1986.

[50] S. R. Nassif, "A methodology for worst-case analysis of integrated circuits," *IEEE Trans. Computer-Aided Design*, vol. 5, no. 1, pp. 104–113, Jan. 1986.

[51] S. G. Duvall, "Statistical circuit modeling and optimization," in *IEEE Proc. of International Workshop on Statistical Metrology*, pp. 56–63, June 2000.

[52] K. K. Parhi and R. S. Berkowitz, "On optimizing importance sampling simulations," *IEEE Trans. Circuits and Systems*, vol. 34, no. 12, pp. 1558–1563, Dec. 1987.

[53] M. Keramat and R. Kielbasa, "A study of stratified sampling in variance reduction techniques for parametric yield estimation," in *IEEE Proc. of International Symposium on Circuits and Systems*, pp. 1652–1655, June 1997.

[54] N. J. Elias, "Acceptance sampling: An efficient, accurate method for estimating and optimizing parametric yield," *IEEE Journal of Solid State Circuits*, vol. 29, no. 3, pp. 323–327, Mar. 1994.

[55] J. F. Swidzinski, M. Keramat, and K. Chang, "A novel approach to efficient yield estmation for microwave integrated circuits," in *IEEE Proc. of 42nd Midwest Symposium on Circuits and Systems*, pp. 367–370, Aug. 1999.

[56] E. Matoglu, *Statistical design, analysis and diagnosis of digital systems and embedded RF circuits*. PhD thesis, Georgia Institute of Technology, 2003.

[57] T. B. Barker, *Quality by experiemental design*. New York: Marcel Dekker, 1994.

[58] J. Chen and M. A. Styblinski, "A systematic approach of statistical modeling and its application to CMOS circuits," in *IEEE Proc. of International Symposium on Circuits and Systems*, pp. 1805–1808, May 1993.

[59] J. P. C. Kleijnen, "Sensitivity analysis and optimization in simulation: design of experiments and case studies," in *IEEE Proc. of Winter Simulation Conference 1995*, pp. 133–140, 1995.

[60] D. S. Gibson, R. Poddar, G. S. May, and M. Brooke, "Statistically based parametric yield prediction for integrated circuits," *IEEE Trans. Semiconductor Manufacturing*, vol. 10, no. 4, pp. 445–458, Nov. 1987.

[61] H. L. Malek and A. Hassan, "The ellipsoidal technique for design centering and region approximation," *IEEE Trans. Computer-Aided Design*, vol. 10, no. 8, pp. 1006–1014, Aug. 1991.

[62] J. M. Wojciechowski and J. Vlach, "Ellipsoidal method for design centering and yield estimation," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 12, no. 10, pp. 1570–1578, Oct. 1993.

[63] S. Sapatnekar, P. M. Vaidya, and S. M. Kang, "Convexity-based algorithms for design centering," *IEEE Trans. Computer-Aided Design*, vol. 13, no. 12, pp. 1536–1549, Dec. 1994.

[64] P. M. Vaidya, "A new algorithm for minimizing convex functions over convex sets," in *IEEE Proc. of Fundamentals of Computer Science*, pp. 332–337, 1989.

[65] S. W. Director and G. D. Hachtel, "The simplicial approximation approach to design centering," *IEEE Trans. Circuits and Systems*, vol. 17, no. 3, pp. 159–165, 1977.

[66] K. K. Low and S. W. Director, "A new methodology for the design centering of IC fabrication process," *IEEE Trans. Computer-Aided Design*, vol. 10, no. 7, pp. 895–903, July 1991.

[67] R. Spence and R. S. Soin, *Response Surface Methodology : Process and Product Optimization Using Designed Experiments*. New York: Wiley, 1995.

[68] A. J. Strojwas, "Design for manufacturability and yield," in *IEEE Proc. of Design Automation Conference*, pp. 454–459, June 1989.

[69] D. E. Hocevar, M. R. Lightner, and T. N. Trick, "An extrapolated yield approximation technique for use in yield maximization," *IEEE Trans. Computer-Aided Design*, vol. 3, no. 1, pp. 279–287, Feb. 1982.

[70] E. Wehrhahn and R. Spence, "The performance of some design centering methods," in *IEEE Proc. of International Symposium on Circuits and Systems*, pp. 1421–1438, May 1984.

[71] K. Singhal, "Statistical design centering and tolerancing using parametric sampling," *IEEE Trans. Circuits and Systems*, vol. 28, no. 7, pp. 692–702, July 1981.

[72] K. Choi and D. Allstot, "Post-optimization design centering for RF integrated circuits," in *IEEE Proc of International Symposium on Circuits and Systems*, pp. 956–959, May 2004.

[73] S. Dalmia, A. Bavisi, S. Mukherjee, V. Govind, V. Sundaram, M. Swaminathan, and G. White, "A multiple frequency signal generator for 802.11a/b/g VoWLAN type applications using organic packaging technology," in *IEEE Proc. of Electronic Components and Technology Conference*, pp. 1664–1670, June 2004.

[74] S. Dalmia, V. Sundaram, G. White, and M. Swaminathan, "Liquid crystalline polymer based RF/wireless components for multiband applications," in *IEEE Proc. of Electronic Components and Technology Conference*, pp. 1866–1873, June 2004.

[75] B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by vector fitting," *IEEE Trans. Power Delivery Networks*, vol. 14, no. 3, pp. 1052–1061, July 1999.

[76] http://www.energy.sintef.no/produkt/VECTFIT/index.asp, Feb. 2007.

[77] R. A. Rohrer, "Circuit partitioning simplified," *IEEE Trans. Circuits and Systems*, vol. 35, no. 1, pp. 2–5.

[78] J. Vlach and K. Singhal, *Computer methods for circuit analysis and design*. New York: Van Nostrand Reinhold, 1983.

[79] J. W. Bandler, R. M. Biernacki, S. H. Chen, and Y. F. Huang, "Design optimization of interdigital filters using aggressive space mapping," *IEEE Trans. Microwave Theory and Techniques*, vol. 45, no. 5, pp. 761–769, May 1997.

[80] S. Haykin, *Neural networks - A comprehensive foundation*. New York: Prentice Hall, 1998.

[81] S. W. Director, "Optimization of parametric yield: A tutorial," in *IEEE Proc. of Custom Integrated Circuits Conference*, pp. 3.1.1–3.1.8, 1992.

[82] http://www.rogerscorporation.com/mwu/pdf/ULTRALAM3000DS.pdf, Mar. 2004.

[83] R. L. Mason, R. F. Gunst, and J. L. Hess, *Statistical design and analysis of experiments: with applications to engineering and science*. New York: Wiley Eastern Limited, 1989.

[84] S. Suresh, *Failure of materials*. United Kingdom: Cambridge University Press, 2001.

[85] J. Strydom, "Investigation of thermally induced failure mechanisms in integrated spiral planar power passives," in *IEEE Proc. of Electronic Components and Technology Conference*, pp. 1481–1486, June 2000.

[86] M. Damani, "Physics-based reliability assessment of embedded passives," in *IEEE Proc. of Electronic Components and Technology Conference*, pp. 2027–2031, June 2004.

[87] G. R. Cooper and C. D. McGillem, *Probabilistic methods of signal and system analysis*. New York: Holt, 1971.

[88] http://www.cadence.com/products/dfm/tech_info.aspx, Mar. 2007.