DESIGN OF HIGH SPEED PACKAGES AND BOARDS USING EMBEDDED DECOUPLING CAPACITORS

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DESIGN OF HIGH SPEED PACKAGES AND BOARDS USING EMBEDDED DECOUPLING CAPACITORS

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SUMMARY

Miniaturization of electronic products due to the current trend in the electronics industry has led to the integration of components within the chip and package. Traditionally, individual decoupling capacitors placed on the surface of the board or the package have been used to decouple active switching circuits. However, with an increase in the clock rates and its harmonics with technology nodes, decoupling has to be provided in the GHz range. Discrete decoupling capacitors are no longer effective in this region because of the increased inductive effects of the current paths of the capacitors, which limits its effectiveness in the tens of MHz range.

The use of embedded individual thick film capacitors within the package is a feasible solution for decoupling core logic above 100 MHz. They overcome the limitations of SMDs (Surface Mount Discretes), primarily in decoupling active circuits in the mid-frequency band. Inclusion of embedded planar capacitors in the board stack up have shown improvements in the overall impedance profile and have shown to exhibit better noise performance. The main contributor to the superior performance is the reduced inductive effects of the power-ground planes because of the thinner dielectrics of the embedded capacitor. The modeling, measurement and characterization of embedded decoupling capacitors in the design of PDNs (Power Distribution Networks) has been investigated in this thesis.

CHAPTER I

INTRODUCTION

Embedded passives are gaining in importance due to the reduction in size of consumer electronic products [1]. Integration of these passives within the package increases the real estate for active components therefore improving the functionality of the system. Among the passives, capacitors pose the biggest challenge for integration in packages because of the large capacitance required for decoupling active circuits.

The scaling of Complimentary metal oxide semiconductors (CMOS) transistors through the technology nodes has resulted in an increase in the number of transistors per chip. The frequency of operation of processors has also increased through the technology nodes. Based on the numbers from the International Technology Roadmap for Semiconductors (ITRS) [2], these trends are expected to continue as we move towards higher technology nodes. With the increase in clock speeds and decrease in the core voltage of the processors, the design of PDNs has increased in complexity for CMOS technology. The proper design of power delivery requires an understanding of the different components that constitute the power distribution networks. Therefore, the next part of this chapter investigates the different components that effect the system performance. The different components highlighted are as follows:

1) Power Distribution Networks.

2) Simultaneous switching noise.

3) Decoupling capacitors.

4) Effect of power planes on impedance profiles.

5) The different decoupling methodologies used in today's systems.

6) The limitations of the present day decoupling solutions and the use of embedded

thin/thick film discrete capacitors in overcoming these limitations.

1.1 Power Distribution Networks

A constant supply of voltage and current is required for the active circuits to operate efficiently. This aspect of electrical design that deals with the delivery of power to the switching circuits is termed as power distribution. The design of the PDN is therefore critical for the proper functionality of a system. The PDN for a high speed digital system consists of power ground planes in the board and the package, a switching regulator, and decoupling capacitors. The PDN supplies the drivers (switching circuits) and receivers, with voltage and current to function. A major challenge in the design of such a network is to maintain a low impedance for the PDN over a determined bandwidth [3]. For superior performance, this target impedance must be met at all frequencies where current transients exists. These transients could exist because of operations that involve data transfer to and from the hard disk, DRAM, or on chip processes. The frequency band to be decoupled extends from DC to multiples of the chip operating frequency depending on the processor function [3]. The fast switching speeds of circuits result in sudden bursts of current which couples with the inductance of the power ground planes generating noise, which is commonly termed as simultaneous switching noise (SSN). It has been observed that the power supply noise induced by a large number of simultaneously switching circuits in the PDN can limit their performance. A desirable plot of the PDN, looking from the chip into the processor is shown in Fig. 1.

The PDN has a capacitive behavior at low frequencies and shows inductive behavior as we move towards the higher frequency range. Noise in the PDN is generated by the current demands of the loads in CMOS circuits i.e. when the drivers in the active circuits transition from the high to low or low to high state simultaneously, large transient currents need to be supplied by the PDN. A small amount of inductance

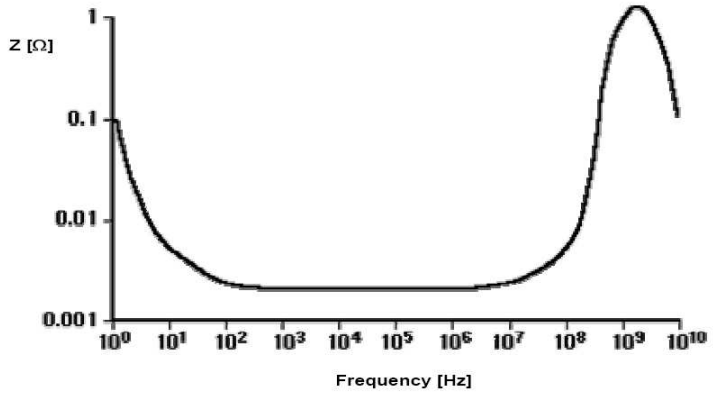


Figure 1: Preferred impedance profile of a power distribution network.

in the PDN will generate noise voltage in the presence of these current transients. Therefore, the inductance of the PDN must be reduced to enable easy flow of charge to the required active circuits to mitigate the noise. The target impedance of the PDN is decided based on the core voltage and average current drawn by the processor. The target impedance is given as [4].

$$Z = \frac{V_{core} \times 0.05}{I \times 0.5} \tag{1}$$

Where V_{core} is the core voltage of the active device and $I \times 0.5$ is the assumed average current drawn by the device. The noise voltage that can be tolerated is assumed to be 5% of the core voltage V_{core}. Also 50% of the maximum current is assumed to flow in the rise and fall time of the clock edge respectively to give a 100% maximum current over the whole clock period [4]. The power dissipated by a processor, the core voltage, and average current are related by the following equation

$$P = V_{core} I \tag{2}$$

Table 1: Variation of cost performance processor parameters through technology nodes

Year	Feature size(nm)	Power (W)	V_{core} (V)	I (A)	Target Impedance (mΩ)
2004	90	84	1.2	70	1.7
2007	65	103.6	0.9	115.11	0.781
2010	45	119	0.6	198.33	0.302

The estimated power dissipated for the 65 nm node cost performance processor from [2] is 103.6 W and V_{core} is 0.9 V. Using equation 2, the maximum current I drawn by the processor is 115.1 A. The target impedance for this processor is calculated by substituting the value of V_{core} and I in equation 1). Table 1 lists the different parameters for cost performance processors in the 90 nm, 65 nm, and 45 nm nodes as listed in [2]. Power(W) is the power that can be sustained by the package in that particular technology node.

The ITRS 2006 update lists the core voltage for the 65nm node as 1.1 V, which translates into a target impedance of 1.1 $m\Omega$ for that particular node. The analysis in this thesis however accounts for the numbers given in table 1. From the table it is evident that the target impedance is decreasing with an increase in the technology nodes. This decrease in the target impedance puts stringent requirements on the design of a PDN and the various decoupling components.

1.2 Simultaneous Switching Noise

Simultaneous switching noise refers to a voltage spike generated in a digital system due to rapid changes in the magnitude of the current caused by the switching of many circuits in the system at the same time. The term "delta I" noise is also associated with this phenomenon because of its direct dependence on the rate of current or called "ground bounce" since the voltage spike corresponds to an effective change of power supply voltage and therefore can be seen as a shift in the internal ground reference voltage level. In a system, the noise generated by the simultaneous switching of N drivers is given by [1].

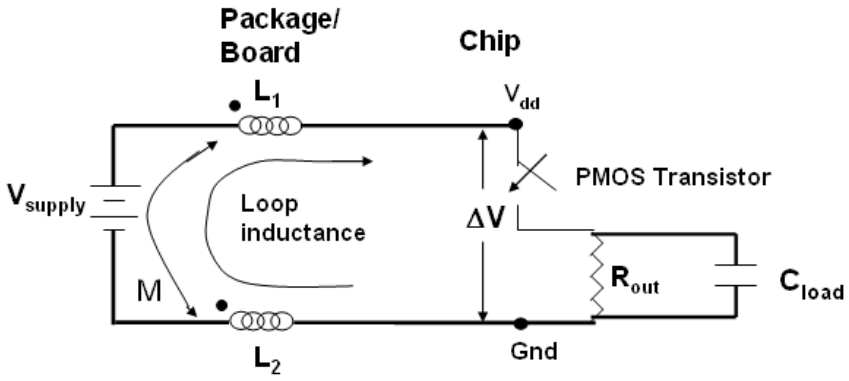


Figure 2: Loop inductance associated with SSN.

$$\Delta V = N L_{eff} \frac{\Delta i}{\Delta t} \tag{3}$$

Where L_{eff} is the effective inductance of the power distribution network which accounts for all the parasitic inductances along the current path in the package. The peak rate of change of current is given by $\frac{\Delta i}{\Delta t}$, where Δi is the current required by each driver during the switching event and Δt is the rise or fall time of the signal. An improvement in the frequency of operation of the processors would increase the rate at which the circuits are switching. It has been recognized that the power supply noise induced by large numbers of simultaneous switching circuits in the power distribution network can limit their performance [1],[5],[6],[7],[8],[9]. Therefore, the switching currents may change by a large amount in small interval of time, increasing the magnitude of the switching noise. Methods to decrease the magnitude of the SSN would be to either reduce the switching speed of the circuits or reduce the effective inductance of the PDN. Decreasing the frequency of the active circuits would degrade performance, therefore the reduction of the inductance of the package is a method of reducing SSN. The contributing inductance to the SSN is because of the current flow from the current sources to the active circuits and back as shown in Fig. 2.

It has been previously shown in [9], that the use of a ball grid array (BGA) package

reduces the inductance as compared to a lead frame package. The parasitics in the BGA package are reduced because of the smaller inductances associated with the vertical current path consisting of vias and solder bumps.

The conducting structures, which have the least amount of resistance and inductance should be used in the power distribution network in the package. A performance comparison of meshed and solid planes was carried out in [10]. The performance parameters were coupled noise, SSN and shielding effectiveness. A five fold increase in the inductance was observed in the meshed plane as compared to solid planes when the plane to plane separation was decreased. Therefore, the most effective way of reducing the inductance of the PDN in the package would be to use solid power/ground planes in the BGA package.

An active switching circuit draws charge from the PDN to energize a load capacitor. This charge is supplied as current from the power supply. A voltage drop is produced when this current flows through the package inductance as mentioned earlier. Also, from equation 3 it can be clearly seen that the magnitude of the SSN depends on the amount of inductance. The presence of capacitors in the PDN provide charge to the load capacitors as well as reduce the loop inductance. Fig. 3 shows a decoupling capacitor of capacitance C_{decap} placed in the PDN. Assume that the capacitor is initially charged to the supply voltage V_{dd}. When the transistor with on resistance R_{on} and load capacitance C switches, charge of amount $Q = CV_{dd}$ is required to charge the load capacitor. This charge is provided by the decoupling capacitor instead of the power supply in the form of a current Δi in time Δt, where Δt is the switching time of the transistor. This is assuming that the charge stored in the decoupling capacitor is greater than the charge required by the load capacitor. From the Fig. 3, it can be clearly seen that the current loop inductance is much less than if the current were supplied by the voltage supply. Therefore, the decoupling capacitors acts as charge reservoirs by charging to the supply voltage when the active circuits

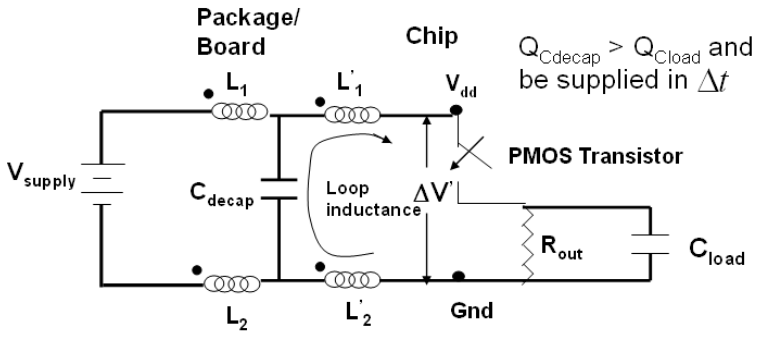


Figure 3: The current path in the presence of a decoupling capacitor.

are idle and supply current when there is a demand. The function of decoupling capacitors as charge reservoirs reduces the loop inductance and the magnitude of the SSN. The next section will investigate the different decoupling components used in PDNs.

1.3 Decoupling Components

This section will briefly describe the different decoupling components used in today's systems and will highlight their advantages and disadvantages. The primary use of the decoupling components is to suppress SSN by placing them on the board, package, and chip. Power delivery decoupling in today's systems is primarily achieved by using voltage regulator modules (VRMs) and surface mount discrete capacitors (SMDs). To support the current needs of fast switching circuits, the decoupling components must provide charge to the circuits at each clock cycle.

The VRM is a DC-DC converter, it senses the voltage near the load and adjusts the output current to regulate the load voltage. VRMs are effective till the lower kilohertz region after which they become highly inductive in their behavior. Surface mount capacitors provide decoupling from the kilohertz region till several hundred megahertz. SMDs start becoming ineffective above this frequency because of the increased effect of its lead inductance and the loop inductance associated with

Figure 4: Equivalent model of a capacitor.

the charge flow from the capacitors to the switching circuits and back again to the capacitors.

Ideally decoupling capacitors should act as a short circuit between the power and ground plane. However, the parasitic inductance of the leads and mounting pads of the decoupling capacitors strongly limit their decoupling capabilities. Decoupling capacitors can be represented by an equivalent R,L, and C circuit as shown in Fig. 4. The parasitic parameters R,L, and C are the equivalent series resistance (ESR),the equivalent series inductance (ESL), and the capacitance of the structure respectively. The decoupling capacitor acts like a short only at frequencies close to its resonant frequency. The impedance of a decoupling capacitor is identical to a RLC circuit and is given by the following equation:

$$Z_{real_decap} = R + j\omega L + \frac{1}{j\omega C} \tag{4}$$

Where $\omega = 2\pi f$ is the angular frequency. The resonant frequency of a decoupling capacitor is a function of its capacitance and inductance and is given by equation5

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{5}$$

At the resonant frequency, the reactive impedances cancel and the effective impedance of the decoupling capacitor is the ESR of the capacitor. In practical applications, the decoupling capacitors are spread across the whole system as the switching time for

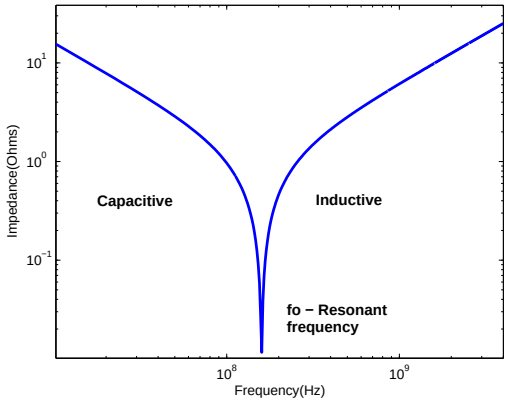


Figure 5: Frequency response of a capacitor.

circuits may be different depending on their function. The loop inductance of these capacitors vary based on their position. Capacitors placed closer to the active circuits will have lower loop inductances associated with them as compared to capacitors placed farther away from the active circuits. This translates to a variation in the resonant frequency of the capacitors as given by equation 5. Above the resonant frequency the capacitor shows an inductive behavior and the performance of the capacitor as a charge provider degrades. The frequency response of a decoupling capacitor is shown in Fig. 5.

Due to this kind of characteristic of decoupling capacitors, different kinds of decoupling capacitors are used over a wide frequency range depending on the board and package structures. Based on the resonant frequency, the decoupling capacitors can be characterized as low frequency, mid frequency and high frequency capacitors. The low and mid-frequency capacitors are placed on the package and the board while the high frequency capacitors are buried in the chip.

1.4 Characteristics of Power Distribution Planes

The bandwidth of the signal transients move to the giga-hertz range, the required target impedance would reach the sub milli-ohm range [11]. If not designed properly, the power/ground planes in the power distribution networks exhibit resonances

in the frequency domain [12], and the resonances at certain frequencies may be higher than the target impedance. In conventional designs decoupling capacitors are placed in the PDN to suppress the resonances at the concerned frequencies. In addition, using different materials and geometries of power-ground planes provide good suppression of plane resonances in the PDN. For instance, an increase in the loss of a dielectric material and a decrease in the dielectric thickness helps to reduce the impedance and resonances [13],[14]. To examine the effects of power-ground planes in the PDN, this section investigates the effect of dielectric loss, the dielectric constant, and the dielectric thickness on the PDN.

1.4.1 Effect of Dielectric Loss

For low loss signal transmission , PCB materials with low dielectric loss have been used; as a result, plane resonances are not suppressed sufficiently [13]. If the dielectric material is to be used just between the power-ground plane then high loss dielectrics would be preferred. Fig. 6 captures the comparison of impedances as a variation of the loss tangent ($tan\delta$) of the dielectric. The impedance magnitude at the resonant frequency decreases as the loss tangent of the dielectric increases. Since the plane capacitance and inductance determine the cavity resonance, this parameter does not change. At a certain value of $tan\delta$, the plane resonances are almost suppressed. The effect of the loss tangent on the impedance response of a power plane structure can be explained by the dependance of the shunt conductance of a power plane on the loss tangent. The shunt conductance is given by:

$$G = \omega C tan\delta \tag{6}$$

The shunt conductance acts like a damping resistor between the power and ground plane and therefore an increase in the loss tangent value increases the value of this damping resistor reducing the peaks of the impedance profile.

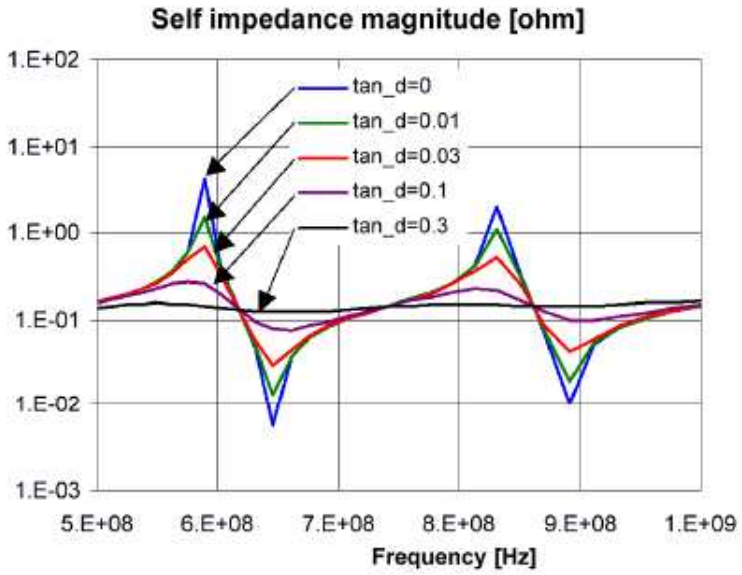


Figure 6: Effect of dielectric loss on the plane impedance.

1.4.2 Effect of Dielectric Constant

Fig. 7, shows the effect of dielectric constant on the plane impedances and resonances for dielectric constant (ϵ_r) = 4, 8, 16, 32 and 64 [14]. An increase in the plane capacitance due to the increase in the dielectric constant reduces the low-frequency impedance and the null and peak resonant frequencies shift to the lower frequencies. This is because the velocity of the plane waves that propagate between the power and ground plane varies inversely with $\sqrt{\epsilon_r}$. The increase in the delay of the plane waves result in the downshift of the resonant frequency proportional to $\sqrt{\epsilon_r}$. The plane impedances in the higher frequency range do not change much as it is determined by the inductance of the power/ground plane, which is fixed.

1.4.3 Effect of Dielectric Thickness

Thin dielectrics between power/ground planes offer advantages in the low as well as high frequency range. For the analysis in this section assume a unit cell of the power plane of length and width w. The capacitance of the unit cell of the power plane is

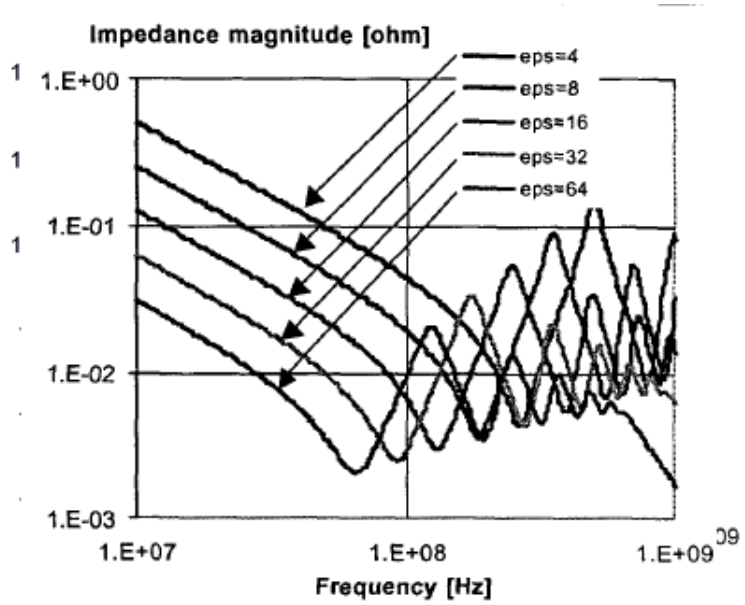


Figure 7: Effect of dielectric constant on the plane impedance.

given by equation 7

$$C = \frac{\epsilon_o \epsilon_r w^2}{d} \tag{7}$$

Where ϵ_o, ϵ_r are the permittivity of free space and relative dielectric constant of the material. A is the area of the power plane and d is the separation between the power and ground plane. The inductance of the unit cell of the power ground plane is given by the equation

$$L = \mu_o d \tag{8}$$

μ_o is the permeability of free space. From, the above equations it is evident that the thinner dielectrics increase the capacitance of the planes and reduce the plane inductance. Thinner dielectrics reduce the impedance over the frequency range as well. This can be explained by the relationship of the impedance of the power-ground plane with the capacitance and the inductance, given by equation 9:

$$Z = sqrt(\frac{L}{C}) \tag{9}$$

An increase in the capacitance and decrease in the inductance reduces the impedance of the power planes. The velocity of a wave between the power-ground plane is given

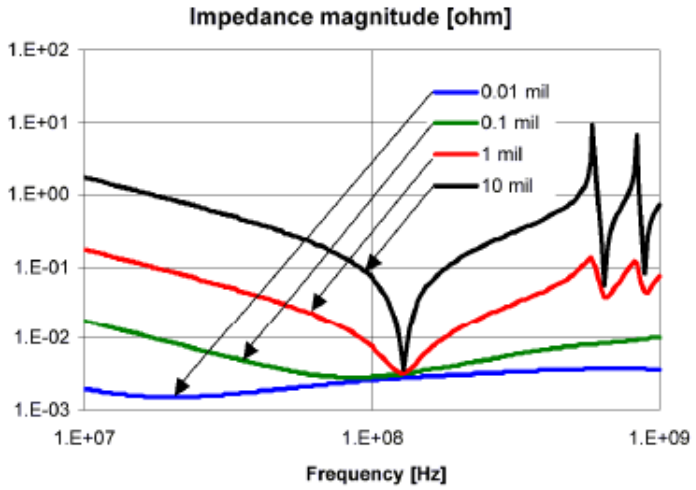


Figure 8: Effect of dielectric thickness on the plane impedance.

by equation 10

$$v = \frac{1}{sqrt(LC)} \tag{10}$$

From the above equation it can be inferred that the peak and null resonant frequencies do not change since the velocity of the wave remains constant since it is not a function of dielectric thickness. The effect of dielectric thickness on the plane impedance is shown in Fig. 8 [13].

1.5 Decoupling Methodologies used in today's systems

The different decoupling methodologies used in today's PDNs will be highlighted in this section. The methodologies are listed below:

a)"Multi-pole" (MP) [3]

b)"Big-V" [15]

c)"Distributed Matched Bypassing" (DMB) [16]

d)"Extended Adaptive Voltage Positioning" (EAVP)

In terms of the impedance profile, the first three methodologies are very similar

to each other. There is no clear boundary between these design approaches and one method can be transformed into another by varying certain parameters. The DMB methodology, calls for a flat impedance profile from DC to a certain corner frequency after which the impedance can increase linearly based on the inductance value. In this methodology, elements with $Q < 1$ are used. The $Q < 1$ condition creates a shallow flat bottom on the impedance curve of each capacitor bank. Capacitor banks that are adjacent on the frequency axis can be represented by a lower frequency R-L and higher frequency R-C elements in parallel. This network approximation is valid only in the vicinity of the capacitor banks as it neglects the capacitance of the lower bank and the inductance of the higher bank. As long as the serial losses between the elements of the DMB network are not significant, the PDN can be represented by a number of such cells in parallel. In the MP design methodology, different values of capacitors are chosen to cover the frequency band over which decoupling has to be provided. The impedance profile of the resultant design of the PDN has multiple peaks and the choice of the capacitors to decouple higher frequency bands depends on the inductance of the capacitor used to decouple the lower frequency region. In the "Big-V" method, a number of capacitors of the same type and value are used to create a "V" in the impedance profile response. The value of the "V" being far below the target impedance. The comparison of the resultant impedance profile of the three methodologies is shown in Fig. 9 [17].

The EAVP method is based on the theory of adaptive voltage positioning (AVP), which is commonly used in voltage regulator module (VRM) design and operation [18]. The (AVP) design will be briefly discussed in this part of the section. The circuit used in AVP is shown in Fig. 10 [19]. The voltage is set to $V_{CC} + T_{OL}$ when no current is consumed as shown in Fig. 11 [19]. When all the current is consumed, the voltage is then $V_{CC} - T_{OL}$. Initially, all the I_{CC} current is supplied by the bulk capacitor, thereby setting the initial voltage drop to $I_{CCMAX} \times R_{BLK}$. In the steady

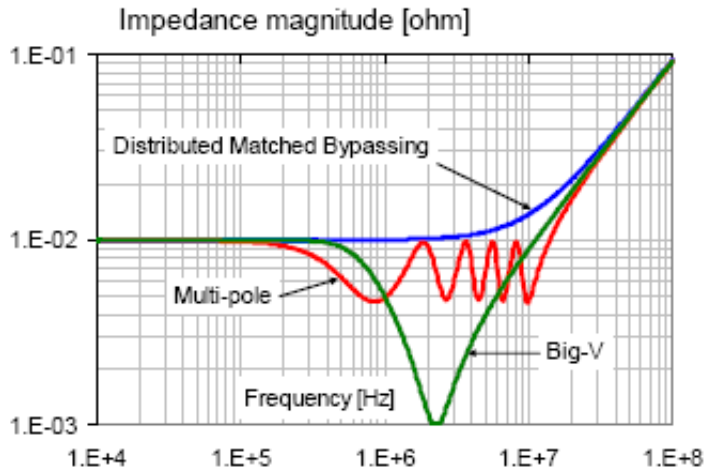


Figure 9: Impedance profile comparison of different methodologies.

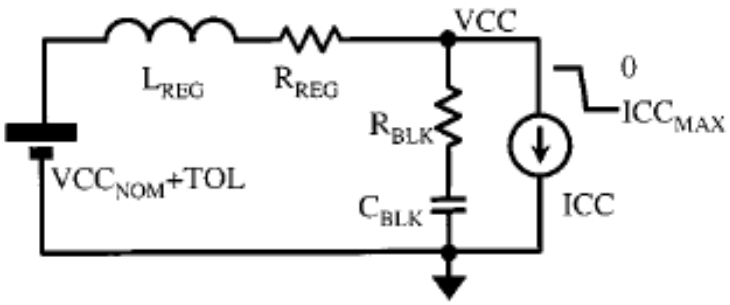


Figure 10: Conceptual circuit diagram of AVP.

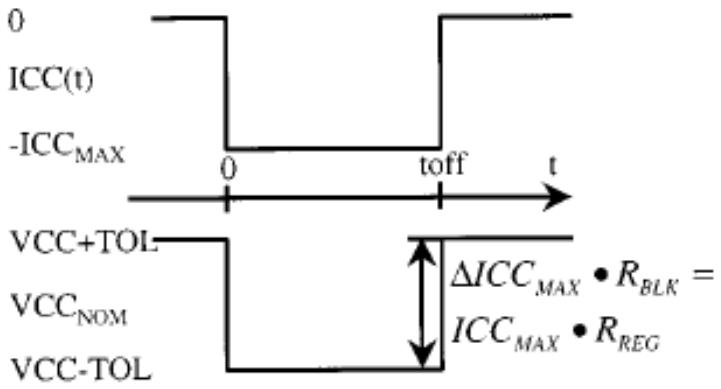


Figure 11: Adaptive voltage positioning waves.

state the voltage drop is $I_{CCMAX} \times R_{REG}$. For identical voltage droops at $t = 0$ and in the steady state, $R_{BLK} = R_{REG}$ should be enforced. Also, to achieve zero overshoot and undershoot, the inductive and capacitive time constants has to be met.

$$R_{BLK}.C_{BLK} = \frac{L_{REG}}{R_{REG}} \tag{11}$$

To meet the tolerance window, R_{BLK} has to be given by:

$$R_{BLK} = \frac{Vcc \times 2 \times T_{OL}}{I_{CCMAX}} \tag{12}$$

Since the effectiveness of the bulk capacitors at higher frequencies is limited by its parasitic inductance L_{BLK}, the EAVP method was introduced. EAVP extends the method that was used for optimized AVP design of bulk capacitors to the successive designs of the mid-frequency and die capacitance parameters. The basic rules used in this methodology are as follows:[19]

Rule 1) Select the equivalent series resistance of the decoupling stage N to be equal to the effective series R of the decoupling stage $N - 1$.

Rule 2) Select the RC time constant of the decoupling stage N to match the L/R time constant of stage $N - 1$ or select the $Z(f)$ 3DB point of decoupling stage N to the $Z(f)$ +3DB point of stage $N - 1$.

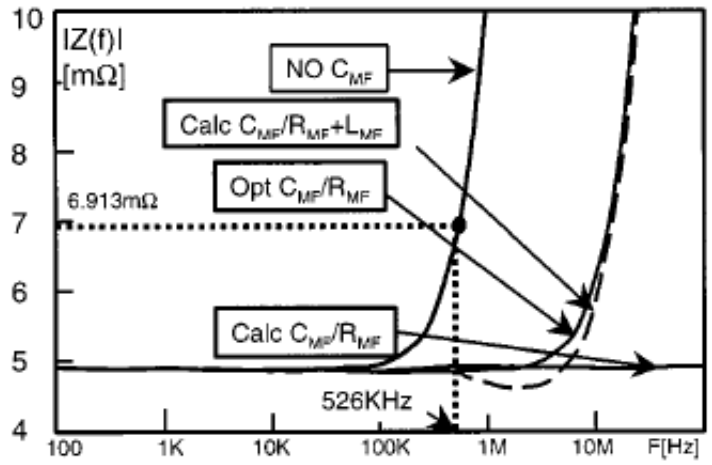


Figure 12: Optimization of the impedance profile.

The 3DB frequency point is where the impedance increases by a factor of $\sqrt{2}$. For example. in Fig. 12 [19] the +3DB frequency for an impedance of $4.88m\Omega$ turns out to be 526 KHz. Therefore, the capacitance required for the next stage can be calculated as follows:

$$C_{MF} = \frac{1}{2 \times \pi \times 4.89 \times 10^{-3} \times 526 \times 10^{3}} = 61.91uF \tag{13}$$

A combination of capacitors can be used to obtain the required capacitance and resistance values for the next stage. The conceptual EAVP principle is illustrated in Fig. 13 [19].

1.6 Limitations of present day decoupling methodologies and proposed solutions.

The proper design of a PDN is critical to the functionality of a digital system. In this section the different core decoupling components used in today's systems will be investigated. The advantages and disadvantages of the different components will be highlighted.

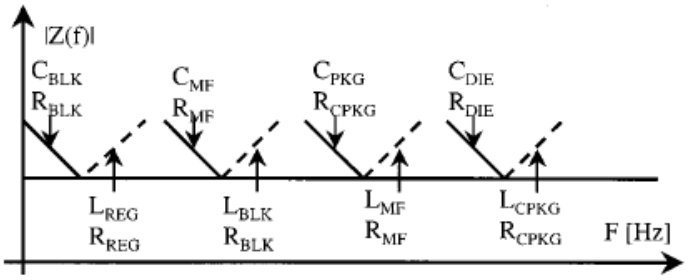


Figure 13: Conceptual diagram of EAVP.

With the increase in power consumption and current demands of processors, the target impedance that the PDN must meet has been decreasing through processor product generations. Core decoupling in today's systems is primarily achieved by using discrete surface mount decoupling capacitors placed on the board, on the package, or in the package. Simulations were carried out to highlight the limitations of such components in decoupling cost performance processors. The schematic of the set up is shown in Fig. 14.

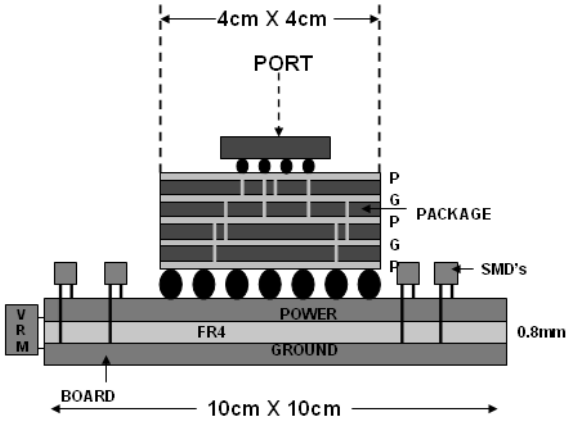


Figure 14: Decoupling schemes in today's systems.

The set up includes a 10 cm × 10 cm board with a dielectric thickness of 0.8 mm and metal thickness of 30 um. A 4 cm × 4 cm package and a 11.8 mm × 11.8 mm processor mounted on the package were also included in the simulations. The input port in the simulation is the processor looking into the package and the board. The PDN

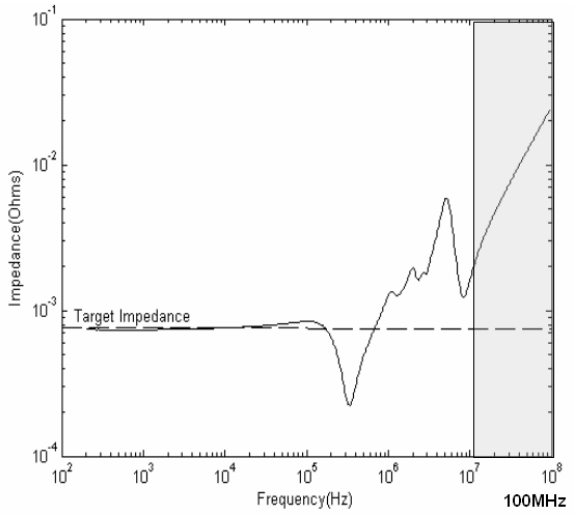


Figure 15: Decoupling limitations of SMDs

was designed to meet the target impedance of 0.78 mΩ for the 2007 cost performance processor. The multi-pole method was used to design the PDN with different valued capacitors. The lower inductance capacitors were placed on the package closer to the active device to decouple the higher frequency range. This was done to reduce the effect of the spreading inductance of the planes on the capacitor performance. Spreading inductance can be defined as the inductance per unit square of power planes [20]. As seen from Fig. 15, at frequencies close to 100 MHz it becomes increasingly difficult to meet the target impedance of 0.78 mΩ. This can be attributed to the increased effect of the loop inductance because of charge flow from the capacitors through the package and to the active circuits and the return current from the active circuits to the capacitors. In order to provide effective decoupling above 100 MHz, it would be required to reduce the effective inductance associated with the capacitors.

The reduced inductance required to target the frequency range above 100 MHz can be achieved in the following ways:

1) Embedding individual surface mount capacitors in the package or at the bottom of the package.

2) Use planar embedded capacitors between the power-ground planes of the package.

3) Use thin/thick film embedded discrete capacitors within the package.

4) Use on-chip capacitance to decouple the higher frequency bands.

The above core decoupling strategies were investigated to highlight their effectiveness in decoupling above 100 MHz.Traditionally, discrete decoupling capacitors placed on the surface of the board or the package have been used to decouple active switching circuits [3],[21],[22],[23]. However, with an increase in the clock rates and its harmonics with technology nodes [2], decoupling has to be provided in the GHz range. Discrete surface mount capacitors can be attached to the bottom of the package as shown in Fig. 16 [24] to reduce the effect of the inductance on the performance of the capacitors. The disadvantage of such an approach is that the real estate to include the capacitors

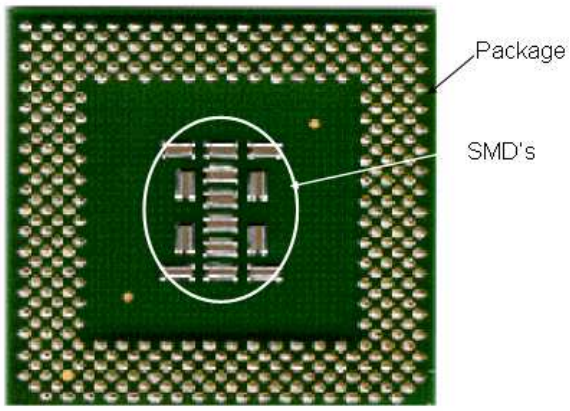


Figure 16: Decoupling limitations of SMDs

is limited. This would be an issue if the target impedance that is required to be met is in the sub-milli ohm range. The relationship between the target impedance and the number of capacitors is given in equation 64

$$Numberofcapacitors = \frac{Z_{target}}{ESR_{cap}} \tag{14}$$

Where Z_{target} is the target impedance that needs to be met and ESR_{cap} is the series resistance of an individual capacitor. The placement of the capacitors in the package is extremely critical, for the most optimized design it is required that the capacitors be placed directly under the die shadow of the processor as shown in the following

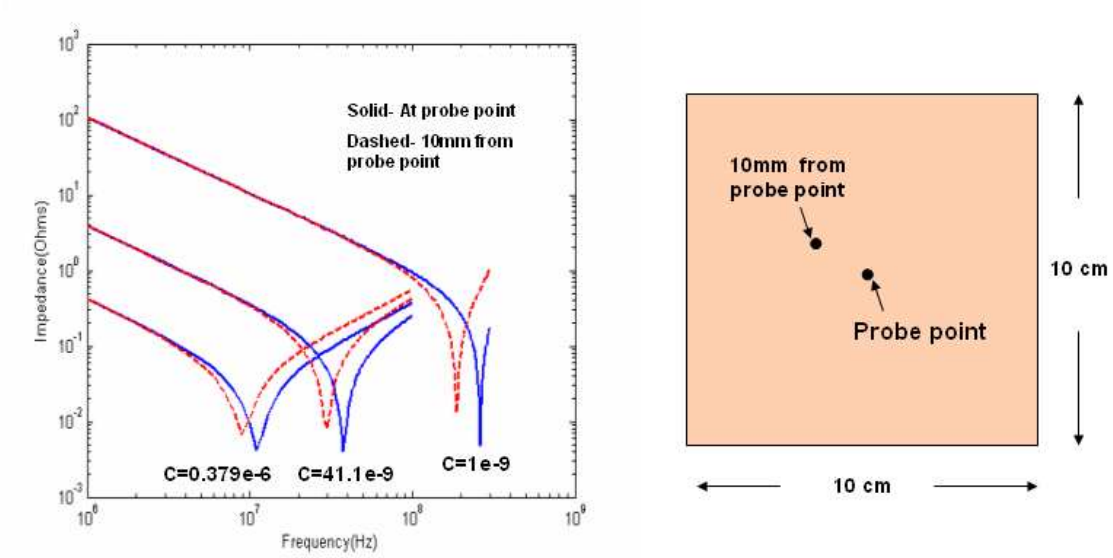


Figure 17: Sensitivity of capacitor performance with position.

analysis. Capacitors were placed on a 10 cm × 10 cm power plane. The capacitor performance is sensitive to position as shown in Fig. 17. The solid line is the performance of the capacitor at the probe location, while the dashed line is the capacitor performance placed 10 mm away from the probe point. The degradation of the frequency response of the capacitors with location is clearly evident and is because of the effect of the inductance and resistance of the power planes. Therefore, the desired frequency may not be targeted because of the plane parasitics. An important requirement of these capacitors is to be able to place them as close to the switching circuits as possible. In the case of discrete embedded capacitors the most important criteria would be to place them directly under the die shadow. Another option would be to use embedded planar capacitors in the PDN. This option has been investigated as shown in [25],[26],[27],[28],[29]. The planar capacitor is primarily a layer of thin dielectric between the power and ground plane in the board or the package. The performance of an embedded planar capacitor layer in a package was investigated. The embedded planar capacitor is connected to the active device with thru vias that extend from the

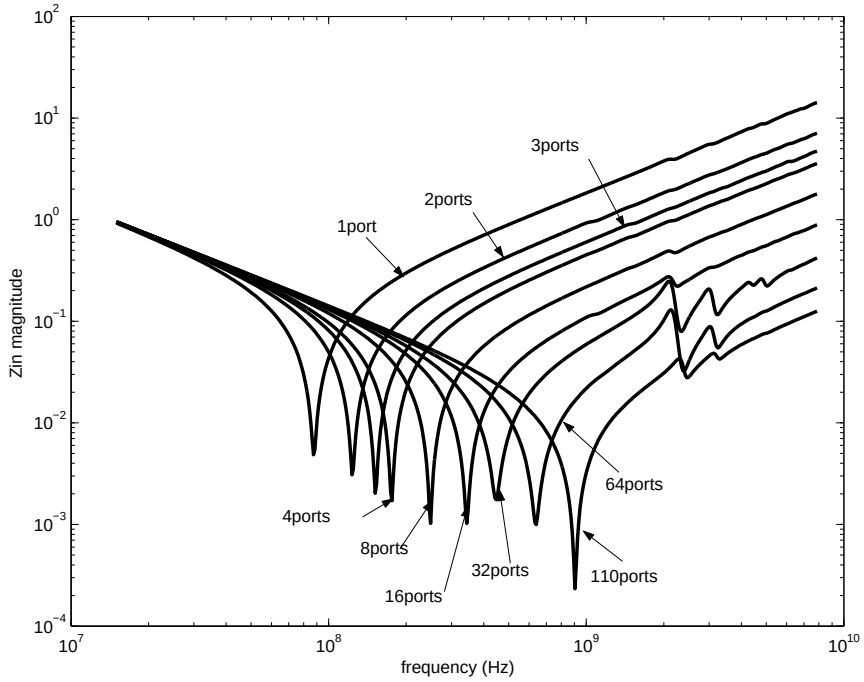


Figure 18: Embedded planar capacitor performance with different number of via pairs

embedded planar capacitor to power-ground bumps of the active device. The performance with different number of thru hole via connections was investigated. A thru via extends through the length of the package. For this particular case a thru hole via pair of length 600 um and spaced 200 um apart was modeled using Fast Henry [30] to extract its inductance. The inductance extracted by the program for a thru hole pair was 280 pH. The planar capacitor has dimensions of four cm by four cm and included a substrate which has a dielectric constant of 11 and thickness 14 um. The top and bottom metal layers have a thickness of 35 um each. The planar capacitor was modeled using the transmission matrix method (TMM) [31]. The details regarding the modeling of these capacitive structures will be given in greater detail in section 3.3. From Fig. 18, it is observed that increasing the number of thru hole via pairs decreases the total inductance of the structure. Lower inductance translates to a higher resonant frequency of the capacitor as seen by the performance of the planar capacitor. A disadvantages of the planar capacitor performance is the frequency

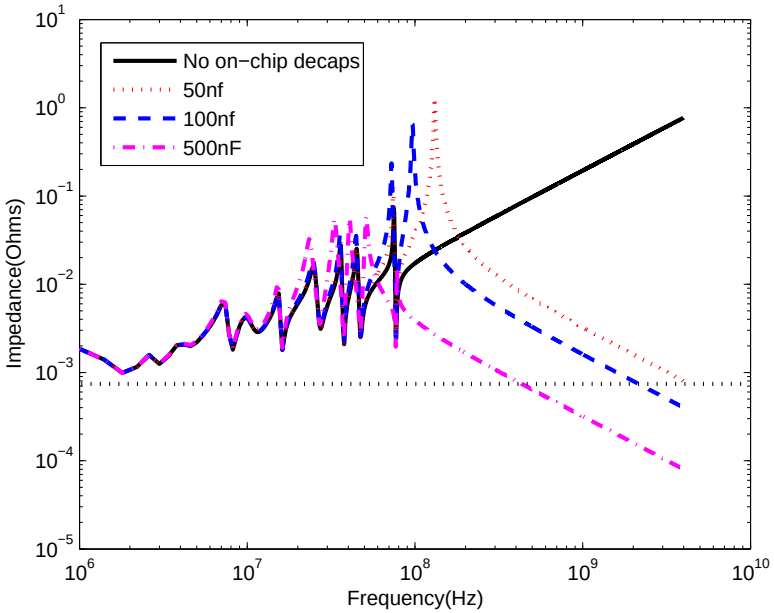


Figure 19: Impedance profile with varying amounts of on-chip capacitance.

band over which the target impedance is met since it is limited to a very small part of complete frequency band. For example, if the target impedance under consideration is 1 mΩ, the frequency band over which this impedance can be met with 110 via pairs on the capacitor is limited to less than 100 MHz as seen from Fig. 18. Also, from a processing stand point, the power and ground planes may get shorted with each other i.e. the pin hole effect is an issue with thin dielectric layers. An innovative method presented in [32] uses a capacitance interposer between the chip and the board to provide decoupling for the switching circuits. In this methodology discrete or custom capacitance is integrated into the interposer rather than on the board. All the pins are mapped in a 1 to 1 between the substrate and the board. This method adds 2-3 mm in height to the overall stack up.

Another option listed above is to use on-chip capacitance to decouple in the higher frequency range. Previous work has illustrated the effect of on-chip capacitance for decoupling switching circuits [33],[34],[35],[36]. The disadvantage with this approach is the low capacitance value associated with the on-chip decoupling component. This

renders them effective at frequencies beyond one to two GHz. The amount of on-chip capacitance can be increased, but this would compromise the amount of real estate available for including logic circuits.

To overcome the limitations of the SMDs, planar embedded capacitors, and on-chip capacitance the proposed solution is to use discrete thin/thick film capacitors that can be used within the package as shown in Fig. 28. These capacitors can be designed with variable sizes, have different capacitances, and therefore resonate at different frequencies. The proximity of these capacitors to the active devices reduces the loop inductance as compared to the SMDs and are effective in targeting frequencies above 100 MHz. Another advantage of using individual thick film capacitors is the high value of capacitance that can be obtained by using this technology.

SSN can be produced by improper return current path as shown in [4]. I/O decoupling is achieved by providing a low impedance path to the return current for the I/O signals. This can be achieved by using embedded planar capacitors in the board. The thin dielectrics increase the capacitance and reduce the inductance decreasing the overall impedance of the structure, therefore providing low impedance for the return current and reducing the noise produced. The details regarding the performance improvements will be explained in detail in chapter 5 of this thesis.

1.7 Proposed Research and Dissertation Outline

The objective of the proposed research is to highlight the performance benefits of using embedded thin/thick film capacitors in decoupling active and I/O circuits. The case for embedded capacitors is made for future packages and boards supporting multi-core processors. This includes investigating the limitations of SMDs in decoupling over 100 MHz to maintain target impedances in the order of milli-ohms. The design, modeling, and measurement of embedded capacitors is done in this thesis.

The design of an array of embedded package capacitors to decouple the mid-band frequency from 100 MHz to 2 GHz and the performance benefits of using this embedded capacitor array is highlighted in the time and frequency domain. This research also includes the use of embedded planar capacitors in boards to decouple I/O circuits.

The simultaneous switching of active circuits leads to generation of noise in the PDN that can propagate and degrade the performance of logic blocks in the vicinity. Therefore, the mitigation of this noise is critical for the proper functionality of a digital system. Based on the issues of noise generation and performance degradation in digital systems, the following research is proposed:

1) **Power dissipation of processors**: High power processors put stringent requirements on the design of PDNs, since higher power translates to a lower target impedance that must be met by the PDN. Therefore, an investigation of the different power dissipation components of processors and a methodology to improve overall performance of processors by reducing the power dissipation and increasing the off-chip bandwidth was done in this thesis. The work done regarding processor power dissipation is listed below:

a) The different components of power dissipation of a processor were investigated. This primarily included the active, static, and I/O power dissipation components.

b) The active power dissipation through the technology nodes was calculated by using an active power dissipation calculation tool SUSPENS [37] and the static power was calculated based on the numbers from ITRS. The numbers obtained from this analysis compared well with the existing numbers of processor power dissipation.

c) The trend of processor power dissipation through technology nodes predict that these numbers would far exceed the maximum amount of power that a package can sustain as per ITRS. Therefore, an analysis into the methodology of reducing power

dissipation while increasing the performance was done. Off-chip bandwidth was defined as performance parameter. This methodology involves the use of multi-core processors to achieve the required performance numbers while reducing the overall power dissipation. The packaging platform required to sustain such high off-chip bandwidth is investigated in the thesis.

2) **Individual Thin/Thick Film Embedded Package Capacitors**: The limitation of SMDs in decoupling active circuits is done with the aid of a PDN modeling tool. The analysis was done to investigate the performance of the SMDs to decouple a PDN with a target impedance in the order of milli-ohms and the advantages of using embedded package capacitors in such scenarios is highlighted. This work included the following:

a) The limitations of SMDs by modeling a PDN with SMD type decoupling capacitors to decouple a high-end microprocessor is shown. The limitations of embedded planar capacitors to meet similar decoupling requirements are also highlighted in this thesis. The different technologies that enable embedded package capacitors are highlighted.

b) The measurement of the embedded capacitors using a two port frequency domain measurement technique is done. The repeatability and robustness of this technique is highlighted by carrying out a series of similar measurements and comparing the results. The frequency dependent capacitance, inductance, and resistance is extracted over the measured frequency range.

c) The capacitive structures are modeled and the model to hardware correlation for the different structures are shown by compensating for the excess inductance of the probes.

d) Using the models developed for the capacitor structures, an array of embedded capacitors within the package was designed to decouple the mid-band frequency range

from 100 MHz to 2 GHz using different sized capacitors. Different arrays were designed with the capacitor technologies developed at the Packaging Research Center (PRC) and by DuPont technologies respectively. The performance investigation in the time and frequency domain were done for both arrays and a significant improvement was observed for both cases.

e) An analysis into the SMD saving with the use of embedded capacitors within the package is also highlighted in this thesis.

f) The benefits of core and I/O decoupling using embedded capacitors was done by implementing the concept on an actual ten metal layer package developed at IBM. The benefits in on-chip capacitance savings using embedded package capacitors is highlighted.

3) **Embedded Planar Capacitors**: The performance of embedded planar capacitors to decouple I/O circuits and improving the overall impedance profile is shown. This work involved the following:

a) Characterization of the impedance profile of a stack up with different thicknesses of planar capacitors was done. The difference in the thickness of the dielectrics translates into a difference in the impedance profile, which is captured using the two port frequency domain measurements.

b) The noise coupling suppression between the signal lines and the power-ground plane was developed. A variation in the noise isolation was observed for the different dielectric thicknesses.

c) Models were developed for the different stripline configurations in the stack-up using modal decomposition and were coupled with the power-ground models to get model to hardware correlation between the model and the measurements.

d) An active test vehicle with the different embedded capacitor dielectric thickness was designed with a 100 MHz clock generator as the source to compare the I/O decoupling performance. Model to hardware correlation between the measurements and

the model were obtained and have been included in the thesis.

e) Simulations were carried out for single ended and differential lines at 1 Gbps and 5 Gbps with different dielectrics, the difference in the performance was captured by the SSN and eye diagram results.

The remainder of the thesis is organized as follows. Chapter 2 presents power dissipation investigation of processors and a proposed methodology to improve overall performance by reducing the power dissipation and increasing the total off-chip bandwidth of processors. The case for embedded capacitors in the package and the board are made in this chapter. Chapter3 investigates the measurement, modeling, and characterization of the embedded capacitors with results showing the model to measurement correlation. Chapter4 deals with the implementation of these capacitors in the design of a capacitor array to decouple core circuits of processors. The performance of embedded planar capacitors in improvement of impedance profile, noise suppression, and decoupling I/O circuits by offering low impedance return current paths is highlighted in chapter 5. The conclusion and future work are presented in chapter 6.

CHAPTER II

PACKAGE REQUIREMENTS FOR MULTI-CORE PROCESSORS

The increasing power trends of processors is putting stringent requirements on the design of PDNs. This is evident with the decreasing target impedances that must be met through the successive technology nodes [table 1]. Therefore an analysis into the different power dissipation components and the use a multi-core processor approach to improve the performance of a processor is investigated. An analysis of the performance trade-offs between single and multi-core processors based on power, frequency, bandwidth, and the role of embedded passives with high density wiring in future packages to support such processors is investigated.

Power in a microprocessor relates to both consumption and dissipation. To maintain the performance improvements of microprocessors, a solution to the power dissipation problem must be found. This would require good power dissipation designs and thermal management solutions. Microprocessor power densities have grown over the technology nodes due to the increase in the number of transistors (active capacitance) and increase in the processor frequency. The supply voltage has scaled down by a factor of 0.8 instead of 0.7 per technology node. The major contributors to the power dissipation of microprocessors in the sub 100 nm node are the active power and leakage power dissipation components. The leakage power scales by a factor of about five in each technology node while the active power scales by a factor of one. Another major challenge for future microprocessors is the performance of on-chip wires at higher processor operating frequencies. Global interconnections on the integrated circuit (IC) that span at least half a chip edge are major causes of latency because of RC

and transmission line delay. While the transistor gate delay decreases linearly with a decrease in the minimum feature size, the wire delay stays nearly constant or increases as the wires become finer and longer. This is due to the increasing wire resistance to load capacitance ratios. In addition, processor clock rates have been increasing and a long wire can affect the processor's cycle time if it belongs to a critical timing path. The result of the above trends is that the micro-architecture of future processors will be critical to the processor performance. The processor resources that communicate with each other in a single cycle must be physically close to each other. This type of architecture would require a CPU consisting of higher speed logic blocks connected by shorter wires.

With the above-mentioned concerns and architectural challenges, the Chip multiprocessor architecture (CMP) has been shown to have the best performance of all the proposed architectures. In the CMP architecture the die is divided into a group of small identical processing cores, that work in parallel with each other [38]. Fig. 20 shows an example of a SPARC microprocessor that is made of eight cores with a shared cache [39]. In this chapter we propose to use the multi-core processor approach to improve the performance of a processor. The performance parameters are defined as the power dissipation and the total bandwidth of the processor. It has been shown that by using a scalable architecture a multi-core processor can outperform the next generation single-core processor [40], [41]. Using the scalable approach an improvement in the bandwidth of a processor can be achieved. Fig. 21, shows the performance improvement expected from using multi-core processors as compared to a single-core processor [42].

The power dissipation for future cost performance processors is expected to be close to 450 W by the end of the decade. Such high value of power dissipation would not be acceptable for single chip package solutions. Leakage power is a major contributor to the total power dissipation and constitutes close to 50% of the total

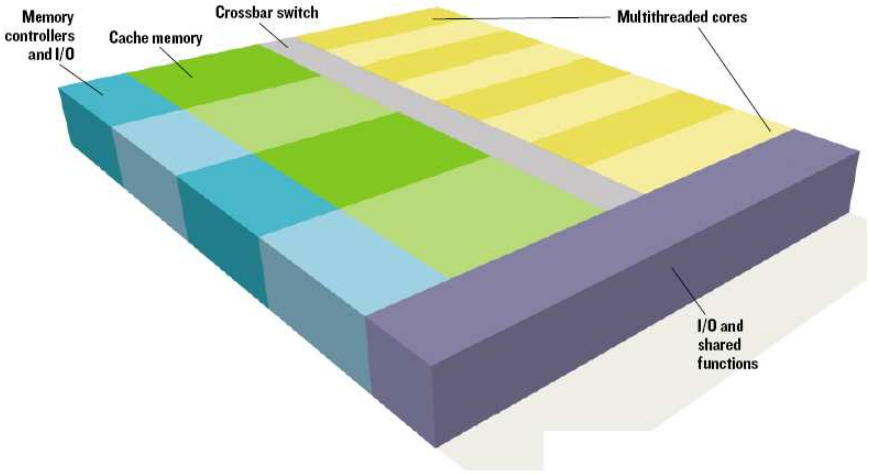


Figure 20: SPARC multi-core processor.

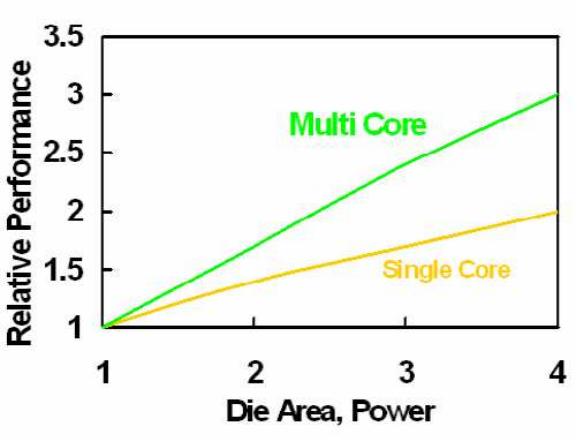


Figure 21: Expected relative performance improvement of a multi-core processor over a single-core processor.

power dissipation for future technology nodes. Therefore, to improve the total power dissipation of the processor, both the active and the leakage power will have to be reduced. A reduction in the power dissipation and an increase in the total bandwidth are achievable using the multi-core approach. This chapter discusses an analysis on the architectural trade-offs between single and multiple processors based on power, frequency, and performance. The multi-core approach would need an extremely high number of I/Os and interconnects to support bandwidths of the order of 1 TByte/s for communications between ICs. The packaging technologies that can enable multi-core processors will be highlighted. An analysis on the need for fine lines and microvias in the package along with fine pitch interconnections between the chip and the substrate is discussed. Embedded passives and microvias are enabling technologies that can provide the maximum amount of functionality and the best electrical performance in the package. All the above technologies can be realized with the system on a package (SOP) paradigm and are required for multi-core processors in the future. This chapter is organized as follows: Section 2.1 discusses the theory behind the power dissipation in active circuits. Section 2.2 explains the methodology used in the power dissipation calculations of the processor for different technology nodes. In Section 2.3 an analysis of the advantages of the multi-core approach is discussed.

2.1 Processor Power Dissipation Calculations

Power dissipation of processors is increasing at an alarming rate through the technology nodes as shown in Fig 22. Active and static power are the main contributors to the total power dissipation in a processor. The general equation that describes active power dissipation is as follows:

$$P_{active} = aCV^2f \tag{15}$$

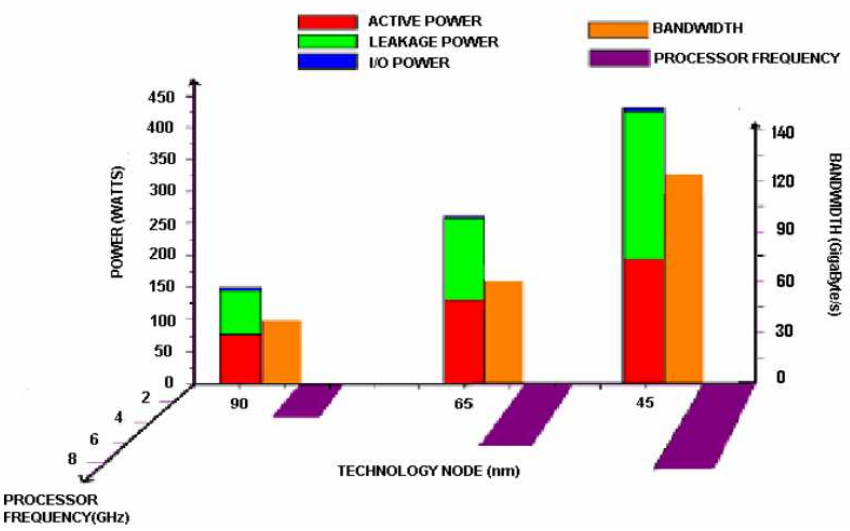


Figure 22: Power dissipation, frequency of operation and bandwidth variation of single-core processors through technology nodes.

Here a is the activation factor of the processor. This number varies between 7% to 15% depending on the application. C is the total switching capacitance of the processor. In equation (15), the frequency of operation of the processor is f and V is the supply voltage. The power lost due to the momentary short circuit at a gates output is given as follows:

$$P_{short} = taI_{short}V \tag{16}$$

Here t is the time for which the short circuit current I_{short} flows. This term has been ignored since the power loss is very small and it contributes to the active power dissipation. The static power dissipation of a processor is given by:

$$P_{static} = VI_{leakage} \tag{17}$$

Where $I_{leakage}$ is the total leakage current in the processor. The third contributor to the total power dissipation is the I/O power or the off chip driving power dissipation. The I/O power is given by:

$$P_{i/o} = 0.5CV^2f \tag{18}$$

Where C is the capacitance that the off chip driver has to charge and discharge. It is the sum of the output capacitance of the driver, the on-chip interconnect capacitance, the solder ball capacitance, and the capacitance of the interconnect on the carrier. Therefore, the total power dissipation of the processor P_{tot} is given by:

$$P_{tot} = P_{active} + P_{static} + P_{i/o} \tag{19}$$

The power trends shown in Fig. 22 far exceed the power dissipation numbers given in the International Roadmap for Semiconductors (ITRS) [2]. Therefore, in order to meet the ITRS numbers it would be required to decrease the total power dissipation of the processor. This can be achieved if the active and static power dissipation components can be reduced. The analysis used to obtain the numbers in Fig. 22 is explained in section 2.2 of this chapter. The leakage current in a transistor which is the source of the static power dissipation is a combination of the subthreshold and gate oxide leakage.

$$I_{leakage} = I_{sub} + I_{goxide} \tag{20}$$

The subthreshold leakage current is given as [43]:

$$I_{sub} = K1 * W * e^{\frac{-V_{th}q}{nkT}}(1 - e^{\frac{-Vq}{nkT}}) \tag{21}$$

The term kT/q is the thermal voltage and is 25 mV at room temperature. W is the width of the gate of a transistor. For calculating the total subthreshold leakage, the combined gate widths of all the transistors in the processor is taken as a measure of W. The terms K and n are experimentally derived and are technology dependent. The gate oxide leakage occurs because of tunnelling of charge carriers through the

gate due to the presence of a high electric field. The gate oxide leakage current is given in a simplified form as follows [43]:

$$I_{goxide} = K2 * W * \frac{V}{T_{ox}} e^{\frac{-\beta T_{ox}}{V}} \tag{22}$$

where $K2$ and β are experimentally derived parameters. T_{ox} is the thickness of the gate oxide and from equation (22) it is observed that an increase in the thickness of the gate oxide would reduce the gate oxide current. This would be against the scaling trends since T_{ox} must decrease proportionally with the technology nodes. Therefore, another option is to increase the dielectric constant of the gate oxide.

However, the major contributor to the leakage power is the subthreshold leakage component [2]. Therefore, I_{sub} would need to reduce to decrease the static power dissipation. From equation (21) there are two ways of reducing I_{sub}. The first one involves switching off the supply voltage, which would make $I_{sub} = 0$. The second approach would be to increase the threshold voltage V_{th}. Increasing V_{th} will reduce I_{sub} because of the negative exponential dependence relation between the two terms. The supply voltage V is also a variable in the static power reduction scenario since it is expected to scale from 1.2 V at the 90 nm technology node to 1 V at the 45 nm technology node for high performance logic. The next part of this section explores the relation between the frequency of operation of the transistor, the supply voltage, and the threshold voltage. The gate delay (T_g) of the chip can be modeled as that of an inverter using the alpha-power model [44]:

$$T_g \ \alpha \ \frac{V}{V - {V_{th}}^{\gamma}} \tag{23}$$

Therefore, the frequency of operation of the chip can be given by

$$f \ \alpha \ \frac{1}{T_g * L_d} \ \alpha \ \frac{V - {V_{th}}^{\gamma}}{V L_d} \tag{24}$$

In equation (24), L_d is the logic depth of the processor. From equation (24) it is observed that an increase in the threshold voltage V_{th} will reduce the frequency of operation if the supply voltage V is kept constant. To compensate for the reduction in the processing resulting from the loss in the frequency of the processor, the scheduled task can be processed in parallel at a reduced operating frequency.

2.2 Power Dissipation Calculations

Equations (15) through (24) in the previous section deals with the general relationship between the voltages, currents, frequency of operation and the active as well as static power dissipation components. In this section a quantitative look into how these factors affect the total power dissipation through the technology nodes is discussed.

The active power component given in equation (15) depends on the total capacitance that has to be switched by the driver. This capacitance includes the output capacitance of the driver, the capacitance of the interconnect on which the signal propagates, and the input capacitance of the receiver circuit. The analysis carried out in this thesis assumes a basic logic block as shown in Fig. 23.

Fig. 23 shows a three input/output NAND gate, which is connected to another three input NAND gate by an interconnect. The method used to calculate the total active power dissipation was based on SUSPENS [37], a system level circuit model for CPUs. The input parameters for all the variables were taken from the ITRS roadmap. This power model was used to calculate the active power dissipation upto the 45 nm node by varying the input parameters based on the technology node. The static power dissipation was calculated by taking the static power dissipation per unit length value from the ITRS and multiplying that by the average gate width of all the transistors in the microprocessor. A few of the parameters used in calculating the active power dissipation numbers, that were input to SUSPENS are listed in table 2.

The width of an N type metal oxide semiconductor (NMOS) and P type metal

Table 2: Input parameters to calculate active power dissipation in SUSPENS for the 90 nm technology node

Input gate capacitance	7.392×10^{-16} F
Input capacitance for a minimum sized NMOS	3.256×10^{-17} F
Interconnect Capacitance	7.36×10^{-16} F
Total capacitance of the interconnect per unit length	8.2×10^{-11} F/m
Permittivity of free space	8.854×10^{-12} F/m
Permeability of free space	1.257×10^{-6} H/m
Chip side length	11.8 mm
Interconnet pitch(Assumed equal on all layers)	5.1×10^{-7} m
Chip clock frequency	3.2 GHz
Rent exponent within a chip	0.404
Width to length ratio of the transistors in a logic gate	11.34
Relative permittivity of oxide	3
Switching factor of all gates	0.15
Average fan out of logic gates	3
Number of wiring layers	13
Number of logic gates on a chip	32166667
Logic depth	25
Core voltage supply	1.2 V

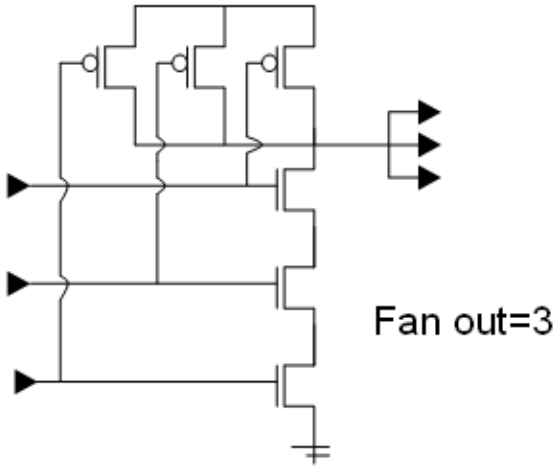


Figure 23: Basic logic gate used in the analysis.

oxide semiconductor (PMOS) are defined as follows:

$$NMOS_{width} = ASIC_{Halfpitch} \times 4 \tag{25}$$

$$PMOS_{width} = NMOS_{width} \times 2 \tag{26}$$

For the 90 nm technology node the ASIC half pitch length is 90 nm. Therefore, the NMOS and PMOS widths are 360 nm and 720 nm respectively. The average width to length ratios is assumed to be 15, which is a standard assumption for logic gates. The physical gate length of a processor in the 90 nm technology node is 37 nm [2]. The static power dissipation per transistor gate length in the 90 nm technology node is 6.6×10^{-16} W/um [2]. The results of the above approach for the 90 nm technology node are as follows: The active power = 77 W and the static power = 70.69 W. Comparing these values to the intel power trends [45], the active and static power are approximately 80 W and 65 W respectively. The power dissipation values obtained at higher technology nodes also compare with the projections [41]. Therefore, the general power dissipation trends are captured using this method and has been used

to carry out further analysis. The I/O power is calculated using equation (18), the capacitance variable in the equation is the sum of the on-chip, solder ball, and off-chip interconnect capacitance. The on-chip interconnect capacitance is calculated using the formula in [46].

$$\frac{C_1}{\epsilon_{ox}} = 2.80(\frac{T}{H})^{0.222} + 1.15\frac{W}{H} \tag{27}$$

Where T and W are the thickness and width of copper respectively. H is the height of copper above the ground plane. For the 90 nm technology node the average capacitance of the on-chip interconnect is 8.2×10^{-11} F.

In Table 3, the power dissipation, operating frequency ,chip-package data rate, and bandwidth are shown through the technology nodes. The off-chip bandwidth (amount of data) of a processor is defined as the product of the off-chip bus speed and the number of I/Os that carry these high speed signals.

$$off\ chip\ bandwidth\ =\ off-chip\ bus\ speed \times\ number\ of\ high-speed\ I/Os \tag{28}$$

For reducing the total power dissipation of the processors it would be required to reduce the active and static power dissipation. The static power dissipation can be reduced by reducing the subthreshold current as seen in equation (21). The method for reducing the subthreshold current is by increasing the threshold voltage (V_{th}). An increase in V_{th} reduces the frequency of operation as shown in equation (24). This reduction in frequency will also reduce the active power dissipation from equation (15). This approach however would lead to a decrease in the performance of the processor, which can be overcome by using a multi-core approach as described in the Section 2.3 .

Table 3: Comparison of single-core processors at different technology nodes

Technology node	90 nm	65 nm	45 nm
Core voltage	1.2 V	1.1 V	1.0 V
I/O pins	1024	1024	1280
Operating frequency	3.0 GHz	4.7 GHz	7.8 GHz
Chip-package data rate	3.0 Gb/s	4.7 Gb/s	7.8 Gb/s
Bandwidth	38.25 GB/s	60 GB/s	124.8 GB/s
Power	153 W	350.3 W	429.78 W

2.3 Analysis of multi-core processors

The processor performance parameters were previously defined as the power dissipation and total bandwidth of the processor. The active power dissipation and bandwidth depend on the frequency of operation of the processor. Another parameter on which the bandwidth depends is the instructions completed per cycle (IPC) of the processor.

An important trend in today's processors is captured by Pollack in [47],[48]. The trend states that in the same technology node, the new architecture outperforms the old architecture by 1.4 - 1.7 times but with a two to three times increase in the area of the processor. If this trend were applied in reverse, the performance of a core would reduce by 40% when the area of the core is reduced by half. For the analysis in this section, the performance loss is assumed due to the degradation of the IPC and frequency. A micro-architecture similar to the one mentioned in [40] is assumed i.e the IPC decreases by 1.4 times when the size of the core is reduced by two times. For this analysis the 90 nm node is taken as the baseline core. The performance per core in the 65 nm and 45 nm technology nodes is assumed to have the same performance as the baseline core in the 90 nm node.

The scaling of the processors assumes that there is no improvement in the micro-architecture of the processor core i.e the micro-architecture remains the same as we

move from one technology node to another. The transistor performance numbers are taken from ITRS. Equation (28) gives the relation of the off-chip bandwidth to the off-chip bus speed and the I/Os that carry these high speed signals. Assume that the number of pins that carry these high speed signals is roughly 10% of all the I/O pins in a particular technology node. For example, consider the 90 nm technology node. Assuming that the chip operates at 3 GHz and that a seamless transition can be provided from the chip to the package, the off-chip signal speed would be 3 Gb/s and the number of I/O pins carrying these signals is 10% of 1024 [2]. Therefore, the bandwidth associated with the single core processor is 38.25 GByte/s. Now consider the 65 nm technology node, making the same assumptions as above and assuming that the processor operates at 4.7 GHz. The bandwidth of the processor at this node would be 59.925 GByte/sec The operating frequency at each node was obtained by solving for the optimum operating point in terms of the threshold voltage, physical parameters of a transistor and the frequency using the relations given in [2]. If we were to use the scalable architecture approach [40] with four cores and use the same micro-architecture as the 90 nm node without any increase in the frequency of operation, the bandwidth in the 65 nm node would increase to $((38.25/1.4^2)) \times 4$ GByte/s, which equals 78.06 GByte/s. This is greater than the bandwidth of a single- core processor. This is assuming that the increase in the number of transistors as we move from one technology node to another is used to increase the computational efficiency rather than on-chip memory [41],[49]. The number of high speed I/Os required to obtain this bandwidth of the chip would increase to 208. Using a similar approach we could increase the bandwidth of the processor by using a larger number of cores. The bottleneck in such an approach would be the total number of I/O pins on the package. A reduction in the frequency of operation from 4.7 GHz to 3 GHz also reduces the active power consumption from 130.894 W to 83.54 W. These numbers were obtained from the analysis explained in the previous section. Using the above

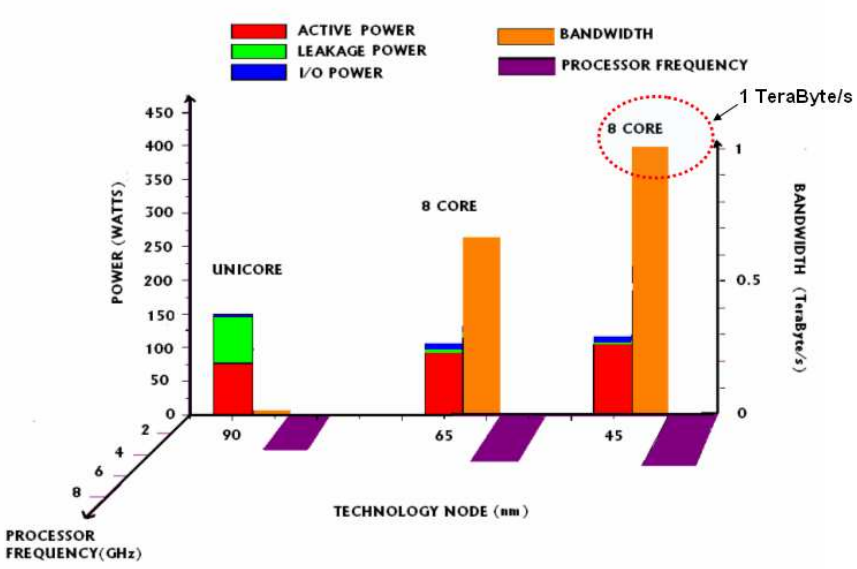


Figure 24: Power dissipation, frequency of operation and bandwidth variation of multi-core processors through technology nodes.

multi-core approach it is possible to obtain a 1 TeraByte/s bandwidth in the future technology nodes with a considerable savings in the power as shown in Fig. 24. An example is discussed in this section.

The single-core processor in the 45 nm technology node dissipates 430 W of power as per the calculations in the previous section. The active and static power components are 195.217 W and 229.58 W respectively. The I/O power is described by equation (18), as given in section 2.1 . The on-chip interconnect was modeled using the method described in [50]. The off-chip interconnect was modeled using the HSpice interconnect models. A scaling factor of 30% based on [2] was applied for the on-chip and off-chip interconnect capacitance through the technology nodes to get the appropriate capacitance value for the 45 nm node. The power dissipation of the I/Os calculated using equation (18) was 4.992 W.

Fig. 24 shows the power dissipation and bandwidth that can be achieved using the multi-core approach for the 65 nm and 45 nm nodes. The analysis of the 45 nm node will be presented here. As mentioned above the multi-core approach is used to reduce

the power and improve the bandwidth of the processor. The optimum operating point in terms of the threshold voltage and frequency of operation is made based on the relations given in [2]. The physical limits of a transistor such as gate oxide thickness are constraints that limit the extent to which the threshold voltage and frequency can be varied. In Fig. 22, it is observed that the major contributor to the power dissipation is the static power. Therefore, the static power is reduced by increasing the threshold voltage V_{th}. This leads to a decrease in the frequency of operation. The optimal operating frequency of the processor was at 4 GHz, a decrease from 7.8 GHz for a single processor. With the assumption made that the micro-architecture of the processors does not improve, this core at 45 nm would be almost identical to the cores in the preceding technology nodes. To obtain the 1 Terabyte/s number using eight cores in the 45 nm technology node, the initial baseline assumption of 10% of all I/O pins that carry high speed signals has been increased to 50% i.e the number of signal lines that now carry these high data rates is $1280 \times 0.5 = 640$. By using the reasoning mentioned earlier in the section, the bandwidth of 1 TeraByte/s was obtained using eight cores, an increase from 124 GByte/s for a single-core processor. The bottleneck for the 1 TeraByte/s would be the number of I/Os required on the package to sustain such a high rate of data. The number of I/Os required to maintain 1 TeraByte/s bandwidth with the chip to board data rate of 4 Gb/s is, 2000. Assuming a 50% overhead of signal pins, the total number of signal pins would be 3000. The total number of pins on the chip with 3000 signal I/Os is 9000, since the number of signal pads are assumed to be one-third of the total pads in the chip [2]. The 9000 pins include the power, ground and I/O pins. The total power dissipation of the eight core processor is 107 W. The active power is close to 100 W, the static power dissipation is negligible and the I/O power is 7 W. Table 4 below compares a single- core processor with a multi-core processor for the 45 nm technology node.

The analysis for the number of metal levels and pins for the package are discussed

Table 4: Comparison of single-core and multi-core processor for the 45 nm technology node

Parameters	Single-core processor (45nm)	Multi-core processor (45nm)
Core Voltage	1.0 V	1.0 V
I/O pins (total)	1280 (ITRS)	3000 (Estimated)
Operating frequency	7.8 GHz	4 GHz
Chip-package data rate	7.8 Gb/s	4 Gb/s
Bandwidth	12.5 GByte/s	1 TeraByte/s
Power	429.78 W	107.39 W
Total number of pins on chip	3840	9000 (Estimated)
Number of pins on the package	2480	4500 (Estimated)

next in this section. The estimate for the total number of pins on chip for the multi-core case has been based on ITRS. The power savings achieved with this scenario could potentially reduce the number of pins required. As an example the number of power ground pins could be reduced from 6000 pins to 3000 pins to support 107.39 W of power. This would reduce the stress on wiring and bump technologies.

A different scaling scenario is presented in which the Instruction per cycle (IPC) is assumed to remain constant as the processors are scaled. Considering the 90 nm single processor as the baseline, 1 TeraByte/s can be achieved in future technology nodes assuming that the trend mentioned in [48] continues. The number of cores required in the 45 nm node to obtain this bandwidth at 4 Gb/s per I/O with 10% of I/O lines carrying these high speed signals at this data rate is 16. If the number of I/Os that carry this high speed signal is increased to 50% as done previously, the number of cores required reduces to four. There are other possible benefits to multi-core processors. For example each core could be turned on or off based on the processing requirements, saving power in the process. In the analysis provided above, it was assumed that all the cores work with the same supply voltage and frequency. This need not be the case, each processor could work with different supply voltages and frequencies of operation,

which could lead to power savings. The above mentioned scenario's are possible with an improvement in the micro-architecture of the processors along with the continuing historical trend in the improvement of transistor performance.

The above analysis shows that a multi-core approach to future processors can improve the overall performance of processors. In order to support the bandwidth that can be provided by these processors it is required that the packages have a high density of I/Os. Also, the scaling of transistors leads to fine pitch interconnects on silicon that are moving towards the nano scale. These fine features increase the resistance of the wire, which leads to an increase in the loss and the RC delay. To overcome this latency and loss, the wires can be moved onto the package with a dielectric of low dielectric constant and low loss. The dimensions of the wires on the package would be in the microns range and would lead to extremely high density wiring on the package. To meet the decoupling requirements for on-chip circuits for future processors, a large portion of the die would have to be used for fabricating decoupling capacitors. This would lead to a reduction of valuable real estate for transistors, which would decrease the computational logic of a processor. Embedded decoupling capacitors on the package address this issue. The next section deals with the packaging technologies that can meet the above requirements.

2.4 Packaging Platform

As highlighted in the previous sections multi-core processor packages would need to support high number of I/Os. This requirement coupled with decoupling that needs to be provided for the core and the I/Os puts stringent requirements on the design of such packages. Real estate for putting surface mount capacitors for core decoupling is an issue, since space is limited. Therefore, the approach would be to use embedded capacitors for decoupling the core as well as the I/O circuits, which is the focus of this thesis. Core decoupling can be achieved by placing individual thin/thick film

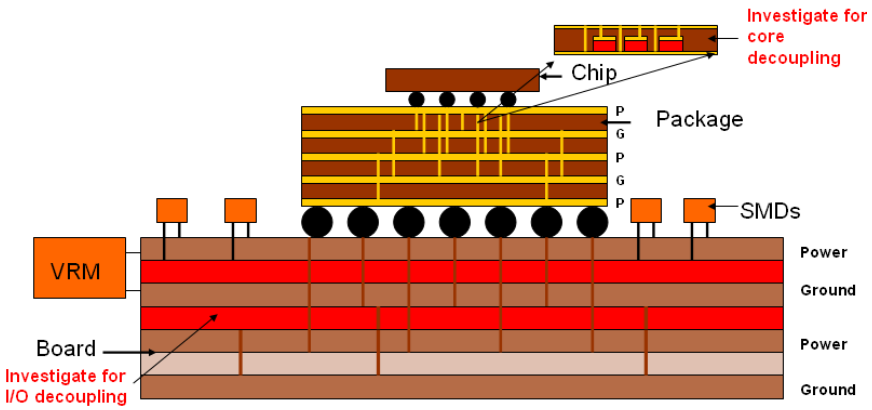


Figure 25: Cross section showing individual embedded capacitors for core decoupling in a package and embedded planar capacitors in a board for I/O decoupling.

capacitors in the package and I/O decoupling can be provided by using embedded planar capacitors in the board as shown in Fig .25.

This section describes the enabling technologies that can provide a potential solution to the packaging issues in multi-core processors. Integral passives are becoming increasingly important in realizing next generation electronics industry needs through gradual replacement of surface mount components. The need for integral passives emerges from the increasing demand for product miniaturization thus requiring components to be smaller and packaging to be space efficient. The remaining part of this chapter highlights the packaging platform required to support future multi-core processor packages with high density I/Os and decoupling requirements.

2.4.1 Package details estimation

The number of metal levels and pins required for the 45 nm node multi-core processor package is discussed in this section. The number of signal I/Os on the chip was calculated to be 3000. With a 12.5 um width and spacing line, the pitch of the interconnect is 25 um. Assuming the size of the solder bump is 50 um, the space between the edges of the solder bump will be 75 um in a 125 um solder bump pitch.

Therefore, there would be three escape rows between two solder bumps. The number of I/Os that can escape on the first metal layer is 1104. Therefore the number of metal levels required for 3000 signal I/Os would be three. If there are two power ground plane pairs with embedded discrete capacitors and a common power or ground plane, and a ground plane between each signal layer, the number of metal planes needed would be seven. The total number of metal planes required in the package will then be 10. The number of pins and pin pitch at the bottom of the package will decide its size. With 9000 chip pins, the package pins could be reduced to around 4500 i.e 3000 signal I/Os and 1500 power and ground pins. There need not be a one-to-one correspondence between the pins on the chip and the number of pins at the bottom of the package because of common power and ground buses within the package, which reduces the number of power and ground pins on the bottom of the package. With a 0.5 mm board bump pitch, the size of the package would be 33.5 mm X 33.5 mm. It is assumed here that the board bump technology can support high signal data rates. The above calculation was based on the scenario listed in the ITRS regarding the ratio of signal pins to power and ground pins. In the case of the multi-core processor for the 45 nm node, the power dissipation is very less. Therefore the number of power ground pins could be reduced to 3000. The total number of chip pins in this case would then be 6000. Using the same reasoning as given above the number of pins at the bottom of the package can be assumed to be 3500. The size of the package with a 0.5 mm pitch would be 29.5 mm X 29.5 mm, a reduction of 250 mm^2 in area as compared to the earlier case. The above discussion is for a single multi-processor chip on the package. In case of more than one multi-core processor chip, the number of I/O pins in the package will increase. Assuming common power and ground buses for both the chips in the package, the number of power and ground pins on the package would be the same as for a single chip. With 4500 total pins on the bottom side of the package as shown earlier in the section for a single chip, the total number of

pins with 2 multi-core processor chips would be 7500. The size of the package with a 0.5 mm solder ball pitch would be 43.3 mm X 43.3 mm. With 3500 total pins for a single chip, the total number of pins for 2 chips will be 6500, translating into a size of 40.3 mm X 40.3 mm. The worst case assumption is made for the above case i.e all the signal I/Os have to be taken off the package. In the SOP approach this need not be the case, as two chips could communicate with each other in parallel reducing the signal I/Os that need to be taken off the package. The SOP approach assumes that the complete stand alone system is on the package. Assuming the most efficient case, in which both processors communicate with each other in parallel using all the pins, the size of the package will be limited by the chip sizes. A package size of 25 mm X 25 mm is possible with an individual chip size of 11.4 mm X 11.4 mm. Different scenarios are possible with a SOP approach. RF, optical, and memory could also be integrated with the multi-core processor in the package. This could lead to different pin counts and different size of the package depending on the application. Therefore the minimum size package of a single multi-core processor chip with 0.5 mm board bump pitch is 29.5 mm X 29.5 mm. With the above estimations, the passive technologies that can support a SOP concept are given in the next section.

2.4.2 Fine pitch interconnects

Packages that support multi-core processors would require high density of I/Os along with fine pitch high speed interconnects. The NEMI roadmap defines the need for four to eight layers of $5-10$ um wiring for future system boards. High speed signals require low loss dielectric materials of the order of 0.001. Signal delays in global interconnects on ICs will dominate gate delay and therefore impact the system performance. Global wiring on chip is typically less than 1 um width using $1-2$ um dielectric thickness. These small dimensions translate into very high resistivity lines which limits the high speed of signals on interconnects that are greater than 10 mm.

The SOP approach would provide the opportunity for global wires on-chip to be integrated on the package if line widths of the order of $10-13$ um are made available using thin dielectric films. With a dielectric constant of four, 50 Ω characteristic impedance for a 12.5 um wide line can be achieved if the thickness of the dielectric is 7.5 um. Line widths in the range of $3-5$ um will further reduce the total number of signal levels, the thickness of the dielectric and therefore the total thickness of the package. The typical methodologies used to increase wiring density are: 1) reducing the line width and line space; 2) increasing the number of layers and, 3) using small capture pads. The research at Packaging Research Center (PRC) is focused on all of these including 1) ultra-fine lines of $3-5$ m dimensions, and 2) stacked microvias of $10-15$ m diameter. Precise control of the photolithography process combined with high resolution liquid photoresists coated as thin films has been used to achieve copper lines with less than 5% control of X, Y and Z dimensions. With the technologies that are being developed, the wiring density of future packages can be met. For example, consider the 45 nm node in which it was estimated that the total number of pins on chip would be 9000. If the pins were to be distributed evenly on a package of size 140 mm^2, the pitch required would be approximately 125 um. An example of fine pitch routing for 100 m pitch flip chip packages is shown in Fig. 26, which illustrates two lines per channel using 12 m lines/spaces fabricated on build-up layers on an FR-4 substrate. Planar embedded capacitors are useful in providing low impedance to the return current, which enables decoupling high speed I/O's as shown in Chapter 5.

2.4.3 Microvias

A novel low cost process for fabricating multilayer stacked via structures has been developed using a panel electroplating and subtractive etch process called P2ES (panel plating etched stud) [51]. Filled stacked vias of 50 um, 75 um and 100 m diameter up to four metal layers have been demonstrated using this low cost large area approach.

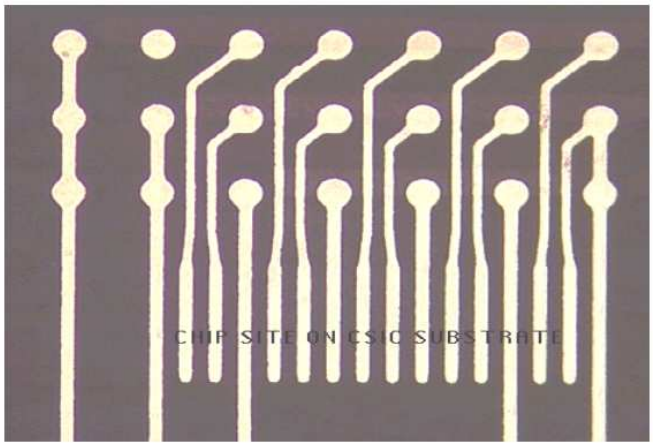


Figure 26: Two 12 um lines through a 100 um pitch flip chip.

Stud height uniformities of less than 1 m have been demonstrated using this technique on 300 mm x 300 mm FR-4 substrates. The stacked via structure along with the ultra-fine lines can potentially meet the interconnection and global wiring requirements of next generation SOP packages.

2.4.4 Embedded Capacitors

Among various passive devices, capacitors are the hardest to integrate owing to non-availability of material systems to cover the range of capacitances required to provide decoupling over the entire frequency band for today's systems. With the trend towards higher power and lower voltage, clean power has to be supplied to the integrated circuits. Decoupling capacitors act as reservoirs of charge and supply the transient currents for the switching circuits, reducing the switching noise. On-chip decoupling capacitance with negligible parasitic inductance provides the lowest power supply impedance at high frequencies. Thin oxides are generally used to supply the capacitance on-chip though they occupy valuable silicon real estate leading to trade-offs in chip area, cost and noise tolerance. To reduce the decoupling capacitance burden

on the chip, highest impedance peaks in the frequencies of 100s of MHz that lead to mid-frequency noise are currently reduced by placing individual decoupling capacitors across the power rail in mother boards. Individual SMD capacitors are now becoming speed limiting factors by the nature of their size, configurations, and consequent distance from the active circuit they serve. These are relatively large in size and cannot be mounted close to the IC which leads to higher series inductance. The lead inductance of discrete capacitors limit the frequency of operation to the lower MHz range section 1.6 and also do not enable microminiaturization at system-level.

Embedded capacitance in the package can help decouple higher frequency bands because of the smaller inductances associated with them. To be useful in decoupling a fast load, any capacitor must have low impedance over a reasonable range of frequencies. For future microprocessors, the smaller voltage tolerances and higher operating frequencies necessitate smaller inductance for the capacitor components. For an array application, where the capacitor has multiple power and ground pins, these inductances will be reduced by a factor of N, where N is the number of power-ground terminal pairs. Surface mount decoupling strategies typically string excess capacitance in parallel in order to compensate for the overall inductance. The much lower inductance of embedded thick/thin film decoupling capacitors enables less total capacitance to be used. These capacitors can be integrated within a package at different layers as shown in Fig. 27. More details regarding the positioning, placement, and design of these capacitors will be explained in chapters 3 and 4 respectively.

I/O decoupling can be achieved by using embedded planar capacitors in a board to provide low impedance paths for return currents. The thin dielectrics increase the capacitance and reduce the inductance decreasing the overall impedance of the structure. Details regarding the advantages of these capacitors will be highlighted in chapter 5.

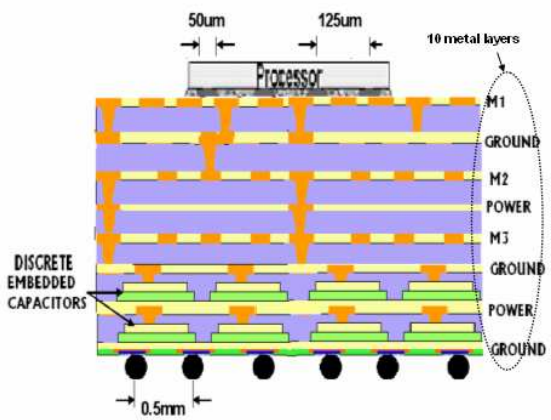


Figure 27: Cross section showing the placement of embedded capacitors in a package.

2.5 Summary

The power dissipation trends of processors has been captured in this chapter by developing models to capture the active and static power dissipation trends. The analysis of multi-core processors has been shown to improve overall performance i.e an increase in the off-chip bandwidth and decrease in power dissipation of processors. A description into the packaging platform required to support high density I/Os to support future processors has also been investigated in this chapter. The rest of this thesis investigates the measurement, modeling, characterization, and performance of the individual embedded capacitors developed at the PRC using the hydrothermal process and capacitors fabricated by DuPont. These capacitors are primarily used for core decoupling high performance circuits. The performance of embedded planar capacitors fabricated by DuPont in decoupling I/O circuits by providing low impedance to the return current of I/O signals has also been investigated in this thesis.

CHAPTER III

DESIGN AND CHARACTERIZATION OF INDIVIDUAL EMBEDDED PACKAGE CAPACITORS

The advantages of using discrete thin/thick film capacitors was briefly mentioned in chapter 1. An analysis into the performance improvements using these capacitors is presented in this section. As an illustration of the concept, a simulation of the performance of a decoupling array with the DuPont capacitors within a package was performed. Fig. 29 shows the performance of an embedded decoupling network that can be designed to provide decoupling at frequencies above 100 MHz and can target impedances of the order of 1 mΩ as compared to the profile shown in Fig. 15. Care was taken that all the capacitors were placed directly under or around the processor to minimize the effect of the spreading inductance of the power ground planes. The different sized capacitors that were used to obtain the impedance profile shown in Fig. 29 were placed in two discrete capacitor layers within a package. The details regarding the package stack up are presented in section 4.1. 25 1.2 mm $\times$ 1.2 mm capacitors along with 25 0.5 mm $\times$ 0.5 mm capacitors were used to target the lower frequency band. The higher frequency band was targeted using 25 1.2 mm $\times$ 1.2 mm capacitors and 42 0.75 mm capacitors. The two combinations of 1.2 mm $\times$ 1.2 mm capacitors were placed in different levels of the package. Due to their different placement, the via inductances associated with each combination were different and they therefore resonate at different frequencies. This analysis was done to show the advantages of using embedded capacitors and by proper selection of the sizes of the capacitor the mid-frequency band from 100 MHz to 2 GHz can be targeted for decoupling. The rest of this chapter is organized as follows 1) The description of the

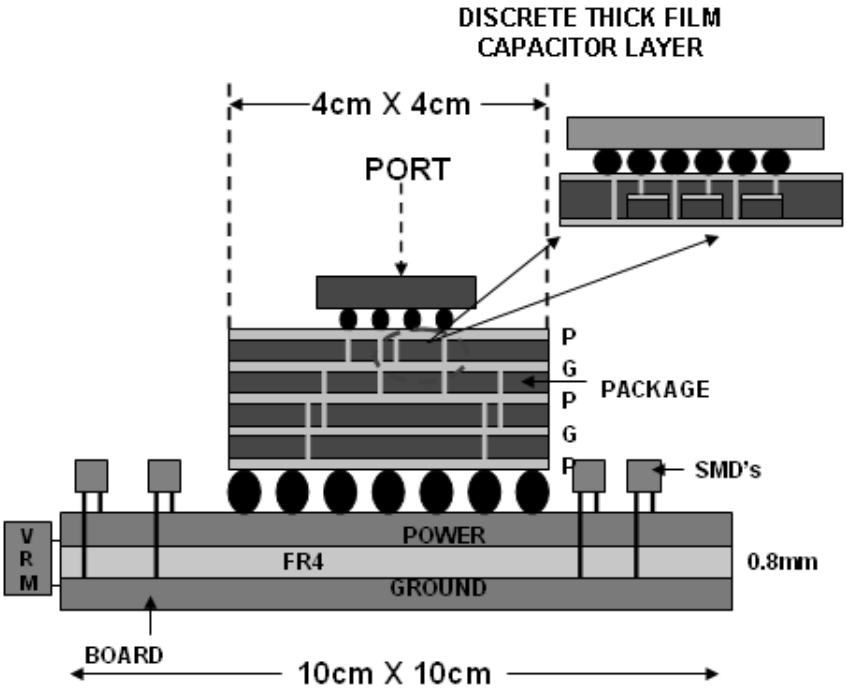


Figure 28: Discrete capacitor layer in the package

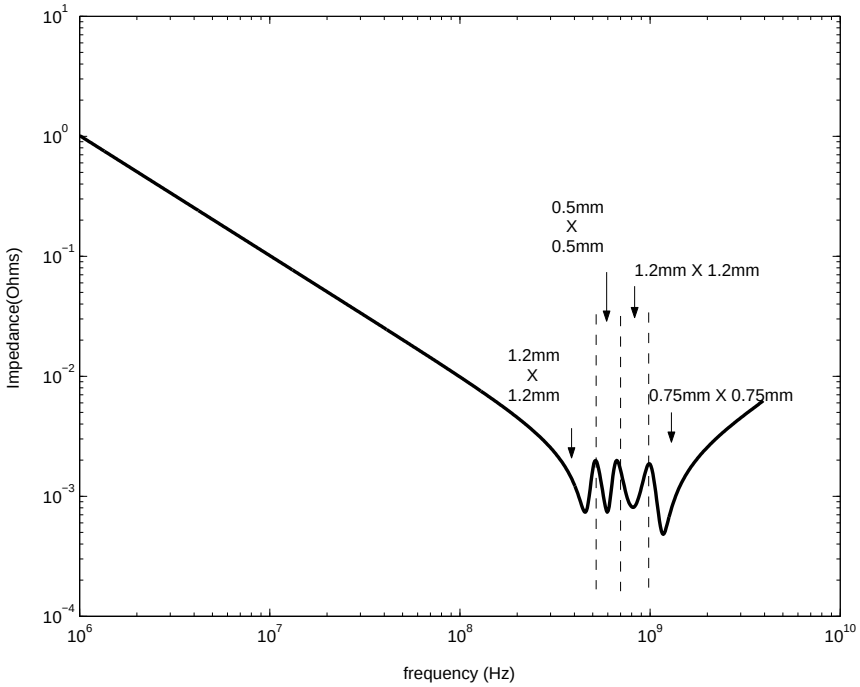


Figure 29: Impedance profile with embedded capacitors in the package

capacitor structures which includes the design, shape and the material properties will be presented; 2) The modeling methodology used to model these structures is highlighted in this chapter; 3) The measurement and characterization of the thin/thick film embedded capacitors is explained. A detailed analysis into the self and transfer impedance measurement methodology used to characterize these capacitors will be presented; 4) The model to hardware correlation of the results is also highlighted in this chapter.

3.1 Description of capacitor structures

This section highlights the properties of the different materials used as dielectrics for the embedded capacitors. The first material is a thin film hydrothermal based barium titanate capacitor manufactured at the Packaging Research Center(PRC) [52].

A brief description into the process used to fabricate the capacitors is presented in this part of the section. These capacitors are fabricated on laminated copper foils using low cost and low temperature($< 100^oC$) hydrothermal process. The copper laminate is clad with Titanium and treated with Barium ions (Ba^{+2}) in highly alkaline solution at 95^oC. The resultant Barium Titanate film is 300 nm thick and has a dielectric constant of 300. The top electrode is 2 um thick copper. The loss tangent of the material is less than 0.06 and the capacitance density is of the order of 1 μF/cm^2. The thickness of the grain sizes of barium titanate in the dielectric vary from 60 nm to 80 nm. The cross section of a barium titanate capacitor is shown in Fig 30. The top electrode is 2 um thick copper and the bottom electrode is 12 um thick copper with 500 nm thick titanium as shown in Fig 30. Square capacitors of size 1 mm$\times$1 mm that were fabricated and measured are shown in Fig. 31.

The other material investigated is a thick film capacitor material from DuPont. The thickness of the dielectric is 20 um and the dielectric constant is 3000. The capacitance density is of the order of 1.328 nF/mm^2 and the loss of the dielectric is less

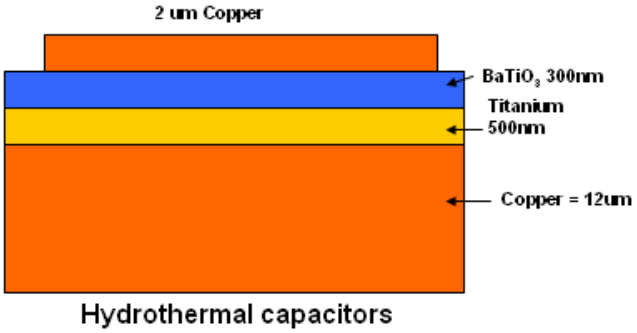


Figure 30: Cross section of capacitors fabricated at PRC using the hydrothermal process.

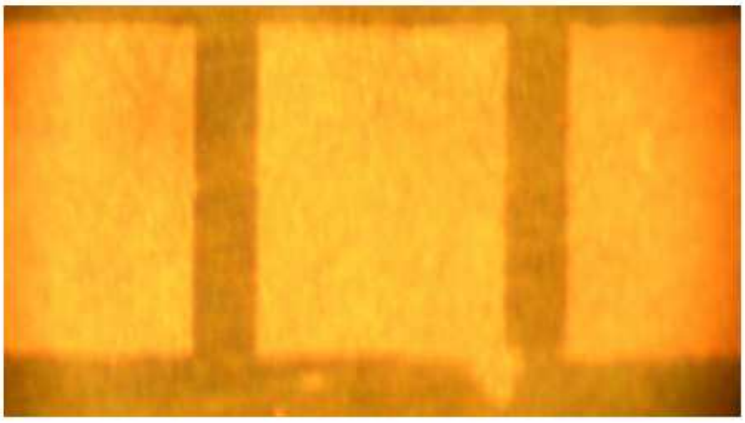


Figure 31: Fabricated square barium titanate capacitors.

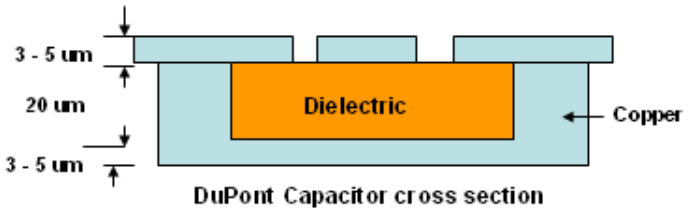


Figure 32: Cross section of DuPont's embedded capacitor.

than 0.01 at 1 MHz. The cross-section of the capacitor fabricated by DuPont is shown in Fig 32 and a snapshot of the actual capacitor embedded in BT laminate is shown in Fig 33. Different size capacitors were designed and fabricated as shown in Fig. 34. A brief description of the fabrication process of these capacitors is presented in this section. The process uses a fired-on-foil approach. A thick film capacitor dielectric and electrode paste is screen printed on to the copper foil in the location desired in the circuit and fired in nitrogen at approximately 900^oC to form the fired-on-foil components. Following this, the foil maybe treated to improve adhesion to prepeg and then it is bonded component face down, into a laminate structure used to fabricate inner-layers for a multi-layer printed wiring board. The inner layer is then etched to form the capacitor electrodes from the copper foil. Following this, the inner layer may receive additional treatment before it is incorporated inside a multi-layer printed wiring board [53]. The placement of these capacitors in the package was previously shown in Fig 27 in chapter 1. This chapter investigates the design, characterization, and modeling of the thin/thick film discrete embedded capacitors.

3.2 Measurement and Characterization of capacitors

A two port frequency domain measurement methodology was used to measure the impedance of the capacitive structures [54]. One port measurements are usually

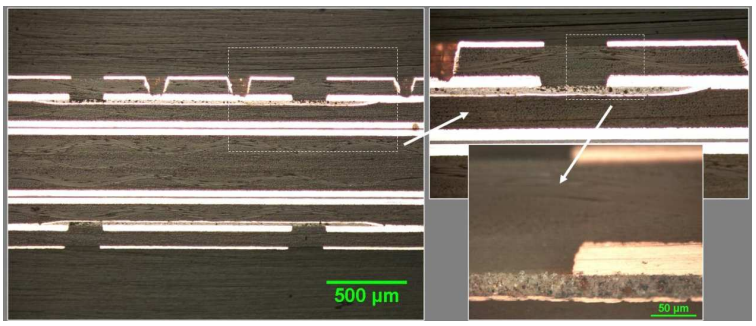


Figure 33: Embedded individual capacitor in BT laminate.

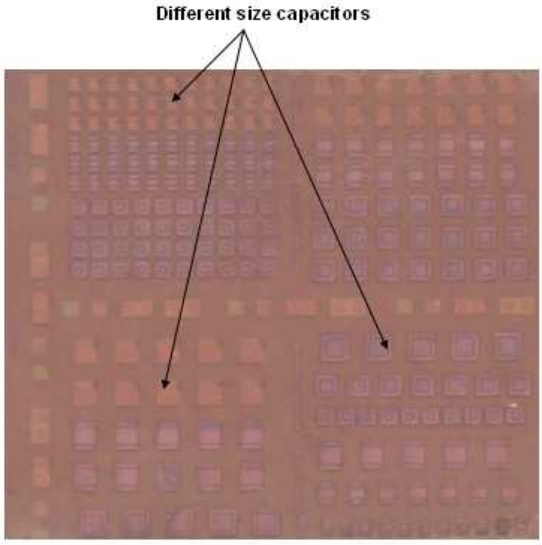


Figure 34: Designed test vehicle with different sized capacitors fabricated by DuPont.

inaccurate when measuring low impedance structures of the orders of $10's$ of mΩ. This is because near the resonant frequency of the structure, the value of the reflection coefficient is close to -1. This can be explained as follows; the reflection coefficient is given as:

$$\Gamma = \frac{Z_L - Z_O}{Z_L + Z_O} \tag{29}$$

The system impedance of the VNA is 50 Ω , and if the structure has an impedance in the mΩ range at frequencies close to the resonant frequency, then from the above formula all the energy will be reflected back and the readings will be very noisy. Another important source of error in one port measurements is the contact resistance of the probe when it touches the structure. This value of resistance depends on the contact and could vary for different measurements i.e it is not repeatable. The contact resistance ends up in series with the impedance of the structure and adds to the inaccuracy of the readings.

To overcome the above limitations of a one port measurement, two ports are generally used to measure power plane structures. The advantage of two port measurements is that the impedance of the structure is extracted from the $S21$ parameters rather than $S11$ or $S22$. The advantage being that the discontinuities that were present in the one port measurement were in series with the device under test (DUT). In the two port measurement methodology the resistance and inductance due to the discontinuity are in series with the 50Ω system impedance of the VNA and the following sections in this chapter will highlight the error introduced by these discontinuities, which are negligible. Since, the impedance of the DUT is extracted from the $S21$ measurements, an approximation to a one port reading can be done if the two ports are placed very close to each other. The method will be briefly described in this section.

The measurement equipment included Agilent's 8720ES vector network analyzer (VNA) with a bandwidth of 50 MHz to 20.5 GHz and 500 um GS-SG cascade probes. A standard short,open,load, and thru SOLT calibration was carried out on the probes using

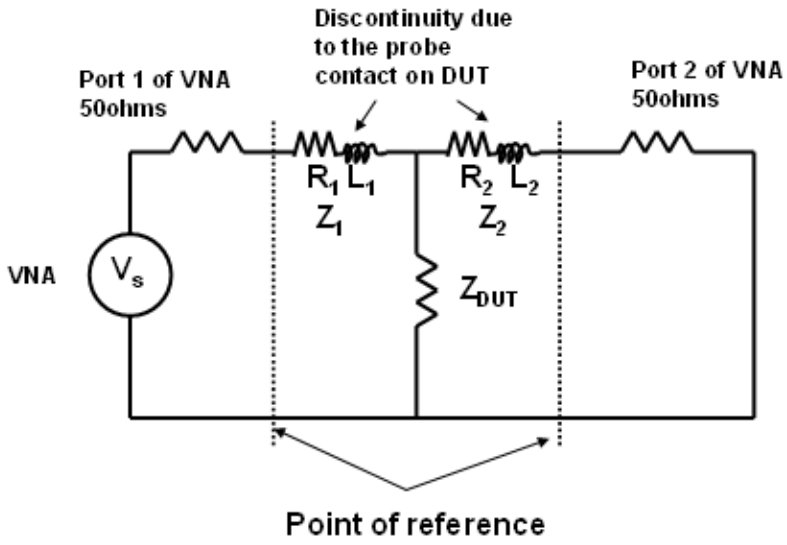


Figure 35: The equivalent circuit of the measurement showing the discontinuity with the two ports placed very close to each other.

the ISS substrates.

3.2.1 Self Impedance Measurement

The basic equations used to characterize these structures is explained: For the self impedance measurement of the DUT, the two probes connected to the VNA are placed very close to each other. The equivalent circuit diagram by including the parasitics is shown in Fig. 35.

The S matrix can be obtained by using the transformation equations. The transformation equation used to convert the Z parameters to the S parameters is as follows [55]:

$$S21 = \frac{2 \times Z12 \times Z_O}{(Z_{11} + Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}} \tag{30}$$

The above equations are modified based on the discontinuities. The discontinuities can be expressed as:

$$Z_1 = R_1 + j\omega L_1 \tag{31}$$

and

$$Z_2 = R_2 + j\omega L_2 \tag{32}$$

Where R_1, R_2 and L_1, L_2 are the contact resistances and inductances between the probe and the DUT. From Fig. 35, $Z11$ and $Z22$ are derived from the Z parameter equations and are $Z_{DUT} + R_1 + j\omega L_1$ and $Z_{DUT} + R_2 + j\omega L_2$ respectively. S_{21} is derived by using the standard conversion factor

$$S21 = \frac{2 \times Z12 \times Z_O}{(Z11 + Z_O)(Z22 + Z_O) - Z12 \times Z21} \tag{33}$$

Substituting the values for $Z11$, $Z22$ and $Z12$, we get the following equation for $S21$.

$$S21 = \frac{2Z_{DUT}Z_O}{(Z_{DUT} + R_1 + j\omega L_1 + Z_O)(Z_{DUT} + R_2 + j\omega L_2 + Z_O) - Z_{DUT} \times Z_{DUT}} \tag{34}$$

where $Z12$=$Z21$=Z_{DUT}. Further simplifying equation 34 by assuming that $Z_O >> R_1$ and $Z_O >> R_2$

$$S21 = \frac{2 \times Z_{DUT} \times Z_O}{(Z_{DUT} + j\omega L_1 + Z_O)(Z_{DUT} + j\omega L_2 + Z_O) - Z12 \times Z21} \tag{35}$$

Solving for Z_{DUT} from the above equation we get

$$Z_{DUT} = \frac{S21}{2} \frac{Z1 \times Z2}{(Z_O - S12\frac{(Z1+Z2)}{2})} \tag{36}$$

Where $Z1$ and $Z2$ are Z_O+$j\omega L_1$ and Z_O+$j\omega L_2$ respectively. The error introduced due to the discontinuities is calculated by making an assumption that Z_1=Z_2. Equation 36, reduces to

$$Z_{DUT} = \frac{S21}{2} \frac{Z1}{\frac{Z_O}{Z_1} - S21} \tag{37}$$

Assuming that the inductance due to the discontinuity is 0.2 nH equation 37 can be rewritten as:

$$Z_{DUT} = \frac{S21}{2} \frac{(50 + j\omega \times 0.2 \times 10^{-9})}{(\frac{50}{50+j\omega\times0.2\times10^{-9}} - S21)} \tag{38}$$

The error introduced by the discontinuity will be less for low impedance structures. From equation 38, it is evident that the error is dependent on the measurement

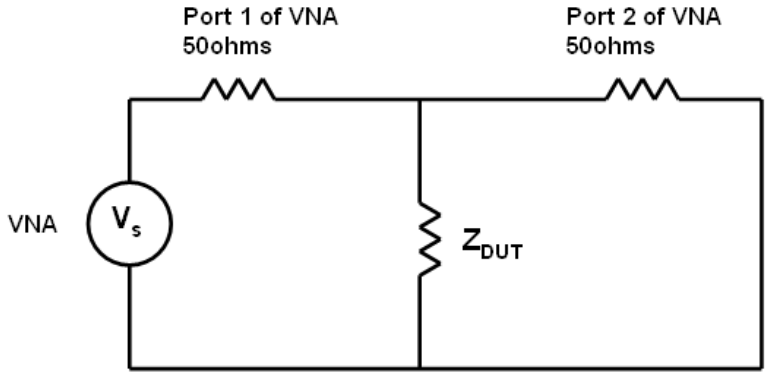


Figure 36: Measurement set up using 2 ports of the VNA

frequency range. At 10 GHz, the $(\frac{50}{50+j\omega\times 0.2\times 10^{-9}})$ term is equal to 0.97. For the error analysis, the denominator is assumed to be $1 - S21$. At 10 GHz, the numerator = 51.55, therefore equation 38 reduces to the following.

$$Z_{DUT} = 25.77 * \frac{S21}{1 - S21} \tag{39}$$

The error introduced from the above equation is 3% when compared to the equation 41, which is derived without the effect of discontinuity. For low values of $S21$, the error introduced would be lower.

Therefore, this part of the section derives the equations used to calculate the impedance profile of the DUT by neglecting the effect of the discontinuities. The equivalent circuit by ignoring the effect of the discontinuity is shown in Fig. 36. The structures can be characterized by assuming a "T" network approach as shown in Fig. 37. $Z11 = Z22 = Z12$ since the two probes are placed very close to each other on the DUT. Therefore, Fig. 37 can be approximated as Fig. 38. All the elements of the two port Z matrix will be equal to each other.

In the above equation Z_0=50Ω, is the impedance of the VNA. The resultant expression for $S21$ by substituting for $Z11 = Z22 = Z12 = Z_{DUT}$ is as follows:

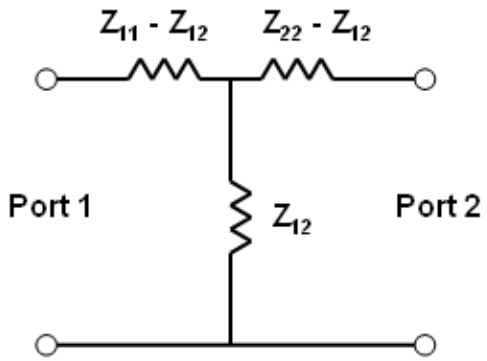


Figure 37: Equivalent T network of the experimental set up.

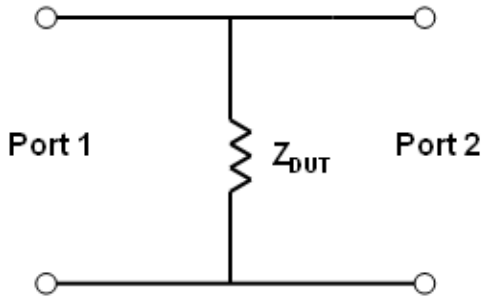


Figure 38: Modified T network of the experimental set up.

$$S21 = \frac{2Z_{DUT}Z_O}{(Z + Z_0)^2 - Z_{DUT}^2} \tag{40}$$

Where $Z_0 = 50\ \Omega$ and solving the above equation for Z_{DUT} we obtain the following equation:

$$Z_{DUT} = 25 * \frac{S21}{1 - S21} \tag{41}$$

Be separating the real and imaginary parts of Z_{DUT} and $S21$, the equations listed below are obtained.

$$ReZ(dut) = 25 \times \frac{(Re(S21) \times (1 - Re(S21)) - Img(S21)^2)}{((1 - Re(S21)^2) + Img(S21)^2)} \tag{42}$$

$$ImZ(dut) = 25 \times \frac{Img(S21)}{((1 - Re(S21)^2) + Img(S21)^2)} \tag{43}$$

Where $ReZ(dut)$ and $ImZ(dut)$ are the real and imaginary parts of the device under test. The above equations were used to characterize the impedance profile of the individual thin/thick film capacitors highlighted in this thesis.

3.2.1.1 Error Analysis

This part of the section investigates error introduced due to via discontinuities. The via can be assumed to be modeled as a series combination of a resistor and an inductor. As done in the previous part of this subsection, the following is assumed: $Z_O >> R_1$ and $Z_O >> R_2$, where R_1 and R_2 are the resistances of the vias. The self impedance is calculated by using reflection theory since the reference impedance has changed from 50Ω to $Z1$ and $Z2$, where $Z1$ and $Z2$ are $Z_O + j\omega L_1$ and $Z_O + j\omega L_2$ respectively. L_1 and L_2 are the series inductances of the vias. $S11$ can be calculated as follows:

$$S11 = \frac{\frac{Z_{DUT} \times Z2}{Z_{DUT} + Z2} - Z1}{\frac{Z_{DUT} \times Z2}{Z_{DUT} + Z2} + Z1} \tag{44}$$

also $S21 = 1 + S11$, solving for $S12$ and rearranging to get Z_{DUT}, the following expression is obtained.

$$Z_{DUT} = S21(\frac{Z1}{2})\frac{1}{1 - S21(\frac{Z1+Z1}{2Z2})} \tag{45}$$

The above equation can be rewritten to analyze the error introduced because of the discontinuity. For this analysis assume that $Z1 = Z2 = Z_O + j\omega L$. L is the inductance due to the discontinuity and is assumed to be 0.2 nH. Equation 45, reduces to the following:

$$Z_{DUT} = S21(\frac{Z1}{2})\frac{1}{1 - S21} \tag{46}$$

Equation further reduces to the following

$$Z_{DUT} = S21 \times 25(\frac{1 + j\omega\varsigma}{1 - S21}) \tag{47}$$

ς is $\frac{L}{50}$, therefore the error introduced by measuring a structure with an impedance of 0.2Ω at 10 GHz with 0.2 nH of inductance is close to 3%. This error analysis is similar to the analysis carried out in [56]. However, the error introduced by the vias depend on the thickness of the board and the frequency range over which the measurement is carried out. The error introduced may be significant for thick boards with vias that span the depth of the board.

3.2.2 Transfer Impedance Measurement

Extraction of the transfer impedance from the $S21$ measurements can also be done and is shown in the following analysis. If the probes are placed a certain distance apart from each other then $Z11 \neq Z22 \neq Z12$, therefore, equation 36 derived for the extraction of the self impedance cannot be used in this situation. The model used for the following analysis is shown in Fig. 37. By including discontinuities in the analysis the equivalent "T" network is modified as shown in Fig. 39. $Z11$ and $Z22$ can be derived from the standard definitions of the Z parameters. From Fig. 39, $Z11$ and

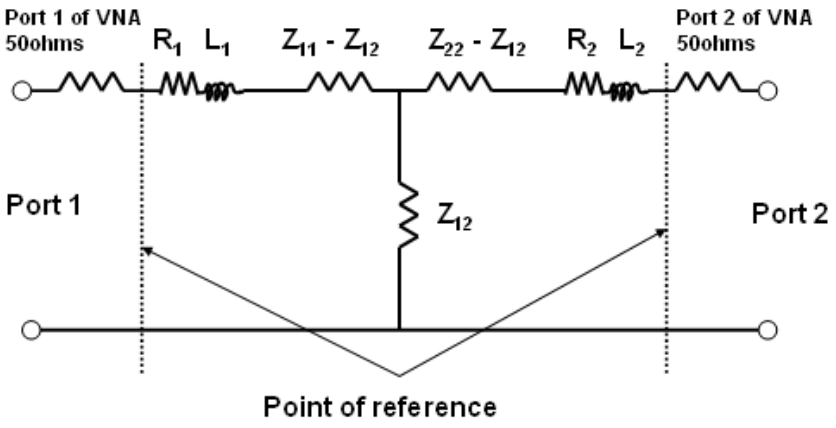


Figure 39: The equivalent circuit of the measurement showing the discontinuity with the two ports placed far apart from each other.

$Z22$ are $Z11 + R_1 + j\omega L_1$ and $Z22 + R_2 + j\omega L_2$ respectively. By using the standard conversion of $S21$ to Z parameters we obtain the following equation.

$$S21 = \frac{2Z12Z_O}{(Z11 + R_1 + j\omega L_1 + Z_O)(Z22 + R_2 + j\omega L_2 + Z_O) - Z12^2} \tag{48}$$

Assuming that $Z_O >> R_1$ and $Z_O >> R_2$, the above equation reduces to the following.

$$S21 = \frac{2Z12Z_O}{(Z11 + Z_1)(Z22 + Z_2) - Z12^2} \tag{49}$$

Solving the above equation, the following equation is obtained for Zij.

$$Zij = \frac{(S21 \times Z1 \times Z2)}{2} \frac{(1 + \frac{Z11}{Z1})(1 + \frac{Z22}{Z2})}{(Z_O + \frac{S21Z12}{2})} \tag{50}$$

For low impedance power plane structures, $Z2 >> Z22$,$Z1 >> Z11$, and $Z_O \approx Z1 \approx Z2$. Therefore, equation 50 can be reduced to the following:

$$Zij \approx S21 \times 25 \tag{51}$$

The above equation was used to characterize the transfer impedance characteristics of the DUT in this thesis. This analysis highlights the negligible effect of discontinuities

on the transfer impedance measurements on low impedance structures using the two port methodology.

Assume that there are no discontinuities involved in the transfer impedance measurement. Therefore, by using the standard conversion for $S12$ to Z parameters we obtain

$$S21 = \frac{2Z12Z_O}{(Z11 + Z_O)(Z22 + Z_O) - Z12^2} \tag{52}$$

Solving for Zij, the following equation is obtained.

$$Zij = \frac{S21}{2} \frac{(Z11 + 50)(Z22 + 50)}{(Z_O + \frac{S21Z12}{2})} \tag{53}$$

Also, assuming that $50>>Z11$, $50>>Z22$ and $Z_O>> \frac{S21Z12}{2}$, the above equation reduces to equation 51.

This part of the section investigates the variation in the transfer impedance measurements because of the via discontinuities. The via discontinuities are modeled by a series combination of resistors and inductors. As done in the previous part of this subsection, the following is assumed: $Z_O >> R_1$ and $Z_O >> R_2$. The transfer impedance is calculated by using reflection theory since the reference impedance is no longer 50Ω. $S11$ can be calculated as follows:

$$S11 = \frac{\frac{(Z11 \times Z22 + Z11 \times Z2 - Z12^2)}{Z22 + Z2} - Z1}{\frac{(Z11 \times Z22 + Z11 \times Z2 - Z12^2)}{Z22 + Z2} + Z1} \tag{54}$$

Where $Z1$ and $Z2$ are $50+j\omega L_1$ and $50+j\omega L_2$ respectively. Solving for $S21 = 1+S11$, and then for Zij, the following equation is obtained.

$$Zij = \sqrt{\frac{S21 \times (Z1)(Z2) - 2 \times (Z11)(Z2)}{(S21 - 2)}} \tag{55}$$

The above equation was obtained by assuming that $Z1>>Z11$ and $Z2>>Z22$.

3.2.3 Measurement and characterization set up

The measurement set up for characterizing the capacitive structure is shown in Fig. 40. Probe 1 is the transmitter and probe 2 measures the voltage drop across the device

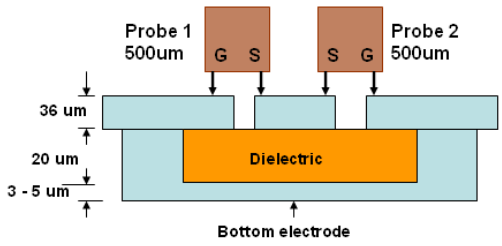


Figure 40: The measurement set up for characterizing the capacitors.

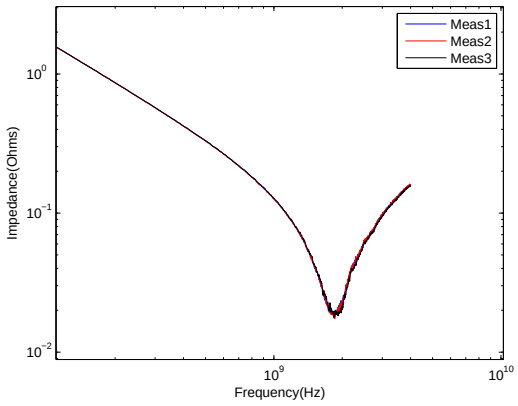


Figure 41: Comparison of three different measurement results on the same capacitor .

in one measurement cycle. The functions of the ports are reversed in the next measurement cycle of the VNA. $S21$ is the insertion loss measured across the device at each frequency point. By calculating the real and imaginary parts of the device the Using equation 41, impedance profile over the measured frequency band can be obtained. The robustness and repeatability of this measurement technique was done by carrying out a number of measurements on the same test capacitor. The square test capacitor was fabricated at the PRC using the hydrothermal process and the dimensions of the capacitor were 0.75 mm $\times$ 0.75 mm. The results are shown in Fig. 41 for three different measurements done with different calibrations. The repeatability of the technique is apparent from the results in the figure. The capacitance, inductance, and resistance were extracted from the measurements and are plotted in Fig's 43, 43,

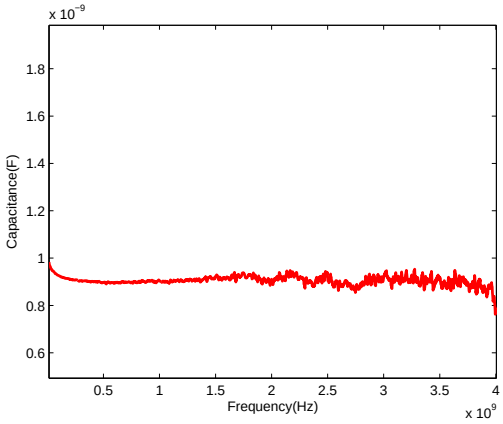


Figure 42: Capacitance extracted from the measurements.

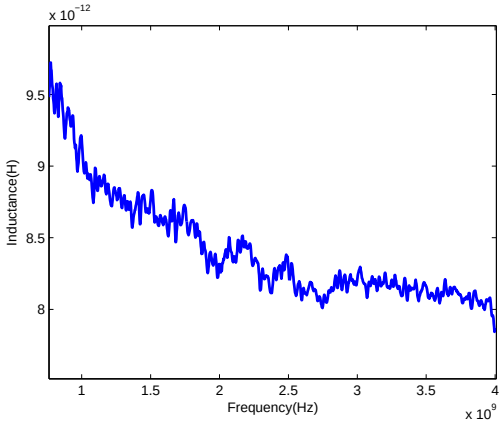


Figure 43: Capacitance extracted from the measurements.

and 44 respectively. The capacitance of the DUT varies from 1 nF at 10 MHz to 0.9 nF at 4 GHz, a 10% variation over the measured frequency band. The capacitance is extracted by applying a correction factor for the inductance as shown in the following equation:

$$C(f) = -\frac{1}{(2\pi f)(ImZ(DUT) - 2\pi f L_{SRF})} \tag{56}$$

Where L_{SRF} is the inductance estimated from measurements. Below the resonant frequency of the structure the impedance is dominated by the capacitance of the DUT. A slight variation of the inductance with frequency does not affect the extracted value of the capacitance. Above the series resonant frequency, the inductance of the DUT dominates the impedance profile as can be seen in Fig. 41. The variation of the

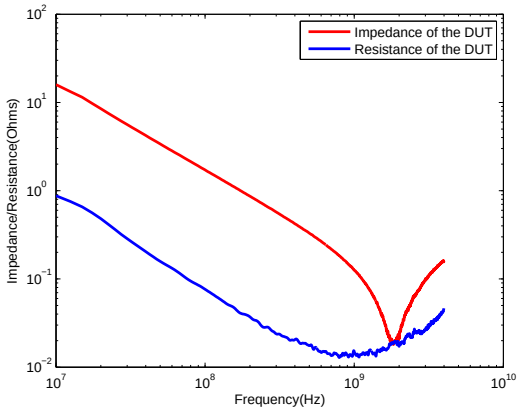


Figure 44: Resistance extracted from the measurements.

inductance with frequency is extracted using the formula:

$$L(f) = \frac{ImZ_{DUT} + \frac{1}{2\pi f C_{SRF}}}{2\pi f} \tag{57}$$

Where C_{SRF} is the extracted value of capacitance at the resonant frequency. The resistance of the DUT is directly extracted from the real part of the measured impedance.

$$R(f) = Re(Z_{DUT}) \tag{58}$$

From Fig. 44, it is observed that at lower frequencies the parallel loss R_p and at frequencies close to and above the series resonant frequency, the series loss R_s of the DUT dominates the resistance. Since the measurements were done after calibration and there were no fixtures involved, the capacitance, inductance, and resistance could directly be extracted from the measured values. De-embedding would be required if fixtures were used to connect to the DUT.

Similarly, Fig. 46 shows the impedance profile of different capacitors of DuPont's materials that were measured using the two port methodology. Fig. 47 shows the extracted dielectric constant value, it remains relatively constant as observed from the figure. The extracted parameters from the measured capacitor shown in Fig. 46 are plotted in table 5

Table 5: Extracted capacitor values from measurements in Fig .47

Capacitor type	Capacitance(nF)	Series Inductance (pH)	Equivalent series resistance (mohms)
1.198mm square capacitor	2.84	42.6	16
2.1mm square capacitor	8.772	23.8	10.26
5mm square capacitor	53.93	22.1	7.22
10mm square capacitor	191	24.1	5

All the measurements shown in this chapter were self impedance measurements. Transfer impedance measurements were done on planar capacitors and the results of these measurements are shown in chapter 5 of the thesis.

3.3 Modeling of the capacitor structures

The capacitors were modeled using the transmission matrix method (TMM) [31]. This tool has been previously used to model power plane structures [57],[58]. 3D full wave EM simulators are generally accurate tools available to obtain the frequency response [59],[60],[61]. However, the rationale of using TMM was that it was an in-house easy to use tool that was developed and well calibrated with measurements.

In the transmission matrix method the power plane is divided into unit cells as shown in Fig. 45 and represented using a lumped element model for each cell [31]. Each unit cell consists of an equivalent circuit with R, L, C and G components which are calculated from the physical structure of the unit cell as shown in Fig. 45. The lumped elements are cascaded together in a Π or T network and each network gives the same result as discussed in [31]. The equivalent circuit parameters for a unit cell can be derived from quasi-static models, provided the dielectric separation d is much less than the metal dimensions (a,b), which is true for power/ground plane pairs [55]. From the lateral dimensions of a unit cell (w), separation between the planes (d), dielectric constant (ϵ), loss tangent of the dielectric ($tan\delta$), metal thickness (t) and metal conductivity (σ_c), the equivalent circuit parameters of a unit cell

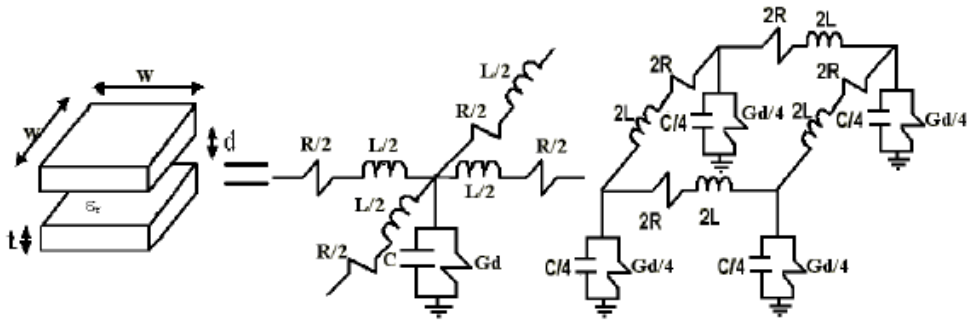


Figure 45: Unit cell and equivalent circuit (T and Π models).

can be computed as follows:

$$C = \frac{\epsilon_o \epsilon_r w^2}{d} \tag{59}$$

$$L = \mu_o d \tag{60}$$

$$G_d = \omega C tan\delta \tag{61}$$

$$R_{DC} = \frac{2}{\sigma_c t} \tag{62}$$

$$R_{AC} = 2\sqrt{\frac{\pi f \mu_o (1+j)}{\sigma_c}} \tag{63}$$

Equations 59, 60, and 61 have been previously introduced in chapter 1 of this thesis. In the above equations ϵ_o is the permittivity of free space, μ_o is the permeability of free space and ϵ_r is the relative permittivity of the dielectric. The parameter R_{DC} is the resistance of both the power and ground planes for a steady DC current, where the planes are assumed to be of uniform cross section. The AC resistance R_{AC} accounts for the skin effect on both conductors. The shunt conductance G_d represents the dielectric loss in the material between the planes. In modeling the capacitive structures the fringing effects have been ignored because of the large aspect ratio of these structures.

The measurement and modeling results of a 2.1 mm diameter circular and a 1 mm a side square barium titanate capacitor are shown in Fig. 48. The modeled result of a Dupont capacitor of size 2 mm $\times$ 2 mm is shown in Fig .49. Ports were appropriately

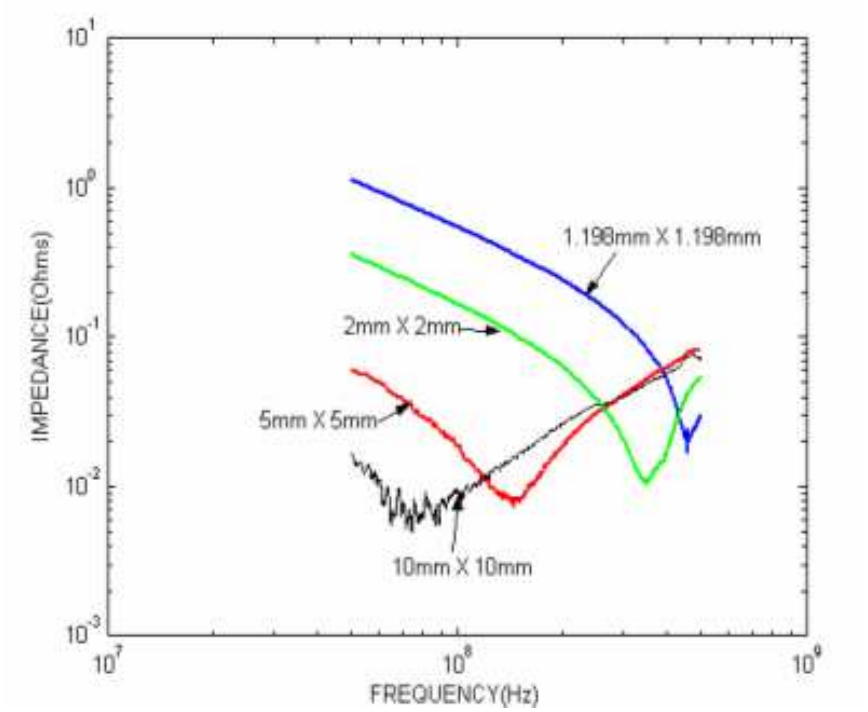


Figure 46: The impedance profiles of different sized capacitors.

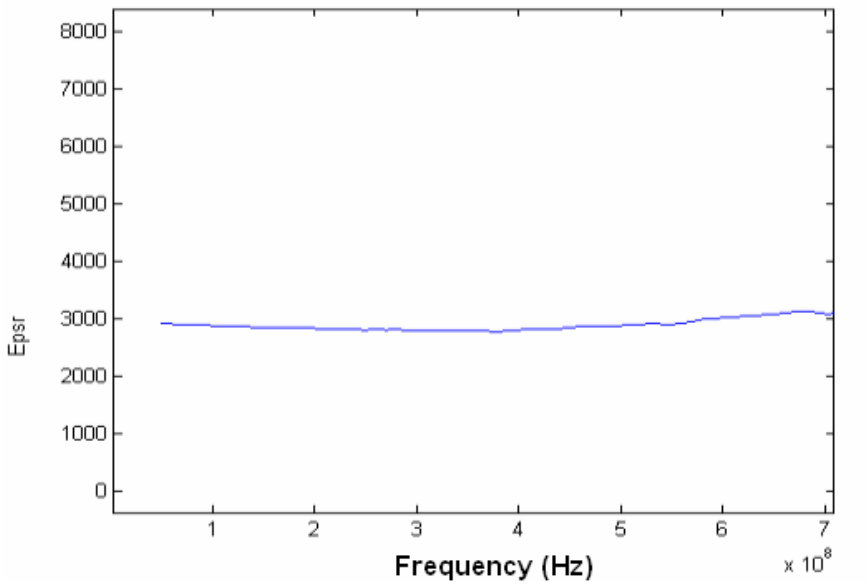


Figure 47: The variation of dielectric constant with frequency.

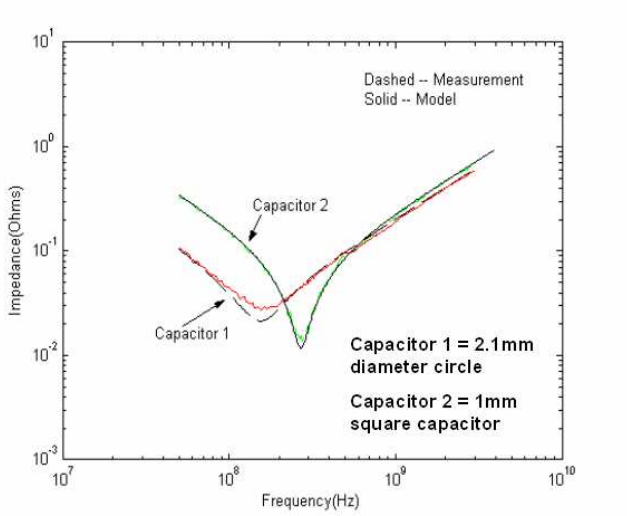


Figure 48: Measured and modeled impedance profiles of $BaTiO_3$ capacitors.

defined in the model to get the correct model to hardware correlation. The definition of the ports corresponded to the exact coordinates of the probes on the measurement structure. The parasitic inductance of the probe set up had to be included in the model to get a good correlation between the model and measurement. The details of the parasitic inductance extraction and model to hardware correlation are also given in [62].

The hydrothermal capacitor measurement results of a 1 mm $\times$ 1 mm and 2.1 mm diameter capacitor using the method described above are shown in Fig. 50 and Fig. 55 respectively. The measurements were done by placing 500 um pitch GS and SG probes 75 um apart from each other. The initial modeling result of the 1 mm capacitor is shown in Fig. 51. The structure resonates at 1.23 GHz. The capacitance of the structure is 9 nF. The equivalent series inductance (ESL) and series resistance (ESR) of the capacitor according to the modeling is 1.85 pH and 16.9 mohms respectively. As can be seen by comparing the initial model to the measurement, there is a large discrepancy in the results. In order to match the measurement results, the inductance associated due to the probes was extracted from the measurement set up. This was done by placing both the probes on the ground electrode exactly the same distance

Table 6: Extracted capacitor values from measurements

Capacitor type	Capacitance(nF)	Series Inductance (pH)	Equivalent series resistance (mohms)	Resonant Frequency (MHz)
1mm square capacitor	9	38	16.9	272.14
2.1mm diameter circle	27.9	35	20	161.05

apart as they were on the device under test. The extracted inductance between the probes is shown in Fig. 52. The model was compensated for by defining two ports 75 um apart and including the extracted inductance of 37.5 pH to the impedance between the ports. The correlation of the hardware to the new model is shown in Fig. 53. The capacitance of the structure was extracted and is plotted in Fig .54. The measurement and modeling result of a 2.1 mm diameter circular capacitor is shown in Fig .55 and Fig .56 respectively. The capacitance of the structure is 27.9 nF and the ESR is approximately 20 mΩ. In order to match the model to the hardware, the inductance associated with the probes was extracted as done earlier. The spacing between the probes was also 75 um in this case. The extracted inductance is shown in Fig .57, this inductance value was included in the model and the correlation between the updated model and measurement is shown in Fig .58. The capacitance of the structure was extracted and is plotted in Fig .59. Fig .60 shows the comparison between the measured values of different sized capacitors. The dimensions of the structures are 0.9 mm square, 1 mm square, and a 2.1 mm diameter circular capacitor. The measurement results show that the impedance responses of the capacitive structures are extremely sensitive to the probe inductances.

The extracted results of the 1mm $\times$ 1mm square and 2.1mm diameter hydrothermal (thin film) capacitor is summarized in table 6.

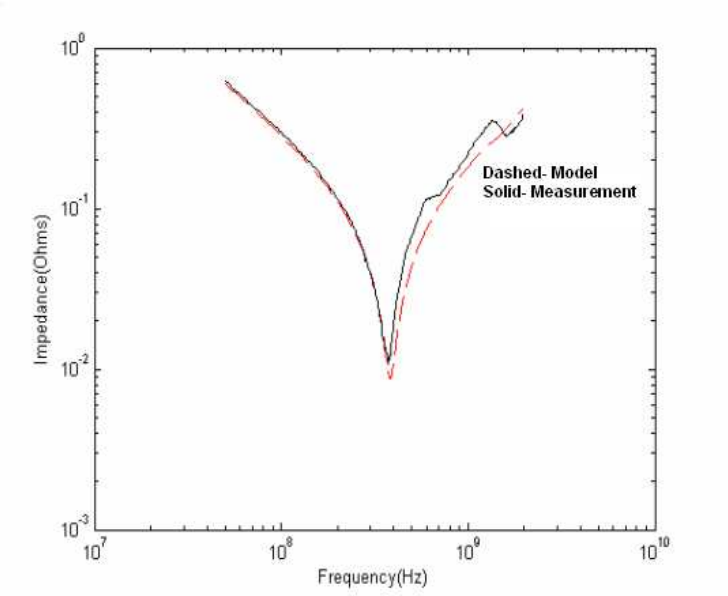


Figure 49: Model to hardware correlation of a 2 mm × 2 mm Dupont capacitor.

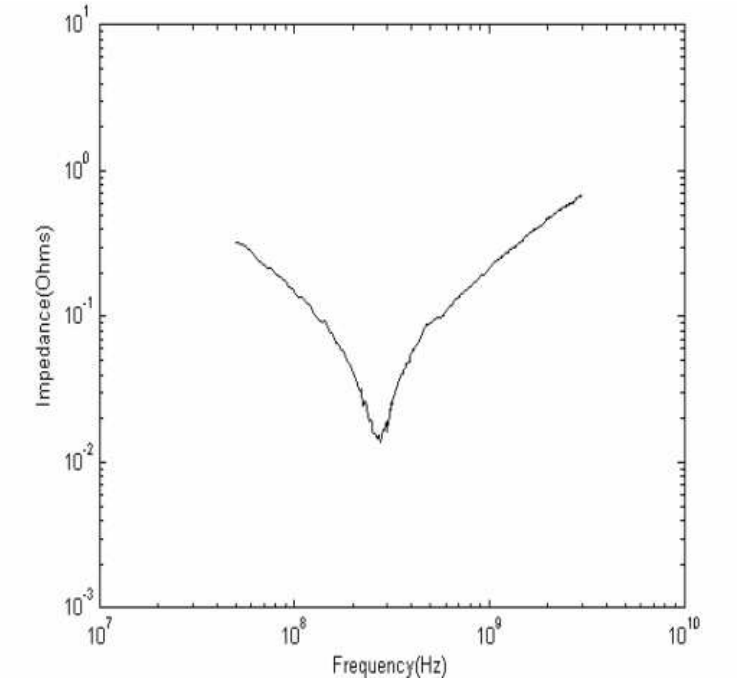


Figure 50: Measured frequency response of a 1 mm × 1 mm hydrothermal capacitor.

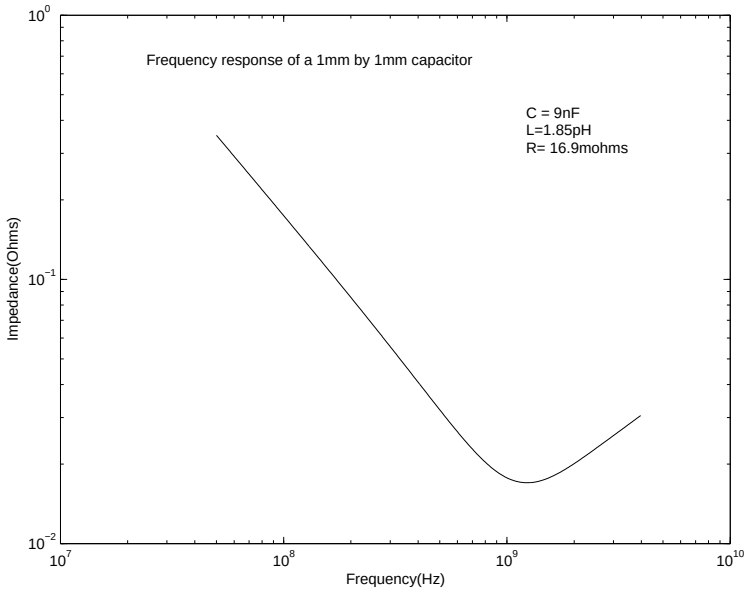


Figure 51: Modeled frequency response of a 1 mm × 1 mm hydrothermal capacitor.

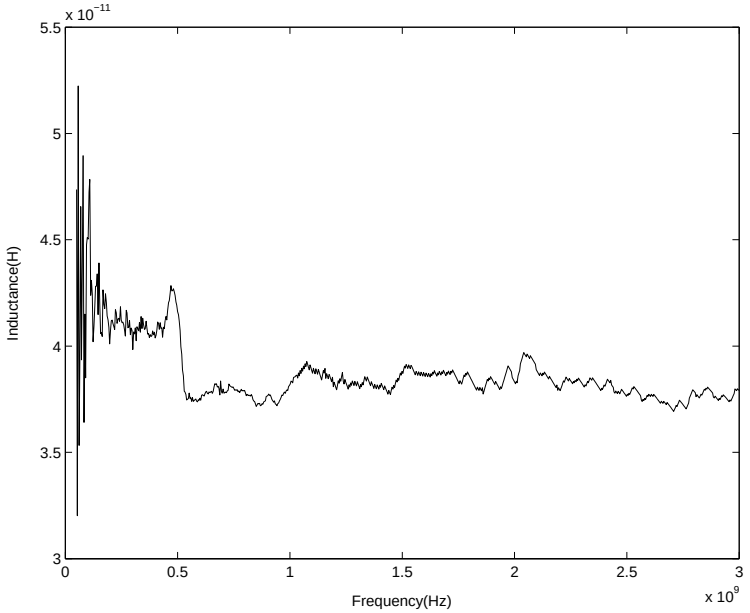


Figure 52: Extracted inductance of the probes placed 75 um apart

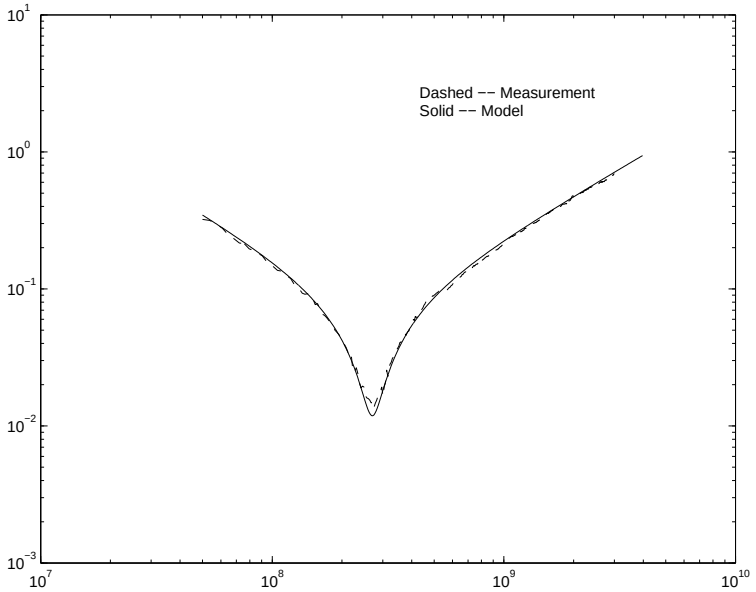


Figure 53: Model to hardware correlation of a 1 mm × 1 mm hydrothermal capacitor with probe compensation inductance.

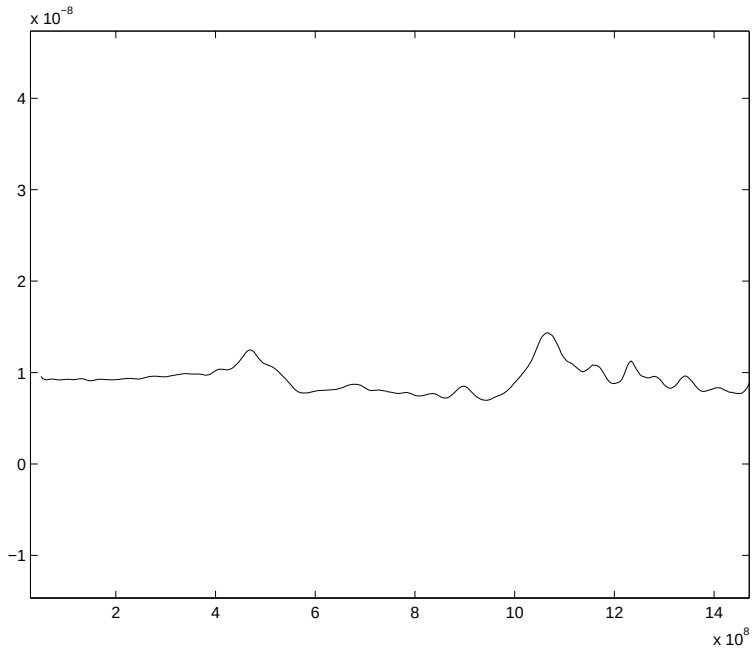


Figure 54: Extracted capacitance of a 1 mm × 1 mm capacitor.

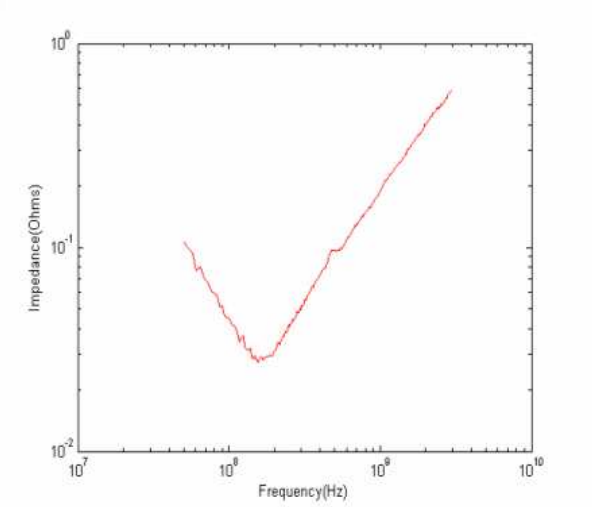


Figure 55: Measurement of a 2.1 mm diameter capacitor.

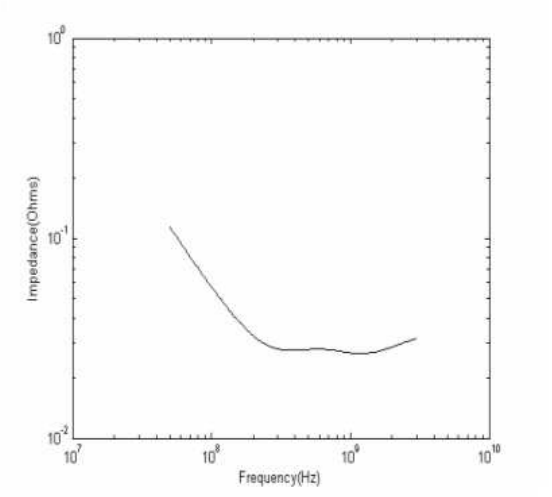


Figure 56: Model of a 2.1 mm diameter capacitor.

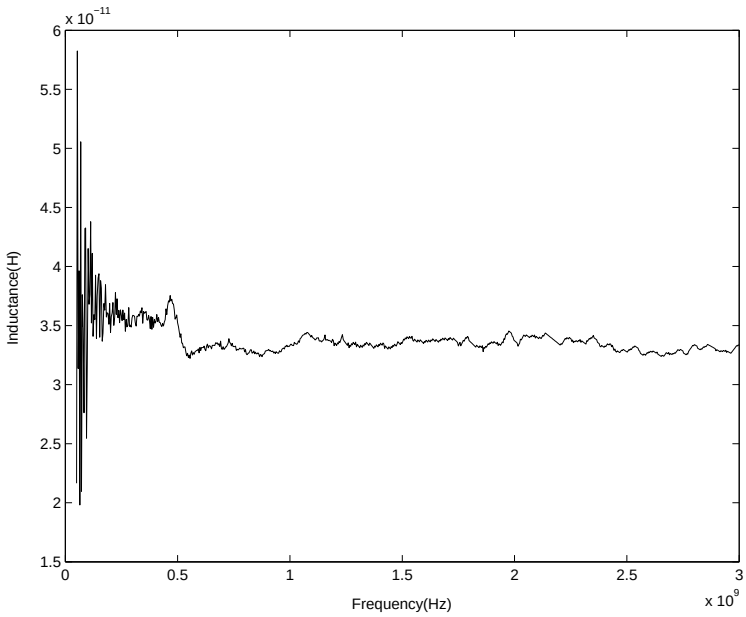


Figure 57: Extracted inductance of the probes placed 75 um apart.

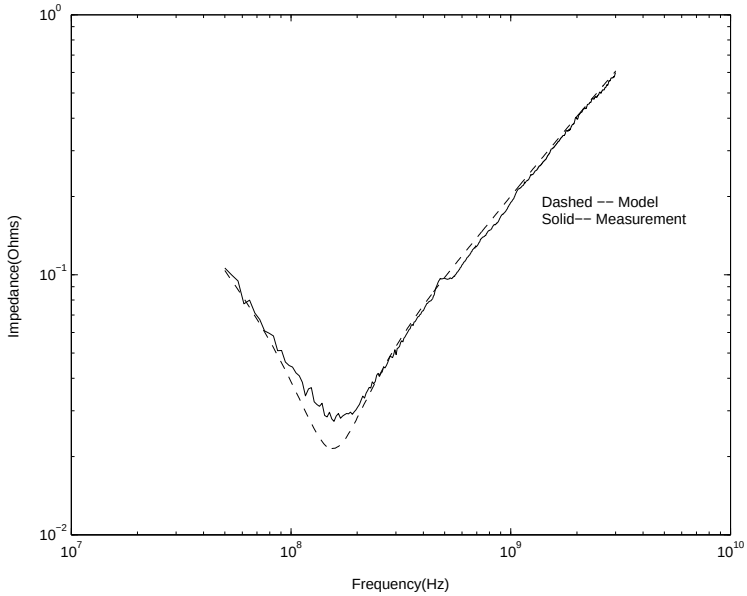


Figure 58: Model to hardware correlation with probe compensation inductance.

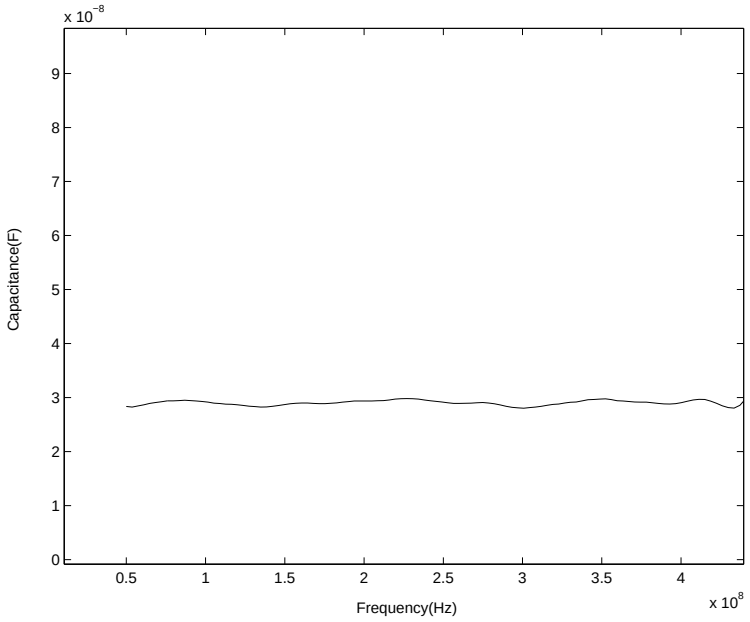


Figure 59: Extracted capacitance of the 2.1 mm diameter capacitor.

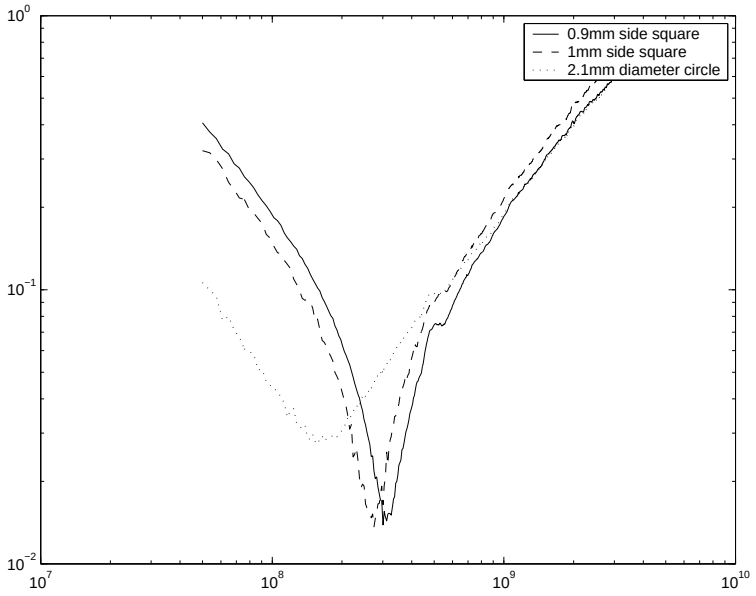


Figure 60: Comparison of measured hydrothermal capacitors of different sizes.

3.4 Summary

The measurement and modeling methodology used to characterize parallel plate structures was presented in this chapter. The measurement methodology included self and transfer impedance measurements. Equations were derived for both cases that accounted for the error introduced because of any discontinuities in the measurement set up and quantified the error terms. It was concluded that for low impedance structures the error introduced by any discontinuity could be neglected if the two port measurement methodology was used. The frequency dependent capacitance, inductance, and resistance were extracted from the measurements. Models were developed for these capacitors using the transmission matrix method. Model to measurement correlation was shown for different capacitors by accounting for the parasitic inductances introduced by the probes.

CHAPTER IV

INTEGRATION OF EMBEDDED CAPACITOR ARRAYS IN PACKAGES

The previous chapter dealt with the measurement, characterization, and design of the thin/thick film capacitors. As highlighted in chapter 1, the advantage of using these capacitors is that they can be used to decouple cost performance processors at frequency bands where SMDs and on-chip capacitors are not viable solutions. The proof of concept of using embedded capacitors to target frequency bands above 100 MHz has been previously highlighted in chapter 1. This chapter details the actual design of embedded capacitor arrays with DuPont and PRC ground rules that are designed to target the mid-band frequency range.

This chapter is organized as follows: 1) The design of a capacitive array to decouple the mid-band frequency range using individual thin/thick film embedded capacitors in the package will be presented. 2) The performance investigation of a capacitor array designed to decouple processors based on the ITRS numbers is presented. The performance parameters are the time and frequency domain responses with and without the embedded capacitors. 3) The frequency domain performance investigation of an IBM package using these capacitors is also presented. 4) The performance investigation of a capacitor array using PRC processes designed to decouple processors based on the ITRS numbers is presented. 5) The performance dependence of embedded capacitors is sensitive to their position within a package. Therefore, an analysis into the performance variation with position is done in this chapter. 6) An analysis into the SMD savings that can be achieved by using embedded capacitors in the PDN is done.

The concept of individual thin/thick film embedded capacitor arrays in the package was presented in chapter 3. The capacitor array is designed to meet a certain target impedance over a frequency band above 100 MHz. The number of capacitors required of each type is given by equation 64 and has been rewritten here.

$$Numberofcapacitors = \frac{Z_{target}}{ESR_{cap}} \tag{64}$$

As mentioned in chapter 3, the embedded capacitors should be placed directly under the die shadow and the vias connecting the capacitors to the processor should connect to the solder bumps of the processor. The frequency band over which decoupling can be provided depends on the capacitor technology and ground rules, however the rules used in the design of the array is transparent over any technology. The DuPont and PRC technologies introduced in chapter 3 are used in this section to design capacitor arrays to decouple frequencies above 100 MHz.

4.1 Design of a capacitive array using Dupont materials and process ground rules for a 65 nm ITRS cost performance processor.

The previous chapter dealt with the modeling, measurement, and characterization of embedded capacitors. The use of these capacitors in decoupling cost performance type applications in the mid-band frequency will be described here. As mentioned before, the mid-band frequency is defined as the frequency range between 100 MHz to 2 GHz. Therefore, the package structures that were modeled for each technology will be described in detail here.

The cross section of the proposed package is shown in Fig. 61. The package consists of a core of thickness 0.6 mm shown in Fig. 62. The core is split into seven constituents as shown in Fig. 62. The total thickness of the structure excluding the metal levels in this case is 600 um.

The build up layers are added to the core in Fig. 62 to obtain the complete package

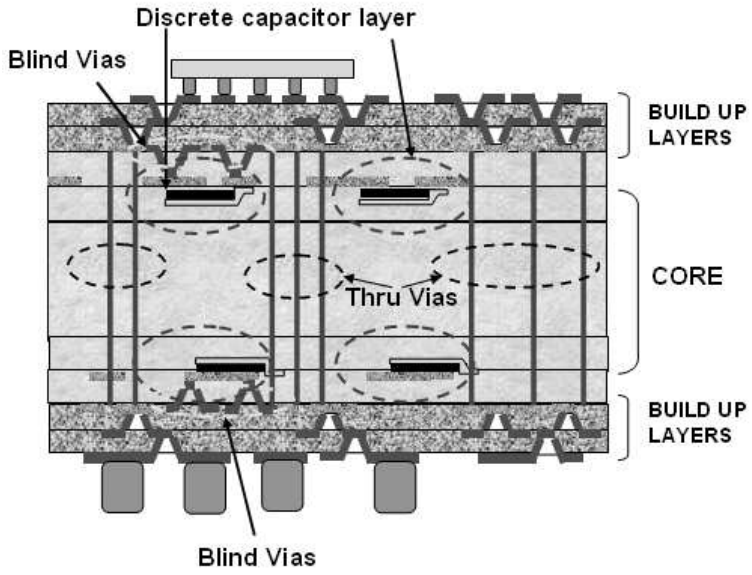


Figure 61: Cross section of the proposed package with individual embedded capacitors.

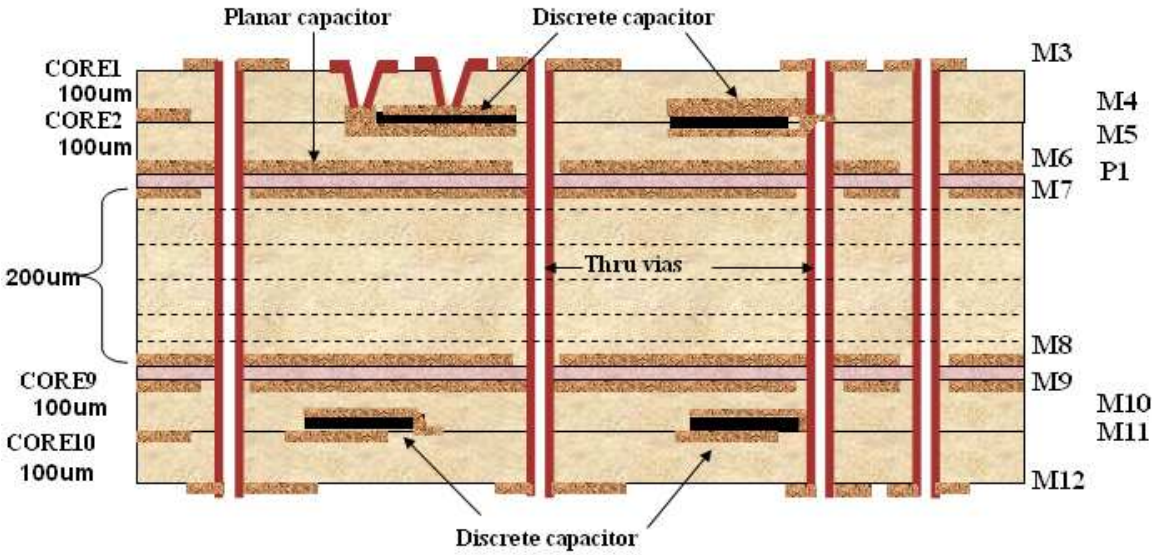


Figure 62: Cross section of the core stack up with planar and individual capacitors.

stack up in Fig. 61. The thickness of each build up layer is 38 um. The total thickness of the stack-up including the top and bottom metal thickness of 35 um each is 822 um. The processor and the PWB solder bumps thickness was neglected in calculating the thickness of the package.

There are 14 metal layers in the package and the power and ground rails at the top and bottom of the package are connected to each other using thru and blind vias. The thru vias run through the core and are 0.6 mm in length. The diameter of the thru vias is 200 um and their edge to edge separation is 200 um. A thru hole via pair was modeled in Fast Henry to extract the inductance, the value extracted was 280 pH for a single pair. The length of the blind vias is dependent on the placement of the individual capacitor in the package. The blind vias have a diameter of 100 um and are spaced 300 um apart and the length of the blind vias can vary from 36 um to 171 um. The associated inductance of the blind vias correspondingly varies from 6 pH to 70.6 pH respectively.

To meet the target impedance between 100 MHz and 2 GHz, a package capacitive network was designed with the individual thick film capacitor material from DuPont. The capacitor performance is sensitive to position as highlighted in section 1.6. An important requirement of the design of such an array is to place these capacitors as close to the switching circuits as possible. The capacitive network was designed with all the individual capacitors placed directly under or around the die shadow in the two layers allocated to them in the package. The size of the die was taken as 11.8 mm $\times$ 11.8 mm from [2] for a cost performance processor for the 65 nm node. The placement of the capacitors under the die shadow was done to reduce the effect of the spreading inductance of plane pairs of the package as previously highlighted in Fig. 17. The network consists of 18 caps of 1 mm and 18 caps of 0.75 mm in each individual capacitor layer giving a total of 72 capacitors in the capacitive array. The individual capacitors in the lower layer of the package were connected to the power

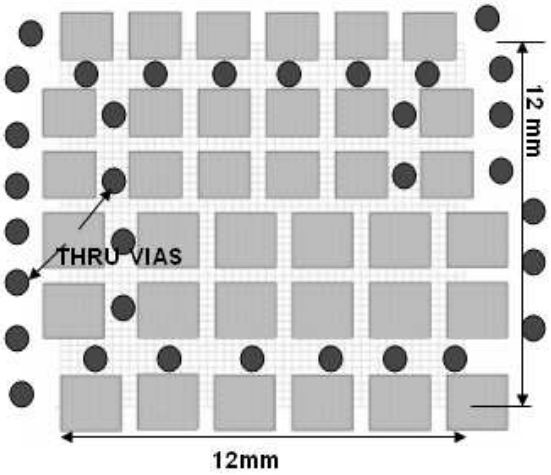


Figure 63: Layout of a individual capacitor layer in the package.

and ground bumps of the processor via blind and thru vias as mentioned earlier in this section. The layout of one of the layers of individual embedded capacitors is shown in Fig. 63. The network is designed such that majority of the vias from the capacitors connect directly to the flip chip solder bumps of the processor. The design ground rules prevent thru vias to be spread uniformly across the die shadow as seen by the non-uniformity of the position of the thru vias in Fig. 63. Process ground rules specific to DuPont capacitor materials were used to design the embedded capacitor layout. A ground rules that were used will be briefly mentioned in this part of the section. Fig. 64 captures a few of the design ground rules for the capacitor network layout. The minimum and maximum size of the electrodes as mentioned before are 0.5 mm and 3 mm a side respectively. The size of a dielectric is 0.625 mm larger than the size of the electrode on each side, therefore the area occupied by the structure is larger than that occupied by the effective capacitor. If there are no thru holes between a capacitor, the distance between dielectrics is 0.625 mm. The spacing between the dielectrics with thru holes between them is 1.05 mm. The process ground rules are listed in table 7. The embedded capacitor network was designed to target the frequency band between 100 MHz and 2 GHz as shown in Fig. 65. To provide decoupling from DC to multiples of chip operating frequencies VRMs, SMDs, and on-chip capacitance would

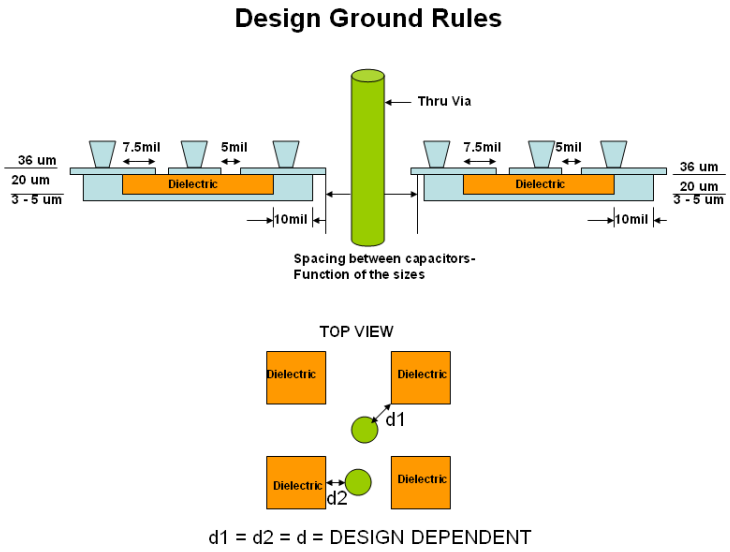


Figure 64: The design ground rules for the capacitor network in the package.

Table 7: DuPont process ground rules

Parameters	Value
Maximum size of a capacitor electrode	120 mils
Minimum size of a capacitor electrode	20 mils
Dielectric constant	3000
Loss tangent	0.05 @ 1 MHz
Thickness of top and bottom electrode	$3-5$ um (0.12-0.3) mils
Spacing between two capacitors	Function of their sizes
The minimum thru via diameter	15 mils
Via clearance diameter	Via diameter + 15 mils
The spacing between the vias	30 mils
Dielectric size	Electrode size + 20 mils (10 mils / side)
Dielectric thickness	20 ± 3 microns fired

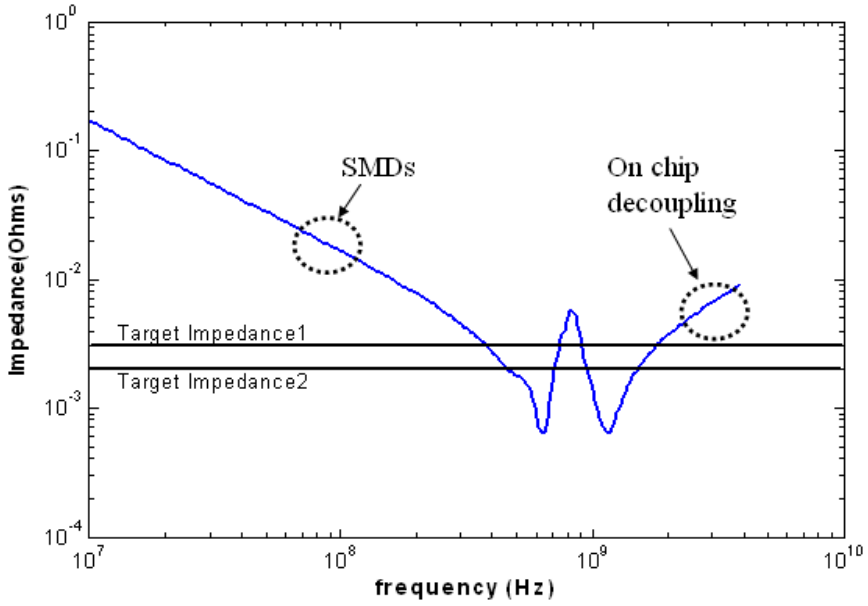


Figure 65: Impedance profile with package capacitors.

also be required. SMDs and on-chip capacitance were used below 100 MHz and above 2 GHz respectively to get the complete frequency response shown in Fig. 66. The figure shows the frequency band over which each decoupling component is effective. VRMs are effective to the lower kHz's region, SMDs provide decoupling from the kHz region till around 100 MHz and on-chip capacitance is used above 2 GHz. It is evident that a target impedance in the order of one mΩ can be met over a broad frequency range from DC to multiples of the chip operating frequencies using the combination of different decoupling components. The perspective view of the array of capacitors under the die shadow in the package is shown in Fig. 67.

4.2 Performance investigation for a 40W chip

The previous section shows the impedance profile obtained by using a combination of board, package and on-chip decoupling components designed to meet the 2007 cost performance processor target impedance value as given in [2]. Decoupling a high power chip with a target impedance of 0.78 mΩ using the present technology is limited to

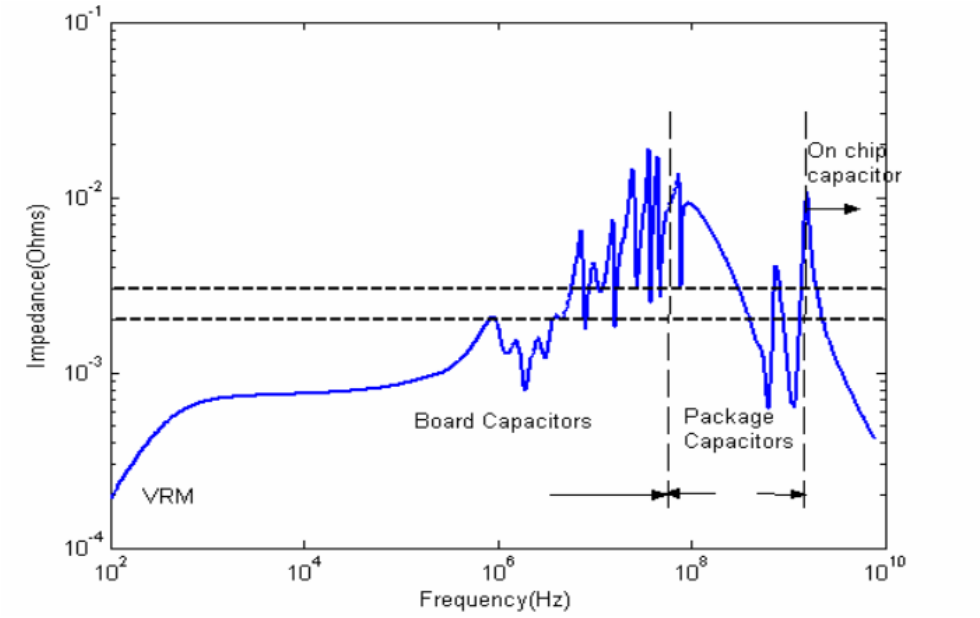


Figure 66: Impedance profile with the VRM,SMDs,package and chip capacitors.

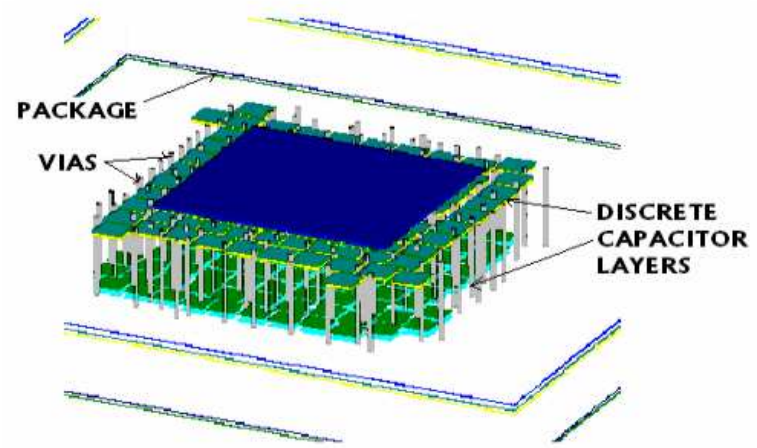


Figure 67: Perspective view of the embedded capacitors in the package.

a very narrow frequency band at 600 MHz and 1 GHz. Therefore, this section looks at alternatives where the capacitive network is used to decouple a lower power chip over a broader frequency range.

4.2.1 Time domain performance of the capacitive array

The time domain performance of the capacitive array targeting a lower power chip is investigated in this section. The simulations were carried out to capture the performance with a 2 GHz clock as the input to the system. The rise time and fall time of the current pulse is 50 psec respectively and the time period of the clock is 500 psec as shown in Fig. 68. The target impedance to be met decides the magnitude of the current pulse. In this simulation, a 40 W chip was considered and a core voltage of 1 V was assumed. Therefore from (2), the magnitude of the current pulse calculated assuming a core voltage of 1 V is 40 A. The target impedance from 1 is 2.5 mΩ. To get the time domain response of the system, the fourier transform of the input current pulse train is multiplied with the frequency domain data of the PDN. The inverse fourier transform of the resultant is then taken to get the time domain response. The system simulation was initially carried out with a VRM, SMDs and on-chip decoupling capacitors. 25 nF of on-chip decoupling capacitance was considered in the simulation. The time domain performance of the system is shown in Fig. 69. Switching noise of the order of 400 mV peak to peak is observed from the figure. To highlight the improvement with embedded package capacitors, the system was simulated with the VRM, SMDs, package and on-chip capacitors. The switching noise observed in this case is 80 mV peak to peak and is shown in Fig. 70. A five time improvement in the switching noise performance is clearly seen with the inclusion of embedded capacitors in the package for a 40 W chip.

From the frequency domain response of the capacitive array, it can be concluded that a 40 W chip can be decoupled in the frequency range from 350 MHz to 2 GHz.

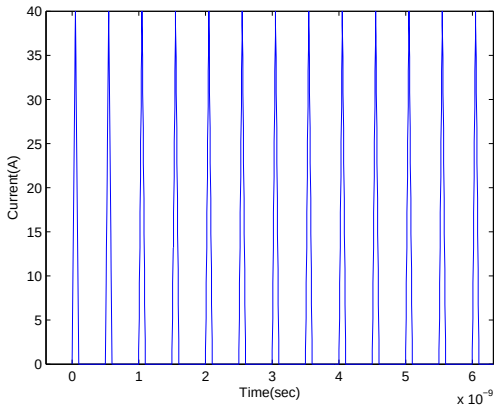


Figure 68: Input current pulse train to simulate a 2 GHz clock.

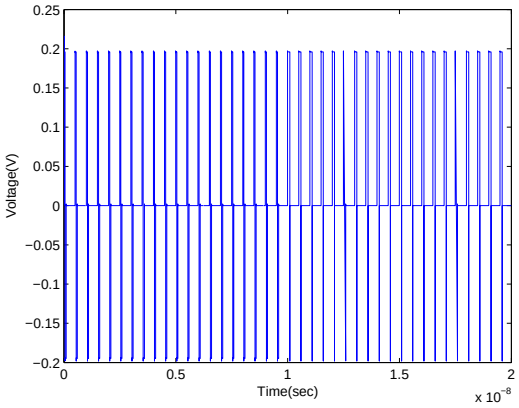


Figure 69: Switching noise with VRM, SMDs, and on-chip capacitors.

Therefore, with the conservative design ground rules used for these examples this technology is more viable for decoupling low power chips.

4.3 Investigation of the performance of an IBM package with DuPont's embedded capacitors

An analysis was carried out with an existing PDN for a high performance component. The decoupling elements included in this PDN were the VRM, SMDs on board, IDCs on the package, and on-chip decoupling. The power dissipated by the component is 40 W and the core voltage of the chip is 1.5 V. The average current drawn by the component is 26.67 A and is applied to Equation. 1. Therefore, the target impedance

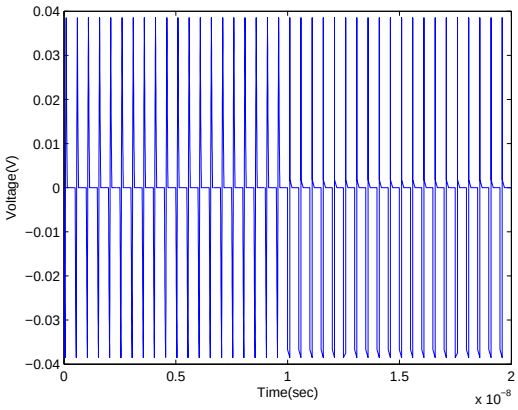


Figure 70: Switching noise with VRM, SMDs, on chip and embedded package capacitors.

that has to be met is 5.6 $m\Omega$. Fig. 71 shows the cross section of the package under consideration. It has a $4-2-4$ laminate stack up and has multiple voltage and ground planes.

The distribution of the power-ground planes is shown in Fig. 72. The layout showing the IDCs on the package and the different voltage planes for the MEM(Memory), Core and I/Os is shown Fig. 78. The frequency domain response was obtained by modeling the package with the different decoupling components using the Transmission Matrix Method [31]. Ten 1206 SMDs were connected to the printed circuit board. The value of the SMD capacitors are C = 22 uF, ESR = 8 mΩ and ESL = 1 nH. Nine IDCs were connected to the package. The value of the IDCs are C = 100 nF, ESR = 8 mΩ and ESL = 90 pH. 400 nF of on-chip decoupling was used in the analysis. Fig. 74 shows the response of the PDN with the above mentioned decoupling elements. The parasitic mounting inductance of the capacitors was included in the simulations. The target impedance of 5.6 mΩ is met over a broad range by using the above mentioned decoupling elements except for two parallel resonance peaks as observed in Fig. 74. The first parallel resonance is between the PCB SMDs and the IDC capacitors and the second resonance is due to the IDCs and on-chip capacitance. The target impedance is not met in the frequency bands from 5 MHz to 25 MHz

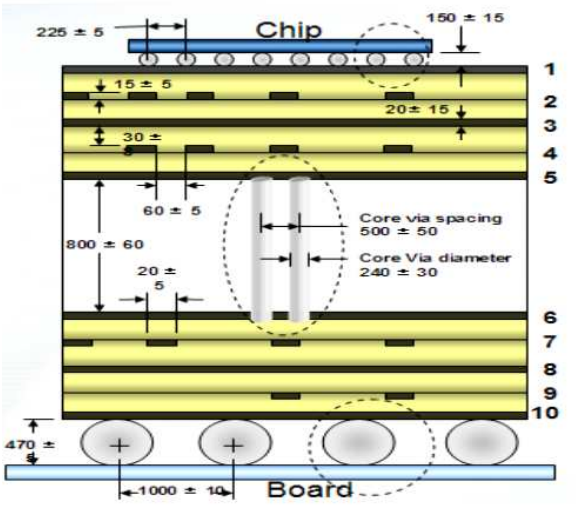


Figure 71: Cross section of the IBM package.

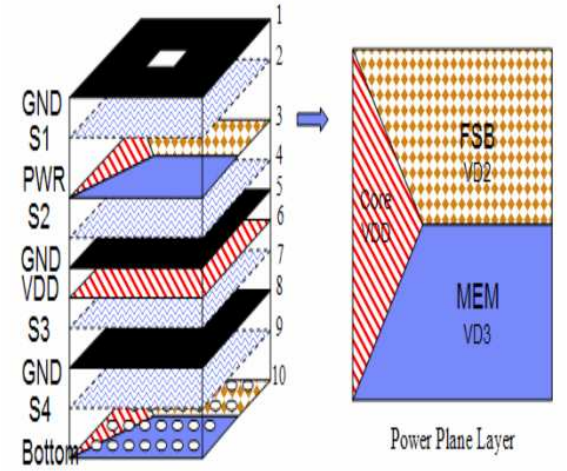


Figure 72: Power planes of the IBM package.

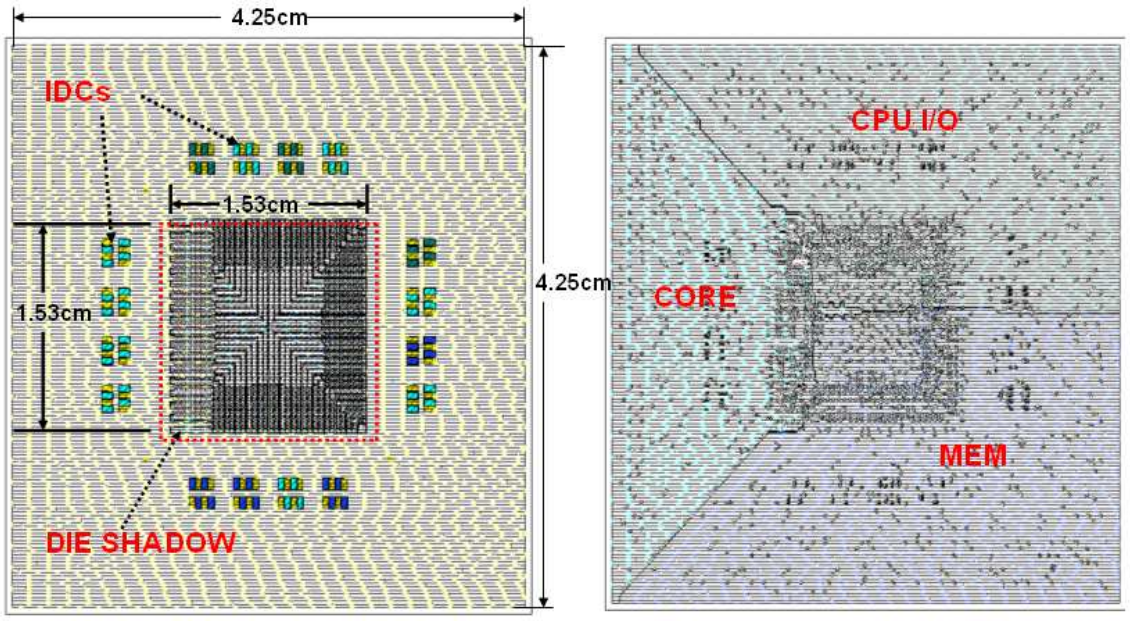


Figure 73: IBM package layout showing the IDCs and voltage planes for core,MEM, and I/O.

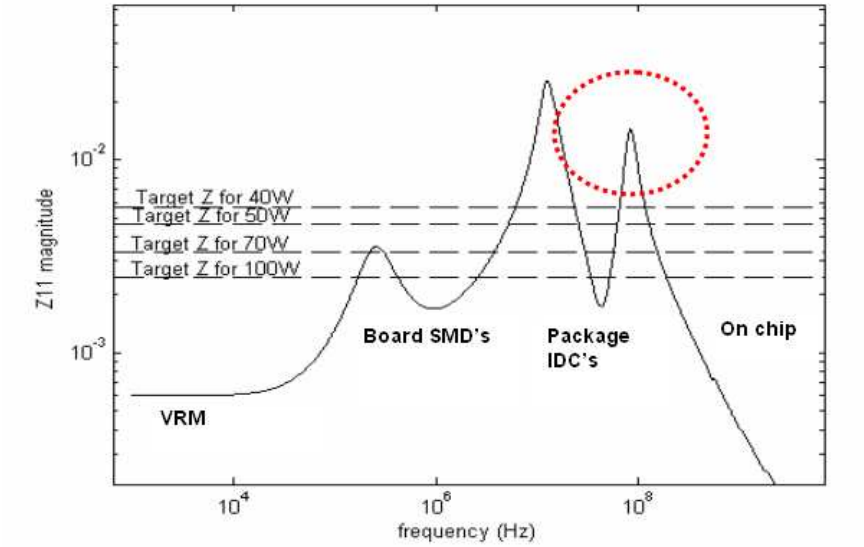


Figure 74: Impedance profile with SMDs and on-chip decoupling capacitor.

and from 60 MHz to 120 MHz respectively because of these resonances. The focus of this analysis is on the use of package embedded capacitors to target the frequency band in the range of 100 MHz and above. Therefore, the following analysis is done to target the second parallel resonance between the IDCs and on-chip capacitance. The first resonance could be reduced by proper selection of SMDs. Meeting the target impedance for higher power components would be an issue with the traditional decoupling elements. To illustrate the problem, if high density components in the order of 50 W,70 W, and 100 W were to be decoupled by the same elements then the target impedance numbers that have to be met for a core voltage of 1.5 V in each case are 4.5 mΩ, 3.2 mΩ and 2.25 mΩ respectively. These target impedances are shown in Fig. 74. It can be observed that frequency band over which the target impedance can be met with the above mentioned decoupling elements is restricted to smaller bands for higher power components. To target the frequency band from 60 MHz to 120 MHz shown in the circled area in Fig. 74, embedded package capacitors can be used. To target the desired frequency band in this case, two capacitors with 25 mm^2 area were placed in layers two and five each with different number of via connections to target different frequency bands in the 60 MHz to 120 MHz range. The loop inductance of power/ground (P/G) C4 solder ball of diameter 150 um and pitch 225 um along with a pair of P/G vias from the C4 layer to the core voltage level in layer three is computed as 43 pH using FastHenry [30]. Similarly, the loop inductance of a similar structure from the C4 layer to layer five is 70 pH. The frequency response of the PDN with the embedded capacitor in the package is shown in Fig. 75 and the impedance in the frequency band from 60 MHz to 120 MHz is met.

4.3.1 I/O Decoupling Analysis

This section focuses on the use of embedded capacitors in decoupling I/Os. Two different single ended I/O configurations are analyzed in this section. The two I/O

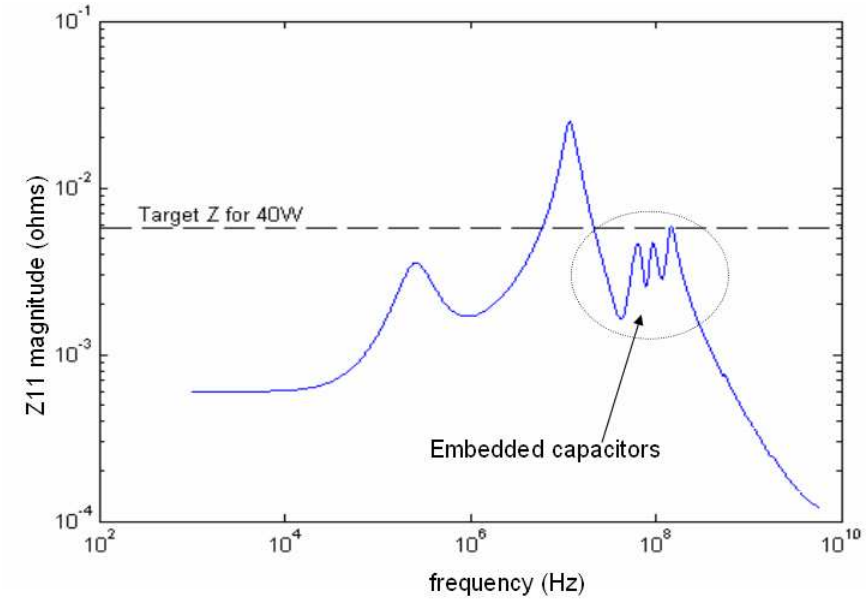


Figure 75: Impedance profile with SMDs, embedded package capacitors, and on-chip decoupling capacitor.

networks under consideration are the memory (MEM) and the CPU bus. The core voltages for the MEM and CPU bus are 1.2 V and 1.15 V respectively. The worst case currents in both cases are 3.34 A and 7 A which translates into target impedances of 35.9 mΩ and 16.42 mΩ. The decoupling components of MEM include four 100 nF IDCs on package and 54 nF of on-chip capacitance. The frequency response of the decoupling components of the IDCs and on-chip capacitance is shown in Fig. 76. A parallel resonance peak of the IDCs and the on-chip capacitance is formed at 100 MHz. A 5 mm embedded capacitor is placed in layer three in the VD3 region under the die shadow. The resulting frequency response of the IDCs, the 5 mm embedded capacitor and on-chip capacitance is shown as the dashed line in Fig. 76. The decoupling elements of the CPU bus include three IDC capacitors of 100 nF and 44 nF of on-chip capacitance. These elements need to decouple common clock interfaces running at 166 MHz, source synchronous double data rate address bus and data bus running at 333 MHz and 667 MHz respectively.

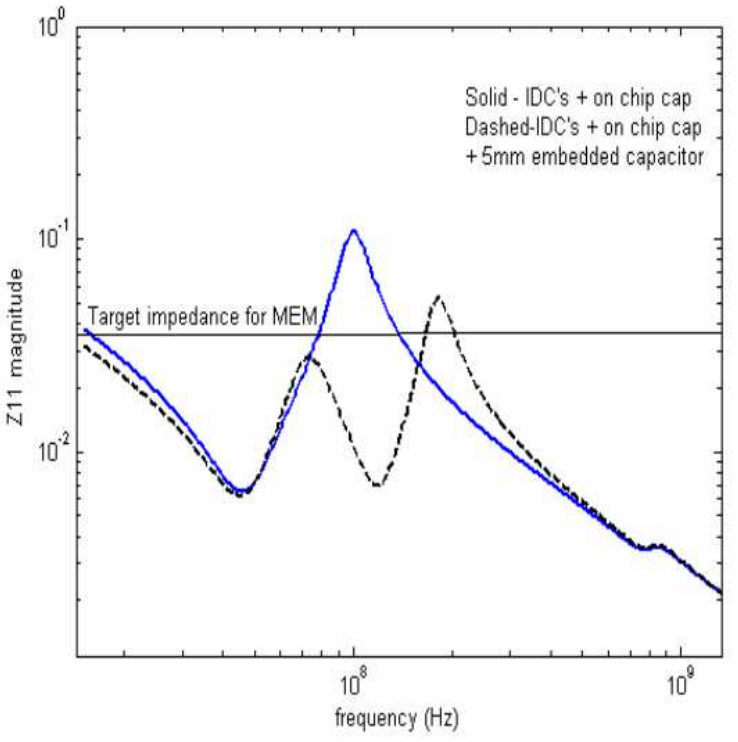


Figure 76: PDN response of MEM I/O.

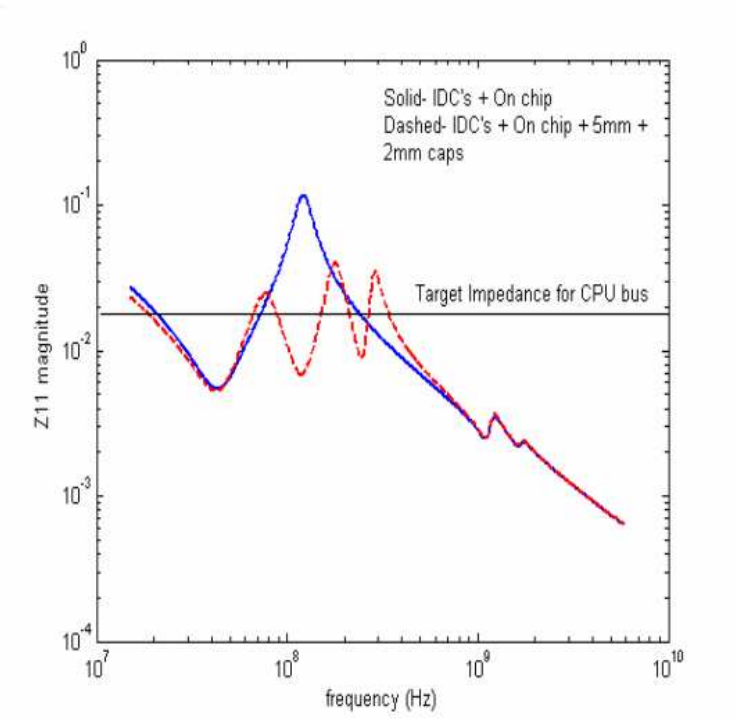


Figure 77: PDN response of CPU bus I/O.

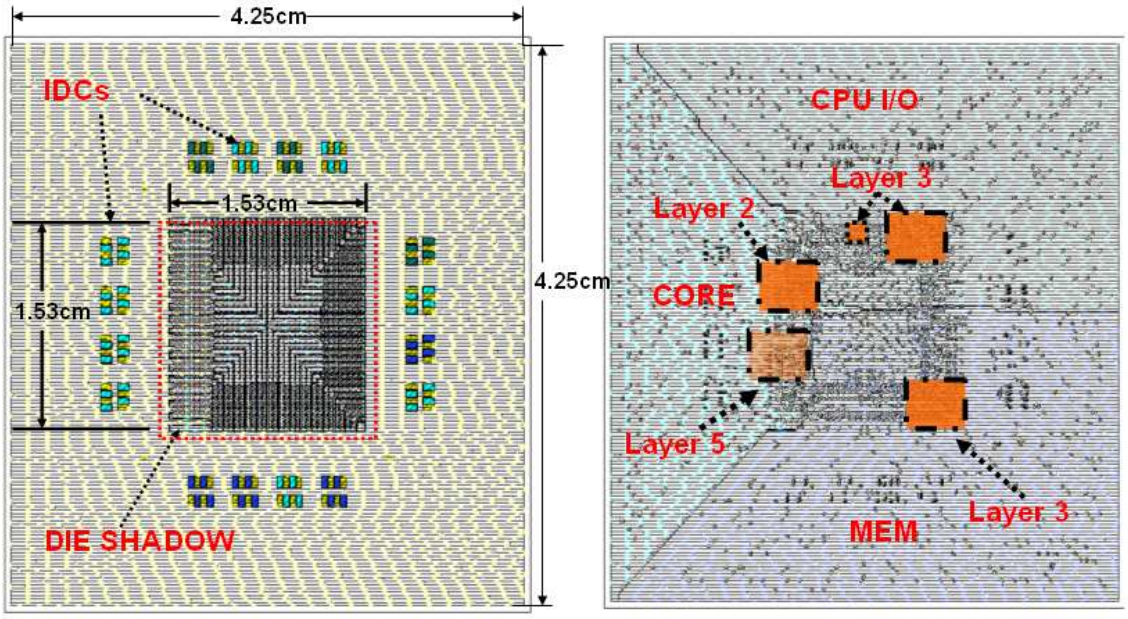


Figure 78: IBM package layout showing the IDCs, embedded capacitors, and voltage planes for core,MEM, and I/O.

Fig. 77 shows the comparison of the impedance profiles with and without embedded capacitors. One 25 mm^2 and one 4 mm^2 embedded capacitors were used to obtain the impedance profile shown with the dashed line. Both the capacitors were placed in layer three of the stack up and the separation between the capacitors is based on the material manufacturers ground rules for the embedded capacitors.

Fig. 78, shows the layout of the IBM package. All the embedded capacitors used in different layers to obtain the frequency response are shown in the figure. The embedded capacitors were placed directly under the die shadow and in their respective planes. The layout of the embedded capacitors shows that there is sufficient real estate to carry out routing of the I/O signals and that the placement of the embedded capacitors in the die shadow is not an issue.

4.3.2 On-chip capacitance for decoupling high performance components

- This section focuses on the effect of on-chip capacitance to decouple high performance components. The results of decoupling PDNs with various decoupling components have been shown in the previous sections. In this section it is shown that an increase in the amount of on-chip decoupling capacitance can replace some of the higher frequency decoupling components. In the previous analysis the amount of on-chip capacitance for decoupling the core was assumed to be 400 nF. Fig. 79 shows the analysis results for core decoupling using fixed number of SMDs and IDCs but with different values of on-chip capacitance values. It is observed that the use of higher frequency decoupling components can be reduced with an increase in the on-chip capacitance. A drawback of such an approach is that the amount of real estate and additional process steps that the on-chip capacitance requires. The trade-off of increasing the on-chip capacitance could be a decrease in the logic density or additional manufacturing technology investments. Therefore, an alternate approach could be to provide most of the high frequency decoupling from embedded package capacitors as shown in [63],[62]. The advantage would be an increase in the amount of real estate for logic on-chip and increase in the capacitance that can be provided for decoupling from the package. Resistance of on-chip decoupling capacitors is the major drawback in decoupling I/O circuits. This can be overcome by the use of less resistive package embedded capacitors. Other advantages of using package capacitors for I/O decoupling could be an increase in the real estate for circuitry on chip. The major contributors to I/O noise are the SSN that can couple from one driver to another and crosstalk between traces. A reduction in the switching noise due to the embedded capacitors can be used as an incentive to place the traces on the package closer to each other as the noise budget for cross talk is increased. This translates to reduction in the number of wiring layers and an overall reduction in the size and cost of the package [64]. It is noted that with the knowledge of the current pulse signature

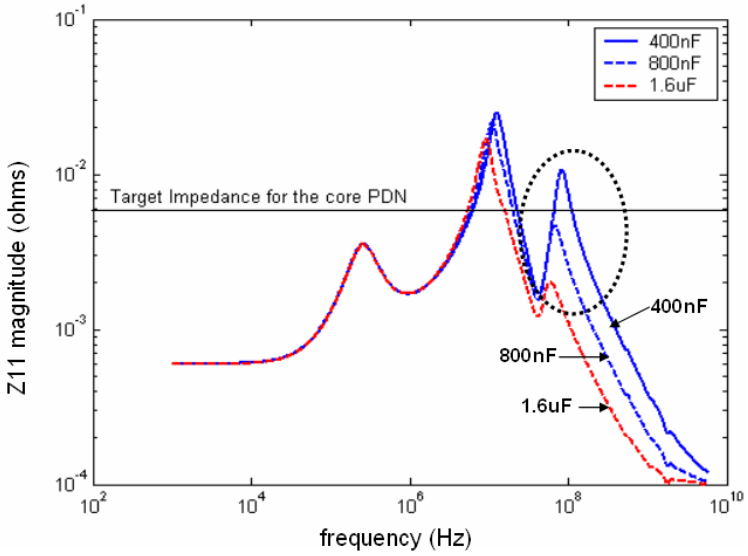


Figure 79: Frequency response of the core PDN with different values of on-chip capacitance .

of the component, time domain analysis can be done which could help in obtaining a more optimum design of the PDN as shown in [65].

4.4 Design of capacitive array for decoupling using the hydrothermal capacitor material and Packaging Research Center (PRC) process ground rules

The previous sections of this chapter highlighted the performance improvements in decoupling above 100 MHz by using the DuPont capacitors and ground rules for designing a package with these capacitors. This section investigates the performance improvements by using hydrothermal capacitors fabricated at the PRC. The package for the hydrothermal capacitors is different in structure as compared to the DuPont ground rules. The structure is shown in Fig. 80. The capacitors are placed at the two bottom most layers, the rest of the layers are built up after the capacitor layers are tested. The package dimensions are based on the packaging research center(PRC) ground rules. The ground rules that were used to propose the package are listed in table 8. The methodology used to design the capacitive array in the package

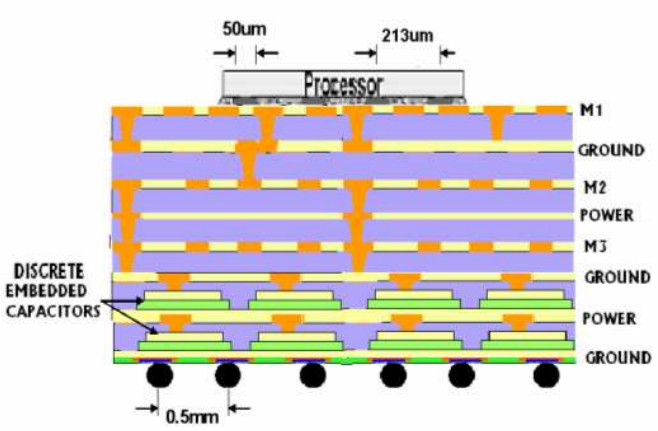


Figure 80: Stack up of the package with hydrothermal capacitors.

Table 8: Packaging Research Center(PRC) ground rules

Parameters	Value
Power ground plane dielectric thickness	9 um
Power ground plane dielectric constant	2.65
Loss tangent	0.008
Line and space	10 um
Via diameter	20 um
Via pad size	40 um
Via pitch	60 um
Capacitor minimum size	300 um side
Capacitor maximum size	3000 um side
Spacing between capacitors	100 um

is described in this section. The capacitor array was designed to meet the target impedance number of 0.7 mΩ [2] over the mid band frequency range from 100 MHz to 2 GHz. Therefore, different sized capacitors constitute this array. As mentioned before, the rationale for using various sized capacitors is that the capacitance associated with each of them is different, which translates into a different resonant frequency. To meet the target impedance, the capacitors in the package are connected together in parallel. The number of capacitors required of a particular type is given by equation 64. Where Z_{target} is the target impedance of the PDN and ESR_{cap} is the equivalent series resistance of an individual capacitor. The results in this chapter have been presented for a single reference port in the structure. The capacitor frequency response is very sensitive to its position in the package. It is important to be able to place these low ESL capacitors in the die shadow of the processor. Placement of these capacitors outside the die shadow will cause routing problems and change the predicted performance of a capacitor because of the increased spreading inductance and resistance of the planes. The port of reference (Port 1) is the chip looking into the package and the board. The board is assumed to have a single plane layer. A 0.8 mm thick, 10 cm by 10 cm FR4 board of copper thickness 30 um is assumed for the board. The board is assumed to have a single plane layer. The package is assumed to be of size 4 cm by 4 cm as shown in Fig. 80. The dielectric thickness and copper thickness of 9 um each is assumed as per PRC ground rules. The flip-chip bump inductance and ball grid array (BGA) solder ball inductance have been included in the model. The flip-chip bumps and solder balls were modeled in FastHenry. For the chip to the package interface, the flip-chip bump diameter of 50 um was assumed and a pitch of 213 um was calculated based on [2]. The inductance of a single bump pair was calculated to be 16.45 pH. In the 65 nm node, for 1024 bump pairs [2], the total effective inductance of the bumps is $1.6e^{-}14$ H. Carrying out a similar analysis for the PWB technology, the inductance of a single supply BGA ball pair was calculated

as 90.13 pH. The diameter of the BGA ball and the pitch was assumed as 500 um. For 500 such pairs [2], the effective inductance is $1.80e^{-}13$ H. Different SMT capacitors were placed on the board in the form of capacitor rings to meet the PDN target impedance for low frequency band till 100 MHz. To reduce the effect of the plane spreading inductance, the lower ESL capacitors were placed closer to the BGA balls. The embedded capacitors were placed directly under the die shadow as in the previous case with Dupont capacitors. 80 capacitors of 0.75 mm along with 80 capacitors of 1 mm a side were used to target the higher frequency part of the mid-band frequency range. 21 capacitors of 2.58 mm a side were combined with the above capacitors to get the complete embedded capacitor response. From the above figure the mid frequency band under consideration can be targeted with the two capacitor layers. In summary, 181 $BaTiO_3$ capacitors in all of sizes 0.75 mm, 1 mm, and 2.58 mm were used in the two bottom layers allocated for the capacitors. The complete frequency band using all the decoupling components is shown in Fig .81. For frequencies above 2 GHz, on-chip capacitance has been used to meet the target impedance. The improvement in the frequency response can be clearly seen by the use of package embedded capacitors. The total capacitance of the package capacitors is 2.163 uF. The area occupied by the embedded capacitors in the package is approximately the area of the processor die shadow (i.e., 140 mm^2). In comparison, the real estate occupied by the SMDs on the board is approximately 452 mm^2. To capture the SSN, a transient simulation of the system was carried out. The perspective view of the embedded capacitor layout placed directly under the die shadow of the chip in the package is shown in Fig. 82.

A 115 A current excitation pulse train of rise and fall time of 25 psec and period of 0.25 nsec was injected to the system at Port 1 to mimic a transient current by switching a 4 GHz clock.The amplitude of the current pulse was calculated based on the average current of a processor for the 65 nm node as calculated from the numbers given in [2]. The input current pulse waveform is shown in Fig. 83. The FFT of

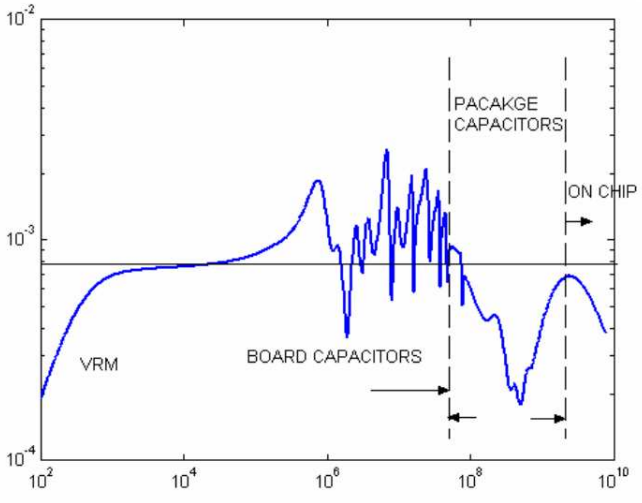


Figure 81: Complete frequency band with hydrothermal capacitors and all the decoupling components.

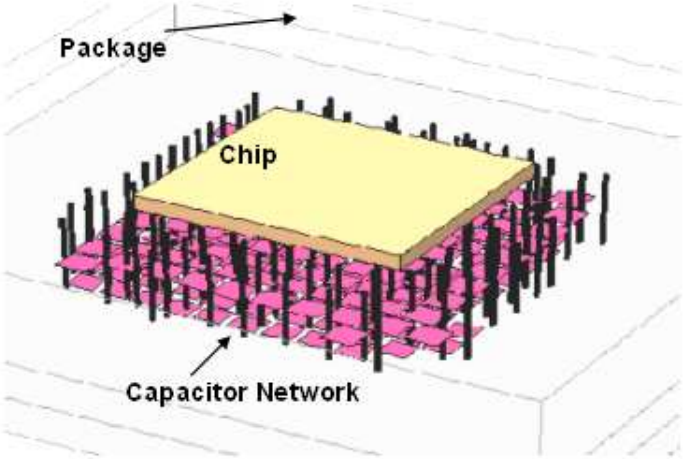


Figure 82: Perspective view of the PRC package with hydrothermal embedded capacitors.

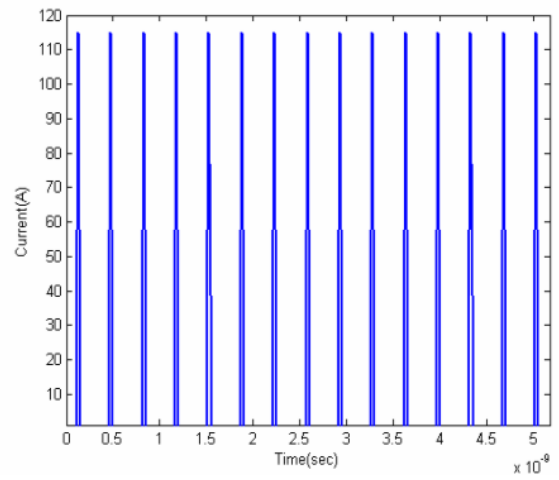


Figure 83: 4 GHz clock input current pulse to the system .

the pulse was multiplied by the frequency domain Z parameters of the system. The IFFT was taken of the resultant product to get the transient response and is shown in Fig. 84 and Fig. 85 for two cases [63]. Case 1 is the response of the system with board and on-chip decoupling capacitors and case 2 is the response with the board, package, and chip capacitors. The effect of the decoupling capacitors can be clearly seen from the system response in each case. There is a three fold improvement in the SSN, when embedded capacitors are used in the system with on-chip and SMDs. The time domain simulations clearly show the benefit of embedded capacitors in the system.

4.4.1 Process for Integration of capacitors in an organic substrate

This section explains the process used to integrate embedded capacitors in organic packages. The hydrothermal films were synthesized directly on the boards owing to the low process temperatures. Evaporated Ti on copper clad laminates was used as the Ti source. The films deposited on FR4 are shown in Fig. 86. A subsequent metal/dielectric layer with multiple via connections was built on the laminates. Further details regarding the process involved in the integration of passives in organic

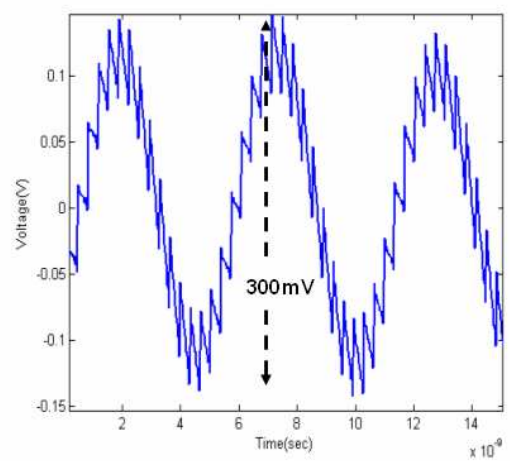


Figure 84: SSN magnitude with VRM, SMDs and on-chip capacitance.

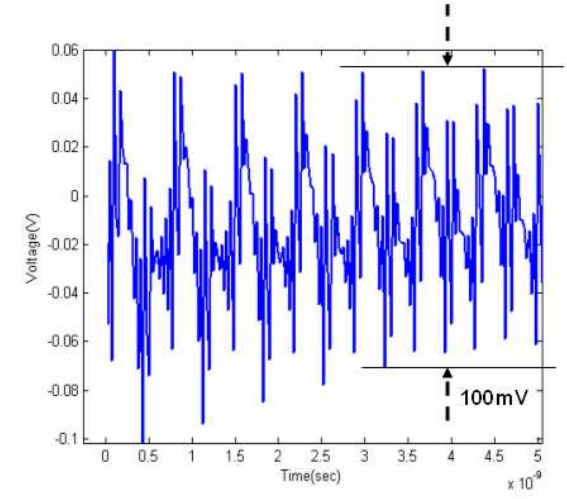


Figure 85: SSN magnitude with VRM, SMDs ,embedded capacitors and on-chip capacitance.

substrates can be found in [66] and has not been mentioned in this thesis. A picture of a combination of assembled capacitors is shown in Fig. 87.

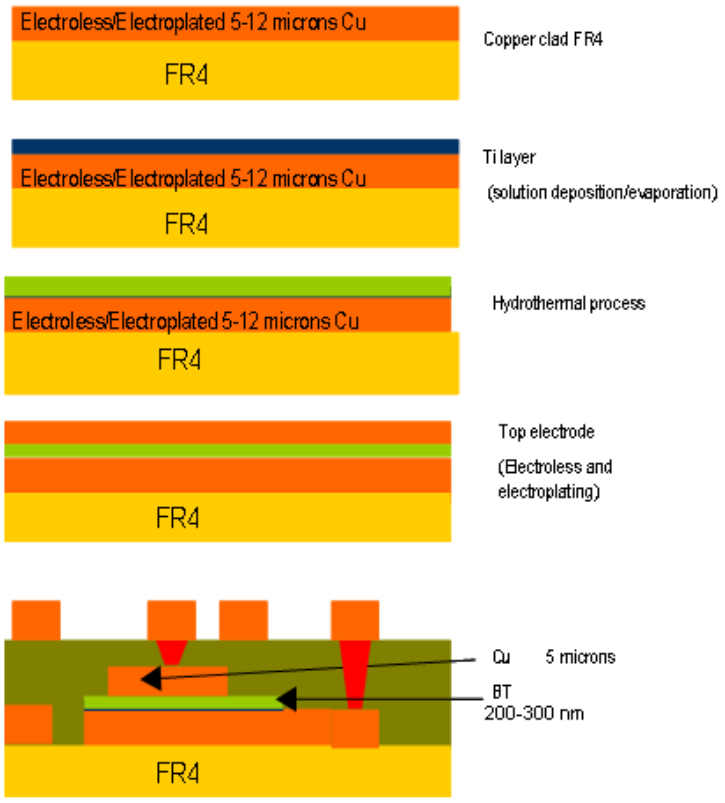


Figure 86: Integration process of hydrothermal capacitors in an organic package.

4.5 Frequency performance dependence on location

A series of simulations were carried out to highlight the performance variation of embedded capacitors with change in position within the package. The Dupont process ground rules were used to carry out the analysis. The simulations were done to highlight two important position variations. An array of four 2mm $\times$ 2mm capacitors was used to highlight the concept instead of the whole decoupling array. The parameters of a single 2mm $\times$ 2mm capacitor is as follows- C = 5.31 nF, ESR = 8.59 mΩ and ESL =17.24 pH + the inductance of the vias, where 17.24 pH is the equivalent series inductance of the capacitor. In case$A$ as shown in Fig. 88, the capacitor location was changed vertically in the package. In case B, the capacitor location was changed horizontally with respect to the processor as shown in Fig. 90.

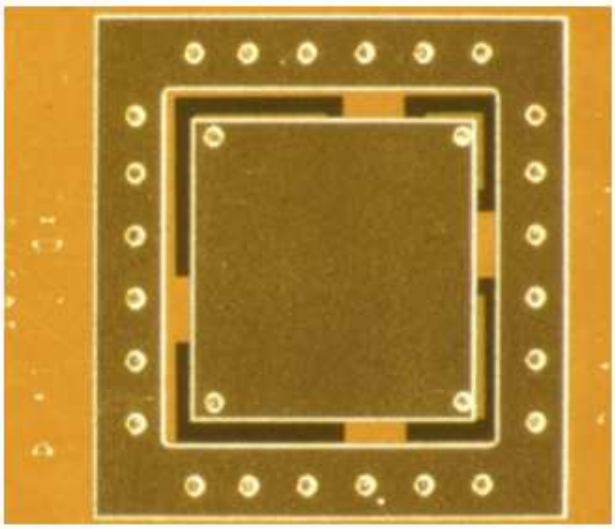


Figure 87: Picture of combination of capacitors.

Case*A*)- The simulations in this case were carried out with the location of the embedded capacitors varying in the vertical distance in the package. There were five test cases that were investigated in these simulations- 1) The individual capacitor layer is put in the top ABF build up layer. The length of the blind via is 38 um and the inductance is 6 pH; 2) The individual embedded capacitors are placed at the top of the core BT laminate. The length of the via pair is 76 um and the inductance of the via pair is 19.74 pH; 3) The individual embedded capacitors are placed 100 um inside the core BT laminate. The length of the via pair is 171 um and the inductance of the pair is 70.6 pH; 4) The individual capacitor is placed in the middle of the core. The via length comprises half the length of the thru holes and the discrete via pairs. The total length of the vias is 376 um and the total inductance associated with the via pair is 123.56 pH; 5) The individual capacitor layer is placed at the bottom of the core laminate, below the bottom most ABF layer. The total length of the thru

Table 9: Via length and inductance values for different cases

Case	Via length(um)	Via inductance(pH)
1	38	6
2	76	19.74
3	171	70.6
4	376	123.56
5	752	319.48

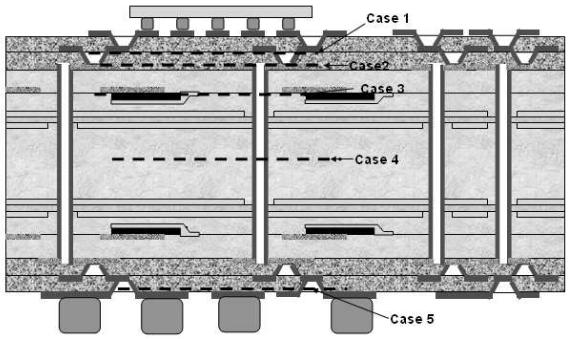


Figure 88: Different vertical locations of the embedded capacitor in the package.

hole and discrete via pair is 752 um and the associated inductance of the via pair is 319.48 pH. The via length and inductance values have been summarized for the different cases in table 9.

The change in array performance is evident from Fig. 89. The shift in the resonant frequency to the lower frequency band can be attributed to the increase in the via inductance in each corresponding case. The minimum series resistance of the array remains almost constant because of the negligible resistance of the vias. These results can be translated into the design of a capacitive array such that the capacitors that are required to target the lower frequency band are placed vertically farther away from the active circuit than the capacitors that decouple higher frequency ranges.

Case$B$) This case analyzes the variation of the four 2 mm $\times$ 2 mm capacitor array performance with a change in the horizontal placement as shown in Fig. 90. It had been mentioned previously that all the embedded capacitors were placed close to or slightly around the processor. Fig. 91, shows the performance change with the horizontal variation of the capacitor array position. The vertical distance of

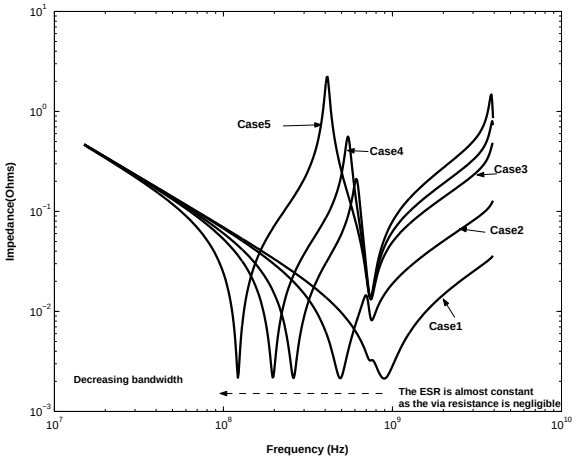


Figure 89: Variation of capacitor array performance with vertical distance.

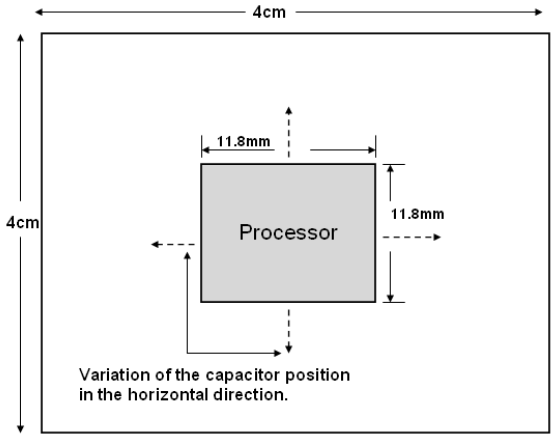


Figure 90: Horizontal variation of the embedded capacitor in the package.

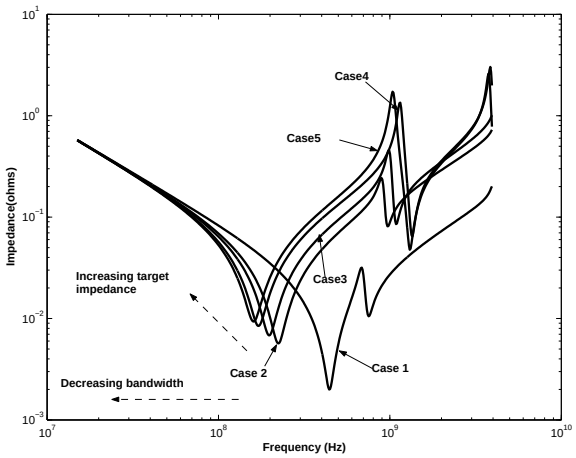


Figure 91: Variation of capacitor array performance with horizontal distance.

the capacitors is kept constant in all the simulation scenarios for this case. The inductance of the a via pair was taken as 19.74 pH. Two via pairs were considered for each capacitor in the array.

Five test cases were investigated 1) The capacitor array was placed directly under the processor. 2) The array was placed 2 mm away from the processor. 3) The array was placed 4 mm away from the processor. 4) The array was placed 1.2 cm away. 5) The placement of the array was 1.9 cm away from the processor. The reduction in the resonant frequency of the capacitor array is because of the increased effect of the spreading inductance of the planes as they are placed further away from the processor. An increase in the distance of the capacitor array from the processor also leads to the increased effect of the resistance of the planes. The effect can be seen in the variation of the minimum series resistance of the array, which increases from one through five. Therefore, from the above analysis it is evident that stacking the capacitors vertically would be advantageous if the PDN is required to decouple active high current densities circuits with very low target impedances.

4.5.1 SMD savings using Embedded Capacitors

SMD savings with the introduction of embedded capacitors in the PDN is highlighted in this section. It has been shown in section 1.6 that SMDs reach their decoupling limitation close to 100 MHz, therefore this frequency point has been chosen for carrying out the following analysis.

The steps involved in determining the number of SMDs that can be saved are determined as follows- Step 1 Use only SMDs in the PDN to meet a target impedance till 100MHz. Step 2 Design the PDN by using embedded capacitors to meet the same target impedance and then introduce SMDs to meet the target impedance at 100 MHz. Observe if there any savings in the SMDs in step 2 as compared to step 1. The analysis was carried out with Dupont capacitor and process ground rules.

In the simulations, it is assumed that the SMDs are connected directly to the PWB solder balls. The dimensions and the pitch of the solder ball are assumed to be 500 um each. A pair of the solder balls were modeled in Fast Henry and the associated inductance of a single pair was calculated to be 138.22 pH. The SMDs under consideration are the low inductance capacitors that are available from AVX [67]. The lead inductance of the AVX LICA capacitors is 25 pH and that of a single thru hole via pair is 280 pH. 100 via pairs are assumed within the package, therefore the effective inductance of the thru vias is 2.8 pH. A single blind pair via is assumed to complete the loop from the bottom and the top of the package. The inductance of a single blind via pair is 19.74 pH as in case two in section 4.5. The complete loop inductance of a SMD is 2.8 + 25 + 138.22 + 39.48 = 205.5 pH. The ESR of the LICA capacitors is 100 mΩ as given in [67]. SMD capacitors that resonate at 50 MHz and 100 MHz were chosen to carry out the analysis. The capacitance required to resonate at 50 MHz and 100 MHz with the calculated inductance is 147.5 nF and 37 nF respectively.

An embedded capacitor of size 5 mm $\times$ 5 mm was chosen for the analysis as it resonates close to 100 MHz as seen in Fig. 92. The parameters of the capacitor are as

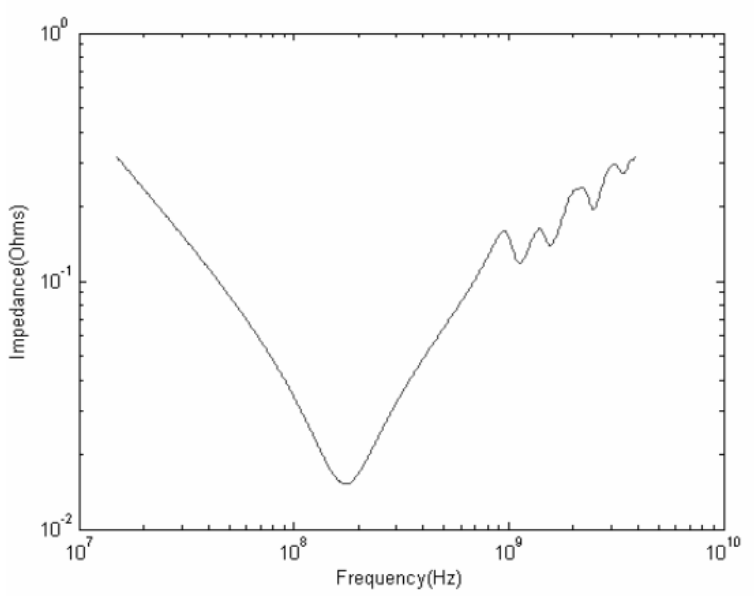


Figure 92: Impedance profile of a 5 mm × 5 mm capacitor used in the analysis.

follows- C = 33.2 nF, ESL = 25.13 pH and ESR = 15.1 mΩ. The target impedance chosen for the analysis is 2 mΩ. Fig. 93, shows the analysis comparison between the two simulations. The solid line is the simulation result with SMD capacitors, 50 capacitors that resonate at 50 MHz and 100 MHz each were used in the analysis. The dashed line is the frequency response of the simulation with 64 SMDs that resonate at 50 MHz and ten 5 mm × 5 mm embedded capacitors. The embedded capacitors were placed at the two individual capacitor layers in the package as previously mentioned in the paper. A savings of 36 SMDs is obtained as per the simulation results. The amount of capacitance available in both cases is almost the same. 9.77 uF of capacitance is available in the case with embedded capacitors as compared to 9.225 uF of capacitance without embedded capacitors.

4.6 Summary

This chapter analyzes the use of thin/thick film capacitors in decoupling processors by using them as an array embedded in a package. The capacitor arrays show performance benefits in both the time and frequency domain and are able to decouple

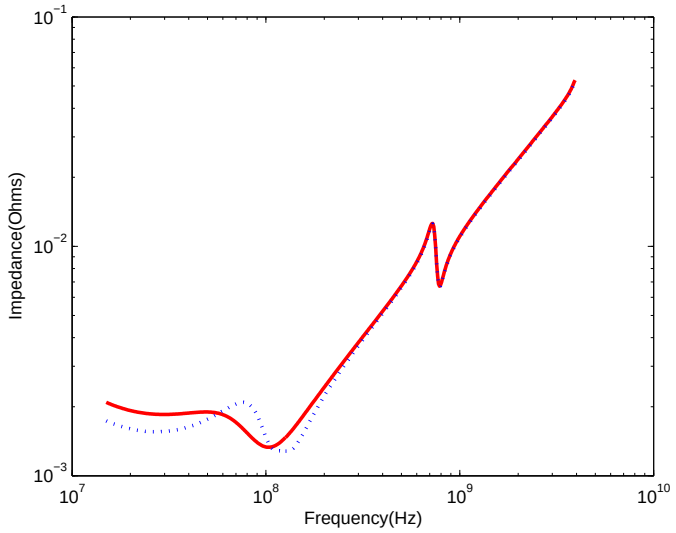


Figure 93: Profile comparison of simulations with and without embedded capacitors.

Table 10: Performance parameters for the DuPont and hydrothermal capacitors

Parameter	Hydrothermal (Barium Titanate)	DuPont
Capacitance density	10nF/mm^2	1.32nF/mm^2
Chip Power	103.6W	40W
Target Impedance decoupled	0.78 mohms	(2-3) mohms
Frequency Band Targeted	100MHz - 2GHz	300MHz - 2GHz
Noise improvements	3X	5X

PDNs that have a target impedance of less than a milli-ohm. An IBM package was analyzed to show the performance improvements by using embedded capacitors. SMD savings and the frequency dependence on position was also highlighted in this chapter. Table 10 compares the performance parameters of the hydrothermal and DuPont capacitors.

CHAPTER V

EMBEDDED PLANAR CAPACITORS IN BOARD

The role of embedded planar capacitors in decoupling active circuits was briefly mentioned in chapter 1. This chapter will investigate the role of these capacitors in more detail. Embedded planar capacitors are thin dielectric layers sandwiched between the power and ground planes in a board or a package as shown in Fig 94. These dielectrics are essentially low-k materials with dielectric constants of the order of 3-4. As mentioned in chapter 1, the main disadvantage of using embedded planar capacitors to decouple active circuits is the narrow frequency band that can be targeted with these capacitors. Also, the capacitance of these structures is of the order of $2-3$ nF for a 4 cm by 4 cm capacitor of thickness 18 um and dielectric constant of 3.5. This value is considerably less than the capacitance value of $2-3$ uF obtained by using an array of embedded thin/thick film capacitors investigated in the previous chapters. This difference in the capacitance value between the planar and individual embedded capacitors make the individual thin/thick film embedded capacitors more viable to decouple core circuits.

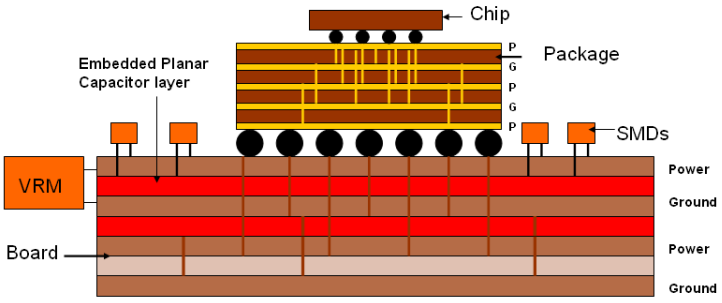


Figure 94: Cross section of a board and package showing the embedded capacitor layers.

The thin planes of the embedded planar capacitors offer a significant increase in capacitance and reduce inductance and resistance. All this results in impedance reduction and this property of embedded planar capacitors make them very useful for providing low impedance path for return currents and help in decoupling I/O circuits as highlighted later in this chapter. The main contributor to the superior performance is the reduced inductive effects of the power-ground planes because of the thinner dielectrics of the embedded capacitor.

The use of relatively thin Printed Wiring Board (PWB) laminates for power distribution layers in multilayer PWBs goes back to the early $1990's$ [68], [69]. The advantages of thin dielectrics for power distribution in high performance (PWBs) have been known for some time. Inclusion of embedded planar capacitors in the stack up have shown improvements in the overall impedance profile and have shown to exhibit better noise performance [70], [71]. The main contributor to the superior performance is the reduced inductive effects of the power-ground planes because of the thinner dielectrics of the embedded capacitor. Thin dielectrics offer low power distribution system impedance, reduced power system noise and reduced EMI. They also offer the opportunity to have additional power or signal layers within a fixed board thickness.There are many publications on the materials, design and application of thin laminates, [72],[73],[74],[75],[76],[77],[78],[79],[80],[81],[82],[83],[84],[85],[86],[87],[88], [89],[90] many from the early proponents and adopters of the technology in the computer and server industries. In these applications thin dielectrics, two to four mils in thickness, replaced the thicker dielectric layers used at the time and higher dielectric constant materials also became available [91],[90].

In this chapter we investigate the performance of various embedded planar capacitors in improving the impedance profile of a board, improving noise coupling between the signal trace and power-ground planes, and in decoupling I/O circuits. As stated earlier in this section, the low capacitance of the planar capacitors do not

make them viable to decouple core circuits. The contributions of this chapter is as follows. 1) Investigation of the impedance profile of the stack up containing embedded planar capacitors with and without surface mount decoupling components along with the model to hardware correlation. The description of the test vehicle along with the modeling and measurement techniques will be highlighted. An analysis of the global placement of the decoupling capacitors using a simple $L-C$ circuit and the prediction of the start and stop frequencies of the band-gap using the electromagnetic band-gap concept will be done; 2) Demonstration of noise coupling suppression between signal traces and power-ground planes is highlighted in this chapter. This includes the description of the test vehicle designed to characterize the coupling, the modeling, and the measurement methodology used; 3) The design of an active test vehicle was done to show the time domain performance improvements by capturing the noise between the power-ground plane for the different dielectric thicknesses. The modeling and characterization methodology used to quantify the noise improvements will be described in detail in this chapter; 4) Eye diagram simulations for different interconnect configurations and embedded planar capacitors was done to highlight the performance improvements with different planar embedded capacitors.

This chapter is organized as follows. Section 5.1.1 the coupling between a signal line and the power ground planes will be described. A model will be shown based on modal decomposition and model to measurement correlation of the measured test vehicle will also be presented. In section 5.2.1 discusses the impedance profile variation with the different dielectrics. The description of the test vehicle designed to capture the differences will be highlighted in detail. The performance of the stack up with and without the surface mount decoupling capacitors will also be investigated. In section 5.2.5, the design of an active test vehicle to capture the simultaneous switching noise phenomenon because of I/O return currents will be described. In section 5.3, simulations of high speed buses with single ended and differential I/Os at data rates

of 1Gbps, 5Gbps and 10Gbps will be highlighted. The performance comparison of the different embedded planar capacitor layers will be done by comparing the eye diagrams.

5.1 Passive Test Vehicle A

This section describes the test vehicle that was designed to characterize the noise coupling suppression between the signal trace and power-ground planes because of the embedded planar capacitors.

5.1.1 Design and Description

The stack up of the test vehicle is shown in Fig. 95. The test vehicle was designed with the signal via passing from the top surface of the test board through the embedded capacitor layer to the second signal trace as shown in Fig. 96. The noise coupling from the signal trace to the power ground planes is captured by probing the signal trace and the power ground plane. The description and measurements of the test vehicle is described next.

The cross section of the stack up is shown in Fig. 96. The test vehicle is a six metal layer stack up with the planar capacitor layer sandwiched between metal layers three and four. Metal layers one, three, and six are the ground layers. Metal layers two and five are the signal layers and metal layer four is the power layer. The signal layers are stripline of 50 Ω and are embedded in a 16 mil thick dielectric material of dielectric constant 3.5. The thickness of the metal layers are 35 um each and effective dielectric constant of the planar capacitor layer is 3.5 with a loss tangent of 0.003. Thicknesses of the capacitor dielectric layers are 18 um, 25 um, and 50 um respectively. These dielectric layers were used in the stack up for a board size of 6" $\times$ 6" as shown in Fig. 95. For measurement of the power-ground impedance, probe points were designed to access the power and ground planes in the test vehicle. Agilent's $E8363B$ vector network analyzer and Cascade ACP 250 um G-S-G probes were used for the

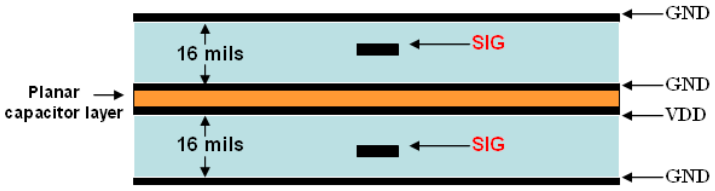


Figure 95: Cross section of stack up for Passive A

measurements. A detailed analysis into the coupling between the signal trace and the power ground plane of the stack up is done in this section. The measurement set up, modeling technique, and model to measurement correlation of the results are presented.

5.1.2 Measurement setup

The signal trace in Fig. 96 is excited from the surface at the first probe point (SIG probe point). The transmission line test vehicle was designed such that the signal via passes through the planar capacitor layer onto the signal trace SIG. The signal trace extends for five and half inches across the board and all the ground planes in the stack up are tied to one another by through vias. The signal trace SIG has a stripline configuration and has a characteristic impedance of 50 Ω. The trace is referenced to a power and ground plane as seen in Fig. 96 and the load end of the signal trace is left unterminated. The second probe point (P-G probe point) was defined on the power-ground plane and was defined as the receiver port. i.e. the transmitter port was used to excite the signal trace and the coupled signal to the power ground plane was measured using probe2. The measurements were done to investigate the performance of all three planar capacitance materials embedded in the board.

The measured coupling results between port 1 and port 2 (S21) are plotted for all three cases in Fig. 97. The results clearly show that the energy coupled from the

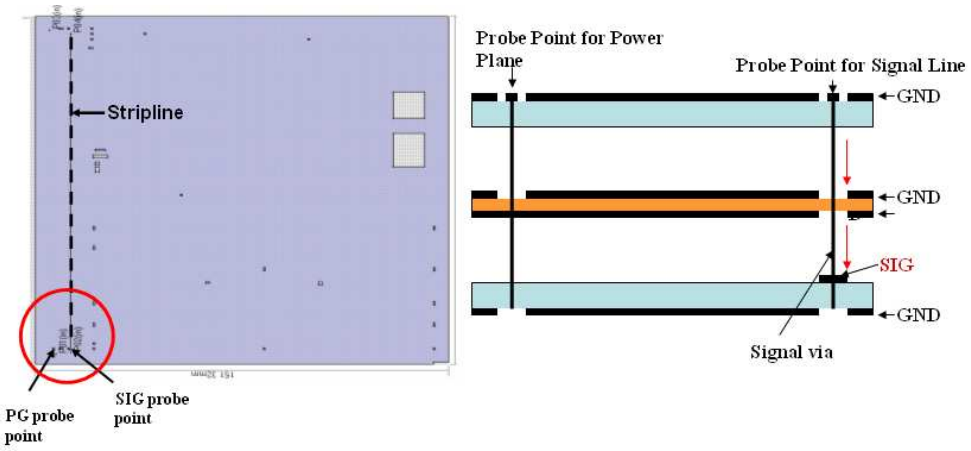


Figure 96: Cross section of the signal to power ground coupling experimental set up.

signal trace to the power-ground plane is the least in the case of the 18 um thick dielectric. In the following the modeling technique used to capture the effect of the signal coupling to the power-ground planes and model to hardware correlation of the measurement will be shown.

5.1.3 Modeling of signal to power-ground plane coupling

The modeling technique used in the analysis will be described in this section. The modeling technique has to be able to capture the voltage fluctuations between the power-ground plane. Such as stripline model has been proposed in [92], which was used in this paper. Previous stripline models as listed in [93] and [94] assume that the reference planes of the transmission lines are at the same potential, which may not be the case in practical situations. The theory supporting the model will be briefly discussed in this section. The multiconductor transmission line(MTL) equations can be expressed in the frequency domain as

$$\frac{d}{dz}\overrightarrow{V}(z) = -\overrightarrow{Z}\,\overrightarrow{I}(z) \tag{65}$$

$$\frac{d}{dz}\overrightarrow{I}(z) = -\overrightarrow{Y}\,\overrightarrow{V}(z) \tag{66}$$

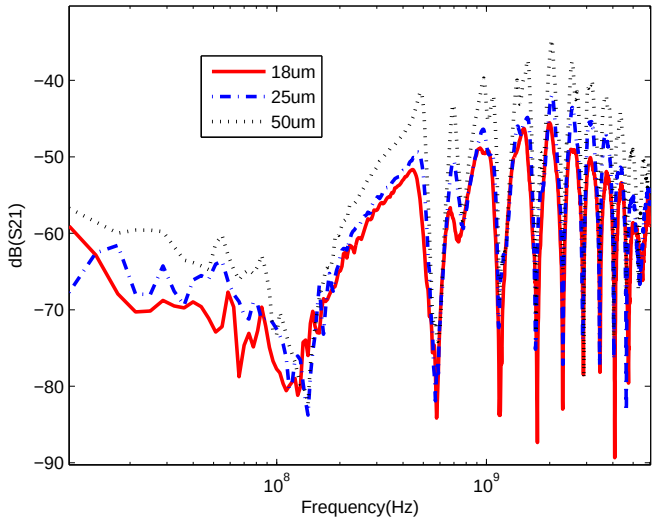


Figure 97: Signal to power ground coupling for all dielectrics.

where $\overrightarrow{Z} = \overrightarrow{R} + jw\overrightarrow{L}$ and $\overrightarrow{Y} = \overrightarrow{G} + jw\overrightarrow{C}$. $\overrightarrow{R}$, $\overrightarrow{L}$, $\overrightarrow{G}$ and $\overrightarrow{C}$ are the per unit length matrices. Two modal transformation matrices $\overrightarrow{T}_V$ and $\overrightarrow{T}_I$ can be defined as

$$\frac{d}{dz}\overrightarrow{V}_m(z) = -\overrightarrow{T}_V^{-1}\overrightarrow{Z}\overrightarrow{T}_I\overrightarrow{I}_m(z) = -\overrightarrow{Z}_m\overrightarrow{I}_m(z) \tag{67}$$

$$\frac{d}{dz}\overrightarrow{I}_m(z) = -\overrightarrow{T}_I^{-1}\overrightarrow{Y}\overrightarrow{T}_V\overrightarrow{V}_m(z) = -\overrightarrow{Y}_m\overrightarrow{V}_m(z) \tag{68}$$

where $\overrightarrow{Z}_m$ and $\overrightarrow{Y}_m$ are diagonal matrices. $\overrightarrow{V}(z) = \overrightarrow{T}_V\overrightarrow{V}_m(z)$ and $\overrightarrow{I}(z) = \overrightarrow{T}_I\overrightarrow{I}_m(z)$ define the modal transformations for the voltages and the currents respectively. Equations (67) and (68) form a set of n single transmission line equations.

Striplines can be modeled using the modal decomposition method . A cross section of the stripline is shown in Fig. 98,where the thickness of the conductors is neglected. The thickness of the lower and upper substrates are $h1$ and $h2$ and the widths of the planes and the signal conductor are w_p and w_s respectively.

Assume that the conductor losses are neglected and the substrates between the planes is homogeneous and the electromagnetic field is confined between the planes. Then the stripline can be considered as a MTL consisting of three conductors in a

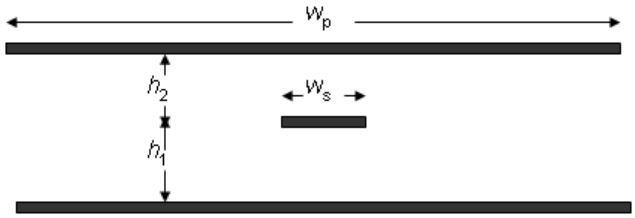


Figure 98: Cross section of a stripline.

homogeneous medium. For this analysis, the bottom plane is chosen as the reference conductor. One of the initial assumptions is the modal decomposition into the stripline and parallel plate mode. In the parallel plate mode, all of the current flowing into one of the planes returns on the other plane, whereas in the stripline mode, which is the intended mode of operation for signal transmission, there is no voltage difference between the planes. Since the bottom plane is chosen as the reference conductor, these statements can be expressed in terms of the transformation matrices

$$\overrightarrow{I}(z) = \begin{pmatrix} \overrightarrow{I}_p(z) \\ \overrightarrow{I}_s(z) \end{pmatrix} = \overrightarrow{T}_I \overrightarrow{I}_m(z) = \begin{pmatrix} 1 & a \\ 0 & b \end{pmatrix} \begin{pmatrix} \overrightarrow{I}_{par}(z) \\ \overrightarrow{I}_{str}(z) \end{pmatrix} \tag{69}$$

$$\overrightarrow{V}(z) = \begin{pmatrix} \overrightarrow{V}_p(z) \\ \overrightarrow{V}_s(z) \end{pmatrix} = \overrightarrow{T}_V \overrightarrow{V}_m(z) = \begin{pmatrix} c & 0 \\ d & 1 \end{pmatrix} \begin{pmatrix} \overrightarrow{V}_{par}(z) \\ \overrightarrow{V}_{str}(z) \end{pmatrix} \tag{70}$$

where the subscripts *par* and *str* represent the parallel plane and the stripline modes, where s and p represent the signal conductor and the upper plane, respectively. For perfect conductors (i.e $\overrightarrow{R}$=0) in a homogeneous medium, $\overrightarrow{C}$ and $\overrightarrow{G}$ are both diagonalized [95], if L can be diagonalized by the transformation matrices $\overrightarrow{T}_v$ and $\overrightarrow{T}_l$ as in equation (67). Therefore, in order that this choice of the transmission matrices be appropriate, it must be shown that $\overrightarrow{L}$ is diagonalized by the product $\overrightarrow{T}_v^{-1} \overrightarrow{L} \overrightarrow{T}_l$. By explicitly doing this multiplication, it can be shown that the $\overrightarrow{L}$ is diagonalized if the following relations hold

$$a = -\frac{L_{12}}{L_{11}}\, b \tag{71}$$

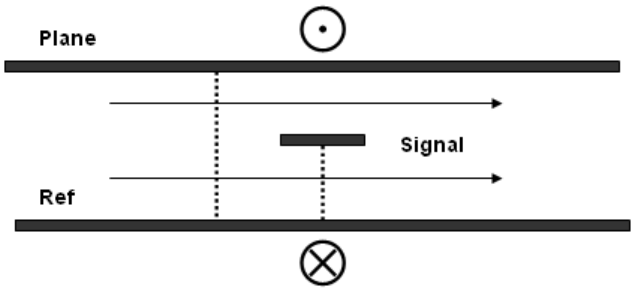


Figure 99: Alignment of the uniform magnetic flux lines and the imaginary lines for the computation of the inductance matrix.

$$d = \frac{L_{12}}{L_{11}}\, c \tag{72}$$

where L_{11} and L_{12} represent the per-unit-length self inductance of the upper plane and the per-unit-length mutual inductance between the upper plane and the signal conductor, respectively.

In striplines, the ratio $\frac{L_{12}}{L_{11}}$ can be obtained from the geometrical dimensions. Assume that no current flows on the signal conductor, such that the current flowing in the upper plane returns through the bottom plane.

If an arbitrary imaginary line is drawn from the signal to the reference conductor as shown in Fig. 99, then L_{12} is given by the ratio of the magnetic flux penetrating this line to the current flowing in the planes. L_{11} can be obtained similarly by the ratio of the magnetic flux penetrating a line drawn between the two planes, to the current flowing in the planes. For such an excitation, the electromagnetic field between the planes can be approximated to be uniform by neglecting the fringing effects. It can then be observed that the following relation holds

$$\frac{L_{12}}{L_{11}} = \frac{h_1}{h_1 + h_2} \tag{73}$$

Without loss of generality, the elements of the transformation matrices can be chosen as

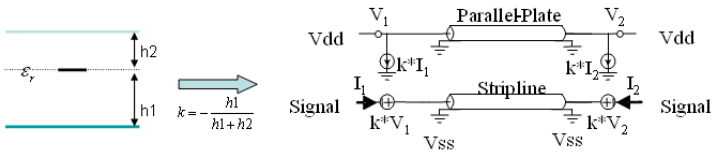


Figure 100: Equivalent model of a stripline.

$$b = \ c = \ 1 \tag{74}$$

$$a = -d = -\frac{L_{12}}{L_{11}} = -\frac{h_1}{h_1 + h_2} = k \tag{75}$$

An equivalent multiport model of the stripline can be found as shown in Fig. 100. Z^c_{par} and Z^c_{str} represent the characteristic impedance of the parallel plate and stripline modes respectively. The controlled sources represent the coupling between the two modes and can be obtained from the dielectric thicknesses.

The stripline SIG was designed to be a 50 Ω line, the thickness of the dielectric in which the stripline is embedded is 16mils thick and has a dielectric constant of 3.5, which translates into a line width of 7.1 mils for the transmission line. The transmission line is placed at the center of the 16 mil thick dielectric. Since the ground planes are tied together using vias, the effect of the parallel combination of all the power ground pairs need to be taken into account. The thickness of the dielectric in which the stripline is embedded is 16 mils (406.4 um) as compared to the 18 um, 25 um and 50 um thick planar dielectric layers. The dielectric constant of both materials are comparable and since they are in parallel, the capacitance of the thinner power ground layer will dominate.

The input parameters to the power plane were obtained by modeling the power ground plane pair using the transmission matrix method. A total of three ports were defined in the model at the input, output and power-ground probe locations

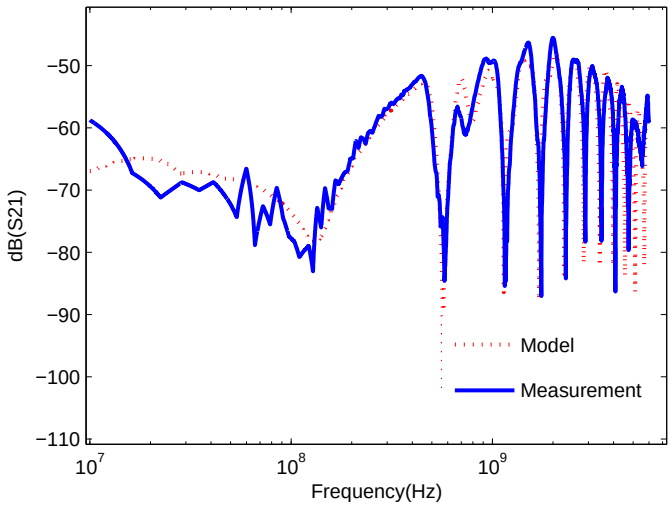


Figure 101: Modeled to measured coupling between signal trace and power ground planes for the 18 um thick dielectric.

corresponding to the similar locations on the planes. The S parameter frequency response of the 3 ports were used as the input to the model, which was simulated using ADS. The signal via transitions from the top surface of the board to the SIG layer through the embedded capacitive layer. The coupling from the signal trace to the power-ground planes as obtained with the model and measurement for the 18 um thick embedded capacitor layer is plotted in Fig. 101. The modeled to measured result shows good correlation over the frequency band of interest. The discrepancy from 10 MHz to 100 MHz is because of the smaller number of points taken for measurement in that frequency band.

As shown in the previous section, the measured results of all three capacitive layers are plotted in Fig. 97 and it can be clearly seen that the 18 um thick dielectric provides the best isolation between the signal and the power-ground probe point.

5.2 Passive Test Vehicle B

This section describes the test vehicle that was designed to characterize the impedance profile with planar embedded capacitors in the stack up.

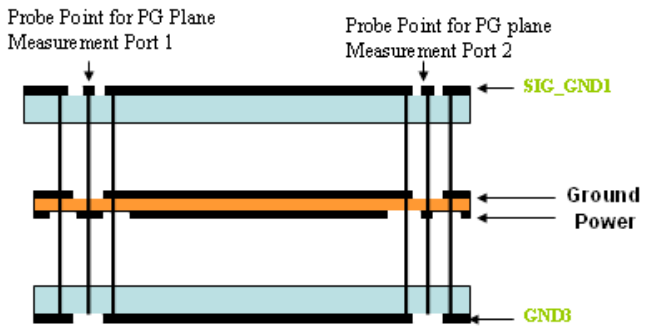


Figure 102: Cross section of stack up for Passive B

5.2.1 Design and Description

The board was designed to highlight the impedance profile improvements by inclusion of embedded planar capacitors in the stack up. The results presented in this section are for the boards with and without surface mount discrete capacitors mounted on the board. The cross section of the stack up is shown in Fig. 102. The stack up of passive test vehicle B is similar to passive test vehicle A. Passive test vehicle B is a four metal layer stack up with the planar capacitor layer sandwiched between metal layers two and three. Metal layers one, two, and four are the ground layers and metal layer three is the power layer. The dielectric layer between metal layer one and two and between three and four is a 16 mil thick with a dielectric constant of 3.5. The thickness of the metal layers are 35 um each and the effective dielectric constant of the planar capacitor layer is 3.5 with a loss tangent of 0.003. Thicknesses of the capacitor dielectric layers were 18 um, 25 um and 50 um respectively. These dielectric layers were used in the stack up for a board size of 8"$\times$ 8" as shown in Fig. 95. For measurement of the power-ground impedance, probe points were designed to access the power and ground planes in the test vehicle. Agilent's $E8363B$ vector network analyzer and Cascade ACP 250 um G-S-G probes were used for the measurements.

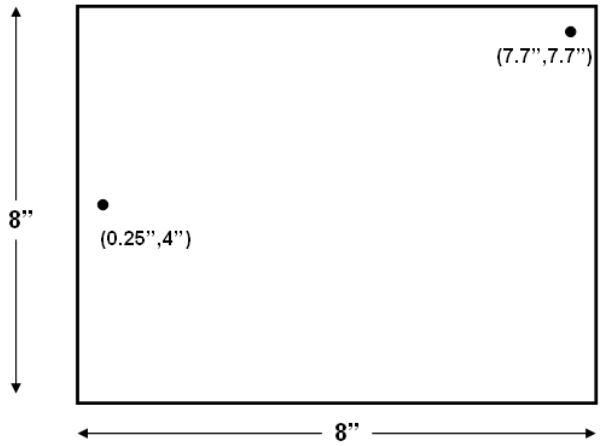


Figure 103: Measurement port locations for the two port measurement methodology.

The impedance profile was generated using a 2 port measurement methodology as described in [54]and in chapter 3. The ports were defined as shown in Fig. 103. The stack up was modeled by using the transmission matrix method [31]. This tool has been previously used to model power plane structures [57],[58]. In the transmission matrix method the power plane is divided into unit cells. Each unit cell consists of an equivalent circuit with R,L,C, and G components and are cascaded together in a Π or T network.

5.2.2 Measurement and Modeling of the passive test vehicle B

The model to measurement correlation for the 18 um thick dielectric with the two port measurement methodology is shown in Fig. 104. The measurement curve was obtained by using equation 51. This equation is an approximation, but as seen in Fig. 104, the correlation between the model and the measurement is accurate. This result concludes that the via inductances do not have a significant effect on the impedance profile of the structure i.e if the impedance of the power-plane structure is much less than 25Ω, then the via inductances do not have any effect on the measurements. The measurement results shown in Fig. 104 were done on a bare board, without any surface mount

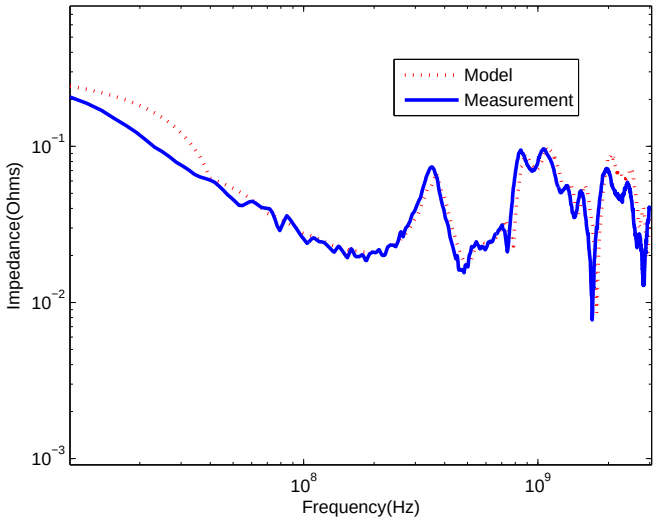


Figure 104: Measured and modeled impedance profiles for the 18 um dielectric.

decoupling capacitors. The measurement comparison of the three dielectric layers is shown in Fig. 105. The measurement results clearly show the benefits of using thinner dielectrics for improving the impedance profile. Since the thin dielectrics provide low impedance to the flow of electro-magnetic waves between the power-ground planes, the electro-magnetic radiation at the edges of the power planes is reduced [96], [97].

The measurement results with the same board populated with 168 0402 surface mount decoupling capacitors is shown in Fig. 106. The parameters of the surface mount decoupling capacitors are - Capacitance = 1 nF, series inductance = 400 pH and series resistance = 0.161 Ω. The modeled results in Fig. 106 include the via inductance that connects the capacitors to the power-ground planes. The diameter of the via is 19 mils and the center to center distance is 35 mils. The inductance of the vias and the pads was calculated using Fast Henry [30] and the resultant inductance of 300 pH was included in the simulations. The capacitors were placed in a regular fashion across the board in a pattern of 12 rows and 14 columns spaced equidistance from each other as shown in Fig. 107, which translates into an EBG like response shown in Fig. 106. This global placement of capacitors on a board is commonly used

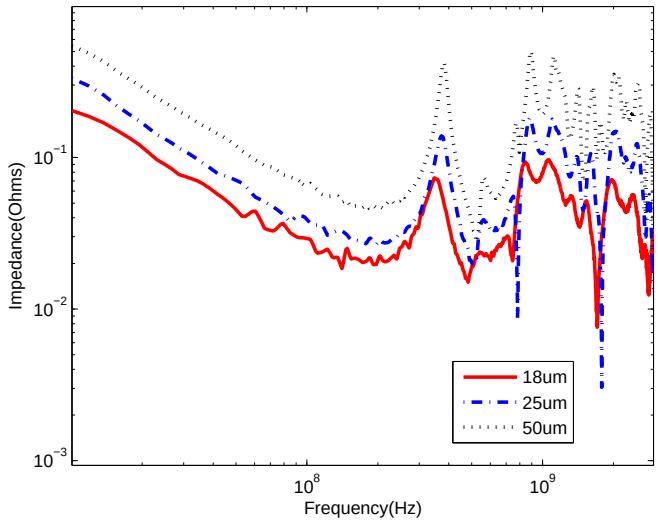


Figure 105: Impedance profile comparison of bare boards for the three different dielectrics.

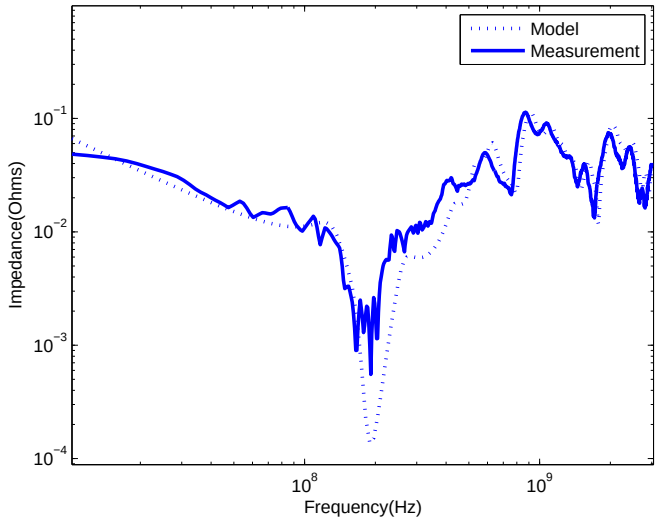


Figure 106: Measured and modeled impedance profiles for the 18 um dielectric with SMD capacitors.

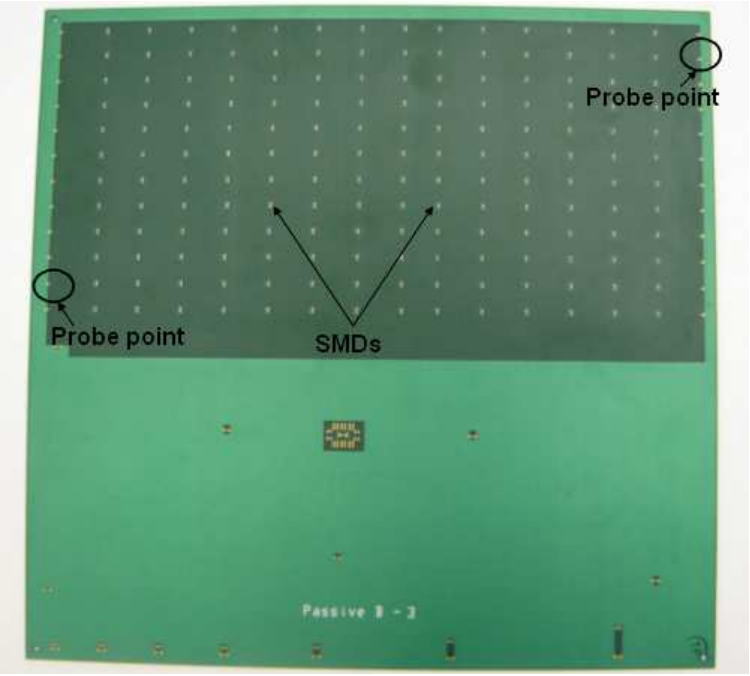


Figure 107: Test vehicle with SMDs uniformly distributed.

to control electromagnetic interference (EMI) and essentially represents an electromagnetic band-gap (EBG) structure. The electromagnetic band-gap structures have been described extensively in literature [98], [99], [100], [101], [102], [103]. The EBG structure is a periodic structure in which the propagation of electromagnetic waves is not allowed in a specific frequency band. The measured impedance profile with the capacitors shows a band gap like characteristic as observed in Fig. 106. The same measurement was repeated with the 25 um and 50 um thick dielectrics. The measurement results of all three cases are plotted in Fig. 108. It is observed that the embedded capacitors do not have any effect on the impedance profile at lower frequencies. The embedded capacitors are more effective only above 500 MHz i.e, after the surface mount decoupling capacitors become ineffective. The performance variation of the embedded capacitors can be clearly seen with the difference in the amplitude of the Z parameters. The 18 um thick dielectric has the minimum value of the Z parameters through the frequency band over 500 MHz. This can be attributed to the lower inductance associated with the 18 um thick dielectric as compared to

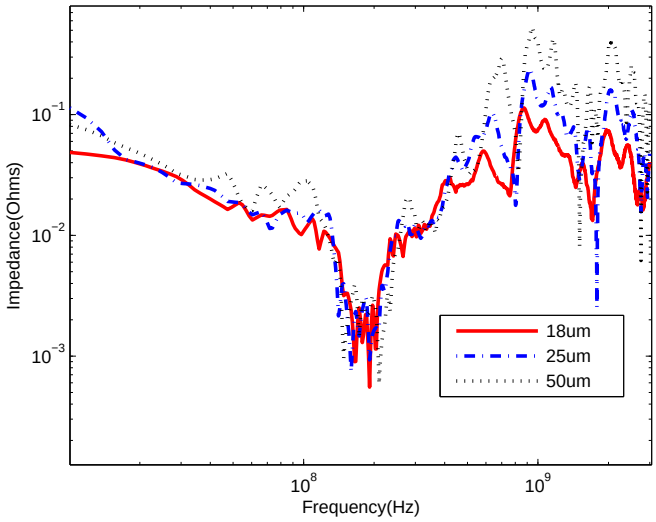


Figure 108: Measured impedance profiles for all the dielectric with SMD capacitors.

the 25 um and 50 um thick dielectrics. The comparison of the impedance profiles of different dielectrics with and without the SMDs is show in Fig. 109 and Fig. 110. The comparison is between the populated 50 um thick dielectric and the bare 25 um board and bare 18 um board respectively. The impedance profile clearly shows the benefits of the SMDs in lower frequency region. Above 500 MHz the benefits of the thinner dielectrics is obvious because of the reduced inductance of the planes.

5.2.3 Analysis of band-gap characteristic

An analysis was done to determine the band gap characteristic of the stack up with the SMDs. The SMDs are attached to the power -ground plane which is 18 um thick and has a dielectric constant of 3.5 contributing a total capacitance of 69 nF. To analyze the stack up, the power-ground pair around which the capacitors were mounted was assumed to be divided into 168 equal parts. The resultant unit cell is shown in Fig. 111. The resonant frequency of the band gap of the resultant unit cell can be calculated by equation (76):

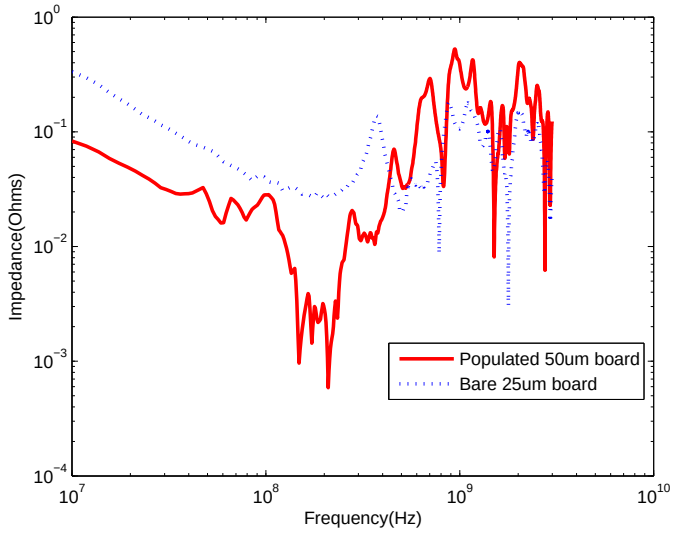


Figure 109: Measured impedance profile comparison of a bare 25 um and populated 50 um board.

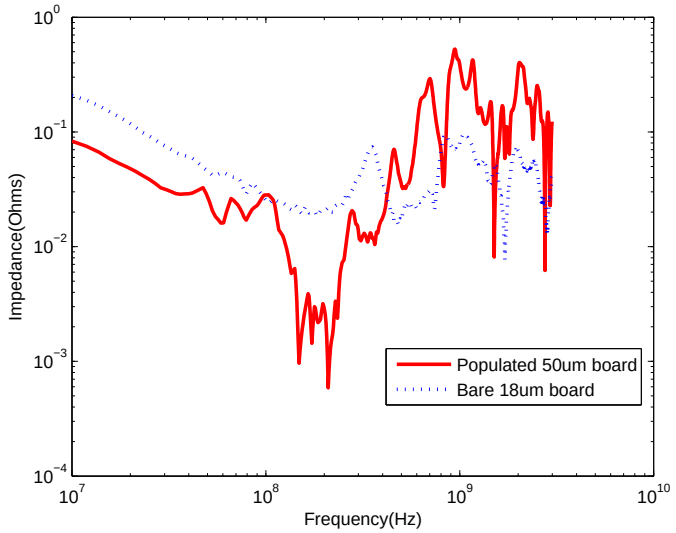


Figure 110: Measured impedance profile comparison of a bare 18 um and populated 50 um board.

$$f = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{76}$$

C_1 is the capacitance of an individual SMD in the unit cell and L_1 is the inductance of the SMD capacitor. The resonant frequency was calculated as 190.2 MHz and is captured in the measurements. The effective resistance of the capacitor array is calculated by dividing the series resistance of one capacitor by the total number of capacitors. Therefore, the effective resistance of the capacitor array is 0.95 mΩ as can be seen in Fig. 106.

The measurement results of the global placement of the capacitors show a band gap like result. Therefore, to predict the start and stop frequencies of the band gap an equivalent circuit model of the meshed structure was formed and analyzed, similar to the methodology used in [104]. The stopband and passband properties of the EBG structure could be understood through a circuit analysis of only one unit cell. The capacitor and the via inductance present a shunt susceptance given by

$$Y = \frac{j\omega C_1}{1 - \omega^2 L_1 C_1} \tag{77}$$

The two dimensional periodic structure is simplified to an array of one dimensional unit cells as shown in Fig. 111

The TEM mode excited within a unit cell of height h and width d is modeled as a simple parallel plate transmission line of characteristic impedance and phase constant given by following equations:

$$Z_o = \frac{\eta_o}{\sqrt{\epsilon}} \frac{h}{d} \tag{78}$$

$$\beta = \frac{\omega}{c}\sqrt{\epsilon} \tag{79}$$

where η_o is the wave impedance of free space (377 Ω), c is the speed of light in

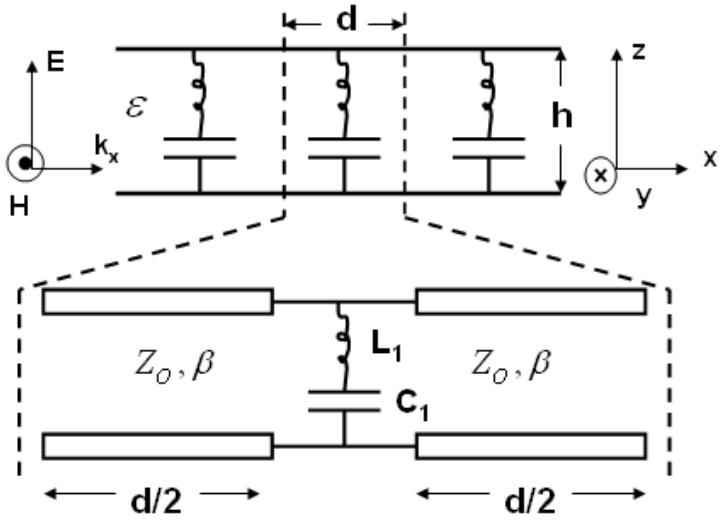


Figure 111: Transmission line for one unit cell in the approximated EBG structure.

vacuum, ω is the radian frequency and the ϵ (3.5) is the dielectric constant of the power-ground unit cell. To predict the dispersive behavior of this structure, the unit cell can be analyzed by using the $ABCD$ parameters, where the unit cell has the effective phase constant k_x as

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} cos(k_x d) & jZ_o sin(k_x d) \\ jY_o sin(k_x d) & cos(k_x d) \end{pmatrix}$$

$$= \begin{pmatrix} cos(\beta\frac{d}{2}) & jZ_o sin(\beta\frac{d}{2}) \\ jY_o sin(\beta\frac{d}{2}) & cos(\beta\frac{d}{2}) \end{pmatrix} \begin{pmatrix} 1 & 0 \\ \mathrm{Y} & 1 \end{pmatrix}$$

$$\begin{pmatrix} cos(\beta\frac{d}{2}) & jZ_o sin(\beta\frac{d}{2}) \\ jY_o sin(\beta\frac{d}{2}) & cos(\beta\frac{d}{2}) \end{pmatrix}$$

Evaluation of the A component yields the dispersive equation

$$cos(k_x d) = cos(\beta d) + j\frac{Z_o Y}{2} sin\beta d \tag{80}$$

From equation (80) we can explicitly solve for the effective phase constant k_x

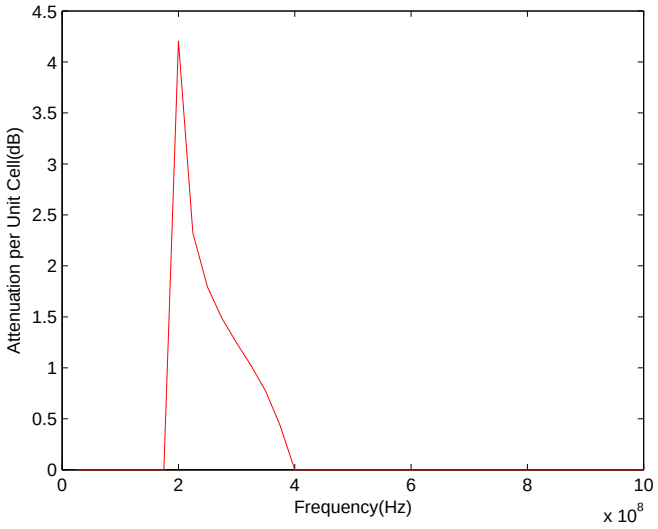


Figure 112: Calculated attenuation per unit cell of the EBG structure.

$$k_x = \frac{1}{d} cos^{-1}[cos\beta d - \frac{\omega C_1 Z_o}{2(1-\omega^2 L_1 C_1)} sin\beta d] \tag{81}$$

From the above equation, the attenuation can be calculated as follows.

$$Attn = -20log_{10}(e^{-\alpha_x d}) \tag{82}$$

where, α_x is the real part of the effective phase constant k_x and the field decay over one unit cell is $e^{-\alpha_x d}$. This quantity has been expressed as the power attenuation per unit cell in decibels using equation (82). This quantity is plotted in Fig. 112, the regions where the attenuation constant is non-zero is the stop band of the periodic structure. According the values in the Fig. 112 the stopband should exist from approximately 170 MHz to 400 MHz, however the measured stop-band for the 18 um dielectric exists from 130 MHz to 300 MHz. There is a difference between the predicted and the measured values, since a simple $1D$ unit-cell approach was used to generate the attenuation plot.

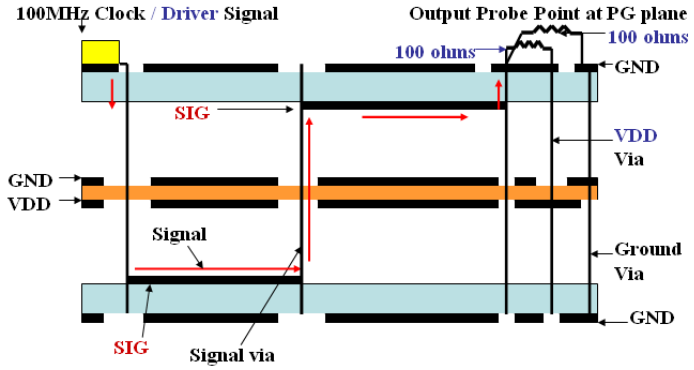


Figure 113: Cross section of active test vehicle.

5.2.4 Active Test Vehicle

An active test vehicle was designed using the embedded capacitor layers to investigate their performance in the time domain. The test vehicle consisted of a clock generator, transmission lines, termination resistors and probe points to measure the power-ground noise as well as the clock signal.

5.2.5 Description of the active test vehicle

The cross section of the active test vehicle showing the signal path is shown in Fig. 113. The stack up of the signal is identical to that of Passive test vehicle A. The test vehicle consists of two stripline configurations. The upper SIG layer has two ground planes as its reference planes while the bottom SIG layer has a power and ground plane as its references as shown in Fig. 113.

The length of the transmission line from the driver to the termination resistor is 20 inches and the width of the reference planes are 1 inch. A 100 MHz clock oscillator was used as the input excitation signal. The transmission line on the signal trace was designed to be 50 Ω. The dielectric constant and the thickness in which the transmission lines were embedded were identical (i.e, the thickness and dielectric constant of the material are 16 mils and 3.5 respectively). The width of the transmission line is 7.1 mils and the thickness of copper on all planes is 1.4 mils. The test vehicle

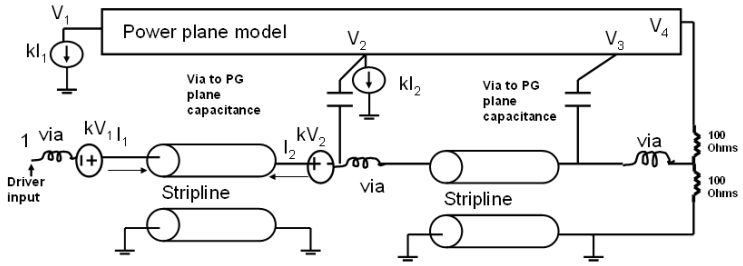


Figure 114: Equivalent model of the signal configuration of the active test vehicle.

was powered at 3.3 V by connecting it to a power supply using an SMA connector. The active test vehicle included two decoupling capacitors of values 0.1 uF and 0.01 uF as specified in the data sheet for the clock oscillator. The transmission line was terminated with two 100 Ω resistors connected to the power and ground plane respectively to give an equivalent termination resistance of 50 Ω. Probe points for a passive probe were defined along the length of the transmission line to measure the power ground noise that was generated due to the return current issue. An SMA connector was connected at the load end of the transmission line to measure the power ground noise. The equivalent model of the cross section of the active test vehicle is shown in Fig. 114. The via inductance in the model near the driver end, between the signal traces and at the load corresponds to the discontinuity because of the vias in the test vehicle. The coupling between the signal trace and the power plane is the represented by a capacitance in the model, which is of the order of 100 fF.

5.2.6 Model to measurement correlation of the active test vehicle

As mentioned previously, the input excitation waveform is a 100 MHz clock. The driver model to simulate the clock oscillator was developed by using a combination of switching resistors. One end of the driver model is connected to the V_{DD} plane while the other is connected to the ground plane as shown in Fig. 115.

The driver acts like a voltage divider and the output of the model is fed as the input to the transmission line model. The input parameters to the switching resistors

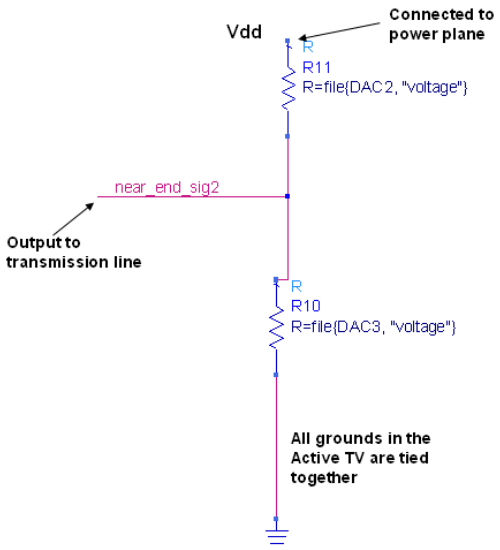


Figure 115: Driver model used to generate square wave.

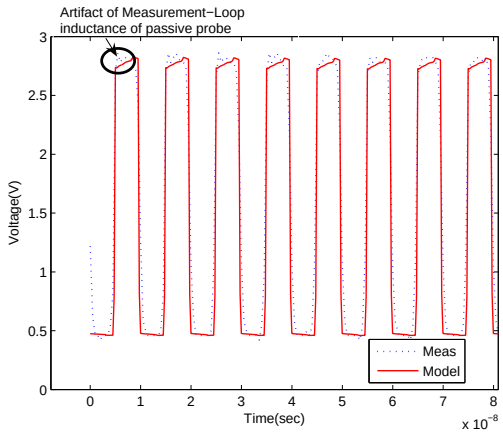


Figure 116: Model to measurement correlation of the input waveform.

are the rise, fall and time period of the 100 MHz clock. The model to measurement correlation of the input pulse in the time domain and frequency domain are shown in Fig. 116 and Fig. 117 respectively. The spike observed in the measured result is due to the loop inductance of the signal-ground loop in the passive probe used to probe the output pin of the clock oscillator.

The model included the via inductance from the top surface to the bottom *SIG* layer, the via inductance between the two signal layers and the via coupling between the signal via and the power ground plane. The measurement was done by connecting

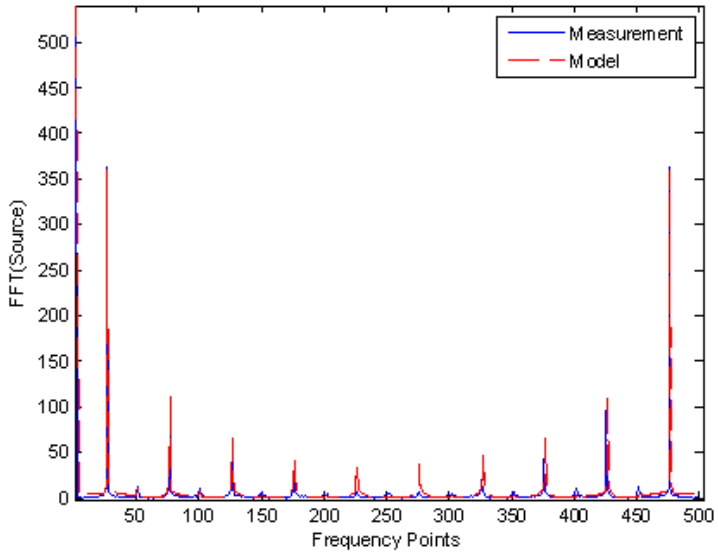


Figure 117: Model to measurement correlation of the FFT of input waveform.

a cable to the SMA connector, which connects to the power-ground plane at the load end. The other end of the cable was attached to the input of a $HP54615B$ 500 MHz oscilloscope with a sampling rate of 1 GSa/s. The noise introduced by the scope is shown in Fig. 118, which is less than 1 mV.

The model to hardware correlation for the switching noise with the 18 um thick dielectric is shown in Fig. 119.

The peak-peak noise voltage is 15 mV and is captured by the model. The spikes observed in the modelled result occur at the low to high and high to low transitions due to the rapid change in the current amplitude. The spikes have not been captured in the measurements and this could be due to the resolution and the number of points that can be captured at any given time interval of the scope. The measured noise comparison for all three dielectrics is plotted in Fig. 120. The noise voltage for the 18 um, 25 um and 50 um are 15 mV, 18 mV and 37 mV respectively. The decrease in the noise waveform magnitude can be explained as follows: The thin dielectrics

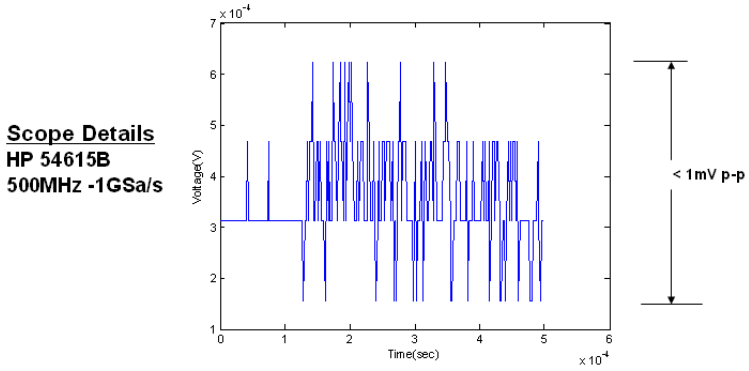


Figure 118: Noise introduced by the scope.

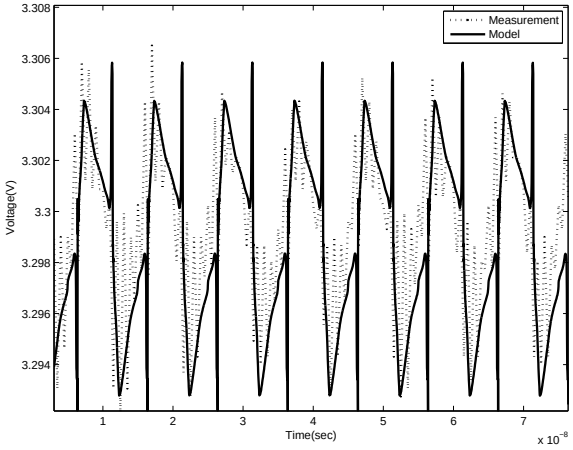


Figure 119: The model to hardware correlation of the noise waveform for 18 um thick dielectric.

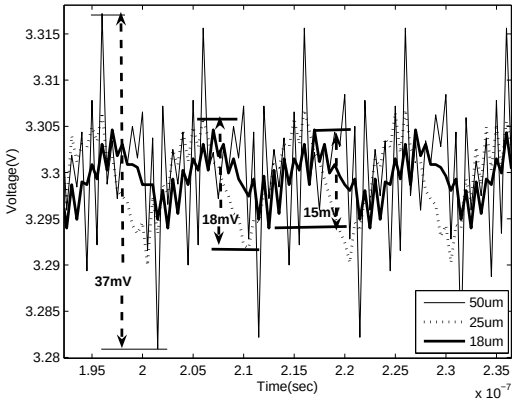


Figure 120: Noise voltage comparison for the 3 dielectrics.

have a two fold advantage, the capacitance of the structure increases for the same dielectric as given by the equation (83):

$$C = \frac{\epsilon_o \epsilon_r A}{d} \tag{83}$$

where, ϵ_o is the relative dielectric constant of the dielectric, A is the area of the capacitive structure and d is separation between the plates of the structure. Also, the inductance of the same structure, which is given by (84) reduces due to a decrease in the separation between the plates.

$$L = \mu_o d \tag{84}$$

The effective increase in the capacitance and decrease in the inductance leads to an overall decrease in the impedance of the power planes as given by equation (85):

$$Z = \sqrt{\frac{L}{C}} \tag{85}$$

Electromagnetic waves propagating through the power-ground plane will see a reduced impedance, therefore generating less noise voltage as per ohms law.

The normalized noise voltage with respect to the thickness in plotted in Fig. 121. The model and the measured results agree very well. The modeled result is plotted

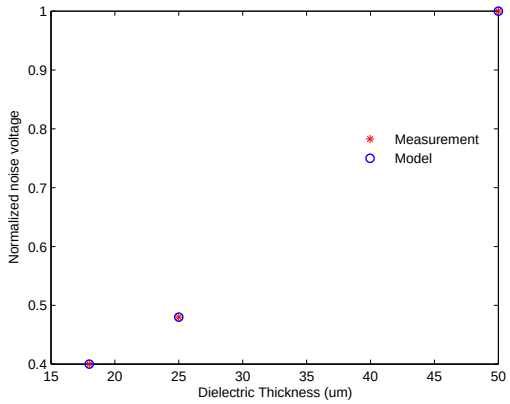


Figure 121: The modeled and measured normalized noise voltage.

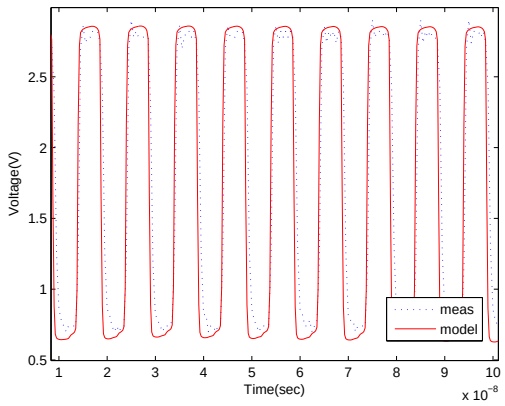


Figure 122: Load waveform for the 18 um thick dielectric.

as a straight solid line and the measured result is plotted as a circle. The model to measurement correlation for the load waveform for the 18 um dielectric is plotted in Fig. 122.

5.3 Benefits of Embedded Planar Capacitors in System Applications

This section describes the simulations carried out for I/O configurations present in todays high data rate digital systems. The configurations were single and differential bus configurations with data rates of 1 Gb/s, 5 Gb/s and 10 Gb/s. The transmission line in these simulations were in the stripline configuration and were terminated

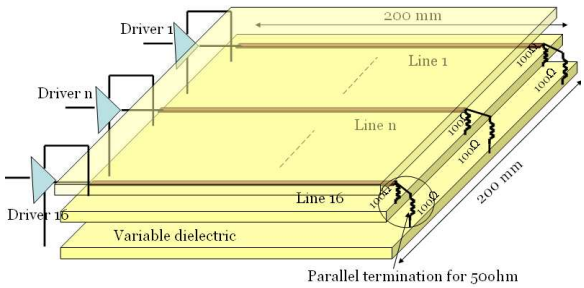


Figure 123: Simulation set up for the 16 bit FSB.

Table 11: Dielectrics used in the SSN and eye opening simulations

Dielectric thickness(um)	Dielectric constant	Loss Tangent
8	3.5	0.003
12	3.5	0.003
18	3.5	0.003
25	3.5	0.003
50	4.2	0.015
50	3.5	0.008

differentially with matched loads.

5.3.1 Single Ended Stripline Configuration

The first configuration was of a 16 bit Front Side bus (FSB). This configuration consists of 16 50 Ω uncoupled single ended transmission lines terminated differentially at the load end with two 100 Ω resistors to give an effective termination of 50 Ω. The model used in this simulation was similar to the stripline model used in the passive test vehicle. The length of transmission line is 200 mm and the dimensions of reference planes are 200 mm by 200 mm. The methodology used to carry out the simulations was similar to the method mentioned in the previous sections. The simulation set up is shown in Fig. 123. The different dielectric layers used in the simulations are listed in table 11.

The simulation for the FSB was done with pseudo random sources (PRBS) at 1 Gb/s. The rise and fall times of the source was 200 psec with a 1 V voltage swing. The driver model used was similar to the driver models used in the active test

Table 12: SSN variation with different dielectrics at 1Gb/s

Dielectric thickness(um)	Dielectric constant	SSN peak to peak magnitude(mV)
8	3.5	237
12	3.5	414
18	3.5	445
25	3.5	489
50	4.2	968
50	3.5	980
50 + 100 × 100nF decaps	3.5	695

vehicles. The variation in the SSN is listed in table 12

The last row in table 12, refers to the case when a simulation was carried out with the 50 um thick dielectric, with a dielectric constant of 3.5 and 100 decoupling capacitors with C=100 nF, ESR=0.03 Ω and ESL=400 pH scattered around the driver end, receiver end and along the length of the transmission line. The effectiveness of the different planar capacitors can be compared by their eye diagrams. Fig. 124 and Fig. 125, compare the eye diagrams of the last 2 rows of table 12 respectively. The improvements in the eye diagrams are evident with the decoupling capacitors. However, the performance improvement can be enhanced considerably when a 18 um thick dielectric with a dielectric constant of 3.5 is used as shown in Fig. 127. From the above results it can be inferred that for decoupling I/O circuits planar embedded capacitors can be more effective compared to using individual decoupling capacitors. Eye diagram and SSN simulations for the above dielectrics listed in table 12 are included in Appendix *A* at the end of thesis.

5.3.2 Differential Microstrip Configuration

Similar analysis was done for a 4 pair differential microstrip configuration. The simulation data rates used were 5 Gb/s and 10 Gb/s with PRBS input waveforms having a voltage swing of 1V. The rise and fall times for a 5 Gb/s driver model were 40 psec with a skew of 10 psec between the 2 differential signals. The common mode and differential mode resistance of the transmission lines were 50 Ω and 100 Ω respectively.

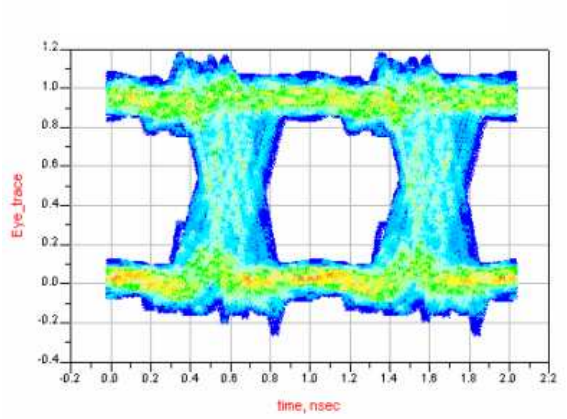


Figure 124: Eye diagram result for row 7 of table 12, 50 um dielectric planar capacitor at a data rate of 1 Gbps.

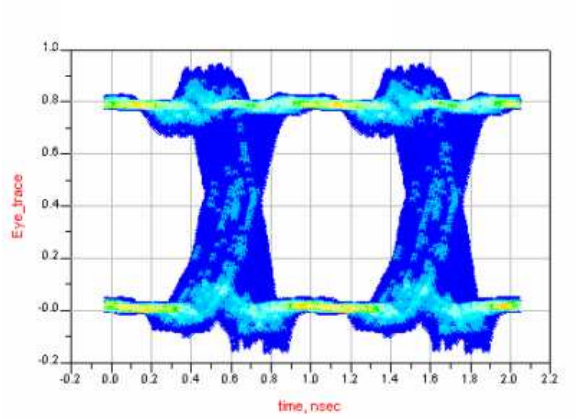


Figure 125: Eye diagram result for row 8 of table 12, 50 um planar capacitor with 100 decoupling capacitors at a data rate of 1 Gbps.

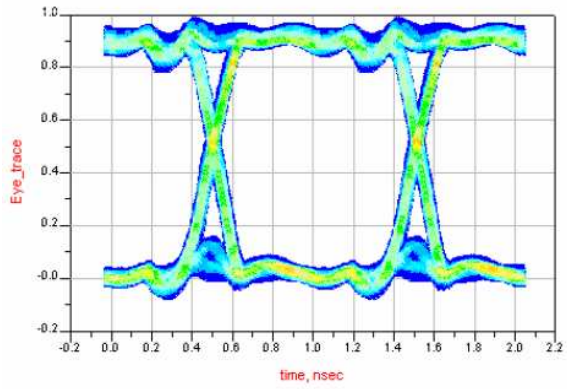


Figure 126: Eye diagram result for row 4 of table 12, 18 um dielectric planar capacitor at a data rate of 1 Gbps.

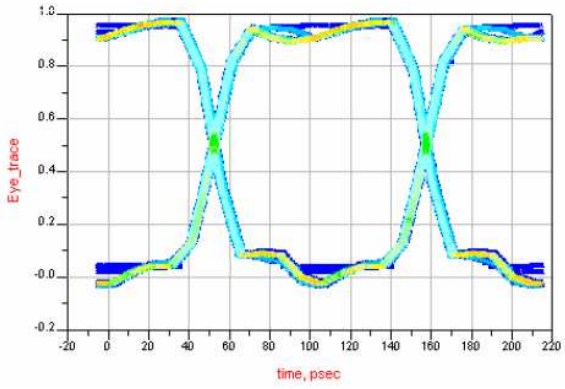


Figure 127: Eye diagram result for the 18 um thick, dielectric constant 3.5 at a differential data rate of 10 Gbps.

The simulation set up for the 10 Gb/s was identical with the previous case, the difference being in the rise time and fall times. The rise and fall time were 20 psec each and the skew between drivers of each differential pair was the same as for the 5 Gbps (i.e 10 psec). The SSN was much less than the single ended as would be expected for a differential driver set up and the eye diagram are much cleaner as shown for the 18 um dielectric and 50 um dielectric with a dielectric constant of 3.5 each in Fig 127 and Fig 128 respectively, for a data rate of 10 Gb/s. The simulation results are tabulated for the different dielectrics in table 13. Eye diagram and SSN simulations for the above dielectrics listed in table 13 are included in Appendix *B* and *C* respectively at the end of thesis. The simulations were carried out to highlight the performance improvements in the SSN and eye diagram results with different dielectrics.

5.4 Summary

This chapter highlighted the role of embedded planar capacitors in decoupling high speed I/O circuits and improving the impedance profile of the stack up in which it is included. Active and passive test vehicles were designed and characterized to illustrate the benefits of these capacitors. Accurate correlation between models and measurements were shown that highlights the validity of the models developed. System

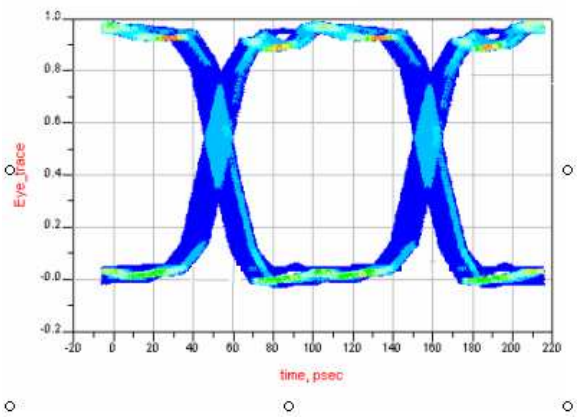


Figure 128: Eye diagram result for the 50 um thick, dielectric constant 3.5 at a differential data rate of 10 Gbps.

Table 13: SSN variation with different dielectrics at 5 Gb/s and 10 Gb/s for a four pair differential microstrip configuration.

Dielectric thickness(um)	Dielectric constant	SSN peak to peak magnitude(mV) at 5Gb/s	SSN peak to peak magnitude(mV) at 10Gb/s
8	3.5	8	44
12	3.5	29.4	74
18	3.5	89.5	106.5
25	3.5	128	157
50	4.2	200	278
50	3.5	225	280

Table 14: Performance variation with different dielectrics at 1 Gb/s 16 bit Single ended strip-line configuration.

Dielectric thickness(um)	Dielectric constant	Jitter (ps)	Eye Height (V)
18	3.5	82.6	0.80
50	3.5	298.54	0.69
50 + 100 X 100nF decaps	3.5	275	0.72

Table 15: Performance variation with different dielectrics at 5 Gb/s and 10 Gb/s for a four pair differential micro-strip configuration.

Dielectric thickness(um)	Dielectric constant	Data rate(Gb/s)	Jitter(ps)	Eye Height (V)
18	3.5	5	1.95	0.88
50	3.5	5	3.91	0.86
18	3.5	10	3.9	0.81
50	3.5	10	15.1	0.83

simulations of single ended and differential bus configurations was done at different data rates to highlight the performance improvements achievable by using embedded planar capacitors. The improvements were quantified by comparing the eye diagrams and SSN for the different cases. Tables 14 and 15 capture the improvement in performance of the system applications by using different embedded capacitors.

CHAPTER VI

CONCLUSION AND FUTURE WORK

The increase in clock frequency and power dissipation of processors has put stringent requirements on the design of power distribution networks. The simultaneous switching of output drivers or logic circuits of a microprocessors generate noise that can deteriorate the performance of sensitive circuits. A large noise spike close to the operating frequency of the device can de-sensitize the circuit and destroy its functionality. Charge must be provided with the least amount of inductance to prevent any malfunctioning of the circuits. To do this, target impedances in the order of sub milli-ohms have to be met over a frequency range that spans from DC to multiples of chip operating frequency. A case for using embedded capacitors in the package to decouple core logic in the mid-band frequency from 100 MHz to 2 GHz for processors has been shown in this thesis.

Individual embedded capacitors developed on the hydrothermal process at PRC and at DuPont were measured, modeled, and characterized. The benefits of using the individual sized capacitors can be made based on decoupling implications for a digital package using the System on Package approach, with no board but only the package as the system.

In a digital package using the SOP concept, the power supplied is from within the package because of the absence of the board. This is advantageous from a decoupling perspective because the inductive effects of the board are removed. However bringing the voltage supply closer the active circuits (chip) does not imply that all the charge can be provided from the power supply at all frequencies of operation as explained in the following paragraph. The VRM is connected to the power supply and converts

one DC voltage level to another. It senses the voltage near the load and adjusts the output current to regulate the load voltage. The VRM consists of a switching regulator that charges and discharges based on the voltage sensed at the load. The rate of switching of the regulator depends on the rate of change of the load voltage. Therefore, even if we were to place the VRMs right next to the active circuits, the switching regulators would need to operate at a very high frequency (100s of MHz to the GHz) range to be able to satisfy the decoupling requirements of circuits operating at that frequency. The VRM on the board with today's technology is effective only from 1 KHz to hundreds of KHz. However, the placement of the VRM on the package would extend its operation to the lower 10's of MHz region (because of the reduced inductance effects) minimizing the need for some of the high value capacitors that were placed on the board. Decoupling also needs to be provided from the 10's of MHz region to multiples of chip operating frequency. For frequencies above 1 GHz on-chip decoupling capacitors is used since high capacitance values in the order of 100's of nF are required to decouple in the high MHz region which reduces the real estate available for logic circuitry. Therefore, the frequency band from the MHz to the GHz region has to be decoupled from the package.

With such a SOP scenario there a variety of decoupling options as listed below: 1) Low inductance surface mount individual capacitors can be placed on the surface of the package to target frequencies that cannot be met by using VRMs. Since they are spread horizontally on the package and away from the processor the inductive loop associated with the current flow of the capacitors will prevent them from targeting higher frequency bands. To target frequencies in the region of 100s of MHz, the loop inductance would further need to be reduced and this can be achieved by placing the charge carriers closer to the active circuits. 2) SMD individual capacitors can be embedded but the frequency band that can be targeted is limited because of the limited real estate under the die shadow. 3) A capacitance interposer between the

chip and the package can be used. The routing of the signal traces is an issue since they would need to pass through a high K dielectric material increasing the coupling between the signal trace and the capacitor layers. The signal traces can be shielded by placing low k dielectric materials around them. 4) A thin high K dielectric capacitor layer with dimensions equal to the die shadow can be placed in one of the package layers. The drawback of this approach is that the bandwidth that can be targeted with this lumped capacitor with different number of via pairs is small compared to the bandwidth obtainable with an array of capacitors as shown in Fig. 129. 5) The required frequency band in the 100s of MHz to the GHz range can be targeted by embedding thin film variable sized capacitors within the package.

Based on the models developed in this thesis , an array of embedded capacitors within the package was proposed to meet a target impedance of 2 mohms to decouple active circuits in the mid-band frequency range of 100 MHz - 2 GHz. The performance comparison of a single capacitor the size of a die shadow was done with an array of capacitors. The simulation results of the comparison are shown in Fig. 129, which shows the impedance profile of an array of capacitors as compared to a single capacitor of size 10 mm a side with 68 via pairs attached to it. The difference in the frequency band that can be targeted is clearly observed from the resultant simulation.

An investigation into the performance improvements of I/O decoupling using embedded planar capacitors was conducted in this thesis. A test vehicle was designed, fabricated, and measured to quantify the plane to plane noise waveforms. Plane bounce represents the potential variation between the voltage and the ground nodes across the surface of the planes. Models of the transmission lines were developed based on modal decomposition and were coupled with the power-ground plane models. Model to measurement correlation was obtained for the SSN as well as the isolation between the signal trace and the power-ground planes for different dielectric thicknesses of the embedded capacitors. The modeling methodology accounted for

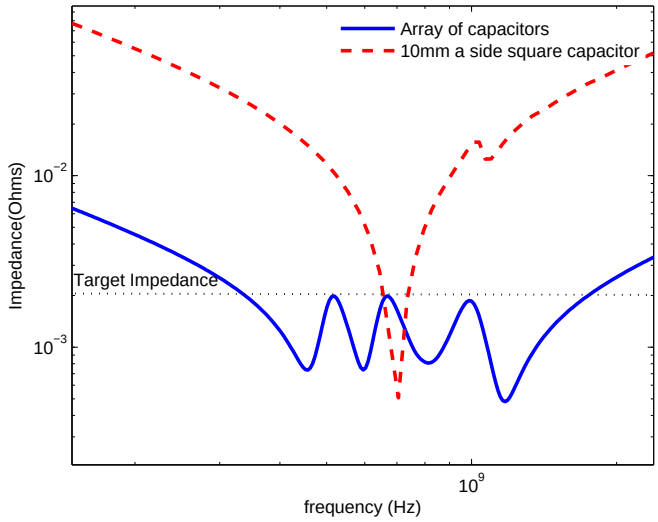


Figure 129: Impedance profile comparison of an array of capacitors and a single 10mm X 10mm capacitor with 68 via pairs.

via transitions and return currents on the planes.

The power dissipation trends of microprocessors was captured through the technology nodes. The different components were analyzed based on the ITRS numbers. The multi-core processor concept was introduced to improve performance by reducing the total power dissipation and increasing the off-chip bandwidth of processors. Although, a reduction in the total power dissipation increases the core target impedance that has to be met by a PDN, the number of high speed I/Os that need to be decoupled is increased. Therefore, I/O decoupling would be a major issue that needs to be addressed for future packages. The design complexity for core PDNs would increase because of the reduced real estate available for decoupling in packages.

A list of the relevant publications is listed below-

1. **Prathap Muthana**, Madhavan Swaminathan, Ege Engin, P.M. Raj, Rao Tummala, "Mid-Frequency Decoupling using Embedded Decoupling Capacitors." Electrical Performance of Electronic Packaging, Oct 24-26, 2005, Page(s)271-274.

2. **Prathap Muthana**, Madhavan Swaminathan, Rao Tummala, V.Sundaram, Lixi Wan, S.K. Bhattacharya, P.M. Raj, "Packaging of Multi-Core processors: Trade-off's and Potential Solutions." Electronic Components and Technology Conference, May31-June3, 2005, Vol2, Page(s) 1895-1903.

3. **Prathap Muthana**, Madhavan Swaminathan, Ege Engin, Rao Tummala, P.M.Raj, Lixi Wan, D. Balaraman, S.Bhattacharya, "Design, Modeling and Characterization of Embedded Capacitor Networks for Mid-Frequency Decoupling in Semiconductor Systems." Electromagnetic Compatibility, August 2005, Page(s)638-643.

4. **Prathap Muthana**, Ege Engin, Madhavan Swaminathan, Rao Tummala, Venkatesh Sundaram, Lixi Wan, S.K Bhattacharya, P.M. Raj, K.J. Lee, Mahesh Vardarajan, Isaac Robin Abothu, "Measurement, Modeling and Characterization of Embedded Capacitors for Power Delivery in the Mid Frequency Range." IMAPS, 2005.

5. **Prathap Muthana**, Erdem Matoglu, Nam Pham, Daniel N de Araujo, Bhyrav Mutnury, Moises Cases and Madhavan Swaminathan, "Analysis of Embedded Package Capacitors for High Performance Components." EPEP, 2006.

6. **Prathap Muthana**, Krishna Srinvasan, Ege Engin, Madhavan Swaminathan, Rao Tummala, Daniel Amey, Karl Dietz and Sounak Banerji, "I/O decoupling in High Speed Packages Using Embedded Planar Capacitors." Accepted for publication at ECTC 2007.

7. **Prathap Muthana**, Ege Engin, Madhavan Swaminathan, P.M. Raj, Rao Tummala, Venkatesh Sundaram, Daniel Amey, Karl Dietz, Sounak Banerji, M. Cases, "Design Modeling and Characterization of Embedded Capacitors for Decoupling Applications." Proceedings of IBM Center for Advance Studies Conference Feb 2006.

8. **Prathap Muthana**, Ege Engin, Madhavan Swaminathan, Venkatesh Sundaram, P.Markondeya Raj, Daniel Amey, Karl Dietz, Sounak Banerji and Rao Tummala, "Design, Modeling and Characterization of Embedded Capacitor Networks in the Mid-Band Frequency Range". Accepted for publication in IEEE Transactions on Advanced Packaging.

9. **Prathap Muthana**, Krishna Srinivasan, Ege Engin, Madhavan Swaminathan, Venkatesh Sundaram, Daniel Amey, Karl Dietz, Sounak Banerji and Rao Tummala, "Improvements in Noise Suppression for I/O circuits Using Embedded Planar Capacitors". Submitted for publication in IEEE Transactions on Advanced Packaging.

10. P.Markondeya Raj, **Prathap Muthana**, T.Danny Xiao, Lixi Wan, Devarajan Balaraman, Isaac Robin Abothu, Swapan Bhattacharya, Madhavan Swaminathan and Rao Tummala, "Magnetic Nanocomposites for Organic Compatible Miniaturized Antennas and Inductors." Advanced Packaging Materials: Processes, Properties and Interfaces, 2005, 16-18 March, Page(s)272-275.

11. Krishna Srinivasan, **Prathap Muthana**, R.Manderaker, E.Engin, J. Choi and M.Swaminathan, "Enhancement of Signal Integrity and Power Integrity with Embedded Capacitors in High Speed Packages" ISQED 2006.

12. Lixi Wan, **Prathap Muthana**, D.Balaraman, P.M.Raj, S.K. Bhattacharya, M.

Vardarajan, I.R. Abothu, M.Swaminathan and Rao Tummala, "Embedded Decoupling Capacitor Performance in High Speed Circuits." ECTC 2005, page(s)1617-1622. Vol 2.

13. Lee, K.J.; Bhattacharya, S.; Varadarajan, M.; Lixi Wan; Abothu, I.R.; Sundaram, V.; **Muthana, P**; Balaraman, D.; Raj, P.M.; Swaminathan, M.; Sitaraman, S.; Tummala, R.; Viswanadham, P.; Dunford, S.; Lauffer, J."Design, fabrication, and reliability assessment of embedded resistors and capacitors on multilayered organic substrates." Advanced Packaging Materials: Processes, Properties and Interfaces, 2005. Proceedings. International Symposium on 16-18 March 2005 Page(s):249 - 254.

14. Christian Schuster, Young Kwark, Giuseppe Selli and **Prathap Muthana**,"Developing a Physical Model for Vias." DesignCon 2006.

A list of the patents that were filed as a result of this work are listed below:

Prathap Muthana, M. Swaminathan, A. E. Engin, and L. Wan, "A package having an array of embedded capacitors for power delivery and decoupling in the mid-frequency range and methods of forming thereof - United States Patent Application: $EL0624USNA$, " August 31, 2006.

Prathap Muthana, A.E. Engin, M. Swaminathan, and K. Srinivasan, "A package having an array of embedded capacitors for power delivery and decoupling of high speed input/output circuit and methods of forming thereof - United States Patent Application: $EL0629USNA$, " August 31, 2006

As a continuation of the work described in this thesis, the following areas of study may be considered.

(*a*) Design, fabrication, and characterization of a prototype with an array of individual embedded capacitors. The performance benefits in the time and frequency domain were highlighted for an array of individual sized embedded package capacitors through simulations. The fabrication of an actual prototype which could be used for performance verifications would aid in optimizing the design of the array and also aid in developing measurement methodologies to characterize such a complex structure.

(*b*) A re-workable design of the embedded capacitor array that could be used for successive generations of processors. Since the power requirements of processors would change through technology nodes, which translates into different decoupling requirements. A re-workable design and fabrication methodology that could be used through successive product generations would be beneficial in time and cost savings.

APPENDIX A

SIMULATION RESULTS FOR INTEL FRONT SIDE BUS (FSB) AT 1 GBIT/S

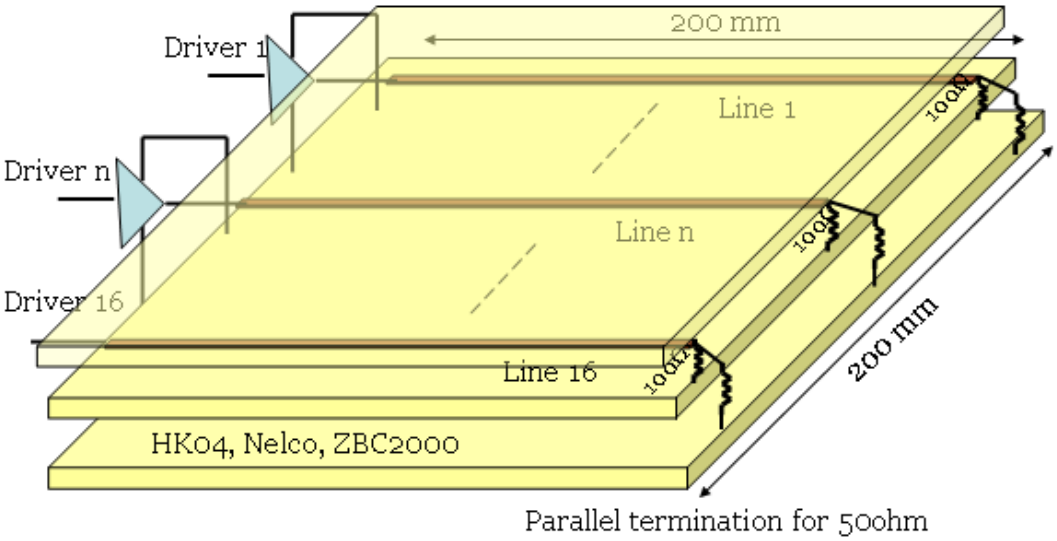


Figure 130: The simulation set up for a 16 bit intel FSB.

Table 16: Summary of the results of the 16 bit INTEL FSB simulations

Dielectric Thickness	SSN peak to peak magnitude (mV)
8 um (HK04)	237
12 um (HK04)	414
18 um (HK04)	445
25 um (HK04)	489
50 um (ZBC2000)	968
50 um (NelcoBC)	980
50 um (NelcoBC) + 100 decaps	695

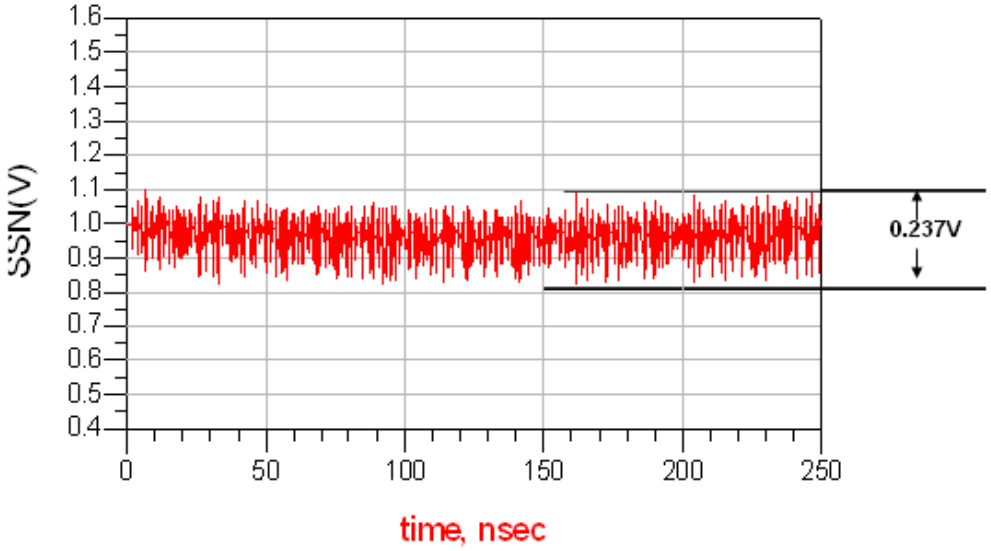


Figure 131: SSN for a 8 um thick dielectric.

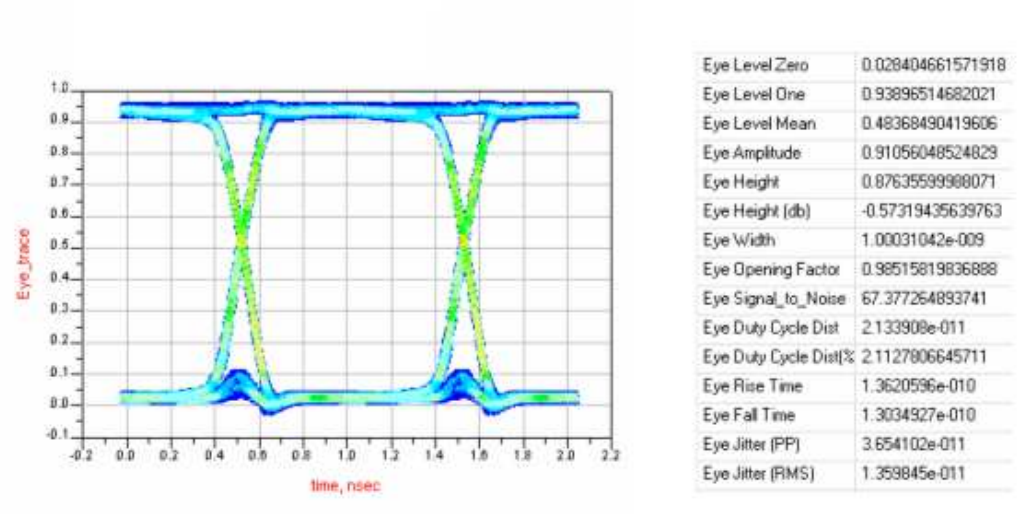


Figure 132: Eye diagram for a 8 um thick dielectric.

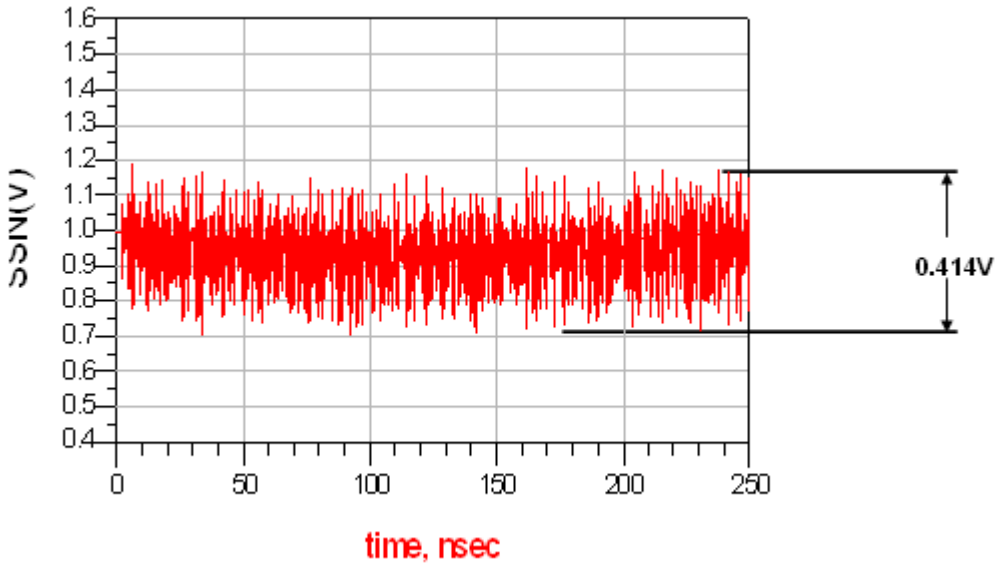


Figure 133: SSN for a 12 um thick dielectric.

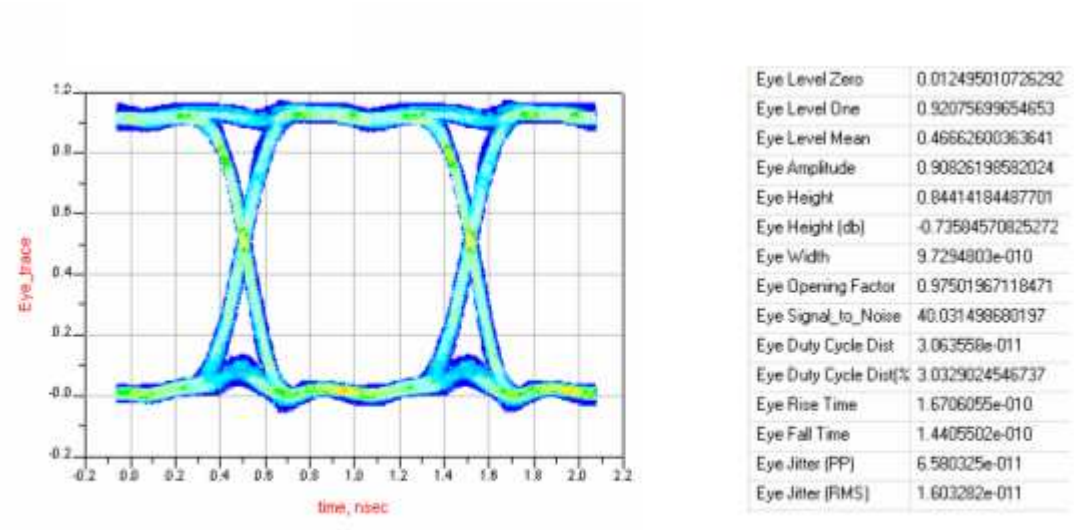


Figure 134: Eye diagram for a 12 um thick dielectric.

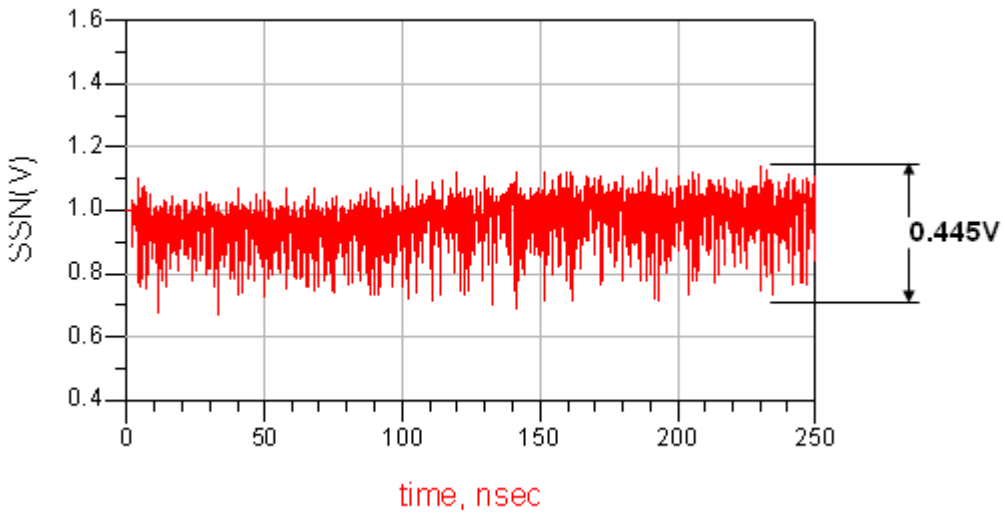


Figure 135: SSN for a 18 um thick dielectric.

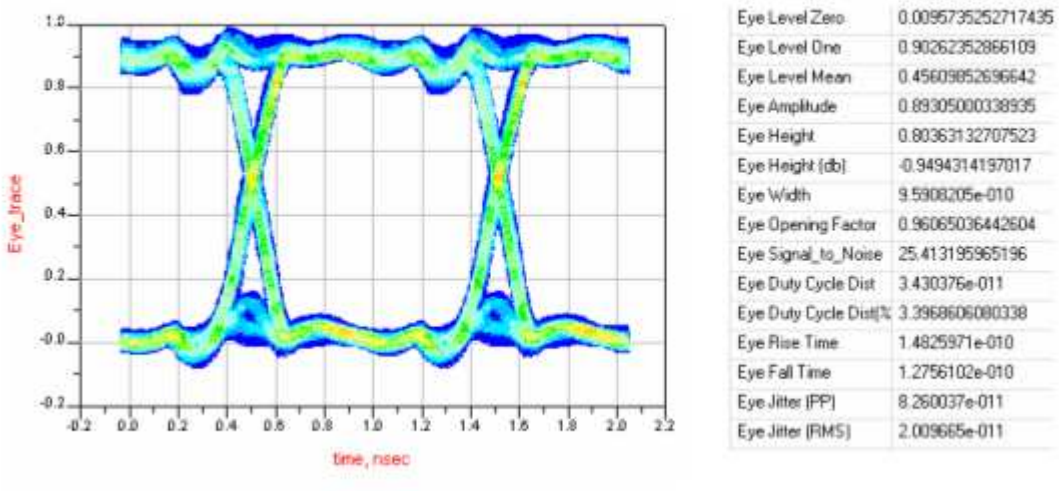


Figure 136: Eye diagram for a 18 um thick dielectric.

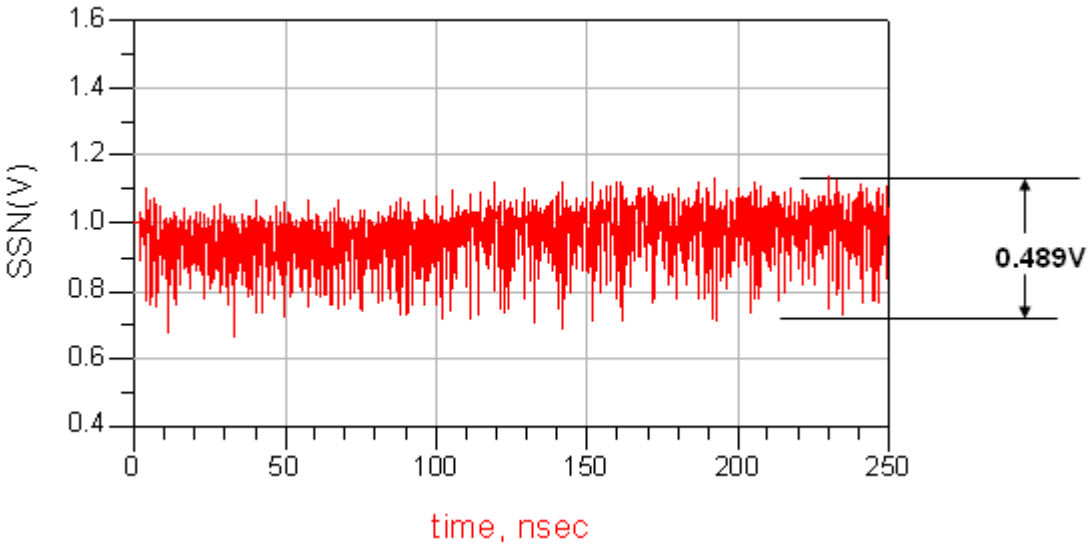


Figure 137: SSN for a 25 um thick dielectric.

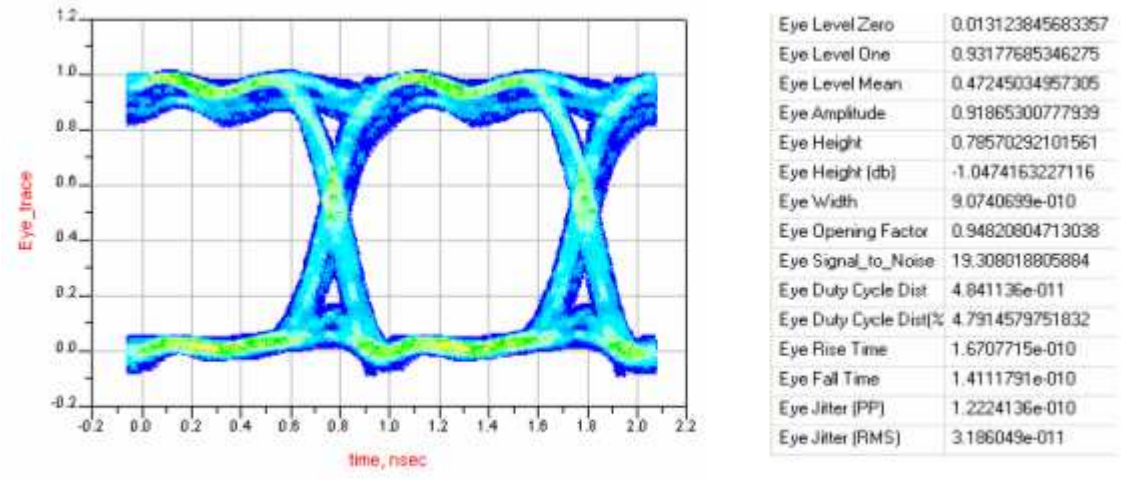


Figure 138: Eye diagram for a 25 um thick dielectric.

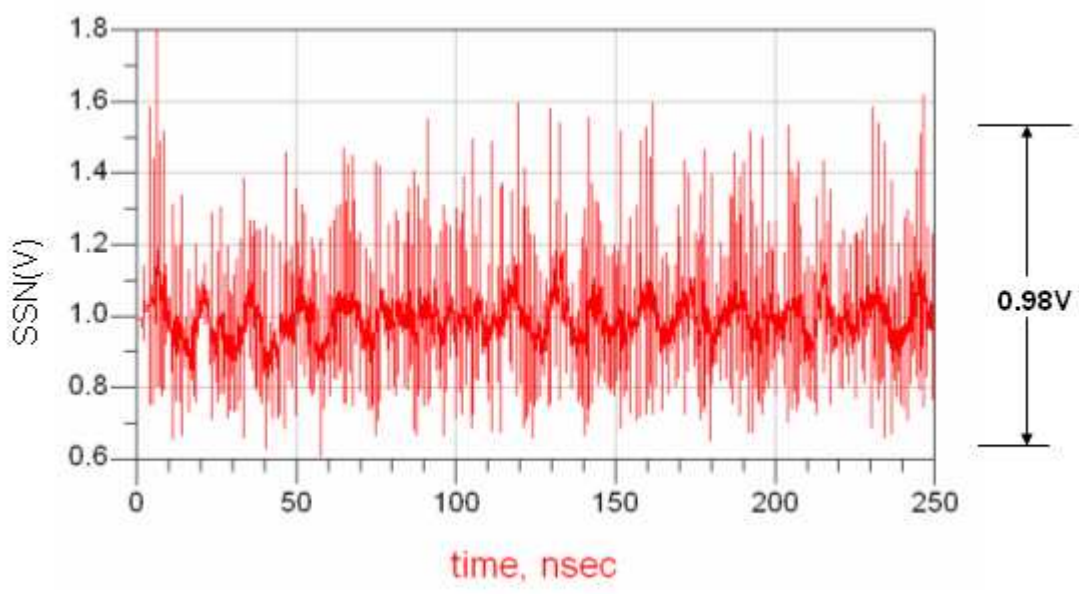
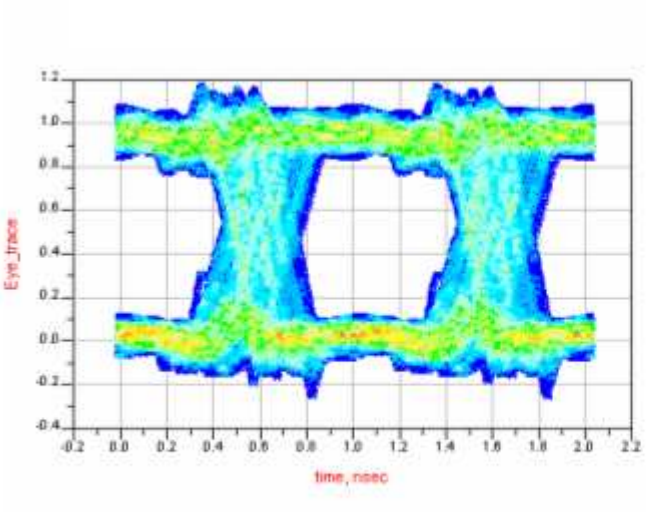


Figure 139: SSN for a 50 um thick dielectric with a dielectric constant of 3.5.



Eye Level Zero	0.028224677524328
Eye Level One	0.95158755719397
Eye Level Mean	0.48990611735915
Eye Amplitude	0.92336287966964
Eye Height	0.69698676723109
Eye Height (db)	-1.5677546720052
Eye Width	6.7932775e-010
Eye Opening Factor	0.91547991289601
Eye Signal_to_Noise	11.831506973835
Eye Duty Cycle Dist	5.359928e-011
Eye Duty Cycle Dist(%	5.3002087004266
Eye Rise Time	1.616792e-010
Eye Fall Time	1.3726336e-010
Eye Jitter (PP)	3.3060617e-010
Eye Jitter (RMS)	8.819297e-011

Figure 140: Eye diagram for a 50 um thick dielectric with a dielectric constant of 3.5.

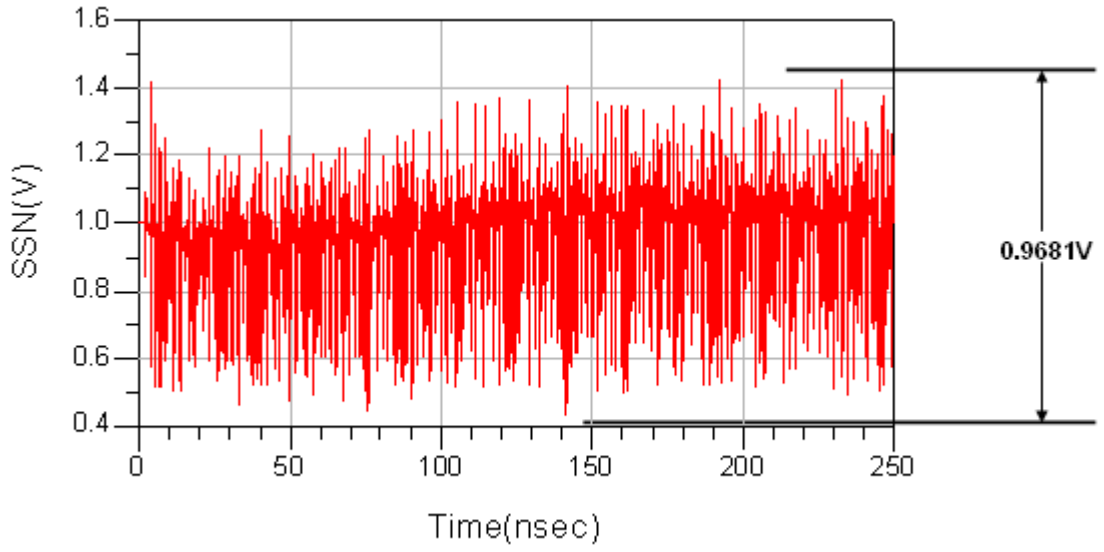


Figure 141: SSN for an 50 um thick dielectric with a dielectric constant of 4.2.

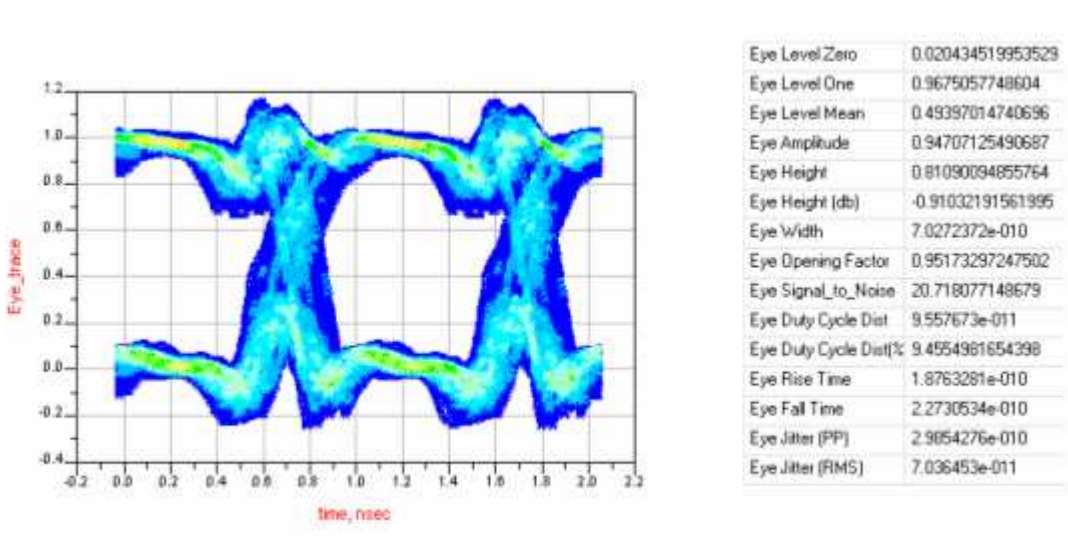


Figure 142: Eye diagram for a 50 um thick dielectric with a dielectric constant of 4.2.

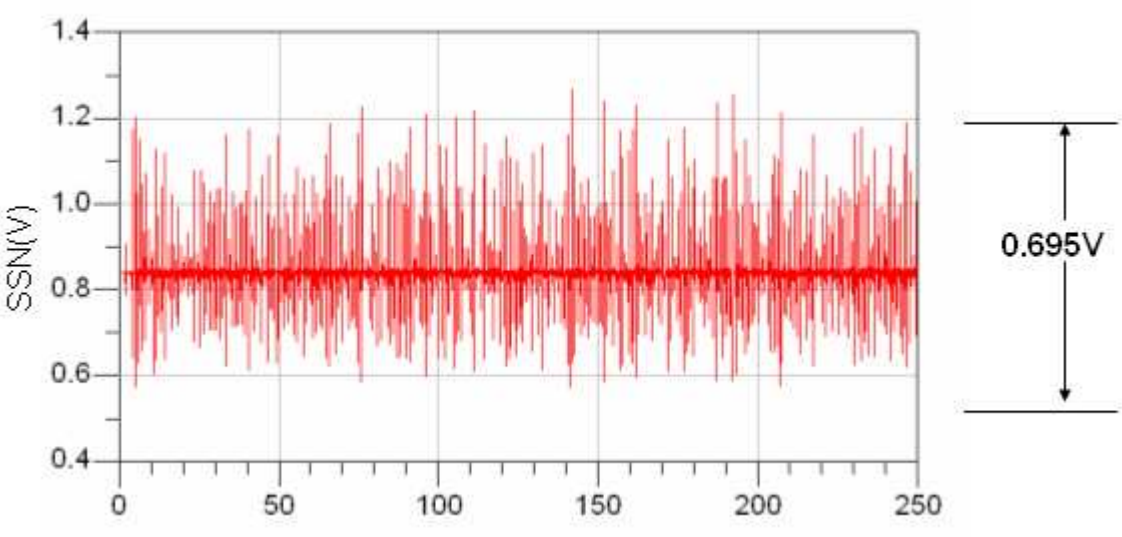
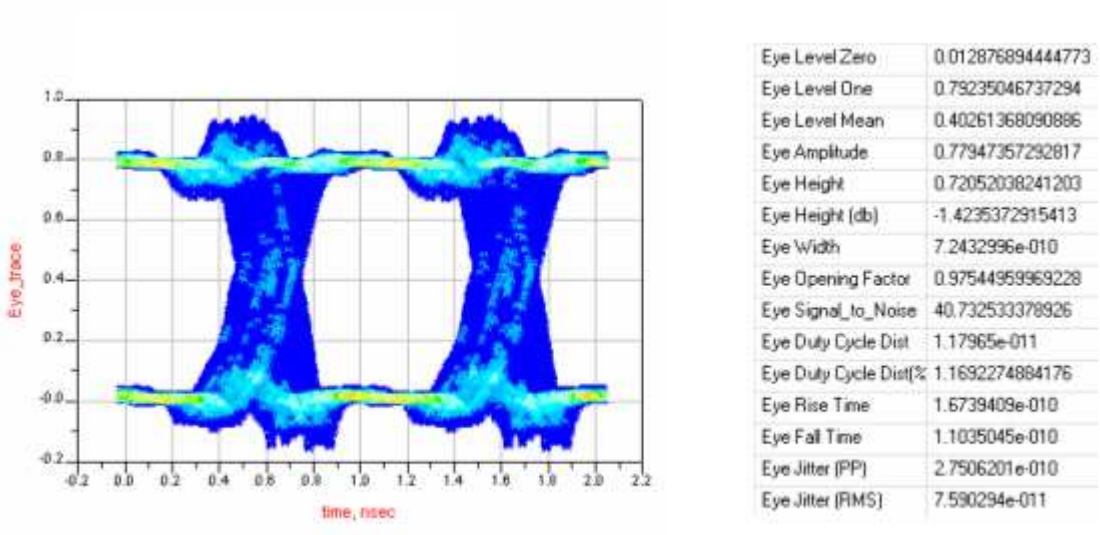


Figure 143: SSN for a 50 um thick dielectric with a dielectric constant of 3.5 with 100 decoupling capacitors (C = 100 nf,ESR = 0.03Ω and ESL = 4 e-10H).



Eye Level Zero	0.012876894444773
Eye Level One	0.79235046737294
Eye Level Mean	0.40261368090886
Eye Amplitude	0.77947357292817
Eye Height	0.72052038241203
Eye Height (db)	-1.4235372915413
Eye Width	7.2432996e-010
Eye Opening Factor	0.97544959969228
Eye Signal_to_Noise	40.732533378926
Eye Duty Cycle Dist	1.17965e-011
Eye Duty Cycle Dist(%	1.1692274884176
Eye Rise Time	1.6739409e-010
Eye Fall Time	1.1035045e-010
Eye Jitter (PP)	2.7506201e-010
Eye Jitter (RMS)	7.590294e-011

Figure 144: Eye diagram for a 50 um thick dielectric with a dielectric constant of 3.5 with 100 decoupling capacitors (C = 100 nf,ESR = 0.03 Ω and ESL = 4 e-10 H).

APPENDIX B

SIMULATION RESULTS FOR PCI EXPRESS (PCIE) AT 5 GBIT/S

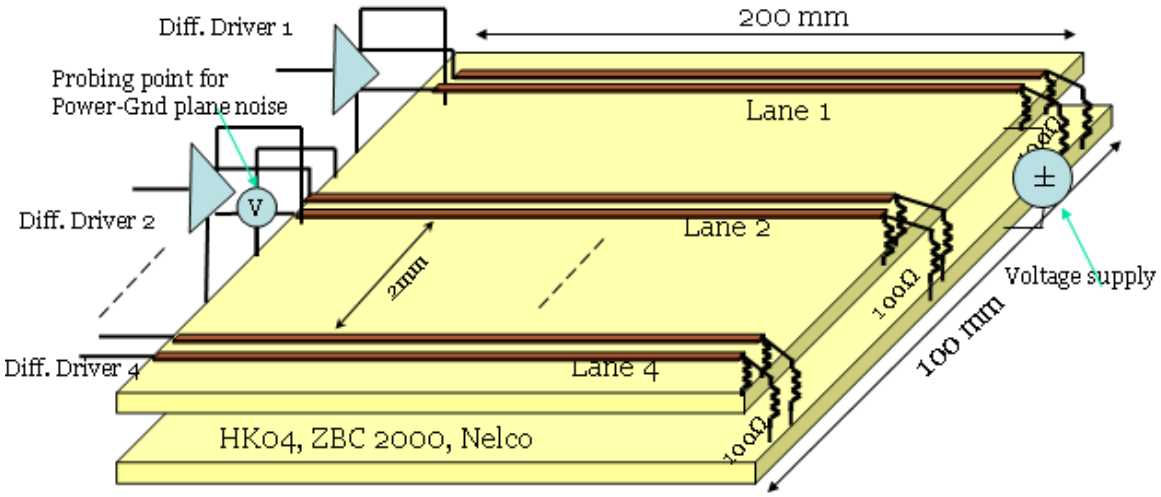


Figure 145: The simulation set up for the differential link simulations.

Table 17: Summary of the results for PCI Express simulations at 5 Gbit/s

Dielectric Thickness	SSN peak to peak magnitude (mV)
8 um (HK04)	8
12 um (HK04)	29.4
18 um (HK04)	89.5
25 um (HK04)	128
50 um (ZBC2000)	200
50 um (Nelco BC)	225

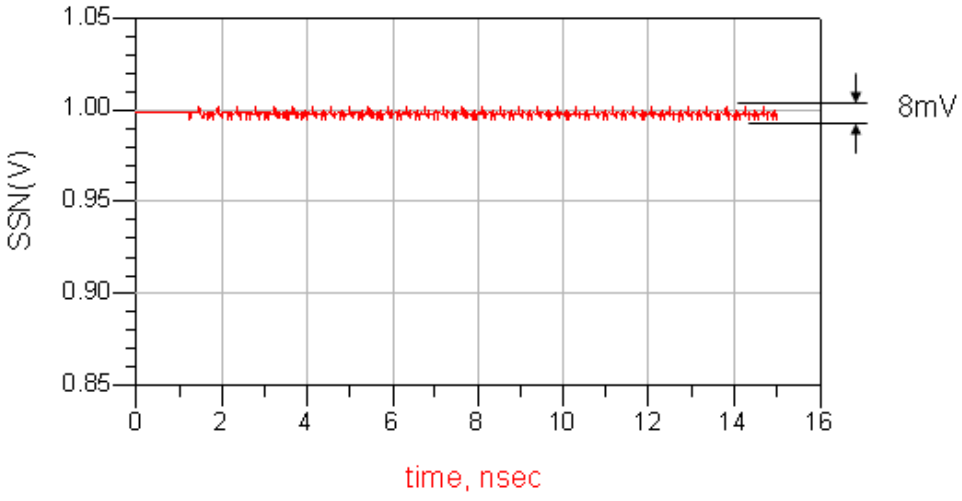


Figure 146: SSN for a differential link with a 8 um thick dielectric.

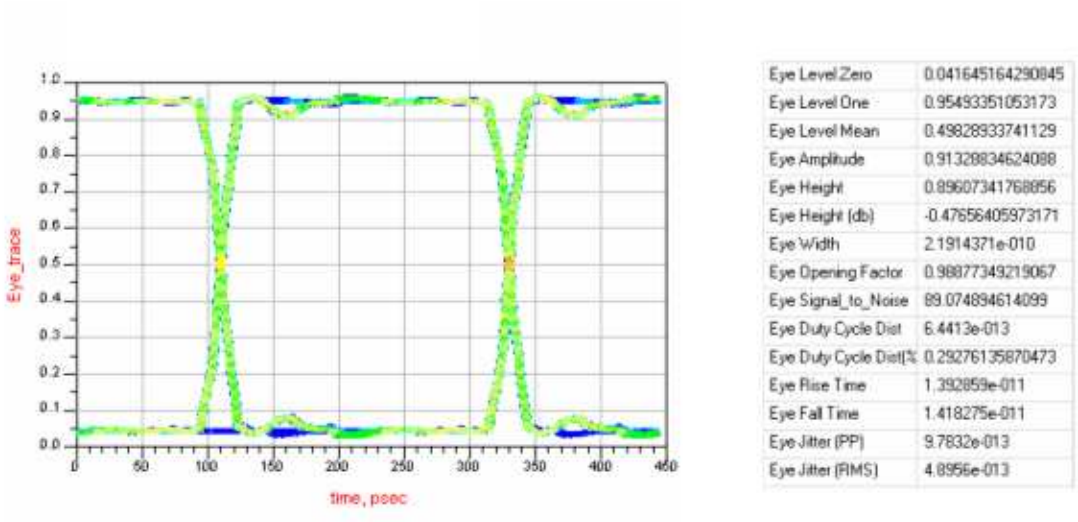


Figure 147: Eye diagram for a differential link with a 8 um thick dielectric.

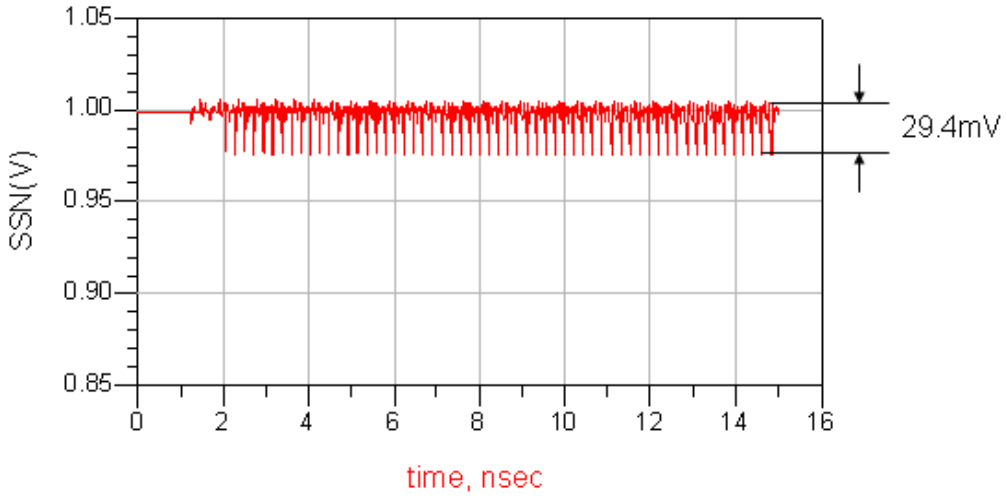
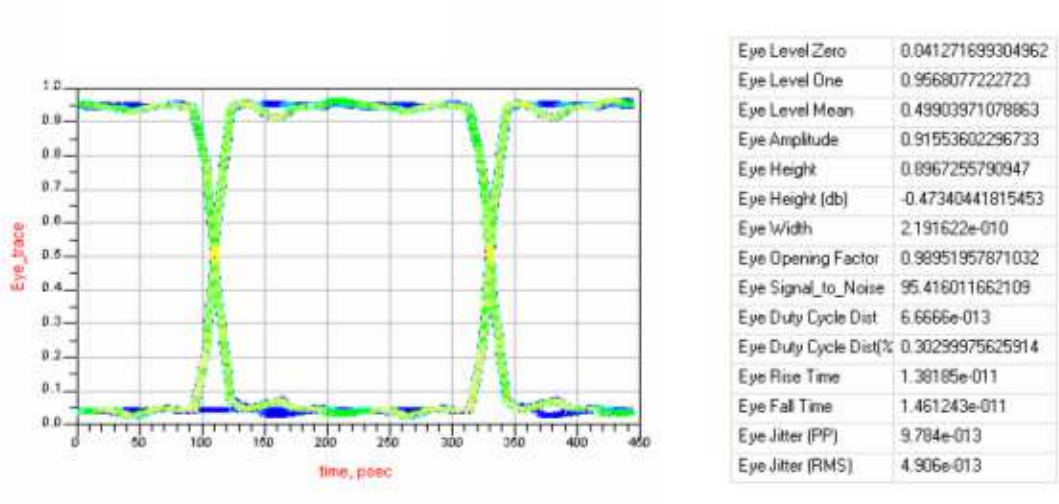


Figure 148: SSN for a differential link with a 12 um thick dielectric.



Eye Level Zero	0.041271699304962
Eye Level One	0.9568077222723
Eye Level Mean	0.49903971078863
Eye Amplitude	0.91553602296733
Eye Height	0.896725579094 7
Eye Height (db)	-0.47340441815453
Eye Width	2.191622e-010
Eye Opening Factor	0.98951957871032
Eye Signal_to_Noise	95.416011662109
Eye Duty Cycle Dist	6.6666e-013
Eye Duty Cycle Dist(%	0.30299975625914
Eye Rise Time	1.38185e-011
Eye Fall Time	1.461243e-011
Eye Jitter (PP)	9.784e-013
Eye Jitter (RMS)	4.906e-013

Figure 149: Eye diagram for a differential link with a 12 um thick dielectric.

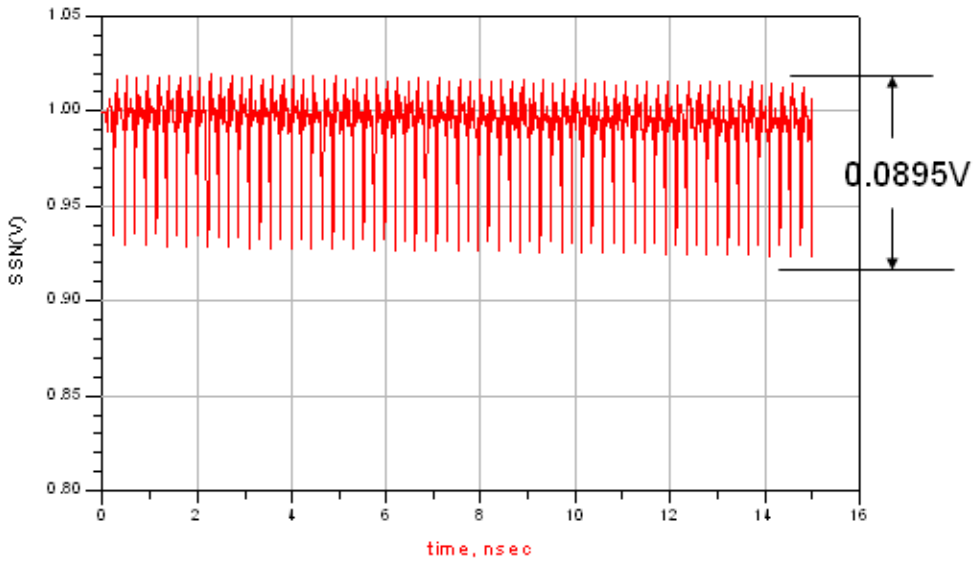
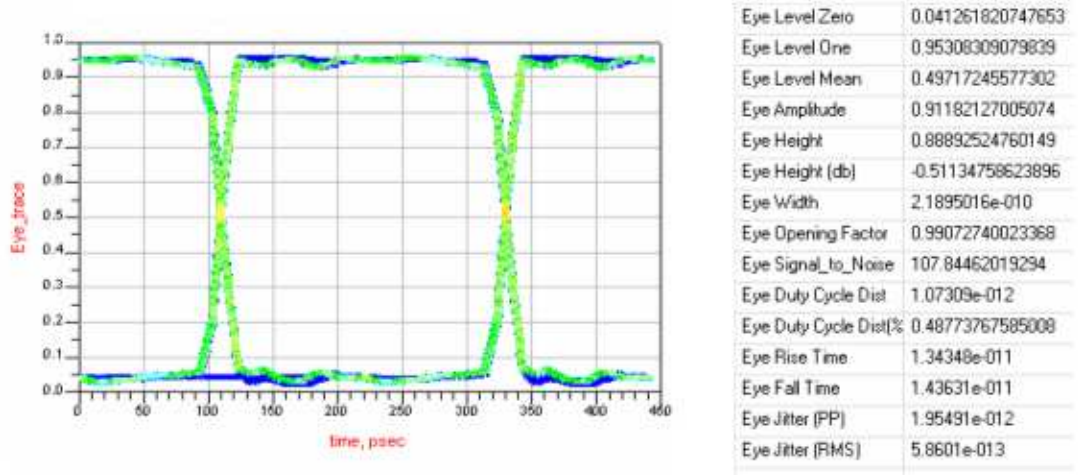


Figure 150: SSN for a differential link with a 18 um thick dielectric.



Eye Level Zero	0.041261820747653
Eye Level One	0.95308309079839
Eye Level Mean	0.49717245577302
Eye Amplitude	0.91182127005074
Eye Height	0.88892524760149
Eye Height (db)	-0.51134758623896
Eye Width	2.1895016e-010
Eye Opening Factor	0.99072740023368
Eye Signal_to_Noise	107.84462019294
Eye Duty Cycle Dist	1.07309e-012
Eye Duty Cycle Dist(%	0.48773767585008
Eye Rise Time	1.34348e-011
Eye Fall Time	1.43631e-011
Eye Jitter (PP)	1.95491e-012
Eye Jitter (RMS)	5.8601e-013

Figure 151: Eye diagram for a differential link with a 18 um thick dielectric.

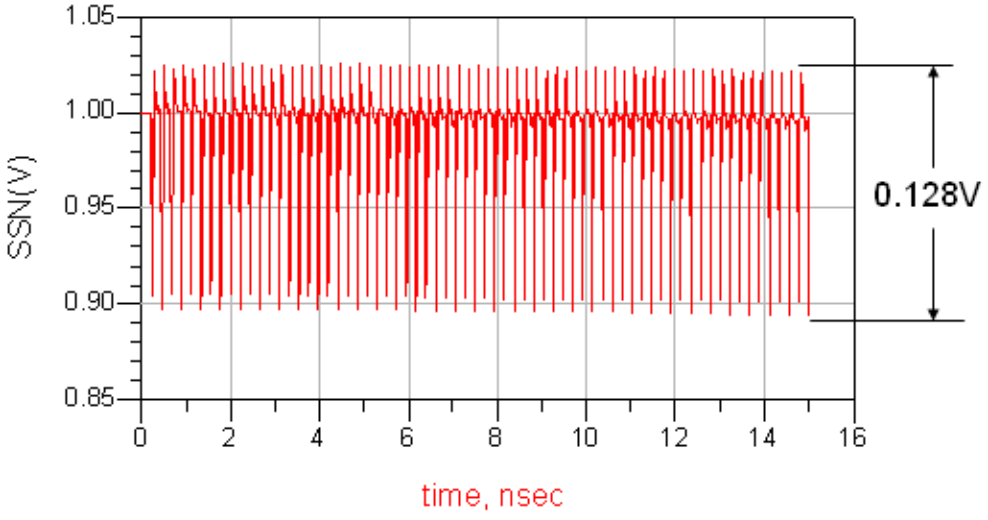


Figure 152: SSN for a differential link with a 25 um thick dielectric.

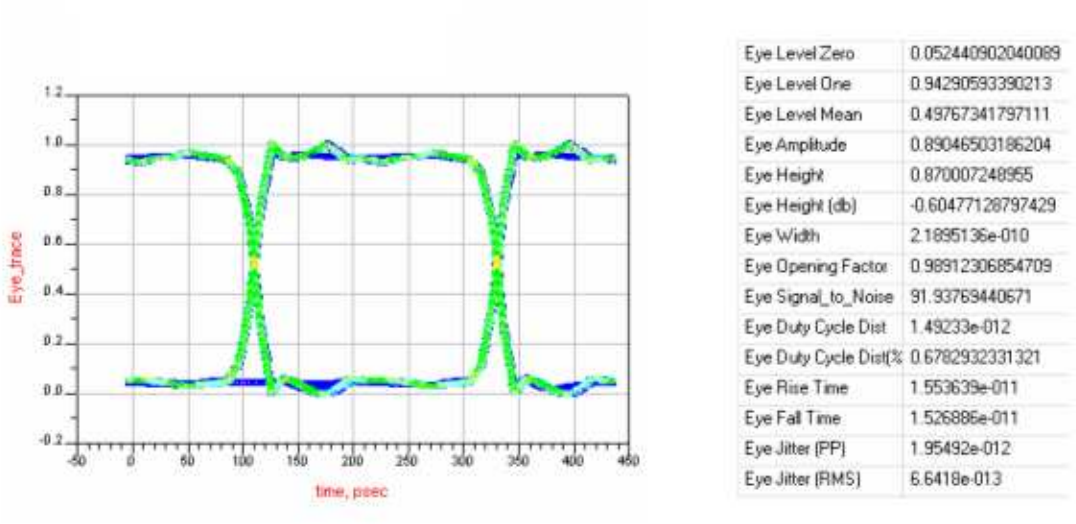


Figure 153: Eye diagram for a differential link with a 25 um thick dielectric.

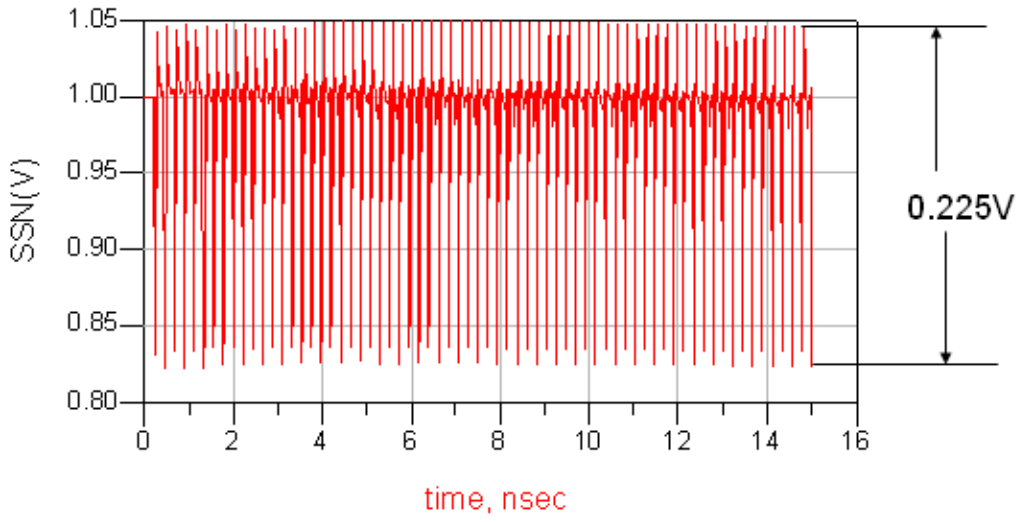


Figure 154: SSN for a differential link with a 50 um thick dielectric with a dielectric constant of 3.5.

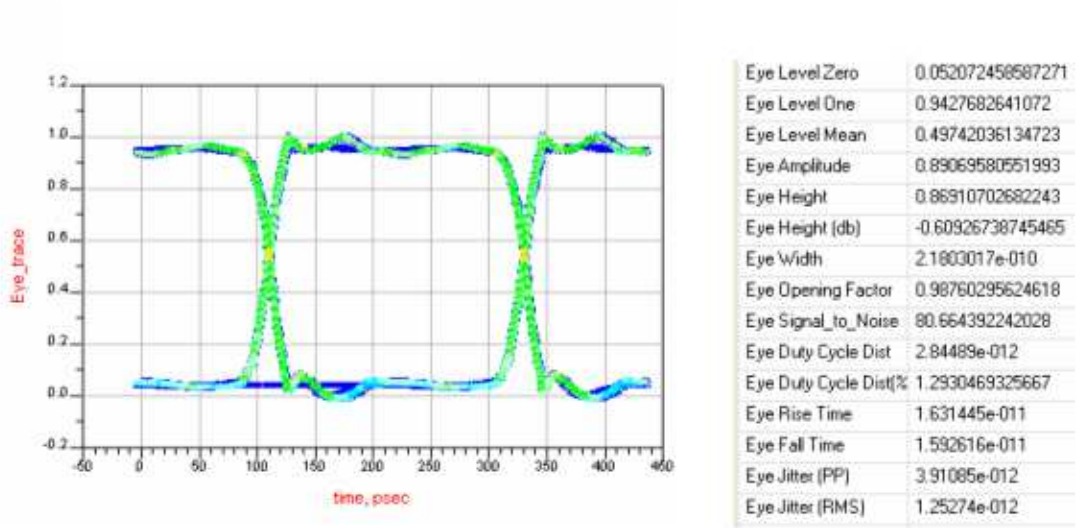


Figure 155: Eye diagram for a differential link with a 50 um thick dielectric with a dielectric constant of 3.5.

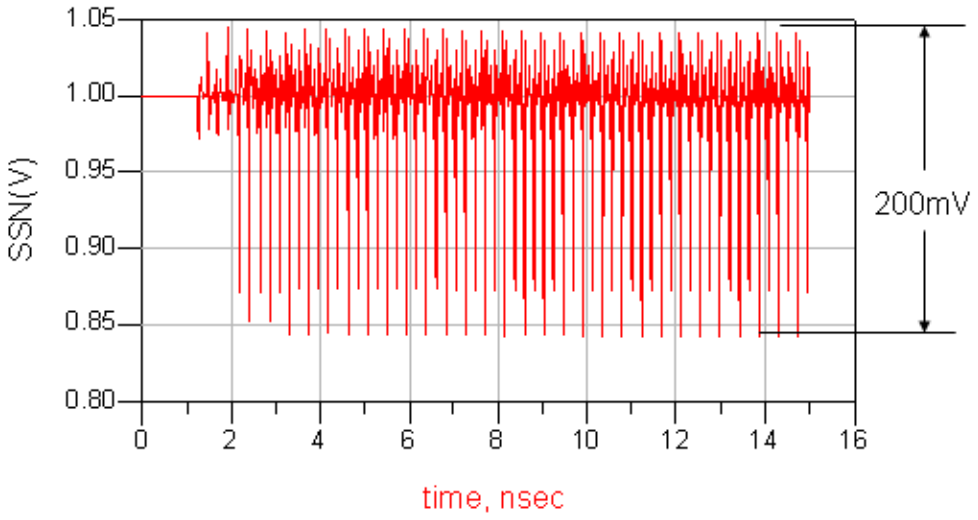
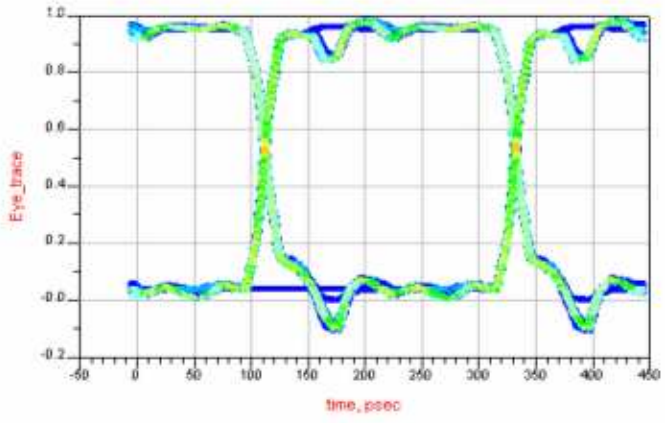


Figure 156: SSN for a differential link with a 50 um thick dielectric with a dielectric constant of 4.2.



Eye Level Zero	0.044922421555829
Eye Level One	0.95505877983549
Eye Level Mean	0.49999060069566
Eye Amplitude	0.91013635827966
Eye Height	0.84448387257983
Eye Height (db)	-0.73408639895775
Eye Width	2.1852757e-010
Eye Opening Factor	0.96527116305746
Eye Signal_to_Noise	28.794514531386
Eye Duty Cycle Dist	2.11497e-012
Eye Duty Cycle Dist(%	0.961230942086
Eye Rise Time	1.392877e-011
Eye Fall Time	1.642896e-011
Eye Jitter (PP)	5.98706e-012
Eye Jitter (RMS)	2.15042e-012

Figure 157: Eye diagram for a differential link with a 50 um thick dielectric with a dielectric constant of 4.2.

APPENDIX C

SIMULATION RESULTS FOR PCI EXPRESS (PCIE) AT 10 GBIT/S

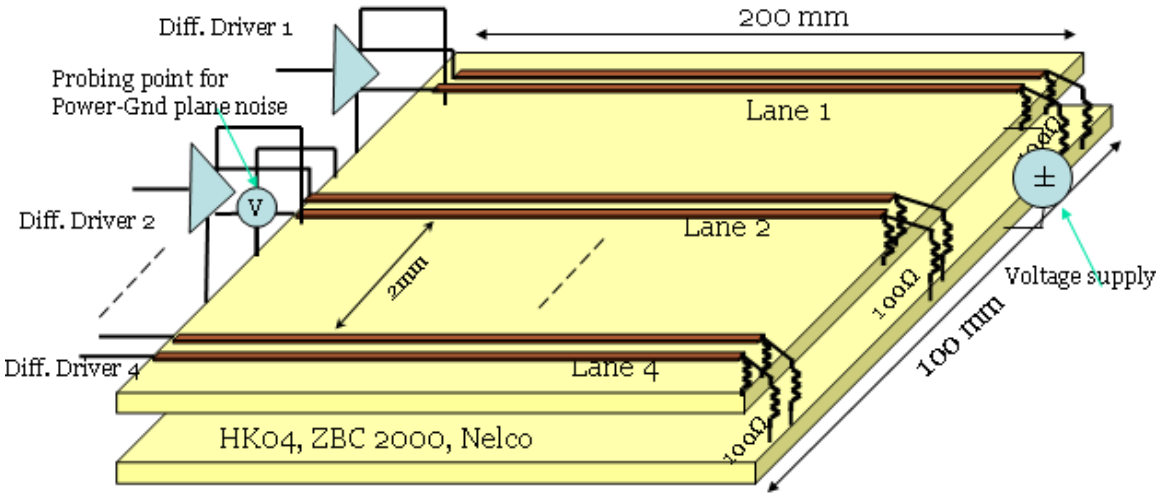


Figure 158: The simulation set up for the differential link simulations.

Table 18: Summary of the results for PCI Express simulations at 10 Gbit/s

Dielectric Thickness	SSN peak to peak magnitude (mV)
8 um (HK04)	44
12 um (HK04)	74.1
18 um (HK04)	106.5
25 um (HK04)	157
50 um (ZBC2000)	278.7
50 um (Nelco BC)	280

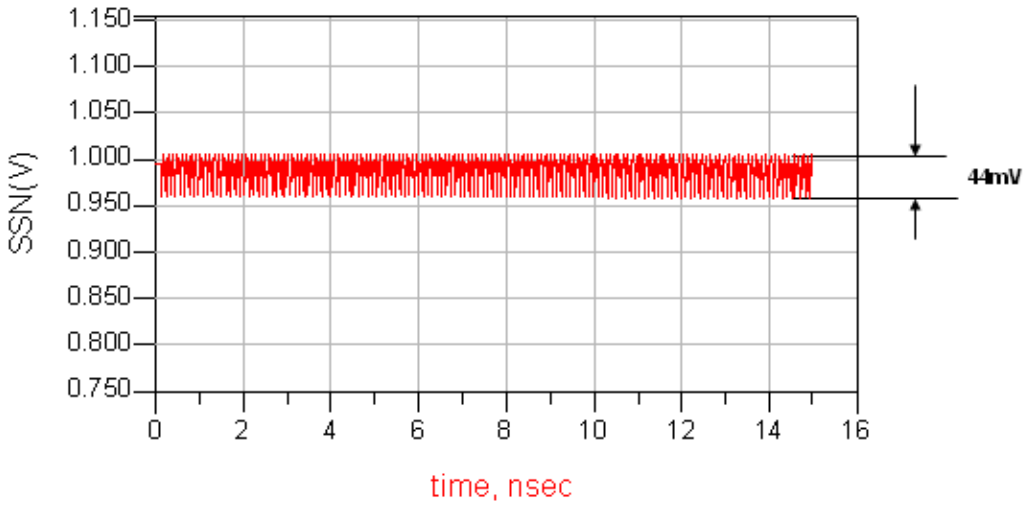


Figure 159: SSN for a differential link with a 8 um thick dielectric.

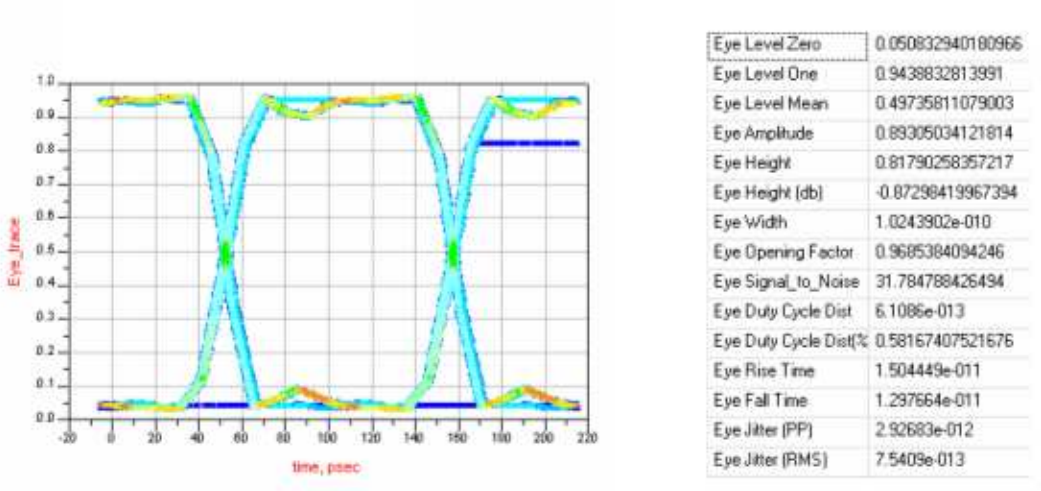


Figure 160: Eye diagram for a differential link with a 8 um thick dielectric.

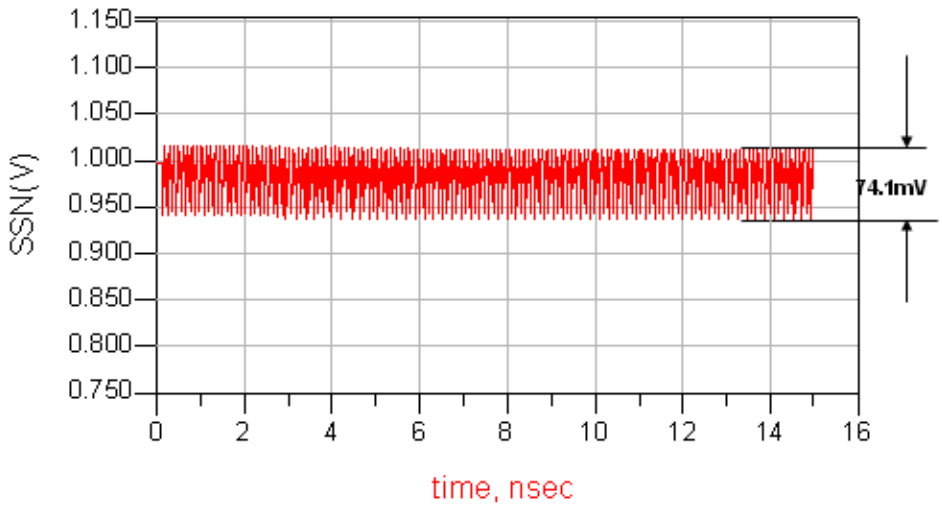
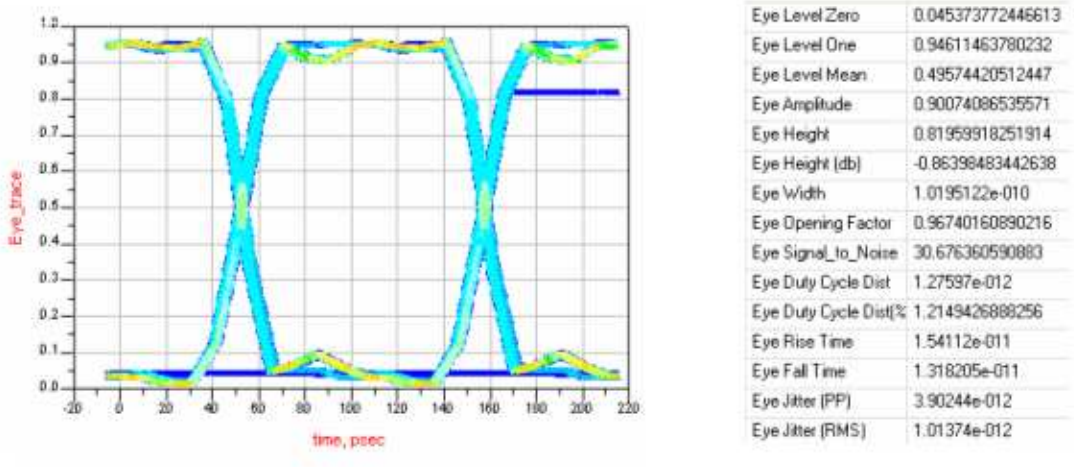


Figure 161: SSN for a differential link with a 12 um thick dielectric.



Eye Level Zero	0.045373772446613
Eye Level One	0.94611463780232
Eye Level Mean	0.49574420512447
Eye Amplitude	0.90074086535571
Eye Height	0.81959918251914
Eye Height (db)	-0.86398483442638
Eye Width	1.0195122e-010
Eye Opening Factor	0.96740160890216
Eye Signal_to_Noise	30.676360590883
Eye Duty Cycle Dist	1.27597e-012
Eye Duty Cycle Dist(%	1.2149426888256
Eye Rise Time	1.54112e-011
Eye Fall Time	1.318205e-011
Eye Jitter (PP)	3.90244e-012
Eye Jitter (RMS)	1.01374e-012

Figure 162: Eye diagram for a differential link with a 12 um thick dielectric.

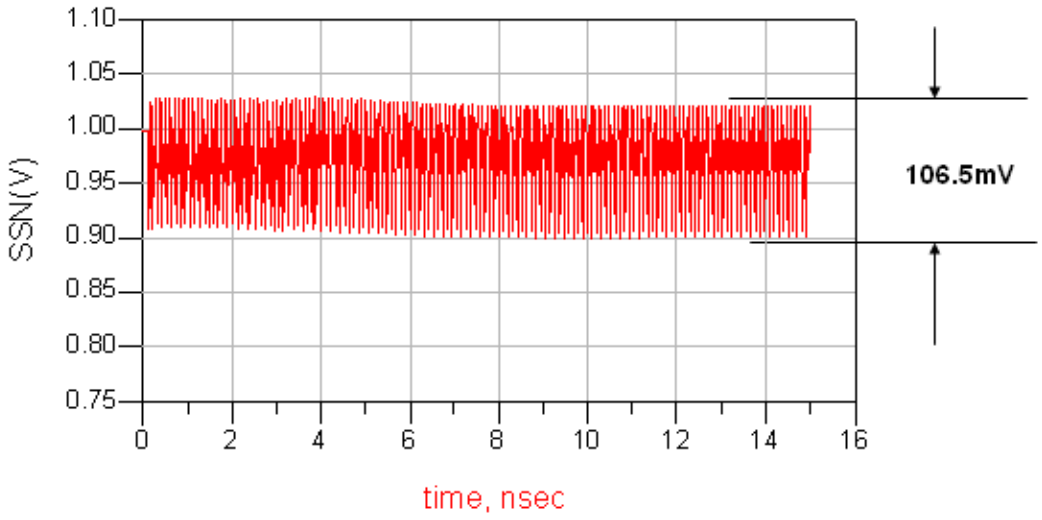


Figure 163: SSN for a differential link with a 18 um thick dielectric.

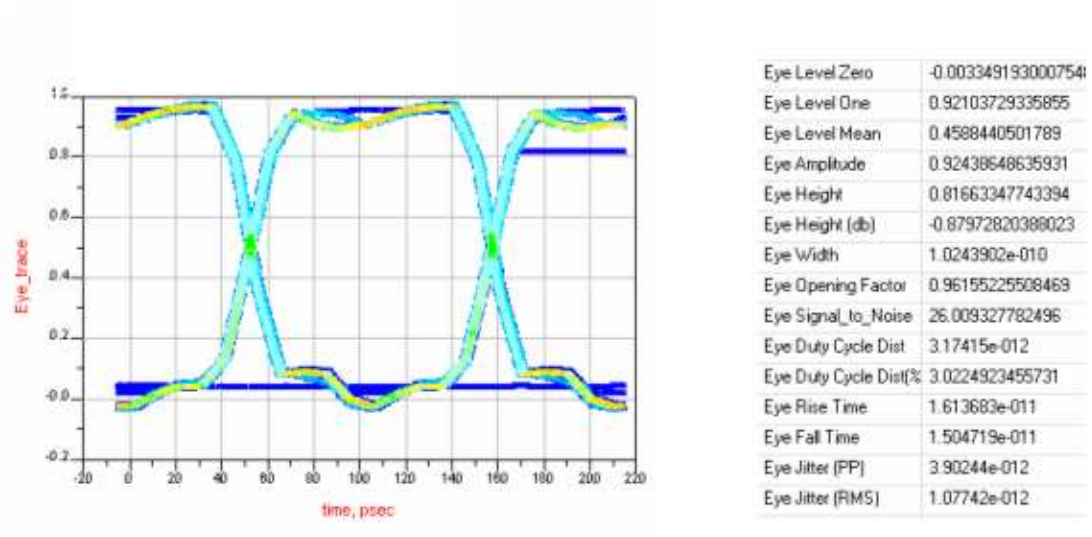


Figure 164: Eye diagram for a differential link with a 18 um thick dielectric.

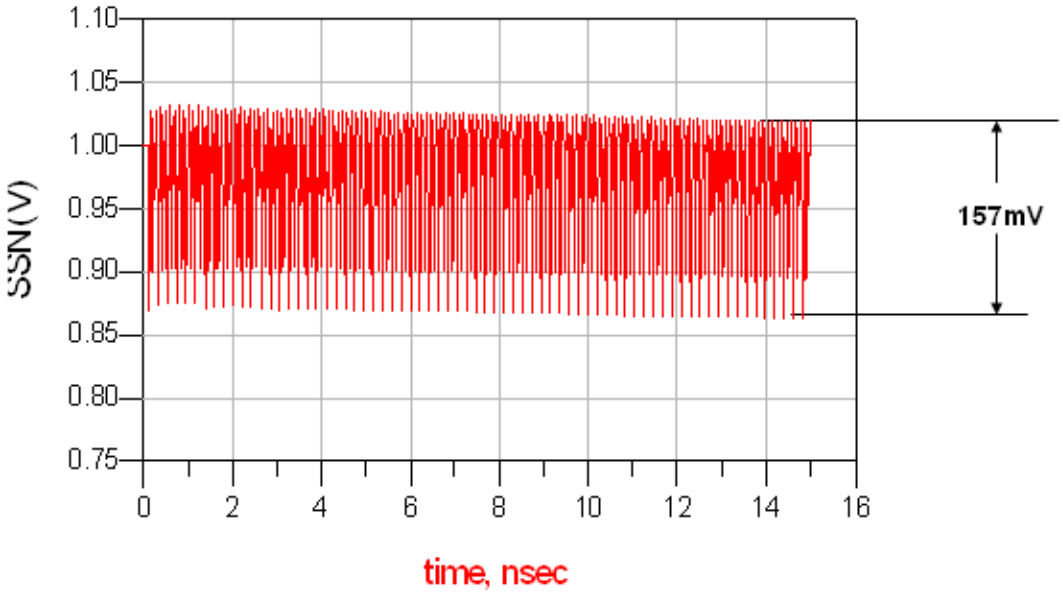


Figure 165: SSN for a differential link with a 25 um thick dielectric.

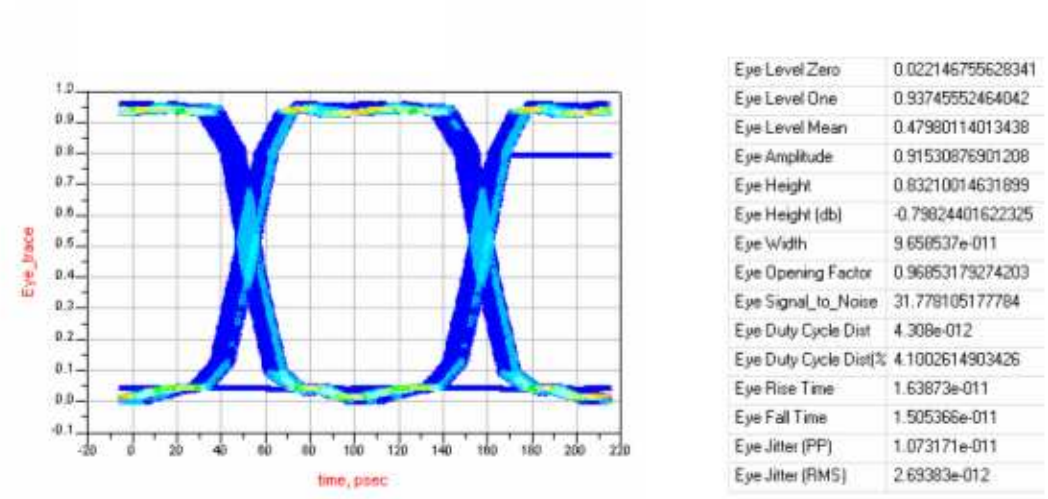


Figure 166: Eye diagram for a differential link with a 25 um thick dielectric.

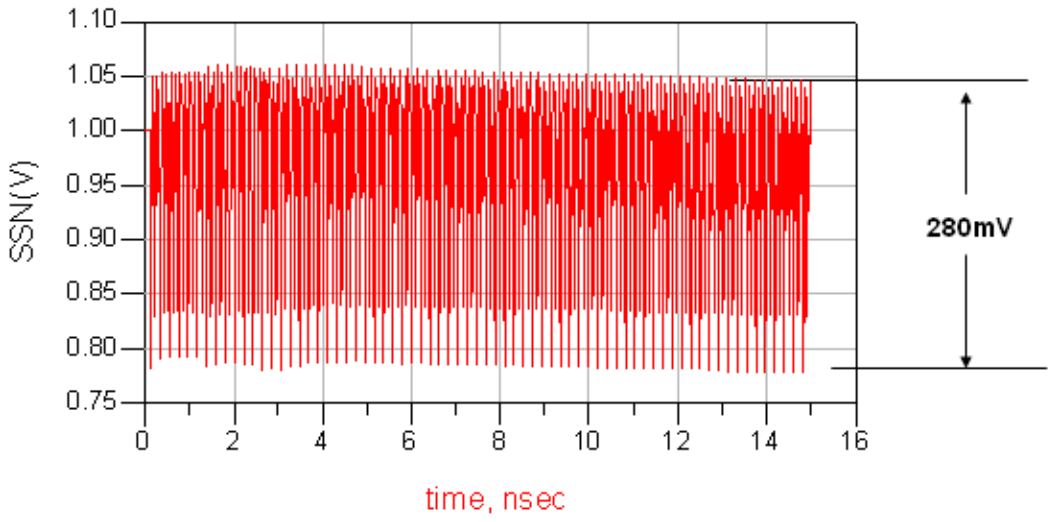


Figure 167: SSN for a differential link with a 50 um thick dielectric with a dielectric constant of 3.5.

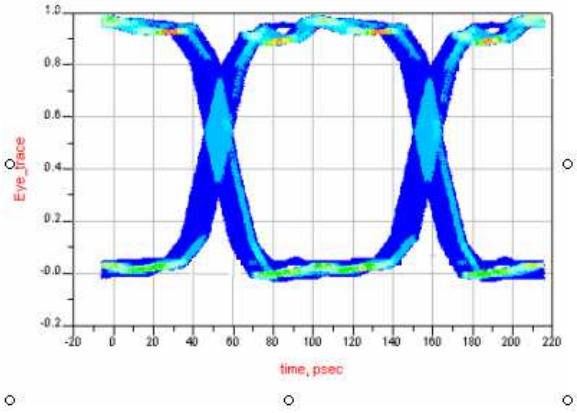


Figure 168: Eye diagram result for the 50 um thick, dielectric constant 3.5.

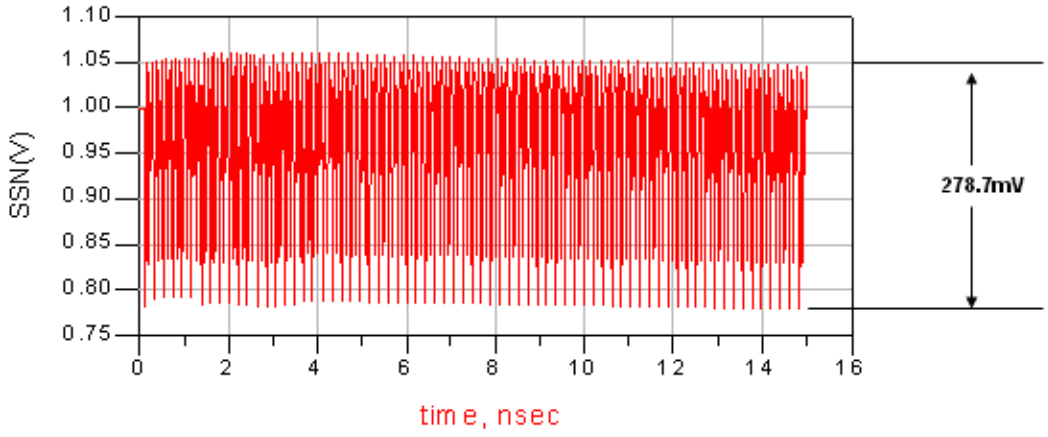
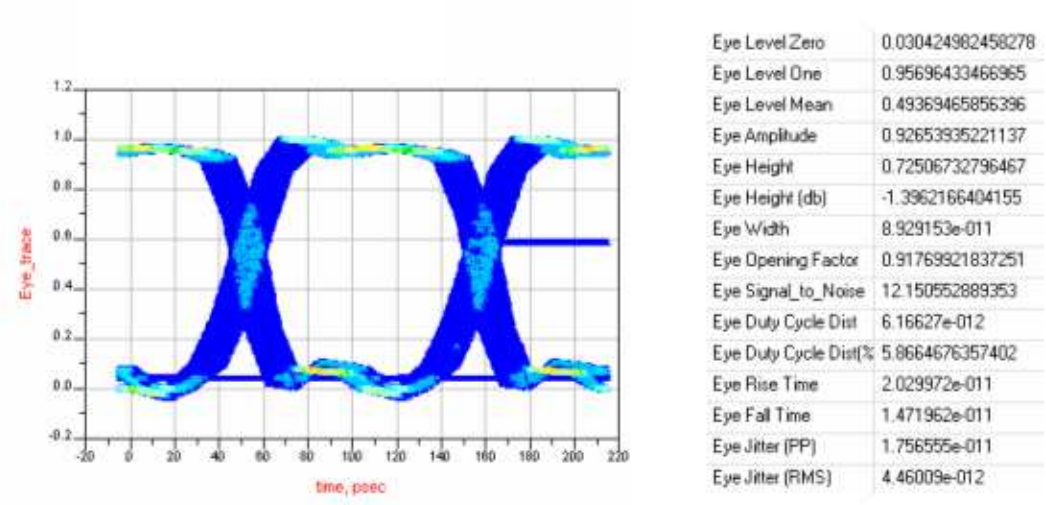


Figure 169: SSN for a differential link with a 50 um thick dielectric with a dielectric constant of 4.2.



Eye Level Zero	0.030424982458278
Eye Level One	0.95696433466965
Eye Level Mean	0.49369465856396
Eye Amplitude	0.92653935221137
Eye Height	0.72506732796467
Eye Height (db)	-1.3962166404155
Eye Width	8.929153e-011
Eye Opening Factor	0.91769321837251
Eye Signal_to_Noise	12.150552889353
Eye Duty Cycle Dist	6.16627e-012
Eye Duty Cycle Dist(%	5.8664676357402
Eye Rise Time	2.029972e-011
Eye Fall Time	1.471962e-011
Eye Jitter (PP)	1.756555e-011
Eye Jitter (RMS)	4.46009e-012

Figure 170: Eye diagram for a differential link with a 50 um thick dielectric with a dielectric constant of 4.2.

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