CORRELATION OF PDN IMPEDANCE WITH JITTER AND VOLTAGE MARGIN IN HIGH SPEED CHANNELS

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CORRELATION OF PDN IMPEDANCE WITH JITTER AND VOLTAGE MARGIN IN HIGH SPEED CHANNELS

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SUMMARY

Jitter and noise on package and printed circuit board interconnects are limiting factors in the performance of high speed digital channels. The simultaneous switching noise (SSN) induced by the return path discontinuities (RPDs) is a major source of noise and jitter on the signal interconnects of these channels. Therefore, optimal design of the power delivery network (PDN) is required to reduce SSN induced noise and jitter and improve the performance of high speed channels.

The design of PDN is done in frequency domain whereas jitter and noise are time domain events. As a result, multiple iterations between frequency domain design of PDN and time domain analysis of noise and jitter are required before a design is taped out.

A new methodology to correlate PDN impedance with jitter and voltage margin is presented in this thesis. Using this methodology, it would be possible to estimate jitter and noise from the PDN impedance and reduce the iterations involved in freezing the PDN design.

The SSN induced at a given RPD is proportional to the PDN impedance at that RPD. As a result, the jitter and the noise can be correlated to the PDN impedance. The PDN impedance is a function of frequency and has alternate local minima and local maxima at resonances and anti-resonances respectively. The anti-resonances in the PDN impedance at the RPD cause significant increase in the insertion loss of signal whose return current is disrupted at that RPD. The increase in the insertion loss attenuates significant harmonics of the signal degrading its rise/fall times and voltage levels. This results in reduction of timing and voltage margins of the signal. Thus, based on the insertion loss profile and harmonic content of the signal, an estimate of jitter and noise on the signal can be made. Passive test vehicles consisting of microstrips with RPDs have been designed and fabricated to demonstrate the proof of concept through both simulations and measurements.

Suitable placement of decoupling capacitors is suggested to reduce the PDN impedance

below the target impedance and to minimize coupling between two noise ports on the PDN. Genetic algorithm to optimize the selection and placement of decoupling capacitors has been implemented. The efficacy of the algorithm has been demonstrated by testing it on a power delivery networks consisting of a simple power/ground plane pair.

CHAPTER 1

INTRODUCTION

Rapid advancements in packaging technology have resulted in large scale integration and miniaturization of packages and printed circuit boards (PCBs). This has made it possible to support data rates approaching giga bits per second in interfaces such as double data rate (DDR3) SDRAM. While packaging technology has had a major role to play in the performance improvement of these high speed interfaces, there still exists a performance gap between package/PCB and bare die, as shown in Figure 1 [1].

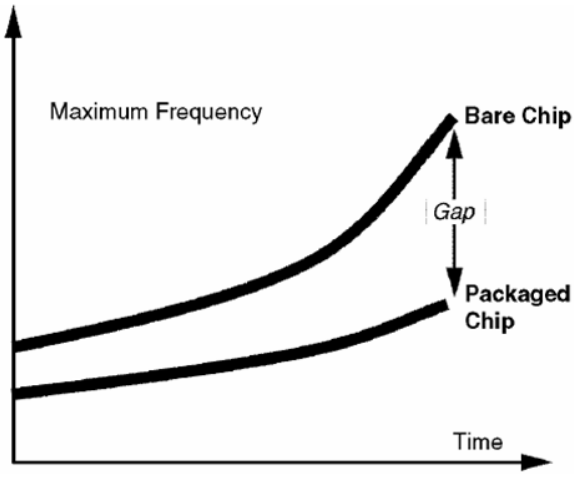

Figure 1. Performance gap in bare die and package over the years (*Reproduced from [1]*)

According to the International Technology Roadmap for Semiconductors (ITRS) 2005 edition, 'Assembly and Packaging are limiting factors in both cost and performance of electronic systems' [5]. Some of the primary factors limiting the performance of package/PCB are:

- Crosstalk between neighboring interconnects.
- Simultaneous switching noise in power supply due to simultaneous switching of multiple drivers.
- Process, temperature and voltage variations.

- Manufacturing tolerance on package and PCB trace lengths and impedances.

Rapid technology scaling at the chip level has resulted in multi-function system on chips with large I/O count. This has resulted in increase in simultaneous noise induced jitter and noise on package and PCB interconnects. The simultaneous switching noise has thus become an important bottleneck in performance of high speed channels. The next few sections give a brief description of the mechanism by which SSN is induced, its impacts on the timing and the voltage margins, prior research on SSN, leading to the motivation behind the work described in this thesis.

1.1 Topology of High Speed Interconnects on the Package and the PCB

In spite of rapid technology scaling and advent of System on Chip (SoC) paradigm, it is prohibitive to include all the digital functions of large systems into a single chip due to yield constraints. Therefore, typical systems such as a laptops and mobile phones consist of multiple chips, both analog and digital talking to each other through interconnects on the package and PCB, as shown in Figure 2 [2]. With the advent of System on Package (SoP) technology, the PCB is being replaced with a single system package as shown in Fig.3 [6].

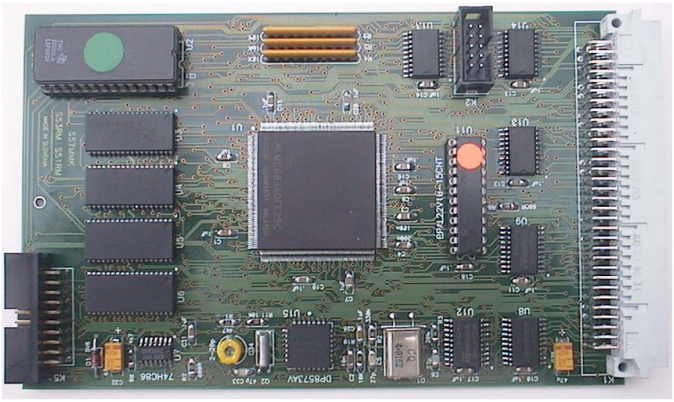

Figure 2. Topology of high speed interconnects on a printed circuit board (*Reproduced from [2]*)

To increase the throughput of the system, high speed signals propagation is required between various digital modules like ASIC/DSP and memories such as DDR SDRAM.

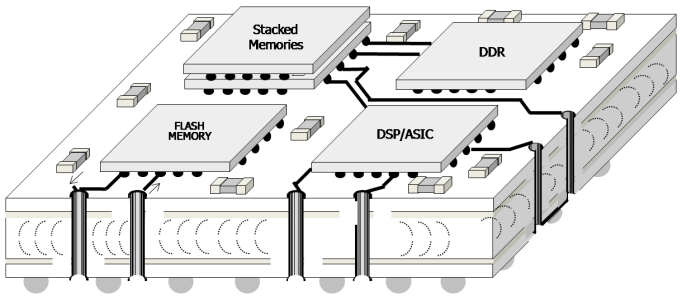

Figure 3. Topology of high speed interconnects on a system on package

These modules or interfaces typically have clock, data, address and control signals routed from one die to the other through package and/or a PCB. The I/O drivers of clock, data, address and control signals on each die are powered by the voltage regulator module (VRM), through the package and the PCB power delivery network as shown in Figure 4 [3].

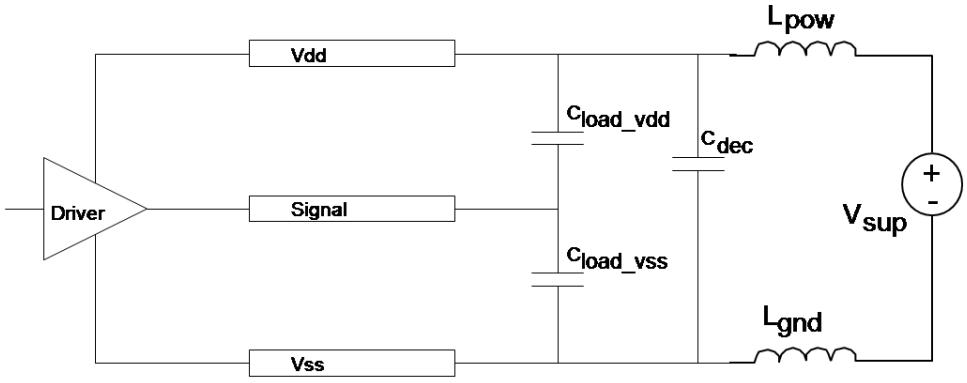

Figure 4. Approximate equivalent circuit showing Power Delivery Network parasitic inductance from VRM to I/O driver (*Reproduced from [3]*)

When multiple I/O drivers switch together a large amount of current drawn from the power supply causes a glitch in voltage seen by the I/O driver due Ldi/dt drop across the finite inductance of the PDN. This noise on the power supply, caused by switching of multiple drivers is referred to as the simultaneous switching noise (SSN). SSN is sometimes referred to as a delta-I noise, because of its dependence on the rate of change of current. SSN is also called ground bounce because just like it causes a glitch in power supply, it causes ground voltage to rise when multiple drivers switch from high to low. As the packaging technology has shifted from traditional lead frame packages to the modern

system-in-package (SiP) or system-on-package (SoP) technology, the SSN problem has shifted from inductance problem to plane bounce problem [7]. This is explained in detail in the next section.

1.2 SSN/Plane Bounce Due to Return Path Discontinuities

To minimize SSN, today's package and PCBs consist of power and ground planes instead of power and ground traces. This is done to minimize the inductance and increase the capacitance of the PDN. Also, to enable propagation of high speed signals, interconnects on packages and PCBs are referenced to either or both of the power and the ground planes. This is to enable interconnects to behave like transmission lines as transmission lines facilitate higher bandwidth compared to that of point to point wiring. When signal propagates through transmission lines, it induces a return current on the reference plane as shown in Figure 5 [4]. The return current is equal in magnitude and opposite in direction to the current on the signal interconnect.

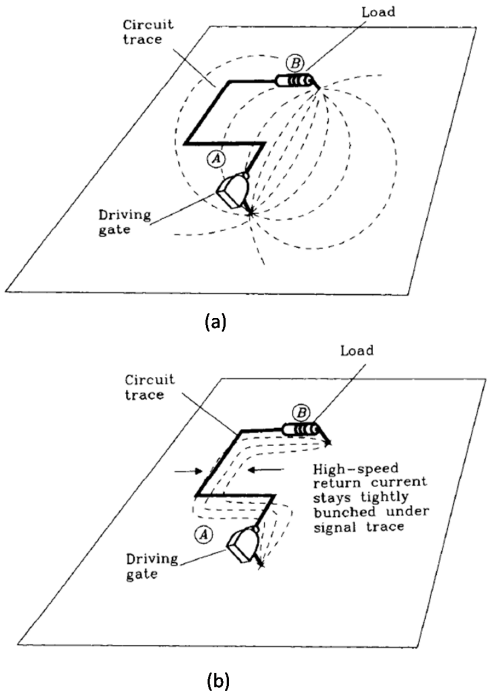

Figure 5. Nature of return currents on reference plane at (a) Low Frequencies (b) High Frequencies (*Reproduced from [4]*)

Whenever there is a change in reference plane of the signal, it gives rise to a discontinuity in the path of the return current. This discontinuity is called the return path discontinuity. The return current jumps from one reference plane to the other at the return path discontinuity as shown in Figure 6. Since, the power and the ground planes are used as

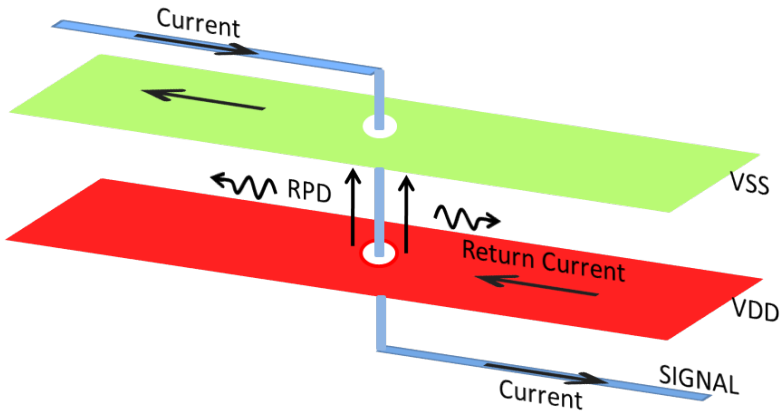

Figure 6. Return Path Discontinuity due to change in reference from power(VDD) to ground (VSS) plane

the reference planes, the return path discontinuities lead to excitation of the power/ground plane pair cavity by the return currents at the return path discontinuity. This excitation causes EM waves to propagate between the plane pair cavity and induce SSN between the two planes [8].

Typical RPDs are either due to microstrip-via-microstrip transition as shown in Figure 7(a) or due to plane cut outs as shown in Figure 7(b). These RPDs cause return current to jump from the power plane to the ground plane or vice versa, inducing SSN between the two planes.

In order to avoid return path discontinuities and minimize SSN, stack-ups shown in Figure 8 are used so that there is no change in the reference planes. In Figure 8(a), the the mictrostrip is referenced only to the power plane all along its length to avoid RPD. Similarly, in case of Figure 8(b), the mictrostrip is referenced only to the ground plane.

In cases where via transitions are unavoidable, the stack-ups shown in Figure 9 are used. If the signal is to be referenced to power plane, two power planes are used as shown

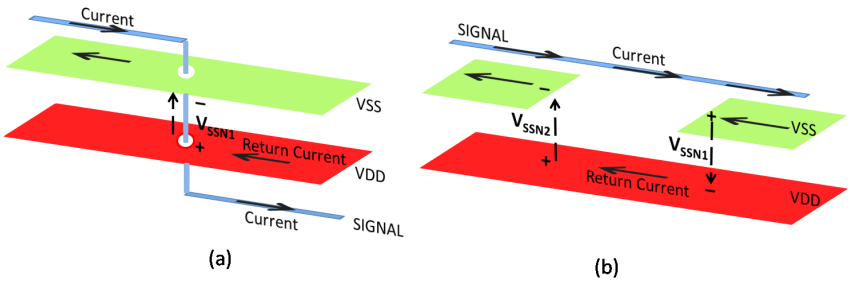

Figure 7. Return path discontinuity due to (a) microstrip-via-microstrip transition (b) plane cut-outs

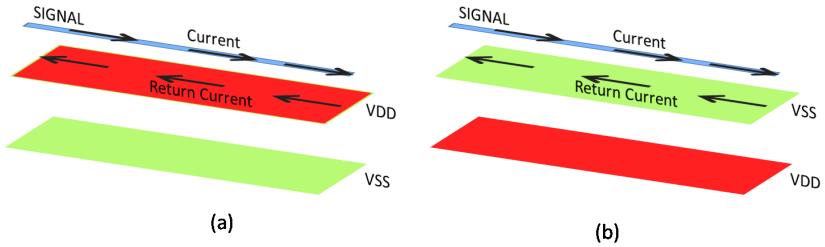

Figure 8. RPDs avoided by referencing the signal only to (a) voltage or power plane (b) ground plane

in Figure 9(a). The power planes are shorted with large number of vias which provide a path for the return current, avoiding RPD on the signal. Similarly, if the signal is to be reference to the ground plane, the two ground planes are used as shown in Figure 9(b). If the power/ground planes are shorted together with large number of vias, then the equivalent arrangement is same as in Figure 8(a) and 8(b).

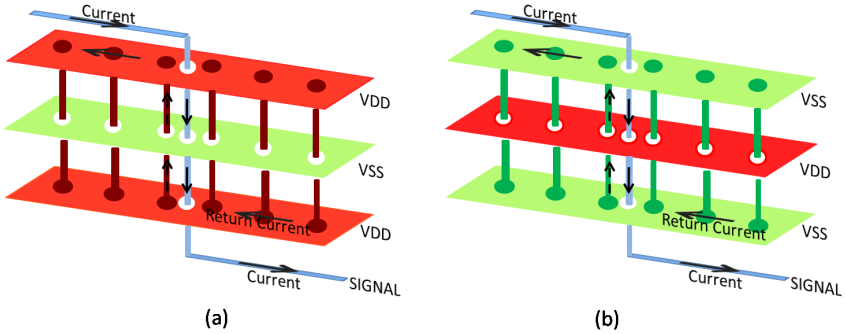

Figure 9. RPDs avoided in case of signal with microstrip to microstrip via transition (a) by shorting two power planes (b) by shorting two ground planes

Even in the absence of the RPDs, the return current may jump from power plane to ground plane due to the nature of currents during low to high and high-to-low transitions.

For example, the transmission line in the Figure 10 has no return path discontinuity. The steady state current when the buffer is 'LOW' is shown in the Figure 10. When the buffer makes a transition from low 'LOW' to 'HIGH', the return current on the power plane jumps from the power to the ground plane inducing an SSN between the power and the ground planes as shown in Fig.11. Similarly, when the buffer makes a 'HIGH' to 'LOW' transition the return current jumps from the ground to the power plane leading to SSN between the power and the ground planes. The detailed explanation of the mechanism of the current flow during 'LOW' to 'HIGH' and 'HIGH' to 'LOW' transition of buffer is explained in [9].

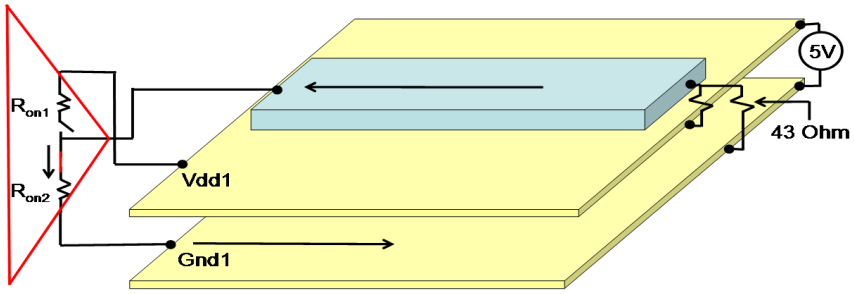

Figure 10. Steady state current profile when the driver is low (*Reproduced from [3]*)

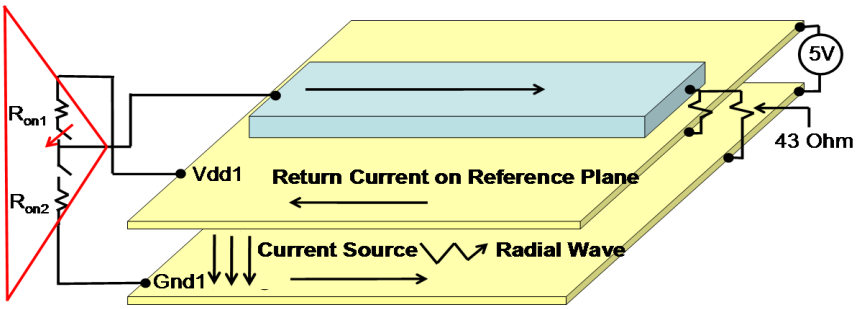

Figure 11. Transient current profile when the driver switches from low to high (*Reproduced from [3]*)

From the above discussion, it is clear that SSN induced between the power/ground plane is due to unavoidable discontinuity in return currents. The impact of SSN on timing and voltage margins is discussed in the next section.

1.3 Impact of SSN on the Timing and the Voltage Margins

High speed communication between two chips such as an ASIC and a memory requires the signal from one chip to meet the timing and voltage specifications of the other chip. The timing specifications are in the form of setup time and hold time requirements which are shown in Figure 12 and explained below.

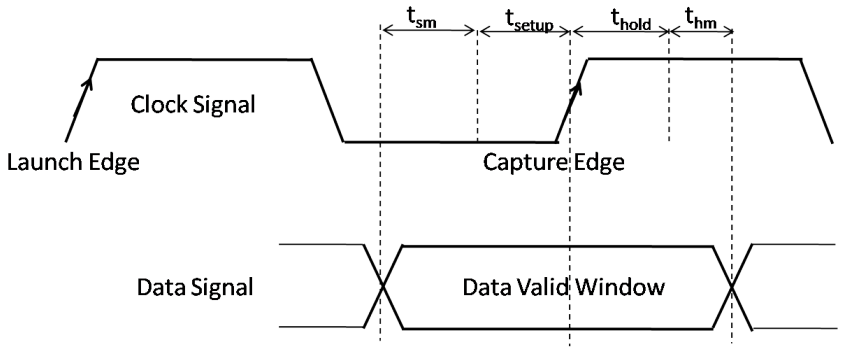

Figure 12. Typical timing specifications in high speed digital signals

1. Setup Time (t_{setup}): The minimum time that the data must remain valid before the capture edge of the clock.

2. Hold Time (t_{hold}): The minimum time that the data must remain valid after the capture edge of the clock.

3. Setup Margin (t_{sm})g: The time difference between the setup time and the time at which the data becomes valid.

4. Hold Margin (t_{hm}): The time difference between the time till which the data remains valid and the hold time.

5. Timing Margin ($t_{sm} + t_{hm}$): The difference between the data valid time and the sum of setup and hold times.

The voltage specifications include V_{IH}, V_{OH}, V_{OL} and V_{IL} specifications which are shown in Figure 13 and explained below.

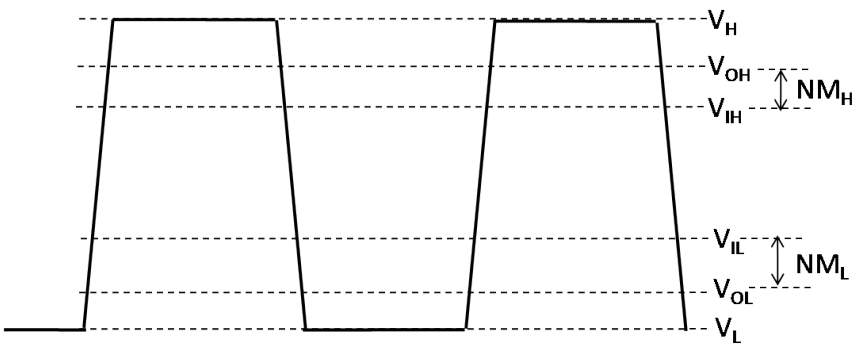

Figure 13. Typical voltage specifications in high speed digital signals

1. V_H: Ideal voltage at the output or the input of the driver for a signal to be considered logic high.

2. V_{OH}: Minimum voltage required at the output of the driver for a signal to be considered logic high.

3. V_{IH}: Minimum voltage required at the input of the driver for a signal to be considered logic high.

4. V_L: Ideal voltage at the output or the input of the driver for a signal to be considered logic low.

5. V_{OL}: Maximum voltage allowed at the output of the driver for a signal to be considered logic low.

6. V_{IL}: Maximum voltage allowed at the input of the driver for a signal to be considered logic low.

7. Noise Margin High (NM_H): The maximum noise that can be tolerated by a logic high signal ($NM_H = V_{OH} - V_{IH}$)

8. Noise Margin High (NM_L): The maximum noise that can be tolerated by a logic low signal ($NM_L = V_{IL} - V_{IH}$)

9. Noise Margin (NM) : The total noise that can be tolerated by signals in high speed channels ($NM = NM_H + NM_L$)

Violation of timing and voltage specifications might result in incorrect data to be captured by the receiver leading to functional failures. For a system to work reliably the timing and voltage specifications must be met under all the worst case scenarios the system might be put into. Since, it is impossible to account for all the worst case scenarios and also to account for inaccuracies in simulation tools, designers over design the systems to meet timing and voltage specifications by margins called timing margin and voltage margin.

In practical applications, signal pulses propagating through high speed channels see different degrees of attenuation and different values of rise/fall delays before they reach the receiver chip. These variations, caused due to changes in process, temperature and voltage seen by the system, cause reduction in timing and voltage margins.

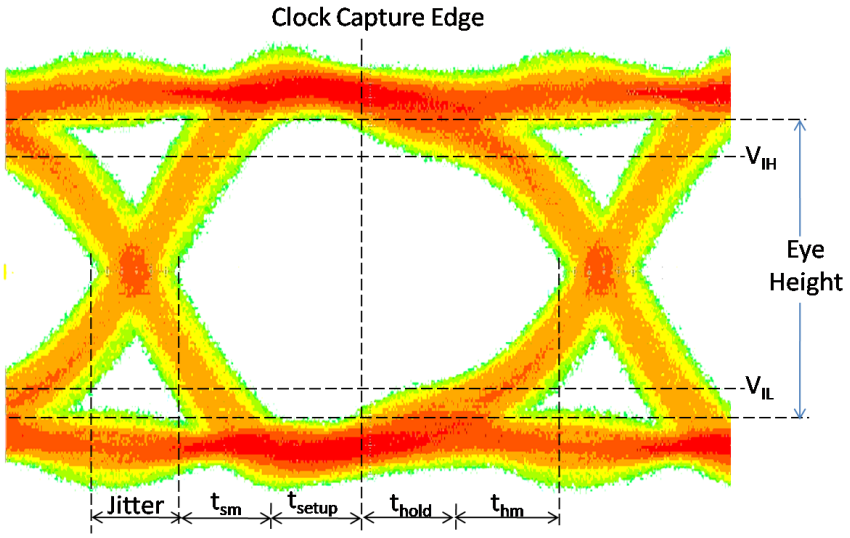

Figure 14. Eye Diagram

An eye diagram is an important tool to visualize the variations in signal delays and amplitude over time. It is obtained by overlapping time separated pulses over a time base equal to the bit period (inverse of bit rate). The eye height or eye opening is the measure of additive noise on the signal, whereas the eye width is the measure of jitter (variations

in propagation delay of signals across pulses). As can be seen from Figure 14, higher amount of noise on the signal causes reduction in voltage margin, whereas higher jitter causes reduction in timing margin.

Simultaneous switching noise is one of primary source of noise and jitter on high speed signals propagating on package/PCB. This can explained using a simplified circuit shown in Figure 15 [3].

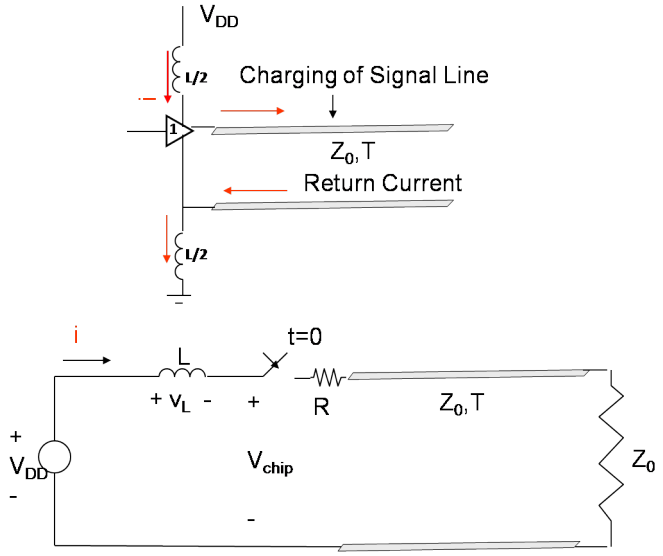

Figure 15. Simplified circuit to explain the impact of SSN on timing and voltage margins (*Reproduced from [3]*)

When the driver-1 switches, a sudden current is drawn from the power supply causing a drop across across the inductance of the PDN. The drop across the inductance is given by the equation 1 [3].

$$V_L = \Delta v = \frac{L \times V_{DD}}{Z_0 t_r}(1 - e^{-t_r/(L/Z_0)}) \tag{1}$$

When 'N' similar linear drivers switch, the drop across the inductance is given by equation 2 [3].

$$V_L = \Delta v = \frac{N \times L \times V_{DD}}{Z_0 t_r}(1 - e^{-t_r/(NL/Z_0)}) \tag{2}$$

Switching of multiple drivers causes large drop in the power supply seen by the driver. This causes reduction in the amplitude of the signal and hence reduction in the voltage margin.

The time domain output voltage of a linear driver shown in Figure 15 is given by equation 3 and equation 4 [3].

$$v(t) = \frac{Z_0 \times V_{DD}}{Lt_r}\left[\frac{L^2}{Z_0^2}\left(e^{\frac{-t}{(L/Z_0)}} - 1\right) + \frac{L}{Z_0}t\right], \quad t \le t_r \tag{3}$$

$$v(t) = A + B(1 - e^{\frac{-t}{(L/Z_0)}}), \quad t > t_r \tag{4}$$

where,

$A = V_{DD} - [V_{DD} - v(t_r)]\, e^{\frac{t}{(L/Z_0)}}$,

$B = [V_{DD} - v(t_r)]\, e^{\frac{t}{(L/Z_0)}}$

The 50% propagation delays can be obtained by substituting $v(t) = 0.5V_{DD}$ in the above equations. It is observed that decrease in V_{DD} causes increase in propagation delay of the signals as shown in Figure 16 [3].

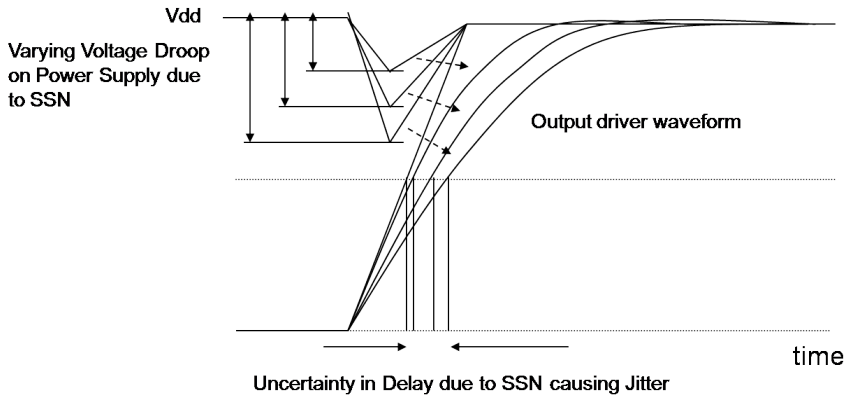

Figure 16. Impact of SSN on propagation delay of the driver (*Reproduced from [3]*)

When multiple drivers switch, there is a large drop in V_{DD} voltage and hence the signal propagation delays are high. On the other hand when few drivers switch, the drop in V_{DD} is less and hence propagation delays are less. Since the number of I/O drivers switching is

arbitrary, different values of SSN voltage induced causes different values of rise/fall delays giving rise to data dependent jitter causing the timing margin to reduce.

The effect of SSN is similar on non-linear drivers. The only difference is that in case of non-linear drivers the SSN voltage and propagation delays do not increase linearly with the number of drivers switching due to feedback effect [10].

Thus, SSN causes reduction in timing and voltage margin of the system degrading its performance.

1.4 Modeling and Design of Power Delivery Network

The power delivery network or the power distribution network (PDN), is used to power the core as well as the I/O drivers in different chips sitting on a PCB or package. The PDN consists of the voltage regulator module (VRM), the PCB and the package power delivery network and the chip power delivery network as shown in Figure 17 [3].

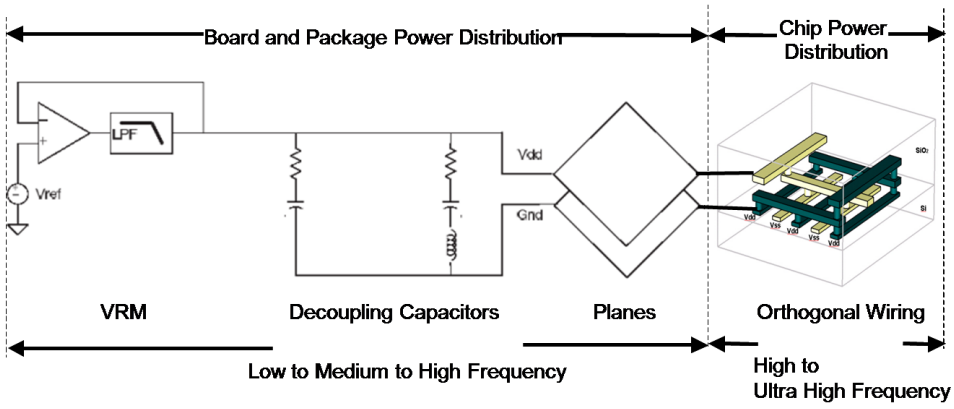

Figure 17. Components of a Power Delivery Network (*Reproduced from [3]*)

The voltage drop across the inductance of a PDN is the primary cause of SSN seen by both the core and the I/O drivers. In order to reduce the parasitic inductance modern packages and PCBs make use of power and ground planes instead of interconnects to supply power to the active circuits. The planes provide following advantage over power/ground interconnects:

1. Planes provide a path of low inductance to the current from decoupling capacitors.

2. The capacitance between the planes is useful for decoupling the power supply at high frequencies.

3. Planes provide a low inductance path to the return currents of signal traces.

4. Planes shield the signal traces and reduce electromagnetic interference (EMI).

However, since the planes act as waveguides with unterminated edges, the excitation of planes creates standing waves which manifest as large voltages across the planes at resonant frequencies [11]. The resonant frequency of plane pair with dimension $a \times b$ is given by equation 5

$$f_{mn} = \frac{1}{2\pi\sqrt{\mu\epsilon}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \tag{5}$$

where, m and n are the resonant modes and ϵ and μ are permittivity and permeability respectively.

Since, the planes are passive structures, they can be characterized by network parameters. Typically, impedance parameters are used to characterize the planes. The two port impedance parameters are given by equation 6 and equation 7.

$$V_1 = Z_{11}I_1 + Z_{12}I_2 \tag{6}$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2 \tag{7}$$

where Z represents the impedance and V and I represent the voltages and currents at the two ports.

The impedance parameters are defined below:

1. Self Impedance : Self impedance represents the magnitude and phase of voltage induced at a port for a unit sinusoidal input applied at that port. For example, Z_{11} represents magnitude of voltage at Port-1 for unit sinusoid current applied at Port-1,

keeping Port-2 open. Similarly, Z_{22} represents magnitude of voltage at Port-2 for unit sinusoid current applied at Port-2, keeping Port-1 open.

2. Transfer Impedance : Transfer impedance between the two ports represents the magnitude and phase of voltage induced at one port for a unit sinusoid input current applied at the other port. For example, Z_{12} represents the magnitude and phase of voltage induced at Port-1 for a unit sinusoid current applied at Port-2. Similarly, Z_{21} represents the magnitude and phase of voltage induced at Port-2 for a unit sinusoid current applied at Port-1.

The magnitude and phase of voltage induced at any port in the PDN is a function of frequency as well as the location of the port. This is illustrated by simulating a power ground plane pair with ports defined as shown in Figure 18 using multi-layered finite difference method (M-FDM) [12]. The voltage distribution between the two planes is obtained by applying a unit sinusoid current at Port-1.

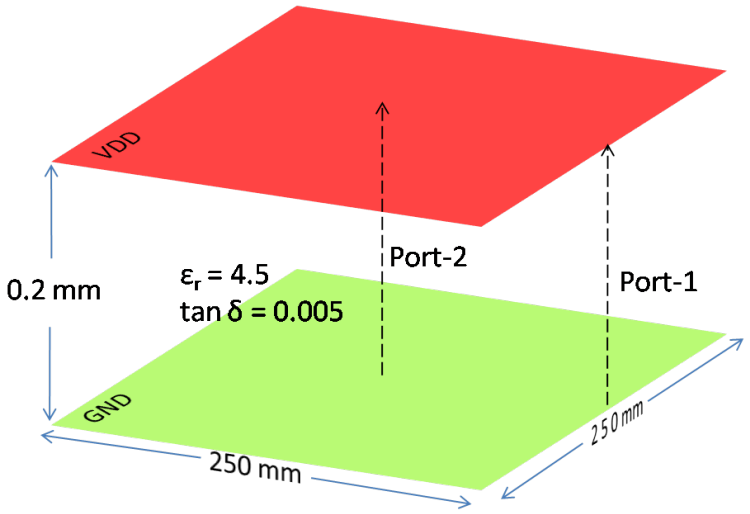

Figure 18. Power-Ground Plane Pair

The distribution of voltage between the planes at 71.38 MHz is shown in Figure 19. Since, at 71.38 MHz, there is a resonance at Port-1, the voltage between VDD and GND at Port-1 is almost close to zero. Thus, the self impedance of Port-1 (Z_{11}) is close to zero at 71.38 MHz as shown in Figure 20.

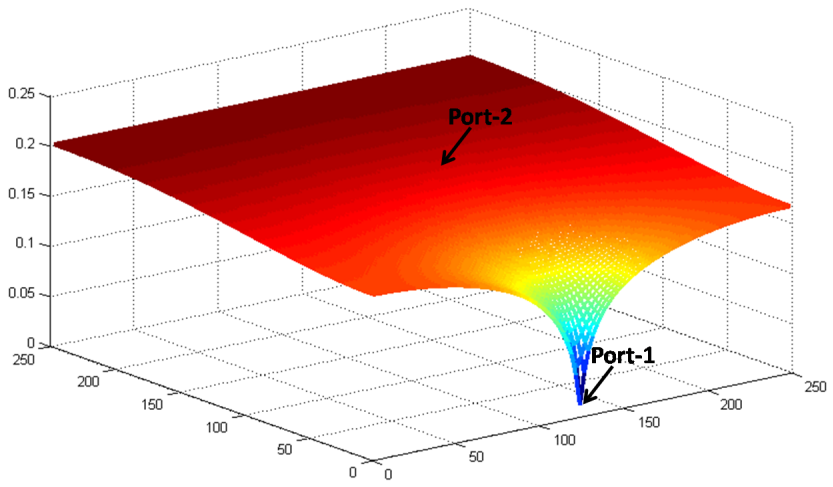

Figure 19. Voltage Distribution between the power ground planes at 71.38 MHz

Similarly, as shown in Figure 21, a large voltage is induced between the VDD and GND at Port-1 due to anti-resonance at 279.3 MHz. Thus, the PDN impedance at Port-1 has a local maxima at 279.3 MHz as shown in Figure 20.

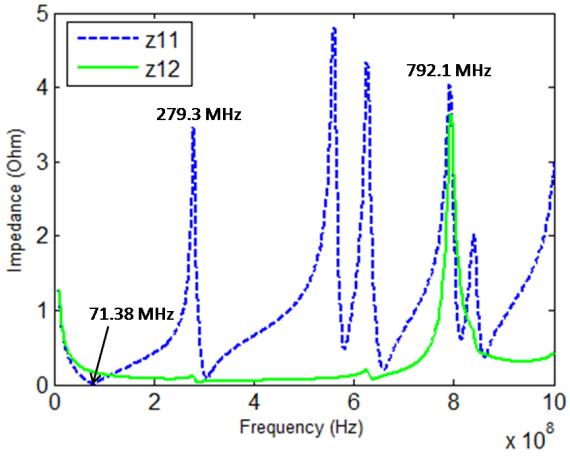

Figure 20. Self and Transfer Impedances or power and ground plane pair shown in Figure 18

The first anti-resonance in the transfer impedance (Z_{12}) occurs at a frequency of 792.1 MHz as seen from Figure 20. Correspondingly, the voltage distribution between the two planes shows a large voltage at Port-2 at 792.1 MHz, as shown in Figure 22.

The resonances and anti-resonances are also brought about by interaction between various components of a PDN. The equivalent series inductance (ESL) of one decoupling

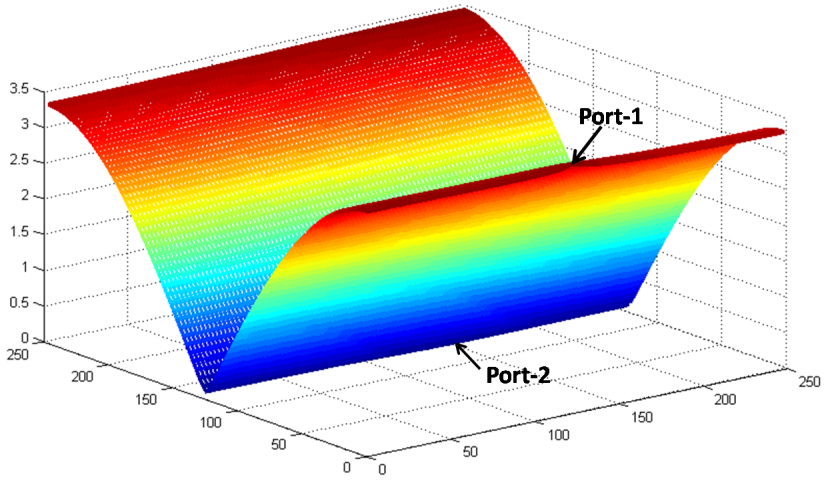

Figure 21. Voltage Distribution between the power ground planes at 279.3 MHz

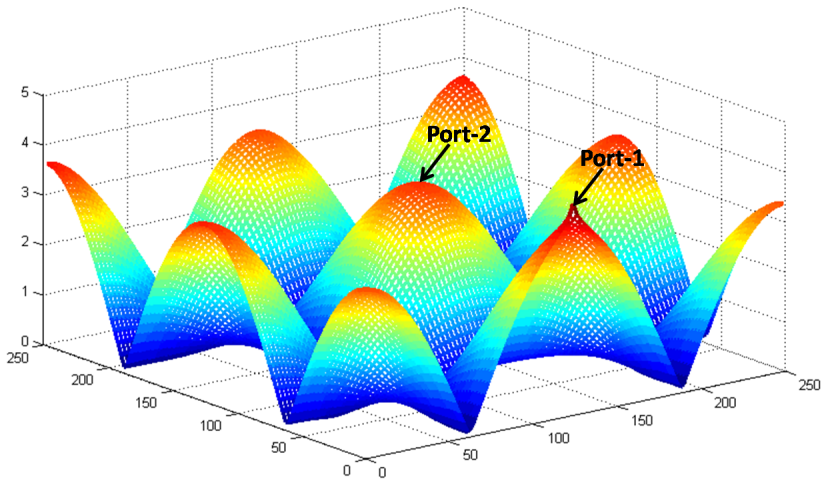

Figure 22. Voltage Distribution between the power ground planes at 792.1 MHz

capacitor might resonate with the capacitance of another decoupling capacitor or the capacitance of the planes to cause anti-resonance. Similarly, there might be chip-package anti-resonance due to interaction between chip capacitance and package inductance. Therefore, a typical profile of the PDN impedance consists of multiple resonances and anti-resonances as shown in Figure 23.

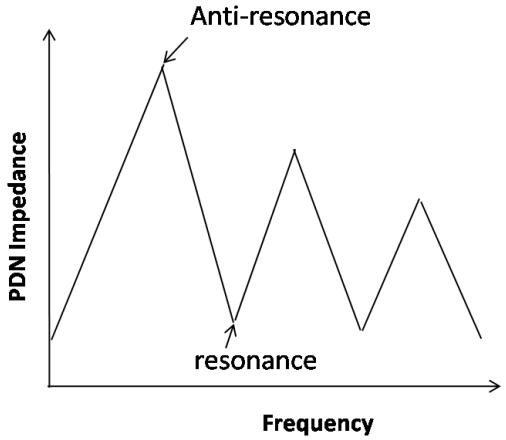

Figure 23. PDN Impedance profile for typical systems

Since today's systems such as mobile phones and computers support multiple frequencies, the objective of PDN design is to reduce the PDN impedance below the target impedance at all frequencies supported by the system as shown in Figure 24. The target impedance is given as:

$$Z_{tar} = \frac{V_{DD} \times ripple}{50\% \times I_{max}} \tag{8}$$

Since, the PDN impedance is a function of frequency and the objective of PDN design is to reduce the PDN impedance over a range of frequency, the design of PDN is done in frequency domain.

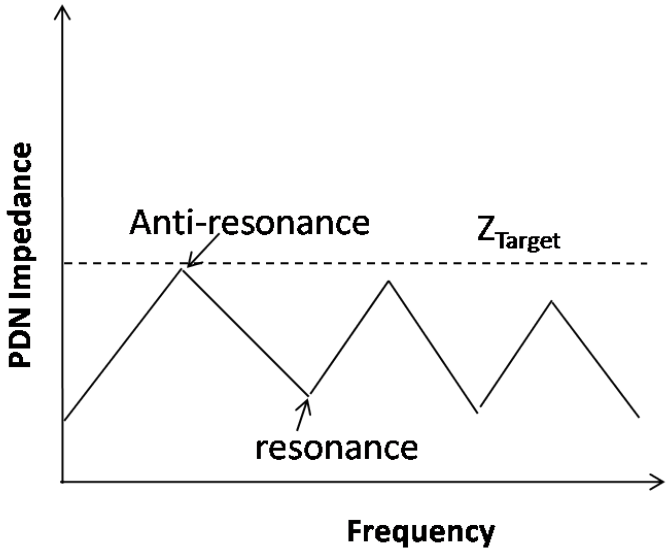

Figure 24. PDN Impedance kept below target impedance

1.5 Motivation

The design of PDN is done in frequency domain. However, the final system specifications are in the form of jitter and noise, both of which are time domain events. Since the PDN impedance impacts timing and voltage margin, the PDN impedance has to be taken into account to find out the exact values of the timing and the voltage margins. As a result the design of PDN involves multiple iterations consisting of frequency domain design and analysis of PDN and time domain simulation and analysis to find out timing and voltage margins. This is shown in Figure 25.

Prior work in this area has mainly focused on modeling and analysis of simultaneous switching noise. Some work has also been done to demonstrate the effect of SSN on signal propagation delays and voltage levels [13, 14, 15]. However, SSN, signal delay and amplitude are all time domain events. The influence of frequency domain PDN impedance on jitter and noise of the signal has not been studied before.

In this thesis, correlation of PDN impedance with jitter and voltage margin has been presented based on which jitter and noise on the signal can be predicted directly from the frequency domain PDN impedance profile. Also, design practices to reduce jitter and

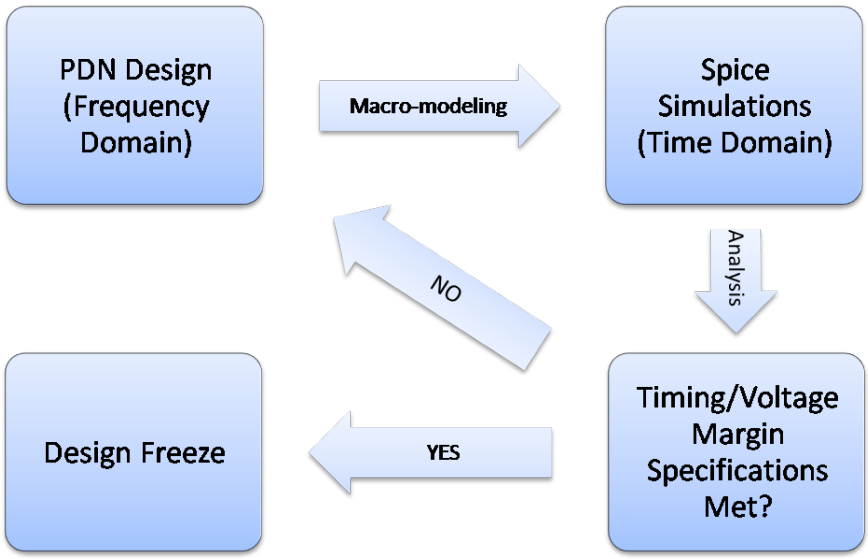

Figure 25. PDN design flow

noise on high speed channels have been suggested. Finally, genetic algorithm for automatic placement of decoupling capacitors has been developed, so that the PDN impedance can be reduced below the target impedance for a given range of frequency.

1.6 Thesis Outline

The rest of the thesis is organized as follows:

1. Correlation of PDN impedance with jitter and voltage margin in high speed channels is discussed in Chapter-2. This is done by analyzing the impact of PDN impedance on the insertion loss of signal having RPD and then analyzing the impact of insertion loss of the signal on timing and voltage margins. Test vehicles have been designed and fabricated and both frequency domain and time domain measurements have been done to validate the analysis. Finally, design practices have been suggested to reduce the jitter and noise on high speed signals.

2. Genetic algorithm (GA) for automatic placement of decoupling capacitors is presented in Chapter-3. The GA terminology and algorithm applied to the problem of decoupling capacitor placement has been explained. The algorithm has been tested on two test vehicles and both frequency and time domain simulation results have been furnished to validate its efficacy.

3. Conclusion and future work is presented in Chapter-4.

1.7 Contribution of this Thesis

The following are the contributions of the research work described in this thesis:

- A methodology to analyze the impact of SSN on timing and voltage margin in terms of power delivery network impedance has been developed based on which number of iterations in design of PDN can be reduced.

- Design practices to minimize jitter and noise in high speed signals have been suggested.

- An algorithm for automated placement of decoupling capacitors to reduce the PDN impedance has been developed to reduce the jitter and noise in high speed signals.

CHAPTER 2

CORRELATION OF THE PDN IMPEDANCE WITH JITTER AND VOLTAGE MARGIN

An interconnect having return path discontinuity induces simultaneous switching noise in the power delivery network. The simultaneous switching noise is proportional to the PDN impedance at the return path discontinuity. Since the PDN impedance is a function of frequency, the value of SSN induced in the PDN depends on the frequency of the signal propagating through the interconnect. However, digital signals are comprised of multiple frequencies with significant harmonics present up to the knee frequency given by equation 9 [4].

$$F_{knee} = \frac{0.5}{T_r} \tag{9}$$

where, F_{knee} = frequency below which most energy in digital pulses concentrates, and T_r = rise time of the pulse measured from 10% to 90% of its amplitude.

Therefore, in order to determine SSN induced noise and jitter on the signal, it is important to consider both the PDN impedance as well as the harmonic content of the signal.

Since, the behavior of a signal through an interconnect depends only on the network parameters of the interconnect and harmonic content of the signal, the correlation of PDN impedance with jitter and noise is done in two steps:

1. Determination of the impact of PDN Impedance at the RPD on the insertion loss of the signal having that RPD.

2. Determination of the impact of signal insertion loss on the jitter and noise of the signal.

The steps enumerated above have been discussed in detail in the next two sections, 2.1 and 2.2. Section 2.3 describes the test vehicles and measurements results to validate the

analysis done in the first two sections. Finally, design guidelines to reduce jitter and noise in high speed signals have been proposed in section 2.4.

2.1 Impact of PDN Impedance on Signal Insertion Loss

The return current induces SSN between the power and ground planes at return path discontinuity. The SSN voltage is equal to the product of the return current and the PDN impedance at the RPD. As PDN impedance is a function of frequency, the SSN voltage also depends on the frequency of the return current. At the anti-resonant frequency of the PDN impedance, a large SSN voltage is induced between the planes. Large value of SSN signifies large coupling (S_{13}) between the signal and the PDN for ports defined as in Figure 26.

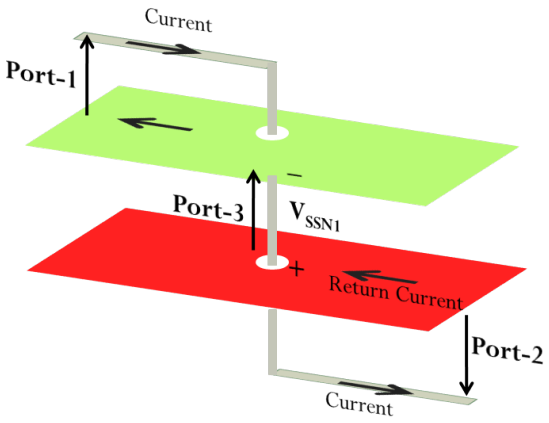

Figure 26. Coupling between signal and PDN due to RPDs

The insertion loss of the signal assuming a loss less system in the above figure is given by equation 10

$$|S_{12}|^2 = 1 - |S_{11}|^2 - |S_{13}|^2 \tag{10}$$

where S_{12} is the insertion loss, S_{11} is the return loss and S_{13} is the coupling between the micro-strip and power/ground plane pair.

From equation 10 it can be inferred that large coupling between signal and PDN results

in smaller amount of energy of the signal to reach from Port-1 to Port-2. In other words, large coupling between signal and PDN causes increase in insertion loss of the signals. Since, there is a very large coupling between the signal and PDN at anti-resonant frequency of PDN, anti-resonances in the PDN impedance result in peaks in the insertion loss of the signal.

To validate the above analysis, four test structures TS1, TS2, TS3 and TS4 were simulated. The frequency domain response consisting of the PDN impedance and the signal insertion loss for each of the test structure was obtained by using student version of electromagnetic field solver, Sphinx [16].

The test structure, TS1 consists of a microstrip referenced to the ground plane all along its length as shown in Figure 27. As there is no return path discontinuity, the insertion loss of the signal (S_{12}) is similar to that of a lossy transmission line as shown in Figure 28.

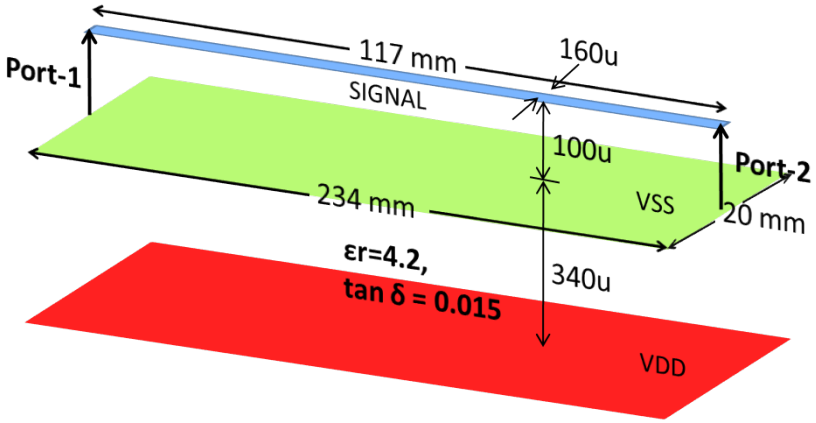

Figure 27. Test Structure, TS-1

The test structure, TS2 consists of a microstrip referenced to both the ground and power planes with via transition at the center of the plane as shown in Figure 29. The PDN impedance at the RPD and the corresponding insertion loss of the signal in TS2 are shown in Figure 30. The frequency response shows peaks in the insertion loss of the signal at all the anti-resonant frequencies of the PDN.

The test structure, TS3 consists of a microstrip referenced to both the ground and power

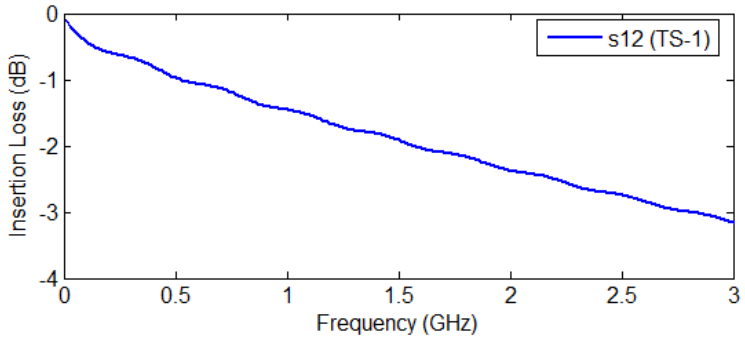

Figure 28. Insertion loss (S_{12}) of TS-1

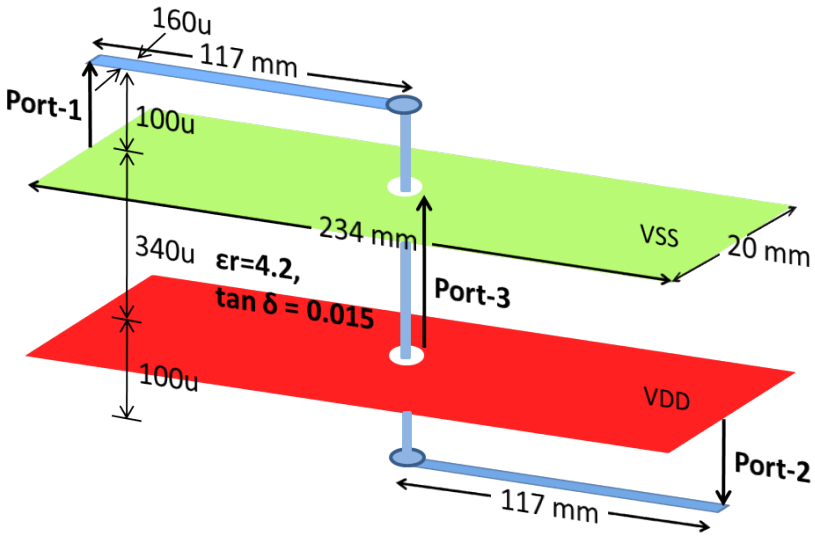

Figure 29. Test Structure, TS-2

planes with via transition at the edge of the plane as shown in Figure 31. The frequency response of TS3 is shown in Figure 32. The frequency response is similar to that of TS2. However, since the PDN impedance at the edge of the plane has higher number of anti-resonances as compared to the PDN impedance at the center of the plane, the insertion loss for TS3 has larger number of peaks as compared to that of TS2. This further validates the fact that the anti-resonances in PDN impedance cause peaks in the insertion loss of the signal.

The test structure, TS4 consists of two via transitions giving rise to two RPDs as shown in Fig 33. As a result, SSN voltages are induced at each of the two RPDs. In this case,

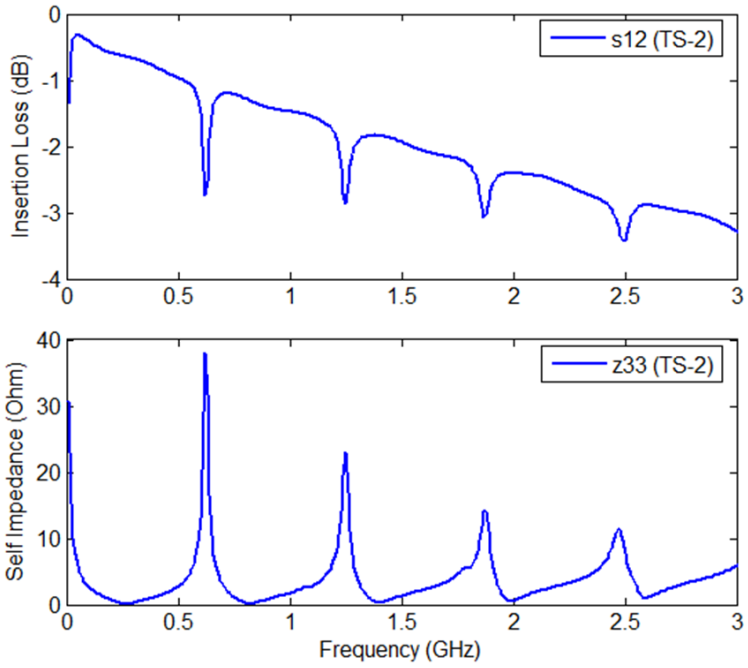

Figure 30. Insertion loss (S_{12}) and Self Impedance at Port-3 of TS-2

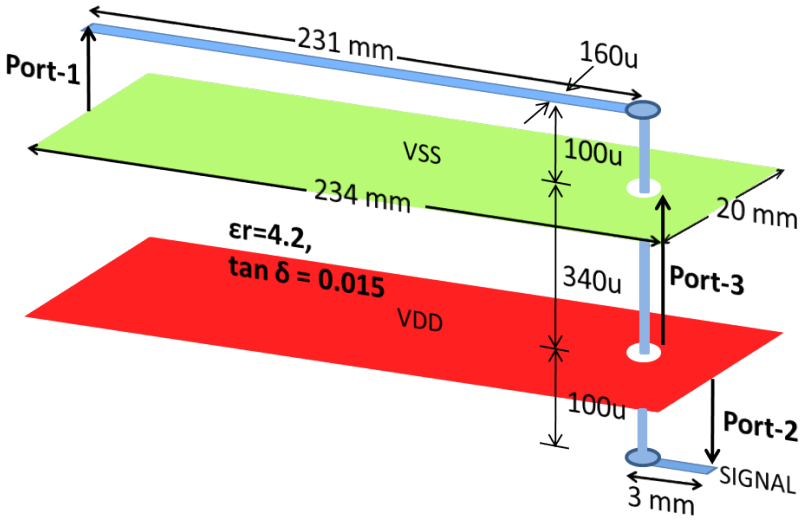

Figure 31. Test Structure, TS-3

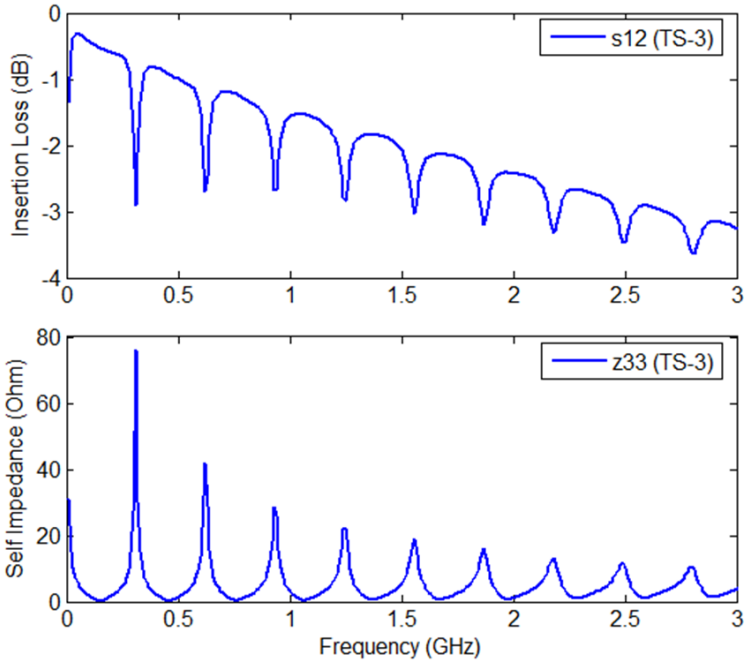

Figure 32. Insertion loss (S_{12}) and Self Impedance at Port-3 of TS-3

the insertion loss profile of the signal depends on the magnitude and phase of the SSN voltage induced at each RPD. The magnitude and phase of the SSN voltage in turn depends on the magnitude and phase of return currents and the PDN impedance at the RPD. At certain frequencies, the SSN voltages induced at each RPD add up causing large coupling between the signal and the PDN and hence large increase in insertion loss. At certain other frequencies the SSN voltages at each RPD cancel each other out and hence do not cause an increase in insertion loss. For example, in case of TS4, there are anti-resonances at 600 MHz in PDN impedance at both Port-3 and Port-4. These anti-resonances cause large SSN voltages to be induced between the power and ground planes. However, these SSN voltages cancel each other out due to which there is not much impact on the insertion loss of the signal as shown in Figure 34.

From the above analysis, it can be concluded that the insertion loss profile of the signal depends on the magnitude and phase of SSN voltages induced at each RPD. The SSN voltages induced in turn depend on the PDN impedance. Thus, the insertion loss of the signal depends on the PDN impedance.

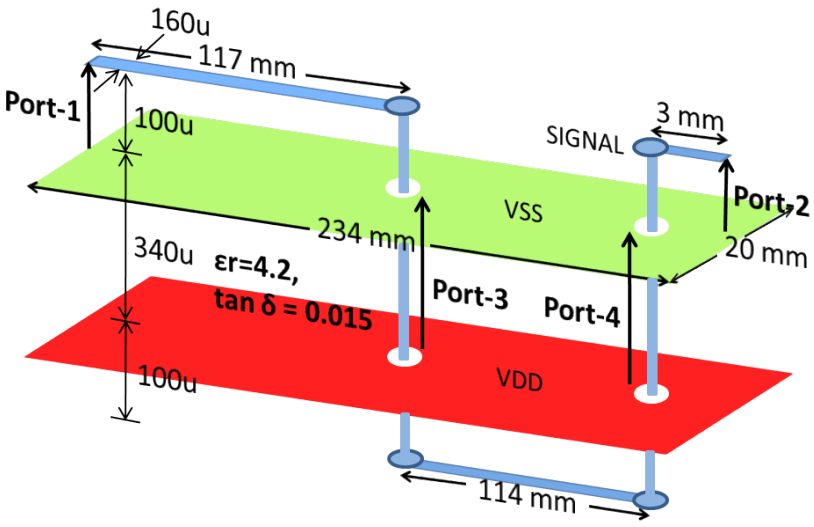

Figure 33. Test Structure, TS-4

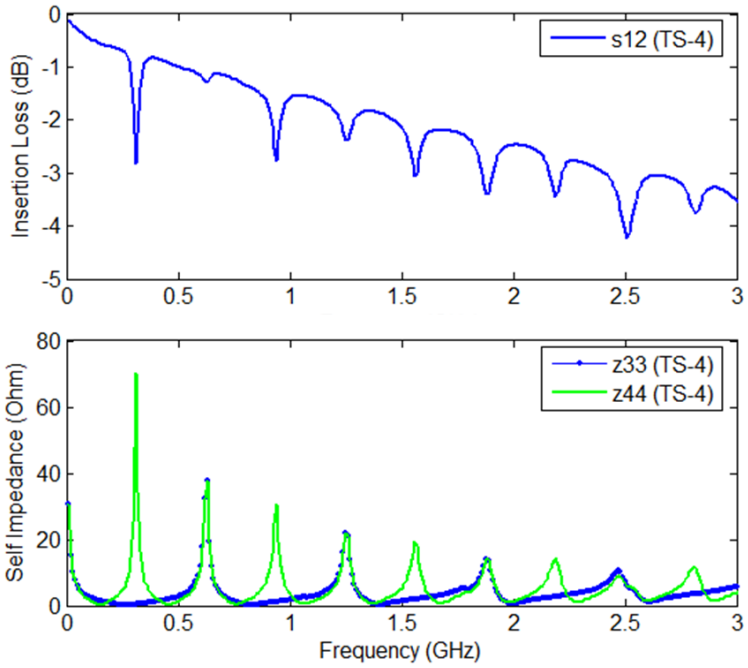

Figure 34. Insertion loss (S_{12}) and Self Impedance at Port-3 and Port-4 of TS-4

2.2 Impact of Signal Insertion Loss on the Timing and the Voltage Margins

The timing and the voltage margins or the jitter and noise on the signal depend on its:

1. Insertion Loss profile

2. Harmonic Content

The insertion loss of the signal depends on the PDN impedance at the RPD. The harmonic content of a digital signal depends on the bit patterns. Data, address, control and clock signals are typical signals used in high speed digital channels. The data, address and control signals are random in nature and hence can be modeled using pseudo random bit stream (PRBS). Thus, the problem of finding jitter and noise on the signals reduces to analyzing the impact of insertion loss of the signal on clock and PRBS signals.

2.2.1 Impact of Insertion Loss on Jitter and Noise of Clock Signal

In order to find the impact of insertion loss on clock signal, the harmonic content of clock signals was found by using Fourier transforms. The frequency spectrum of clock signal consists of harmonics concentrated at odd multiple of its frequency. In other words, a significant amount of energy of the clock signal is stored in few harmonics at odd multiples of its frequency. For example, a 300 MHz clock has significant harmonics present at 300 MHz, 900 MHz and so on as shown in 35.

If the significant harmonics of clock coincide with the peak in the insertion loss of the signal, they would undergo a large attenuation causing reduction in the amplitude and increase in rise/fall time of clock pulses. To illustrate this, TS-4 was simulated with 0.8V, 300 MHz clock as input at port-1. Since, the fundamental frequency of 300-MHz clock coincides with peak in the insertion loss of TS-4, it undergoes a large attenuation causing reduction in amplitude and increase in rise/fall time of the clock signal as shown in Figure 36. On the other hand, since the significant harmonics of 350 MHz clock do not coincide with the peak in insertion loss of TS4, it does not see a large reduction in amplitude and

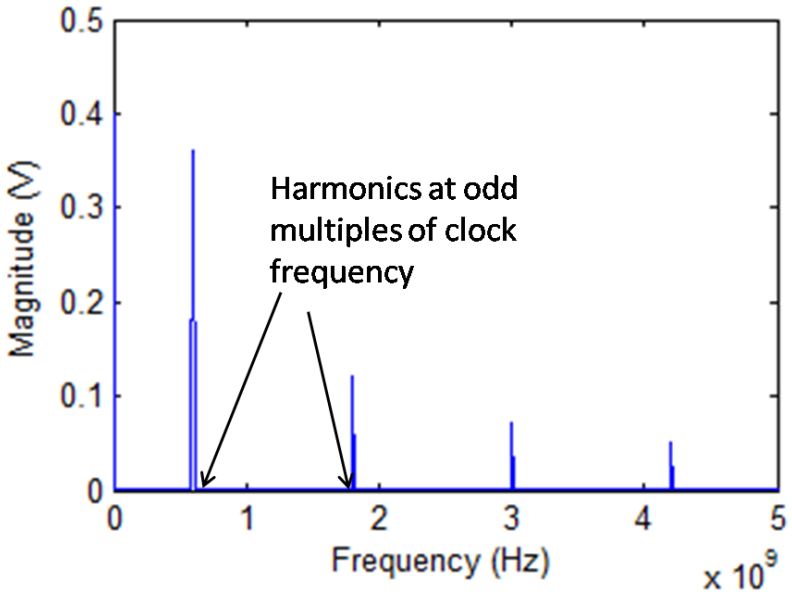

Figure 35. Spectrum of 0.8V, 600-MHz clock signal

increase in rise/fall times of the signals as shown in Figure 37. Hence, attenuation of significant clock harmonics causes large reduction in amplitude and voltage margin in clock signal.

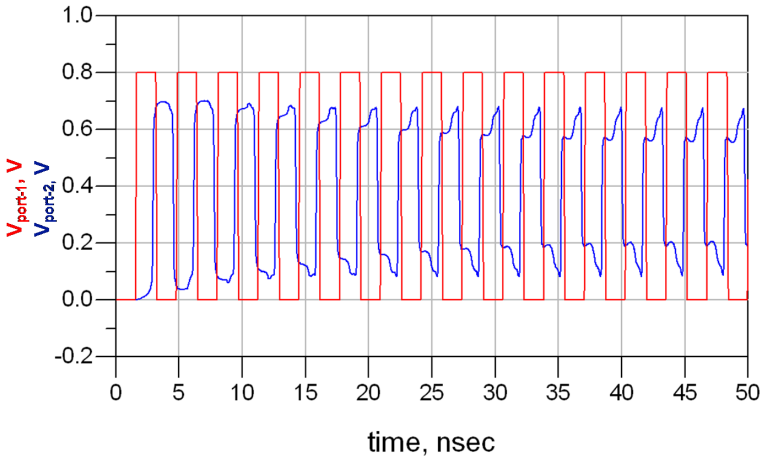

Figure 36. Input and Output waveforms with 0.8V, 300-MHz clock applied at Port-1 of TS-4

Even if significant clock harmonics are attenuated very little jitter is induced in the clock signal. Since the clock is periodic function, the increase in rise/fall times due to attenuation of significant harmonics is seen by all the clock pulses. As there is not much variation in the rise/fall times of individual clock pulses, very little jitter is induced in clock and hence

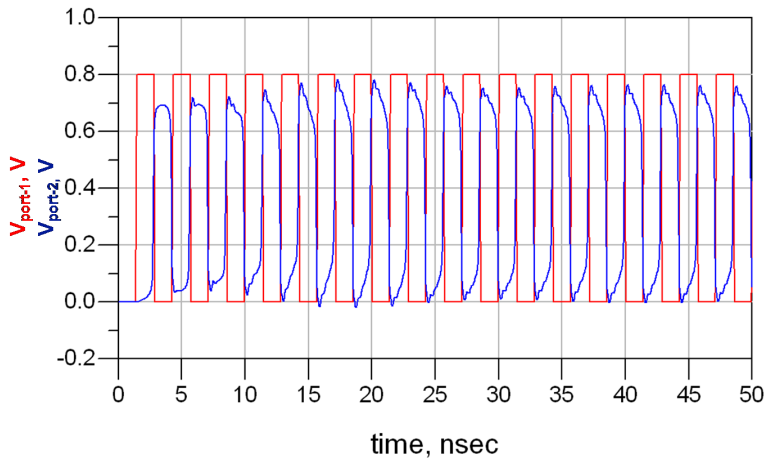

Figure 37. Input and Output waveforms with 0.8V, 350-MHz clock applied at Port-1 of TS-4

there is no significant impact on the timing margins. For instance, the eye diagram of clock in Figure 36 does not show any significant jitter as shown in Figure 38.

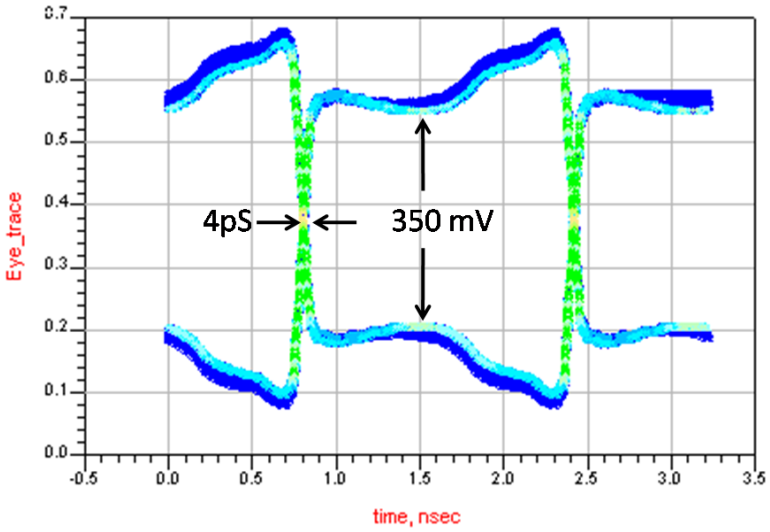

Figure 38. Eye Diagram of 0.8V, 300-MHz clock shown in Figure 36

From the above analysis it can be concluded that, attenuation of significant clock harmonics due to large insertion loss causes huge reduction in its voltage margin but no significant decrease in timing margin.

2.2.2 Impact of Insertion Loss on Jitter and Noise of PRBS Signal

In order to find the impact of insertion loss on PRBS signal, the harmonic content of PRBS signals was found by using Fourier transform. The frequency spectrum of PRBS consists

of harmonics distributed across multiple frequencies. The envelope of the spectrum is a sinc squared function with nulls at the multiples of bit rate of the PRBS. For example the spectrum of 600 Mbps PRBS consists of nulls at multiples of 600 MHz and has significant harmonic content at 900 MHz, 1500 MHz and so on as shown in Figure 39.

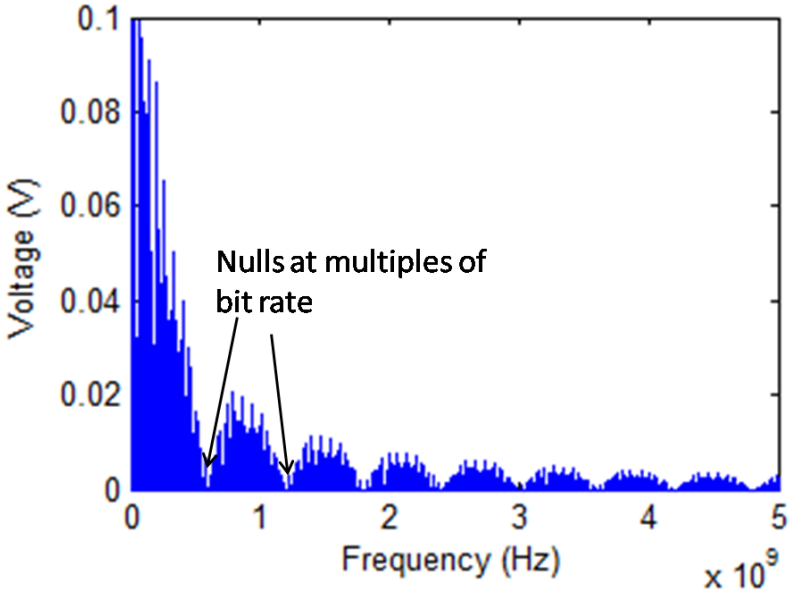

Figure 39. Spectrum of 0.8V, 600-Mbps PRBS signal

If significant harmonics of PRBS coincide with peak in the insertion loss of the signal, they undergo large attenuation reducing the amplitude of the PRBS pulses and increasing their rise/fall times. However, since the energy of PRBS is distributed across multiple frequencies, attenuation of few harmonics does not cause a very large reduction in the amplitude of PRBS signal. Those pulses whose harmonic content coincides with the peak in the signal insertion loss get attenuated and see degradation in rise/fall times. On the other hand, pulses whose harmonics do not coincide with peaks in the insertion loss pass through un-attenuated and don't see much degradation in rise/fall times. As a result of this, the rise/fall times an well as the amplitude of each pulse keeps changing resulting in increase in jitter and decrease in voltage margin. To illustrate this, TS4 was stimulated with 0.8V, 600-Mbps PRBS at Port-1 and the eye pattern was observed at Port-2 (terminated with 50 Ohm resistance). The eye diagram shown in Figure 40 clearly shows a significant jitter of

28pS induced on the PRBS signal.

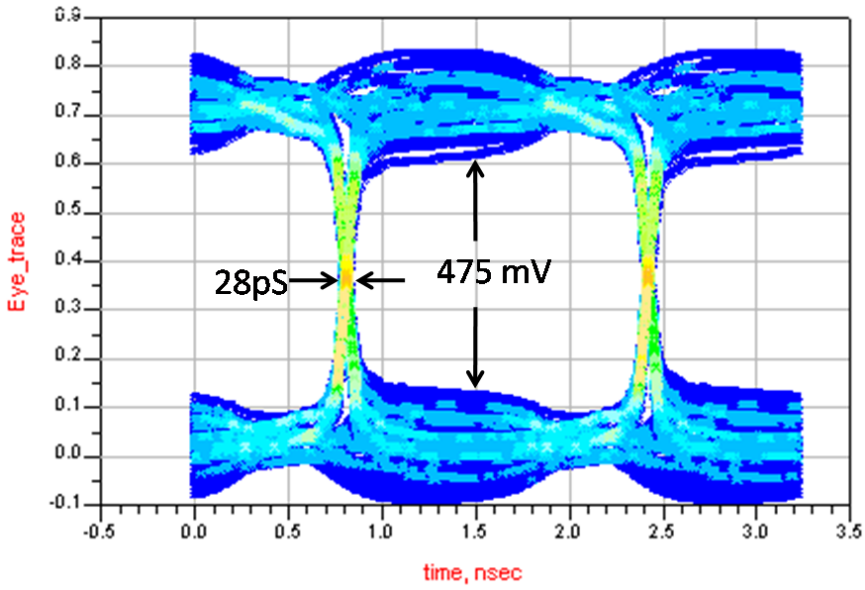

Figure 40. Eye pattern at Port-2 obtained with 0.8V, 600-Mbps PRBS applied at Port-1 of TS-4

From the above analysis it can be concluded that attenuation of significant harmonics of PRBS due to large insertion loss results in both noise and jitter on the signals decreasing its voltage as well as timing margin.

2.2.3 Comparison of Jitter and Noise in the Clock and the PRBS signals

By comparing the spectrum of the clock and the PRBS following conclusions can be made:

1. Comparison of Voltage Margins: Since a lot of energy of the clock signal is concentrated in only a few significant harmonics, attenuation of any one of the significant clock harmonics due to high insertion loss causes large reduction in clock amplitude. On the other hand since the energy of a PRBS is distributed across multiple harmonics, attenuation of few harmonics does not cause a large reduction in amplitude of pulses in case of PRBS. Thus, attenuation of significant harmonics due to high insertion loss in clock causes larger reduction in voltage margin as compared to that of PRBS signal. Comparison the eye pattern of clock and PRBS in Figure 38 and Figure 40 clearly shows that the voltage margin is higher in case of PRBS as compared to

that of clock.

2. Comparison of Timing Margins: Since the clock signal is periodic in nature and the harmonic content remains the same at all times, the increase in rise/fall times due to attenuation of significant harmonics is seen by all the clock pulses. Since, there is not much variation in the rise/fall times between different pulses of the clock, very little jitter is induced in clock signal. On the other hand, the spectrum of PRBS at any given instant of time depends on the bit pattern at that instant. Based on the bit patterns the significant harmonics of PRBS may or may not coincide with peak in the insertion loss of the signal. This leads to different rise/fall delays for different pulses of a PRBS giving rise to jitter. Thus, attenuation of significant harmonics due to high insertion loss in PRBS causes larger reduction in timing margin as compared to that of clock signal.Comparison the eye pattern of clock and PRBS in Figure 38 and Figure 40 clearly shows that the jitter is higher in case of PRBS as compared to that of clock.

2.3 Test Vehicles and Measurement Results

Two test vehicles, TV1 and TV2, were designed and fabricated to validate the analysis done in the previous section. Each test vehicle consists of four layers with microstrips on the top and the bottom layers and ground and power planes on the second and third layer respectively. TV1 consists of two via transitions and TV2 consists of four via transitions respectively. Each via transition causes a return path discontinuity at the via location. Capacitor pads have been provided near each via transition, so that suitable capacitors can be soldered to reduce the PDN impedance at the RPD. The capacitors used had C=4700pF, ESL=0.3nH and ESR=0.25 Ohm. The photographs, schematic, dimensions and port placement of TV-1 and TV-2 are given in Figure 41 and 42 respectively.

Both frequency and time domain simulation and measurements were done to demonstrate the proof of concept described in the previous section. The measurement results are

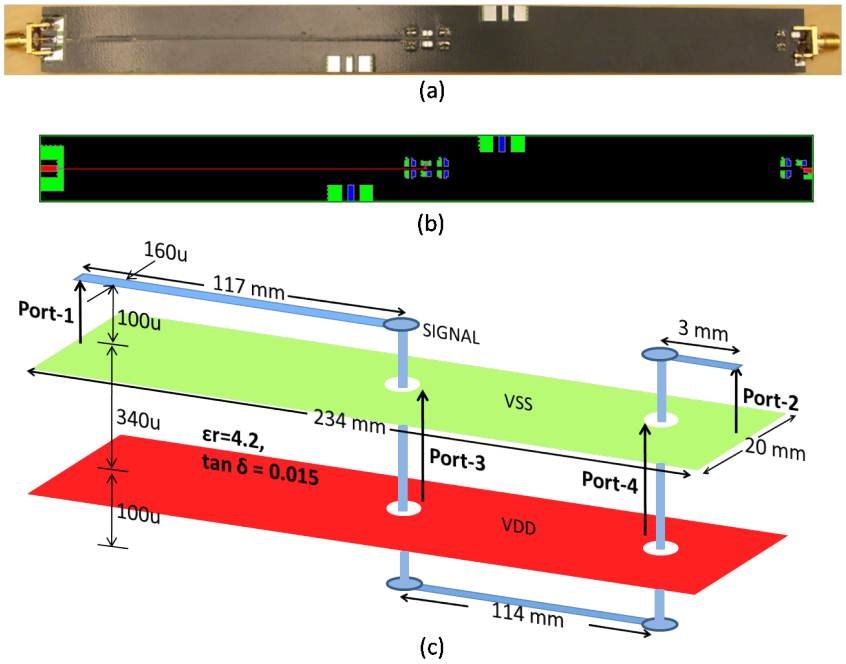

Figure 41. Test Vehicle, TV-1 (a) Photograph of top view (b) Schematic of top-view (c) Dimensions and Port placement

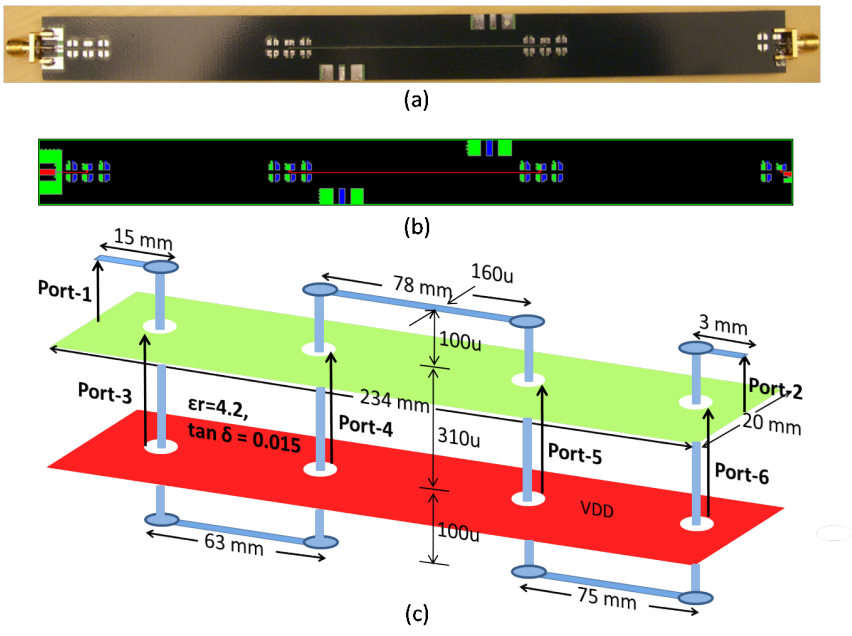

Figure 42. Test Vehicle, TV-2 (a) Photograph of top view (b) Schematic of top-view (c) Dimensions and Port placement

organized into following three sections.

- Comparison of simulation and measurement results for simulation to hardware correlation
- Comparison of measured PDN impedance and insertion loss with and without decoupling capacitors to validate the impact of PDN impedance on insertion loss of the signal.
- Comparison of measured jitter and noise on clock and PRBS signals with and without decoupling capacitors to validate the impact of insertion loss of signal on timing and voltage margins.

2.3.1 Comparison of Simulation and Measurement Results

In this section, comparison of simulation results is done with the measured values of PDN impedance and insertion loss for model to hardware correlation. The simulations were done using Sigrity's PowerSI electromagnetic field solver [17]. The measurements were done using Vector Network Analyser (VNA) with ports defined as shown in Figure 41(c) and Figure 42(c). A comparison of some of the simulated and measured values of PDN impedance and insertion loss have been shown in Figure 43, Figure 44, Figure 45 and Figure 46.

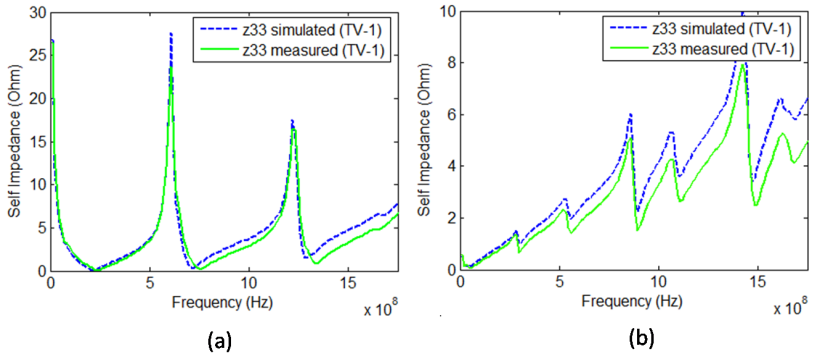

Figure 43. Comparison of simulated and measured values of PDN impedance of TV-1 at Port-3 (a) without decoupling capacitors (b) with decoupling capacitors

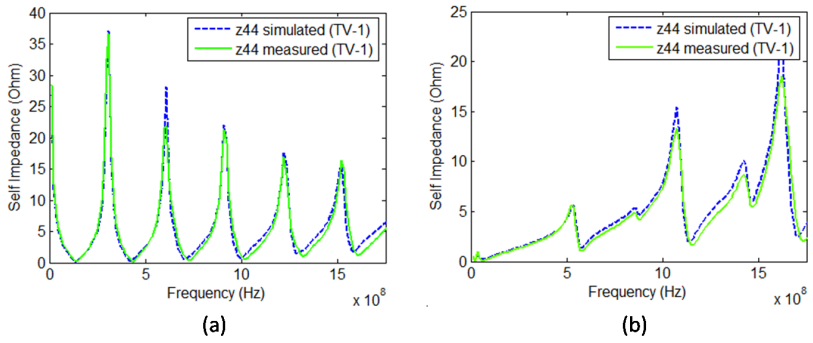

Figure 44. Comparison of simulated and measured values of PDN impedance of TV-1 at Port-4 (a) without decoupling capacitors (b) with decoupling capacitors

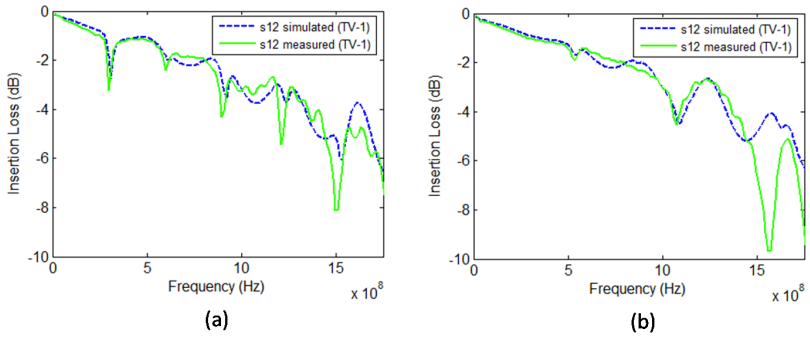

Figure 45. Comparison of simulated and measured values of insertion loss of TV-1 microstrip (a) without decoupling capacitor (b) with decoupling capacitors

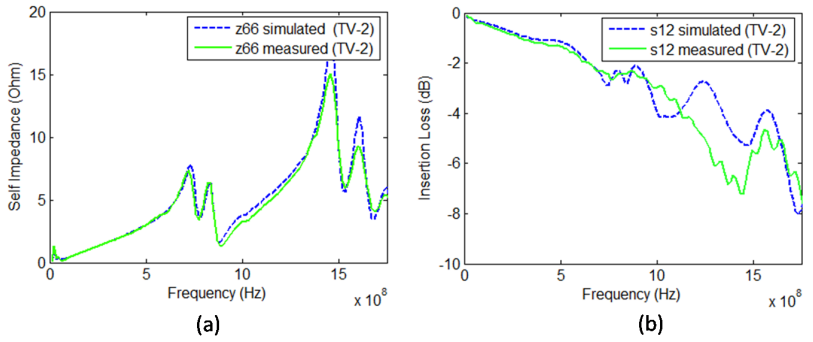

Figure 46. Comparison of simulated and measured values of (a) PDN impedance at Port-6 of TV-2 with decoupling capacitors added (b) insertion loss of TV-2 micro-strip with decoupling capacitors added

From these figures it can be inferred that there is an excellent match between the simulation and measurement results validating the analysis done earlier.

2.3.2 Comparison of Measured PDN Impedance and Insertion Loss with and without Decoupling Capacitors

In this section, the analysis on impact of PDN impedance on the insertion loss of signal with RPD is validated by comparing the PDN impedance and insertion loss profiles with and without decoupling capacitors.

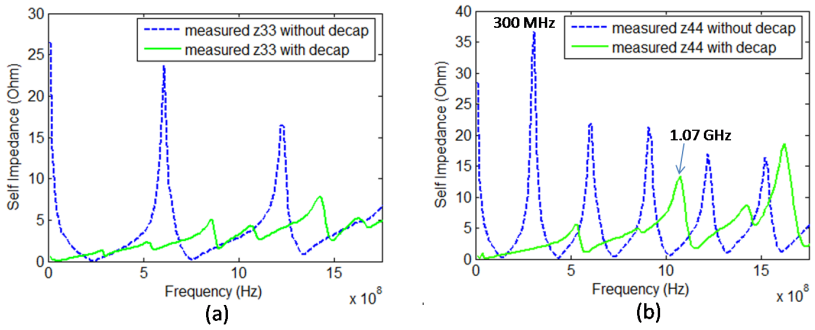

Figure 47. Comparison of measured PDN impedance of TV-1 with and without decoupling capacitor at (a) Port-3 (b) Port-4

A comparison of measured values of PDN impedance at Port-3 and Port-4 of TV-1 with and without decoupling capacitors is shown in Figure 47. Addition of decoupling capacitors removes the anti-resonance in the PDN impedance at 600-Mhz. As a result of this, the peak in insertion loss of TS-1 micro-strip goes away as shown in Figure 48(a).

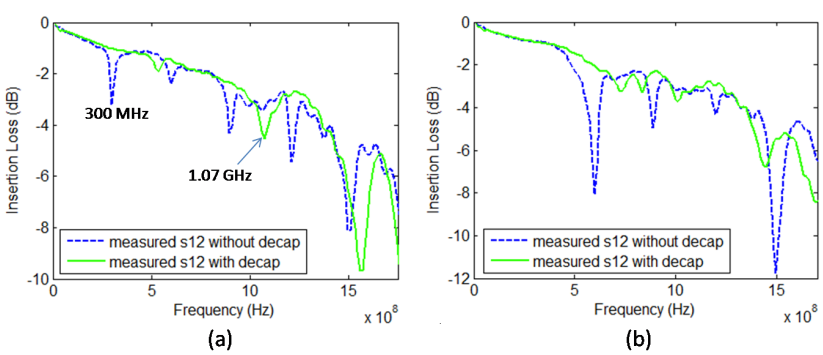

Figure 48. Comparison of measured insertion loss with and without decoupling capacitor for (a) TV-1 (b) TV-2

Similarly, comparison of measured values of insertion loss of TS-2 micro-strip with and without decoupling capacitors is shown in Figure 48(b). Again, it is observed that addition of decoupling capacitors removes the peak in insertion loss of TS-2 micro-strip.

In both the examples above, addition of decoupling capacitors resulted in reduction of the PDN impedance at anti-resonances at low frequencies thereby eliminating the peak in insertion loss. For example, addition of decoupling capacitors removed the anti-resonance in PDN impedance of TV-1 at port-4 at 300 MHz as shown in Figure 47. As a result, the peak in the insertion loss of TV-1 microstrip at 300 MHz goes away with the addition of decoupling capacitor. Also, addition of decoupling capacitors results in new anti-resonances at other frequencies, causing increase in PDN impedance. Due to this, the insertion loss of signal increases at frequencies where new anti-resonances are created. For example, at 1.07 GHz, an anti-resonance in PDN impedance at port-4 of TV-1 is created due to addition of decoupling capacitors. Coresspondingly, the insertion loss of TV-1 mictrostrip has a peak at 1.07 GHz. This validates the analysis that higher values of PDN impedance, especially at anti-resonances causes large increase in the insertion loss of the signal having RPD.

2.3.3 Comparison of Measured Jitter and Noise with and without Decoupling Capacitors

In this section, time domain measurements have been shown to compare jitter and noise on clock and PRBS signals with and without decoupling capacitors. The clock and PRBS signals were given using Agilent 81133A pulse/pattern generator and time domain waveforms were measured using Agilent 86100C digital communications analyzer. In all the measurements, the input signal was applied at Port-1 of the TVs and the output signal was measured at Port-2 (terminated with 50 Ohm resistance).

2.3.3.1 Measurements with PRBS signal

A comparison of the eye diagram of 600-Mbps PRBS signal applied to TV-1 with and without decoupling capacitors is shown in Figure 49. The addition of decoupling capacitor removes the anti-resonances in the PDN impedance and hence the peak in the insertion loss

of the TV-1 micro-strip. Due to this, fewer significant harmonics of PRBS are attenuated with decoupling capacitors added, in comparison to when no decoupling capacitors are added. Hence, the eye diagram with decoupling capacitors added shows smaller noise and jitter compared to the one without decoupling capacitors added. TV-2 eye diagrams show similar trend as seen from Figure 50.

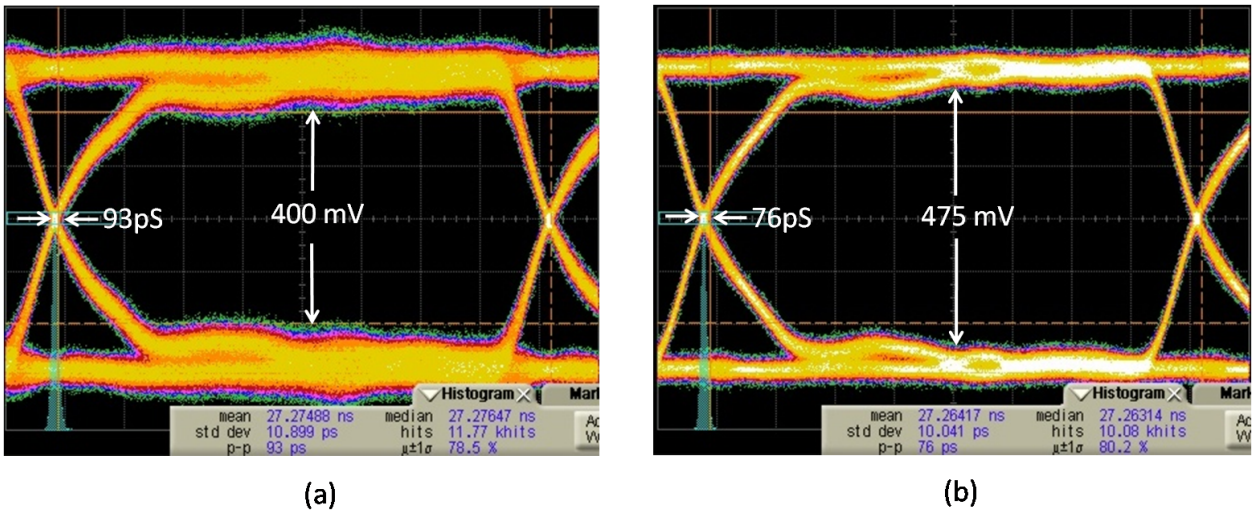

Figure 49. Measured eye diagram at port-2 of TV-1 (a) without decoupling capacitors (b) with decoupling capacitors

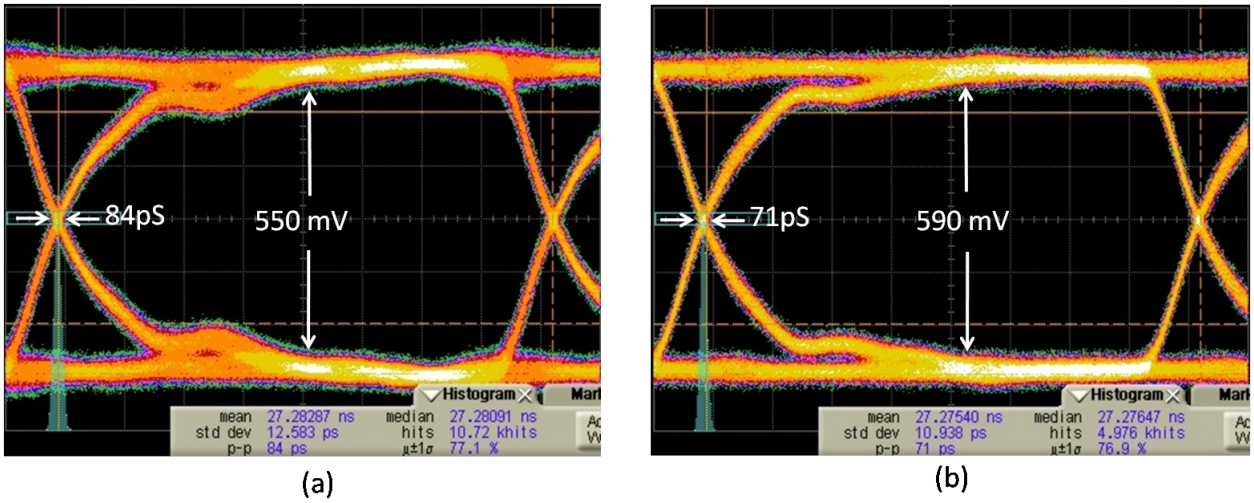

Figure 50. Measured eye diagram at port-2 of TV-2 (a) without decoupling capacitors (b) with decoupling capacitors

A comparison of TV-1 and TV-2 eye diagrams shows that in spite of having fewer

RPDs, TV-1 induces higher noise and jitter in 600-Mbps PRBS than TV-2. To explain this, the frequency spectrum of 600-Mbps PRBS is overlapped with the insertion loss profiles of TV-1 and TV-2 micro-strips as shown in Figure 51. The peak in insertion loss profile of TV-1 micro-strip at 300-MHz coincides with significant harmonics of 600-Mbps PRBS. On the other hand, there are no significant harmonics of 600-Mbps PRBS at the peak in insertion loss of TV-2 micro-strip at 600 MHz. As a result, TV-2 attenuates fewer significant harmonics compared to TV-1 inducing smaller jitter and noise on 600-Mbps PRBS signal.

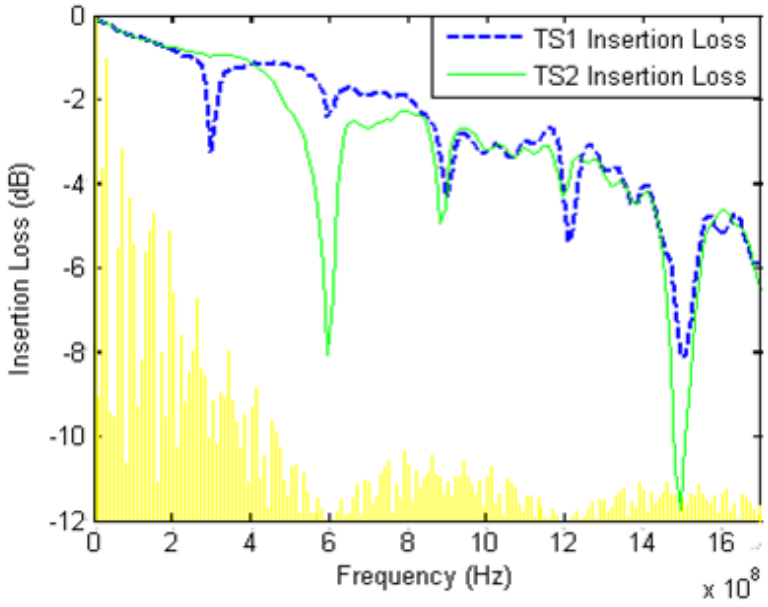

Figure 51. Comparison of insertion loss of TV-1 and TV-2 microstrip

2.3.3.2 Measurements with clock signal

A 0.8V, 600-MHz clock signal is propagated through TS-2 microstrip so that its fundamental harmonic coincides with the peak in the insertion loss of TV-2 at 600-MHz. The attenuation of fundamental harmonic of clock due to peak in the insertion loss causes a large reduction in the amplitude of the clock signal, as shown in Figure 52(a).

When the peak in the insertion loss is removed by adding decoupling capacitors, the clock does not undergo a large reduction in amplitude, as shown in Figure 52(b). As expected, a very little jitter is induced on the clock signal in both the above measurements.

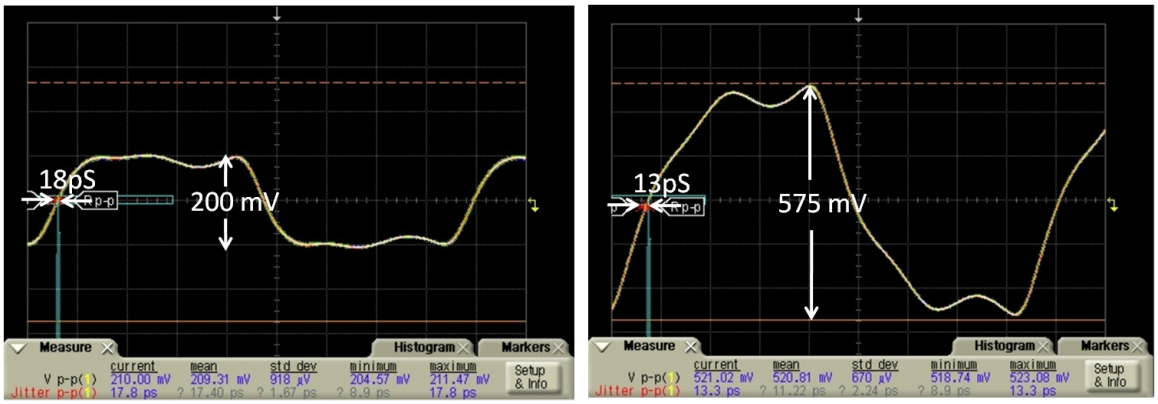

Figure 52. Comparison of 600 MHz clock waveforms at Port-2 of TV-2 (a) without decaps (b) with decaps

These measurements confirm the analysis that attenuation of significant clock harmonics causes larger reduction in its amplitude, but no significant jitter.

Table 1 summarizes the various time domain measurement results.

Table 1. Summary of eye height and jitter obtained from time domain measurements on clock and PRBS signals

Signal Type	0.8V, 600 MHz, Clock		0.8V, 600 MHz, Clock	
Test Structure	Jitter	Amplitude	Jitter	Eye Height
TV-1 without decap	15 pS	590 mV	93 pS	400 mV
TV-1 with decap	12 pS	680 mV	76 pS	475 mV
TV-2 without decap	18 pS	200 mV	84 pS	550 mV
TV-2 with decap	13 pS	575 mV	71 pS	590 mV

The measurements on both the clock and PRBS confirm the validity of the analysis done in the previous section.

2.4 Design Guidelines to Minimize Jitter and Noise on Signals

From the analysis done in section 2, it is found out that the jitter and noise on the signal is primarily due to significant harmonics being attenutated by the peaks in the insertion loss. Therefore, jitter and noise on the signal can be minimized by removing the peaks in the insertion loss. Based on this idea, the following design guidelines have been suggested:

1. The PDN impedance at RPDs should be minimized. Suitable decoupling capacitors

might be added for the same

2. For a given PDN, the RPDs should be chosen at the point of minimum PDN impedance.

3. Multiple RPDs at optimal locations can be used to reduce the impact of PDN impedance on insertion loss of the signal at desired frequencies.

4. The PDN design should be done in such a way that the anti-resonances do not coincide with significant harmonic content of the signals supported on the system.

5. Passive equalization networks can be designed to remove the resonant peaks in the insertion loss of the signal [18]. Passive equilization involves addition of passive components in the channels to improve the frequency response of a given transfer function. Equalization networks can be placed on the PCB so as to optimize the insertion loss of the signal traces as shown in Figure 53.

Figure 53. Equalization network to improve the insertion loss profile of the signal and minimize SSN induced jitter and noise

2.5 Summary

In this chapter correlation of PDN impedance with jitter and voltage margin was done, first, by determining the impact of PDN impedance on insertion loss of the signal, and then by determining the impact of insertion loss of the signal on SSN induced jitter and noise. Simple test structures consisting of one or more return path discontinuities were simulated in both frequency and time domain. It was found out that the PDN impedance at return path discontinuity affects the insertion loss profile of the signal having RPD. Anti-resonances in the PDN impedance cause peaks in the insertion loss of the signal. When significant harmonics of signals such as clock and PRBS are attenuated, they cause reduction in amplitude and increase in rise/fall times of the signals. Different degrees of attenuation and

changing rise/fall times of pulses give rise to jitter and noise on the signal degrading its timing and voltage margins. Attenuation of significant clock harmonics causes large reduction in voltage margin but only a small amount of jitter, while attenuation of harmonics of PRBS causes smaller reduction in voltage margin, but large reduction in timing margin as compared to that of a clock. Hardware measurements on structures similar to the simulated test structures confirm the validity of the analysis. Finally, design guidelines have been formulated to help reduce jitter and noise in high speed channels.

CHAPTER 3

AUTOMATED PLACEMENT OF DECOUPLING CAPACITORS TO REDUCE PDN IMPEDANCE

In Chapter-2, reduction of PDN impedance at RPD was suggested as one of the design practices to reduce jitter and noise in high speed channels. In order to reduce PDN impedance, decoupling capacitors (decaps) are added in the power delivery network as shown in Figure 54 [3].

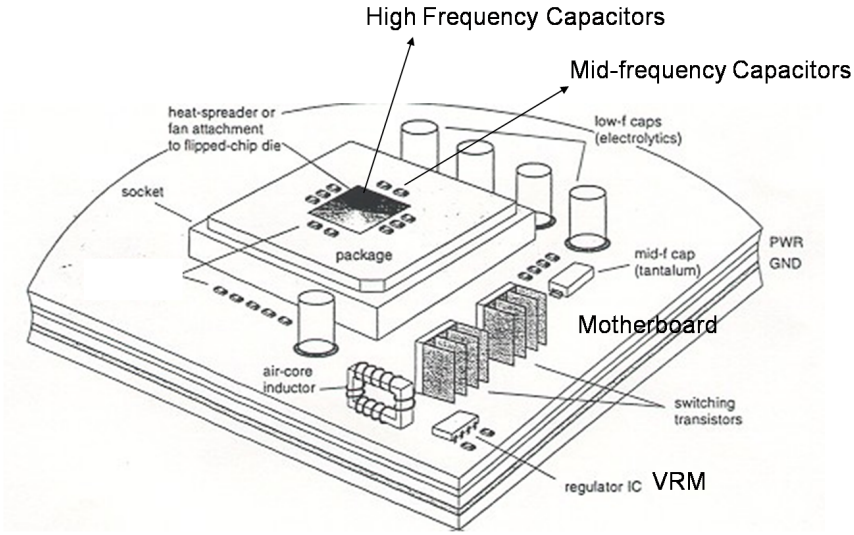

Figure 54. Placement of decoupling capacitors on PDN to reduce PDN impedance (*Reproduced from [3]*)

The decoupling capacitors act as charge reservoirs and supply transient currents required by switching circuits. Due to proximity of decoupling capacitors to the switching circuits the switching current sees a smaller inductance and hence a smaller value of SSN is induced. Thus, decoupling capacitors help to minimize SSN by reducing the PDN impedance.

However, in reality finite inductance and resistance called ESL and ESR respectively are associated with each decoupling capacitor as shown in Figure 55.

Due to the parasitic inductance and resistance, a decoupling capacitor is effective only till its self resonant frequency (SRF) given by equation 11. For frequencies greater than the

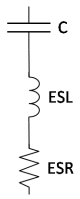

Figure 55. Parasitics associated with a practical decoupling capacitor

SRF, the decoupling capacitor behaves like and inductor.

$$f_{resonance} = \frac{1}{2\pi\sqrt{LC}} \tag{11}$$

where, $f_{resonance}$ is the self resonant frequency, L is the inductance of ESL and C is the capacitance of the capacitor.

In order to minimize the PDN impedance over a broad range of frequency, multiple decoupling capacitors with different SRF values are added to the PDN. The PCB contains the low-SRF capacitors, the package contains mid-SRF and the chip has the high-SRF capacitors. Adding multiple decoupling capacitors reduces the PDN impedance at certain frequencies but causes impedance maxima at other frequencies, due to parallel resonance or anti-resonance between ESL of one capacitor and capacitance of other capacitor. Figure 56 [3] shows typical profile of PDN impedance in the presence of PCB, package and on-chip decoupling capacitors. The PDN impedance profile depends on the values of decaps and their location on the power delivery network. Therefore, a proper selection of decaps and their location is required to meet the target impedance.

Since, there are infinite combinations of values and locations of decoupling capacitors, manual placement of decoupling capacitors is a tedious and time consuming. Also, the problem of decoupling capacitor placement is not deterministic as addition of decoupling capacitors changes the behavior of the system being solved. As a result, a stochastic search of design space is needed to determine optimal placement of decoupling capacitors in a power delivery network.

Genetic algorithm is a popular algorithm to optimize problems where stochastic search

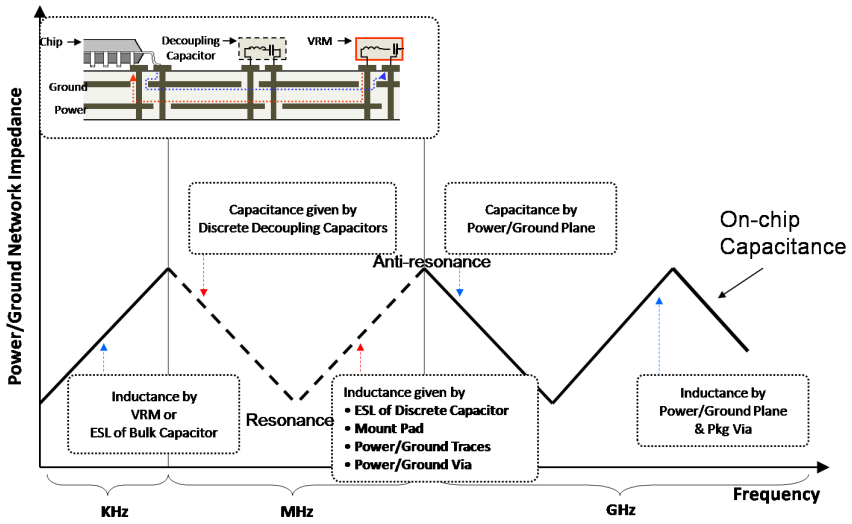

Figure 56. Typical PDN impedance profile due to interaction between various components of PDN (*Reproduced from [3]*)

of design space is required [19]. In this chapter, genetic algorithm based on multi layered finite difference method (M-FDM) has been suggested for automatic placement of decoupling capacitors to reduce the PDN impedance below a given target impedance over a specified range of frequency.

Prior work in optimization of decap placement using GA involved random placement of decoupling capacitors during the initialization process [20]. However, this results in larger convergence time as the placement of capacitors does not consider the location of the ports where PDN impedance has to be reduced. A new methodology of generating the initial population based on port locations has been suggested so as to reduce the number of iterations required to converge to the optimal solution. The rest of the chapter is organized into following sections:

- Genetic Algorithm (GA) applied to the problem of placement decoupling capacitors
- Test Cases and Simulation Results

3.1 Genetic Algorithm to Optimize Decoupling Capacitor Placement

The genetic algorithm (GA) uses techniques inspired by evolutionary biology so that given set of possible solutions evolve towards better solutions. In this section, the genetic algorithm as applied to the problem of decoupling capacitor placement is explained.

3.1.1 GA Terminology

Some of the terms used in GA applied to decoupling capacitor placement are explained below.

1. Chromosome: A chromosome represents one of the many possible solutions to the problem being solved. For GA applied to decap placement, a possible solution represents the choice and location of the decaps on the PDN. Therefore, each chromosome contains information on the choice and location of every decap used in the solution. For example, consider a PDN consisting of power/ground plane pair with 25 possible locations for adding decoupling capacitors as shown in Figure 57(a). Let one of the possible decap placement solutions be as shown in Figure 57(b). The chromosome corresponding to this solution is shown in Figure 57(c). In case of multi-layered PDN, the chromosome also has the information of layer location of the decap.

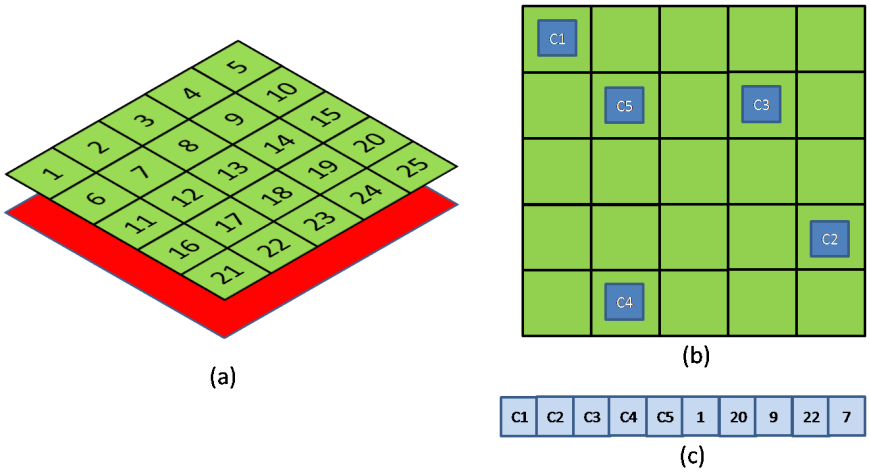

Figure 57. Explanation of chromosome structure (a) Power/Ground Plane pair with possible capacitor locations numbered (b) Top view showing capacitor placement (b) Chromosome

2. Population: Population represents the set of possible solutions used in GA. It is equal to the number of chromosomes GA works on to evolve the given solutions to better and more optimal solutions.

3. Cross over: Cross over is one of the steps in GA where the two chromosomes interact to give rise to a third possibly better chromosome. The two chromosomes involved in cross over are called parent chromosomes, while the new chromosome produced is called the child. The child inherits some characteristics from the first parent and the other characteristics from the second parent. The percentage of inheritance from each parent is determined by the cross over location which is random. The probability of cross-over happening is called cross over rate.

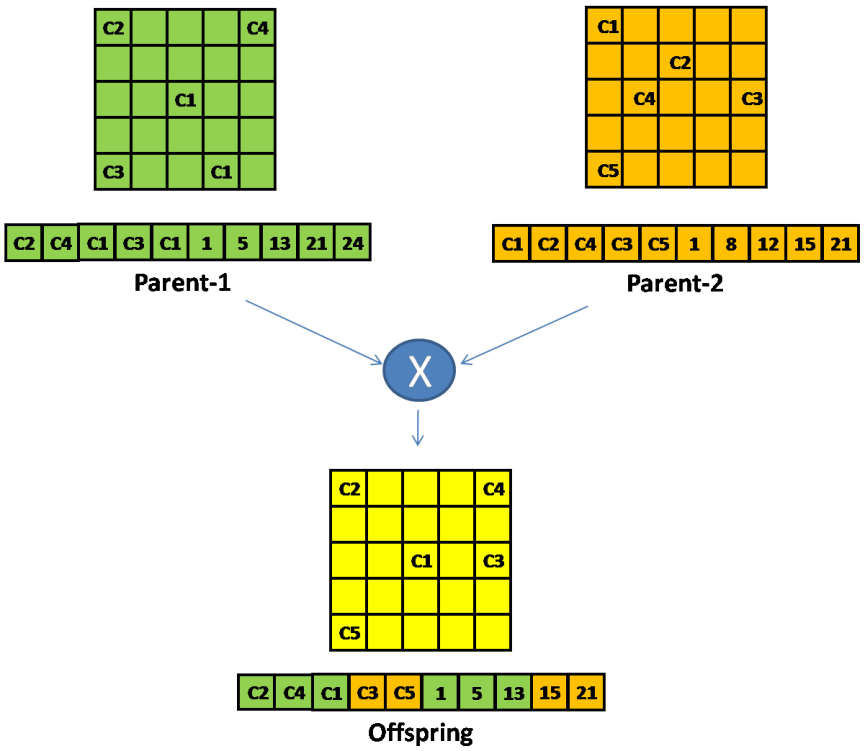

Figure 58. Explanation of cross over of parent chromosomes to produce offspring

A simple example to explain cross over is explained in Figure 58. The cross over of Parent-1 and Parent-2 chromosomes results in an offspring chromosome that inherits the location of C2, C4 and C1 from Parent-1 and, C3 and C5 from Parent-2.

4. Mutation: Genetic algorithm has a tendency to converge towards local optima or arbitrary solutions rather than the global optimum of the problem. To avoid convergence to local optima at the expense of global optima, random changes are introduced in the offspring produced after crossover [19]. These random changes are called mutation. Mutation causes a random change in chromosome causing a modification in the solution. Small changes increase the probability of solution converging but the convergence is more likely towards local optima. On the other hand, large changes increase the probability of solution converging to global optima, at the expense of rate of convergence. The probability of mutation happening called the mutation rate can be also be controlled to alleviate the problem of solution converging to local optima.

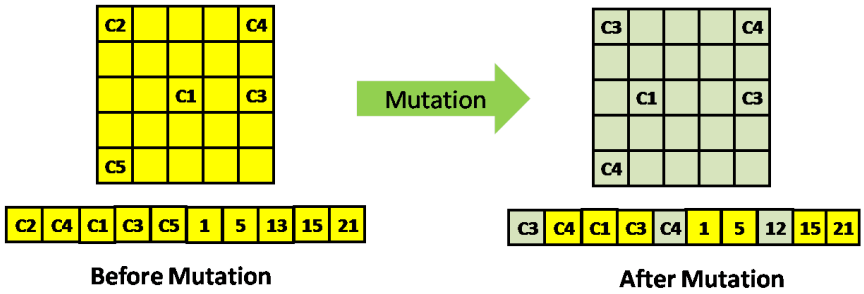

Figure 59. Explanation of mutation in offspring

A simple example to explain mutation is shown in Figure 59. The capacitor C2 and C5 change to C3 and C4 respectively, whereas there is a small change in position of capacitor C1. In order to ensure that only small changes in solutions occur, it is necessary to number the capacitors either in ascending or descending order of their self resonant frequencies.

3.1.2 GA Applied to Decap Placement Problem

The flow chart of GA applied to decap placement problem is shown in Figure 60. The various steps of GA are explained below.

1. Getting Specifications and Inputs: The specifications to GA are the target impedance

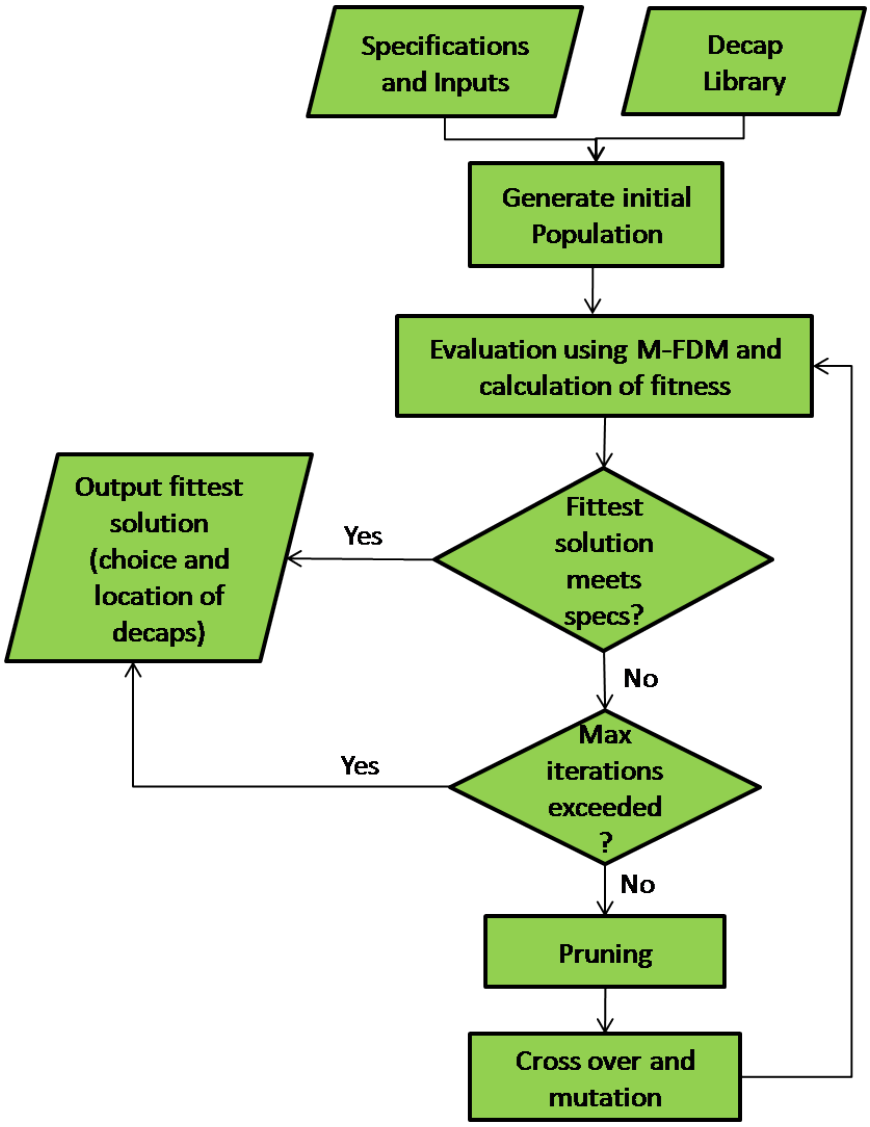

Figure 60. Flowchart explaining GA applied to decap placement problem

and the frequency range over which the target impedance is to be met. The inputs to GA include:

- The package or PCB layout.
- Decap Library: The decap library consists of a list of available decaps with their ESL and ESR values. The decaps should be arranged either in ascending or descending order of their self resonant frequency to enable faster convergence of GA.

- Number of Capacitors to be used (N_{cap})
- GA population ($GAPop$): GA populations controls the number of solutions GA has to work on to evolve them into better solutions. A high value of population requires larger run time, but might lead to faster convergence.
- Cross over rate (p_c): The probability of cross over can be specified using the cross over rate.
- Mutation rate (p_m): The probability of mutation can be specified by specifying the mutation rate.

2. Generation of initial population (Initialization): Initialization involves generation of many individual solutions to form an initial population. In the previous work on GA applied to decap placement problem, the individual solutions generated initially were completely random in nature. The capacitors were chosen randomly and the locations were independent of port locations. In the proposed work, the generation of initial population is based on the port locations. The capacitors are placed closer to the noise ports as this results in smaller impedance at the port. The region area around the port where capacitors are to be placed can be specified based on the application.

3. Evaluation and calculation of fitness: Each of the potential solutions is evaluated using M-FDM field solver to calculate the impedance at each of the ports the impedance has to be reduced. The fitness of each solution is then calculated using the fitness function given in equation 12.

$$fitness = \sum_{i=1}^{N_{port}} \left[\sum_{j=1}^{N_{freq}} (Z_{tar,i} - Z_{i,i}(j)) \times bandcoverage \right] \tag{12}$$

where, N_{port} = Number of ports where the PDN impedance has to be reduced

N_{freq} = Number of frequency points where PDN impedance is evaluated

bandcoverage = Percentage of frequency points where target impedance has been met.

4. Checking if specifications are met: If the solution with highest fitness meets the specification or if number of iterations equal the maximum allowed iterations, the algorithm terminates with output as the solution with highest fitness. If the specifications are not met and more iterations are allowed, the algorithm goes to the next step - Pruning.

5. Pruning: The potential solutions are arranged in the order of their fitness. The solution set is then pruned to retain only the potential solutions with high fitness values. The number of solutions retained is equal to the specified value of N_{elite}. Optimal value of N_{elite} can be chosen based on the application to get the fastest possible convergence.

6. Cross over and Mutation: The top N_{elite} solutions undergo cross over and mutation to produce next generation of solutions or chromosomes (offspring). The top N_{elite} solutions are retained in the next generation to prevent the solution from becoming worse in the next generation.

   The next generation again undergoes fitness check, pruning, cross over and mutation till the the specifications are met or maximum allowed iterations are completed.

3.2 Test Cases and Results

The genetic algorithm for automated placement of decoupling capacitor was tested on two test cases. The test cases and results obtained are summarized in the next two sections.

3.2.1 Test Case, TC-1

The test case, TC-1, consists of a simple power/ground plane pair as shown in Figure 61. The decap placement optimization was done to keep the self impedance of port-1 (Z_{11}) and transfer impedance (Z_{12}) between port-1 and port-2 below the target impedance. The self

impedance (Z_{11}) and transfer impedance (Z_{12}) of TC-1 without any decaps added between the power and ground plane pair is shown in Figure 62.

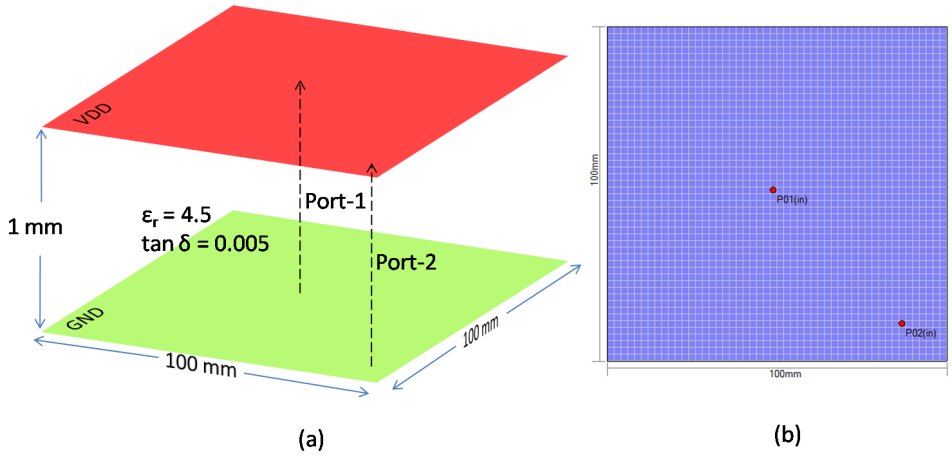

Figure 61. Test case, TC-1 (a) Port placement and dimensions (b) Top-view

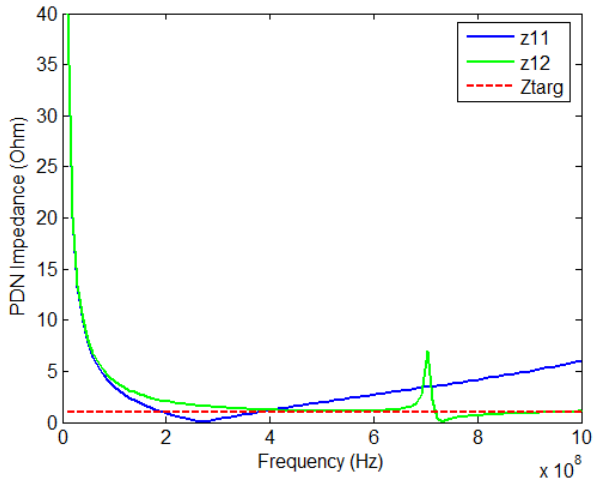

Figure 62. Self and transfer impedance of TC-1 without any decaps

The algorithm was tested with the following inputs and specifications:

- Decoupling capacitor library shown in table 2
- Z_{11_targ} = 1 Ohm
- Z_{12_targ} = 1 Ohm
- Frequency range: 10 MHz to 1 GHz

- Number of capacitors (N_{cap}) = 10
- GA Population ($GAPop$) = 30
- Number of elite chromosomes (N_{elite}) = 10
- Cross over rate (p_c) = 0.5
- Mutation rate (p_m) = 0.2

Table 2. Table summarizing the C, ESL and ESR values of capacitors used

S.No	C	ESR ($m\Omega$)	ESL (nH)	S.No	C	ESR($m\Omega$)	ESL(nH)
1	27pF	850.0	0.4	13	8.2 nF	88.9	0.519
2	33pF	700.0	0.4	14	19.8 nF	44.3	0.572
3	130pF	373.4	0.458	15	41.1 nF	25.7	0.435
4	174.4pF	313.1	0.509	16	83 nF	19.9	0.416
5	207.1pF	243.1	0.468	17	179 nF	15.9	0.548
6	304.7pF	148.6	0.413	18	379 nF	14.1	0.543
7	511.4pF	139.8	0.4	19	0.81 uF	9.8	0.485
8	595.8pF	120.0	0.432	20	1.93 uF	6.7	0.686
9	1.0nF	75.0	0.370	21	3.86 uF	4.8	0.703
10	2.2nF	62.1	0.426	22	7.87 uF	5.5	0.876
11	2.9nF	203.8	0.533	23	21.2 uF	2.7	1.628
12	4.2nF	141.1	0.523	24	81.2 uF	2.4	2.834

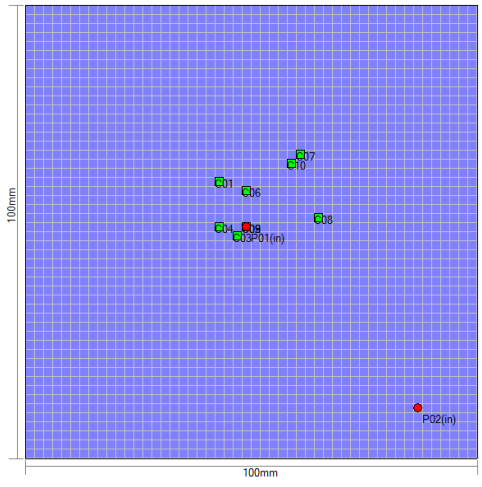

Figure 63. Decap choice and placement obtained from GA

The port location based GA applied to TC-1 took 12 iteration to complete. The fitness value increased from -534.6602 to 3404.6156 and the band coverage (percentage frequency points over which target impedance was met) increased from 56% to 100%. The progress of the algorithm after every iteration has been shown in Appendix A. The choice and location of the capacitors obtained from GA are shown in Figure 63. On the other hand, GA based on random initialization could not meet the target impedance even with 50 iterations. The log file of GA based on random placement of decoupling capacitors is shown in Appendix B.

A comparison of self impedance (Z_{11}) with random, manual and GA optimized decap placement is shown in Figure 64. A similar comparison of transfer impedance is shown in Figure 65.

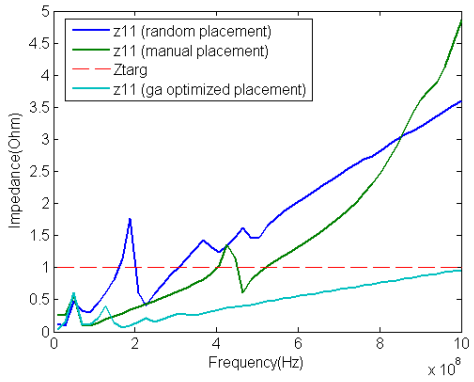

Figure 64. Comparison of self impedance at port-1 of TC-1 obtained with random decap placement and GA based decap placement

From the comparison of self and transfer impedances obtained by random, manual and GA optimized decap placements, it can be inferred that optimized capacitor placement using GA gives better results compared to both random and manual placement.

3.2.2 Test Case, TC-2

The test case, TC-2, is similar to the test structure, TS-4 described in Chapter-2. The test case is shown again in Figure 66 for reference. The decap placement optimization was done using genetic algorithm to keep the self impedance of port-3 (Z_{33}) and port-4 (Z_{44}) below

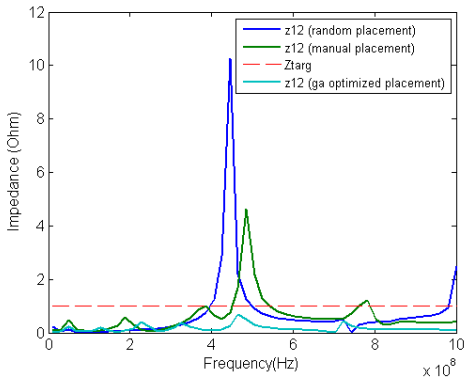

Figure 65. Comparison of transfer impedance between at port-1 and port-2 of TC-1 obtained with random decap placement and GA based decap placement

the target impedance of 1-Ohm, to reduce the noise and jitter induced on TC-2 micro-strip. The impedances at port-1 and port-2 in the absence of any decoupling capacitors have been shown in Figure 67.

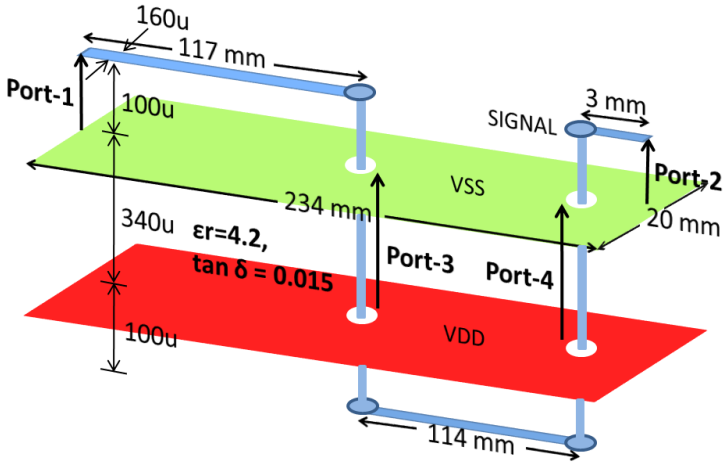

Figure 66. Test case, TC-2

The following inputs and specifications were used.

- Decoupling capacitor library shown in table 2
- Z_{11_targ} = 1 Ohm
- Z_{22_targ} = 1 Ohm
- Frequency range: 10 MHz to 1 GHz

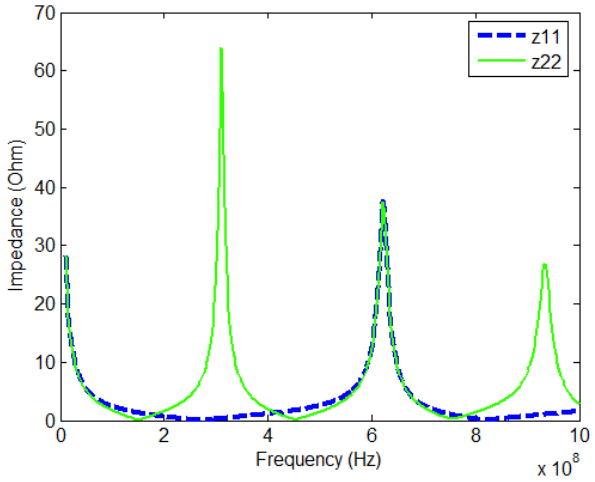

Figure 67. Self impedance of TC-2 at port-3 and port-4 without any decaps

- Number of capacitors (N_{cap}) = 20
- GA Population ($GAPop$) = 30
- Number of elite chromosomes (N_{elite}) = 10
- Cross over rate (p_c) = 0.5
- Mutation rate (p_m) = 0.2

GA applied to TC-2 took 40 iterations to complete. The fitness value increased from 356.6962 to 2063.0679 and the band coverage (percentage frequency points over which target impedance was met) increased from 61.25% to 100%. The progress of the algorithm after every iteration has been shown in Appendix C. The choice and location of the capacitors obtained from GA are shown in Figure 68. On the other hand, GA based on random initialization could not meet the target impedance even with 49 iterations. The log file of GA based on random placement of decoupling capacitors is shown in Appendix D.

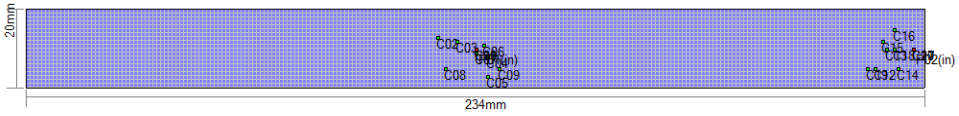

Figure 68. GA optimized capacitor placement for TC-2

A comparison of self impedances (Z_{33} and Z_{44}) obtained using random, manual and GA optimized decap placement is shown in Figure 69. From these comparisons it can be inferred that GA is an effective algorithm for decap placement as it gives better results compared to both the random and manual placement.

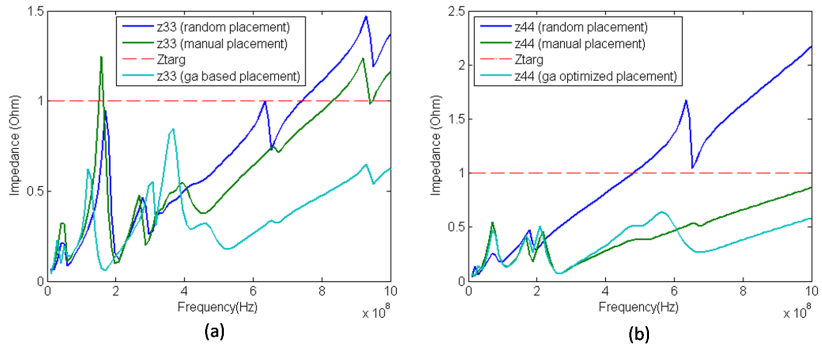

Figure 69. Comparison of self impedances of TC-2 with and without GA optimized decap placement at (a) Port-3 (b) Port-4

A comparison of eye diagrams measured at port-2 by exciting port-1 with 600-Mbps PRBS is shown in Figure 70. From Figure 70, it can be inferred that reduction of PDN impedance by proper placement of decoupling capacitors using GA reduces the jitter and increases the voltage margin of the signal.

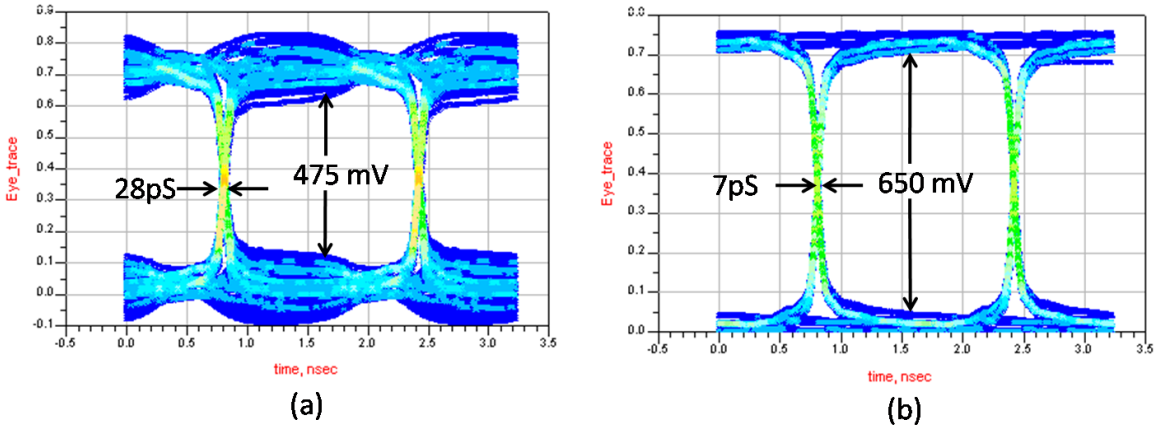

Figure 70. Eye diagram showing jitter and noise on TC-2 microstrip (a) without decoupling capacitor placement (b) with decoupling capacitors placed using GA

Thus, optimizing the decoupling capacitor placement using GA, is an effective way to reduce the PDN impedance and increase the timing and voltage margin.

3.2.3 Proposed Test Vehicle for Model to Hardware Correlation

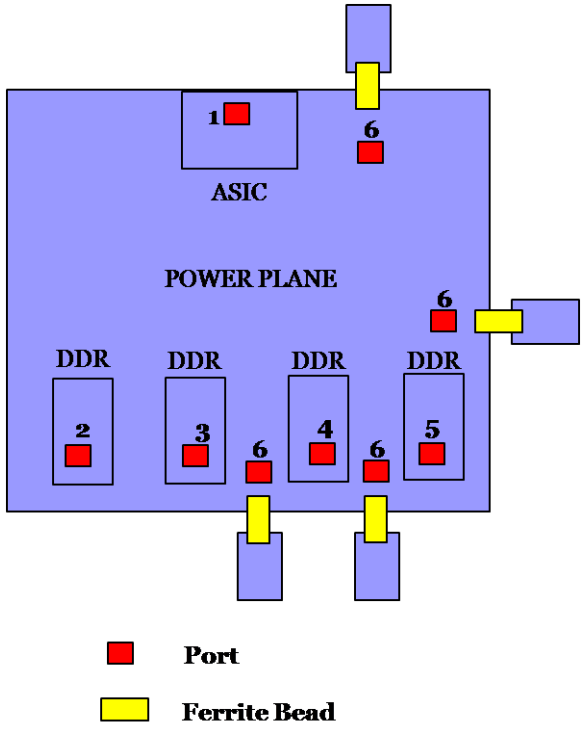

Figure 71. Test vehicle for model to hardware correlation to demonstrate the efficacy of GA based decap optimizer

The test vehicle shown in Figure 71 is being designed to validate the proof of concept using model to hardware correlation. The test vehicle represents a typical design scenario that arises in high speed channel design. The application specific integrated circuit (ASIC) and and double data rate synchronous dynamic random access memory (DDR-SDRAM) chips are placed on the PCB as shown in Figure 71. The ASIC and the DDR belong to the same voltage domain and hence are on the same voltage plane. In order to reduce the noise coupling from the ASIC to other sensitive modules, the power is supplied to the ASIC and the DDRs using ferrite bead. The ferrite bead can be placed at any of the locations represented by port-6 so as to achieve minimum coupling from ASIC to the VRM. Also, in order to reduce the SSN induced due to switching of drivers in ASIC and the DDR, the PDN impedance is to be minimized at the location where ASIC and DDR are placed.

The problem thus reduces to placement of decoupling capacitors on the PCB to minimize Z_{11}, Z_{22}, Z_{33}, Z_{44}, Z_{55} to reduce the SSN and to minimize S_{16} to minimize the coupling between the ASIC and other sensitive modules. The GA based decap optimizer can be effectively used to optimize the capacitor placement to archive the target impedance and required isolation in the test vehicle described above.

The test vehicle is being designed and the results are not included in this thesis.

3.3 Summary

In this chapter, genetic algorithm for automated placement of decoupling capacitors to reduce PDN impedance was presented. The algorithm involves improvement of initial set of potential solutions using principles inspired by biological evolution. Initial set of solutions are generated either randomly or based on heuristics. These initial solutions, organized as chromosomes, then undergo evaluation, pruning, cross over and mutation repeatedly till the target impedance is met. The efficacy of the algorithm is demonstrated by testing it on two test cases. Based on both frequency and time domain simulations results obtained from the two test cases, it can be inferred that the algorithm converges faster and gives better results compared to random placement of decoupling capacitors. Thus, GA is an effective algorithm that can be employed to solve the problem of selection and placement of decoupling capacitors in the design of PDN.

CHAPTER 4

CONCLUSIONS AND FUTURE WORK

A detailed analysis of the effect of PDN impedance on timing and voltage margin has been done. It is shown that anti-resonances in PDN impedance cause significant increase in the insertion loss of interconnect whose return current is disrupted at return path discontinuities. The increase in insertion loss may attenuate significant harmonics of a signal degrading its rise/fall times and voltage level leading to decreased timing and voltage margins. Therefore, the jitter and noise on the signal depends not only on the insertion loss of the signal but also on its harmonic content.

The clock and the PRBS represent typical signals present in high speed channels. The energy of the clock signals is concentrated in few harmonics which are present at odd multiples of clock frequency. Therefore, attenuation of these harmonics due to peak in the insertion loss causes larger reduction in clock amplitude and voltage margin. However, though the attenuation of significant clock harmonics increases the rise/fall times of the clock pulses, the increase is uniform across all the clock pulses. As a result, no significant jitter is induced in clock.

The PRBS signal, on the other hand, has its energy distributed across multiple harmonics whose envelop is a sinc squared function with nulls at the multiples of bit rate. As a result of this, attenuation of significant harmonics due to peak in the insertion loss of the signal causes only a slight reduction in amplitude and increase in rise/fall time of the pulses. However, due to random nature of PRBS, the decrease in amplitude and increase in rise/fall times is not uniform across all the pulses of PRBS. This leads to noise as well as jitter in PRBS signals causing both timing and voltage margins to reduce.

The above analysis has been validated by doing hardware measurements on simple test vehicles having two or more microstrip to microstrip via transitions. Both frequency and time domain measurements on the test vehicles show a good model to hardware correlation

validating the analysis. Based on the analysis, it can be inferred that it is possible to predict jitter and noise on the signal from the PDN impedance profile. Also, based on the analysis, it can be established that jitter and noise on the signal can be reduced by reducing the PDN impedance.

Suitable placement of decoupling capacitors is suggested to reduce the PDN impedance below the target impedance, so as to reduce the jitter and noise on the signal. Genetic algorithm applied to the problem of selection and placement of decoupling capacitor has been implemented and its efficacy has been verified by taking a simple power/ground plane pair as a test case.

As an extension to research described in this thesis, following future work is proposed:

- The qualitative analysis of relation between PDN impedance, jitter and voltage margin has been presented in this thesis. The idea can be extended to do a quantitative analysis in order to find the exact value of noise and jitter on the signal for a given PDN impedance profile. The block diagram in Figure 72 illustrates how this can be done.

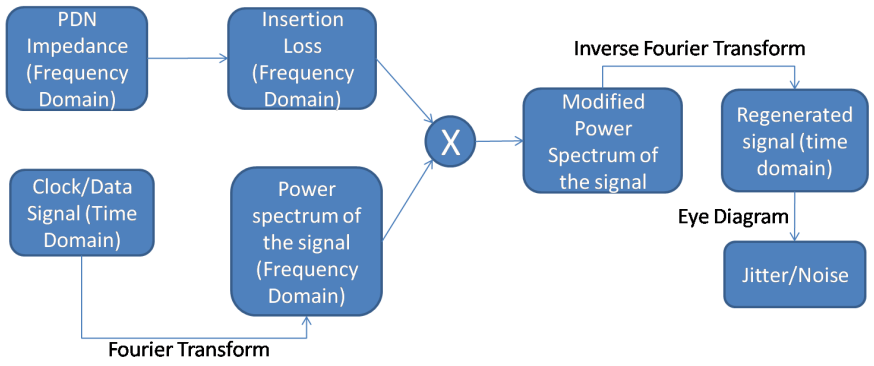

Figure 72. Proposed methodology for calculation of exact value of jitter and noise from the PDN impedance profile

Based on the location of RPD, the insertion loss profile of the signal can be obtained from the PDN impedance profile at the RPD. The time domain signal can then be converted to frequency domain using Fourier transforms. In frequency domain, the individual harmonics of the signal can be scaled based on the value of insertion loss at

that frequency. The scaled harmonics can then be used to regenerate the time domain signal using inverse Fourier transforms. Finally, the regenerated time domain signal can be used to construct an eye diagram from which exact value of jitter and noise can be calculated.

- The genetic algorithm for automated placement of decoupling capacitors presented in this thesis is based on placement of capacitors near the ports to generate the initial population. Since, the quality of initial population has a large impact on the quality of the final solution, other analytical methods can be used to generate the initial population. The concept can also be extended to placement of decoupling capacitors on chip to reduce the noise induced in the power delivery network at critical locations or hot-spots.

APPENDIX A

LOG FILE OF PORT LOCATION BASED GA APPLIED TO TC-1

The progress of port location based decap placement GA optimizer applied to TC-1 is shown below.

Iteration: 1 Fitness: -534.6602 Band coverage: 56

Iteration: 2 Fitness: -375.3833 Band coverage: 57

Iteration: 3 Fitness: 1866.7728 Band coverage: 80

Iteration: 4 Fitness: 2917.7435 Band coverage: 95

Iteration: 5 Fitness: 2917.7435 Band coverage: 95

Iteration: 6 Fitness: 3025.5332 Band coverage: 97

Iteration: 7 Fitness: 3167.7565 Band coverage: 97

Iteration: 8 Fitness: 3202.5124 Band coverage: 98

Iteration: 9 Fitness: 3218.8676 Band coverage: 98

Iteration: 10 Fitness: 3298.3086 Band coverage: 99

Iteration: 11 Fitness: 3298.3086 Band coverage: 99

Iteration: 12 Fitness: 3404.6156 Band coverage: 100

APPENDIX B

LOG FILE OF RANDOM INITIALIZATION BASED GA APPLIED TO TC-1

The progress of GA optimizer for decap placement with random initialization applied to TC-1 is shown below.

Iteration: 1 Fitness: -391.3396 Band coverage: 52.381

Iteration: 2 Fitness: -379.5541 Band coverage: 54.7619

Iteration: 3 Fitness: -229.126 Band coverage: 57.1429

Iteration: 4 Fitness: -175.7942 Band coverage: 61.9048

Iteration: 5 Fitness: -138.6014 Band coverage: 59.5238

Iteration: 6 Fitness: -138.1777 Band coverage: 59.5238

Iteration: 7 Fitness: -96.7081 Band coverage: 64.2857

Iteration: 8 Fitness: -4.0277 Band coverage: 59.5238

Iteration: 9 Fitness: 0.79263 Band coverage: 61.9048

Iteration: 10 Fitness: 416.018 Band coverage: 78.5714

Iteration: 11 Fitness: 420.636 Band coverage: 78.5714

Iteration: 12 Fitness: 427.1801 Band coverage: 78.5714

Iteration: 13 Fitness: 427.8906 Band coverage: 78.5714

Iteration: 14 Fitness: 435.2483 Band coverage: 78.5714

Iteration: 15 Fitness: 439.5366 Band coverage: 80.9524

Iteration: 16 Fitness: 439.6945 Band coverage: 80.9524

Iteration: 17 Fitness: 439.6945 Band coverage: 80.9524

Iteration: 18 Fitness: 451.392 Band coverage: 78.5714

Iteration: 19 Fitness: 451.392 Band coverage: 78.5714

Iteration: 20 Fitness: 453.3367 Band coverage: 78.5714

Iteration: 21 Fitness: 453.3367 Band coverage: 78.5714

Iteration: 22 Fitness: 462.892 Band coverage: 80.9524

Iteration: 23 Fitness: 466.4903 Band coverage: 83.3333

Iteration: 24 Fitness: 466.4903 Band coverage: 83.3333

Iteration: 25 Fitness: 466.4903 Band coverage: 83.3333

Iteration: 26 Fitness: 531.5431 Band coverage: 88.0952

Iteration: 27 Fitness: 531.5431 Band coverage: 88.0952

Iteration: 28 Fitness: 531.5431 Band coverage: 88.0952

Iteration: 29 Fitness: 548.0211 Band coverage: 92.8571

Iteration: 30 Fitness: 548.0211 Band coverage: 92.8571

Iteration: 31 Fitness: 548.0211 Band coverage: 92.8571

Iteration: 32 Fitness: 556.7325 Band coverage: 90.4762

Iteration: 33 Fitness: 556.7325 Band coverage: 90.4762

Iteration: 34 Fitness: 567.1168 Band coverage: 95.2381

Iteration: 35 Fitness: 590.3868 Band coverage: 95.2381

Iteration: 36 Fitness: 597.7642 Band coverage: 97.619

Iteration: 37 Fitness: 597.7642 Band coverage: 97.619

Iteration: 38 Fitness: 597.7642 Band coverage: 97.619

Iteration: 39 Fitness: 597.7642 Band coverage: 97.619

Iteration: 40 Fitness: 597.7642 Band coverage: 97.619

Iteration: 41 Fitness: 597.7642 Band coverage: 97.619

Iteration: 42 Fitness: 597.7642 Band coverage: 97.619

Iteration: 43 Fitness: 597.7642 Band coverage: 97.619

Iteration: 44 Fitness: 597.7642 Band coverage: 97.619

Iteration: 45 Fitness: 601.1432 Band coverage: 97.619

Iteration: 46 Fitness: 601.1432 Band coverage: 97.619

Iteration: 47 Fitness: 601.1432 Band coverage: 97.619

Iteration: 48 Fitness: 601.1432 Band coverage: 97.619

Iteration: 49 Fitness: 601.1432 Band coverage: 97.619

Iteration: 50 Fitness: 603.3621 Band coverage: 97.619

APPENDIX C

LOG FILE OF PORT LOCATION BASED GA APPLIED TO TC-2

The progress of port location based decap placement GA optimizer applied to TC-2 is shown below.

Iteration: 1 Fitness: 356.6962 Band coverage: 61.25

Iteration: 2 Fitness: 408.3454 Band coverage: 62.5

Iteration: 3 Fitness: 461.1993 Band coverage: 66.25

Iteration: 4 Fitness: 722.7951 Band coverage: 76.25

Iteration: 5 Fitness: 722.7951 Band coverage: 76.25

Iteration: 6 Fitness: 813.7635 Band coverage: 75

Iteration: 7 Fitness: 813.7635 Band coverage: 75

Iteration: 8 Fitness: 1257.6567 Band coverage: 90

Iteration: 9 Fitness: 1259.4303 Band coverage: 90

Iteration: 10 Fitness: 1282.1464 Band coverage: 90

Iteration: 11 Fitness: 1315.5587 Band coverage: 92.5

Iteration: 12 Fitness: 1377.112 Band coverage: 93.75

Iteration: 13 Fitness: 1437.5835 Band coverage: 95

Iteration: 14 Fitness: 1510.5574 Band coverage: 93.75

Iteration: 15 Fitness: 1692.8358 Band coverage: 98.75

Iteration: 16 Fitness: 1692.8358 Band coverage: 98.75

Iteration: 17 Fitness: 1692.8358 Band coverage: 98.75

Iteration: 18 Fitness: 1692.8358 Band coverage: 98.75

Iteration: 19 Fitness: 1692.8358 Band coverage: 98.75

Iteration: 20 Fitness: 1722.4646 Band coverage: 98.75

Iteration: 21 Fitness: 1722.4646 Band coverage: 98.75

Iteration: 22 Fitness: 1722.4646 Band coverage: 98.75

Iteration: 23 Fitness: 1727.5139 Band coverage: 98.75

Iteration: 24 Fitness: 1727.5139 Band coverage: 98.75

Iteration: 25 Fitness: 1753.9691 Band coverage: 98.75

Iteration: 26 Fitness: 1857.3654 Band coverage: 98.75

Iteration: 27 Fitness: 1857.3654 Band coverage: 98.75

Iteration: 28 Fitness: 1857.3654 Band coverage: 98.75

Iteration: 29 Fitness: 1857.3654 Band coverage: 98.75

Iteration: 30 Fitness: 1857.3654 Band coverage: 98.75

Iteration: 31 Fitness: 1857.3654 Band coverage: 98.75

Iteration: 32 Fitness: 1857.3654 Band coverage: 98.75

Iteration: 33 Fitness: 1877.7116 Band coverage: 98.75

Iteration: 34 Fitness: 1890.4317 Band coverage: 98.75

Iteration: 35 Fitness: 1890.4317 Band coverage: 98.75

Iteration: 36 Fitness: 1890.4317 Band coverage: 98.75

Iteration: 37 Fitness: 1890.4317 Band coverage: 98.75

Iteration: 38 Fitness: 1890.4317 Band coverage: 98.75

Iteration: 39 Fitness: 1890.4317 Band coverage: 98.75

Iteration: 40 Fitness: 2063.0679 Band coverage: 100

APPENDIX D

LOG FILE OF RANDOM INITIALIZATION BASED GA APPLIED TO TC-2

The progress of GA optimizer for decap placement with random initialization applied to TC-2 is shown below.

Iteration: 1 Fitness: -721.537 Band coverage: 41.25

Iteration: 2 Fitness: -458.7853 Band coverage: 48.75

Iteration: 3 Fitness: -128.5599 Band coverage: 60

Iteration: 4 Fitness: -119.6639 Band coverage: 60

Iteration: 5 Fitness: -99.1964 Band coverage: 58.75

Iteration: 6 Fitness: -44.3783 Band coverage: 58.75

Iteration: 7 Fitness: -10.6573 Band coverage: 61.25

Iteration: 8 Fitness: 170.2927 Band coverage: 61.25

Iteration: 9 Fitness: 170.2927 Band coverage: 61.25

Iteration: 10 Fitness: 170.2927 Band coverage: 61.25

Iteration: 11 Fitness: 170.2927 Band coverage: 61.25

Iteration: 12 Fitness: 211.1107 Band coverage: 63.75

Iteration: 13 Fitness: 222.0289 Band coverage: 65

Iteration: 14 Fitness: 552.9997 Band coverage: 70

Iteration: 15 Fitness: 616.5346 Band coverage: 73.75

Iteration: 16 Fitness: 633.3177 Band coverage: 73.75

Iteration: 17 Fitness: 633.3177 Band coverage: 73.75

Iteration: 18 Fitness: 639.6786 Band coverage: 72.5

Iteration: 19 Fitness: 659.779 Band coverage: 75

Iteration: 20 Fitness: 702.9295 Band coverage: 76.25

Iteration: 21 Fitness: 702.9295 Band coverage: 76.25

Iteration: 22 Fitness: 734.9192 Band coverage: 78.75

Iteration: 23 Fitness: 734.9192 Band coverage: 78.75

Iteration: 24 Fitness: 743.0367 Band coverage: 77.5

Iteration: 25 Fitness: 801.4603 Band coverage: 78.75

Iteration: 26 Fitness: 848.0245 Band coverage: 78.75

Iteration: 27 Fitness: 885.1815 Band coverage: 80

Iteration: 28 Fitness: 885.1815 Band coverage: 80

Iteration: 29 Fitness: 897.105 Band coverage: 77.5

Iteration: 30 Fitness: 897.105 Band coverage: 77.5

Iteration: 31 Fitness: 897.8771 Band coverage: 77.5

Iteration: 32 Fitness: 915.9918 Band coverage: 77.5

Iteration: 33 Fitness: 918.8691 Band coverage: 76.25

Iteration: 34 Fitness: 933.309 Band coverage: 81.25

Iteration: 35 Fitness: 933.309 Band coverage: 81.25

Iteration: 36 Fitness: 938.9384 Band coverage: 80

Iteration: 37 Fitness: 938.9384 Band coverage: 80

Iteration: 38 Fitness: 957.8449 Band coverage: 80

Iteration: 39 Fitness: 957.8449 Band coverage: 80

Iteration: 40 Fitness: 957.8449 Band coverage: 80

Iteration: 41 Fitness: 957.8449 Band coverage: 80

Iteration: 42 Fitness: 957.8449 Band coverage: 80

Iteration: 43 Fitness: 957.8449 Band coverage: 80

Iteration: 44 Fitness: 995.4591 Band coverage: 81.25

Iteration: 45 Fitness: 995.4591 Band coverage: 81.25

Iteration: 46 Fitness: 995.4591 Band coverage: 81.25

Iteration: 47 Fitness: 995.4591 Band coverage: 81.25

Iteration: 48 Fitness: 995.4591 Band coverage: 81.25

Iteration: 49 Fitness: 995.4591 Band coverage: 81.25

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