Modeling of Package and Board Power Distribution Networks Using Transmission Matrix and Macro-modeling Methods

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Modeling of Package and Board Power Distribution Networks Using Transmission Matrix and Macro-modeling Methods

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Dedicated to

my wife, Mi-Ja Jo

and

my daughter, Christine Yerin Kim

for their support, encouragement, and love

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CHAPTER 1

Introduction

Future systems require a larger number of integrated circuits (ICs), more input/output (I/O) connections, and faster operating clock frequencies with low cost, high performance, high functionality, and high reliability. In addition, the next generation of electronic products is becoming more mixed signal in nature because of the integration of digital, RF, optical, and micro-electro-mechanical type functions on a single module. As a result, maintaining the signal and power integrity for future systems is becoming one of the most important issues.

A major problem in the power distribution system (PDS) is simultaneous switching noise (SSN) induced by power/ground plane inductance. As a result, an important area in high-speed digital systems is the design of the power/ground planes arising in power distribution networks. As clock speeds increase, and signal rise time and supply voltages decrease, the transient current injected into the power distribution planes builds up energy due to the resonant cavity and causes voltage fluctuations and circuit delays [1]. This leads to unwanted effects on the PDS such as ground bounce, power supply compression, and electromagnetic interference. Therefore, a major challenge in the design of planes, which forms an integral part of the PDS for gigahertz (GHz) packages and boards, is the supply of clean power to switching circuits. To predict and suppress this noise, there are clear needs not only for understanding the behavior of the PDS and its contribution to SSN but also for accurate and efficient noise prediction methods.

1.1 Power Distribution System (PDS)

Complementary metal oxide semiconductor (CMOS) microprocessors and application specific integrated circuits (ASICs) in a modern digital system consist of a large number of internal circuits and external circuits (I/O drivers). A power distribution network for the typical high-speed digital system is shown in Fig. 1.1. The power distribution network is used to deliver power to core logic and I/O circuits in the modern system. The power distribution network supplies drivers (switching circuits) that generate signals and receivers that receive the signals, with voltage and current to function. With advances in silicon technology, power supply voltage has reduced according to the scaling rules while the amount of power required has increased with every computer generation. As a result, the current delivery requirement for the power distribution network has gone up greatly and the tolerance for the power supply noise has gone down. It has been recognized that the power supply noise induced by large numbers of simultaneously switching circuits in the power distribution network can limit their performance [2]-[4]. The power supply noise, commonly known as delta-I noise, switching noise or ground bounce, appears as undesired voltage fluctuations in power/ground planes, resulting from the fast transient currents that flow between the planes during the high-to-low or low-to-high transitions of the logic gates in digital switching circuits. To prevent the transient currents from causing excess noise on the power distribution network, the power distribution network should be designed to provide a low-impedance power/ground connection to devices and to minimize their coupling to each other. However, the design of the PDS to meet this goal is becoming more difficult with increasing clock speeds and decreasing supply voltage in modern computer systems.

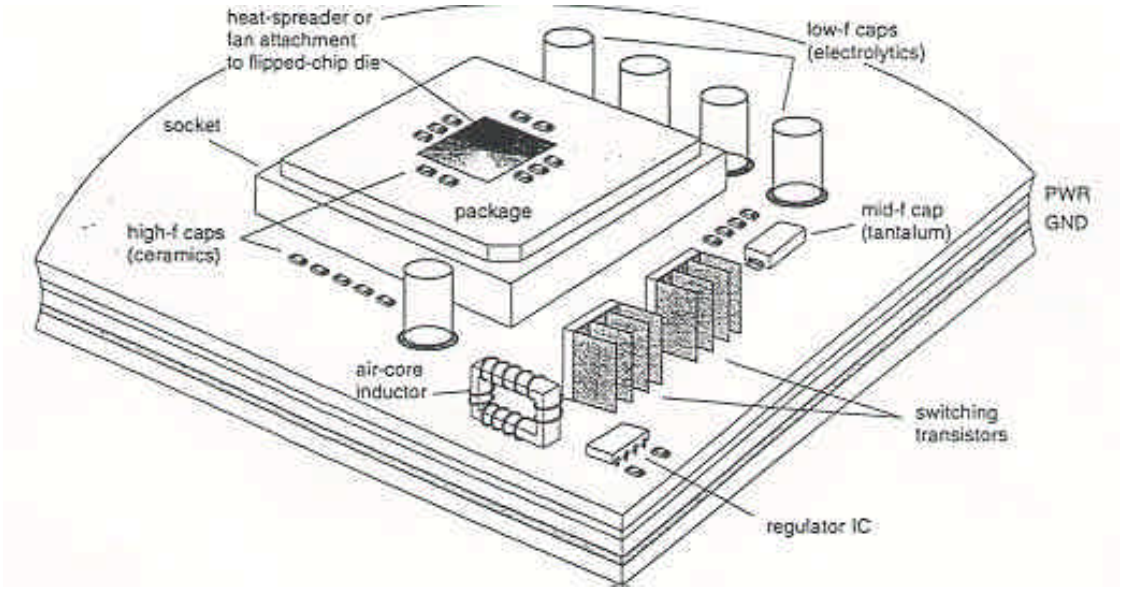


Fig. 1.1. Power distribution network in the power distribution system.

The main issues associated with power distribution are the *IR* voltage drops and the inductive effects [5]. When DC current *I* is supplied to circuit loads, the finite resistance *R* of the package metal layers, which includes vias, interconnects and power/ground planes, causes a voltage drop given by Ohm's Law $V = I R$. Since the IR voltage drop can vary across the chip, the supply voltage for all the circuits may not be the same. This variation of the DC supply voltage can cause the false transitioning of the circuits for spurious input signals. During the high-to-low or low-to-high transitions of the circuits, the inductive effect occurs more seriously due to a time-varying current. Since metal layers are inherently inductive, the time varying current causes a voltage fluctuation to the supply voltage. Hence, the supply voltage oscillates around the DC level with time. This inductive effect leads to the following effects:

1. The inductance of the power distribution network causes the circuits to slow down by introducing excessive time delays to the supply voltage of the circuits.

2. Noise glitches on the power supply may cause false switching of the circuits on both the sending and receiving chips.

Both these effects should be minimized for increasing the reliability of systems.

Fig. 1.2 shows the electrical equivalent circuit of the PDS, which can be mapped from the mechanical structure of the system in Fig. 1.1 [1]. For the good design of the power distribution network, the characteristic impedance of the power/ground planes should be designed to be as low as possible over the entire bandwidth of the signal [6]. As a result, the frequency-dependent driving point impedance (Z) of the PDS at the circuit terminals shown in Fig. 1.2 should be kept very small compared to the impedance of the circuit load of each chip to avoid large voltage drops in the PDS.

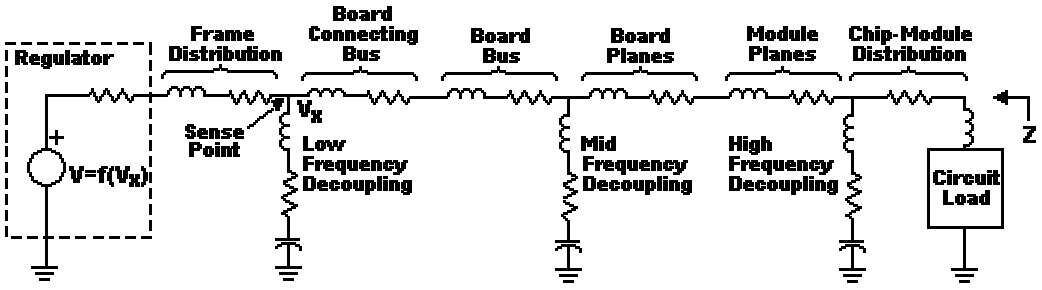


Fig. 1.2. Equivalent circuit diagram for power distribution system [1].

A desirable output impedance plot for the PDS looking back from the circuit loads is shown in Fig. 1.3 [1]. At low frequencies, a power distribution network acts as a capacitor. In the mid-frequency range, a good network should behave as a transmission line with a very low characteristic impedance, with the latter being orders of magnitude lower than the impedance of the circuit load. As the frequency increases beyond the mid-range, the network has an inductive behavior with multiple resonant frequencies.

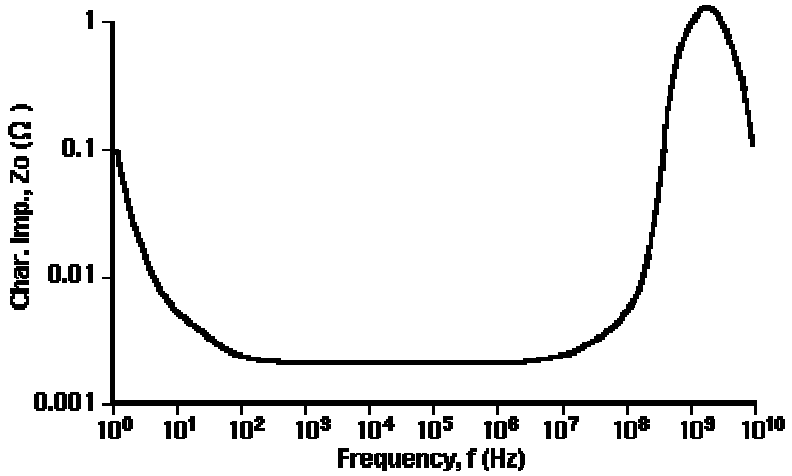


Fig. 1.3. Output impedance for the typical power distribution system [1].

1.2 Simultaneous Switching Noise (SSN)

While recent advances in CMOS technology have resulted in faster device switching speed and higher package density, simultaneous switching noise (SSN) induced by a large number of internal and external switching circuits has become a critical issue. As all these switching circuits cause hundreds or even thousands of millivolts (mV) of SSN between the power supply voltages, a signal error may occur [1]. SSN occurs both on-chip and off-chip due to the internal inductance ($L_{eff/i}$) for an on-chip current loop and the external inductance ($L_{eff/e}$) for an off-chip current loop. Because of the difference in the current loops, there are two different values of the effective inductance (L_{eff}) for these circuits. Generally, $L_{eff/i}$ is smaller than $L_{eff/e}$ because the current loop for the internal circuit is made up of a large number of tightly coupled power and ground vias and planes, whereas the external current path consists of longer and more loosely coupled signals and power/ground paths. The total switching noise is, therefore, the sum of

internal switching noise (SN_{INT}) and external SSN (SN_{EXT}), which are often called core noise and I/O noise, respectively, as shown below [1]:

$$SN_{TOT} = SN_{INT} + SN_{EXT} = L_{eff/i}(N\frac{di}{dt})_{INT} + L_{eff/e}(N\frac{di}{dt})_{EXT} \qquad (1.1)$$

where

di/dt	current slew rate of a single driver;
$L_{eff/i}, L_{eff/e}$	effective inductance;
N	number of simultaneously switching drivers.

It is important to note that the effective inductance can be defined only for a loop of current. As shown in Eq. (1.1), the switching noise is directly proportional to the current slew rate and the effective inductance. As a result, controlling the total allowed system noise requires controlling either the driver's slew rate or the effective inductance. However, the control of the driver's slew rate requiring driver slowdown is not adequate because it adds delay to the driver output and can ultimately increase the machine cycle time. Hence, reducing the effective inductance is the only solution.

With improved circuit speed, the driver's slew rate is increasing within any system. Additionally, the voltage and signal levels are decreasing, as mentioned earlier. As a result, the power supply noise budget must decrease for future systems. To mitigate the effects of power supply noise, not only methods to reduce the effective inductances, but also the noise budget to determine the maximum permitted inductance associated with a power distribution network are necessary for the design of a reliable system. The

maximum effective inductance for each allowed system noise in the power distribution network can be estimated as follows [5]:

$$L_{eff/i} \le \frac{DV(Dt)^2}{NCV_{dd}}$$
$$L_{eff/e} \le \frac{DVZ_0}{N\frac{V_{dd}}{Dt}} \qquad (1.2)$$

where

DV maximum voltage fluctuation;

Dt transition time;

N number of simultaneously switching drivers;

C load capacitor;

V_{dd} power supply voltage;

Z_0 characteristic impedance of the transmission line.

Based on the first-order approximation and a linear model, Eq. (1.2) provides a simple relationship for computing the maximum effective inductance that can be tolerated on the power supply. Linearity of noise is not preserved beyond a certain number of switching drivers since noise saturates due to negative feedback [7], [8]. Actually, when noise becomes excessive, it slows down the drivers by reducing the current output of the drivers during the time interval Dt.

1.3 Decoupling Capacitors

In the PDS, suppression of SSN is critical. One way to reduce the SSN is to use decoupling capacitors on the card, board, module, and/or chip. Decoupling capacitors are used to compensate the natural inductance of the power distribution network, yielding a small impedance for as large a frequency range as possible [1], [9], [10].

Charge supplied by a current from the power supply is required to energize a load capacitor. When the current flows through the package inductance, it produces a voltage drop across it. Decoupling capacitors provide switching drivers with extra current required to charge the load capacitor instead of the power supply. As a result, the power supply noise is reduced since the inductive effect in the loop current path is decreased by the decoupling capacitors.

For a modern computer system operating at high frequency, switching circuits cause waves to propagate between power and ground planes in the package and board. These waves reflect from the edges of the package and board and cause resonances over the frequency range. Therefore, different decoupling capacitors should be used over the wide frequency range, depending on the package structure. Based on the resonant frequency, the decoupling capacitors can be categorized into low-frequency, mid-frequency, and high-frequency capacitors, and incorporated at appropriate places throughout the system, as shown in Fig. 2, for filtering the frequency components of current changes caused by circuit switching. Typically, low-frequency and mid-frequency decoupling capacitors are mounted on the package and board, and high-frequency decoupling capacitors for $f > 1\text{GHz}$ are buried in the chip as trench capacitors.

Since decoupling capacitors are not ideal, they have a self-resonant frequency. This is due to the parasitic inductance and resistance caused by the leads and mounting pads of the capacitor, which severely limit the performance of the capacitor. As a result, the decoupling capacitor can be represented as a series circuit, followed by the impedance equation:

$$Z_{cap} = R_{ESR} + jwL_{ESL} + \frac{1}{jwC} \tag{1.3}$$

where

R_{ESR} equivalent series resistance (ESR);

L_{ESL} equivalent series inductance (ESL);

C capacitance.

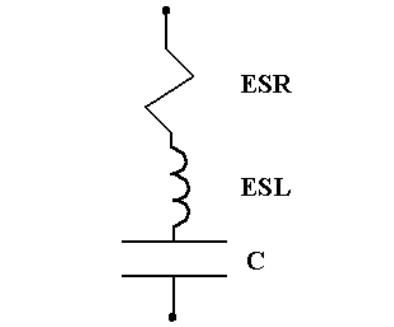
The expression for the resonant frequency of Eq. (1.3) is

$$f_{SR} = \frac{1}{2p\sqrt{L_{ESL}C}} \tag{1.4}$$

at which the reactive impedances are cancelled and the impedance of the decoupling capacitor has a magnitude of R_{ESR}.

Fig. 1.4 shows the equivalent series impedance for seven kinds of decoupling capacitors that were incorporated into CPU core power supply planes for Sun Microsystem workstations. As shown in Fig. 1.4, for filtering the low-to-mid frequency

noise components, several kinds of bulk (low-frequency) and bypass (mid-frequency) capacitors were used over the wide frequency range.



ESR (ohm)	ESC (F)	ESL (H)	Res. Freq (Hz)
0.0391	1.00E-07	4.70E-10	2.3442E+07
0.1000	1.00E-08	4.70E-10	7.4131E+07
0.0158	1.00E-06	7.47E-10	5.8884E+06
0.0158	1.00E-06	4.70E-10	7.4131E+06
0.0060	1.00E-05	1.10E-09	1.5136E+06
0.0060	1.00E-05	7.80E-10	1.8197E+06
0.0078	1.50E-03	7.81E-09	4.6774E+04

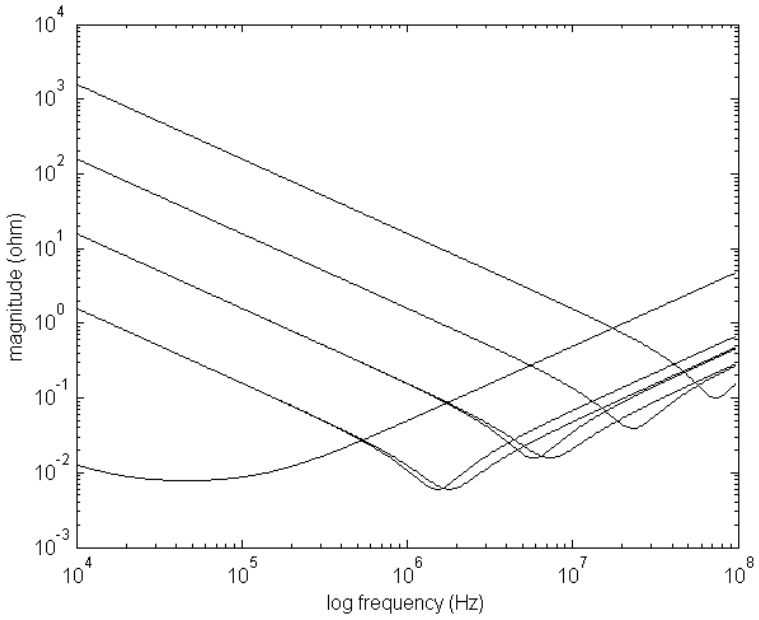


Fig. 1.4. Impedance of decoupling capacitors.

1.4 Characteristics of Power Distribution Planes

While the bandwidth of signal transients moves to the gigahertz range, a required target impedance in power distribution networks may reach the sub-milliohm range [11]. If not designed properly, the power/ground planes in the power distribution network, as shown in Fig. 1.5, exhibit resonances in the frequency domain [12], and the impedances at specific resonant frequencies may be higher than the target impedance. To suppress the resonances, in conventional design, many decoupling capacitors are attached to the power distribution network, as mentioned earlier. In addition, using different materials and geometries of power/ground planes provides good suppression of plane resonances in the

power distribution network. For instance, an increase in the loss of a dielectric material and its dielectric constant, and a decrease in dielectric thickness help to reduce the impedance and resonances [13], [14]. To examine the characteristics of power/ground planes in the PDS, this section describes the effect of the dielectric loss, the dielectric constant, and the dielectric thickness on the power distribution impedance.

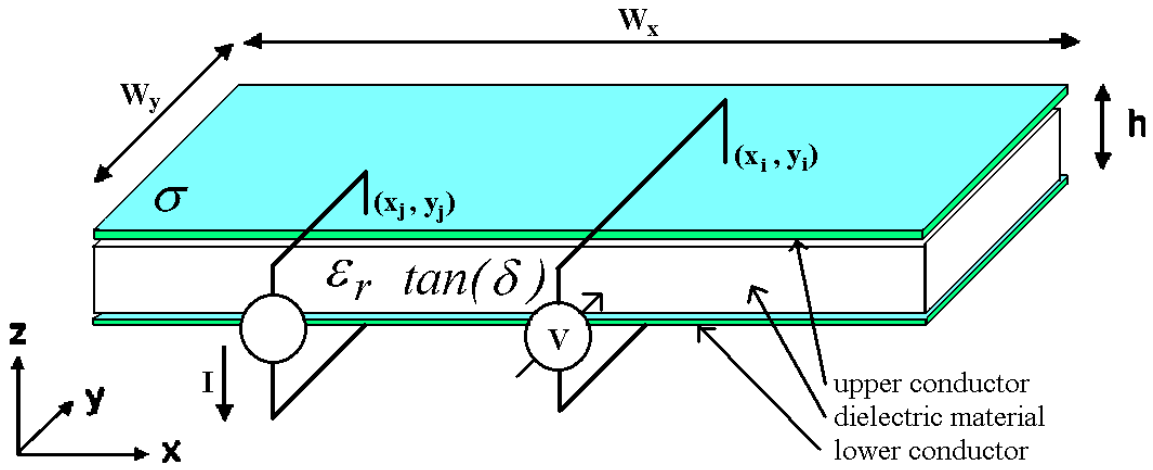


Fig. 1.5. Power/ground planes in the power distribution network.

1.4.1 Effect of Dielectric Loss

For low loss signal transmission, PCB materials with low dielectric loss have been used; as a result, plane resonances are not suppressed sufficiently [13]. However, if used only between power/ground planes, high dielectric loss is preferred. Fig. 1.6 shows the comparison of impedances as varying loss tangent of dielectric ($tan(d)$). As the loss tangent of the dielectric increases, the impedance magnitude at resonant frequencies decreases significantly, but the cavity resonances occur at the same frequencies since the plane inductance and capacitance that determine the resonant frequencies are not

changed. Over some value of *tan(d)*, which is 0.3 in Fig. 1.6, the plane resonances are almost suppressed.

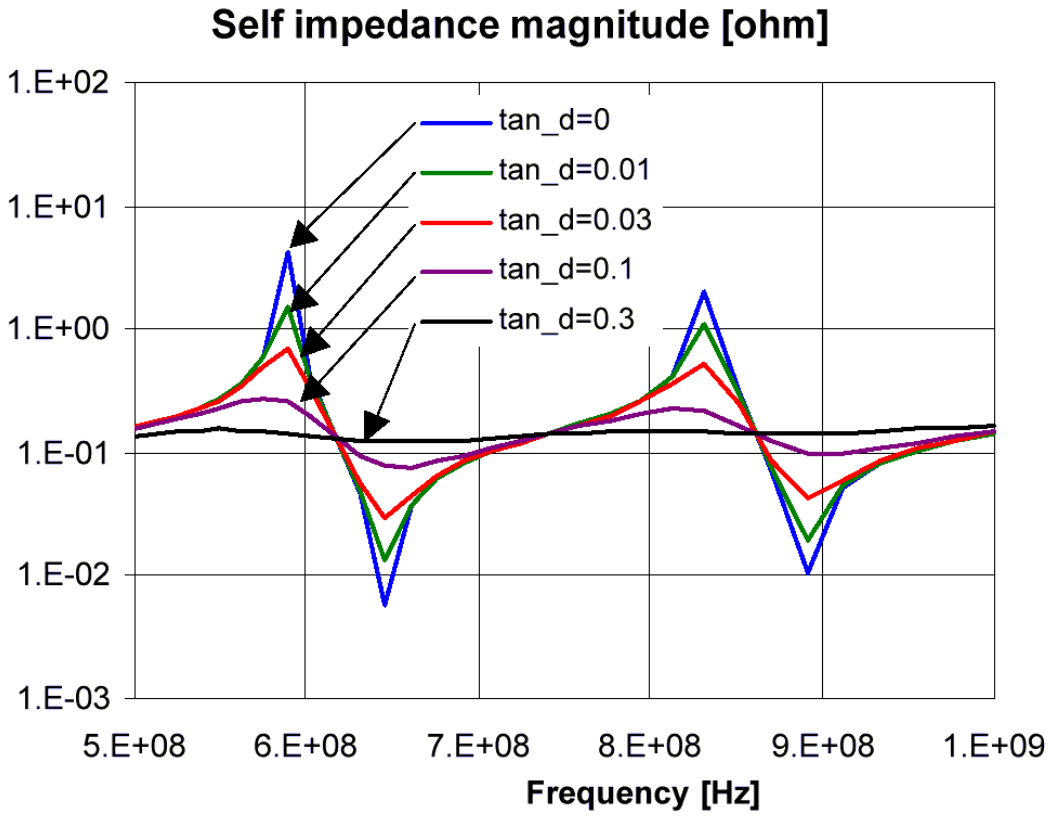


Fig. 1.6. Effect of dielectric loss on impedance magnitude [13].

1.4.2 Effect of Dielectric Constant

Fig. 1.7 shows the effect of dielectric constant on plane impedances and resonances for e_r = 4, 8, 16, 32, and 64 [14]. As the increase in the dielectric constant increases the plane capacitance, accordingly the low-frequency impedances are reduced and all of the null and peak resonant frequencies shift to the lower frequencies. This is because the velocity of the plane waves that propagate between power and ground planes varies

inversely with $\sqrt{e_r}$. The increase in the delay of the plane waves from one side to the other side results in a downshift of the resonant frequencies proportional to $\sqrt{e_r}$. However, the plane impedances in the high frequency range are not changed significantly since the plane inductance is still fixed.

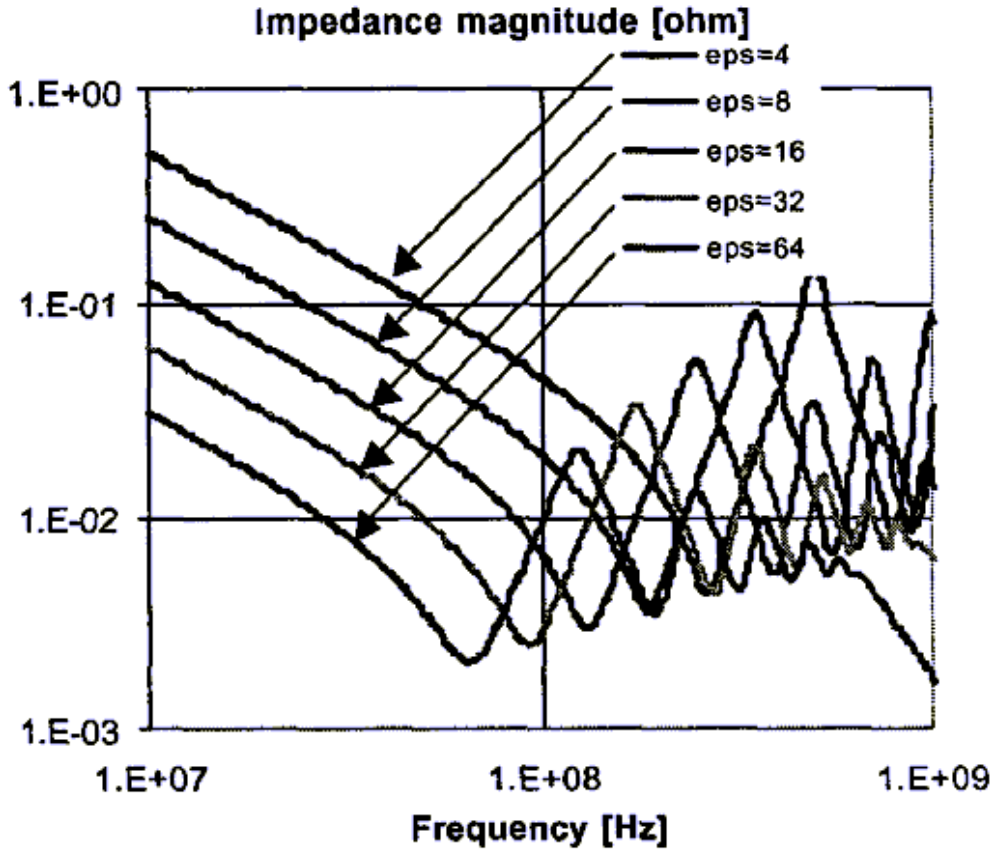


Fig. 1.7. Effect of dielectric constant on impedance magnitude [14].

1.4.3 Effect of Dielectric thickness

Thin dielectrics between power/ground planes offers tremendous advantages for low-impedance power distribution systems both in the low and high frequency range. As the dielectric thickness decreases, the plane capacitance increases, and the plane inductance

decreases. As shown in Fig. 1.8 [13], the thin dielectrics not only reduce the impedances over the frequency range, but also suppress the peak resonant frequencies. However, all of the peak and null resonant frequencies are not changed since the velocity of the plane waves is not a function of dielectric thickness but a function of dielectric constant.

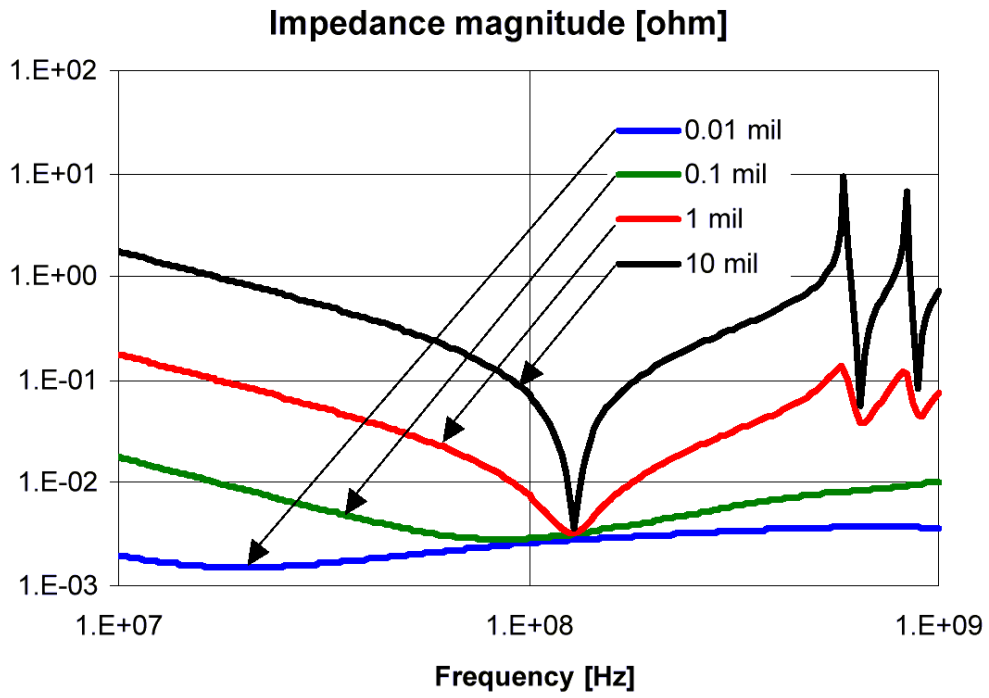


Fig. 1.8. Effect of dielectric thickness on impedance magnitude [13].

Compared with the two factors, described in Sections 1.4.1 and 1.4.2, a decrease in dielectric thickness is the most effective method for designing a low-impedance PDS. Unfortunately, it is not practical to manufacture and handle a dielectric layer that is a few micrometers thick using standard printed wiring board (PWB) technology [13].

1.5 Plane Modeling in Power Distribution Networks

Relying on empirical techniques such as fabrication, testing, and debugging, the hardware can be made to work, but making fast computers work properly can result in a very long turnaround time [1]. In these days of short market cycle time, relying only on empirical techniques is not sufficient for many high-frequency products. Therefore, design, modeling and simulation methods are necessary. The modeling and simulation techniques play an important role in minimizing recovery times and design errors.

To achieve high-frequency performance in high-speed digital multichip modules (MCMs) or single-chip modules (SCM), power/ground planes, shown in Fig. 1.5, are used for power distribution. In the past, the power distribution planes were successfully modeled using lumped elements [15], [16]. However, the accuracy of the lumped models has been limited to rise times much longer than the propagation time across the planes [17]. As the cut-off frequency in the PDS increases, comprehensive electromagnetic (EM) models have to be constructed and analyzed to properly predict the levels of the various types of noise in the PDS. To capture cavity resonances in modern power distribution networks containing thousands of vias and interconnections, accurate predictions of SSN require a more distributed model.

Recently, various numerical methods have been developed for the analysis of power/ground planes using an electromagnetic (EM) model based on Maxwell's equation or a distributed circuit model. Examples include Partial Element Equivalent Circuit (PEEC) [18], [19] using an integral equation formulation, Method of Moments (MoM) [20], Finite Difference Time Domain (FDTD) [21], [22], circuit analysis using a two-dimensional array of transmission lines or distributed RLCG elements [13], [23], and a

direct calculation using an analytical solution [24], [25]. Each method has its own advantages and disadvantages. The first three methods are based on the full wave solution of Maxwell's equations. Since power/ground planes are electrically large, these methods are computationally expensive. While the analytical solution method is a gridless approach where ports and decoupling capacitors can be arbitrarily placed at any location [25], it depends on the propagating modes, and its computation time is dependent on the number of decoupling capacitors, number of vias, and number of modes used for computation. In contrast, the method based on a two-dimensional array of transmission lines is a grid-based approach requiring that decoupling capacitors and vias be placed at fixed grid locations. However, this method can be applied to arbitrary structures and extended to multiple plane layers. In a realistic package/board, which consists of numerous vias, decoupling capacitors, irregular geometries, and multiple plane layers, the number of transmission line segments required may become very large, requiring large memory and CPU time for analysis. Hence, there is a clear need for more efficient and accurate modeling methods for modeling planes in high-performance packages that capture the high frequency behavior.

The objective of this proposed research is to develop an efficient numerical method for electromagnetic (EM) modeling of the power distribution system (PDS). This proposed research presents a new technique for analyzing multi-layered arbitrary shaped power distribution networks both in the frequency and time domain.

1.6 Proposed Research and Dissertation Outline

The goal of this proposed research is the development of the transmission matrix and macro-modeling methods and their application to digital systems for computing core and I/O switching noise in realistic power distribution networks. Based on the issues for analyzing switching noise in high-performance systems, the following research is proposed:

1. **Development of the transmission matrix method for a pair of rectangular and irregular shaped power/ground planes using a two dimensional array of distributed lumped RLCG circuits:** For the accurate prediction of simultaneous switching noise (SSN) and for noise reduction, a power/ground plane pair can be electrically modeled as a two dimensional array of distributed lumped RLCG circuits. Based on both T and Π unit cell models, the transmission matrix method has been developed to compute the impedance matrix at specific ports on the network.
2. **Incorporation of decoupling capacitors in the transmission matrix method:** To nullify the plane resonances and suppress SSN, numerous decoupling capacitors with low impedance are often incorporated into the power distribution network. The transmission matrix method has been modified to include decoupling capacitors without increasing the CPU run time.
3. **Verification of the transmission matrix method:** The transmission matrix method has been compared with SPICE, an analytical solution, and measurements. For a rectangular geometry, the transmission matrix method showed good

agreement with an analytical solution that required a large number of propagating modes (m, n =100). Additionally, the transmission matrix method perfectly matched all resonant frequencies and magnitudes with SPICE for both rectangular and L-shaped geometries.

4. **Application of the transmission matrix method to realistic geometries:** The transmission matrix method has been applied to realistic power distribution networks, containing irregular shaped geometries, as described below:
    a. L-shaped geometry: This structure is being used as the CPU core power supply planes in Sun Microsystems' workstations. All of the decoupling capacitors attached to the L-shaped plane and the plane impedances were measured using a network analyzer. The measured and simulated results were analyzed and compared.
    b. Split plane: A split power plane structure with decoupling capacitors consisting of two pairs of rectangular planes separated by a dielectric was analyzed. The bottom plane was continuous while the top plane was split into two parts separated by a 5 mm gap, but connected through a ferrite core. The aim of this analysis was to evaluate the noise transferred through the ferrite core used for AC blocking. The results from the transmission matrix method had good agreement when compared to the cavity resonator method.
    c. Motorola Bravo Plus pager: In consumer mixed signal applications, the power distribution structure is of arbitrary shape. The transmission matrix method was applied to the power distribution structure in a Motorola

Bravo Plus pager, which contained an arbitrary shaped plane pair with large cutouts and numerous via openings.

5. **Modeling of Multi-layered Planes:** The transmission matrix method was extended to a third dimension for modeling multi-layered power distribution planes. To reduce the impedance over a wide frequency range, multi-layered power distribution networks are often used in modern computer applications. Multi-layered power distribution planes can be represented as a cascade of a power/ground plane pair connected in parallel through vertical vias. The transmission matrix method has been modified to analyze multi-layered power distribution networks. While three matrix inversions were required in earlier work [26], [27], the transmission matrix method has been simplified to require only one matrix inversion for modeling multi-layered networks.
6. **Incorporation of vias:** Vias are a common type of discontinuity in multi-layered power distribution networks, where thousands of via connections are used to reduce the via inductances and for thermal dissipation. Their effects, which have generally been neglected in the past, are not totally negligible as the cut-off frequency on the PDS increases. Using FastHenry [54], partial self and mutual inductances for vias were extracted and included in the transmission matrix method.
7. **Analysis of multi-layered rectangular shaped power distribution planes with vias:** For analyzing the effect of multi-layered plane pairs in parallel, several issues such as the number of plane pairs, the number of vias, proximity between vias and ports, coupling between vias and plane capacitances, etc. should be

considered. Multi-layered power distribution networks have been modeled with vias represented as short circuits, with vias represented as partial self inductances, and with vias coupled to each other. With the three modeled via connections, multi-layered power distribution networks made up of 5, 10, and 15 plane pairs have been analyzed and compared using the transmission matrix method to demonstrate the effects of vias and multi-layered power/ground planes.

8. **Application of the transmission matrix method to multi-layered irregular shaped planes:** The transmission matrix method was applied to a multi-layered irregular shaped plane structure where each pair of power/ground planes had different shape and dielectric thickness. The aim of this analysis was to show that the transmission matrix method could be used for analyzing large networks.
9. **Transient response in the time domain:** For the analysis of a computer system, time domain analysis is finally required to compute the time varying voltage drop or fluctuation at specific points in the power distribution network. The transmission matrix method has been developed to compute the frequency dependent parameters (S, Y, or Z matrices) in the frequency domain. Using spline interpolation, inverse discrete Fourier transform (IDFT), and convolution, these parameters have been converted to the time domain response for computing the transient core switching noise in the PDS.
10. **Model to hardware correlation for an arbitrary shaped power distribution network:** The power distribution network, consisting of three different DC islands of core power supply planes, is part of a high speed commercial image processing system for high resolution printing from Kodak. The main core plane was

simulated and correlated with hardware measurements using a Vector Network Analyzer.

11. **Model to hardware correlation by considering unknown parasitics:** The power distribution network supplied by IBM includes unknown parasitics generated by the leads and pads of decoupling capacitors. Based on the measurements, the unknown parasitics were extracted and included in the transmission matrix method for modeling.
12. **Development of Y and Z parameter based equivalent circuits using macro-models for power distribution networks:** A macro-modeling method for generating rational functions was developed for transient simulation using both Y and Z parameters. The Y-parameter based macro-modeling method, which uses weighted least squares approximation and solution of an eigenvalue problem, is suitable for implementing an equivalent circuit; however, it is prohibitively expensive for an electrically large system consisting of multiple resonances and requiring a large number of ports. On the contrary, the Z-parameter based macro-modeling method, which uses direct computation, is efficient for such large systems. Both the methods have been applied to power distribution networks to reduce the model size by eliminating the internal nodes.
13. **Computation of I/O noise:** Methods have been developed for analyzing core switching noise in a computer system using IDFT [36]. However, for I/O noise computation, the interconnects in the presence of power/ground planes have to be considered. The charging and discharging of the interconnects behaving as transmission lines and the path traversed by the return currents results in noise on

the PDS. The interconnects have been incorporated into the power distribution planes with non-linear drivers for analyzing I/O noise. As an example, test vehicles from Sun Microsystems and IBM were analyzed for the computation of I/O noise using the transmission matrix method and the macro-modeling method based on Z parameters.

The remainder of this thesis is organized as follows. Chapter 2 presents the transmission matrix method for a pair of power/ground planes in detail. As an example, the transmission matrix method has been applied to rectangular, L-shaped, split-plane, and arbitrary shaped plane geometries. In Chapter 3, the transmission matrix method has been extended to a third dimension for modeling multi-layered rectangular and irregular shaped power distribution planes. To demonstrate the effects of vias and multi-layered power/ground planes, multi-layered power distribution networks made up of 5, 10, and 15 plane pairs have been analyzed and compared using the transmission matrix method in Chapter 4. Chapter 5 shows model to hardware correlation in the frequency domain for an actual structure used by Eastman Kodak, which has an arbitrary shaped plane geometry with a large number of via holes, and a test vehicle supplied by IBM, which consists of a CMOS ASIC test chip, a HyperBGA package and a printed wiring board (PWB). A Y-parameter based macro-modeling method which generates reduced circuit models using rational functions is discussed in Chapter 6. However, this is limited to systems requiring a small number of ports. To increase the number of ports, in Chapter 7, a Z-parameter based macro-modeling method has been developed. Using the method and the transmission matrix method, two test vehicles made by Sun Microsystems and IBM

were analyzed for the computation of I/O noise. The conclusion and future work are provided in Chapter 8.

CHAPTER 2

Modeling of a Power/Ground Plane Pair

An important area in high-speed digital systems is the design of the power/ground planes arising in power distribution networks. Realistic power distribution networks in the package and board are electrically large structures containing numerous discontinuities and components, as mentioned in the previous chapter. The analysis of the entire power distribution network can demand large memory requirements and a considerable CPU run time on the most powerful computers. In the past, various numerical methods have been developed for the analysis of power distribution networks. Examples include Speed from Sigrity [28], [29], which is based on a finite difference time domain (FDTD) method, Transmission Line method [13], [23], which uses a two dimensional array of transmission lines or distributed RLCG elements in SPICE, and the cavity resonator method simulated in SPICE [30], [31]. Although these methods have their advantages for specific structures, their use is still limited for electrically large structures. The transmission matrix method discussed in this proposed research offers a more efficient technique for analyzing realistic power distribution networks. Using the property that power distribution networks in the package and board can be represented as a cascade of unit cells consisting of distributed and repeated RLCG circuit elements, the multi-input/multi-output transmission matrix method can be used to simulate arbitrarily shaped, electrically large structures efficiently. Since the transmission matrix method is based on a multi-input/multi-output transfer function, the response of the power

distribution network at specific ports can be computed by multiplying the individual square matrices. Once the matrix of the overall network is computed, it can be converted into a scattering matrix (S), an admittance matrix (Y), or an impedance matrix (Z) at specific points on the network. Therefore, while retaining the same size of the matrix for the overall network, the transmission matrix method provides the flexibility for analyzing large networks containing up to 20 power/ground plane pairs with relative ease. The salient features of the method are that it requires small memory and the CPU time scales linearly as the number of power/ground planes are increased.

This chapter describes the physical principle, formulation and implementation of the transmission matrix method for a power/ground plane pair. The transmission matrix method has been applied for analyzing rectangular and irregular shaped power/ground planes. Where applicable, the results have been compared with the analytical solution, SPICE or measurements.

2.1 Power Plane SPICE Models

Power/ground planes can be divided into unit cells with a lumped element model for each cell, as described in [17]. Each cell consists of an equivalent circuit with R, L, C, and G components, as shown in Fig. 2.1 for a rectangular structure. Each unit cell can be represented using either a T or Π model [32], [33] as shown in the figure. The primary difference between these two models is an offset of half a unit cell between each other. Both models, however, lead to similar results, as shown in later sections. The equivalent circuit parameters for a unit cell can be derived from quasi-static models provided the

dielectric separation (*d*) is much less than the metal dimensions (*a*, *b*) [34], which is true for power/ground plane pairs.

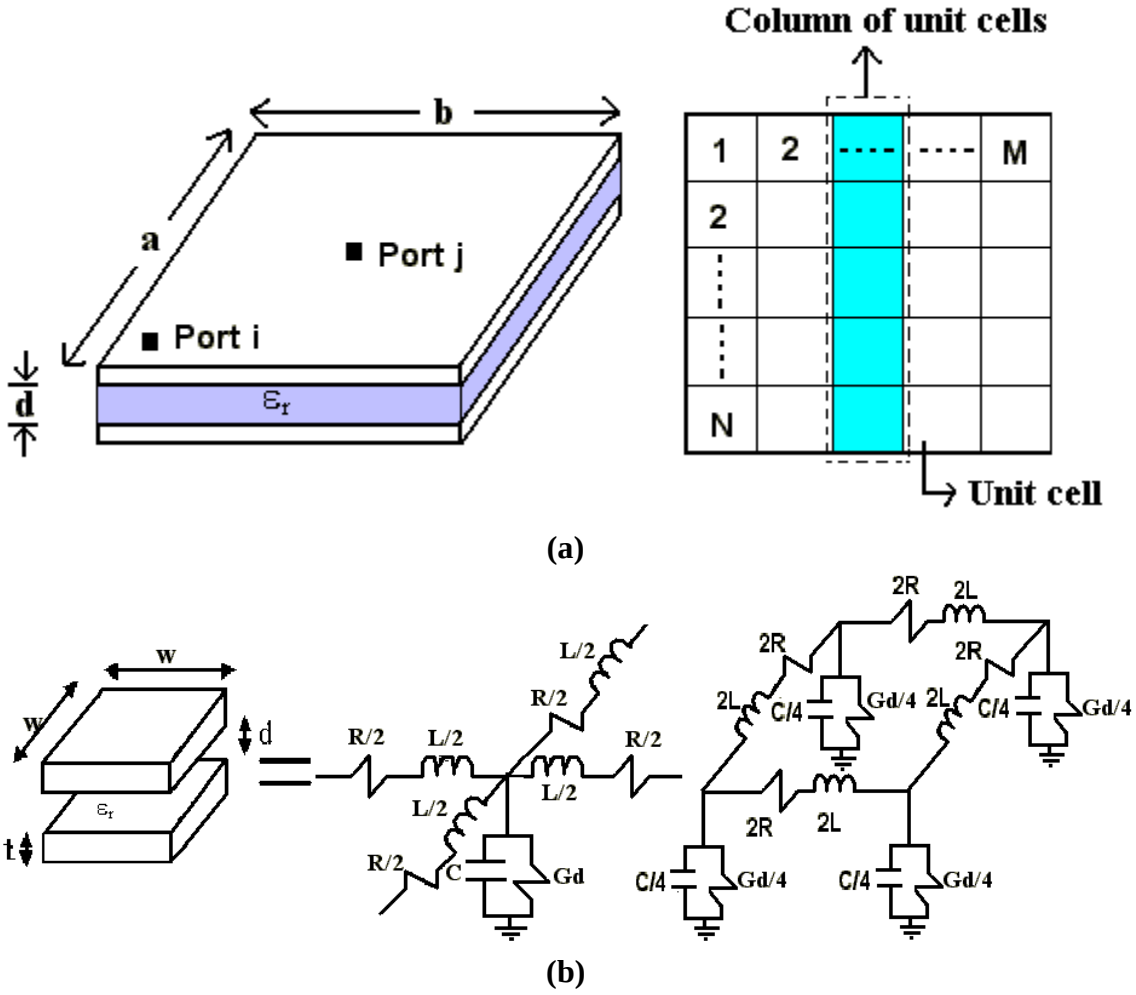


Fig. 2.1. (a) Plane pair structure and (b) unit cell and equivalent circuit (T and Π models).

From the lateral dimension of a unit cell (*w*), separation between planes (*d*), dielectric constant (e), loss tangent of dielectric ($tan(d)$), metal thickness (*t*), and metal conductivity (σ_c), the equivalent circuit parameters of a unit cell can be computed as:

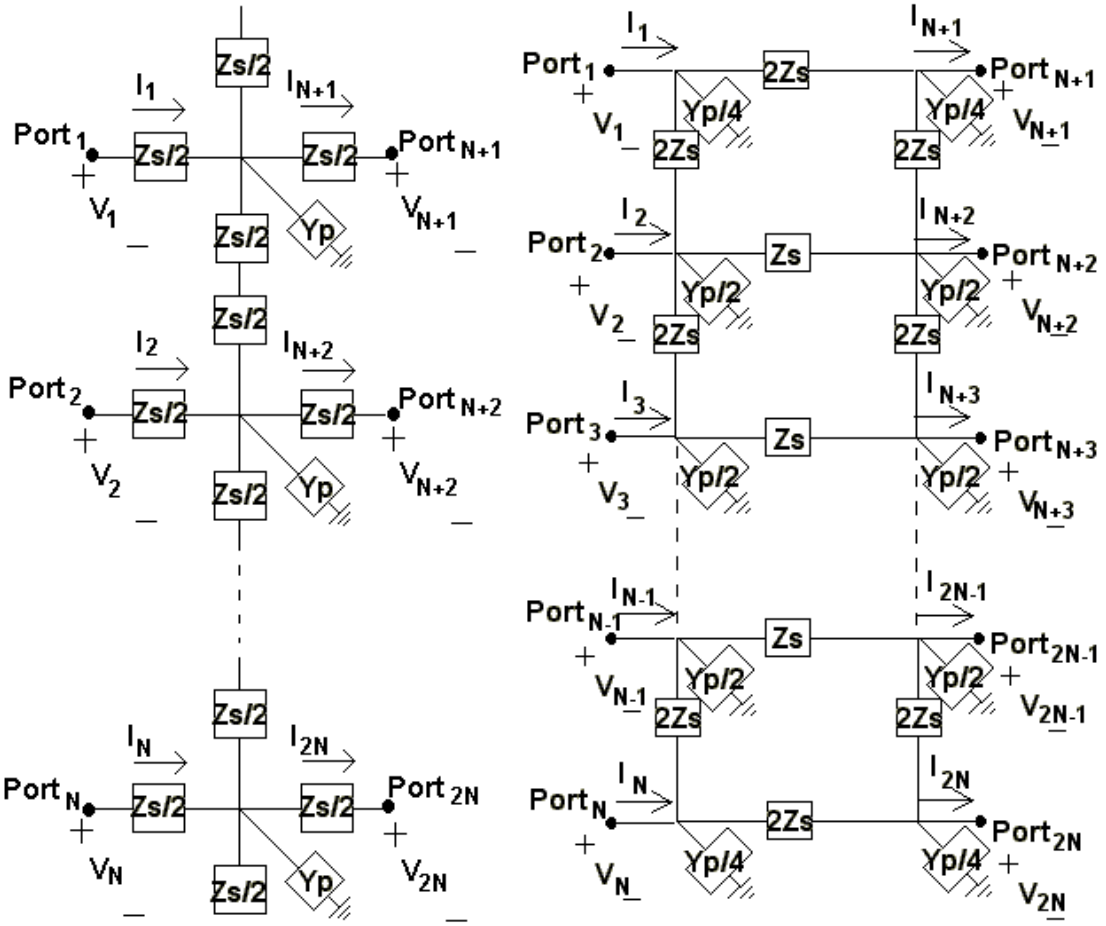
$$C = e_o e_r \frac{w^2}{d} \quad L = m_o d \quad R_{dc} = \frac{2}{s_c t} \quad R_{ac} = 2\sqrt{\frac{pfm_o}{s_c}}(1+j) \quad G_d = wC\tan(d). \quad (2.1)$$

In the above equation, e_o is the permittivity of free space, m_o is the permeability of free space, and e_r is the relative permittivity of the dielectric. The parameter R_{dc} is the resistance of both the power and ground planes for a steady dc current, where the planes are assumed to be of uniform cross-section. The ac resistance R_{ac} accounts for the skin effect on both conductors. The shunt conductance G_d represents the dielectric loss in the material between the planes.

Using the unit cell, a distributed network of RLCG elements can be generated for rectangular planes, as shown in Fig. 2.1. In the figure, a total of $N \times M$ unit cells have been used to represent the rectangular plane. Since this is a circuit model, it can be simulated in SPICE by generating the Modified Nodal Analysis (MNA) equations. For the T model, it is important to note that the edges of the planes are magnetic walls, which require the nodes at the edges to be terminated with resistors having a large value in SPICE ($R_{eg} = 10^{17}\,W$), so that the resistors can mimic an open circuit. To obtain good accuracy, a unit cell size that is 10 times less than the wavelength at the highest frequency of interest was used. For the rectangular structure, the T model was used in SPICE for simulation.

2.2 Transmission Matrix Method

As shown in Fig. 2.1, using a distributed network of RLCG elements, the rectangular plane can be divided into $N \times M$ unit cells. Consider a column of unit cells ($N \times 1$ unit cells), which is shown as a dashed line in Fig. 2.1. The $N \times 1$ unit cells can be represented as a $2N \times 2N$ matrix formed by N input ports and N output ports. This is shown in Fig. 2.2 for the T and Π equivalent circuits for the unit cells.



$$Z_S = R_{dc} + R_{ac} + j\omega L$$
$$Y_P = j\omega C + \omega C \tan\delta$$

Fig. 2.2. Equivalent circuit for a column of unit cells (T and Π models).

In Fig. 2.2, the input and output ports are indexed as 1 to N and N+1 to 2N, respectively. The transmission matrix for the 2N-port network can be derived in terms of the node voltages and port currents as

$$\begin{bmatrix} V_1 \\ \vdots \\ V_N \\ \cdots\cdots \\ I_1 \\ \vdots \\ I_N \end{bmatrix} = \left[\begin{array}{ccc:c:ccc} T_{1,1} & \cdots & T_{1,N} & & T_{1,N+1} & \cdots & T_{1,2N} \\ \vdots & & \vdots & & \vdots & & \vdots \\ T_{N,1} & \cdots & T_{N,N} & & T_{N,N+1} & \cdots & T_{N,2N} \\ \cdots\cdots & \cdots\cdots & \cdots\cdots & \cdots\cdots & \cdots\cdots & \cdots\cdots & \cdots\cdots \\ T_{N+1,1} & \cdots & T_{N+1,N} & & T_{N+1,N+1} & \cdots & T_{N+1,2N} \\ \vdots & & \vdots & & \vdots & & \vdots \\ T_{2N,1} & \cdots & T_{2N,N} & & T_{2N,N+1} & \cdots & T_{2N,2N} \end{array}\right] \begin{bmatrix} V_{N+1} \\ \vdots \\ V_{2N} \\ \cdots\cdots \\ I_{N+1} \\ \vdots \\ I_{2N} \end{bmatrix}. \quad (2.2)$$

The above transmission matrix can be rewritten in the simpler form:

$$T = \begin{bmatrix} T_A & T_B \\ T_C & T_D \end{bmatrix} \quad (2.3)$$

where $[T_A]$, $[T_B]$, $[T_C]$, and $[T_D]$ are $N \times N$ matrices. In Eq. (2.4), the [T] matrices for the T and Π equivalent circuit unit cells are of the form:

$$[T]_T = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 & \vdots & Z_s/2 & 0 & \cdots & 0 & 0 \\ 0 & 1 & \cdots & 0 & 0 & \vdots & 0 & \ddots & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots & & \vdots & & Z_s/2 & \vdots & \\ 0 & 0 & \cdots & 1 & 0 & \vdots & 0 & 0 & \cdots & \ddots & 0 \\ 0 & 0 & \cdots & 0 & 1 & \vdots & 0 & 0 & \cdots & 0 & Z_s/2 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & 0 & 0 & \vdots & 1 & 0 & \cdots & 0 & 0 \\ 0 & 0 & \cdots & 0 & 0 & \vdots & 0 & 1 & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots & & \vdots & \ddots & \vdots & \vdots & \\ 0 & 0 & \cdots & 0 & 0 & \vdots & 0 & 0 & \cdots & 1 & 0 \\ 0 & 0 & \cdots & 0 & 0 & \vdots & 0 & 0 & \cdots & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 & \vdots & 0 & 0 & \cdots & 0 & 0 \\ 0 & 1 & \cdots & 0 & 0 & \vdots & 0 & 0 & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots & & \vdots & \ddots & \vdots & \vdots & \\ 0 & 0 & 0 & \cdots & 1 & 0 & \vdots & 0 & 0 & \cdots & 0 & 0 \\ 0 & 0 & \cdots & 0 & 1 & \vdots & 0 & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ Y_a & Y_b & 0 & \cdots & 0 & 0 & \vdots & 1 & 0 & \cdots & 0 & 0 \\ Y_b & Y_c & Y_b & \cdots & 0 & 0 & \vdots & 0 & 1 & \cdots & 0 & 0 \\ \vdots & & \ddots & \vdots & \vdots & & \vdots & \vdots & \ddots & \vdots & \vdots & \\ 0 & 0 & & \ddots & Y_c & Y_b & \vdots & 0 & 0 & \cdots & 1 & 0 \\ 0 & 0 & & & Y_b & Y_a & \vdots & 0 & 0 & \cdots & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 & \vdots & Z_s/2 & 0 & \cdots & 0 & 0 \\ 0 & 1 & \cdots & 0 & 0 & \vdots & 0 & \ddots & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots & & \vdots & & Z_s/2 & \vdots & \\ 0 & 0 & \cdots & 1 & 0 & \vdots & 0 & 0 & \cdots & \ddots & 0 \\ 0 & 0 & \cdots & 0 & 1 & \vdots & 0 & 0 & \cdots & 0 & Z_s/2 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & 0 & 0 & \vdots & 1 & 0 & \cdots & 0 & 0 \\ 0 & 0 & \cdots & 0 & 0 & \vdots & 0 & 1 & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots & & \vdots & \ddots & \vdots & \vdots & \\ 0 & 0 & \cdots & 0 & 0 & \vdots & 0 & 0 & \cdots & 1 & 0 \\ 0 & 0 & \cdots & 0 & 0 & \vdots & 0 & 0 & \cdots & 0 & 1 \end{bmatrix} \quad (2.4a)$$

$$\textit{where} \qquad Y_a = Y_p + \frac{1}{Z_s} \qquad Y_b = -\frac{1}{Z_s} \qquad Y_a = Y_p + \frac{2}{Z_s}.$$

$$[T]_\Pi = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 & \vdots & 0 & 0 & \cdots & 0 & 0 \\ 0 & 1 & \cdots & 0 & 0 & \vdots & 0 & 0 & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots & \\ 0 & 0 & 0 & \cdots & 1 & 0 & \vdots & 0 & 0 & \cdots & 0 & 0 \\ 0 & 0 & \cdots & 0 & 1 & \vdots & 0 & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ Y_a & Y_b & 0 & \cdots & 0 & 0 & \vdots & 1 & 0 & \cdots & 0 & 0 \\ Y_b & Y_c & Y_b & \cdots & 0 & 0 & \vdots & 0 & 1 & \cdots & 0 & 0 \\ \vdots & & \ddots & \vdots & \vdots & & \vdots & \vdots & \ddots & \vdots & \vdots & \\ 0 & 0 & & \ddots & Y_c & Y_b & \vdots & 0 & 0 & \cdots & 1 & 0 \\ 0 & 0 & & & Y_b & Y_a & \vdots & 0 & 0 & \cdots & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 & \vdots & 2Z_s & 0 & \cdots & 0 & 0 \\ 0 & 1 & \cdots & 0 & 0 & \vdots & 0 & Z_s & & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots & & Z_s & \vdots & \\ 0 & 0 & \cdots & 1 & 0 & \vdots & 0 & 0 & \cdots & Z_s & 0 \\ 0 & 0 & \cdots & 0 & 1 & \vdots & 0 & 0 & \cdots & 0 & 2Z_s \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & 0 & 0 & \vdots & 1 & 0 & \cdots & 0 & 0 \\ 0 & 0 & \cdots & 0 & 0 & \vdots & 0 & 1 & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots & & \vdots & \ddots & \vdots & \vdots & \\ 0 & 0 & \cdots & 0 & 0 & \vdots & 0 & 0 & \cdots & 1 & 0 \\ 0 & 0 & \cdots & 0 & 0 & \vdots & 0 & 0 & \cdots & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 & \vdots & 0 & 0 & \cdots & 0 & 0 \\ 0 & 1 & \cdots & 0 & 0 & \vdots & 0 & 0 & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots & \\ 0 & 0 & 0 & \cdots & 1 & 0 & \vdots & 0 & 0 & \cdots & 0 & 0 \\ 0 & 0 & \cdots & 0 & 1 & \vdots & 0 & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ Y_a & Y_b & 0 & \cdots & 0 & 0 & \vdots & 1 & 0 & \cdots & 0 & 0 \\ Y_b & Y_c & Y_b & \cdots & 0 & 0 & \vdots & 0 & 1 & \cdots & 0 & 0 \\ \vdots & & \ddots & \vdots & \vdots & & \vdots & \vdots & \ddots & \vdots & \vdots & \\ 0 & 0 & & \ddots & Y_c & Y_b & \vdots & 0 & 0 & \cdots & 1 & 0 \\ 0 & 0 & & & Y_b & Y_a & \vdots & 0 & 0 & \cdots & 0 & 1 \end{bmatrix} \quad (2.4b)$$

$$\textit{where} \qquad Y_a = \frac{Y_p}{4} + \frac{1}{2Z_s} \qquad Y_b = -\frac{1}{2Z_s} \qquad Y_c = \frac{Y_p}{2} + \frac{1}{Z_s}.$$

As can be seen in Eq. (2.4), the transmission matrix for a column of unit cells is sparse, which enables a reduction in memory and CPU time when applied to realistic structures. Using the 2×2 block matrix representation in Eq. (2.4), the transmission matrix can be used to relate the voltages and currents as

$$\begin{aligned} \overline{V_{in}} &= [T_A]\overline{V_{out}} + [T_B]\overline{I_{out}} \\ \overline{I_{in}} &= [T_C]\overline{V_{out}} + [T_D]\overline{I_{out}} \end{aligned} \quad (2.5)$$

$$\textit{where} \qquad \overline{V_{in}} = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{bmatrix} \quad \overline{I_{in}} = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix} \quad \overline{V_{out}} = \begin{bmatrix} V_{N+1} \\ V_{N+2} \\ \vdots \\ V_{2N} \end{bmatrix} \quad \overline{I_{out}} = \begin{bmatrix} I_{N+1} \\ I_{N+2} \\ \vdots \\ I_{2N} \end{bmatrix}.$$

Since the network is reciprocal, det[T]=1. The $2N \times 2N$ transmission matrix for the overall power distribution network, which consists of a cascade of two or more networks, can now be obtained by multiplying the individual matrices [34]. For the rectangular plane structure in Fig. 2.1, since all the matrices for the column of unit cells are the same, the response of the entire geometry can be obtained as a single $2N \times 2N$ matrix. The cascade connection of 2N-port networks is shown in Fig. 2.3 using the [T] matrix representation in Eq. (2.5).

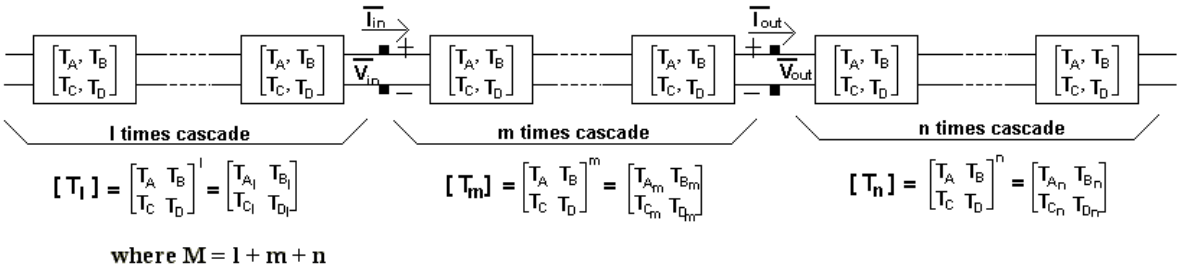


Fig. 2.3. Cascade connection.

For a cascade connection of 'M' $[T]$ matrices, where $[T_l]$ and $[T_n]$ represent the input and output matrices of the entire structure, the total voltage and current equations can be derived as

$$\overline{I_1} = \overline{I_{in}} - \overline{I_2} \qquad where \quad \overline{I_2} = \overline{Y_l}\,\overline{V_{in}}$$
$$\overline{I_3} = \overline{I_{out}} + \overline{I_4} \qquad where \quad \overline{I_4} = \overline{Y_n}\,\overline{V_{out}}$$

$$\begin{bmatrix} I & 0 \\ -\overline{Y_l} & I \end{bmatrix}\begin{bmatrix} \overline{V_{in}} \\ \overline{I_{in}} \end{bmatrix} = \begin{bmatrix} T_{Am} & T_{Bm} \\ T_{Cm} & T_{Dm} \end{bmatrix}\begin{bmatrix} I & 0 \\ \overline{Y_n} & I \end{bmatrix}\begin{bmatrix} \overline{V_{out}} \\ \overline{I_{out}} \end{bmatrix} \tag{2.6}$$

$$where \qquad \overline{Y_l} = T_{Dl}^{-1}T_{Cl} \quad \overline{Y_n} = T_{Cn}T_{An}^{-1}\,.$$

A block representation of Eq. (2.6) showing the input and output voltage and current variables is shown in Fig. 2.4.

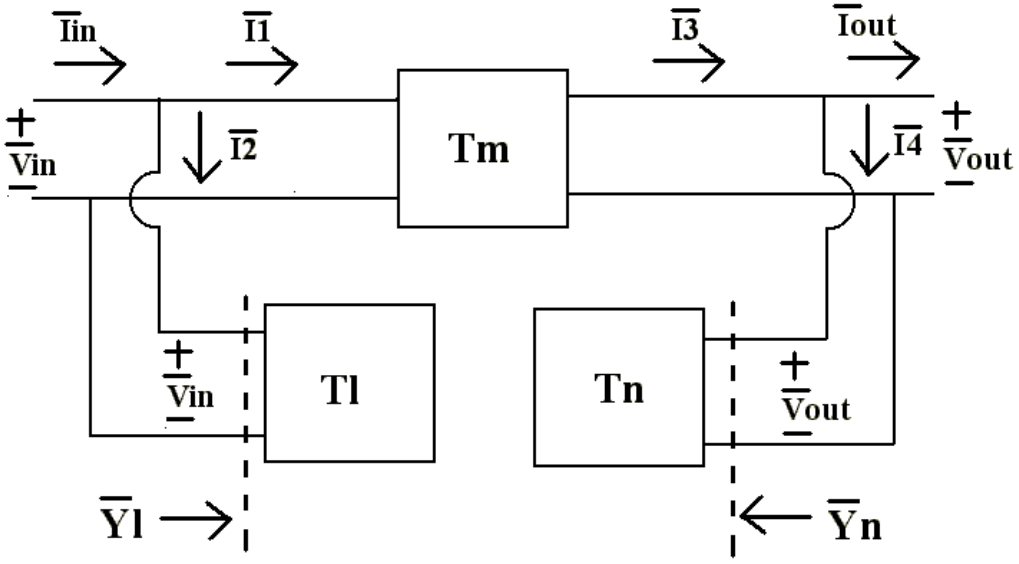


Fig. 2.4. Block diagram of entire system.

In Eq. (2.6), $\overline{Y_l}$ and $\overline{Y_n}$ are $N \times N$ input admittance matrices seen looking into the l^{th} column from the input ports and $(l+m+1)^{th}$ from the output ports, respectively. Using Eq. (2.6), the overall $2N \times 2N$ transmission matrix $\left[T'\right]$ for the entire structure is:

$$\left[T'\right] = [T_{Yl}][T_m][T_{Yn}] = \begin{bmatrix} \vdots & \vdots & \vdots \\ T'_A & \cdots & T'_B \\ \vdots & \vdots & \vdots \\ T'_C & \cdots & T'_D \\ \vdots & \vdots & \vdots \end{bmatrix} \tag{2.7}$$

where $$[T_{Yl}] = \begin{bmatrix} I & 0 \\ T_{Dl}^{-1}T_{Cl} & I \end{bmatrix} \quad [T_{Yn}] = \begin{bmatrix} I & 0 \\ T_{Cn}T_{An}^{-1} & I \end{bmatrix}.$$

It is important to note that if indices 'l' or 'n' are zeros, T_{Yl} or T_{Yn} are $2N \times 2N$ identity matrices, which represent open circuits. Using the transmission matrix of the network, the $2N \times 2N$ impedance matrix [Z] of the network can be derived, which can be simplified and represented as:

$$\begin{aligned} \overline{V_{in}} &= [Z_A]\overline{I_{in}} - [Z_B]\overline{I_{out}} \\ \overline{V_{out}} &= [Z_C]\overline{I_{in}} - [Z_D]\overline{I_{out}} \end{aligned} \tag{2.8}$$

where $$[Z_A] = \begin{bmatrix} Z_{1,1} & \cdots & Z_{1,N} \\ \vdots & & \vdots \\ Z_{N,1} & \cdots & Z_{N,N} \end{bmatrix} \quad [Z_B] = \begin{bmatrix} Z_{1,N+1} & \cdots & Z_{1,2N} \\ \vdots & & \vdots \\ Z_{N,N+1} & \cdots & Z_{N,2N} \end{bmatrix}$$

$$[Z_C] = \begin{bmatrix} Z_{N+1,1} & \cdots & Z_{N+1,N} \\ \vdots & & \vdots \\ Z_{2N,1} & \cdots & Z_{2N,N} \end{bmatrix} \quad [Z_D] = \begin{bmatrix} Z_{N+1,N+1} & \cdots & Z_{N+1,2N} \\ \vdots & & \vdots \\ Z_{2N,N+1} & \cdots & Z_{2N,2N} \end{bmatrix}.$$

As mentioned earlier, since the network is reciprocal, $Z_B = Z_C$ and $Z_{i,j} = Z_{j,i}$. Using the relation between the transmission matrix and the impedance matrix, the impedance of the power plane becomes:

$$[Z_B]=[Z_C]=\left[T_C^{'}\right]^{-1} \quad [Z_A]=\left[T_A^{'}\right][Z_C] \quad [Z_D]=[Z_C]\left[T_D^{'}\right]. \tag{2.9}$$

During the design of the power delivery system, the impedance at specific points on the network is often desired. This can either be the self impedance at a port or the transfer impedance between ports. Using Eq. (2.9), the self impedance and transfer impedance can be computed as:

$$Z_{Ai,j}=\frac{det\begin{bmatrix} T_{C1,1}^{'} & T_{C1,2}^{'} & \cdots & T_{C1,N}^{'} \\ T_{C2,1}^{'} & T_{C2,2}^{'} & \cdots & T_{C2,N}^{'} \\ \vdots & \vdots & \vdots & \vdots \\ \underline{\underline{T_{Ai,1}^{'}}} & \underline{\underline{T_{Ai,2}^{'}}} & \cdots & \underline{\underline{T_{Ai,N}^{'}}} \\ \vdots & \vdots & \vdots & \vdots \\ T_{CN,1}^{'} & T_{CN,2}^{'} & \cdots & T_{CN,N}^{'} \end{bmatrix} \leftarrow_{jth}}{det\left[T_C^{'}\right]} \tag{2.10}$$

$$Z_{Di,j}=\frac{det\begin{bmatrix} T_{C1,1}^{'} & T_{C1,2}^{'} & \cdots & \underline{\underline{T_{D1,j}^{'}}} & \cdots & T_{C1,N}^{'} \\ T_{C2,1}^{'} & T_{C2,2}^{'} & \cdots & \underline{\underline{T_{D2,j}^{'}}} & \cdots & T_{C2,N}^{'} \\ \vdots & \vdots & \cdots & \vdots & \cdots & \vdots \\ T_{CN,1}^{'} & T_{CN,2}^{'} & \cdots & \underline{\underline{T_{DN,j}^{'}}} & \cdots & T_{CN,N}^{'} \end{bmatrix}}{det\left[T_C^{'}\right]} \qquad Z_{Ci,j}=(-1)^{i+j}\frac{det\left[M_{Cj,i}\right]}{det\left[T'_C\right]}$$

where $\left[M_{Cj,i}\right]$ is the $(N-1)\times(N-1)$ matrix obtained from $\left[T_C^{'}\right]$ by deleting the j^{th} row and the i^{th} column.

2.3 Application to Irregular Geometries

The transmission matrix modeling approach discussed in the previous section can be extended to irregular geometries. As an example, the method has been applied to an L-shaped plane structure, as described in Fig. 2.5. The modeling method for the L-shaped power/ground planes is similar to that for the rectangular planes with the difference that two different matrix sizes are required for the L-shaped structure. This is because the size of the [T] matrix in Fig. 2.3 is not constant as indicated by dashed lines in Fig. 2.5. Using an identity matrix for the interface of the smaller column, the matrix size for the smaller column can be expanded to match the larger column in Fig. 2.5.

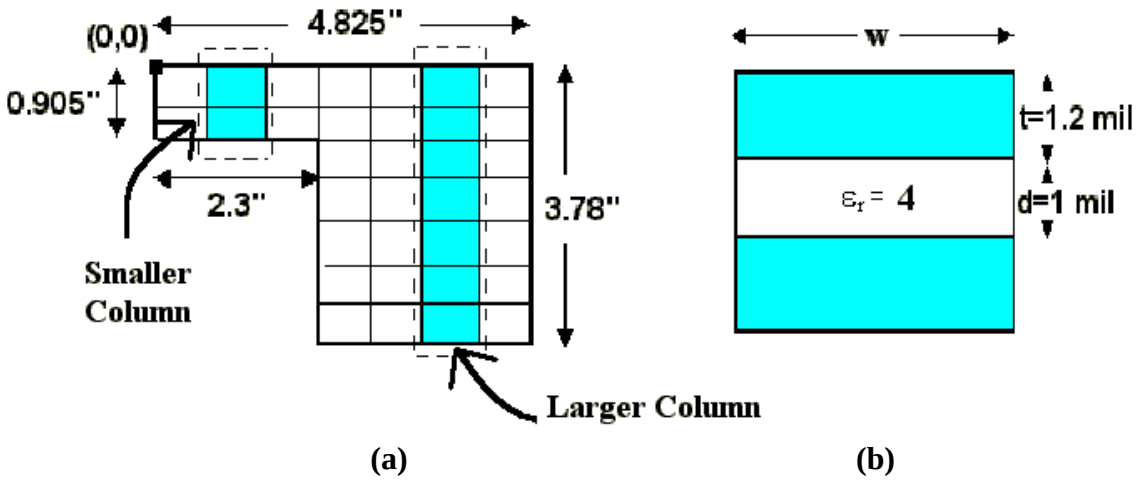


Fig. 2.5. (a) Top view for L-shaped plane (b) side view for a unit cell.

To further illustrate the procedure, assume that the smaller column can be represented as a $2k \times 2k$ square matrix ($[T_S]_{2k\times 2k}$) formed by 2k-port networks having k input ports and k output ports. Similarly, let the larger column be represented as a $2N \times 2N$ matrix with $N > k$. The matrix representing the smaller column can be expanded and written as:

$$[Ts]_{2N\times 2N}=\begin{bmatrix} Ts_A & 0 & \vdots & Ts_B & 0 \\ 0 & I & \vdots & 0 & 0 \\ \cdots & \cdots & \vdots & \cdots & \cdots \\ Ts_C & 0 & \vdots & Ts_D & 0 \\ 0 & 0 & \vdots & 0 & I \end{bmatrix} \quad where\ [Ts]_{2k\times 2k}=\begin{bmatrix} Ts_A & \vdots & Ts_B \\ \cdots & \vdots & \cdots \\ Ts_C & \vdots & Ts_D \end{bmatrix}. \quad (2.11)$$

As a result, using a single matrix size for the columns, the matrix of the smaller column is expanded to match the matrix size of the larger column by changing the elements at the interface. After the matrix expansion, the impedance computation for the L-shaped planes is similar to the rectangular planes, as described in the previous section.

2.4 Incorporation of Decoupling Capacitors

In the transmission matrix method, decoupling capacitors can readily be included into the matrices. The impedance of a decoupling capacitor is represented using Eq. (1.3). The transmission matrix for decoupling capacitors can be represented as follows:

$$[T_{cap}]=\begin{bmatrix} I & 0 \\ Tc_{cap} & I \end{bmatrix} \quad where \quad [Tc_{cap}]=\begin{bmatrix} Y_{cap,1} & & & & \\ & \ddots & & 0 & \\ & & Y_{cap,i} & & \\ & 0 & & \ddots & \\ & & & & Y_{cap,n} \end{bmatrix} \quad (2.12)$$

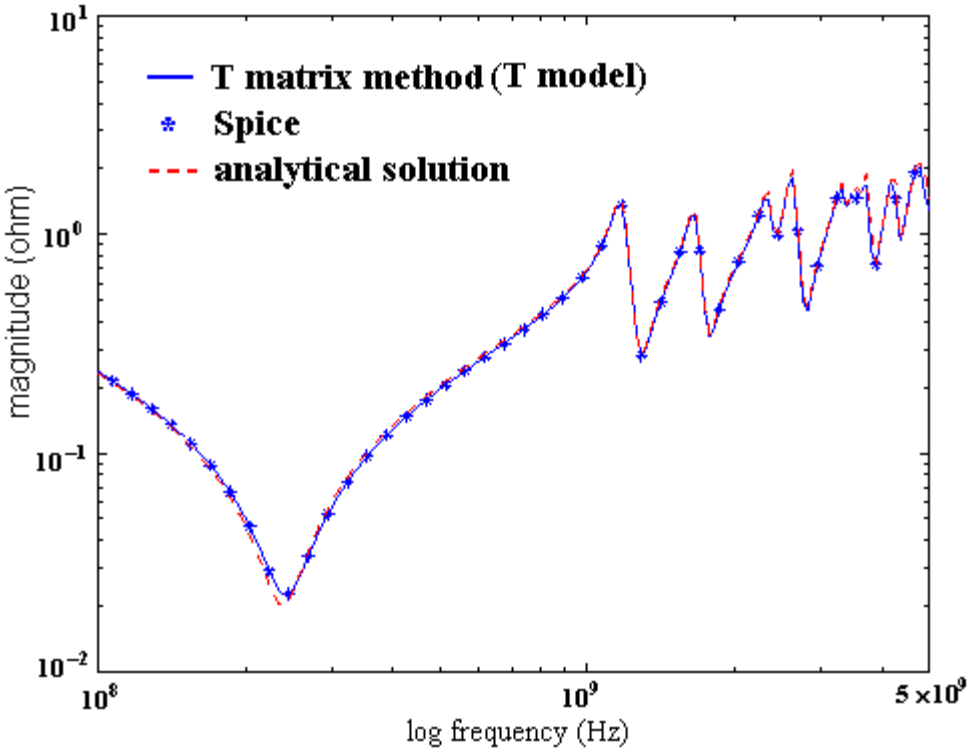
where $Y_{cap,i}=(Z_{cap,i})^{-1}$ and if there is no decoupling capacitor in the i^{th} row, then $Y_{cap,i}=0$. As an example, let the decoupling capacitors be connected between the k^{th} column and the $(k+1)^{th}$ column of unit cells shown in Fig. 2.4. Then, the transmission matrix of the entire structure can be updated as:

$$[T]_{total} = \cdots [T]_k \times [T]_{cap} \times [T]_{k+1} \cdots \quad (2.13)$$

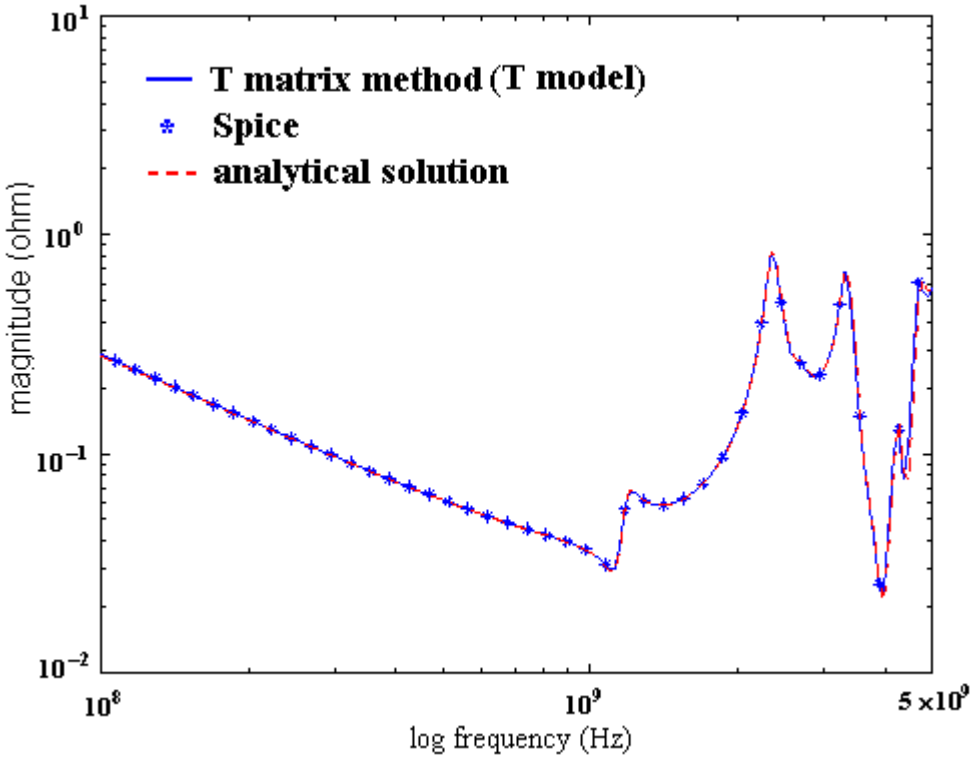
2.5 Application of the Transmission Matrix Method to a Plane Pair

2.5.1 Rectangular Geometry

To check the accuracy of the transmission matrix method, the results have been compared with two other techniques for a rectangular plane structure shown in Fig. 2.1 [26]. The two techniques are based on the analytical solution described in [24], [25] and the SPICE simulation of a distributed RLCG network described in [23], [33]. The plane has dimensions of 2.5 inch by 2.5 inch with a 1-mil thick FR4 dielectric with relative permittivity e_r = 4. Both conductor planes are assumed to be copper ($s_c = 5.8 \times 10^7$ S/m) with a thickness of 1.2 mils. Using a unit cell size of 0.1 inch by 0.1 inch, the rectangular plane was divided into 25 by 25 cells. Using Eq. (2.1), the unit cell parameters were computed as C = 8.983 *pF*, L = 31.92 *pH*, Rdc = 1.131 mW, and Rac = $0.5218\sqrt{f}$ mW. For this test case, the dielectric loss was assumed to be negligible (no G_d component). For comparison, the propagating modes were set to m, n = 100 in the analytical solution described in [24], [25]. An excitation point (Port 1) was located at (x = 0 inch, y = 0.05 inch) and an observation point (Port 2) at (x = 1.2 inch, y = 1.25 inch). Both the self impedance Z11 and transfer impedance Z12 were computed over the frequency range 100 MHz to 5 GHz, as shown in Fig. 2.6. All these methods show good agreement.



(a)

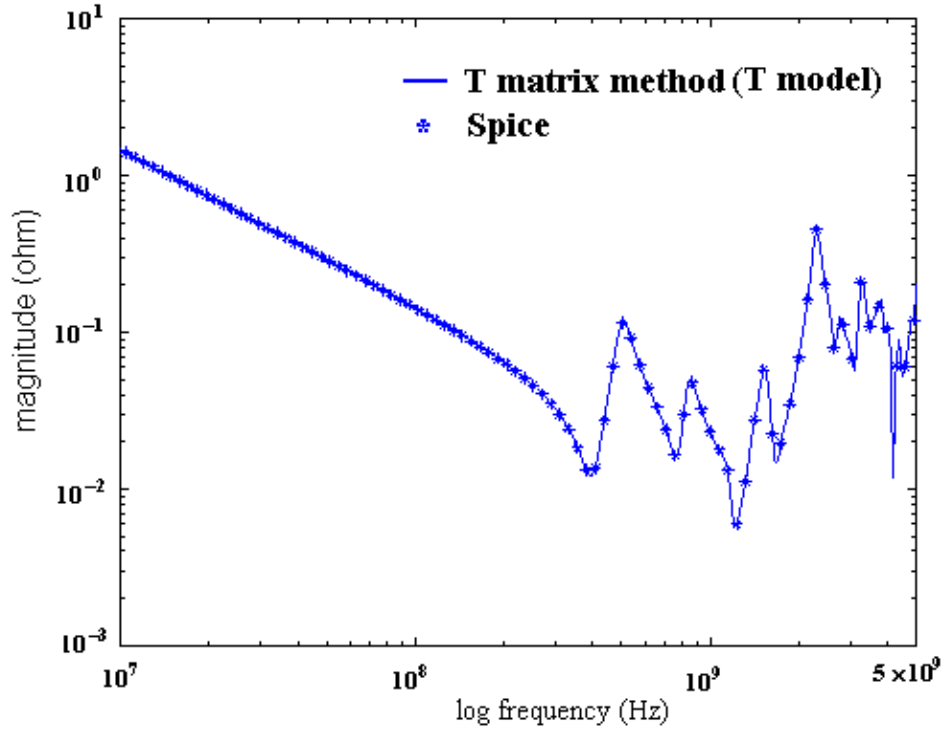


(b)

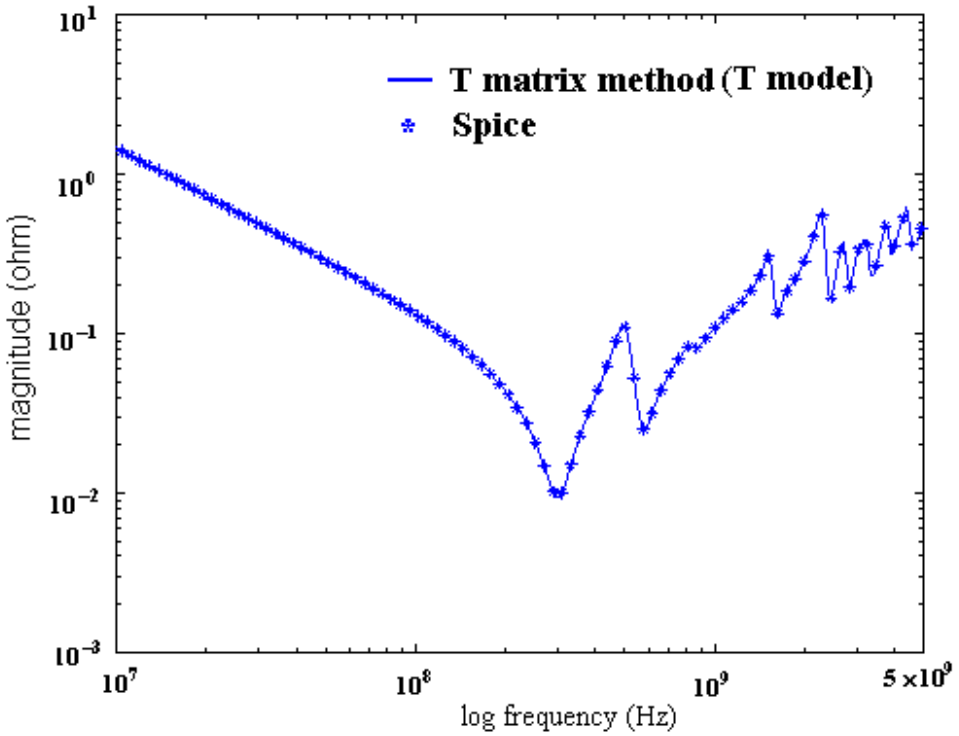
Fig. 2.6. Rectangular plane: (a) self impedance at Port1 and (b) transfer impedance.

2.5.2 L-Shaped Geometry

The transmission matrix method was next applied to an L-shaped plane described in Fig. 2.5 [26]. This structure is currently being used in Sun workstations. The L-shaped structure provided by Sun Microsystems consisted of two pairs of planes connected through 180 vertical vias, which can be represented as parallel inductances. The inductance contribution from the vias was therefore negligible. By reducing the dielectric separation to half its original value and increasing the metal thickness to double its original value, a pair of power/ground planes was simulated to mimic two plane pairs. Therefore, the test structure consisted of a pair of planes with 1-mil thick FR4 dielectric with relative permittivity e_r = 4. The conductor planes were made of copper (s_c = 5.8×10^7 S/m) with a thickness of 1.2 mils. Using a unit cell size of 0.2 inch by 0.2 inch, the R, L, and C parameters were computed as C = 35.93 pF, L = 31.92 pH, Rdc = 1.131 mW, and Rac = $0.5218\sqrt{f}$ mW. An excitation point (Port 1) was defined at (x = 3.19 inch, y = 2.68 inch) and an observation point (Port 2) at (x = 3.63 inch, y = 2.33 inch) for a co-ordinate system with the origin as defined in Fig. 2.5. The frequency response of the self impedance and transfer impedance for the L-shaped plane is shown in Fig. 2.7 and has been compared with SPICE. The results from the two models show good correlation over a frequency range 10 MHz to 5 GHz.



(a)

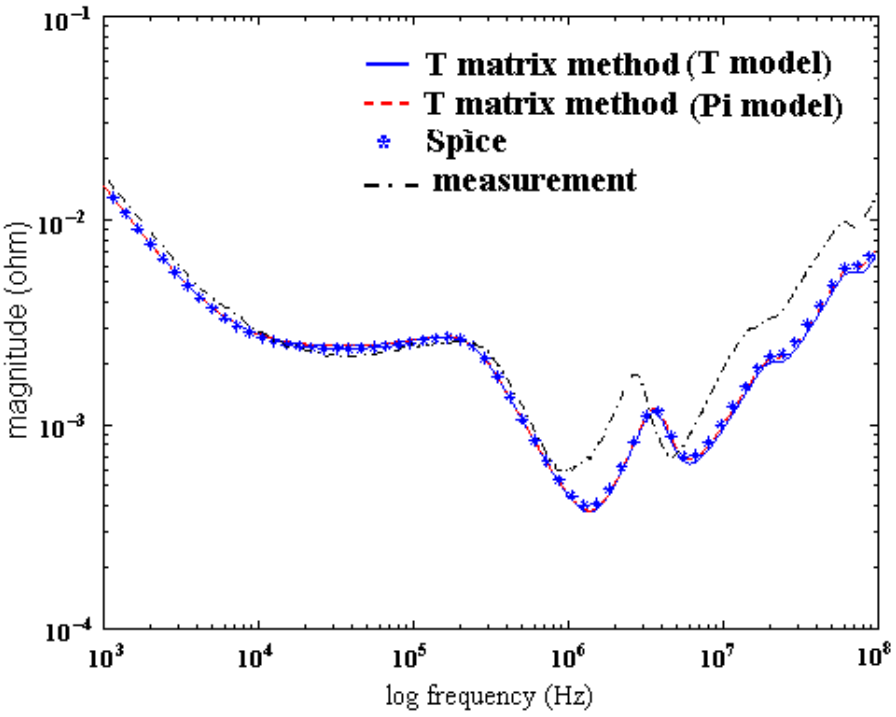


(b)

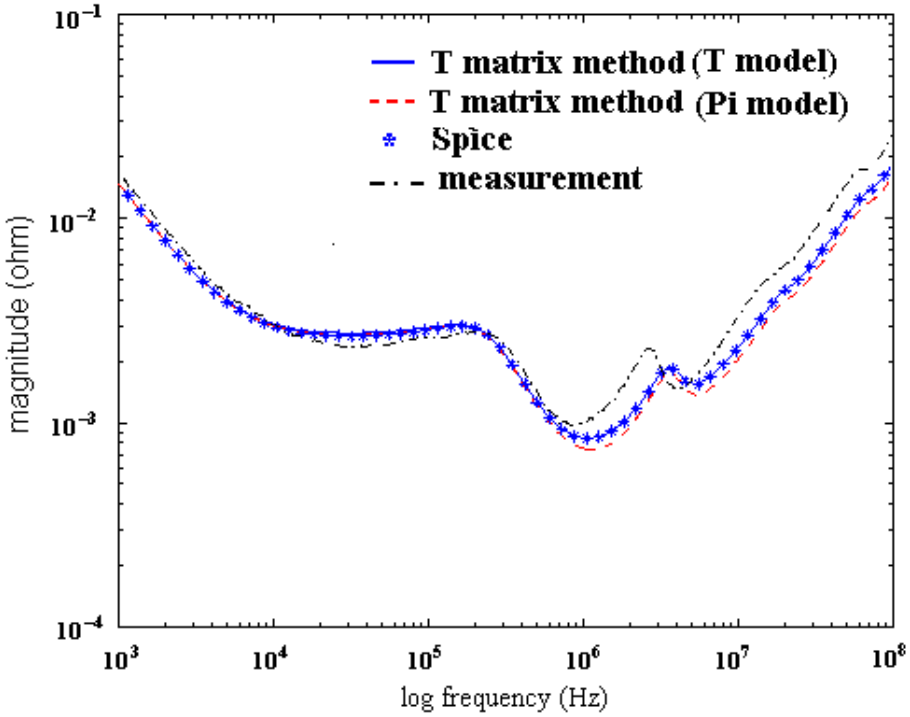
Fig. 2.7. L-shaped plane without decoupling capacitors: (a) transfer impedance and (b) self impedance at Port 2.

Resonant frequencies caused by the reflection of incident waves at the plane edges result in build-up of energy between the planes, which can induce excessive simultaneous switching noise (SSN). To nullify the resonances and suppress SSN, decoupling capacitors with a low-impedance response are often attached to the PDS. Since a capacitor is nonideal, the effective series resistance (ESR) and the effective series inductance (ESL) values of a capacitor affect the frequency response of the PDS. In this section, seven different capacitors with measured ESR, ESL, and C values were attached to the L-shaped plane. The measured values of the capacitors are shown in Fig. 1.4.

As mentioned earlier, the L-shaped plane is a realistic structure which contains ninety-seven decoupling capacitors of seven different types, as shown in Fig. 1.4. Their locations are defined in Appendix A. Each capacitor was included in the transmission matrix, as described in Eqs. (2.12) and (2.13). The self impedance and transfer impedance were computed at the ports defined earlier, which are shown in Fig. 2.8. Using both the T and Π models, the structure was simulated and the results were found to agree with SPICE. However, Fig. 2.8 shows a discrepancy between simulation and measurements above 1 MHz. The major reason for the difference between the measured and simulated results in Fig. 2.8 was due to horizontal strips in series with the planes making contact with the vias. These vias were used as thermal relief vias by Sun Microsystems. The thermal relief vias were accidentally connected to planes. This effect was not included in the simulation. This caused an error between the simulation and measurements resulting in the measurements having larger inductances than the simulated results. As a result, the resonances moved to lower frequencies and had larger magnitudes above 1 MHz as compared to the simulated results.



(a)



(b)

Fig. 2.8. L-shaped plane with decoupling capacitors: (a) transfer impedance and (b) self impedance at Port 2.

Using an Inverse Fast Fourier Transform (IFFT), a transient response in the time domain can be generated from the frequency domain data. The equivalent circuit diagram using a two-port impedance matrix is shown in Fig. 2.9. To compute the transient response of the plane, the time signal source was first changed to a frequency-domain representation using a Fast Fourier Transform (FFT). The frequency response at the output was next computed by evaluating the product of the transfer impedance obtained from the impedance matrix and the current source. The output transfer voltage was then converted to a time-domain representation using an IFFT.

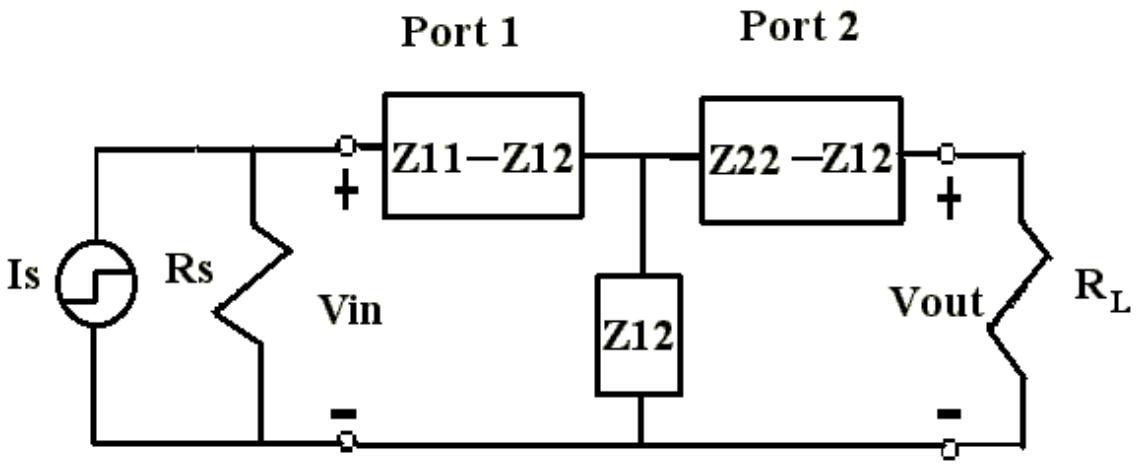
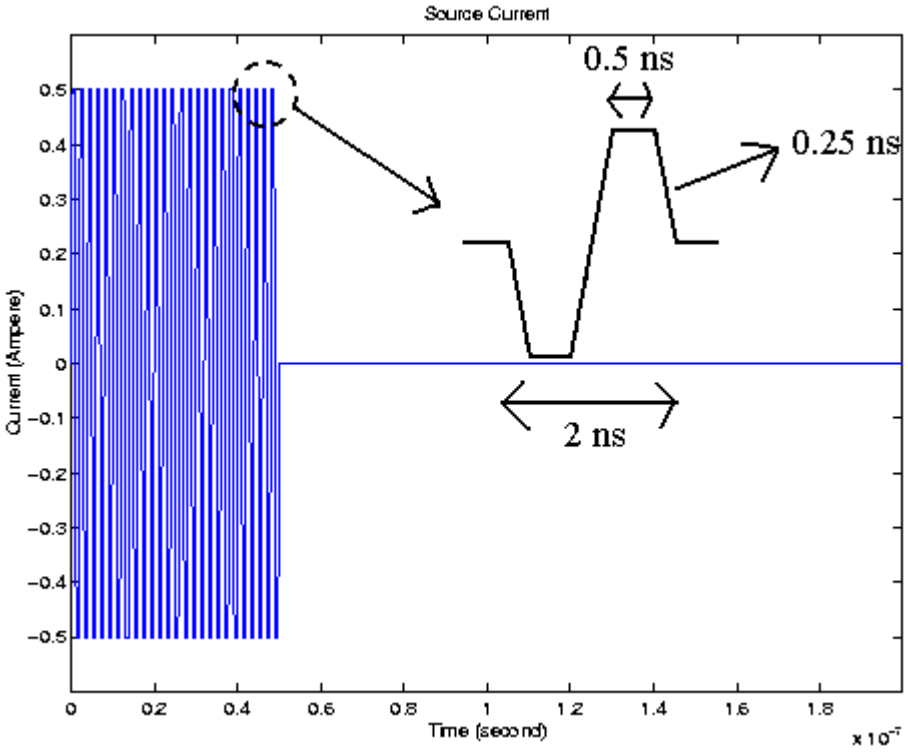


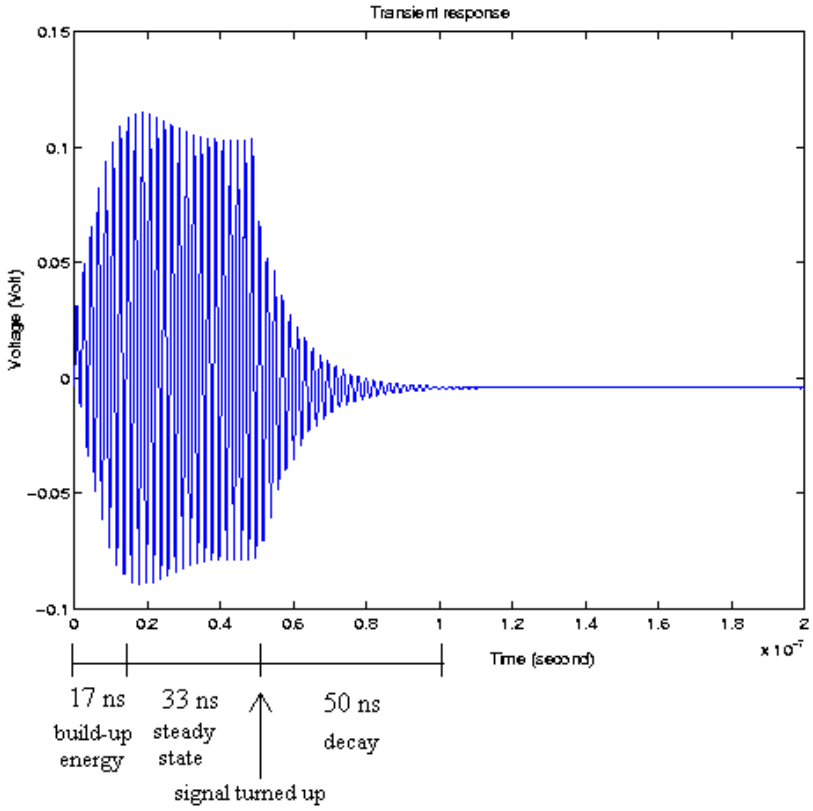
Fig. 2.9. Equivalent circuit for transient response.

For the L-shaped plane, a time signal output voltage was generated from the frequency impedance data from 5 MHz to 1 GHz. A one ampere current source (peak to peak) with open source resistance, consisting of 25 clock pulse waveforms having a width of 0.5 ns, rise time of 0.25 ns, fall time of 0.25 ns, and a period of 2 ns, was used and sampled up to 200 ns using a sampling interval of 0.25 ns, as shown in Fig. 2.10 (a).

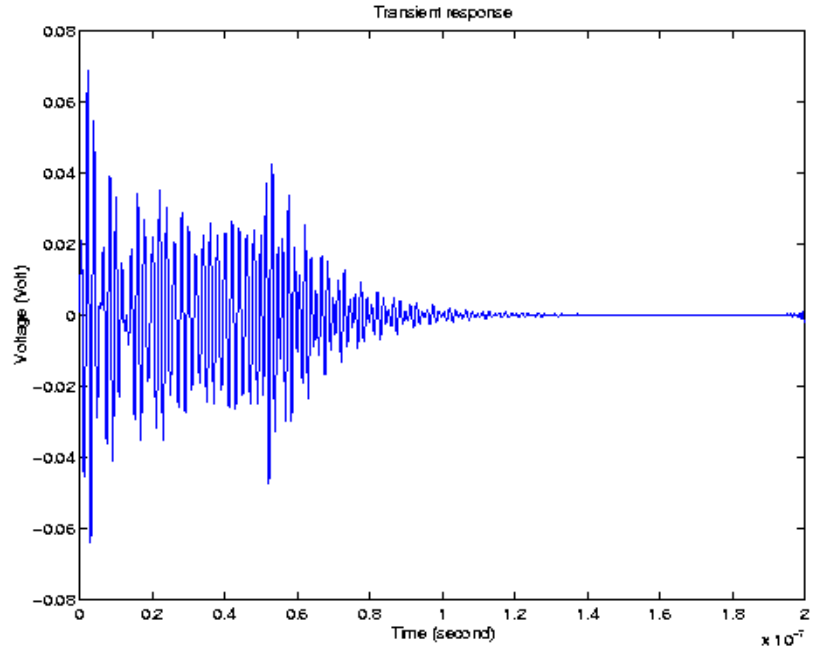
The source was placed at Port 1 in Fig. 2.5. After 50 ns, the source was turned off to understand the effect of the source on the cavity. The period of the source signal was set to the inverse of the first maximum resonant frequency (500 MHz). In Fig. 2.10, the response of the L-shaped cavity has been captured in the time domain. As is typical of a resonant cavity, initially the L-shaped plane builds up energy, then reaches the steady state and finally decays to zero after the power is turned off, as shown in Fig. 2.10 (b). The presence of the decoupling capacitors on the plane reduces the coupling between ports 1 and 2, as shown in Fig. 2.10 (c).



(a)



(b)



(c)

Fig. 2.10. Transient response of L-shaped plane: (a) current source at Port 1, (b) voltage output at Port 2 without decoupling capacitors and (c) voltage output at Port 2 with decoupling capacitors.

2.5.3 Split Planes

In this section, a split power plane structure with decoupling capacitors, as shown in Fig. 2.11 [18], [30], was analyzed with the Π model transmission matrix method. The power plane structure consists of two pairs of planes separated by a dielectric. The bottom plane is continuous while the top plane is split into two parts with a 5 mm gap. The two planes are connected together with a ferrite core, which is represented as a parallel equivalent circuit of C = 0.15 *pF*, R = 95 W and L = 0.17 *nH*, between points A and B shown in Fig. 2.11. The dimension of the planes is 300 mm by 120 mm with a 0.7 mm thick FR4 dielectric with relative permittivity e_r = 4. Both the top and bottom conductor planes are made of copper ($s_c = 5.8\times10^7$ S/m) with a thickness of 0.025 mm. The edges of the planes including the split plane edges are assumed to be magnetic walls, which is a good approximation over the frequency band of interest. The square and triangular marks form a uniform grid in Fig. 2.11 which indicate the locations of the decoupling capacitors with C = 220 *pF*, ESR = 0.1 W , ESL = 2 *nH*, and C = 10 *nF*, ESR = 0.1 W , ESL = 2 *nH*, respectively. An excitation port was located at the point 'S' (x = 175 mm, y = 40 mm), and two observation ports were defined at measurement points 'M1' (x = 50 mm, y = 1000 mm) and 'M2' (x = 200 mm, y = 100 mm). Using a unit cell size of 5 mm by 5 mm, the PDS was divided into 60 by 24 cells. The dielectric loss G_d was assumed to be negligible and therefore ignored. Fig. 2.12 shows the impedance magnitudes.

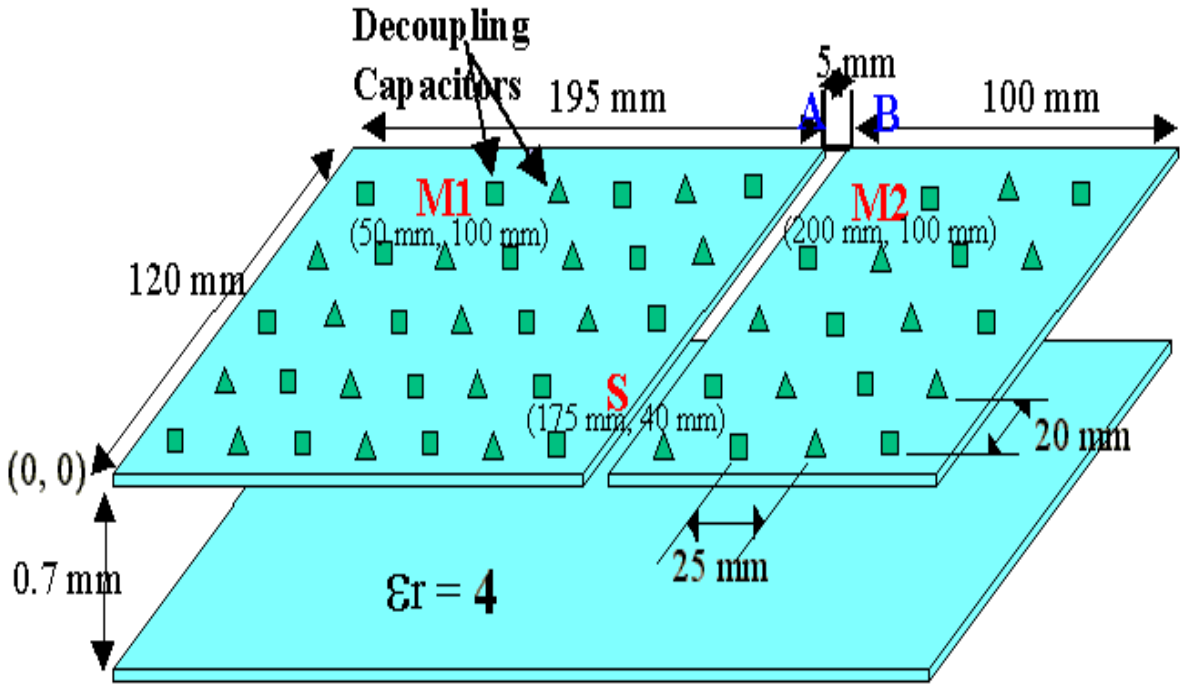
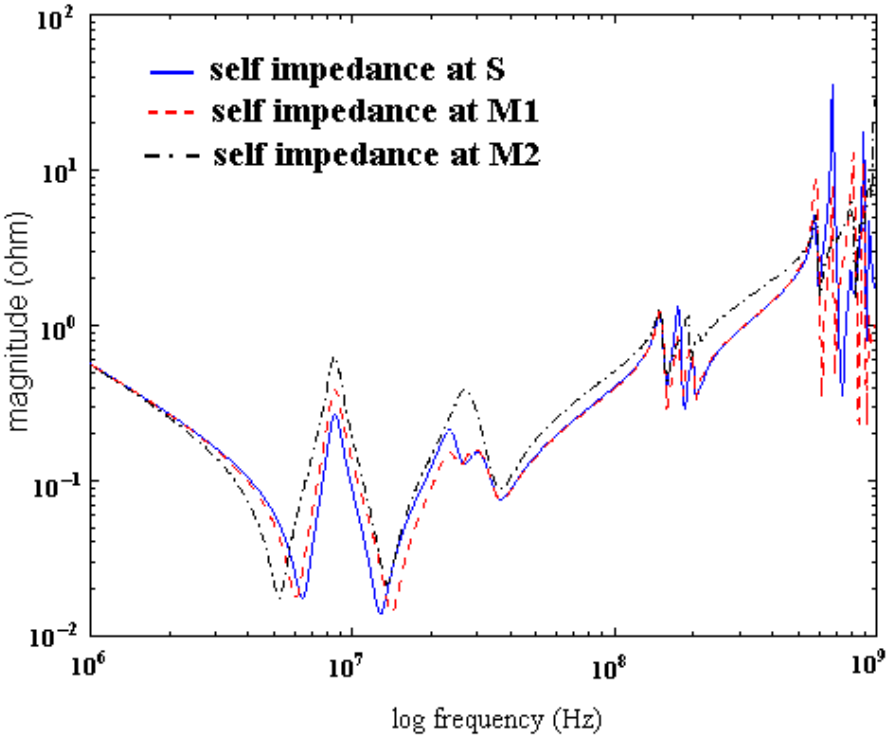
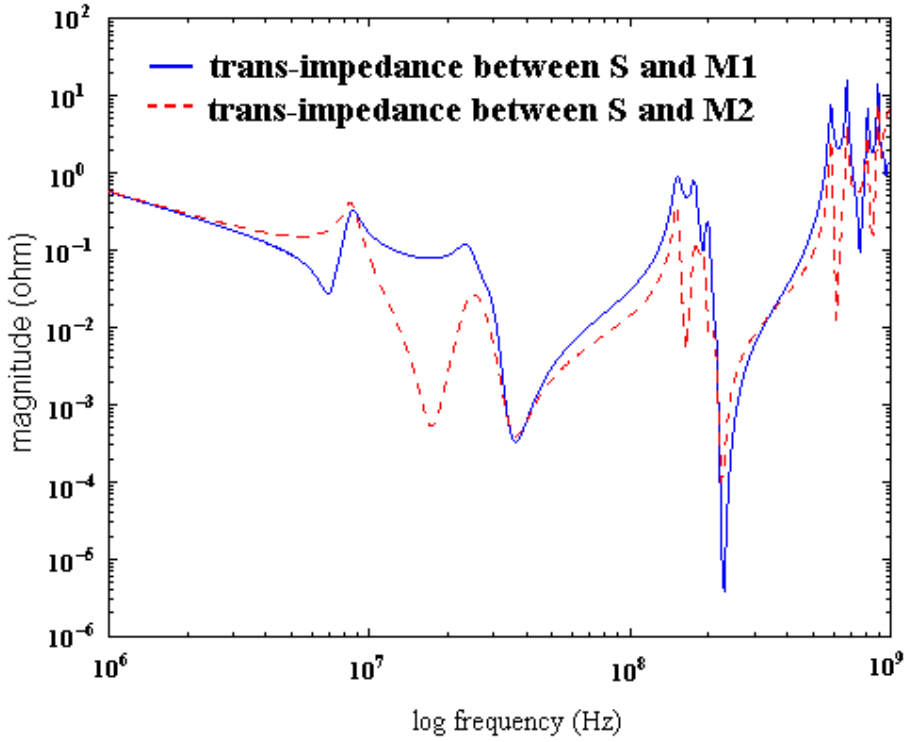


Fig. 2.11. Split plane structure.

The aim of this analysis was to evaluate the noise transferred to the smaller plane through the ferrite core for a source at the excitation port 'S'. Fig. 2.13 shows the transient response at port ‘M1’ and ‘M2’ using inverse fast Fourier transform (IFFT). In Fig. 2.13 (a), the voltage source (1 volt) consists of a step signal with a source resistor R_S = 10 Ω and 0.4 ns rise time. The voltage outputs at port ‘M1’ and ‘M2’ with open termination is shown in Fig. 2.13 (b). As shown in Fig. 2.13 (b), the coupled noise at port ‘M2’ is smaller than that of port ‘M1’.

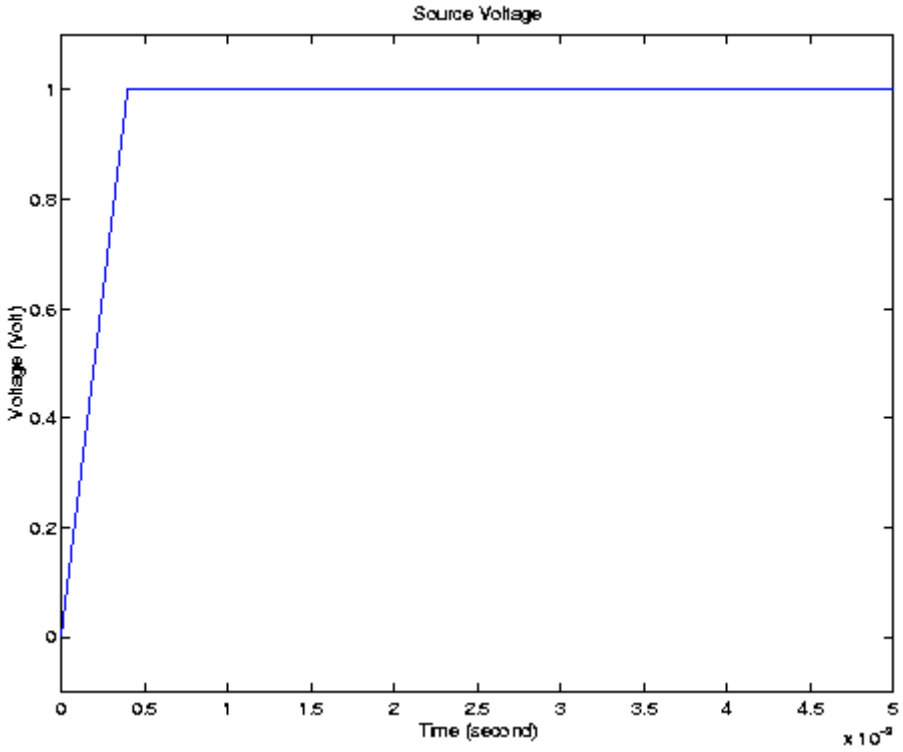


(a)

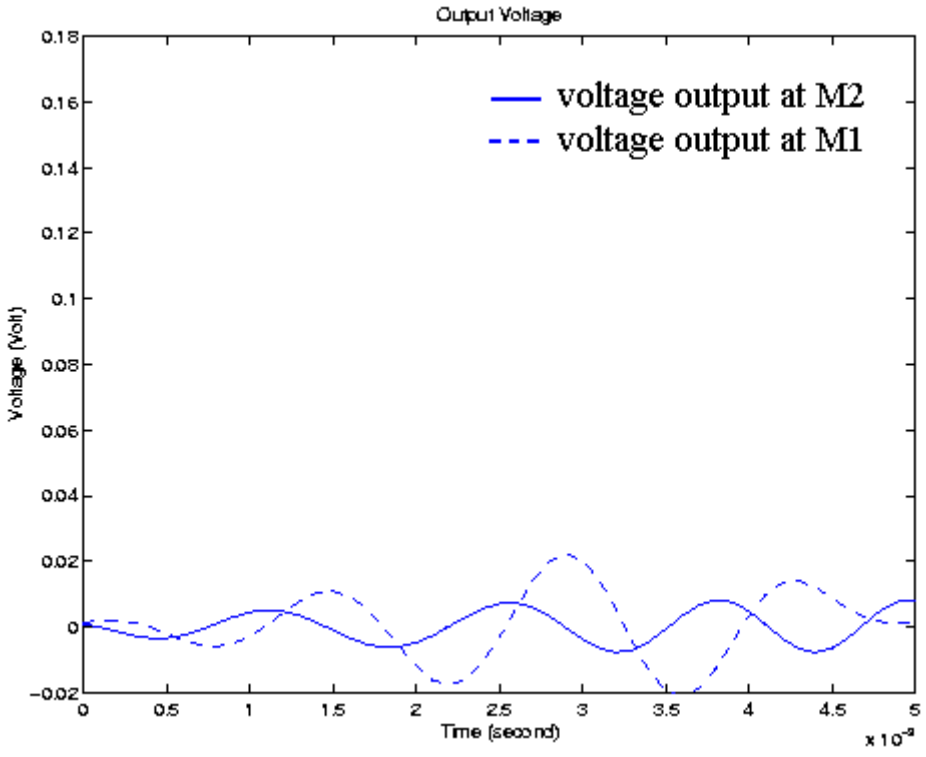


(b)

Fig. 2.12. Split plane with decoupling capacitors: (a) self impedances and (b) transfer impedances.



(a)



(b)

Fig. 2.13. Transient response of split planes: (a) voltage source and (b) voltage outputs.

2.5.4 Arbitrary Shaped Geometry

Mixed signal applications contain a combination of digital, RF, and analog circuits. In consumer mixed signal applications, the power distribution structure is typically of irregular shape. As an example of an irregular geometry, a Motorola Bravo Plus pager was selected. Fig. 2.14 shows the top view and two port locations P1 and P2 [27]. The board was assumed to have a 200-mm thick FR-4 dielectric, a 20-mm thick copper planes ($s_c = 5.8 \times 10^7$ S/m), dielectric of relative permittivity e_r = 4, and dielectric loss tangent $tan(d)$ = 0.02 at 5 GHz. Port 1 was located at (x = 0.5 cm, y = 0.5 cm) and Port 2 at (x = 1.1 cm, y = 3.1 cm) for a co-ordinate system with origin, as defined in Fig. 2.14. A unit cell with 0.1 cm by 0.1 cm size was used to analyze the structure. From the dimensions and parameters of the planes, the self impedance and transfer impedance between the two ports were computed using the transmission matrix method, as shown in Fig. 2.15. Due to the many boundaries in the structure, the resonant frequencies for an irregular shaped plane occur at more frequencies than in a rectangular plane.

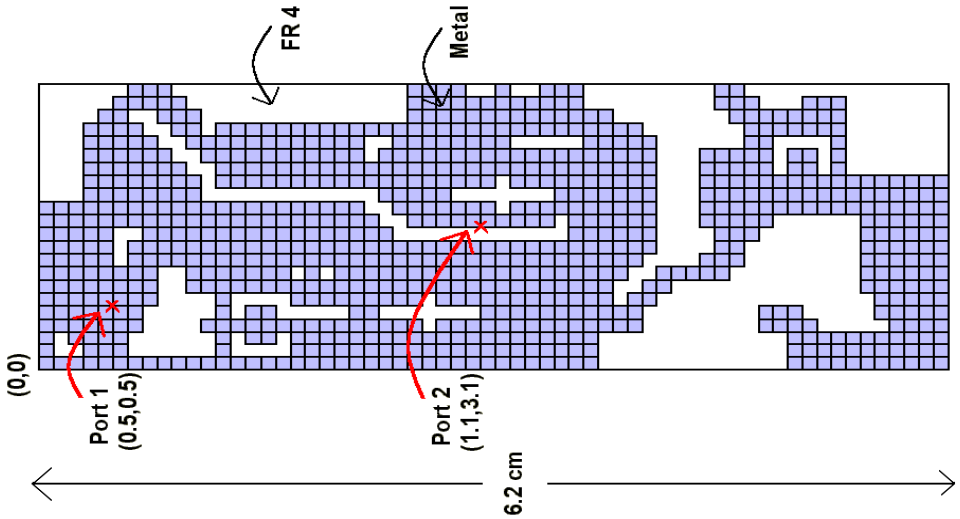


Fig. 2.14. Motorola Bravo Plus pager planes.

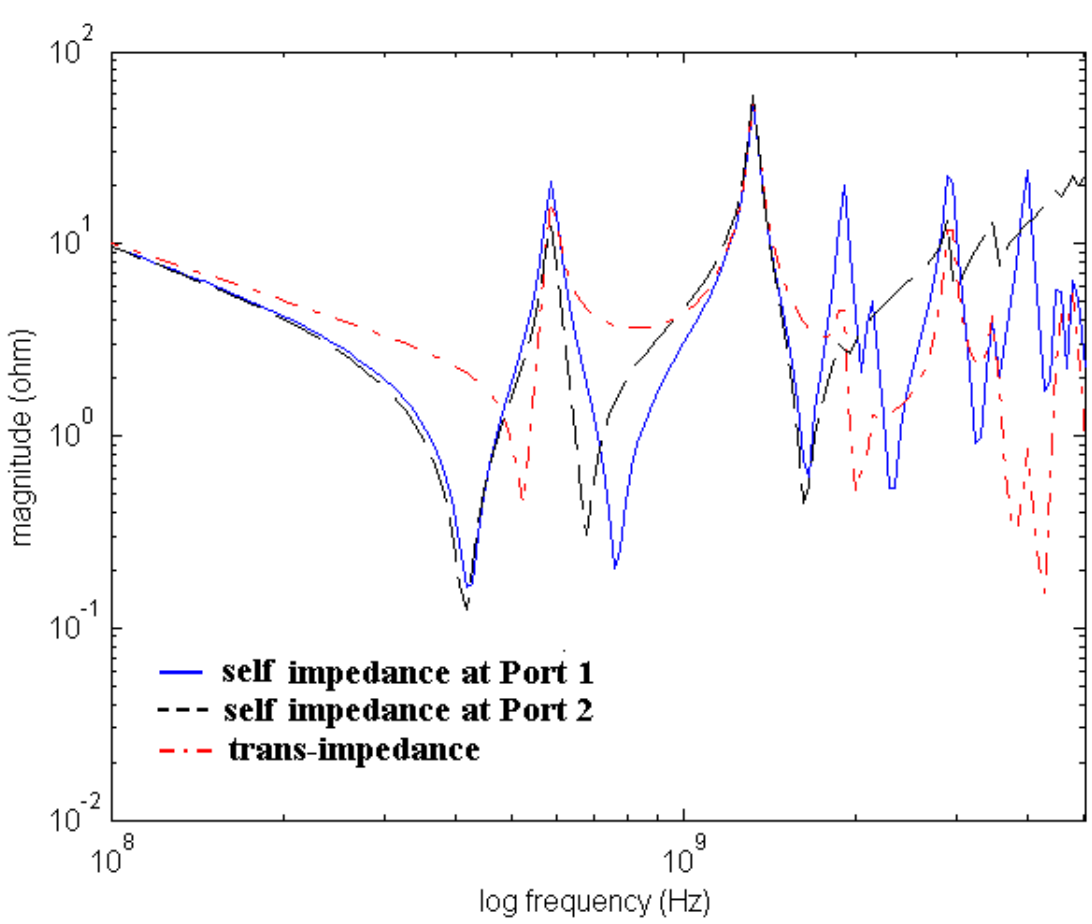
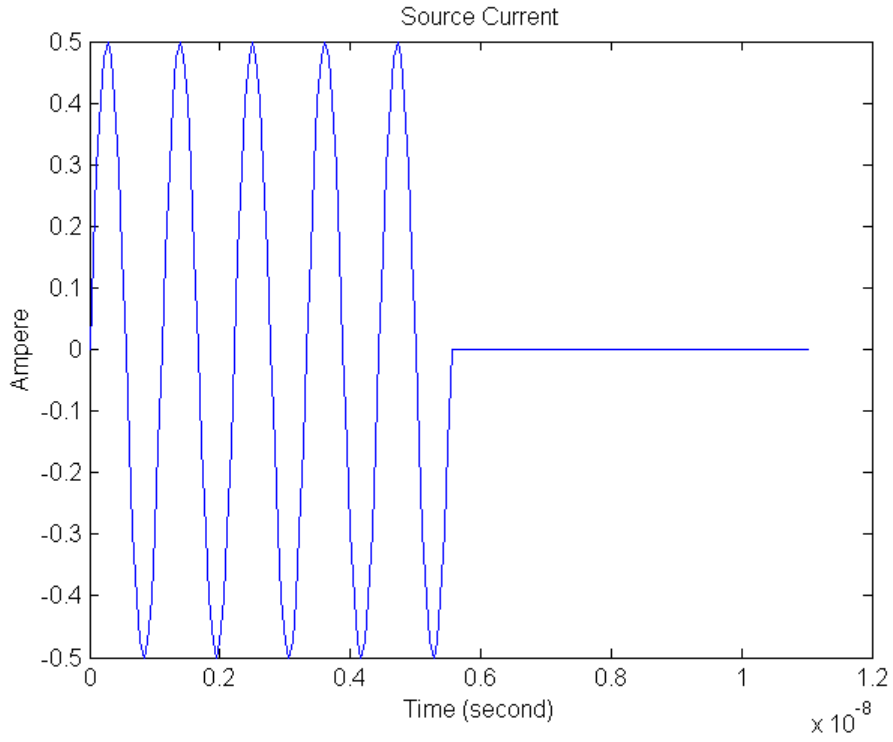
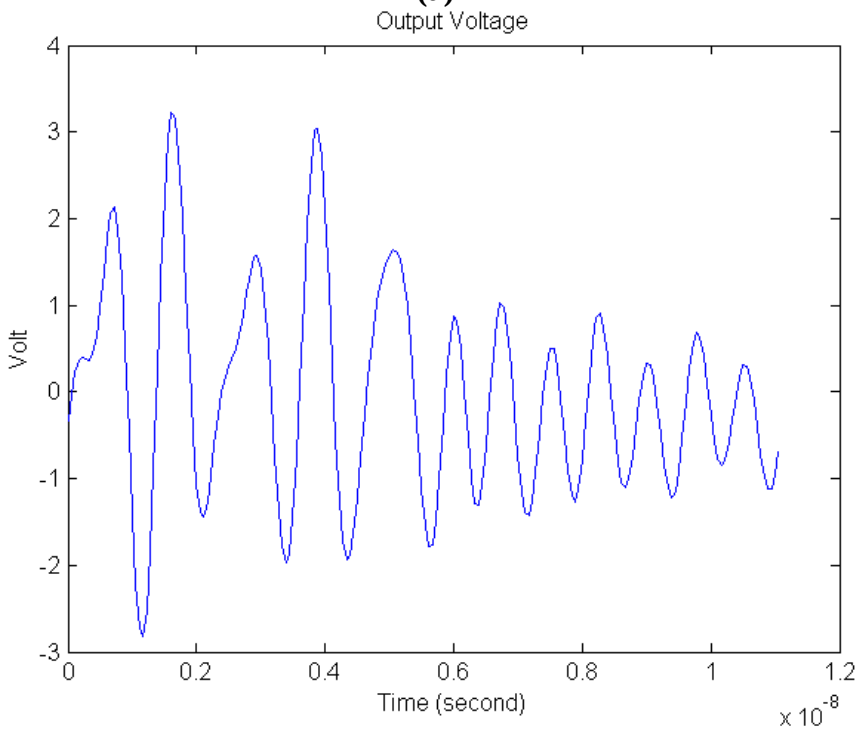


Fig. 2.15. Impedance of pager plane.

To compute the transient response, a one ampere current source (peak to peak) was injected at Port 2 which consists of 5 sinusoid waveforms with period of 1.111 ns, which represents a 900 MHz source signal, as shown in Fig. 2.16 (a). The transient response is shown in Fig. 2.16 (b) where the response continues even after the source is switched off, indicating the high quality factor of the plane cavity.



(a)



(b)

Fig. 2.16. Transient response of pager plane: (a) current source at Port 2 and (b) voltage output at Port 1.

2.6 CPU Time Comparison

The frequency range and run time of the plane model depend on the number of cells. As the number of cells increases, the frequency range and run time increase. Table 2.1 compares the run time between SPICE and the transmission matrix method. The transmission matrix method was simulated in MATLAB using 300 sampling points on a Sun Ultra 30 computer. From Table 2.1, a speed-up in the range 7X-13X can be obtained by using the transmission matrix method to solve the circuit equations. In addition, the transmission matrix method enables large memory savings which enable the extension of the method to a third dimension for analyzing multi-layered structures, as discussed in later chapters.

Table 2.1

CPU Time

Method	Shape of Geometry	Grid Size (Inch)	the Number of Cells	Run Time (Second)	Matrix Size
Spice	Rectangular	0.1" by 0.1"	625	233.58	5928 X 5928
	L-shape	0.2" by 0.2"	302	78.57	2979 X 2979
Transmission Matrix	Rectangular	0.1" by 0.1"	625	18.43	56 X 56
	L-shape	0.2" by 0.2"	302	10.12	32 X 32

2.7 Summary

In this chapter, the transmission matrix method has been developed to compute the impedance matrix at specific ports of interests on a power/ground plane pair. The method was applied to realistic power distribution networks, containing arbitrary shaped geometries. The transmission matrix method showed good correlation with SPICE, analytical solution and measurements.

It was shown that the transmission matrix method is computationally more efficient than SPICE, which is commonly used for most power distribution system analysis. Compared with SPICE, the method leads to small memory requirements and large savings in computer run time. In this chapter, the application of the transmission matrix method for two test cases resulted in a speed-up in the range 7X-13X over SPICE. It is believed that a larger speed-up can be obtained as the number of unit cells increase.

CHAPTER 3

Modeling of Multi-Layered Planes

In this chapter, the transmission matrix method has been extended to a third dimension, which is made up of two-dimensional plane pairs connected in parallel by vertical vias. In addition, vias have been included in the method. Using the via inductance extraction program FastHenry[54], which was developed at Massachusetts Institute of Technology (MIT), self and mutual inductances for power/ground via pairs have been extracted and added to the transmission matrix method. This chapter discusses the use of the transmission matrix method with Π model unit cells for analyzing multi-layered power distribution planes. However, each individual square matrix is based on a pair of power/ground planes while it was based on a column of unit cells for a power/ground plane pair in [26], [27], [35]. For computing the transient core switching noise, the impedance matrix obtained by the transmission matrix method has been converted to the time domain response using an Inverse Discrete Fourier Transform (IDFT) and convolution.

3.1 Power/Ground Planes

Fig. 3.1 shows the structure of multi-layered power distribution planes, which are commonly used in computer applications. Each two-dimensional plane pair is connected through vertical vias. As shown in Fig. 3.1, using a distributed network of RLCG elements, each rectangular plane pair can be divided into $(M-1)\times(N-1)$ unit cells.

The $(M-1)\times(N-1)$ unit cells can be represented as a $2(M\times N)\times 2(M\times N)$ matrix formed by $(M\times N)$ input ports and $(M\times N)$ output ports. This is shown in Fig. 3.2 for the Π equivalent circuits for the unit cells, which are cascaded to represent a pair of power/ground planes shown in Fig. 2.1 (b).

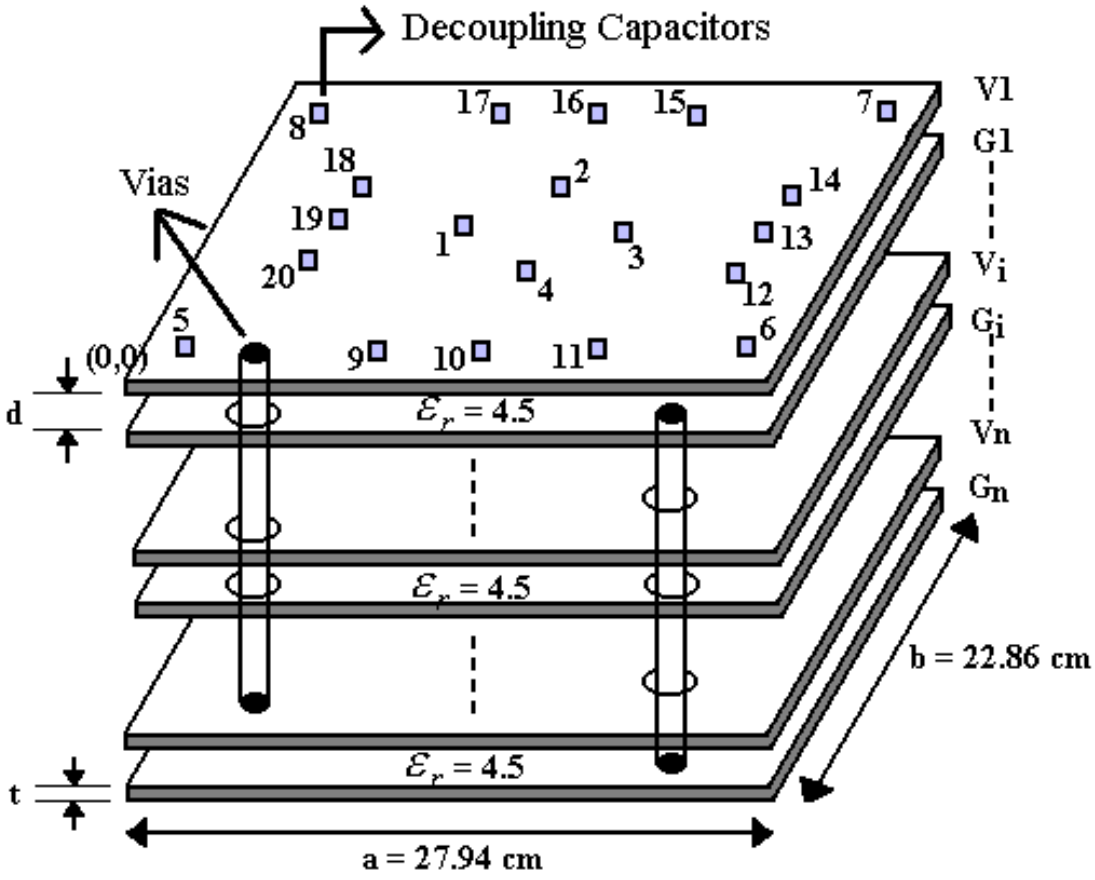


Fig. 3.1. Multi-layered power/ground plane structure.

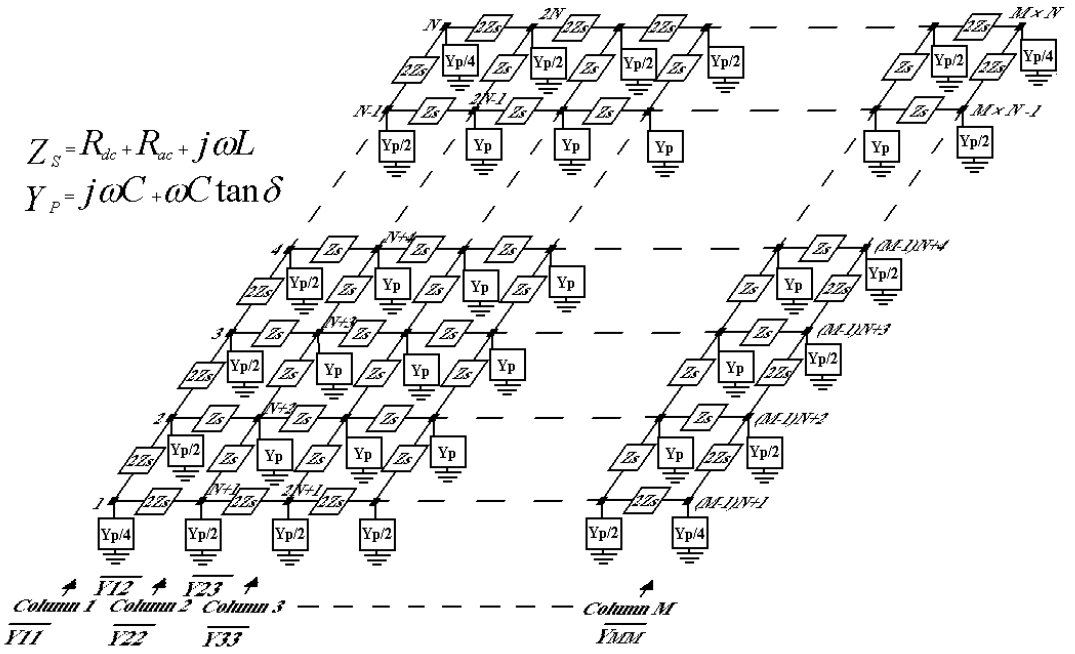


Fig. 3.2. Equivalent circuit for a pair of power/ground planes.

From Fig. 3.2, the input ports are indexed as 1 to $(M \times N)$, and the output ports are indexed as $(M \times N)+1$ to $2(M \times N)$. The transmission matrix for the $2(M \times N)$ port network can be derived in terms of the node voltages and port currents. Using the 2×2 block matrix representation, the transmission matrix can be represented to relate the voltages and currents as:

$$\begin{aligned} \overline{V_{in}} &= [A_p]\overline{V_{out}} + [B_p]\overline{I_{out}} \\ \overline{I_{in}} &= [C_p]\overline{V_{out}} + [D_p]\overline{I_{out}} \end{aligned} \tag{3.1}$$

$$\text{where } \overline{V_{in}} = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_{M\times N} \end{bmatrix} \overline{I_{in}} = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{M\times N} \end{bmatrix} \overline{V_{out}} = \begin{bmatrix} V_{M\times N+1} \\ V_{M\times N+2} \\ \vdots \\ V_{2(M\times N)} \end{bmatrix} \overline{I_{out}} = \begin{bmatrix} I_{M\times N+1} \\ I_{M\times N+2} \\ \vdots \\ I_{2(M\times N)} \end{bmatrix}.$$

The above transmission matrix for a power/ground plane pair can be rewritten in the simpler form:

$$T_p = \begin{bmatrix} A_p & B_p \\ C_p & D_p \end{bmatrix} = \begin{bmatrix} I & 0 \\ C_p & I \end{bmatrix} \tag{3.2}$$

where $[I]$ is the identity matrix, $[0]$ is the null matrix, and $[C_p]$ represents $(M \times N) \times (M \times N)$ matrices. In Eq. (3.2), the matrix $[C_p]$ is of the form

$$[C_p] = \begin{bmatrix} \bar{Y}_{11} & -\bar{Y}_{12} & 0 & 0 & \cdots \\ -\bar{Y}_{12} & \bar{Y}_{22} & -\bar{Y}_{23} & 0 & \cdots \\ 0 & -\bar{Y}_{23} & \bar{Y}_{33} & -\bar{Y}_{34} & \cdots \\ \vdots & \vdots & \vdots & \vdots & \cdots \\ 0 & 0 & 0 & 0 & \cdots \bar{Y}_{MM} \end{bmatrix} \tag{3.2A}$$

where $\bar{Y}_{11} = \bar{Y}_{MM} = 0.5\bar{Y}_{22} = 0.5\bar{Y}_{33} = \cdots\cdots = 0.5\bar{Y}_{(M-1)(M-1)} =$

$$\begin{bmatrix} \frac{Y_p}{4} + \frac{1}{Z_s} & -\frac{1}{2Z_s} & 0 & \cdots & 0 & 0 \\ -\frac{1}{2Z_s} & \frac{Y_p}{2} + \frac{2}{Z_s} & -\frac{1}{2Z_s} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \ddots & \vdots \\ 0 & 0 & \cdots & \ddots & \frac{Y_p}{2} + \frac{2}{Z_s} & -\frac{1}{2Z_s} \\ 0 & 0 & \cdots & & -\frac{1}{2Z_s} & \frac{Y_p}{4} + \frac{1}{Z_s} \end{bmatrix}$$

$$\bar{Y}_{12} = \bar{Y}_{23} = \cdots\cdots = \bar{Y}_{(M-1)M} =$$

$$\begin{bmatrix} \frac{1}{2Z_s} & & & & 0 \\ & \frac{1}{Z_s} & & & \\ & & \ddots & & \\ & & & \frac{1}{Z_s} & \\ 0 & & & & \frac{1}{2Z_s} \end{bmatrix}.$$

As can be seen in Eq. (3.2A), the transmission matrix for a power/ground plane pair is tri-diagonal and sparse, which enables a reduction in memory usage and CPU run time when applied to realistic structures. The use of repeated unit cells enables the propagation of electromagnetic (EM) waves between the planes [17].

3.2 Vias and Via Coupling

Multi-layered power distribution structures can be represented as power/ground plane pairs connected by vias. In a realistic structure, there are thousands of via connections for reducing the via inductances and for thermal dissipation. For high clock rates, these effects have to be included for computing the response in the high frequency range. Fig. 3.3 shows the side view of three conductor planes, which can be separated into two pairs of power/ground planes. The voltage planes PL1 and PL3 are connected together through vias for maintaining the same potential. It is assumed here that there are $(M \times N)$ power/ground via pairs, which can be decomposed into self and mutual inductances as shown in Fig. 3.3.

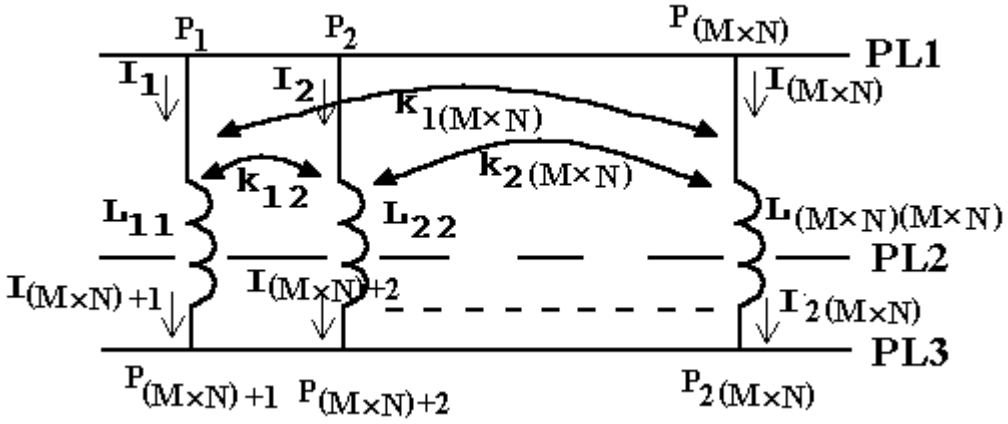


Fig. 3.3. Side view of power/ground planes with vias.

In terms of PL1 and PL3 conductor planes, the voltage and current between point P_1 and $P_{(M\times N)+1}$, shown in Fig. 3.3, can be represented as follows:

$$\begin{aligned} V_{p_1 p_{(M\times N)+1}} &= jwL_{11}I_1 + jwM_{12}I_2 + \cdots + jwM_{1(M\times N)}I_{(M\times N)} \\ I_1 &= I_{(M\times N)+1} \end{aligned} \tag{3.3}$$

where mutual inductance $M_{ij} = k_{ij}\sqrt{L_{ii}L_{jj}}$. Other node voltages and port currents follow Eq. (3.3). In Eq. (3.3), the inductances of the vias represent loop inductances for each power/ground via pair.

Since mutual inductance can couple energy instantaneously between spatially separated points, the use of Eq. (3.3) can violate causality in the time domain. Hence, Eq. (3.3) is in direct contradiction to the modeling technique used for power/ground planes where an electromagnetic wave takes finite time to travel between spatially separated points. To ensure causality, the currents for mutual inductances (I_2, $I_{3,}\cdots$, $I_{(M\times N)}$) shown in Eq. (3.3) are not excited until the EM wave reaches the via location. Hence, since the currents are causal, Eq. (3.3) preserves causality. This method has been used in Chapter 5.2 to generate a causal solution.

From Eq. (3.3), the self and mutual inductances can be included in the transmission matrices of the vias based on the current direction in Eq. (3.3). The FastHenry extraction program from MIT provides losses, inductances, and polarity. The extracted real (loss) and imaginary (inductance) impedance values are frequency dependant. As an approximation, frequency independent values have been used in this thesis. These have been derived using two frequency data samples; namely, a low-frequency sample and a

high-frequency sample. Since inductance values are dominant in the high frequency range, the high frequency inductances are used over the entire frequency band. The loss (real) term for the via has been approximated as $(R_{dc} + R_{ac}\sqrt{f})$ which represents a skin effect approximation. From the two real parts of the data, the two unknown variables can be found and represented using the equation:

$$R_{dc} = \frac{D_1\sqrt{f_2} - D_2\sqrt{f_1}}{\sqrt{f_2} - \sqrt{f_1}}$$
$$R_{ac} = \frac{D_2 - D_1}{\sqrt{f_2} - \sqrt{f_1}} \tag{3.4}$$

where D_1 and D_2 are the real values of data at frequencies f_1 and f_2, respectively. From these values, the transmission matrix for vias in terms of input ports on PL1 and PL2, and output ports on PL3 and PL2 planes can be represented as follows:

$$[T_{via}] = \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix} \tag{3.5}$$

$$\text{where } [B_{via}] = \begin{bmatrix} Z_{via,11} & Z_{via,12} & Z_{via,13} & \cdots & Z_{via,1(M\times N)} \\ Z_{via,12} & Z_{via,22} & Z_{via,23} & \cdots & Z_{via,2(M\times N)} \\ Z_{via,13} & Z_{via,23} & Z_{via,33} & \cdots & Z_{via,3(M\times N)} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ Z_{via,1(M\times N)} & Z_{via,2(M\times N)} & Z_{via,3(M\times N)} & \cdots & Z_{via(M\times N)(M\times N)} \end{bmatrix}.$$

In Eq. (3.5), $Z_{via,ij} = R_{dc,ij} + R_{ac,ij}\sqrt{f} + jwL_{ij}$. As seen in Eq. (3.5), the transmission matrix loses the sparsity as the number of via pairs increases. To maintain sparsity, the

negligible coupling coefficients (k_{ij}) in Eq. (3.5) can be neglected during matrix computation.

3.3 Impedance Computation

The $2(M \times N) \times 2(M \times N)$ transmission matrix for the overall power distribution network, which consists of a cascade of two or more networks, can now be obtained by multiplying the individual matrices [26], [27], [35]. For the rectangular multi-layered planes in Fig. 3.1, since all the matrices for planes, vias, and decoupling capacitors have the same size, the response of the entire geometry can be obtained as a single $2(M \times N) \times 2(M \times N)$ matrix. The block representation of the cascade connection of $2(M \times N)$ port networks is shown in Fig. 2.4 using the [T] matrix representation. As seen in Fig. 2.4, the entire system can be simplified into 3 blocks in terms of input and output ports, which have input voltage and current variables, and output voltage and current variables, respectively. The transmission matrix for the block diagrams in Fig. 2.4 can be represented as follows:

$$
\begin{aligned}
&[T_l] = \begin{bmatrix} A_l & B_l \\ C_l & D_l \end{bmatrix} = \\
&\begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_l \times \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{1,2} \times \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_2 \times \cdots \times \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_l \times \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{l,l+1} \\
&[T_m] = \begin{bmatrix} A_m & B_m \\ C_m & D_m \end{bmatrix} = \\
&\begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_{l+1} \times \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{l+1,l+2} \times \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_{l+2} \times \cdots \times \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_{l+m} \\
&[T_n] = \begin{bmatrix} A_n & B_n \\ C_n & D_n \end{bmatrix} = \\
&\begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{l+m,l+m+1} \times \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_{l+m+1} \times \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{l+m+1,l+m+2} \times \cdots \times \begin{bmatrix} I & 0 \\ C_p + C_{cap} & I \end{bmatrix}_{l+m+n}
\end{aligned}
\tag{3.6}
$$

where l, m, and n represent the number of power/ground plane pairs, and C_{cap} is a matrix for decoupling capacitors shown in Eq. (2.12). From Fig. 2.5, two inversions of a $2(M \times N) \times 2(M \times N)$ matrix are needed to obtain the overall transmission matrix, and one inversion of a matrix is needed to convert to the $2(M \times N) \times 2(M \times N)$ impedance matrix [Z] of the network [26], [27]. However, since most of the computational time is taken to invert a matrix, the number of matrix inversions needs to be minimized. Using one inversion of a matrix, which is the overall 'C' matrix computed by multiplications of the transmission matrix from Plane 1 to Plane (l+m+n), it is possible to convert to the impedance matrix in Eq. (3.6). The overall $2(M \times N) \times 2(M \times N)$ impedance matrix for the multiple input and output ports can be computed as follows:

$$\begin{aligned} &[Z_A] = R_n \times C_{inv} \times D_l \quad [Z_D] = A_n \times C_{inv} \times R_l \\ &[Z_B] = [Z_C] = A_n \times C_{inv} \times D_l \\ &\textit{where} \quad C_{inv} = \left(\begin{bmatrix} C_l & D_l \end{bmatrix} \times \begin{bmatrix} A_m & B_m \\ C_m & D_m \end{bmatrix} \times \begin{bmatrix} A_n \\ C_n \end{bmatrix} \right)^{-1} \\ &\qquad R_n = A_m \times A_n + B_m \times C_n \quad R_l = C_l \times B_m + D_l \times D_m \,. \end{aligned} \tag{3.7}$$

During the design of the power delivery system, the impedance at specific points on the network is often desired. This can either be the self impedance at a port or the transfer impedance between ports. This can reduce about half the computations during the matrix multiplications, requiring only the 'C' full matrix, the rows of R_n and A_n, and the columns of R_l and D_l at the specific points.

3.4 Transient Response

Using an Inverse Discrete Fourier Transform (IDFT) and convolution, the transient response of the power distribution network can be generated from the frequency domain data. Once the impedances in the frequency domain are computed using the transmission matrix method, a spline interpolation technique was applied to the complex data to obtain enough samples for the IDFT. A transfer function ($H(w)$) was then constructed depending on the excitation source and converted to its impulse response ($h(t)$) using the IDFT. Using the property that the output response in the time domain is real, the IDFT equation for computing the impulse response can be represented as [36]:

$$h(t) = T_s F_s \, Re\{ H(0) + 2 \sum_{n=1}^{k} H(2pF_s n) e^{j2pF_s nt} \}_{t=T_s m} \quad ;m=0,1,2,\ldots\ldots \tag{3.8}$$

where T_s is the sampling time and F_s is the sampling frequency. Finally, from the convolution of the two sequences $h(t)$ and $x(t)$ (input source), the output transfer voltage ($v(t)$) can be computed. In the next chapter, a triangular excitation current source was used with a short termination to mimic a transient current generated from the switching circuit.

3.5 Summary

In this chapter, the transmission matrix method has been extended to compute the impedance matrix at specific ports of interests on multi-layered power/ground planes, which is made up of two-dimensional plane pairs connected in parallel by vias. After

extracting via inductance using FastHenry, self and mutual inductances for power/ground via pairs have been added to the transmission matrix method, which should be considered for obtaining accurate modeling results in a high performance system. Compared with Chapter 2, impedance computation in this chapter has been simplified for fast computation. For implementing multi-input sources efficiently, an IDFT and convolution were used. In the next chapter, the method discussed in this chapter is applied to verify the accuracy of the method and to analyze multi-layered planes with via inductance.

CHAPTER 4

Analysis of Multi-Layered Planes

In this chapter, the transmission method discussed in Chapter 3 is applied for analyzing multi-layered rectangular and irregular shaped power distribution planes in the frequency and time domain. The analysis includes the effect of vias on the power distribution network. Using the transmission matrix method, via effects and the effects of multiple rectangular power/ground plane pairs without and with decoupling capacitors have been analyzed for realistic structures. Where applicable, the results have been compared with SPICE, where the cavity resonator model was used for simulation [31], [32]. Multi-layered power/ground planes have also been modeled with via inductances represented as short circuits, with vias as self inductances which are defined as loop inductances for each power/ground via pair, and with vias coupled to each other to demonstrate the differences in the computed results. Using the three types of via connections, the frequency response of multi-layered power/ground plane structures made up of 5, 10, and 15 plane pairs has been compared.

4.1 Comparison of Transmission Matrix Method and Cavity Resonator Method

The test structure consists of five 27.94 cm by 22.86 cm rectangular pairs of power/ground planes, where the conductor planes stack up in the order: V1/G1/V2/G2/V3, with FR4 dielectric with relative permittivity e_r = 4.5, as shown in

Fig. 4.1.While V1/G1, V2/G2, and V3/G2 plane pairs have a 109.22 μm dielectric thickness, V2/G1 and V3/G3 plane pairs have a 337.82 μm dielectric thickness. Fig. 4.1 shows the details of the plane layers. The conductor planes are made of copper (s_c = 5.8×10^7 S/m) with a thickness of 30 μm and dielectric loss tangent $tan(d)$ = 0.02 at 1 GHz. An excitation point (Port 1) was located at (x = 13.8 cm, y = 11.25 cm) and an observation point (Port 2) at (x = 2 cm, y = 2 cm) between V1 and G1 planes. Three kinds of 32 decoupling capacitors (C = 47 nF, ESL = 1 nH, ESR = 0.1 Ω; C = 10 nF, ESL = 1 nH, ESR = 0.1 Ω; and C = 20 μF, ESL = 10 nH, ESR = 0.1 Ω), with locations as shown by the rectangular dots in Fig. 4.1, were incorporated between V1 and G1 planes. Twenty vias, which have the same locations as the decoupling capacitors, were vertically connected from power plane to power plane and from ground plane to ground plane. This ensures that the voltage planes and ground planes are at the same potential.

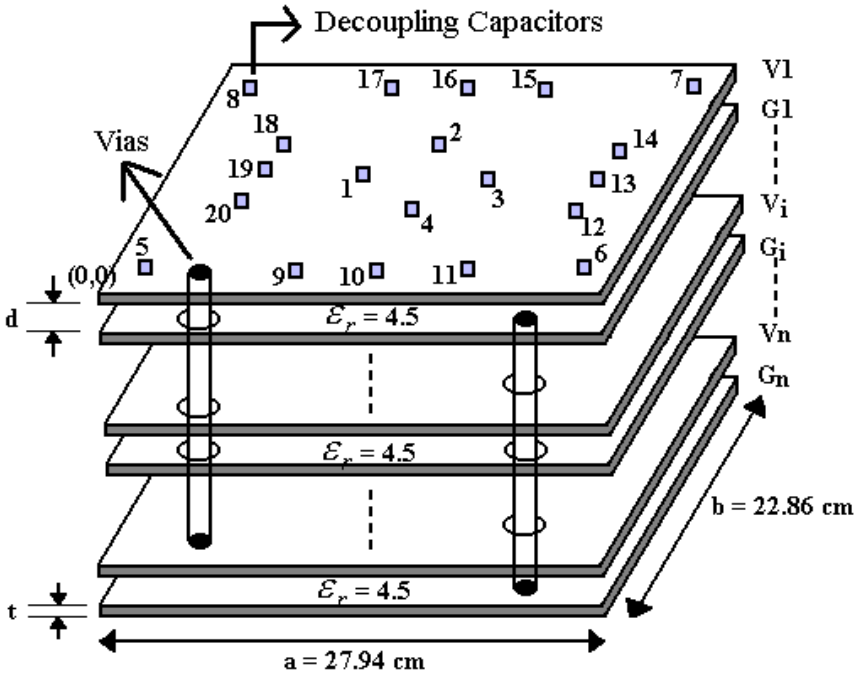


Fig. 4.1. Multi-layered power/ground plane structure.

To check the accuracy of the transmission matrix method, the results have been compared with the cavity resonator model [31], [32] for the structure shown in Fig. 4.1. Fig. 4.2 shows the transfer impedance between Port 1 and Port 2. In this section, via inductances were not included. Each plane pair was connected by a small value of resistor ($1\,mW$), so that the resistors can mimic a short circuit. For comparison, the propagating modes were set to m = 6, and n = 5 in the cavity resonator model described in [31], [32]. As shown in Fig. 4.2, both the methods show good agreement over a frequency range of 1 GHz.

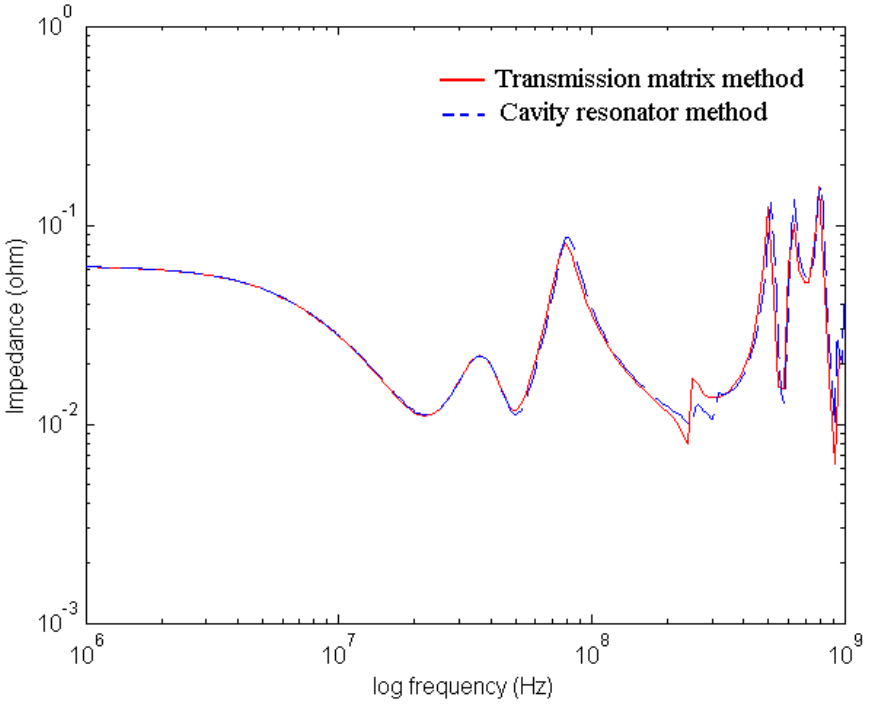


Fig. 4.2. Impedance without via effects.

4.2 Effect of Multi-Layered Power/Ground Planes with Vias

Vias are a common type of discontinuity in multi-layered power distribution networks which can contain thousands of via connections. To accurately model such multi-layered

structures, it is necessary to consider via effects as the frequency bandwidth of the PDS increases. Since vias can be represented as inductances, the impedance of the PDS is affected in the high frequency range and the null resonant frequencies of the PDS are shifted to lower frequencies. To quantify the effect of multi-layered power distribution planes with vias, three cases were compared for the multi-layered network made up of 5, 10, and 15 pairs of planes. The three test cases are 1) vias represented as short circuits, 2) vias represented as self inductances, and 3) vias represented as self and mutual inductances.

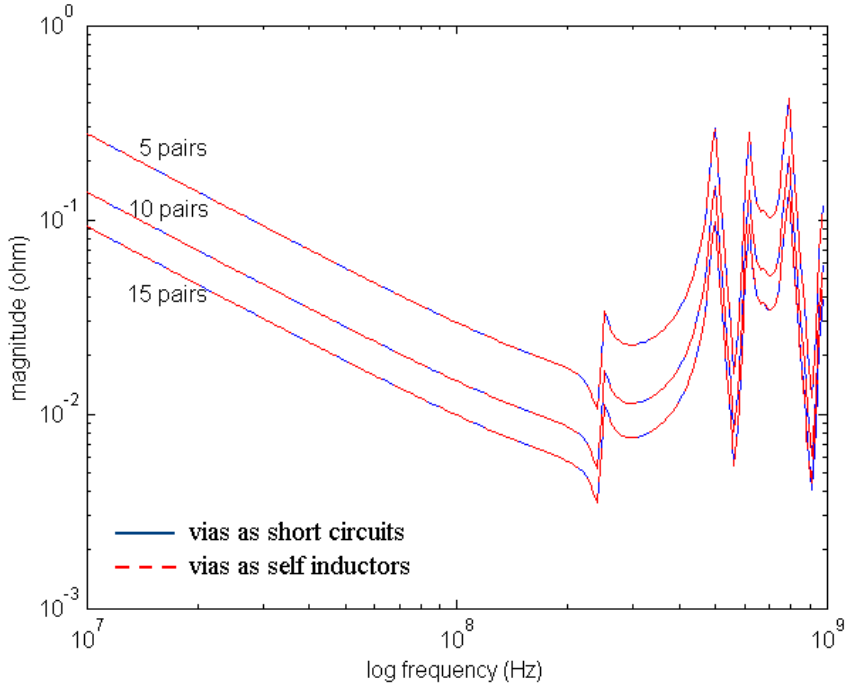
Fig. 4.1 shows the cross section of 'n' multi-layered power distribution planes. Each two-dimensional plane pair is connected through vertical vias. The test structure consists of 5, 10, and 15 rectangular pairs of power/ground planes with a 223.56-μm thick FR4 dielectric with relative permittivity e_r = 4.5. The conductor planes were made of copper ($s_c = 5.8\times10^7$ S/m) with a thickness of 30 μm and dielectric loss tangent $tan(d)$ = 0.02 at 1 GHz. Using a unit cell size of 7.62 mm by 7.62 mm, the PDS was divided into 37×30 unit cells, which resulted in a matrix size of 2356×2356 for each individual square transmission matrix. An excitation point (Port 1) was located at (x = 0 cm, y = 0 cm) and an observation point (Port 2) at (x = 13.94 cm, y = 11.43 cm) between V1 and G1 planes (top plane pair) for 5, 10, and 15 plane pairs. Decoupling capacitors with values described in the previous section with locations as shown by the rectangular dots in Fig. 4.1 were incorporated between the V1 and G1 planes. For analysis, the test structure was simulated using two different scenarios for via connections; namely uniformly distributed via connections and randomly distributed via connections. While vias were connected to each plane at every unit cell (7.62 mm) position for uniformly

distributed via connections (1178 vias), vias were only connected to each plane at the decoupling capacitor locations shown in Fig. 4.1 for randomly distributed via connections (20 vias). Using the via inductance extraction program FastHenry, self (~ 0.11 nH) and mutual inductances between vias were extracted and incorporated into the transmission matrix. Since coupling coefficients between the vertical layers were small, they were neglected in the computation.

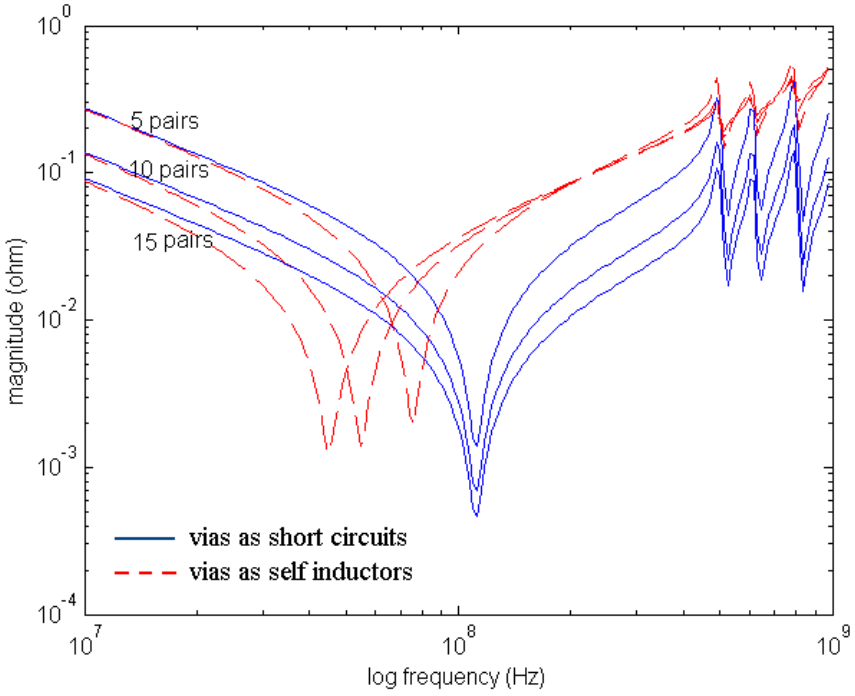
Fig. 4.3 shows the simulated impedances without decoupling capacitors for 5, 10, and 15 pairs, in which the vias were modeled as short circuits and as self inductances at every unit cell position (1178 vias). In the case of the via connections modeled as short circuits, when all the plane pairs have the same dimensions (a and b) with no decoupling capacitors, all the plane resonant frequencies (peak and null) remained unchanged, but the impedance magnitudes changed according to the number of plane pairs. This is due to the additional capacitance of the plane layers. However, the frequency response of the self impedance changed with the via self inductances, as shown in Fig. 4.3 (b). As the number of plane pairs increased, the null resonant frequencies shifted to lower frequencies while the peak resonant frequencies remained the same. In addition, the impedance magnitudes were closer to each other after the first null resonant frequency. This change is caused by the increased capacitance between the planes, which is proportional to the number of plane pairs. Hence, the low-frequency impedances were reduced, but the high-frequency impedances were not changed significantly as the number of plane pairs was increased. The effect of via inductance becomes prominent at high frequencies. For the transfer impedance, the resonant frequencies and magnitudes with via inductance connections were similar to those with short circuit connections, as

shown in Fig. 4.3 (a). This means that the transfer impedances on the same layer are not changed due to the presence of via inductances.

Fig. 4.4 shows the simulated impedances without and with decoupling capacitors for each structure, in which vias were modeled as short circuits, self inductances, and self and mutual inductances for 10 pairs of planes. In this simulation, the vias were randomly distributed (20 vias). As shown in Fig. 4.4, the null resonant frequencies and magnitudes of all self and transfer impedances are affected in all three cases (even in the case of short circuit connections which have the same null resonant frequencies for 5, 10, and 15 planes, as shown in Fig. 4.3) as the frequency increases. While multi-layered power/ground planes with via inductances have the same peak resonant frequencies of the planes without via inductances, they have additional resonant frequencies since the via inductances are coupled with the capacitances of the planes. However, if vias are modeled as short circuits, the additional resonant frequencies cannot be seen. As the number of planes with the via connections is increased, the frequency response can be affected by the vias at high frequencies even though the low-frequency impedances are reduced. The impedance magnitude with self and mutual inductances is close to the magnitude with stand-alone self inductances, but the additional resonant frequencies shift to lower frequencies due to the additional mutual inductances. Depending on the separation and number of vias, the coupling coefficients between power/ground via pairs can be secondary effects to the PDS. As the decoupling capacitors mentioned above are incorporated, the low-frequency impedances and the magnitude of the peak resonant frequencies are reduced, as shown Fig. 4.4 (b). However, the inductances in the high frequency range are close to those without decoupling capacitors.

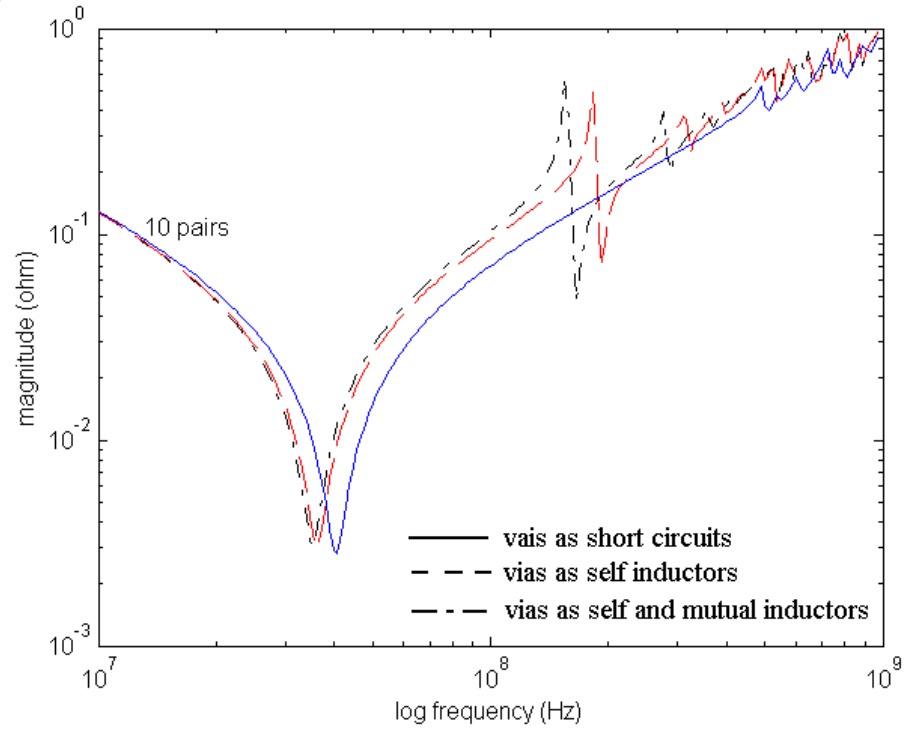


(a)

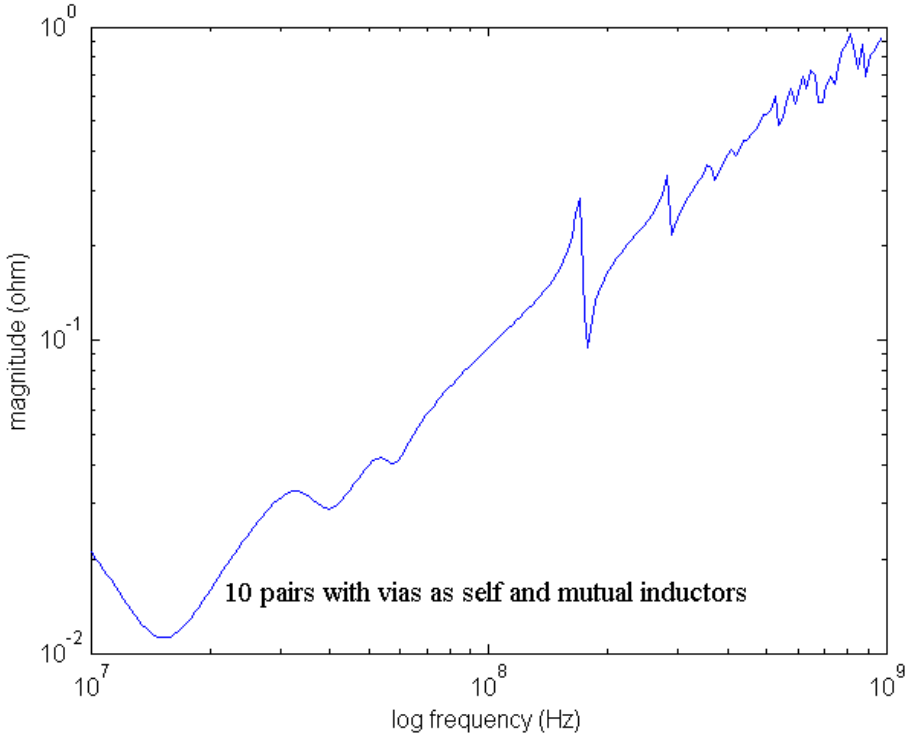


(b)

Fig. 4.3. Impedance magnitude without decoupling capacitors with vias connected at every unit cell position: (a) transfer impedance and (b) self impedance at Port 2.



(a)



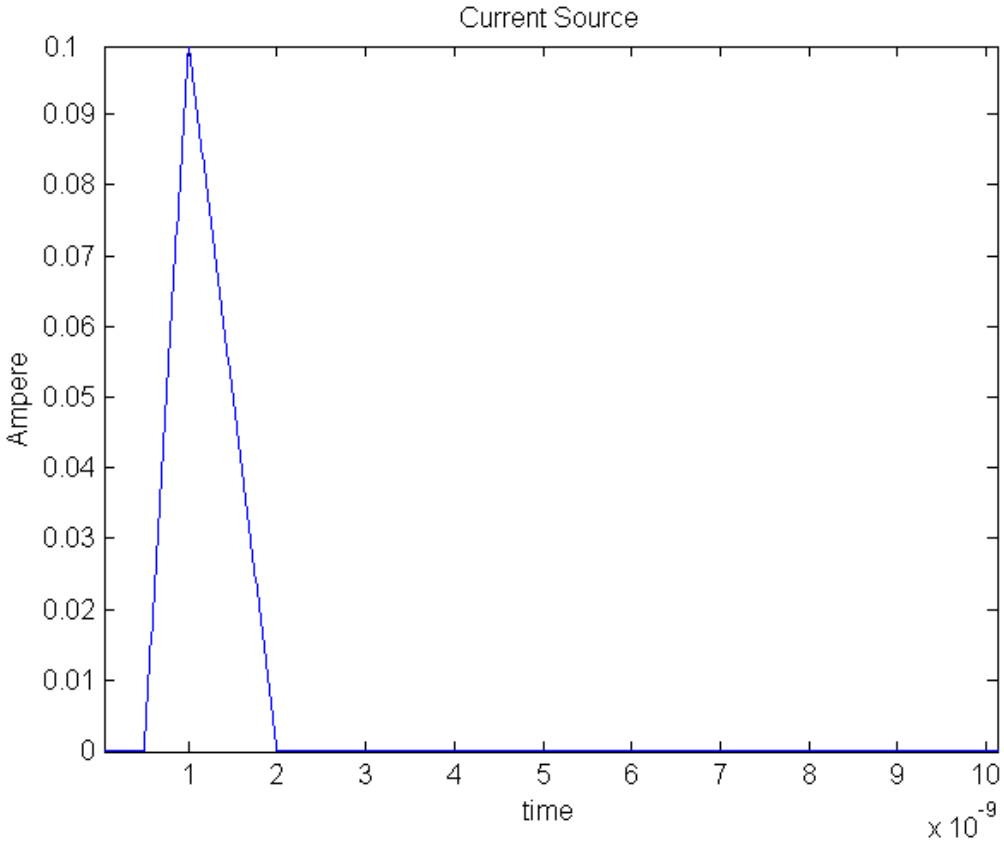
(b)

Fig. 4.4. Impedance magnitude without and with decoupling capacitors with vias randomly connected: (a) self impedance without decoupling capacitors at Port 2 and (b) self impedance with decoupling capacitors at Port 2.

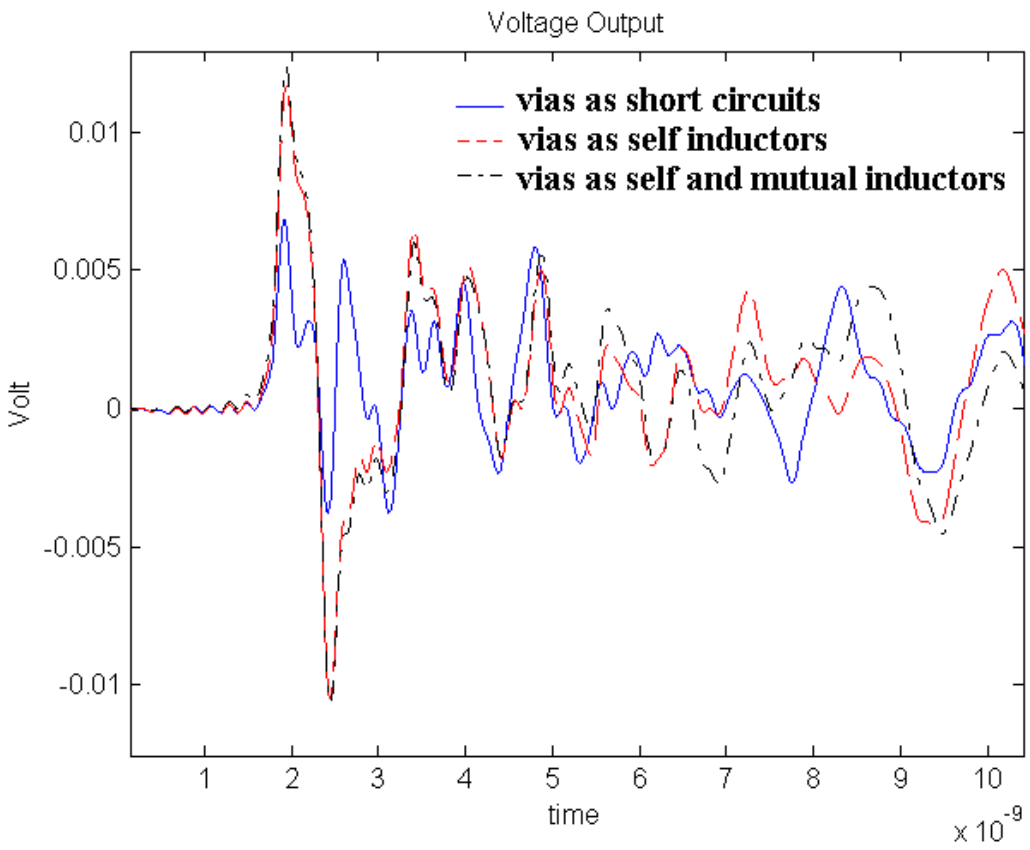
Based on the results in Figs. 4.3 and 4.4, for the analysis of multi-layered plane pairs with vias, several issues have to be considered such as: a) the inductance and number of the vias in parallel connecting the planes, b) the separation between the vias and port locations at which the impedance is desired, and c) the interaction between vias and plane capacitances. Based on the comparison between the self impedances at Port 2 in Figs. 4.3 and 4.4, the inductance of the plane pairs is reduced as the number of vias is increased. Since vias are connected in parallel, the via inductance is reduced as the number of vias increases. This results in a reduction in the plane impedance with the additional resonant frequencies, which are caused by the coupling between the via inductances and the plane capacitances, that occur at higher frequencies.

To evaluate the noise due to the via inductances, the transient response for the 5 plane pairs with the randomly distributed via connections (20 vias) were compared for the three cases described earlier in the time domain. The transient output voltages were generated from the frequency impedance data from 0 Hz to 5 GHz. With a short termination at (x = 27.94 cm, y = 22.86 cm) between V3 and G3 planes (bottom plane pair), a 0.1 ampere triangular current source with open source resistance was used to mimic a transient current generated from a switching circuit. The current source had a rise time of 500 ps and fall time of 1 ns, and sampled up to 100 ns using a sampling interval of 10 ps, as shown in Fig. 4.5 (a). The transient output voltage for the three cases is shown in Fig. 4.5 (b), where the voltage fluctuations continue even after the source is switched off, indicating the high quality factor of the plane cavity. As a comparison, vias modeled as inductances generate about twice as much peak noise as compared to vias modeled as short circuits. However, the responses for the two cases viz., vias modeled as self

inductors and vias modeled as self and mutual inductors, are close to each other. In addition, the transient output voltage begins after a delay which is caused by the physical separation between the ports. The delay time of ~ 1.1 ns for the three cases is the same, indicating that causality of the system is preserved for all three cases, as described in Chapter 3.



(a)



(b)

Fig. 4.5. Transient response of 5 plane pairs with the randomly distributed via connections (20 vias): (a) current source at Port 1 and (b) voltage output at Port 2.

4.3 Efficiency of Transmission Matrix Method

As mentioned in Chapter 2, the transmission matrix method enables memory saving and reduction in computation time. The memory required and computational time between SPICE and the transmission matrix method have been compared in Table 4.1 for 5, 10, 15 plane pairs with randomly distributed via connections, where vias were modeled as self and mutual inductances. On an average, the transmission matrix method requires less than 1 % of the memory required by SPICE. All the impedances between the two ports (Z11, Z12, and Z22) were simulated with 200 frequency-sampling points in

MATLAB, and the CPU run time is shown in Table 4.1. Since the transmission matrix method retains the same matrix size, the CPU time is almost linear for each additional plane pair. Most of the computational time is required to invert a matrix, as mentioned in Chapter 3.3. Hence, the smaller the matrix, the smaller the computation time. As shown in Table 4.1, the small size of the transmission matrix leads to savings in CPU time.

Table 4.1

Matrix Size and CPU Run Time Comparison

Number of Unit Cells	Parameter	Spice (MNA)	Transmission Matrix Method	Matrix Size comparison CPU: (without, with decaps)
	Elements	57,520	57,520	
37 X 30 X 5	Nodes	40,195	5,890	0.1380%
	Matrix size	63,410 X 63410	2,356 X 2,356	(483 s, 538 s)
	Elements	115,040	115,040	
37 X 30 X 10	Nodes	80,390	11,780	0.0345%
	Matrix Size	126,820 X 126,820	2,356 X 2,356	(967 s, 1069 s)
	Elements	172,560	172,560	
37 X 30 X 15	Nodes	120,585	23,560	0.0153%
	Matrix Size	190,230 X 190,230	2,356 X 2,356	(1417 s, 1622 s)

4.4 Application of Transmission Matrix Method for Multi-Layered Irregular Shaped Planes

The transmission matrix method was next applied to a multi-layered irregular shaped plane structure shown in Fig. 4.6. The aim of this analysis was to demonstrate that the transmission matrix method can be applied to multi-layered arbitrary shaped power/ground planes that are typical in a number of applications.

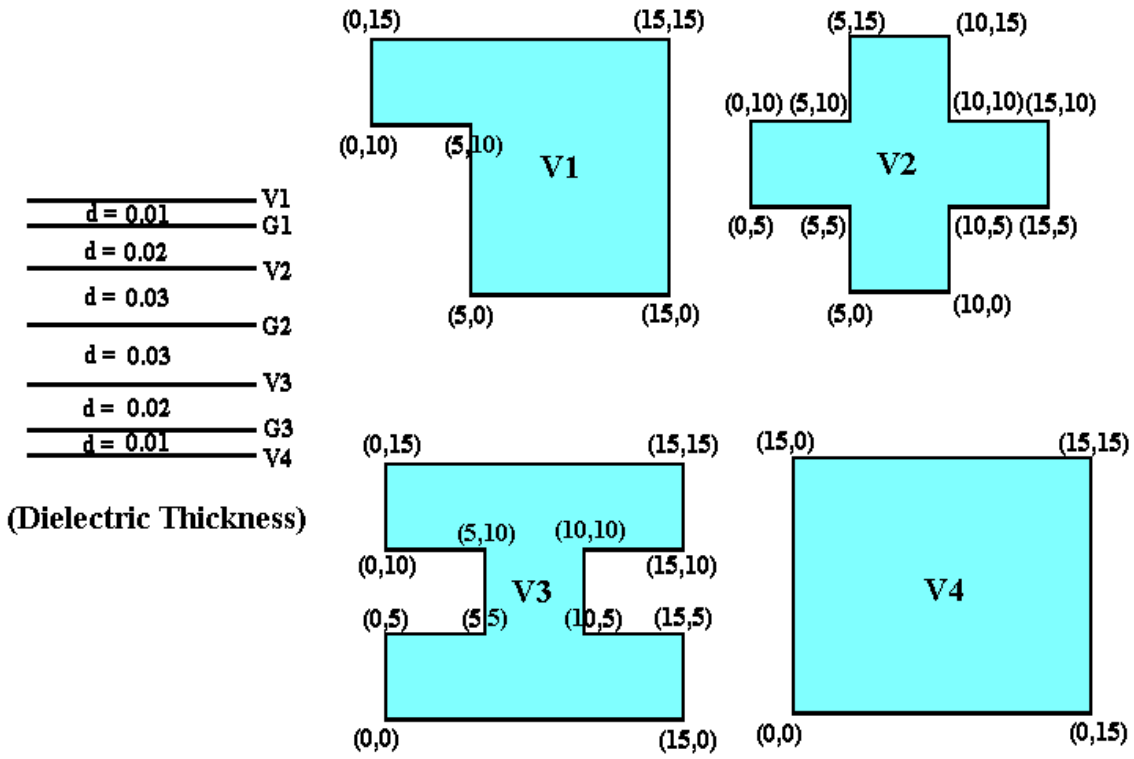


Fig. 4.6. Multi-layered irregular shaped power/ground planes.

The structure consisted of 7 layers that were modeled as 6 power/ground plane pairs using a unit cell size of 5 mm by 5 mm. Each power/ground plane was connected in parallel using a 1 μΩ resistor to mimic vias modeled as short circuits. The positions of the vias were at every 5 mm interval from x = 5 cm to x=10 cm and from y = 5 cm to y =10 cm using a co-ordinate system with the origin as defined in Fig. 4.6. All ground planes were assumed to have the same rectangular shape as the V4 plane. Each plane pair had a different dielectric thickness, as shown in Fig. 4.6, with relative permittivity $e_r = 4$ and dielectric loss tangent $tan(d) = 0.02$ at 1 GHz. The conductor planes were made of copper with a thickness of 30 μm. An excitation point (Port 1) was defined at (x = 5 cm, y = 5 cm) on V4 - G3 plane pair and an observation point (Port 2) at (x = 9 cm, y = 9 cm)

on V1 – G1 plane pair. The impedance magnitudes between the two ports are shown in Fig. 4.7. Due to many boundaries in the structure, the resonant frequencies in a multi-layered irregular shaped plane structure occur at more frequencies than in a multi-layered rectangular plane structure.

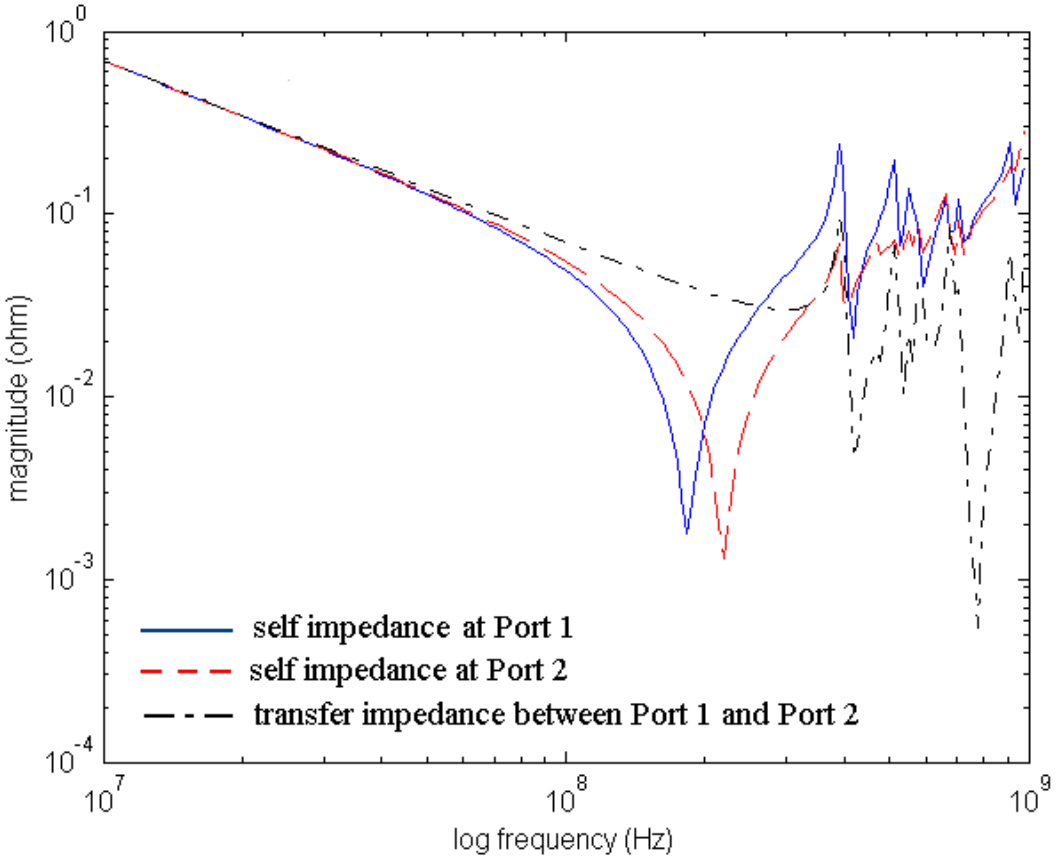
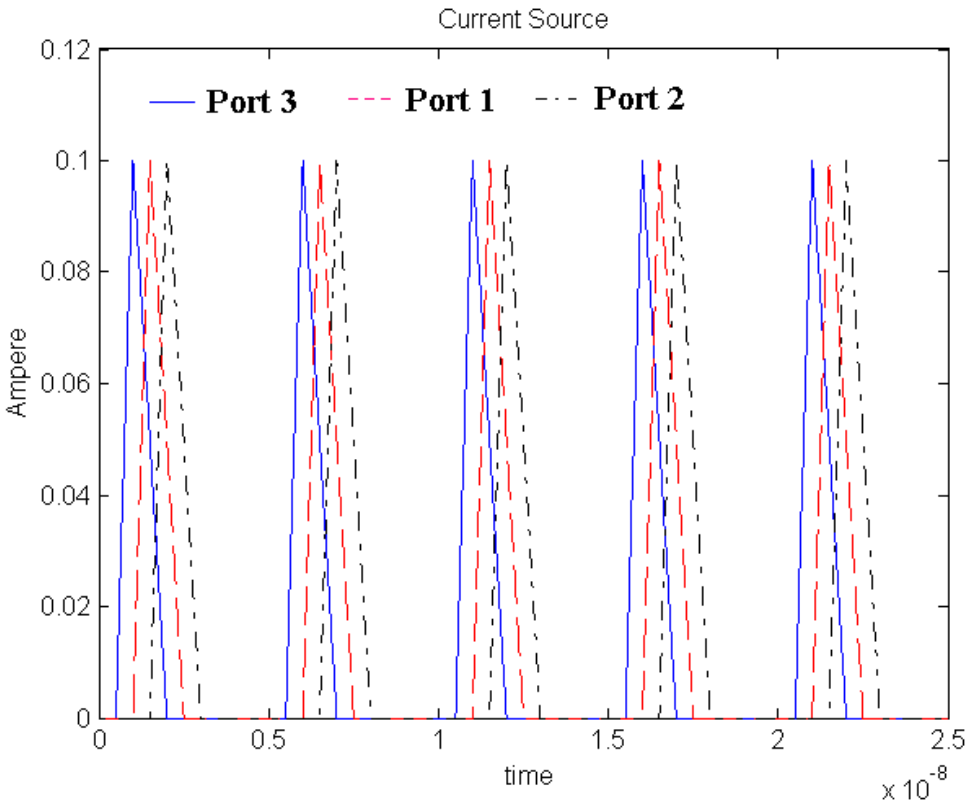


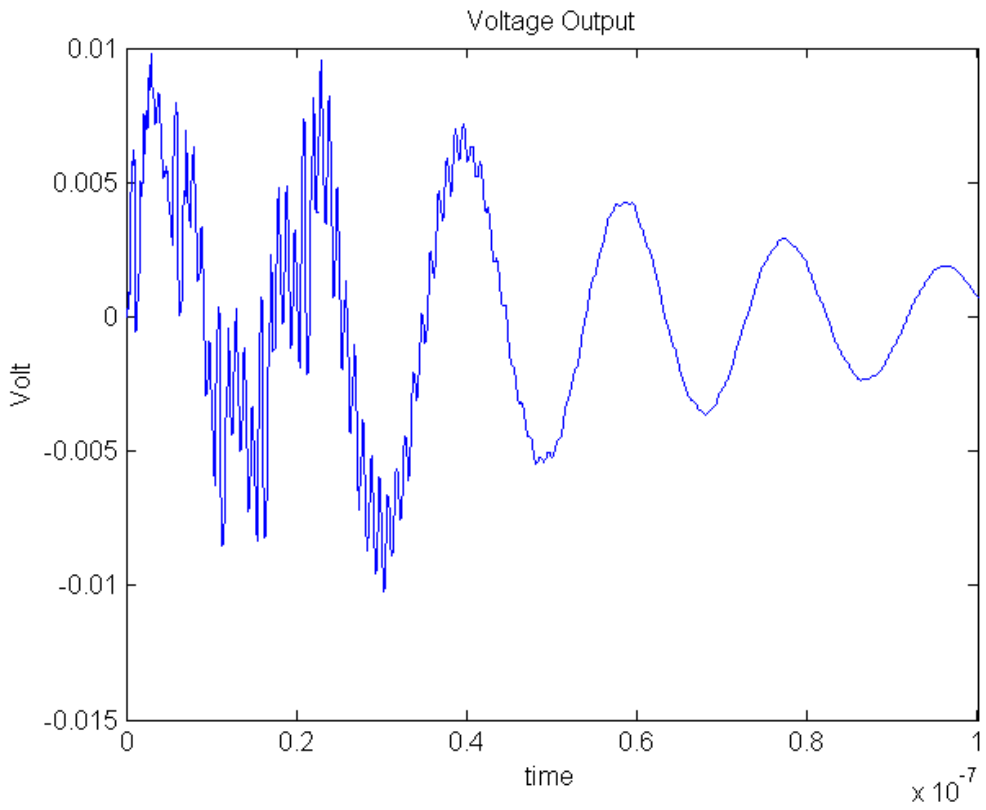
Fig. 4.7. Impedance of multi-layered irregular shaped planes.

To understand the resonant behavior of the structure in the time domain, multiple triangular current sources with a period of 5 ns having a rise time of 500 ps and fall time of 1 ns, which are produced by a switching circuit generating 200 MHz voltage clock waveforms, were injected at Port 1, Port 2, and Port 3 defined at (x = 7.5 cm, y = 7.5 cm)

on V4 - G3 plane, as shown in Fig. 4.8 (a). The structure was terminated using 1 mΩ at (x = 15 cm, y = 0 cm) between V4 - G3 plane. Fig. 4.8 (b) shows the transient response of the multi-layered irregular shaped cavity at Port 1. As is typical of a resonant cavity, the multi-layered plane structure initially builds up energy generated by each current source until the energy gained equals the energy lost on each cycle, then reaches the steady state, and finally decays to zero due to the losses in the planes after the switch is turned off. In addition to the oscillating waveform, high frequency glitches can be seen in the initial time period due to the switching circuits. The transmission matrix method is ideally suited for analyzing irregular shaped plane geometries, as demonstrated by the results in Fig. 4.8.



(a)



(b)

Fig. 4.8. Transient response of multi-layered irregular shaped planes: (a) current source at Ports 1, 2, and 3 and (b) voltage output at Port 1.

4.5 Summary

In this chapter, after the transmission matrix method was verified with the cavity resonator method for the multi-layered rectangular power/ground planes, via effects and the effects of multi-layered power/ground planes both in the frequency and time domain have been studied using the transmission matrix method. As the number of planes and vertical vias in parallel increases, the total inductance of planes with vias decreases due to a reduction in the loop current path. In addition, the resonant frequencies caused by the coupling of via inductance and plane capacitance occur at higher frequencies. Compared

with an irregular shaped geometry, the rectangular shaped power/ground planes are preferred because more boundaries in the structure can cause the resonant frequencies to occur at more frequencies.

The transmission matrix method is computationally more efficient than SPICE, which is commonly used for most power delivery system analysis. With linear CPU time and small memory requirements, the transmission matrix method provides the flexibility to analyze a large network containing up to 20 power /ground plane pairs.

CHAPTER 5

Model to Hardware Correlation

In the previous chapters, the transmission matrix method for an arbitrary shaped power distribution network was discussed. This chapter discusses model to hardware correlation in the frequency domain for an actual structure used by Eastman Kodak in their image processing boards and a test vehicle used by IBM with a CMOS ASIC test chip. In this chapter, one of three isolated core power supply planes in the Kodak power distribution network and one of three isolated core and I/O power supply planes in the IBM power distribution network have been simulated using the modeling method described in the previous chapters and correlated with hardware measurements using a Vector Network Analyzer.

5.1 Kodak Power Distribution Network

5.1.1 Structure and Model Description

The Kodak power distribution network is part of a high-speed commercial image processing system for high-resolution printing. It consists of three different DC islands of core power supply planes, which are called 1V5, 1V8 and 2V5 planes supplying 1.5, 1.8, and 2.5 DC voltages, respectively. Fig. 5.1 shows the top view for the power plane layer. The three power planes are isolated, as shown in Fig. 5.1, while their ground plane is continuous as a large rectangular plane.

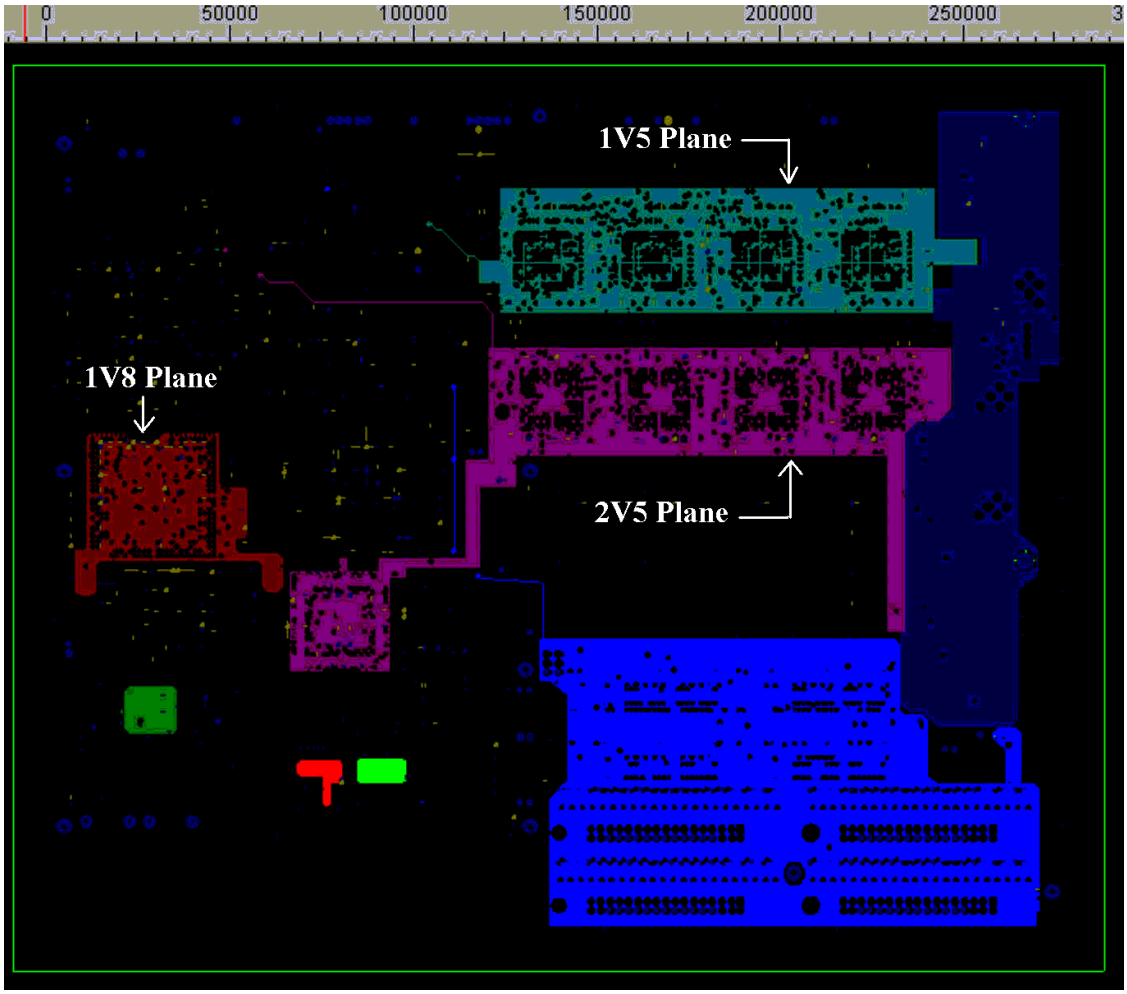


Fig. 5.1. Power plane layout for Kodak power distribution network.

The 1V8 plane is the main core power plane supplying power to the Motorola MPC8245 CPU chip, which is simulated and correlated with hardware measurements in this chapter. Fig. 5.2 shows the details of the 1V8 plane according to both original and gridded geometry co-ordinates. As shown in Fig. 5.2, the structure has arbitrary shaped power/ground planes including cutouts and a large number of via holes. In Appendix B, all the via holes are defined. The structure consists of a pair of power/ground planes with 3.8 mil FR4 dielectric with relative permittivity e_r = 4. The conductor planes were made

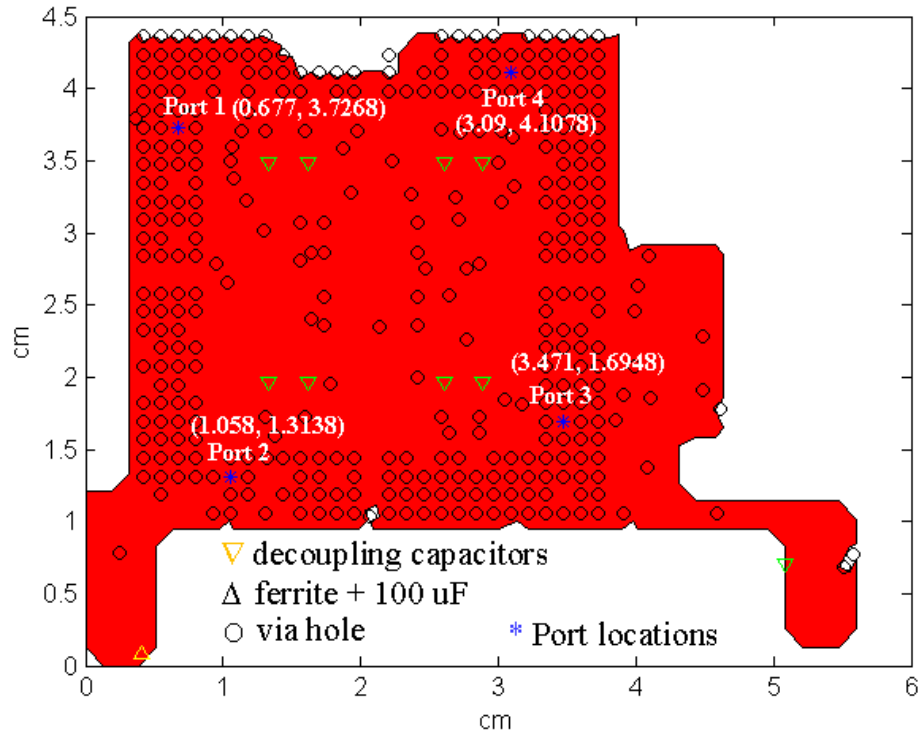
of copper ($s_c = 5.8 \times 10^7$ S/m) with a thickness of 12 μm. The dielectric loss tangent ($tan(d)$) varies linearly from 0.02 at 1 GHz to 0.06 at 3 GHz to include the loss of via holes. All ports of interest are defined in Fig. 5.2. Three kinds of surface mount capacitors were incorporated with locations shown by the triangular dots in Fig. 5.2. Their locations and values are shown in Table 5.1.

Table 5.1

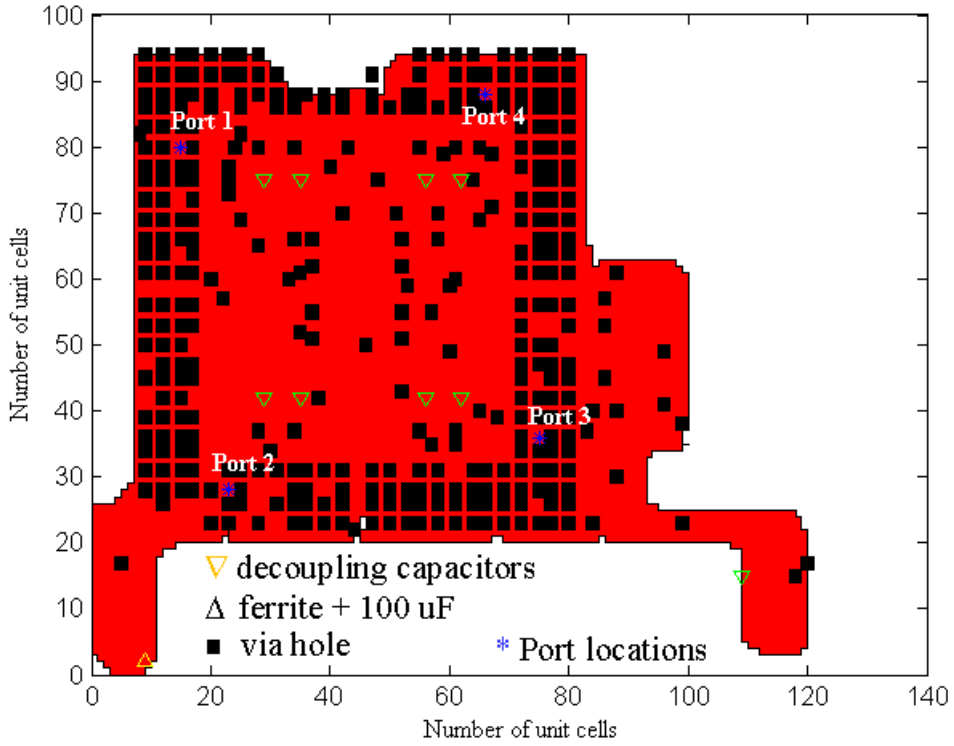
Decoupling capacitors in Kodak Power Distribution Network

#	x (cm)	y (cm)	C (F)	ESL (H)	ESR (Ω)
1	5.0800	0.7092	100E-06	10.0E-09	0.07
2	2.8829	1.9685	220E-12	2.05E-09	0.11
3	2.8829	3.4925	220E-12	2.05E-09	0.11
4	2.6035	1.9685	100E-09	2.00E-09	0.07
5	2.6035	3.4925	100E-09	2.00E-09	0.07
6	1.6129	1.9685	220E-12	2.05E-09	0.11
7	1.3335	1.9685	100E-09	2.00E-09	0.07
8	1.6129	3.4861	220E-12	2.05E-09	0.11
9	1.3335	3.4861	100E-09	2.00E-09	0.07
10	0.4064	0.0826	100E-06	10.0E-09	0.07.

To consider the effect of via holes, the planes were gridded, as shown in Fig. 5.2 (b), using a rectangular unit cell size of 0.46527 mm, whose area is approximately equal to that of a via hole size. The via hole was modeled using the plane capacitance with inductance in the boundary of planes, which is two times larger than the inductance on the inside. As a result, a via hole was represented using capacitance ‘C’ and inductance ‘2L’ of the planes in Eq. (2.1), as shown in Fig. 2.1.



(a)



(b)

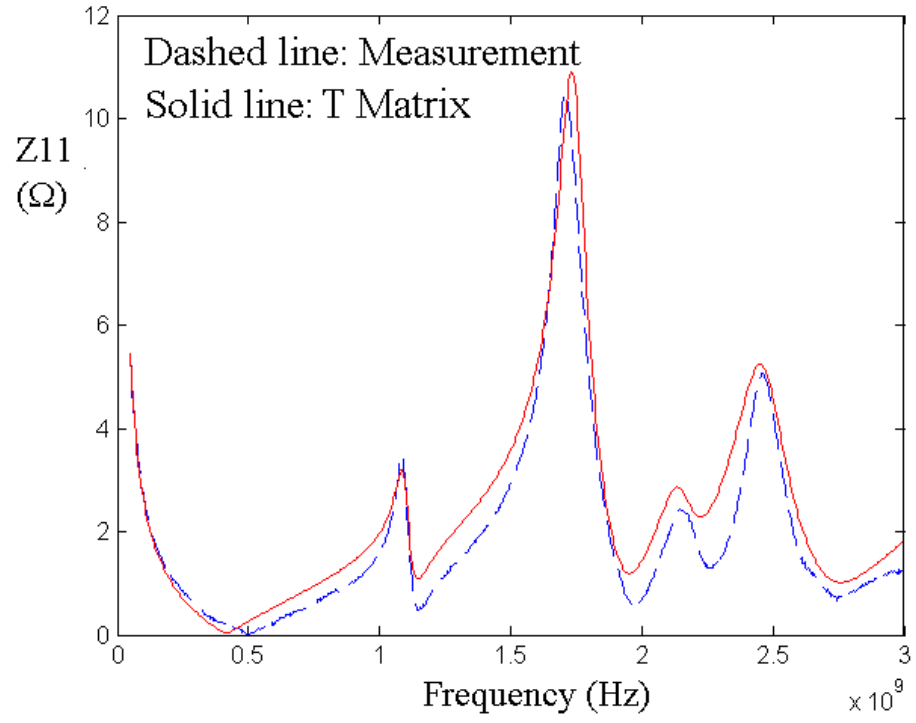
Fig. 5.2. Kodak 1V8 core power supply plane in (a) original and (b) gridded geometry co-ordinates.

5.1.2 VNA Measurements and Simulation

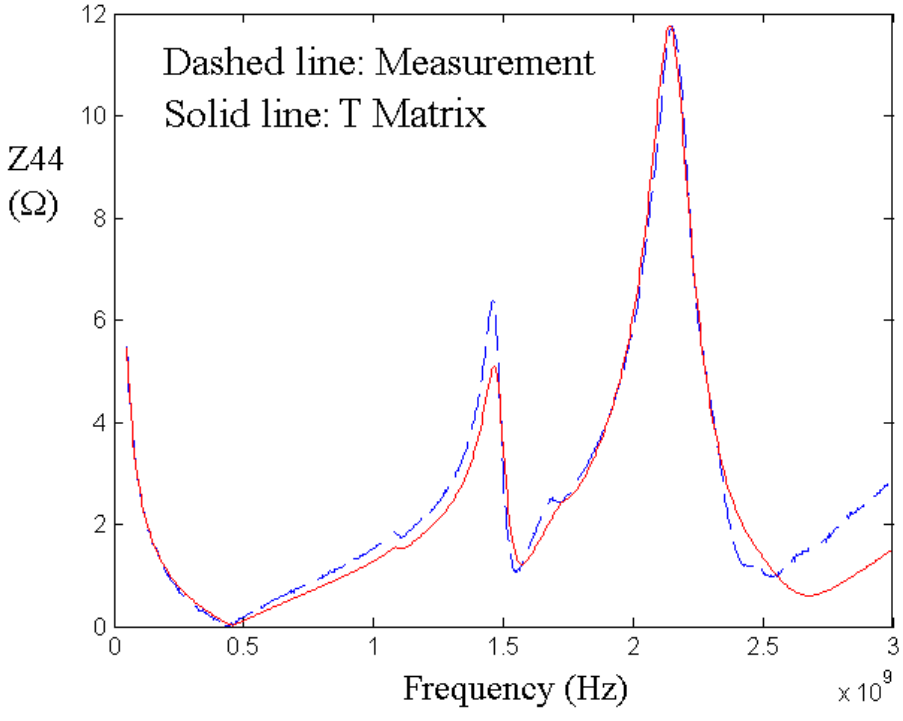
5.1.2a Without Decoupling Capacitors and Ferrites

Using a Vector Network Analyzer (VNA), a Cascade Microtech microprobe (bandwidth of 40 GHz) and coaxial cables, scattering (S) parameters were measured from 50 MHz to 3 GHz at the port locations defined in Fig. 5.2 and converted to an impedance matrix. Using SOLT (short, open, load and through) calibration, which was done using WINCAL software program, a two-port measurement method was applied for measuring low impedance values. As mentioned in the previous section, the unit cell size should be no greater than a via hole size in order to include its effect.

Figs. 5.3 and 5.4 show the comparisons between the measurements and simulations for self impedance and transfer impedance at the ports defined in Fig. 5.2. In this section, the measurements and simulations were done only for the bare board. Both the simulated and measured frequency responses show good correlation. However, a small discrepancy can be seen beyond 2.5 GHz. There are two possibilities for the discrepancy in the simulation and measurement. Although the measurement equipment was calibrated in the measurement, it was not possible to do a perfect calibration in the high frequency range. As a result, a measurement error could be generated in the device under test (DUT—planes), which has low impedance values compared with the 50-ohm termination used in a network analyzer. Another possibility is that the via hole needs to be modeled more accurately. In the simulation, the via hole was approximately modeled using the capacitance and inductance of the planes. This could have caused the discrepancy beyond 2.5 GHz.

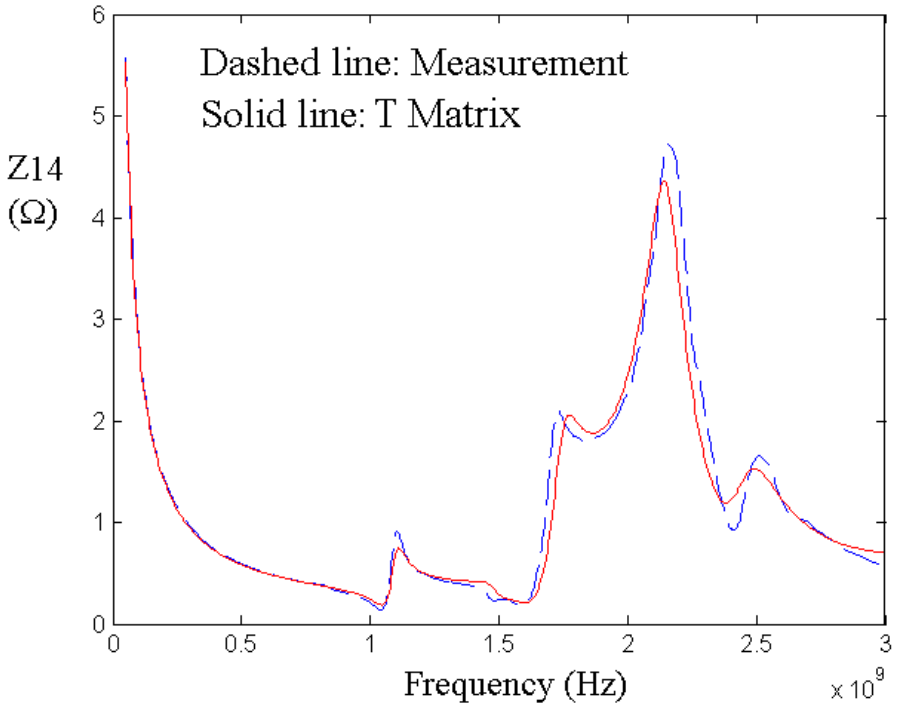


(a)

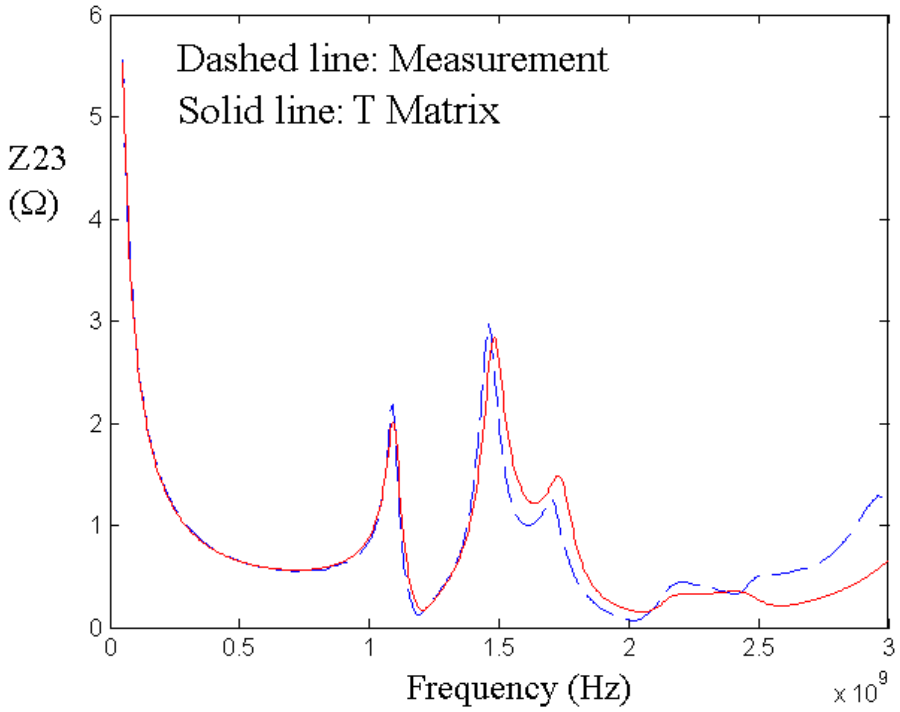


(b)

Fig. 5.3. Self impedance without decoupling capacitors and ferrites at (a) Port 1 and (b) Port 4.



(a)



(b)

Fig. 5.4. Transfer impedance without decoupling capacitors and ferrites between (a) Ports 1 and 4, and (b) Ports 2 and 3.

In the simulation, all the via holes should be considered since via cutouts were very dense compared to the size of the board. Fig. 5.5 shows the effect of the via holes compared with the bare board without via holes. In Fig. 5.5, the resonance frequencies of the bare board with the via holes occurs at lower frequencies. The via holes therefore cause the resonant frequencies to shift to lower frequencies since they are inductive.

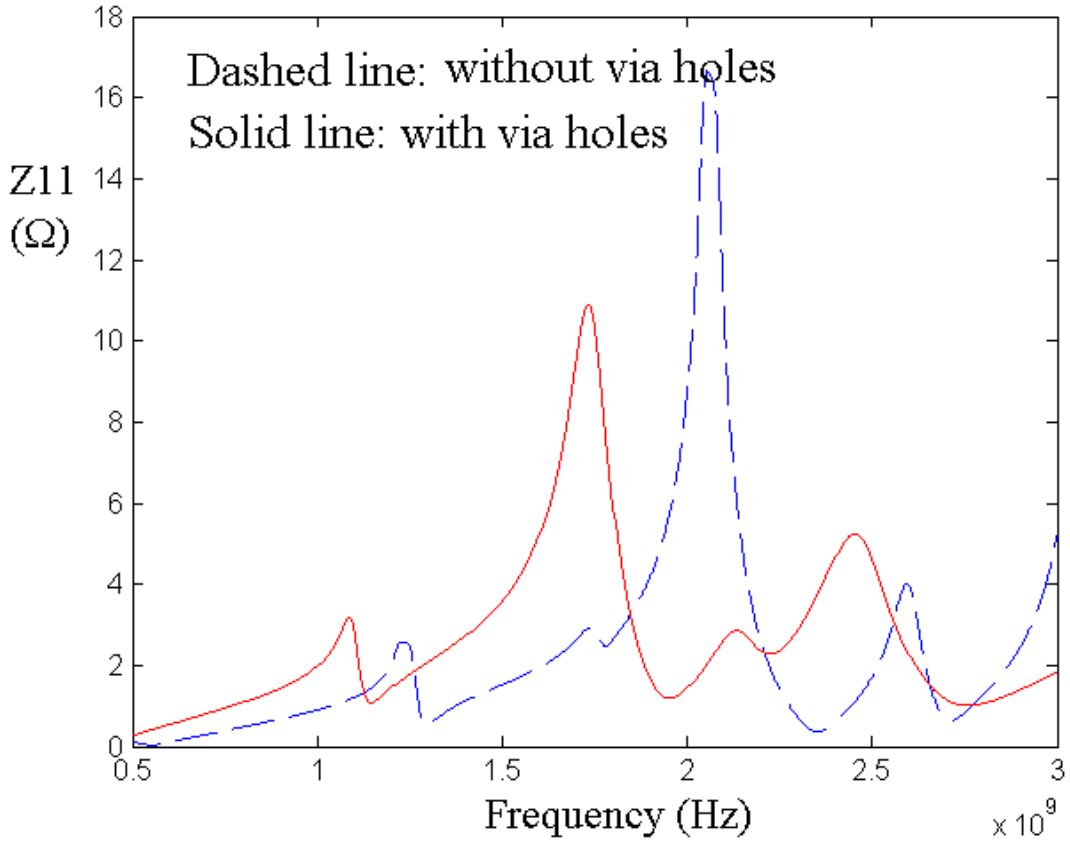
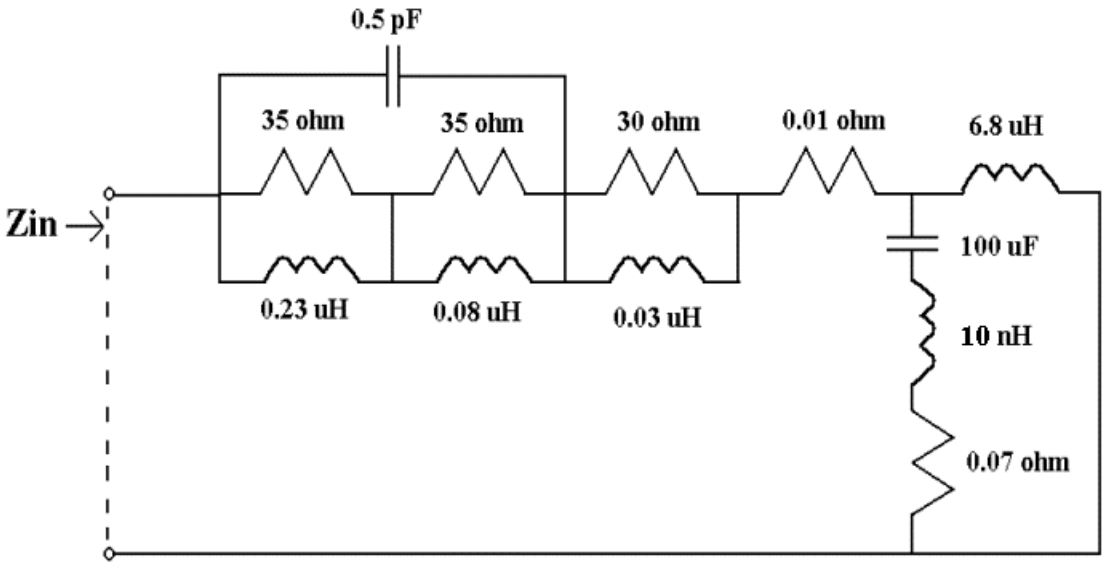


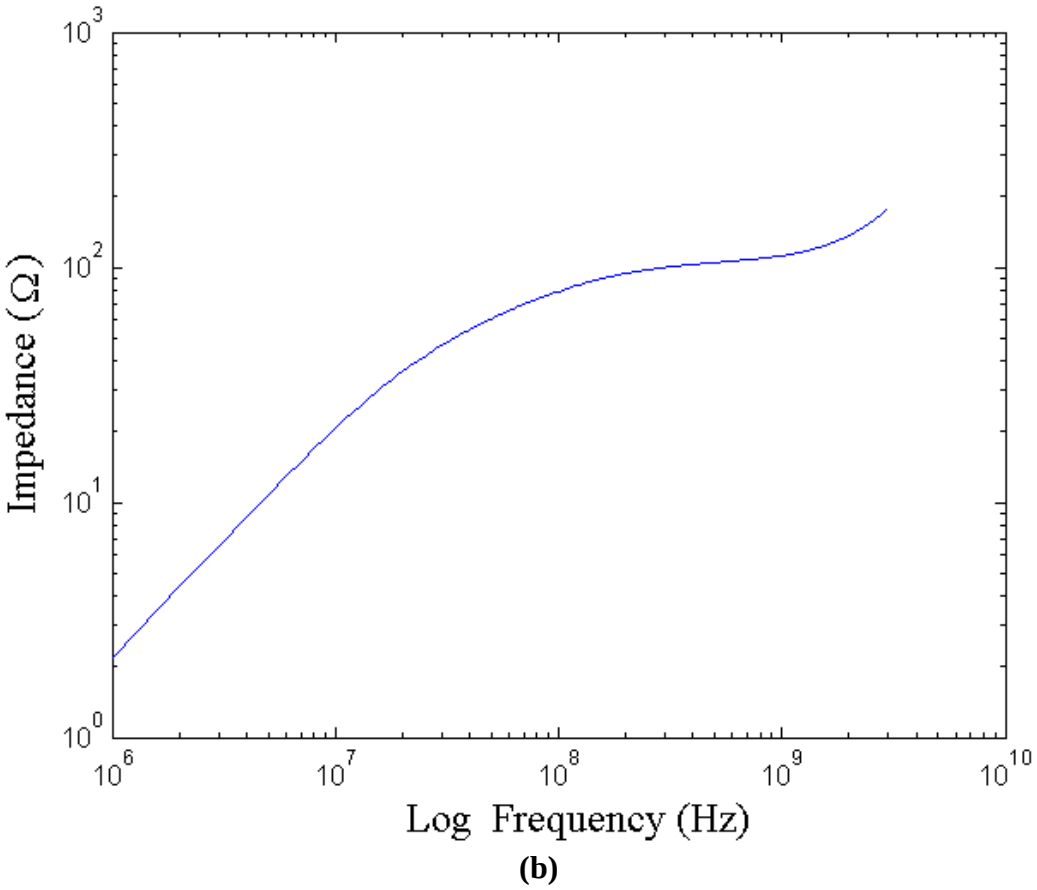
Fig. 5.5. Effect of via holes.

5.1.2b With Decoupling Capacitors and Ferrites

One method to reduce SSN is to use decoupling capacitors on the card, board, module, and chip. Decoupling capacitors are used to compensate the natural inductance of the power distribution networks, yielding small impedance for as large a frequency range as possible. To reduce the low and mid frequency impedance, bulk and bypass capacitors were incorporated into the structure. A ferrite was connected with a voltage regulator module (VRM) for filtering AC noise, the equivalent circuit of which is shown in Fig. 5.6. The ferrite did not affect the plane impedance in the mid and high frequency range since the input impedance of the ferrite was much larger than the plane impedance, as shown in Fig. 5.6 (b).



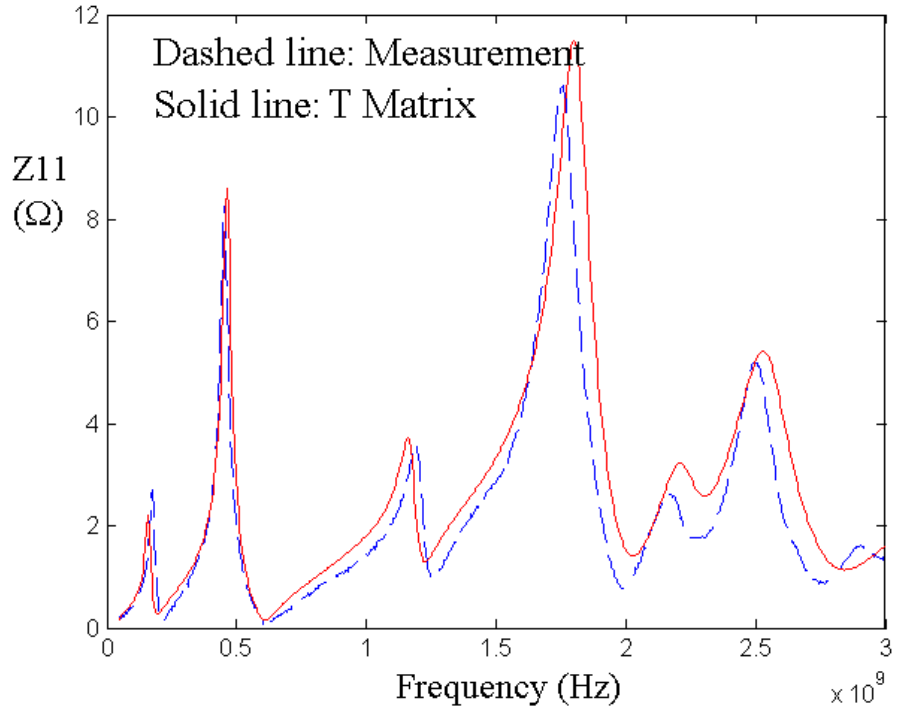
(a)



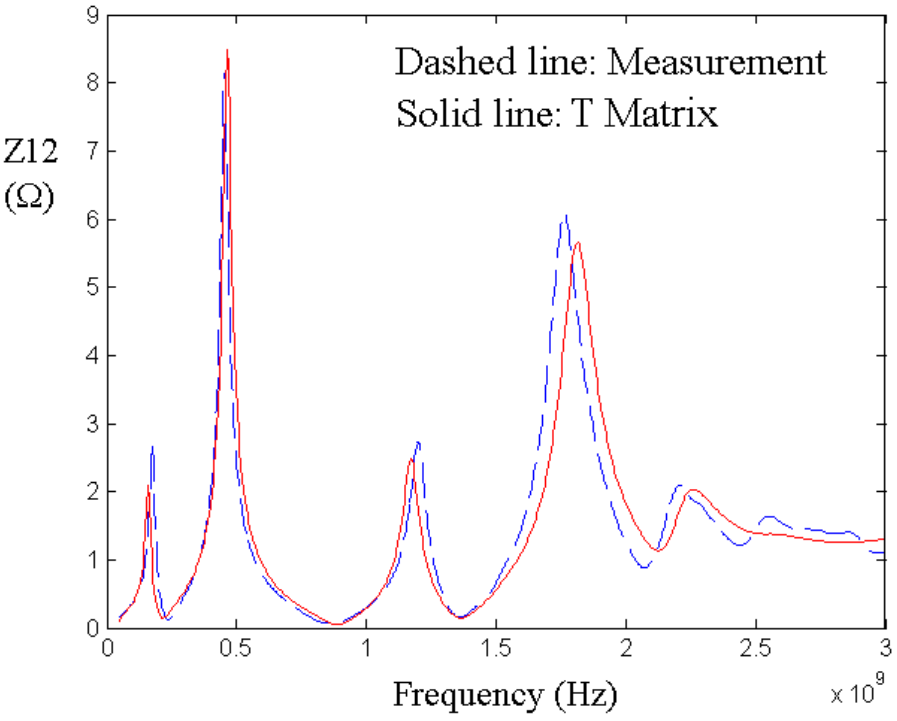
(b)

Fig. 5.6. Ferrite and 100 μF capacitor: (a) equivalent circuit and (b) input impedance.

The transmission matrix method was next applied to the structure including the decoupling capacitors and ferrite, and the impedance of the power distribution structure was recomputed. Self and transfer impedances between Ports 1 and 2 are shown in Fig. 5.7. Compared with the measurements, the simulated frequency responses have good correlation. Overall, the decoupling capacitors reduced low and mid frequency impedance; however, the additional resonant frequency at 500 MHz, which is caused by the coupling of plane impedance and 220 pF capacitors, could generate more noise.



(a)

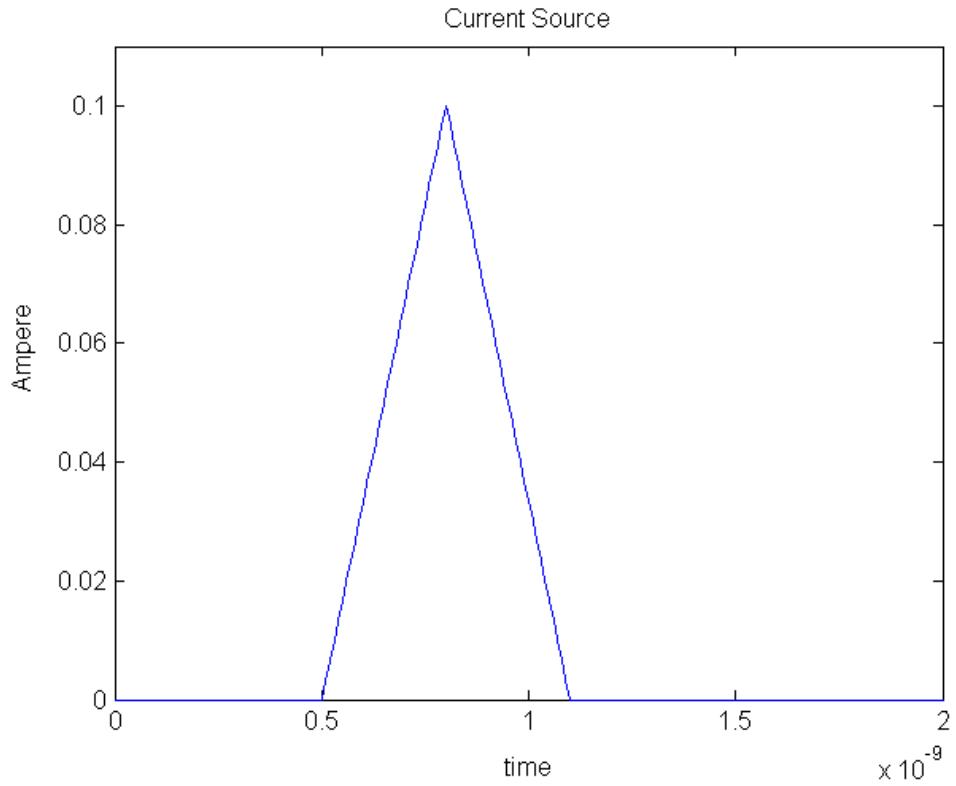


(b)

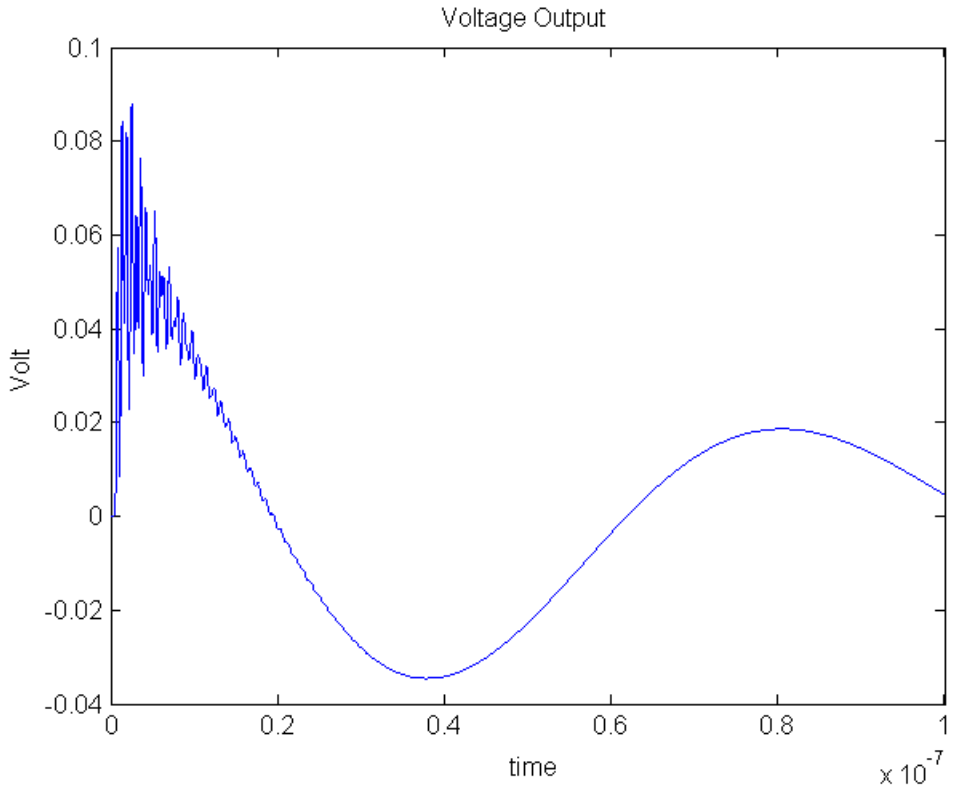
Fig. 5.7. Impedance with decoupling capacitors and ferrite (a) at Port 1 and (b) between Ports 2 and 3.

5.1.2c Transient Response

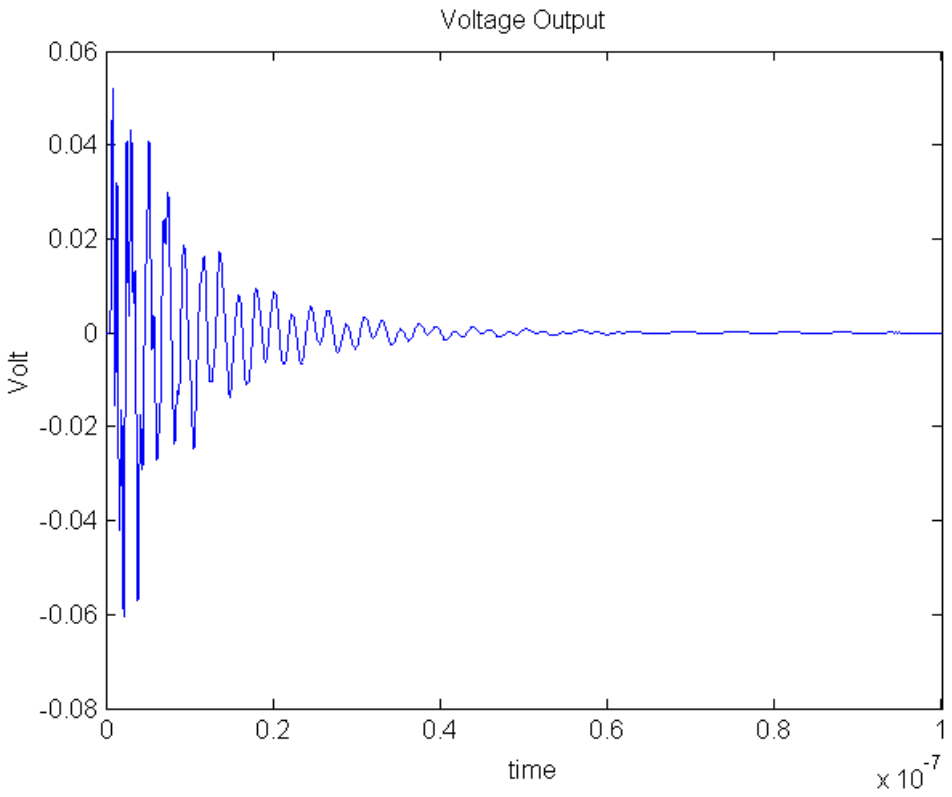
As mentioned earlier, the 1V8 power/ground planes supply power to core logic circuits. To compare vertical core simultaneous switching noise between the planes without decoupling capacitors and the planes with decoupling capacitors, the transient response was generated from the frequency data from DC to 3 GHz using the convolution and IDFT, as described in Chapter 3.4. The location of (x = 0.4064 cm, y = 0.0826 cm) was terminated using the equivalent circuit of the VRM and one 100 uF capacitor shown in Fig. 5.6. A 0.1 ampere triangular current source consisting of a rise time of 300 ps and a fall time of 300 ps with open source resistance was injected at Port 1 to mimic a transient current caused by a switching circuit generating 300 MHz voltage clock wave forms, and the output voltage was captured at Port 2. As shown in Fig. 5.8, although the presence of the decoupling capacitors on the planes reduces the coupling between Ports 1 and 2, they are not enough for maintaining the reliability of the system if a power of 5 watts is consumed in the core logic circuits. If the internal logic circuits simultaneously switch at the same time, 2.78 amperes (5 W / 1.8 V) could simultaneously flow into the core power supply planes. This means that 1.67 volt noise peak can be generated based on the maximum peak noise of 0.06 V shown in Fig. 5.8 (c), which was generated by a 0.1 ampere current source. As a result, the noise generated under the worst case conditions is much higher than the noise tolerance of 180 mV (10 % of 1.8 V). Therefore, this can cause the circuits to slow down and cause false switching of the circuits on the chip.


Current Source
Ampere
0.1
0.08
0.06
0.04
0.02
0
0
0.5
1
1.5
2
time
x 10^-9

(a)


Voltage Output
Volt
0.1
0.08
0.06
0.04
0.02
0
-0.02
-0.04
0
0.2
0.4
0.6
0.8
1
time
x 10^-7

(b)



(c)

Fig. 5.8. Transient response of Kodak planes: (a) current source at Port 1, (b) voltage output at Port 2 without decoupling capacitors and (c) voltage output at Port 2 with decoupling capacitors.

5.2 IBM Power Distribution Network

As another example, a test vehicle, which was designed and fabricated by IBM, was analyzed using the methods described in this dissertation. This section shows model to hardware correlation for a CMOS ASIC test chip packaged in a HyperBGA package and mounted on a printed wiring board (PWB). The extraction of unknown parasitics in the test vehicle was done using Vector Network Analyzer (VNA) measurements. The parasitics were included in the circuit model to obtain model to hardware correlation in the frequency domain.

5.2.1 IBM Test Vehicle Description

Fig. 5.9 shows the schematic of IBM's HyperBGA test vehicle [37], [38]. The CMOS ASIC test chip measured 10.9 mm on a side and was designed by IBM using the CMOS6SF 0.18µm ASIC logic family circuit library. The controlled collapse chip connection (C4) flip-chip technology was used to attach the test chip to the HyperBGA package. As shown in Fig. 5.9, this organic package has 2 signal layers and 4 power distribution layers consisting of two power planes and two ground planes. The V1 plane provides 2.5V to the core logic and I/O circuits. The V2 plane is split into four quadrants along two diagonal lines. Three of them, left, top, and right, are connected to 3.3V. The bottom quadrant is connected to 1.5V. All the quadrants of the V2 plane supply power to the I/O circuits. The power distribution layers in the HyperBGA package are shown in Table 5.2.

Table 5.2

Cross Section of Power Distribution Layers in HyperBGA Package

TSR	Ground
V1	Solid plane 2.5V
GND	Ground
V2	Split plane 3.3V+1.5V.

With a size of 45×30cm, the printed wiring board (Saranac PWB) consists of two GND planes, two 2.5V planes, two 1.5V planes, two 3.3V planes and eight signal layers. The assignments of the layers are shown in Table 5.3. The S3, S5, S7, S9, S10, S12, S14 and S16 are signal layers in the Saranac PWB. There are 40 decoupling capacitors mounted

on the board with values: 20μF×10, 0.47μF×15 and 0.01μF×15. Their parasitic inductance and resistance, as given by the manufacturer, are shown in Table 5.4.

Table 5.3

Cross Section of Power Distribution Planes in Saranac Board

V2 plane	Full layer ground plane
V4 plane	Full layer plane V1 = 2.5V
V6 plane	Full layer plane V2 = 1.5V
V8 plane	Full layer plane V3 = 3.3V
V11 plane	Full layer plane V4 = 2.5V
V13 plane	Full layer plane V5 = 1.5V
V15 plane	Full layer plane V6 = 3.3V
V17 plane	Full layer ground plane.

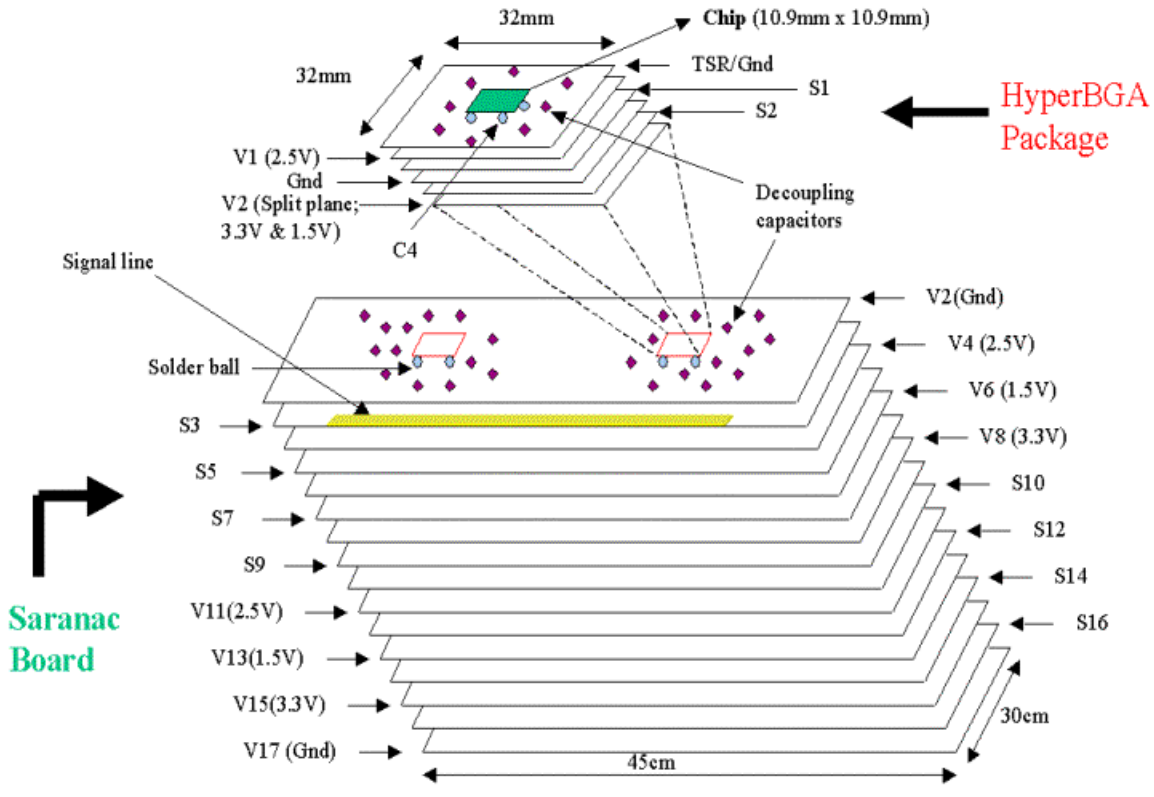


Fig. 5.9. IBM's HyperBGA test vehicle [38].

Table 5.4

Decoupling Capacitors in IBM Test Vehicle

C (*mF*)	ESR (*W*)	ESL (*nH*)
20	1	10
0.47	0.1	1
0.01	0.1	1

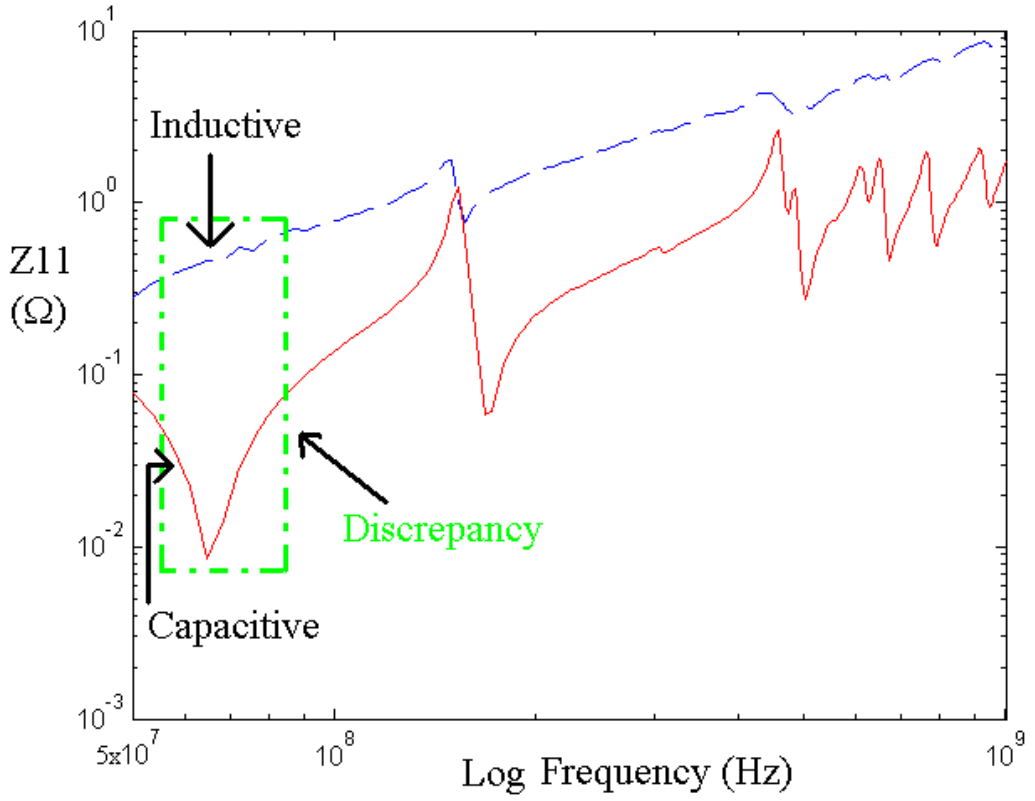
This test vehicle is actually a double module structure having two HyperBGA packages, as shown in Fig. 5.9. The Saranac PWB also consists of two separate parts for supplying power to the right and left packages. They are symmetric and have the same frequency response. In this section, the right package and upper layers shown in Fig. 5.9 were modeled.

5.2.2 VNA Measurements and Simulation

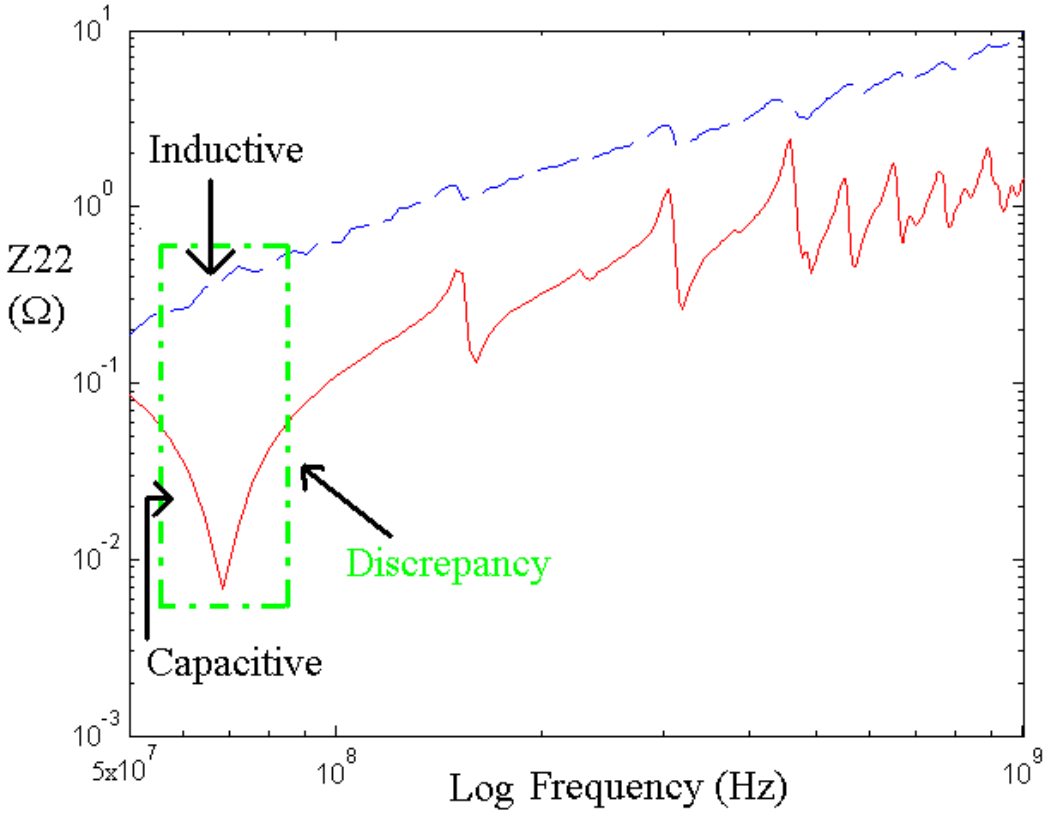
5.2.2a Bare board Without Decoupling Capacitors and no Package

First, the V2 (Gnd) and V4 (Vdd) plane pair was analyzed without decoupling capacitors. The package was also absent from the board for this analysis. This section discusses the frequency domain measurements. The time domain measurements are discussed in Chapter 7.3.2. Both the planes have dimensions of 45 cm by 30 cm with a 12.5756-mil thick FR4 dielectric with relative permittivity e_r = 4.6. . The conductor planes are made of copper ($s_c = 5.8\times10^7$ S/m) with a thickness of 33.528 μm and dielectric loss tangent $tan(d)$ = 0.02 at 1 GHz.

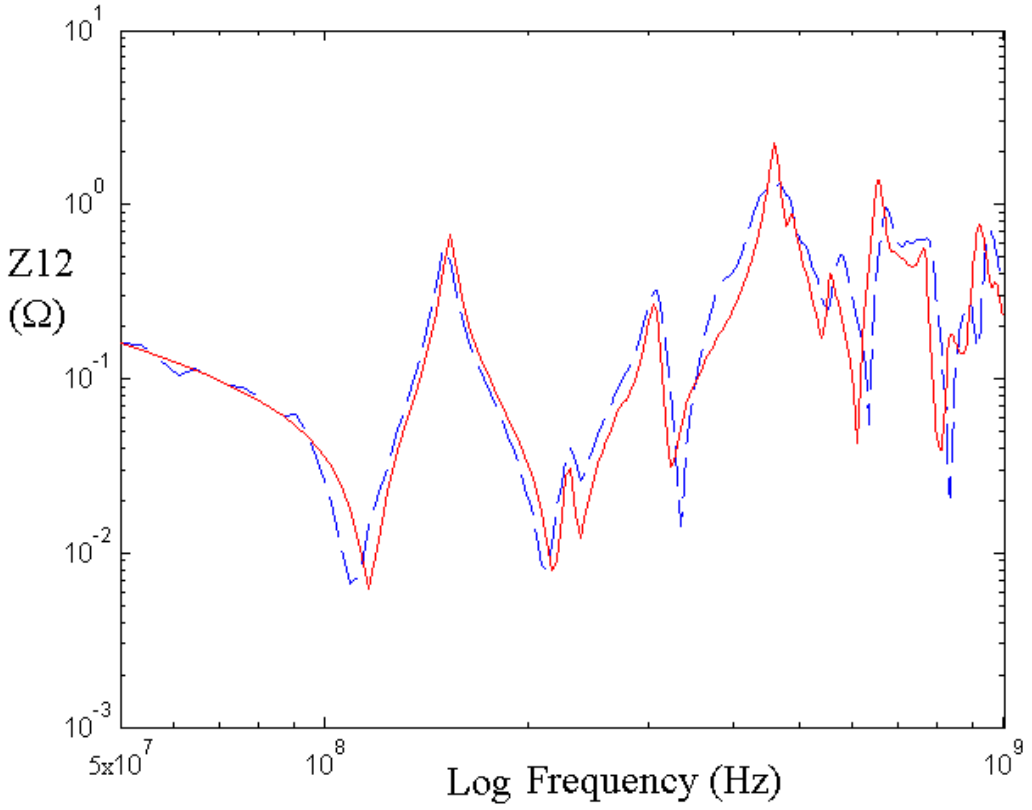
For frequency domain measurements, the measurement method described in the previous section using a VNA was applied to obtain S parameters, which were then converted to Z parameters. The frequency domain measurement was done at the capacitor sites, whose locations are described in Appendix C, to capture unknown parasitics in the structure. To compute the unknown parasitics, the measured and simulated impedance results were first compared for a bare board. Fig. 5.10 shows the impedance response of the simulated and measured results between the C31 and C25 capacitor sites. As shown in Fig. 5.10, the self impedances of both the sites show a large discrepancy between the simulated and measured results while the transfer impedance has a good correlation. In the figure, the measured results of self impedance show inductive behavior around 50MHz, but the simulated results show capacitive behavior around 50MHz. Typically, the self impedance of the bare board should be capacitive at low frequency since the parallel planes form a capacitor. This discrepancy is due to the parasitic series inductance in the bare board due to the inductance of the capacitor pads. Fig. 5.11 explains why the self impedance is inductive while the transfer impedance is capacitive at low frequency. The parasitic inductance is added to the self impedance of the planes at the ports shown in Fig. 5.11, however, it does not affect the transfer impedance. Initially, this pad inductance was not included in the model. This is the reason the self impedances are actually inductive at low frequency.


Inductive
Z11
(Ω)
Discrepancy
Capacitive
Log Frequency (Hz)

(a)


Inductive
Z22
(Ω)
Discrepancy
Capacitive
Log Frequency (Hz)

(b)



(c)

Fig. 5.10. Impedance response of transmission matrix method (solid) and measurement (dashed) without unknown parasitics: (a) self impedance at C31, (b) self impedance at C25 and (c) transfer impedance.

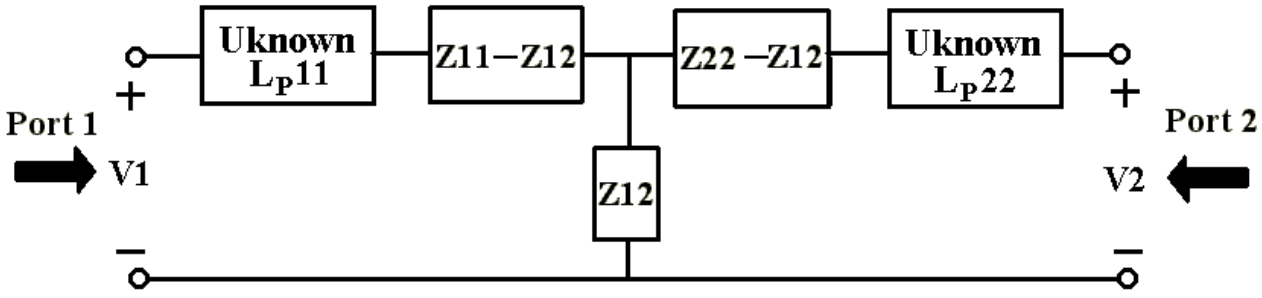
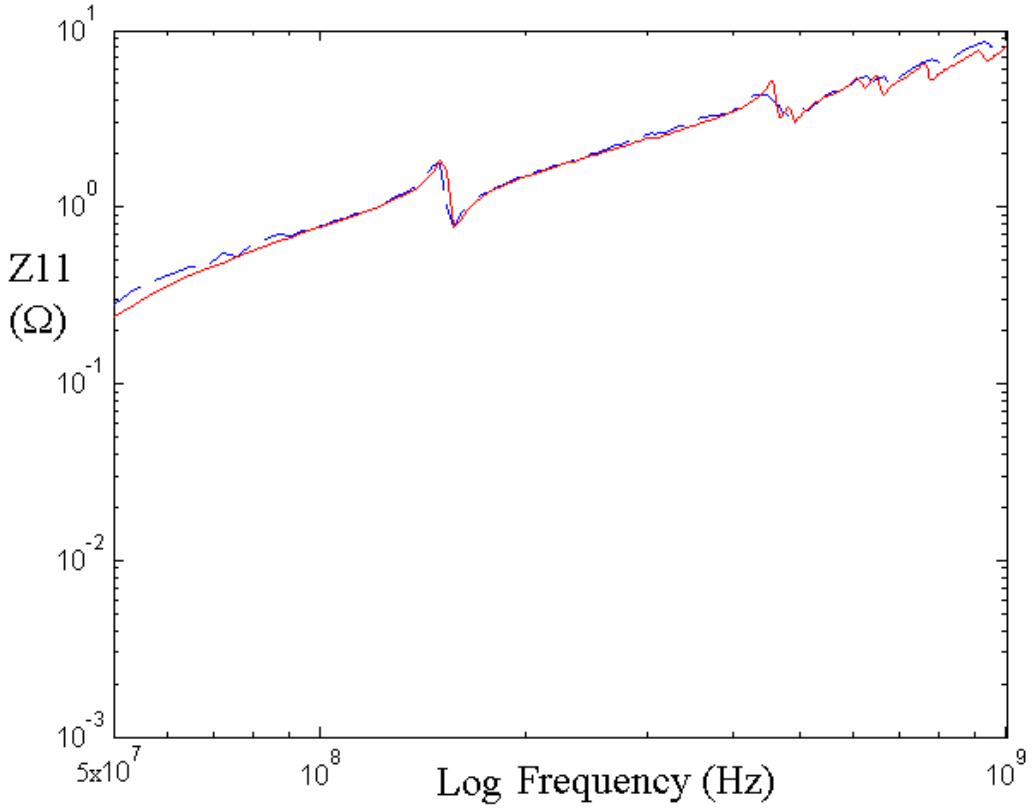


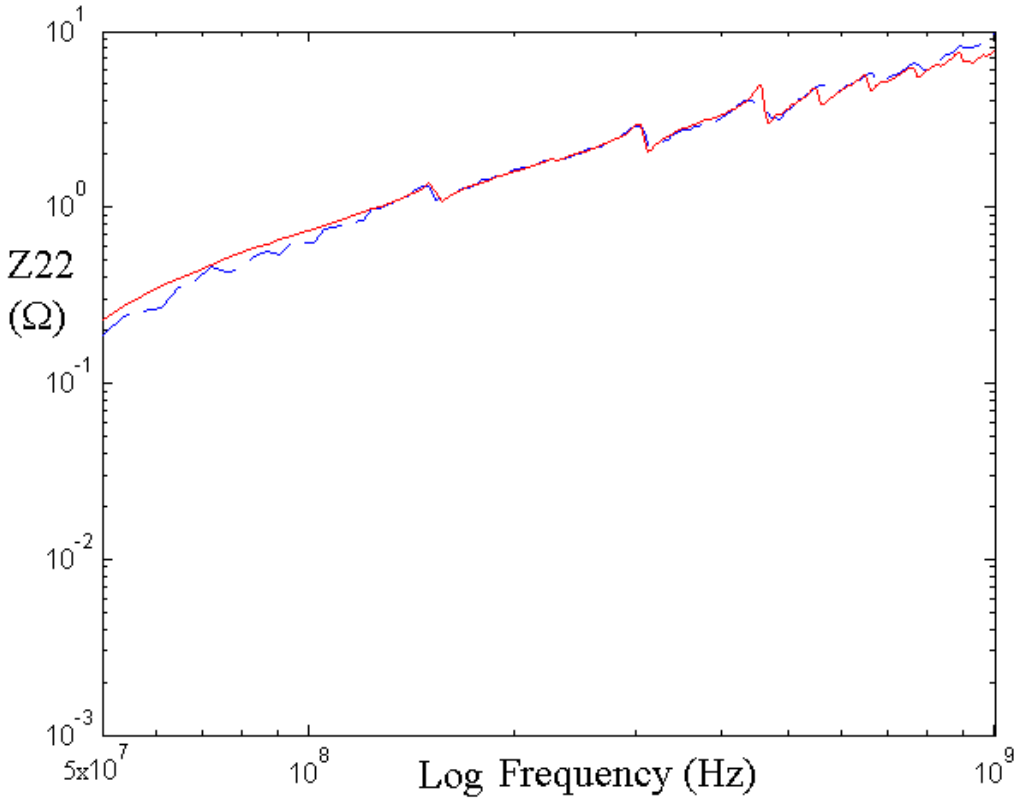
Fig. 5.11. Equivalent circuit diagram for plane impedance and unknown parasitics.

From the comparison between the measured and simulated results, the unknown parasitic series inductance can be estimated. The parasitic series inductance (L_p11, L_p22) for both the port sites shown in Fig. 5.11 was around 1.01 nH. It is important to note that this inductance includes the loop inductance of the capacitor pads. Fig. 5.12 shows the self impedances at both the port sites with the effect of the parasitics. As shown in Fig. 5.12, there is a good correlation between the measured and simulated results up to 1 GHz when the parasitic series inductance is included in the model.

As a next step, the bare board with capacitors was used to capture the parasitic inductance and resistance of capacitors such as equivalent series inductance (ESL) and equivalent series resistance (ESR). These results are described in the next section.



(a)



(b)

Fig. 5.12. Impedance response of transmission matrix method (solid) and measurement (dashed) with unknown parasitics: (a) self impedance at C31 and (b) self impedance at C25.

5.2.2b Board with Decoupling Capacitors and no Package

The V2 and V4 plane pair in the Saranac PWB with decoupling capacitors and no package was next analyzed, as shown in Fig. 5.9. A total of twenty one decoupling capacitors were incorporated into the V2/V4 planes, with locations as shown in Appendix C. All the locations are based on the co-ordinate system where the left bottom corner of the V2/V4 planes is at the origin (0,0). For the measurement, four of the capacitors (C16, C19, C25 and C31) were excluded.

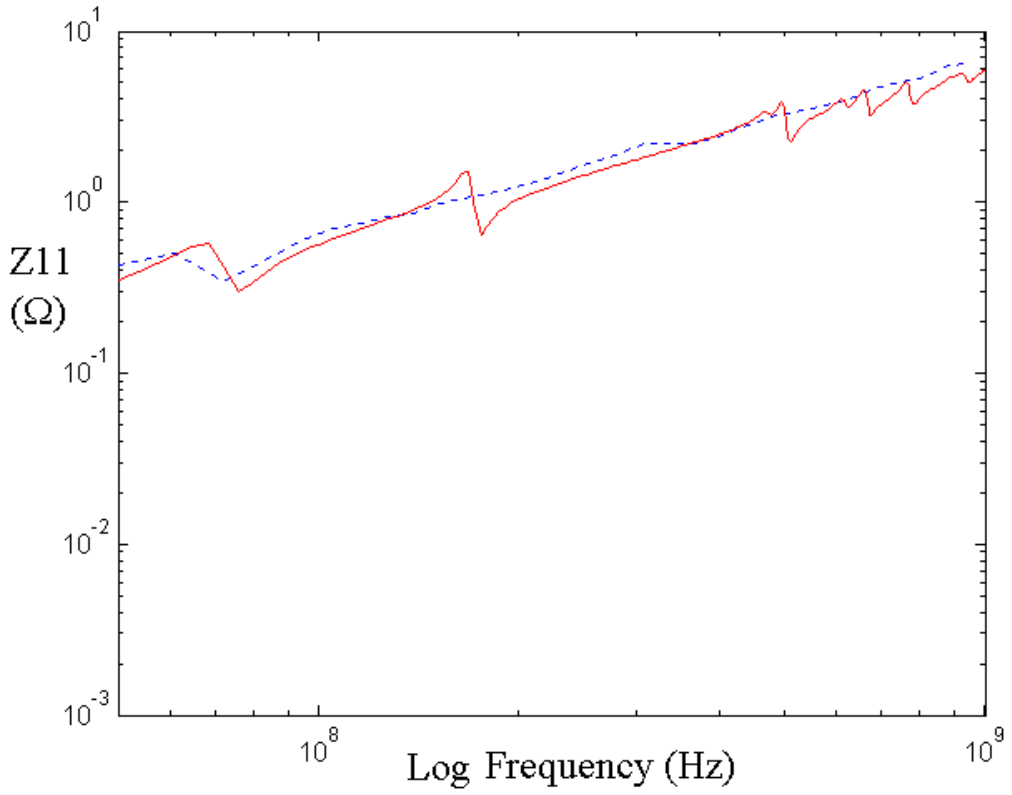
Using the capacitance and its parasitic inductance and parasitic resistance shown in Table 5.4, the modeling results were compared with measurements. The results showed large discrepancy. This was because the loop inductance of the capacitor pads was not included in the model. The equivalent series inductance and resistance were then updated as shown in Table 5.5 to obtain good correlation.

Table 5.5

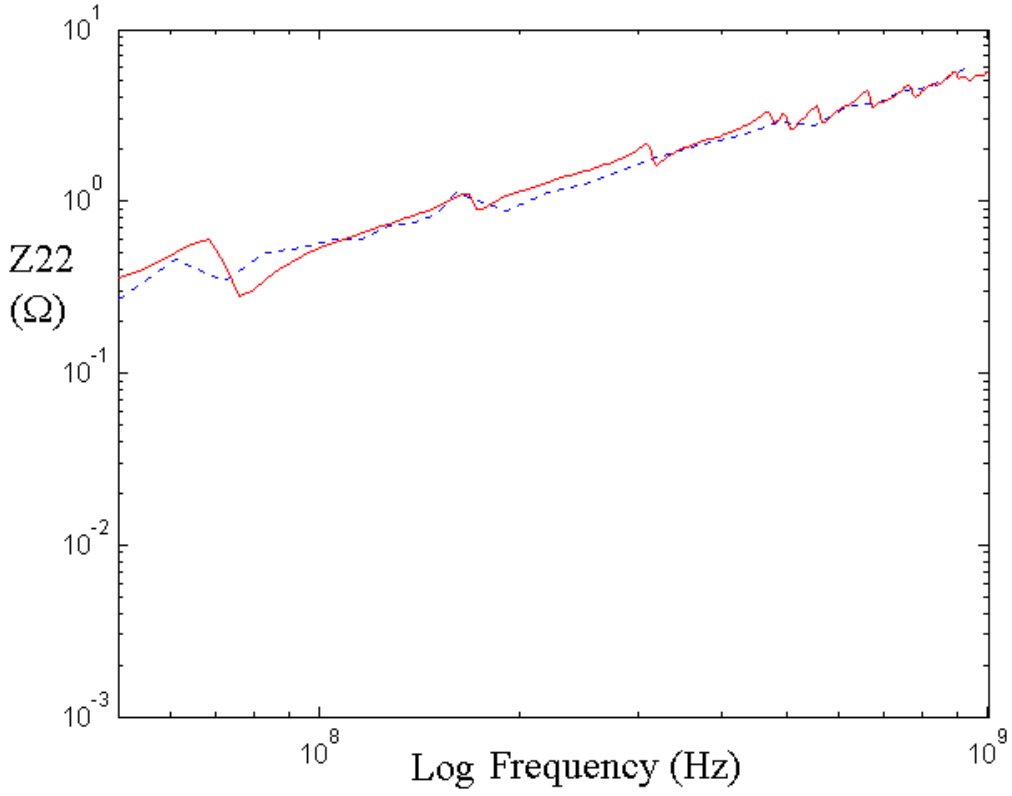
Decoupling Capacitors used for Model to Hardware Correlation

C (*mF*)	ESR (*W*)	ESL (*nH*)
20	1	10
0.47	0.2	2.5
0.01	0.2	2.5

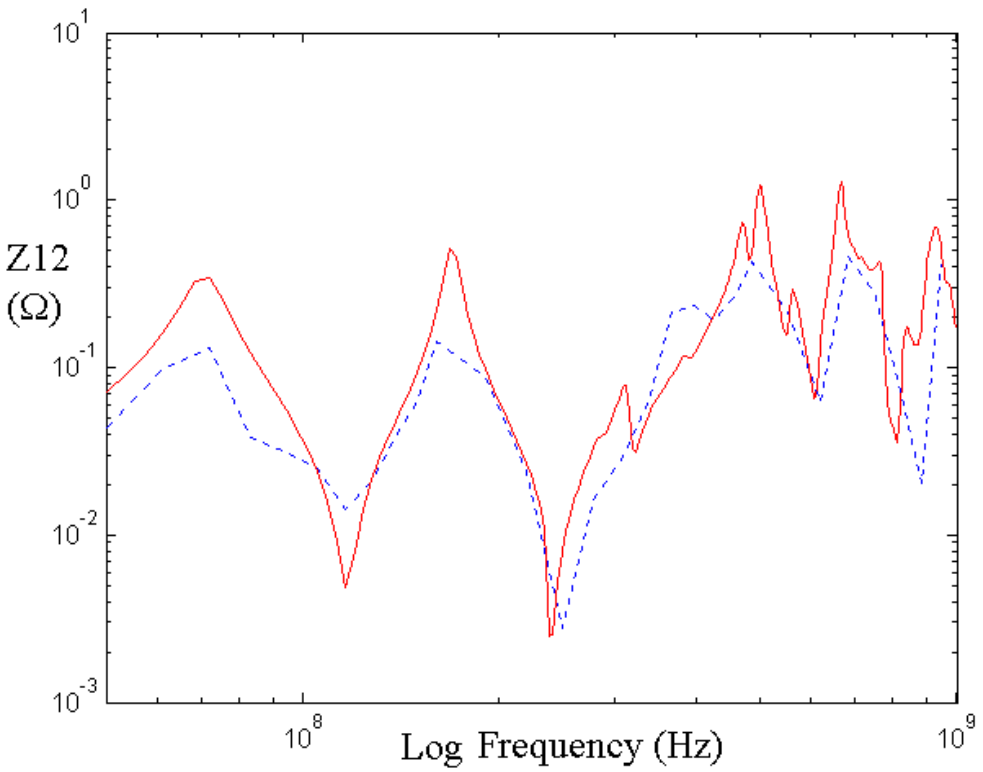
Using the updated values of the decoupling capacitors, the transmission matrix method provided good correlation with measurements, as shown in Fig. 5.13. In the figure, the first resonant peak is due to the 0.01 μF capacitors while resonant peaks related to 0.47 μF and 20 μF capacitors occur below 50 MHz. Since VNA measurements start at 50MHz, these resonances are not shown in the figure. In addition, the ESL and ESR values of 0.47 μF and 20 μF capacitors could not be obtained from measurements. This is the reason for the discrepancy between the model and measurements in Fig.5.13.


Z11
(Ω)
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{8}
10^{9}
Log Frequency (Hz)

(a)


Z22
(Ω)
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{8}
10^{9}
Log Frequency (Hz)

(b)



(c)

Fig. 5.13. Impedance response of transmission matrix method (solid) and measurement (dashed) with decoupling capacitors: (a) self impedance at C31, (b) self impedance at C25 and (c) transfer impedance.

5.3 Summary

In this chapter, the accuracy of the transmission matrix method has been verified through frequency domain measurements. The method showed good model to hardware correlation for an arbitrary shaped power distribution network used by Eastman Kodak in their image processing boards. In addition, rectangular power distribution planes were analyzed and compared with measurements. This test vehicle was supplied by IBM.

Using the transmission matrix method, the Kodak power distribution network having large cutouts and many via holes was analyzed. The simulation results were compared

with the measured response obtained using a Vector Network Analyzer. Good correlation for both without and with decoupling capacitors and ferrites was obtained over a bandwidth of 3 GHz. It is important to note that cutouts and via holes need to be included in the model for obtaining good correlation with measurements.

Using the comparison between measured and simulated responses, unknown parasitics of the decoupling capacitor pads, which can be modeled as equivalent series inductance or resistance, can be extracted. As an example, IBM's HyperBGA test vehicle was analyzed to explain the effect of the pad parasitics on the frequency response. These effects are important for modeling planes in realistic packages and boards.

CHAPTER 6

Macro-modeling using Rational Functions

In the previous chapters, the transmission matrix method has been described for analyzing power distribution networks. This enables the extraction of the frequency response at specific ports in the power distribution network. It has also been shown in the previous chapters that for a linear current source, the time domain response of the power distribution network can be computed using an IDFT and convolution. However, in most systems, the magnitude and time signature of power supply noise is highly dependent on the non-linearity of the drivers. This chapter addresses the computation of power supply noise in the time domain in the presence of non-linear drivers.

High performance computer systems are extremely complex and often contain high density I/O connectors, packages and boards. The complexity of such systems continues to drive the need for improved circuit analysis for system level simulation. However, the use of circuit simulators such as SPICE, ADS and MDS [55] might be inefficient or prohibitive for such electrically large systems. In such cases, the development of reduced electrical behavior models generated through data from Vector Network Analyzer measurements or modeled data from efficient electromagnetic solvers are preferred. This is possible through macro-models, which are based on Pade approximation using rational functions [39]-[44]. Pade approximation enables the representation of frequency data using rational functions. These rational functions capture the input-output behavior of circuits and are called macro-models. The macro-models can be combined with nonlinear

circuits for transient simulation in SPICE or any other circuit simulator. In this chapter, the macro-models have been used to represent the frequency response of the power distribution network computed using the transmission matrix method, as shown in Fig. 6.1. In Fig. 6.1, the geometry information for the power distribution is obtained directly from a Cadence board (.brd) file.

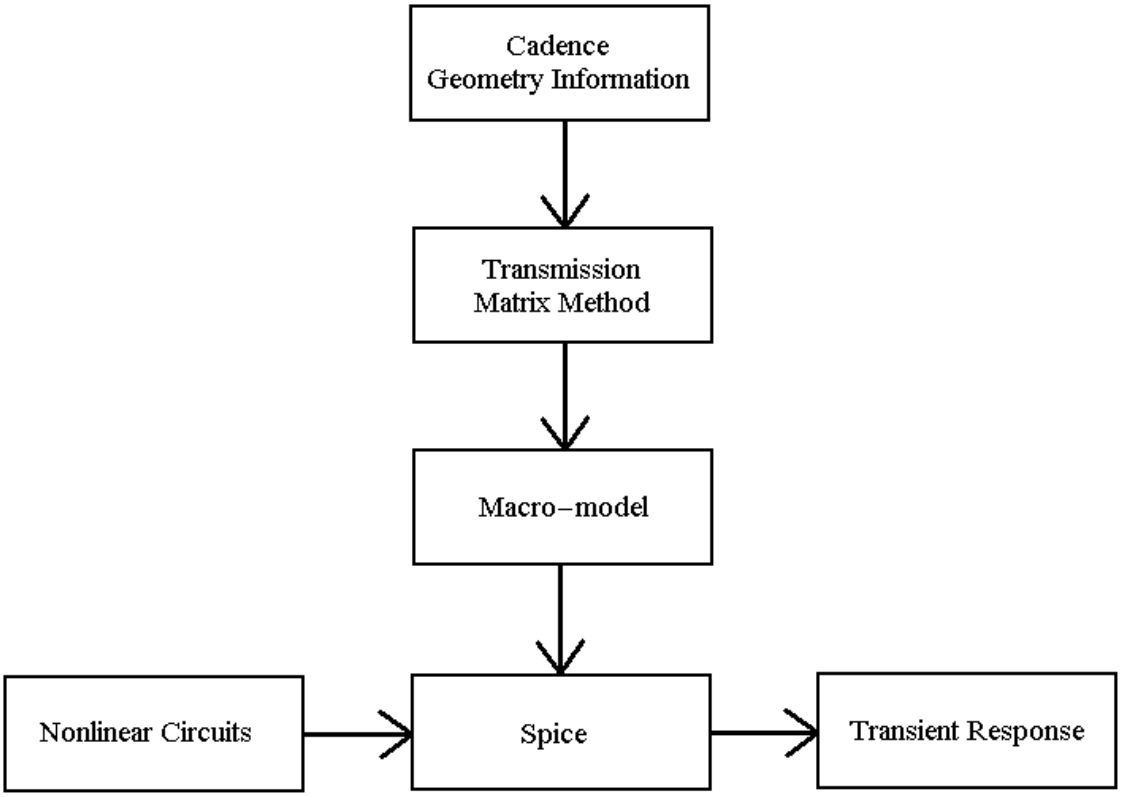


Fig. 6.1. Architecture for the analysis of simultaneous switching noise.

In Fig. 6.1, macro-models reduce the computational complexity for a transient simulation through reduced order models obtained by eliminating the internal nodes in a network. In terms of input and output at the ports of interest, macro-models provide a transfer function. However, it is nontrivial to ensure the passivity of the transfer function,

which ensures absolute stability of the circuit model [45], [46]. In addition, when the frequency range is wide or the order of the approximation is high, a matrix for finding unknown coefficients constructed by the method of least squares using power series or Chebyshev polynomials is highly ill conditioned and nearly singular [44]. This is because the polynomials representing the frequency $\{w^0, w^1, w^2, w^3 \cdots\}$ have a very large dynamic range. Also, when systems require multiple ports and higher order, it is difficult to reduce errors between the original and approximated data.

Using the transmission matrix method described in the previous chapter, the frequency response for multi-layered regular or irregular shaped power distribution networks can be computed, which represents input data for macro-modeling. Macro-models can be generated from Y (admittance), Z (impedance) or S (scattering) matrices. Then, macro-models containing the frequency response at specific ports can be represented using equivalent circuits, which can be represented using R (resistance), L (inductance), C (capacitance) and G (conductance) circuit elements in a circuit simulator such as SPICE. Depending on the matrices used, their equivalent circuits can be represented in different forms even if they are not unique. In this chapter, the macro-modeling method using Y-parameters for multi-port systems and its circuit implementation are discussed.

6.1 Pade Approximation

A Pade approximation seeks to approximate the frequency response H(s) of linear passive networks, which is generated from Y, Z, or S matrices, by generating a rational function that approximates the original data. The desired rational function has the form:

$$H(s)=\frac{P_m}{Q_n}=\frac{\sum_{i=0}^{m} a_i s^i}{\sum_{j=0}^{n} b_j s^j}=\frac{a_0+a_1 s^1+\ldots+a_m s^m}{b_0+b_1 s^1+\ldots+b_n s^n} \tag{6.1}$$

where $s = jw$, w is the angular frequency, 'm' and 'n' are the order of the numerator and denominator, respectively, and a_i and b_i are unknown coefficients to be computed. It is important to note that |m-n| is less than or equal to 1 for circuit representation using R, L, C, and G circuit elements. Eq. (6.1) can be separated into real and imaginary parts assuming real coefficients a_i and b_i as follows:

$$\begin{aligned}\sum_{i=0}^{m} a_i\, Re\{s^i\}-\sum_{j=0}^{n} b_j\, Re\{H(s)s^j\}=0\\ \sum_{i=0}^{m} a_i\, Im\{s^i\}-\sum_{j=0}^{n} b_j\, Im\{H(s)s^j\}=0\end{aligned} \tag{6.2}$$

where $Re\{s^i\}$ and $Im\{s^i\}$ are real and imaginary parts, respectively. Eq. (6.2) can next be rearranged as a matrix equation in the following form:

$$[A][X]=[0]$$

$$\begin{bmatrix} \sum_{i=0}^{m} Re\{s_1{}^i\}-\sum_{j=0}^{n} Re\{H(s_1)s_1{}^j\} \\ \sum_{i=0}^{m} Im\{s_1{}^i\}-\sum_{j=0}^{n} Im\{H(s_1)s_1{}^j\} \\ \vdots \\ \vdots \\ \sum_{i=0}^{m} Re\{s_k{}^i\}-\sum_{j=0}^{n} Re\{H(s_k)s_k{}^j\} \\ \sum_{i=0}^{m} Im\{s_k{}^i\}-\sum_{j=0}^{n} Im\{H(s_k)s_k{}^j\} \end{bmatrix} \begin{bmatrix} a_0 \\ a_1 \\ \vdots \\ a_m \\ b_0 \\ \vdots \\ b_{n-1} \\ b_n \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix} \tag{6.3}$$

where $[A]$ is a $(2k)\times(m+n+2)$ known matrix which is generated from the 'k' points of frequency samples of H(s), and $[X]$ is a column vector for unknown real coefficients. For a multi-port network, the macro-model can be expanded into Eq. (6.3). From the characteristics of a linear passive network and assuming common poles, the matrix $[A]$ for an '*N*' port system can be represented using a common denominator in the following form:

$$[A]=\begin{bmatrix}
\begin{bmatrix} Re\{s_1^{\,0}\} & \cdots & Re\{s_1^{\,m}\} \\ \vdots & & \vdots \\ Re\{s_k^{\,0}\} & \cdots & Re\{s_k^{\,m}\} \\ Im\{s_1^{\,0}\} & \cdots & Im\{s_1^{\,m}\} \\ \vdots & & \vdots \\ Im\{s_k^{\,i}\} & \cdots & Im\{s_k^{\,m}\} \end{bmatrix} & 0 & \cdots & 0 & \begin{bmatrix} -Re\{H_{1,1}(s_1)s_1^{\,0}\} & \cdots & -Re\{H_{1,1}(s_1)s_1^{\,m}\} \\ \vdots & & \vdots \\ -Re\{H_{1,1}(s_k)s_k^{\,0}\} & \cdots & -Re\{H_{1,1}(s_k)s_k^{\,m}\} \\ -Im\{H_{1,1}(s_1)s_1^{\,0}\} & \cdots & -Im\{H_{1,1}(s_1)s_1^{\,m}\} \\ \vdots & & \vdots \\ -Im\{H_{1,1}(s_k)s_k^{\,i}\} & \cdots & -Im\{H_{1,1}(s_k)s_k^{\,m}\} \end{bmatrix} \\
0 & \begin{bmatrix} Re\{s_1^{\,0}\} & \cdots & Re\{s_1^{\,m}\} \\ \vdots & & \vdots \\ Re\{s_k^{\,0}\} & \cdots & Re\{s_k^{\,m}\} \\ Im\{s_1^{\,0}\} & \cdots & Im\{s_1^{\,m}\} \\ \vdots & & \vdots \\ Im\{s_k^{\,i}\} & \cdots & Im\{s_k^{\,m}\} \end{bmatrix} & \cdots & \vdots & \begin{bmatrix} -Re\{H_{2,1}(s_1)s_1^{\,0}\} & \cdots & -Re\{H_{2,1}(s_1)s_1^{\,m}\} \\ \vdots & & \vdots \\ -Re\{H_{2,1}(s_k)s_k^{\,0}\} & \cdots & -Re\{H_{2,1}(s_k)s_k^{\,m}\} \\ -Im\{H_{2,1}(s_1)s_1^{\,0}\} & \cdots & -Im\{H_{2,1}(s_1)s_1^{\,m}\} \\ \vdots & & \vdots \\ -Im\{H_{2,1}(s_k)s_k^{\,i}\} & \cdots & -Im\{H_{2,1}(s_k)s_k^{\,m}\} \end{bmatrix} \\
\vdots & \vdots & \ddots & 0 & \vdots \\
0 & \cdots & 0 & \begin{bmatrix} Re\{s_1^{\,0}\} & \cdots & Re\{s_1^{\,m}\} \\ \vdots & & \vdots \\ Re\{s_k^{\,0}\} & \cdots & Re\{s_k^{\,m}\} \\ Im\{s_1^{\,0}\} & \cdots & Im\{s_1^{\,m}\} \\ \vdots & & \vdots \\ Im\{s_k^{\,i}\} & \cdots & Im\{s_k^{\,m}\} \end{bmatrix} \begin{bmatrix} -Re\{H_{N,N}(s_1)s_1^{\,0}\} & \cdots & -Re\{H_{N,N}(s_1)s_1^{\,m}\} \\ \vdots & & \vdots \\ -Re\{H_{N,N}(s_k)s_k^{\,0}\} & \cdots & -Re\{H_{N,N}(s_k)s_k^{\,m}\} \\ -Im\{H_{N,N}(s_1)s_1^{\,0}\} & \cdots & -Im\{H_{N,N}(s_1)s_1^{\,m}\} \\ \vdots & & \vdots \\ -Im\{H_{N,N}(s_k)s_k^{\,i}\} & \cdots & -Im\{H_{N,N}(s_k)s_k^{\,m}\} \end{bmatrix}
\end{bmatrix}$$

$$[X]=\begin{bmatrix} a_{0_{1,1}} & \cdots & a_{m_{1,1}} & a_{0_{2,1}} & \cdots & a_{m_{2,1}} & \cdots & a_{0_{N,N}} & \cdots & a_{m_{N,N}} & b_0 & \cdots & b_n \end{bmatrix}^T . \quad (6.4)$$

In Eqs. (6.3) and (6.4), each row uses an appropriate frequency scaling to obtain a well-conditioned matrix.

The coefficients of a column vector $[X]$ can be computed using a linear least squares approximation, where the number of samples 'k' should be no less than the unknown

coefficients ($m+n+2$), [47], [48]. In the linear least squares approximation [48], all data is uniformly weighted to compute the unknown coefficients. However, some data points need to be more accurate than others. For example, in the impedance parameters, values at peak resonant frequencies are more important than at null resonant frequencies. As a result, a more accurate scale is required for the impedance values in the vicinity of peak resonant frequencies. Using a weighted least squares approximation, it is possible to minimize the error at specific frequencies even though a larger error can be generated at other frequencies. Depending on the importance of data points, the appropriate data points can be captured more accurately by attaching weights to them. In this chapter, Y-parameters had more weights in the low frequency range and in the vicinity of specific frequencies at which the resonance of Z-parameters occurred. Using a weighted least squares approximation, Eqs. (6.2) and (6.3) can be rewritten as:

$$W_{Re}\left(\sum_{i=0}^{m} a_i\, Re\{s^i\} - \sum_{j=0}^{n} b_j\, Re\{H(s)s^j\}\right) = 0$$
$$W_{Im}\left(\sum_{i=0}^{m} a_i\, Im\{s^i\} - \sum_{j=0}^{n} b_j\, Im\{H(s)s^j\}\right) = 0 \qquad (6.5)$$
$$([W][A])^T [W][A][X] = [0]$$

where W_{Re} and W_{Im} are weighting matrices for real and imaginary parts, respectively. The weighting matrix is a diagonal matrix having 1 for normal points and a large value for weighed points. In this chapter, all the weighed points were set to 10.

6.2 Eigenvalue and Eigenvector Problem

The order of H(s) can be determined by solving the eigenvalues and the coefficients can be obtained from the eigenvector of the minimum eigenvalue [39], [41] as:

$$([W][A])^T [W][A][X] = l_{min}[X] \tag{6.6}$$

where $[A]^T$ is the transpose of the matrix A, and l_{min} is the minimum eigenvalue of the matrix A. Since the matrix A is already separated into the real and imaginary parts in Eq. (6.2), the matrix A is real, and its eigenvalues and eigenvectors are real. As the order of H(s) is increased, the minimum eigenvalue of the matrix A is decreased. As a result, the order of H(s) can be determined, and the unknown coefficients can be found as the eigenvector corresponding to $l_{min} \cong 0$ as described in [39]-[41]. However, a solution with eingenvalue l_{min} closer to zero does not mean that the solution is more accurate. If the order of the rational functions is overestimated, its Z-parameters can have more resonant frequencies or split resonant frequencies or be less accurate than the original data. Depending on the number of poles and frequency scaling, the eigenvector corresponding to the appropriate l_{min} should be selected for the solution. For the test case shown later, an eigenvector corresponding to $l_{min} \cong$ 1E-6 was chosen for the solution.

In addition, the solution does not guarantee the passivity of the macro-models. To make the models passive, constraints need to be applied to the rational functions, which will be discussed in the next section.

6.3 Enforcing Passivity for Macro-models

Power distribution networks are passive resonant structures which are linear and hence can only absorb and/or store energy. These networks return the stored energy to external networks. However, the transferred energy cannot exceed the stored energy in passive networks such as power distribution networks.

To enforce the necessary and sufficient conditions for the passivity of macro-models, the real part of Y, Z or S matrices must be semi-positive definite, meaning that all their eigenvalues are equal to or greater than zero [49]. By definition, the positive real matrix H(s) in Eq. (6.1) possesses the following properties [50], [51]

$$eigs\left(Re\{[H(s)]\}\right) \geq 0 \quad for\ all\ s \geq 0 \tag{6.7}$$

where $s = \sigma + jw$. In Eq. (6.7), σ is the real part of the complex frequency and can be chosen arbitrarily to ensure the convergence of the integration [52]. A given macro-model can therefore be tested to ensure that the real matrix H(s) satisfies the above condition. In Eq. (6.7), the transfer function matrix H(s) has a common denominator.

After the unknown coefficients are found using Eq. (6.6), partial fraction expansion is used to test the passivity and for obtaining the equivalent circuit models. Eq. (6.1) can be expressed in partial fraction expansion in the form:

$$H(s) = \underbrace{\sum_k \left(\frac{a + jb}{s + P_r - jP_i} + \frac{a - jb}{s + P_r + jP_i} \right)}_{Complex\ Conjugate\ Poles} + \underbrace{\sum_l \left(\frac{g}{s + P_{or}} \right)}_{Real\ Poles} + Ks. \tag{6.8}$$

Since all the real poles P_r and P_{or} in Eq. (6.8) have to be on the left half s-plane to ensure stability, the sign of the real poles on the right half s-plane needs to be changed. For preserving the passivity of the macro-models, the real part of all the complex conjugate and real pole-residue forms need to be tested using the enforced conditions described in [49]. In [49], the necessary and sufficient conditions for passivity have been explained and applied to rational functions.

The real and imaginary parts of the complex conjugate pole-residue form in Eq. (6.8) can be expressed as:

$$\begin{aligned} Re\{H(s)\}_{s=jw} &= \frac{2(aP_r - bP_i)(P_r^2 + P_i^2 - w^2) + 4aP_r w^2}{(P_r^2 + P_i^2 - w^2)^2 + 4P_r^2 w^2} \\ Im\{H(s)\}_{s=jw} &= \frac{2aw(-P_r^2 + P_i^2 - w^2) + 4bP_r P_i w}{(P_r^2 + P_i^2 - w^2)^2 + 4P_r^2 w^2}. \end{aligned} \tag{6.9}$$

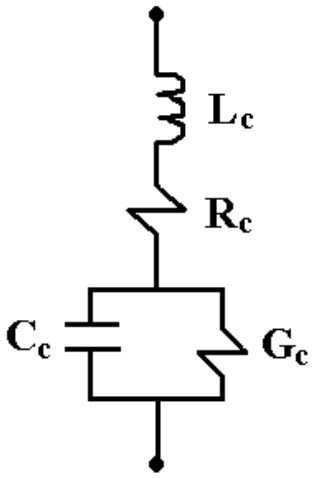
Since P_r, P_i, and w are constant for all the matrix elements of $Re\{H(s)\}$ in Eq. (6.9), the matrices $[a]$ and $[aP_r - bP_i]$ can be tested separately. If each matrix $[a]$ and $[aP_r - bP_i]$ is positive definite, then the sum of matrices $[a]$ and $[aP_r - bP_i]$ is also positive definite [48]. The matrix $[a]$ is first reset by changing negative eigenvalues of the matrix $[a]$ to zero [49], and the matrix $[b]$ is then recomputed by changing negative eigenvalues of the matrix $[aP_r - bP_i]$ to zero. The procedure for enforcing the passivity condition for the real pole-residue form in Eq. (6.8) is similar to the method explained earlier. The matrix $[g]$ is reset by changing negative eigenvalues of the matrix $[g]$ to zero [49]. Although the enforcement of the passivity condition generates

some error between the original and approximated data, macro-models need to satisfy these conditions if they are to be used for computing the transient response.

6.4 Equivalent Circuit Based on Y Parameters

The pole-residue form in Eq. (6.8) can be used to synthesize an equivalent circuit model using R, L, C and G circuit elements. The circuit model can be generated using either series or parallel representations since it is not unique, as has been mentioned earlier. In this section, Y-parameter based macro-models are converted into a circuit model using a parallel representation where all the pole-residue forms are connected in parallel.

From the complex conjugate pole-residue form in Eq. (6.8), R, L, C and G circuit elements can be extracted using P_r, P_i, a and b parameters, as shown in Fig. 6.2.



$$L_c = \frac{1}{2\alpha}$$

$$R_c = \frac{\alpha P_r + \beta P_i}{2\alpha^2}$$

$$C_c = \frac{2\alpha^3}{(\alpha^2 + \beta^2)P_i^2}$$

$$G_c = \frac{2\alpha^2(\alpha P_r - \beta P_i)}{P_i^2(\alpha^2 + \beta^2)}$$

Fig. 6.2. Equivalent circuit for complex conjugate pole-residue form.

From the real pole-residue form in Eq. (6.8), R and L circuit elements can be represented using P_{or} and g, as shown in Fig. 6.3.

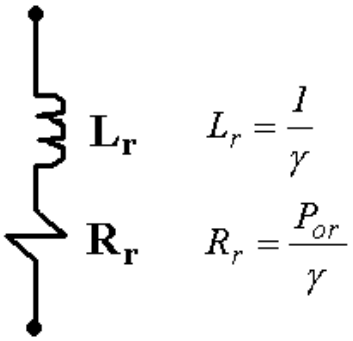


Fig. 6.3. Equivalent circuit for real pole-residue form.

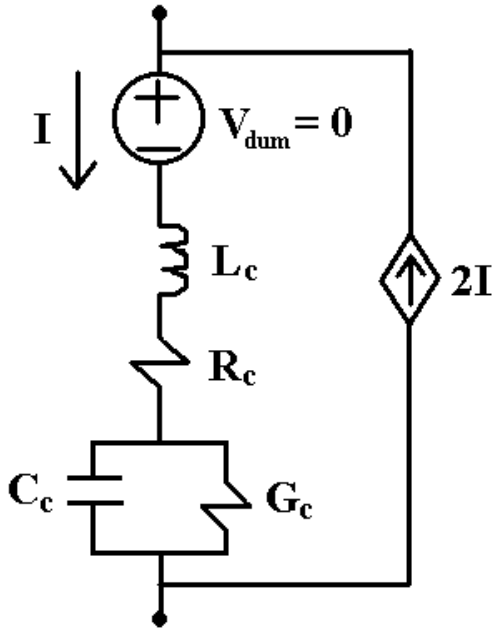
In Eq. (6.8), parameter 'K' is the stand-alone capacitance. As mentioned earlier, all the pole-residue forms are connected in parallel using Y-parameter based macro-models. It is important to note that the macro-models can also be converted into series network representations.

A circuit model based on the equivalent circuits shown in Figs. 6.2 and 6.3 can be implemented using the following equation

$$I_i = \sum_j Y_{ij}(s) V_j \tag{6.10}$$

where $Y_{ij}(s)$ is the admittance matrix which is converted into the equivalent circuits shown in Figs 6.2, and 6.3, I_i and V_i are the current and voltage at Port 'i', respectively. In [43], based on Eq. (6.10), an equivalent circuit model has been implemented in SPICE using dependent voltage and current sources. However, it requires many circuit elements and dependent sources for generating the full Y matrix, and uses absolute grounds for the reference points at all ports.

Using Eq. (6.10) and the property that the matrix of linear passive networks is symmetric and reciprocal ($Y_{ij} = Y_{ji}$), it is possible to reduce circuit elements and to construct a direct circuit model. It requires the triangular matrix of Y and a few dependent current-controlled current sources to represent negative inductances, as shown in Fig. 6.4. It is important to note that SPICE cannot read the negative inductances, hence the need for the dependent sources. As an example, while 16 circuit elements, 2 dependent current-controlled current sources in the self admittance term (Y_{ii}, Y_{jj}), and 2 dependent voltage-controlled voltage sources in the transfer admittance term (Y_{ij}, Y_{ji}) are required to represent one complex conjugate pole-residue form for a 2-port system (2×2 matrix) in [43], the direct circuit model only requires 12 circuit elements. In addition, the direct circuit model can use either absolute or local grounds for the reference points of all ports without increasing the number of ports.



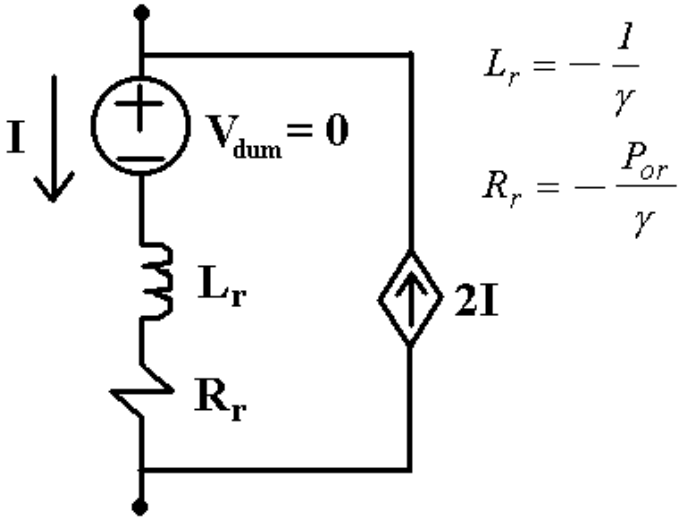
$$L_c = -\frac{1}{2\alpha}$$

$$R_c = -\frac{\alpha P_r + \beta P_i}{2\alpha^2}$$

$$C_c = -\frac{2\alpha^3}{(\alpha^2+\beta^2)P_i^2}$$

$$G_c = -\frac{2\alpha^2(\alpha P_r - \beta P_i)}{P_i^2(\alpha^2+\beta^2)}$$

(a)



(b)

Fig. 6.4. Equivalent circuit for negative inductance: (a) complex conjugate and (b) real pole-residue forms.

In Eq. (6.10), while the transfer admittance terms with opposite signs are needed to convert into a circuit representation, the self admittance terms have been rearranged to interact with the transfer admittance terms. Using the transfer admittance terms, the self admittance terms can be represented as

$$\begin{aligned} Y_{ii} &= \tilde{Y}_{ii} - \sum_j Y_{ij} \quad ; \; i \neq j \\ \tilde{Y}_{ii} &= Y_{ii} + \sum_j Y_{ij} \end{aligned} \tag{6.11}$$

where $\tilde{Y}_{ii}$ is a part of the self admittance term (Y_{ii}). The term $\tilde{Y}_{ii}$ is now needed for conversion into a circuit representation. Based on the circuit representations of $\tilde{Y}_{ii}$ and Y_{ij}, the overall circuit model for a macro-model can be implemented for a 3-port system, as shown in Fig. 6.5.

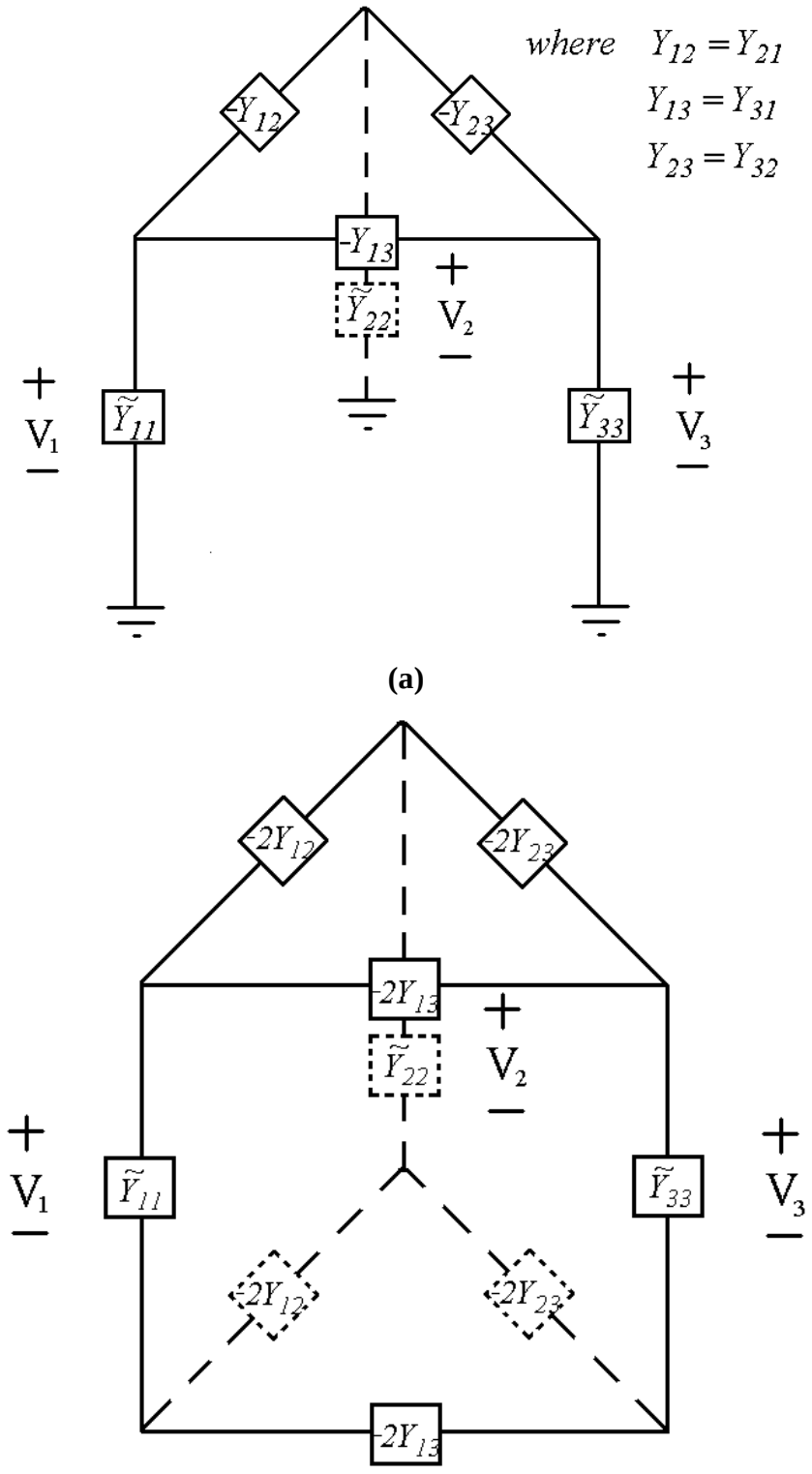


Fig. 6.5. Overall circuit model for Y parameters using (a) absolute and (b) local grounds.

In Fig. 6.5 (b), an absolute ground is the reference point at a DC source location. While simulating power distribution networks, local grounds are necessary and this is possible using the representation in Fig. 6.5 (b). Compared with Z or S parameters, Y parameters can be easily converted into a circuit model with a small number of circuit elements, as shown in Fig. 6.5.

In this section, a method was presented for generating a network representation of Y-parameter based macro-models, using a reduced number of circuit elements. This representation enables the transient simulation of linear networks such as power distribution networks in the presence of non-linear drivers. In the next section, the method developed in this chapter is applied for modeling the image processing board from Kodak.

6.5 Test Case: Irregular Shaped Power/Ground Planes in Kodak board

As an example, the Kodak power distribution network in Fig. 5.2 was simulated using the Y-parameter macro-modeling method described in this chapter. The structure in Fig. 5.2 is complicated, electrically large, and shows multiple resonances over the frequency bandwidth of interest. A two-port macro-model with common poles was generated based on the simulated data from 50 MHz to 3 GHz, for the response between Ports 1 and 2, as described in Fig. 5.2. The rational function based macro-model was generated with m = 16 and n = 15 for numerator and denominator orders in Eq. (6.1) by capturing the poles of the Y matrix. The extracted poles were at the following frequencies: 618.9 MHz, 1.198 GHz, 1.728 GHz, 1.947 GHz, 2.219 GHz, 2.758 GHz and 3.237 GHz. The rational

function based macro-model was decomposed into the partial fraction expansion form in Eq. (6.8) having 7 complex conjugate pole-residues, 1 real pole-residue and 1 capacitor. All the unknown parameters in Eq. (6.8) were computed, as shown in Table 6.1.

Table 6.1

Unknown Parameter for Kodak Power Distribution Network

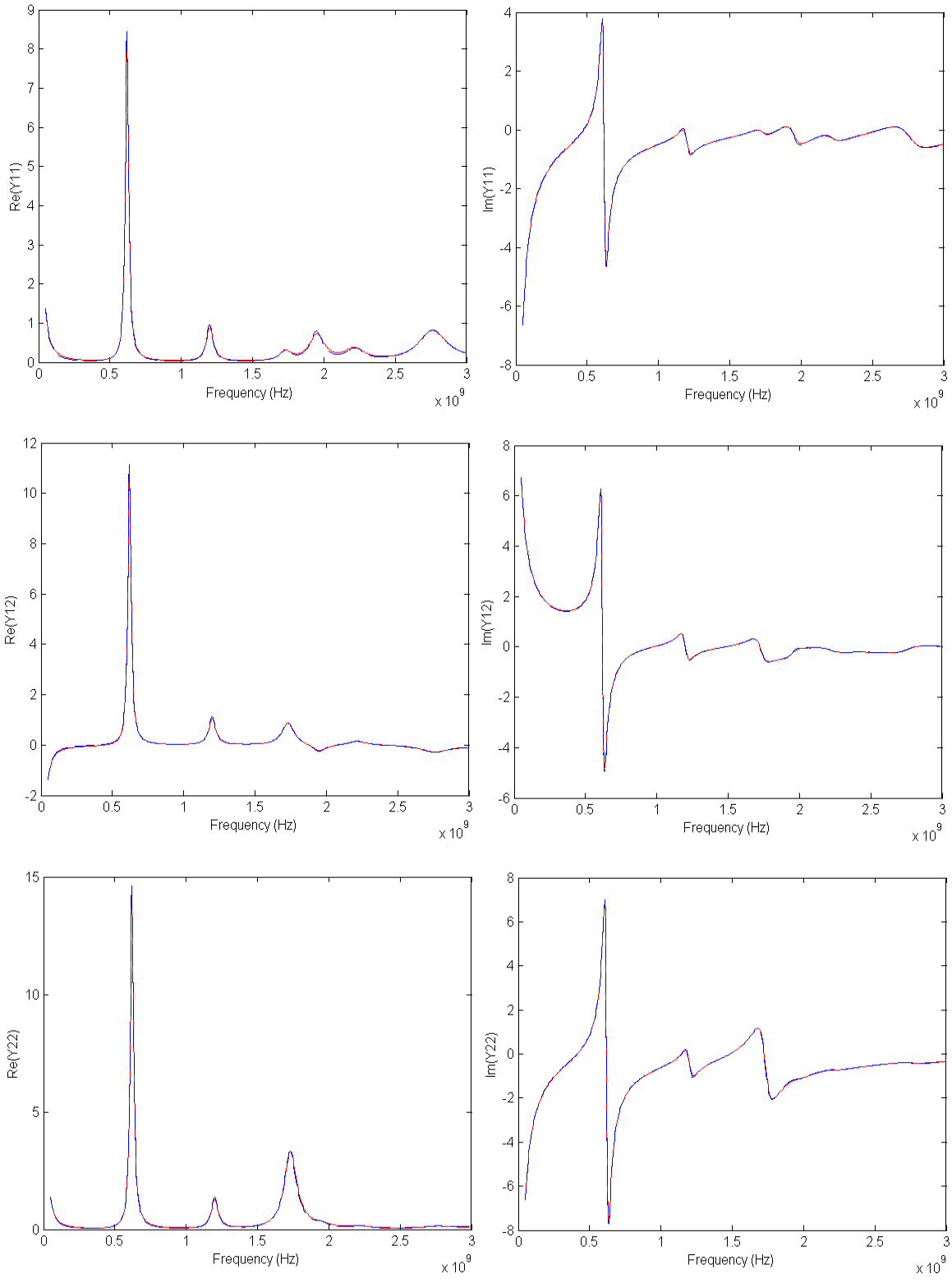
		Y11		Y12		Y22	
P_r	P_i	α_{11}	β_{11}	α_{12}	β_{12}	α_{22}	β_{22}
1.582E+09	2.034E+10	1.847E+08	1.436E+07	-1.452E+08	-1.129E+07	2.694E+08	2.095E+07
7.638E+08	1.733E+10	5.980E+08	2.635E+07	-2.116E+08	-9.326E+06	7.508E+07	3.309E+06
4.693E+08	1.394E+10	1.406E+08	-1.779E+06	7.823E+07	-6.428E+05	4.355E+07	-1.241E+05
3.330E+08	1.223E+10	2.460E+08	7.115E+06	-1.045E+08	-2.370E+06	4.788E+07	6.656E+05
3.264E+08	1.086E+10	8.335E+07	2.506E+06	2.928E+08	8.802E+06	1.079E+09	3.243E+07
1.714E+08	7.528E+09	1.616E+08	3.746E+06	1.913E+08	4.364E+06	2.265E+08	5.082E+06
8.393E+07	3.888E+09	7.153E+08	1.718E+07	9.430E+08	2.073E+07	1.243E+09	2.491E+07
P_{or}		γ_{11}		γ_{12}		γ_{22}	
6.426 E+07		2.185 E+09		2.185 E+09		2.185 E+09	
		K_{11}		K_{12}		K_{22}	
		3.316 E-12		1.259 E-12		3.416 E-12	

The pole-residue form in Table 6.1 can be represented as 93 R, L, C and G circuit elements with 6 dependent current-controlled current sources, as shown in Fig. 6.5 (a), or 124 R, L, C and G circuit elements and 10 dependent current-controlled current sources as in Fig. 6.5 (b). Compared with the method described in the previous chapter which requires over 100,000 elements, the generated macro-model for the 2 port system uses far fewer circuit elements.

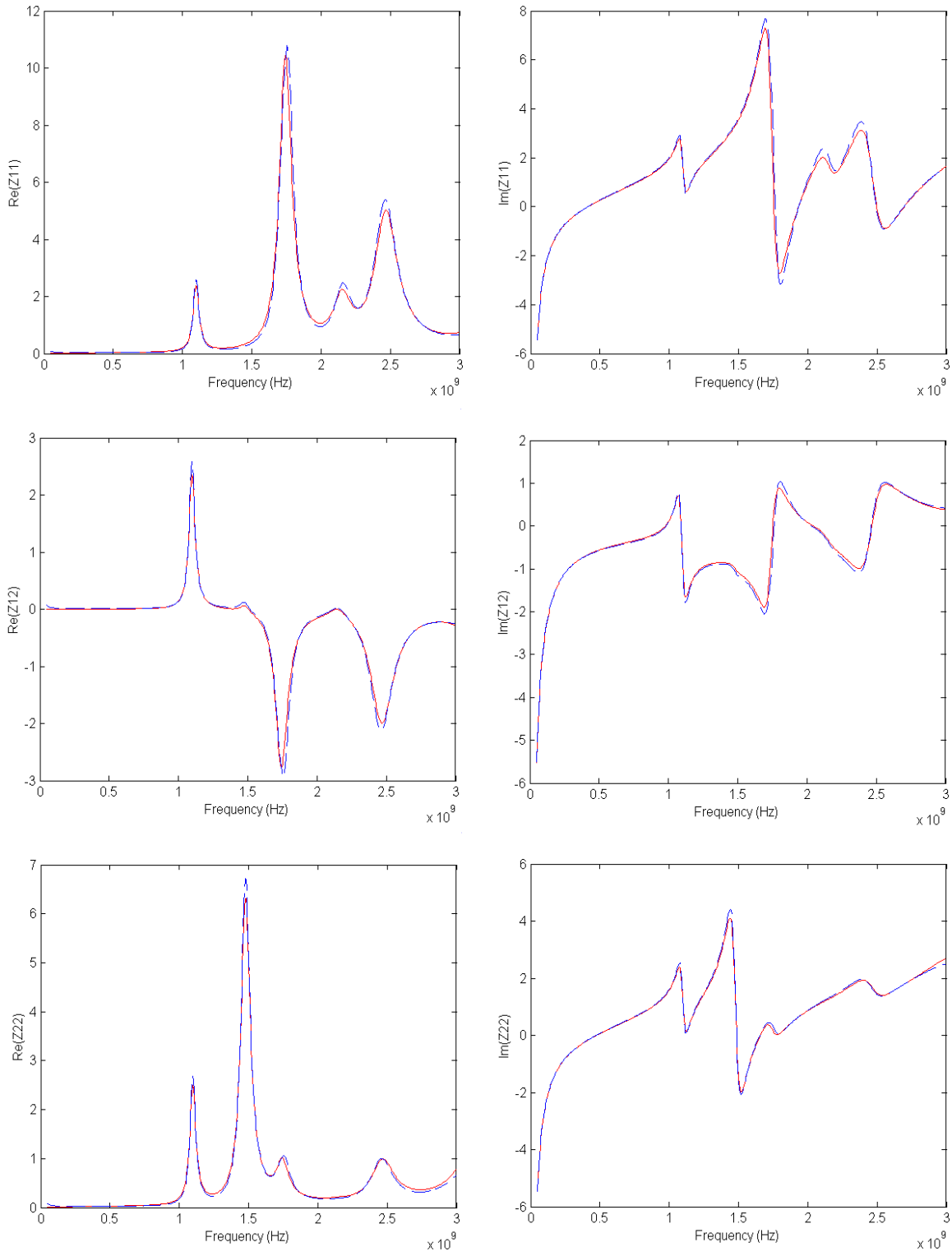
The frequency response for the Y-parameter based macro-model and the transmission matrix method are compared in Fig. 6.6. It is important to note that Z-parameters should be checked even if Y-parameters for the original data and macro-model are close, as

mentioned earlier. Since the sensitivity of the error for Y-parameters is high and the poles of Y parameters are not those of Z parameters, the macro-model based on Y-parameters does not always guarantee the accuracy of Z-parameters. This is especially true for resonant networks.

To check the accuracy of the macro-model in the time domain, the transient response for the original data was obtained using the IDFT described in Eq. (4.8) while the response for the macro-model was generated using SPICE. A unit step voltage pulse having a rise time of 1 ns was injected into Port 1 on the plane, and the voltage output was measured at Port 2. Fig. 6.7 shows the comparison of the transient simulation results using the two methods, which exhibits good agreement. However, the response in the steady state, which is marked by a dashed circle in Fig 6.7 (b), shows a small discrepancy between the two results. This is due to the error at low frequencies and some resonant frequencies, as shown in Fig. 6.6 (b), which were generated by the enforcement of the passivity condition. The damped oscillating response in Fig. 6.7 demonstrates that the model is indeed passive.

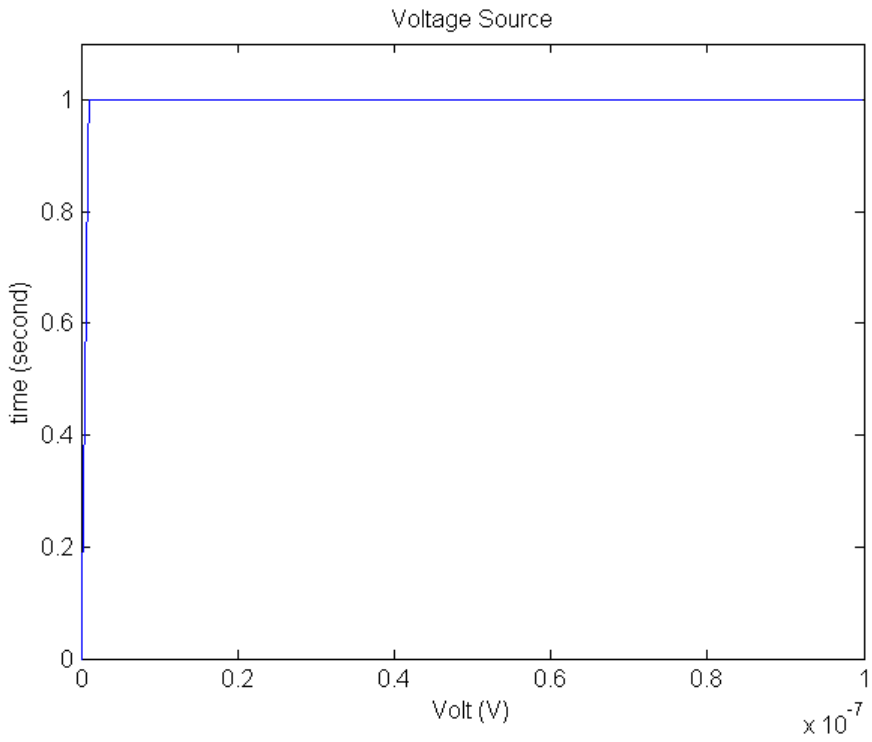

Re(Y11)
Frequency (Hz)
x 10^9
Im(Y11)
Frequency (Hz)
x 10^9
Re(Y12)
Frequency (Hz)
x 10^9
Im(Y12)
Frequency (Hz)
x 10^9
Re(Y22)
Frequency (Hz)
x 10^9
Im(Y22)
Frequency (Hz)
x 10^9

(a)

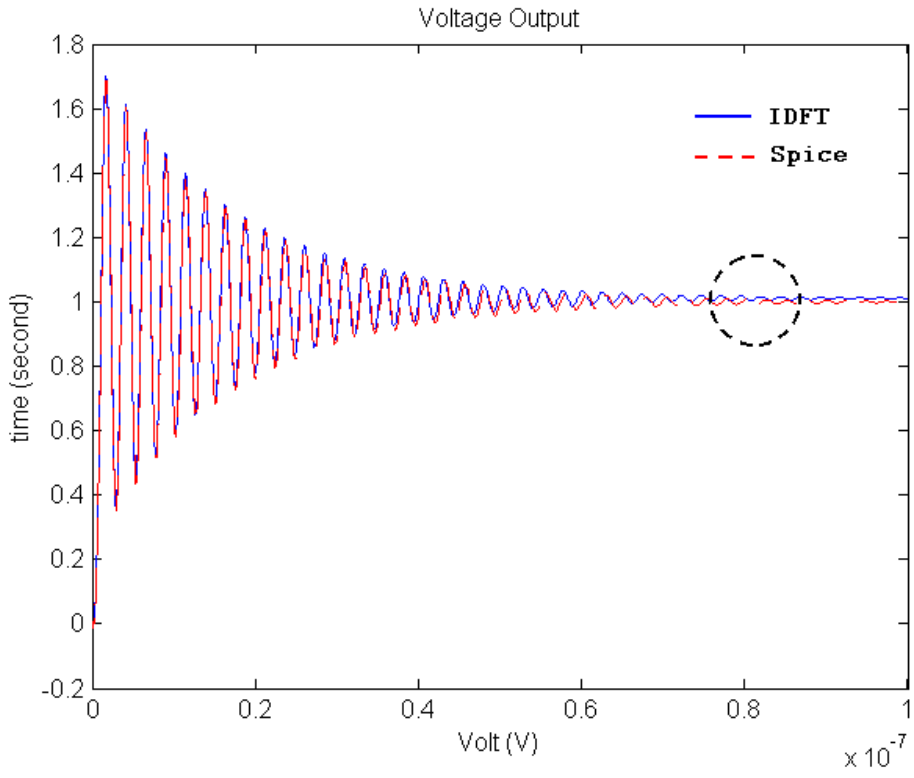


(b)

Fig. 6.6 Comparison between the original (solid) and macro-modeling (dashed) data for (a) Y and (b) Z-parameters.



(a)



(b)

Fig. 6.7 Transient response: (a) voltage source and (b) voltage output.

6.6 Summary

In this chapter, a method for generating rational function based macro-models was discussed. The rational functions were computed using a weighted least squares approximation and by solving an eigenvalue problem. Compared with the method of average least squares approximation, the method of weighted least squares approximation has an advantage for controlling the error at specific points in the frequency response. To ensure the passivity of macro-models, the necessary and sufficient conditions for passivity were enforced by making the real part of the Y matrix positive definite. Though this introduced some error, the models guaranteed passivity.

In this chapter, Y-parameter based equivalent circuits from macro-models were developed for enabling transient simulation. The method reduced the number of circuit elements compared with other methods in the literature. The method presented is ideally suited for networks where the number of ports is limited to 10 and the number of poles does not exceed 20.

However, when an electrically large system consisting of multiple resonances and requiring a large number of ports is modeled, a large matrix ‘A’ in Eq. (6.4) needs to be solved. This can be a problem due to limited computer resources and due to the ill-conditioned matrix in Eq. (6.4). In the next chapter, to solve these kinds of problems, the macro-modeling method has been modified to one based on Z parameters that uses direct mapping, instead of a least squares approximation.

CHAPTER 7

Macro-modeling using Direct Mapping Method

In the computation of Y and S parameters, as the number of ports increases, the ports interact with each other, causing a change in the resonance characteristics. However, Z parameters do not change even if the number of ports increases. For power distribution networks, applying a least squares approximation by solving an eigenvalue problem for Z parameters is not straightforward since the frequency response has large variations in amplitude, making it difficult to capture its behavior at both DC and high frequencies. In addition, if a large number of unknown coefficients need to be solved, the ill-conditioned nature of the matrix 'A' in Eq (6.4) can create problems. Moreover, it is almost impossible to apply the least squares approximation for a large number of ports, especially if a common set of poles are desired.

In this chapter, the macro-modeling of the Z matrix for multi-port systems and its circuit implementations are discussed. The macro-models based on the Z parameters have been simulated with nonlinear switching circuits and transmission line interconnects. Theses methods have been applied to complex structures for computing the simultaneous switching noise. The examples discussed in this chapter include the test vehicles from Sun Microsystems and IBM.

7.1 Direct Mapping Method

While the weighted least squares approximation was used to find the unknown coefficients in Eq. (6.8) in the previous chapter, they can be computed directly from the frequency response of the Z matrix. This is possible by using the relation between the frequency response and the partial fraction expansion in Eq. (6.8). Assuming all ports have common poles, which means that all the Z parameters have the same P_r, P_i and P_{or} in Eq. (6.8), the Z parameters for a multi-port circuit can be summed together and written as:

$$Z_{sum} = \sum_i \sum_j Z_{ij}(s) \tag{7.1}$$

where 'i' and 'j' are the notation for Ports i and j, respectively. In Eq (7.1), Z_{sum} contains the common P_r, P_i and P_{or} parameters. From Eq. (7.1), all the poles in a system can be computed accurately.

From $Re\{Z_{sum}\}$ in Eq. (7.1), P_i for the complex conjugate pole-residue form in Eq. (6.8) can be found first, as described in Fig. 7.1. As shown in Fig. 7.1, P_i is the radian frequency where the maximum value of $Re\{Z_{sum}\}$ occurs. For accurate determination of P_i, enough data points need to be sampled. If the sampling points are insufficient, rational function interpolation can be used to search for P_i [53].

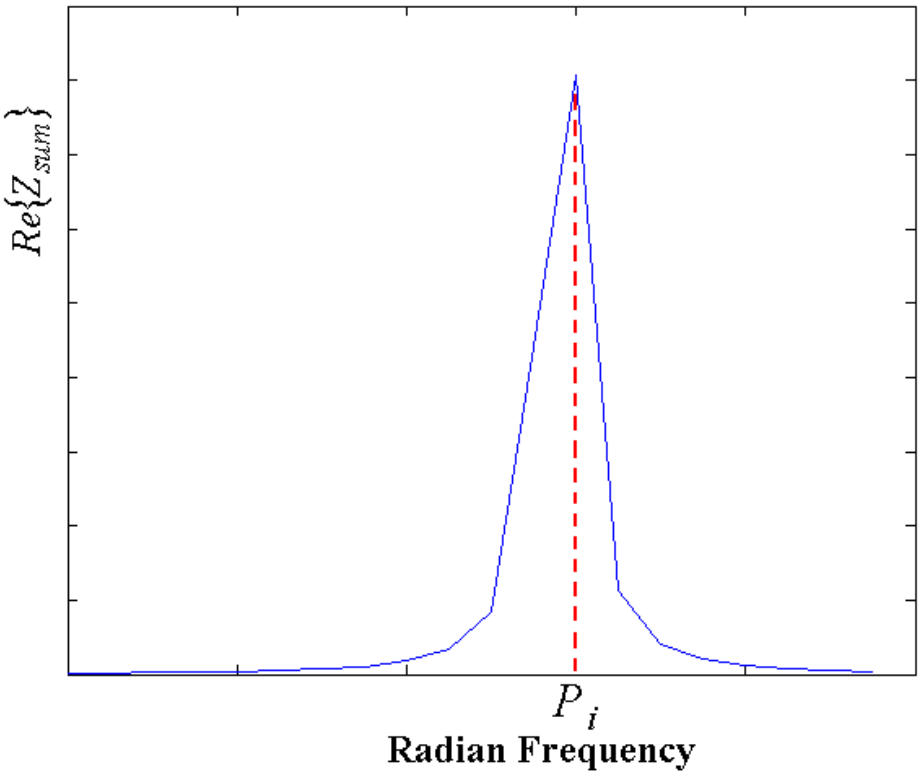


Fig. 7.1. Detection of the imaginary part of complex conjugate pole.

Next, the parameter P_r can be approximated from Eq. (7.1) using $Im\{Z_{sum}\}$. The details for capturing P_r are shown in Fig. 7.2. For accuracy, rational-function interpolation was also applied near the points of interest, as mentioned earlier. Based on P_i and w_r in Fig. 7.2, the parameter P_r can be approximated as follows:

$$P_r \cong w_r - P_i \,. \tag{7.2}$$

In Eq. (7.2), w_r is always larger than P_i. As a result, the real part of the complex conjugate pole in Eq. (6.8), which is negative P_r, is on the left half s-plane. This automatically satisfies the stability condition.

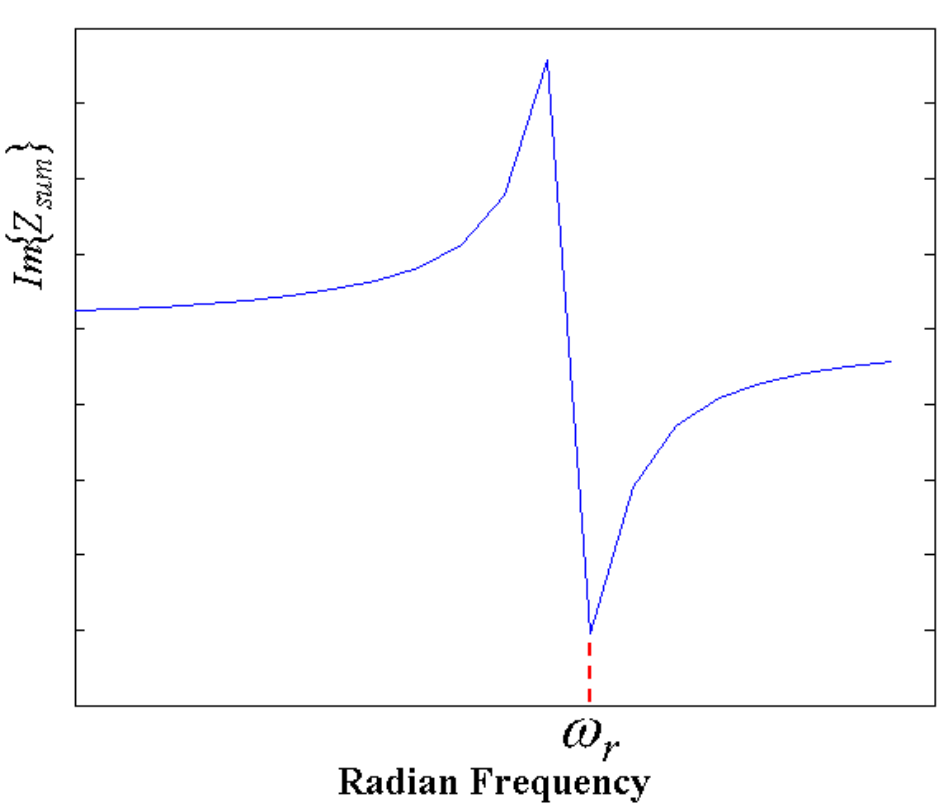


Fig. 7.2. Detection of the real part of complex conjugate pole.

After the parameters P_r and P_i are found, the parameters a and b for each Z parameter can be computed using Eq. (6.9). Based on the original data at a specific radian frequency w, the parameters a and b can be calculated as follows:

$$\begin{aligned} a_{ij} &= P_r \, Re\left\{Z_{ij}(w = \sqrt{P_r^2 + P_i^2})\right\} \\ b_{ij} &= \frac{P_r P_i \, Im\left\{Z_{ij}(w = \sqrt{P_i^2 - P_r^2})\right\}}{P_i^2 - P_r^2}. \end{aligned} \tag{7.3}$$

For obtaining better accuracy, computation for the unknown parameters in the complex pole-residue pairs needs to be done from high to low frequency. After the

parameters are computed for a complex pole-residue pair, Z_{sum} and Z parameters are updated for the next complex pole-residue pair by recursively subtracting the complex pole-residue pair computed in the previous step.

After all the complex pole-residue pairs are computed, the real pole-residue pairs need to be computed. For computing the real pole-residue pairs, only low frequency data up to the first null resonant frequency (capacitance region) is required. The low frequency data is obtained by subtracting all the complex pole-residue pairs from the original data. The real pole-residue pairs can be obtained by using average least squares approximation. In general, the real pole can be represented sufficiently well using a first order approximation. However, the order can be increased for obtaining a better accuracy, if desired.

In this chapter, the first order real pole has been used. Since the matrix 'A' in Eq. (6.3) is set as the first order pole, the size of the matrix is small even for a large number of ports, which alleviates the problems described in the previous chapter. After the real pole-residue pair is computed, it is subtracted from the frequency response for computing the inductance term 'K' in Eq. (6.8). This is the stand-alone capacitance while modeling with Y parameters. The inductance term can also be obtained by using average least squares approximation.

While the real pole-residue pair and inductance term can be calculated accurately, the complex pole-residue pairs need to be computed more accurately since the coefficients that have been obtained through Eqs. (7.1) to (7.3) are based on the data that includes the response of the real pole-residue pair and inductance term. Hence, it is necessary to re-compute the complex pole-residue pairs. All the complex pole-residue forms are initially

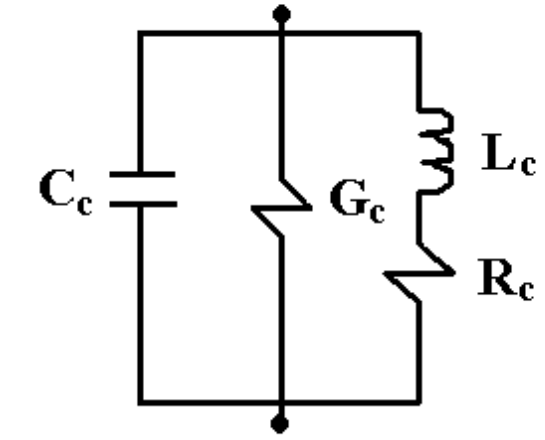
discarded, and then it is assumed that only the real pole-residue pair and inductance term exist. From the original data Z_{sum} in Eq. (7.1), the frequency response from the real pole-residue pair and inductance term are subtracted. Then, all the computations for the complex pole-residue pair are repeated using the procedure described in Eqs. (7.1) to (7.3).

The unknown coefficients (P_i, P_r, a and b) for each complex pole-residue pair are computed based on four data points which are passive. For guaranteeing that the Z-parameter based macro-models are passive, each complex pole-residue pair and the real pole-residue pair are tested by using the conditions of passivity described in Chapter 6.3 and appropriately modified.

7.2 Equivalent Circuit Based on Z Parameters

While parallel equivalent circuits can be efficiently implemented for Y parameters, Z parameters require series equivalent circuit implementations. All the circuit implementations for complex pole-residue forms and real pole residue forms and inductance terms are therefore connected in series.

From the complex conjugate pole-residue form in Eq. (6.8), R, L, C and G circuit elements can be directly represented using P_r, P_i, a and b, as shown in Fig. 7.3. For the transfer impedance terms, negative circuit elements can be generated while constructing the equivalent circuits. To represent negative inductances, a dependent voltage-controlled voltage source is needed for computing the transient response in SPICE.



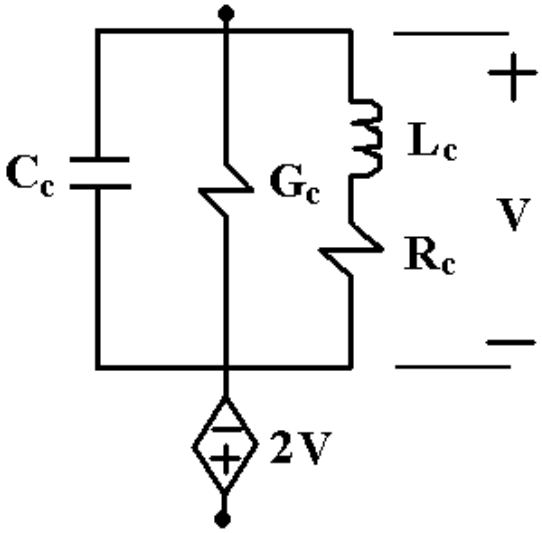
$$C_c = \frac{1}{2\alpha}$$

$$G_c = \frac{\alpha P_r + \beta P_i}{2\alpha^2}$$

$$L_c = \frac{2\alpha^3}{(\alpha^2 + \beta^2)P_i^2}$$

$$R_c = \frac{2\alpha^2(\alpha P_r - \beta P_i)}{P_i^2(\alpha^2 + \beta^2)}$$

(a)



$$C_c = -\frac{1}{2\alpha}$$

$$G_c = -\frac{\alpha P_r + \beta P_i}{2\alpha^2}$$

$$L_c = -\frac{2\alpha^3}{(\alpha^2 + \beta^2)P_i^2}$$

$$R_c = -\frac{2\alpha^2(\alpha P_r - \beta P_i)}{P_i^2(\alpha^2 + \beta^2)}$$

(b)

Fig. 7.3. Equivalent circuit for complex conjugate pole-residue form: (a) positive inductance and (b) negative inductance.

From the real pole-residue form in Eq. (6.8), R and L circuit elements can be represented using P_{or} and g, as shown in Fig. 7.4.

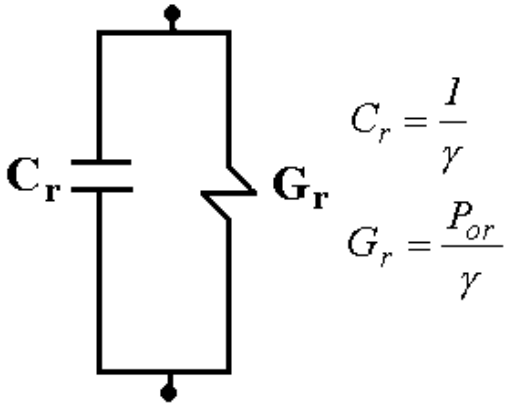


Fig. 7.4. Equivalent circuit for real pole-residue form.

In Eq. (6.8), 'K' is the stand-alone inductance for Z-parameter based macro-models, as mentioned earlier. It is important to note that all the pole-residue forms are connected in series for the above circuit implementation.

A circuit model based on the equivalent circuits shown in Figs. 7.3 and 7.4 can be implemented using the following equation

$$V_i = \sum_j Z_{ij}(s) I_j \tag{7.4}$$

where $Z_{ij}(s)$ is the impedance matrix which is converted into the equivalent circuits shown in Figs 7.3, and 7.4, V_i and I_i are the voltage and current at Port 'i', respectively. Based on Eq. (7.4), an equivalent circuit model can be implemented in SPICE using dependent voltage-controlled voltage sources and dependent current-controlled current sources. Compared with Y-parameter based circuit implementations shown in Fig. 6.5, Z-parameter based circuit implementations require circuit elements and dependent sources for the full Y matrix, and use absolute grounds for the reference points at all ports, as

shown in Fig. 7.5. However, local ground for reference points can be represented by doubling the number of ports. This is important for simulating power supply noise.

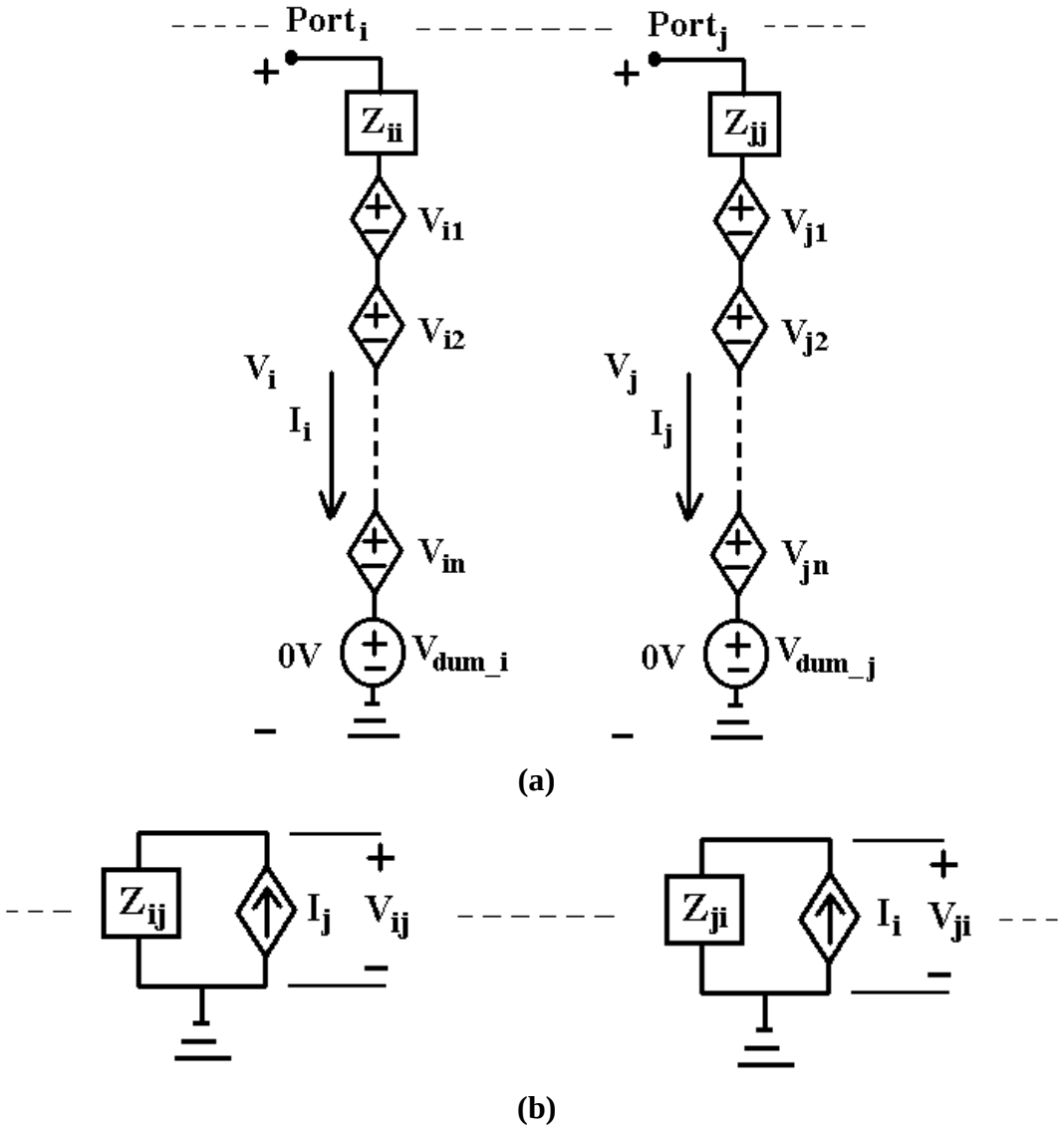


Fig. 7.5. Overall circuit model for (a) self impedance term and (b) transfer impedance term.

Using the direct mapping method, Z-parameter based macro-models can be implemented with ports for the DC source, reference points for I/O interconnects and output ports [31]. In the next section, two test vehicles have been simulated using the

transmission matrix method and the Z-parameter based macro-modeling method described in this chapter. The transmission matrix method has been used to compute the frequency response which has been captured using the macro-models to develop a circuit representation in SPICE. For computing simultaneous switching noise, interconnects and switching circuits in the presence of packages and boards have been analyzed.

7.3 Test Cases

7.3.1 Test Case 1: Test Vehicle from Sun Microsytems

A test vehicle (TV2B) was designed and fabricated by Sun Microsytems for analyzing simultaneous switching noise. Even though this test vehicle was analyzed using the cavity resonator method in [31], the methods described in this dissertation have been applied to verify the accuracy of the methods described in this chapter.

Fig. 7.6 shows the test vehicle consisting of multi-layered planes, I/O interconnects and non-linear switching circuits, with details in [31]. It is a seven-layered board with interconnects consisting of four wide microstrip transmission lines with $Z_0 = 22\ W$. The stackup of the test vehicle includes 4 power/ground planes and 3 signal layers in the order: sig1/vdd1/gnd1/sig2/sig3/vdd2/gnd2, as shown in Fig. 7.6. All the power/ground plane pairs have dimensions of 20 inch by 0.3 inch, which are very narrow and behave as transmission lines. The transmission lines in the signal layers have the same length as the power/ground planes and a width of 30 mils, and are driven by Texas Instrument ABT244 buffer drivers. The dielectric separation is 4 mils of FR4 with relative permittivity e_r = 4.7 between all copper layers except sig2 and sig3 where the separation is 24 mils. Four silicon drivers are located on the left side of the test vehicle in a 20 pin

DIP package. They were powered from vdd1 and gnd1 planes, using vias. Two sets of 50-ohm stripline transmission lines were embedded between gnd1 and vdd2 planes. The sig2 layer is one set of striplines that is close to the gnd1 plane while the other set in the sig3 layer (designated Strip5, Strip6, Strip7, Strip8) is close to the vdd2 plane. The two power planes and two ground planes were connected together on the right side of the test vehicle, while they are not connected on the left side. This enables independent voltage measurements on the left side between the vdd1 and gnd1 planes, vdd2 and gnd1 planes, and the vdd2 and gnd2 planes, where the differential voltages are named PP1, PP2 and PP3, respectively.

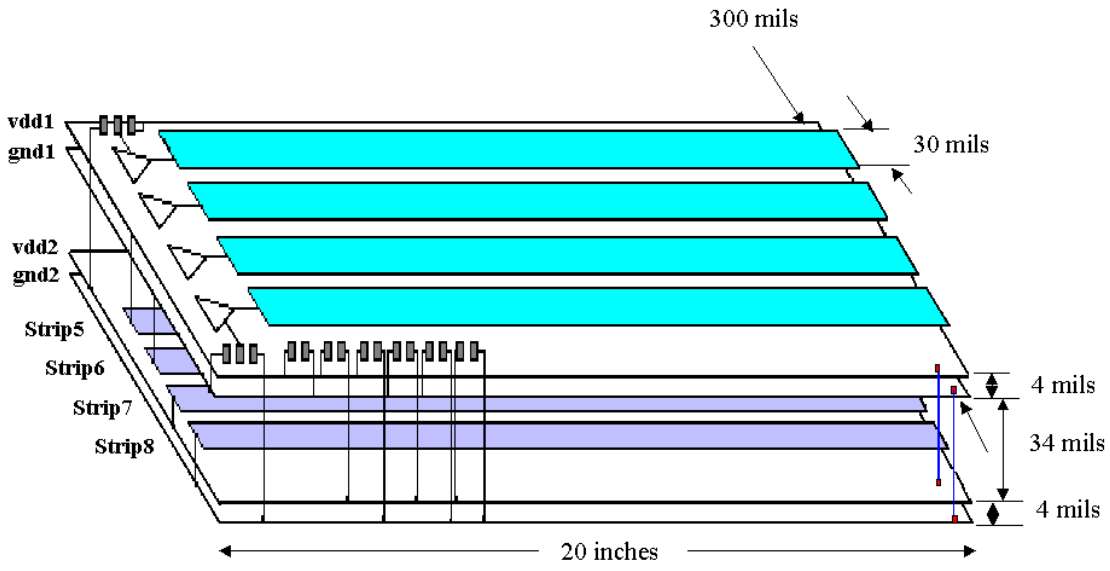


Fig. 7.6. Test vehicle from Sun Microsystems.

In the frequency domain, the transmission matrix method was applied to compute each 2×2 impedance matrix between the ports on the right and left sides of the test vehicle for the vdd1/gnd1, vdd1/gnd2 and vdd2/gnd2 planes. Figs. 7.7 and 7.8 show the impedance response for the vdd1/gnd1 and vdd2/gnd2 planes, respectively. As mentioned

in Chapter 1.4.3, both the vdd1/gnd1 and vdd2/gnd2 planes have the smaller amplitude in the frequency response as compared to vdd2/gnd1 planes. However, all the three-power/ground plane pairs have the cavity resonances at the same frequencies. In addition, the self impedances at the two ports for each power/ground plane pair are the same since the planes are symmetric.

After obtaining the frequency response using the transmission matrix method, the impedance response was used as look-up data for constructing the equivalent circuits using the Z-parameter based macro-model. The frequency response for Z-parameters using the macro-modeling method described in this chapter and the transmission matrix method are compared in Figs. 7.7 and 7.8. The test vehicle shown in Fig. 7.6 has multiple resonances over the frequency bandwidth of interest. Two Z-parameter based macro-models with common poles were generated based on the simulated data from 1 MHz to 1 GHz between the two ports both on the vdd1/gnd1 and vdd2/gnd1 planes. The rational function for both the vdd1/gnd1 and vdd2/gnd1 planes was generated with m = 16 and n = 15 for numerator and denominator orders in Eq. (6.1) by capturing the poles of the Z matrix at 135.84 MHz, 272.04 MHz, 408.16 MHz, 544.28 MHz, 680.28 MHz, 816.28 MHz and 952.28 MHz. As mentioned earlier, the two-dimensional power/ground planes behave as one-dimensional transmission lines since the power/ground planes are narrow in width and long in length. The resonant frequencies occur at regular intervals. The rational functions for both the power/ground plane pairs were decomposed into the partial fraction expansion form in Eq. (6.8) having 7 complex conjugate pole-residues, 1 real pole-residue and 1 inductor. All the unknown parameters in Eq. (6.8) were computed as shown in Tables 7.1 and 7.2.

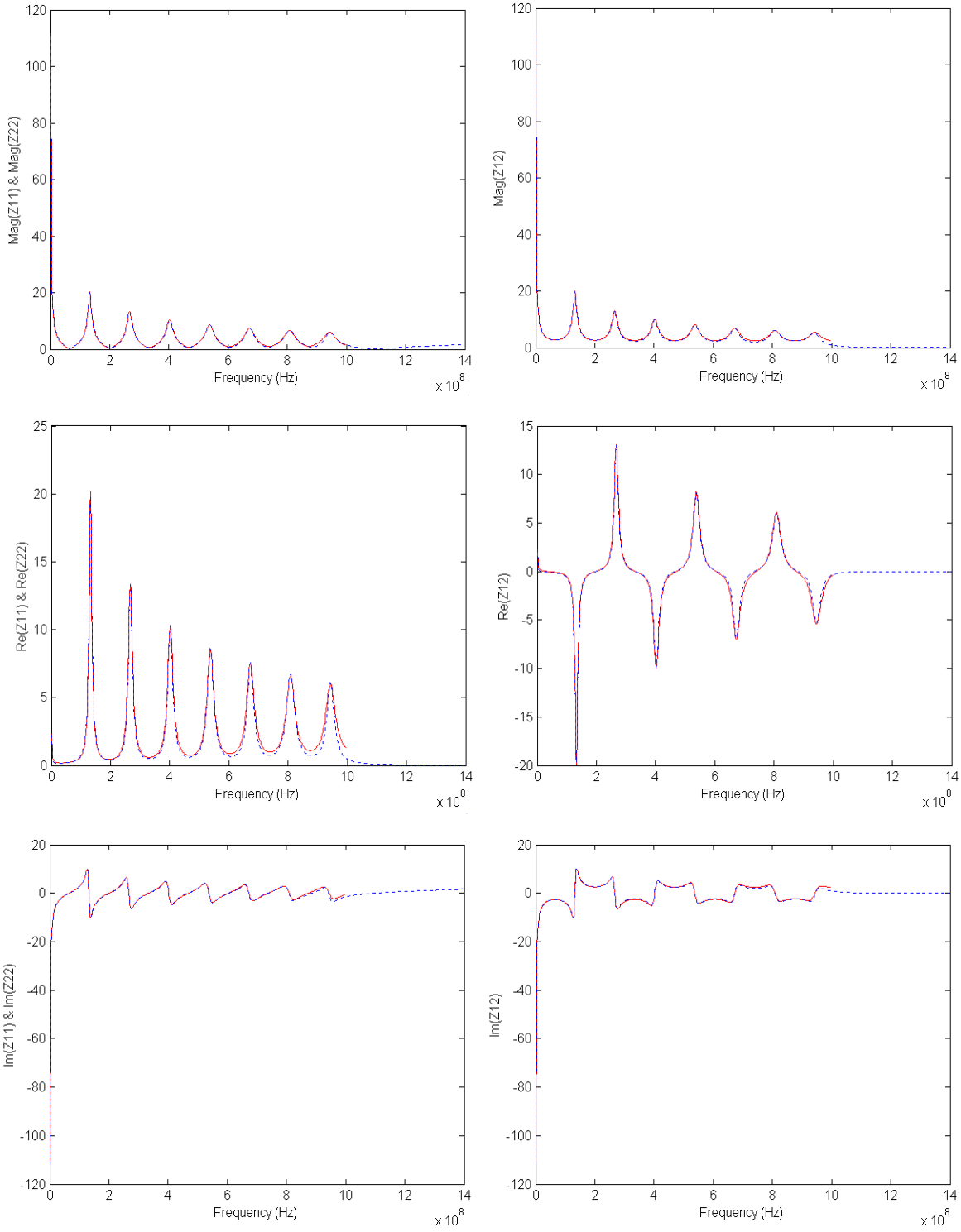


Fig. 7.7. Impedance response for both the vdd1/gnd1 and vdd2/gnd2 planes computed by transmission matrix method (solid) and Z-parameter based macro-modeling method (dashed).

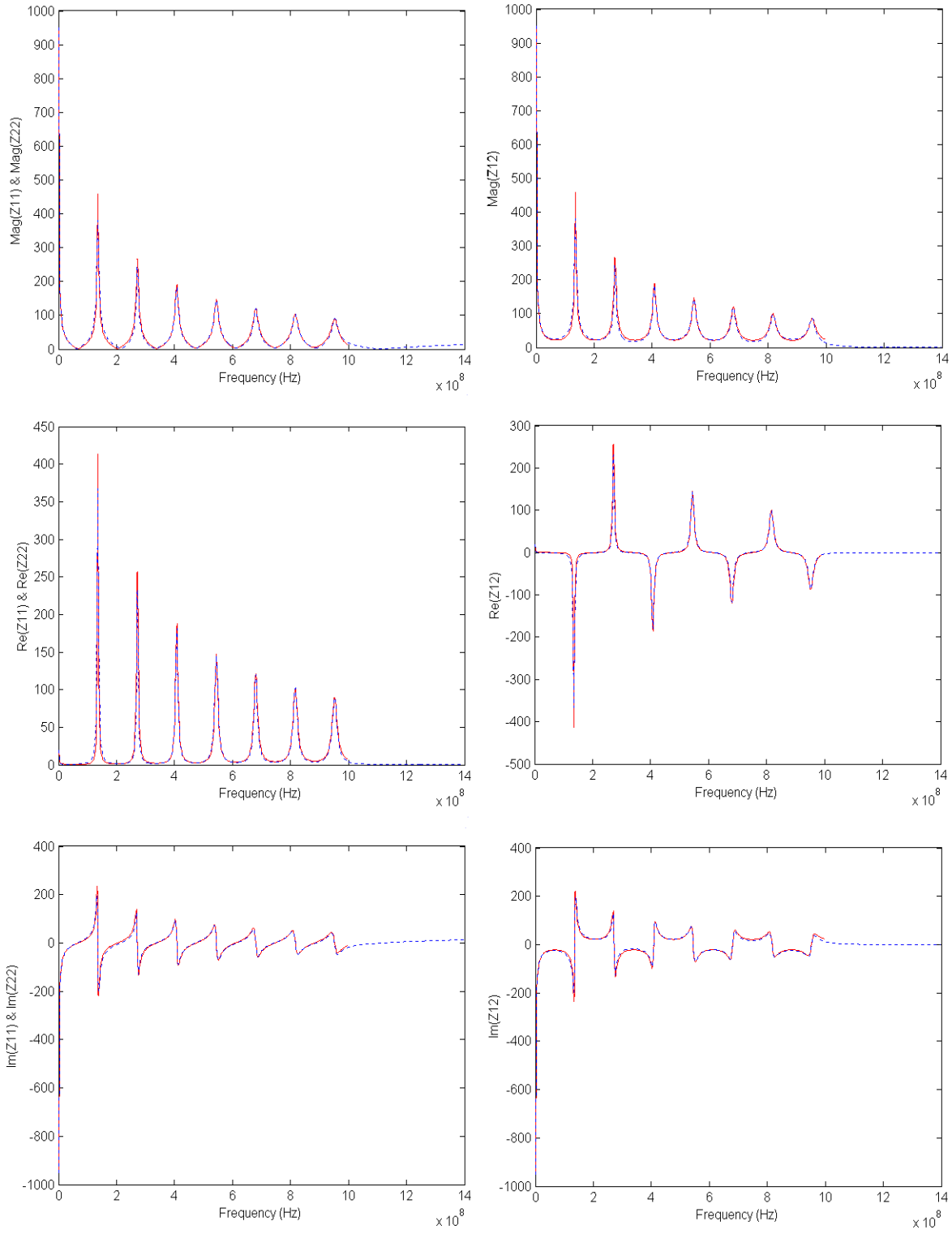


Fig. 7.8. Impedance response for the vdd2/gnd1 planes computed by transmission matrix method (solid) and Z-parameter based macro-modeling method (dashed).

Table 7.1

Unknown Parameters for Vdd1/Gnd1 Planes

		Y11		Y12		Y22	
P_r	P_i	α_{11}	β_{11}	α_{12}	β_{12}	α_{22}	β_{22}
9.425E+07	5.927E+09	5.662E+08	3.300E-03	-5.097E+08	-1.300E-03	5.662E+08	3.300E-03
1.068E+08	5.078E+09	6.993E+08	-8.500E-03	6.567E+08	1.340E-02	6.993E+08	-8.500E-03
8.168E+07	4.228E+09	5.996E+08	-1.630E-02	-5.773E+08	-1.000E-02	5.996E+08	-1.630E-02
8.168E+07	3.378E+09	6.920E+08	-2.230E-02	6.710E+08	1.330E-02	6.920E+08	-2.230E-02
6.283E+07	2.528E+09	6.399E+08	2.450E-02	-6.301E+08	-1.730E-02	6.399E+08	2.450E-02
5.027E+07	1.679E+09	6.627E+08	-2.670E-02	6.566E+08	1.950E-02	6.627E+08	-2.670E-02
3.770E+07	8.326E+08	7.490E+08	-2.970E-02	-7.476E+08	-3.040E-02	7.490E+08	-2.970E-02
P_{or}		γ_{11}		γ_{12}		γ_{22}	
1.0429 E+07		2.9717 E+07		3.3613 E+07		2.9717 E+07	
		K_{11}		K_{12}		K_{22}	
		0.3462 E-09		-0.0173 E-09		0.3462 E-09	

Table 7.2

Unknown Parameters for Vdd2/Gnd1 Planes

		Y11		Y12		Y22	
P_r	P_i	α_{11}	β_{11}	α_{12}	β_{12}	α_{22}	β_{22}
6.283E+07	5.983E+09	5.609E+09	2.310E-02	-5.438E+09	-1.080E-02	5.609E+09	2.310E-02
5.655E+07	5.129E+09	5.759E+09	-3.300E-02	5.679E+09	8.700E-02	5.759E+09	-3.300E-02
4.398E+07	4.274E+09	5.261E+09	-5.800E-02	-5.212E+09	-5.900E-02	5.261E+09	-5.800E-02
4.398E+07	3.420E+09	6.403E+09	-9.300E-02	6.364E+09	7.890E-02	6.403E+09	-9.300E-02
3.142E+07	2.565E+09	5.829E+09	-1.043E-01	-5.817E+09	-8.290E-02	5.829E+09	-1.043E-01
1.885E+07	1.709E+09	4.815E+09	-9.530E-02	4.811E+09	5.950E-02	4.815E+09	-9.530E-02
1.885E+07	8.535E+08	7.469E+09	5.224E-01	-7.468E+09	-7.456E-01	7.469E+09	5.224E-01
P_{or}		γ_{11}		γ_{12}		γ_{22}	
1.0569 E+07		2.5900 E+08		2.8539 E+08		2.5900 E+08	
		K_{11}		K_{12}		K_{22}	
		0.2961 E-08		-0.0353 E-08		0.2961 E-08	

For computing simultaneous switching noise using SPICE, an equivalent circuit model for the test vehicle in Fig. 7.6 was implemented as a 6-port system for all the power/ground plane pairs. For the details of the SPICE implementation using the 6 ports, a SPICE netlist is shown in Appendix E. Using a small resistor ($1\times10^{-6}\ W$), they were connected together on the right side of the test vehicle (P2, P4, and P6 shown in Appendix E). A power supply of 5 volts was applied at the right side of the test vehicle to power up the structure. The 22-ohm microstrip transmission lines were modeled using the W-Element lines (lossy lines) in HSPICE, with parameters $L = 1.237\times10^{-7}\ H/m$, $C = 3.573\times10^{-10}\ F/m$, $R = 7.001\times10^{-1}\ W/m$ and $R_{ac} = 4.943\sqrt{f}\times10^{-4}\ W/m$. The microstrip transmission lines were unterminated and represented as a 4-port circuit with reference to the vdd1 plane at the right and left side of the test vehicle.

Return currents on the planes cause the planes to bounce when the signal transmission lines are incorporated into the plane models [31]. The reference planes are not perfect, and they bounce as the return currents accumulate and charge the parallel plate capacitance, causing waves to propagate between power/ground planes. Since the ground planes beneath the reference planes are not ideal grounds, their effect due to the charging and discharging of the signal lines need to be considered. As a result, two sets of extra transmission lines having very large characteristic impedance with reference to the vdd2 plane for both the vdd1/gnd2 and vdd2/gnd plane pairs were added to the drivers for enabling the noise to propagate vertically through the layers [31]. These transmission lines capture the noise on the lower layers (PP2 and PP3) accurately. To include these effects, lossless T lines (HSPICE) were used for generating the circuit models.

Fig. 7.9 shows the modeling and measurement result for the transmission lines with no termination, where the output signal had a period of 200 ns with rise time of 10 ns. As shown in Fig. 7.9, the noise mostly occurs during the high to low transition of the drivers while very little noise occurs during the low to high transition. In [31], this phenomenon was explained based on the return currents. When the drivers transition from low to high, current flows into the transmission lines, and the return current flows on the power planes (vdd1, vdd2). The current loop is completed through the power planes, the drivers, the transmission lines, and the capacitance between the transmission lines and the power planes. As a result, noise is not excited between power/ground planes since the ground planes are not part of the current loop. On the contrary, when the transition is from high to low, the current loop is completed through the drivers, which connect the transmission lines to the ground planes (gnd1, gnd2), and the power planes, where the transmission lines are referenced and the return current flows. As a result, this current loop excites a radial wave between the power/ground planes that bounces off the edges of the planes, causing the planes to bounce [31].

In this section, the transmission matrix method was used to compute the impedance response in the frequency domain, a macro-model was generated based on the response, and simultaneous switching noise was simulated using SPICE. Since a good correlation between the original data and macro-model was obtained in the frequency domain in Figs. 7.7 and 7.8, the simulated transient response also showed good correlation with the measurement data, as shown in Fig. 7.9.

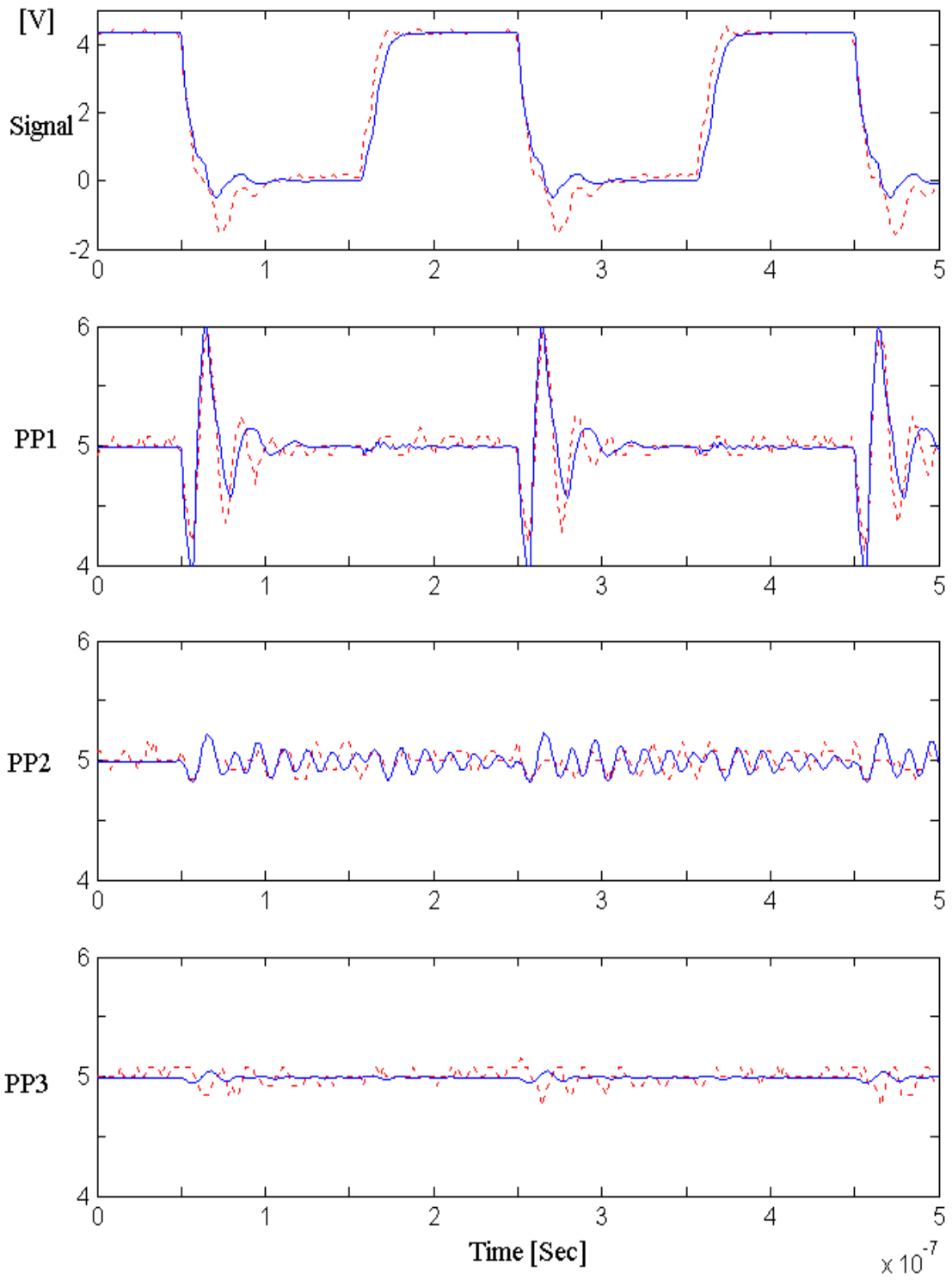


Fig. 7.9 Simultaneous switching noise: modeling (solid) result and measurement (dashed) result: PP1 = voltage between the vdd1 and gnd1, PP2 = voltage between vdd2 and gnd1, and PP1 = voltage between the vdd2 and gnd2.

7.3.2 Test Case 2: Test Vehicle from IBM

As another example, based on the model to hardware correlation shown in Chapter 5.2, the analysis was expanded for computing simultaneous switching noise in IBM's HyperBGA test vehicle shown in Fig. 5.9. Using the transmission matrix method and the macro-modeling method described in this chapter, the board and package planes have were analyzed with I/O interconnects and nonlinear drivers.

For the time domain simulation, two power distribution planes for a 2.5 V and 3.3 V power supply were considered in the test vehicle, which consists of 1.5 V, 2.5 V and 3.3 V planes, as shown in Fig. 5.9. The 2.5 V power distribution network, which consists of the V1/TSR(Gnd) and V1/Gnd package plane pairs and the V4/V2(Gnd) board plane pair, is used to supply power to core logic circuits while the 3.3 V power distribution network, which consists of the three split package plane pairs (left, top and right) between the Gnd and V2(split) layers and the V8/V2(Gnd) board plane pair, supplies power to the I/O circuits, as shown in Fig. 7.10. A set of 18 transmission lines on the S1 layer, which are sandwiched between the V1 and Gnd layers on the package, are driven by the 3.3V I/O drivers. Through the vertical via connections, they are connected with another set of 18 transmission lines on the S3 layer, which are sandwiched between the V2(Gnd) and V4 layers on the board. Due to the return currents, the voltage disturbance is induced in the 2.5 V power distribution network.

Using the transmission matrix method, one bare board plane pair and two package plane pairs in the 2.5 V power distribution network, which are connected through via connections, were analyzed. All the details for the Saranac board were discussed in Chapter 5.2. In the package, the planes have dimensions of 3.2 cm by 3.2 cm with

relative permittivity e_r = 2.7, with corners at (28.067 cm, 12.065 cm), (31.267cm, 12.065 cm), (31.267 cm, 15.265 cm) and (28.067 cm, 15.265 cm), based on the co-ordinate system described in Chapter 5.2. The dielectric thickness between the V1 and TSR(Gnd) layers was 12.5756 mils while 83.999 mils was used between the V1 and Gnd layers. The conductor planes for both the pairs are made of copper ($s_c = 5.8 \times 10^7$ S/m) with a thickness of 33.528 μm and dielectric loss tangent $tan(d)$ = 0.02 at 1 GHz. The package was attached to the bare board without decoupling capacitors. The package planes included four decoupling capacitors of 32 nF with ESL=1.5 nH and ESR=0.2 Ω between the V1 and Gnd layers. The decoupling capacitors were located at (31.201 cm, 14.449 cm), (29.951 cm, 15.199 cm), (29.201 cm, 13.949 cm) and (30.451 cm, 13.199 cm).

The 2.5 V power distribution network consists of three split package plane pairs and one board plane pair, as mentioned earlier. The top view of the geometry for the network is shown in Fig. 7.10. All the parameters for the board and package planes in the 3.3 V power distribution network are the same as those in the 2.5 V power distribution network except the dielectric thickness. The dielectric thickness between the V2(Gnd) and V8 layers is 55.525 mils while it is 3.307 mils between the Gnd and V2(split) layers.

The transmission matrix method was first applied to compute a 15×15 impedance matrix for the 2.5 V power distribution network and a 4×4 impedance matrix for the 3.3 V power distribution network at the port locations, which are shown in Appendix D. As shown in Appendix D, the matrices for the 2.5 V and 3.3 V power distribution networks were defined from Ports 1 to 15 and from Ports 16 to 19, respectively. Then, using the macro-modeling method described in this chapter, two Z-parameter based macro-models with common poles were generated for both power distribution networks, based on the

simulated data from 1 MHz to 1 GHz. The impedance response generated by the methods is compared in Figs. 7.11 and 7.12. The test vehicle shown in Fig. 5.9 has multiple resonances over the frequency bandwidth of interest. The rational function for the 2.5 V power distribution network was generated with m = 43 and n = 42 for numerator and denominator orders in Eq. (6.1), and was decomposed into 20 complex conjugate pole-residue pairs, 1 real pole-residue pair, 1 capacitance and 1 inductance term in the partial fraction expansion shown in Eq. (6.8). The rational function for the 3.3 V power distribution network was generated with m = 45 and n = 44, and was decomposed into 21 complex conjugate pole-residue pairs, 1 real pole-residue pair, 1 capacitance and 1 inductance term. In the figure, the response has a discrepancy at higher frequencies. To reduce the error, more data is needed in the higher frequency range for interpolation.

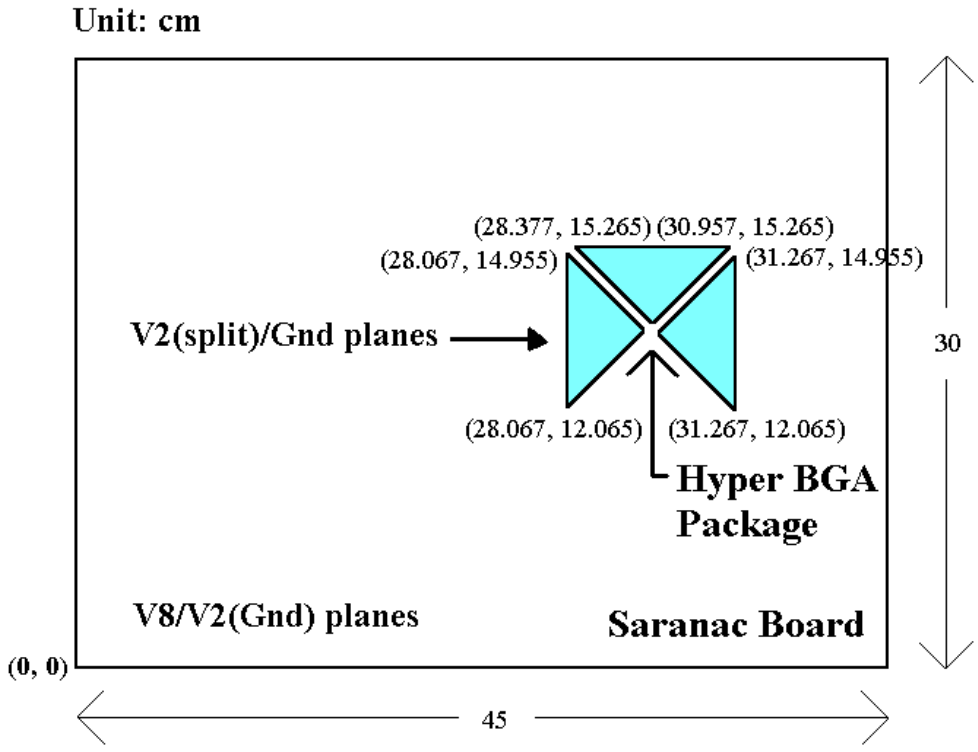
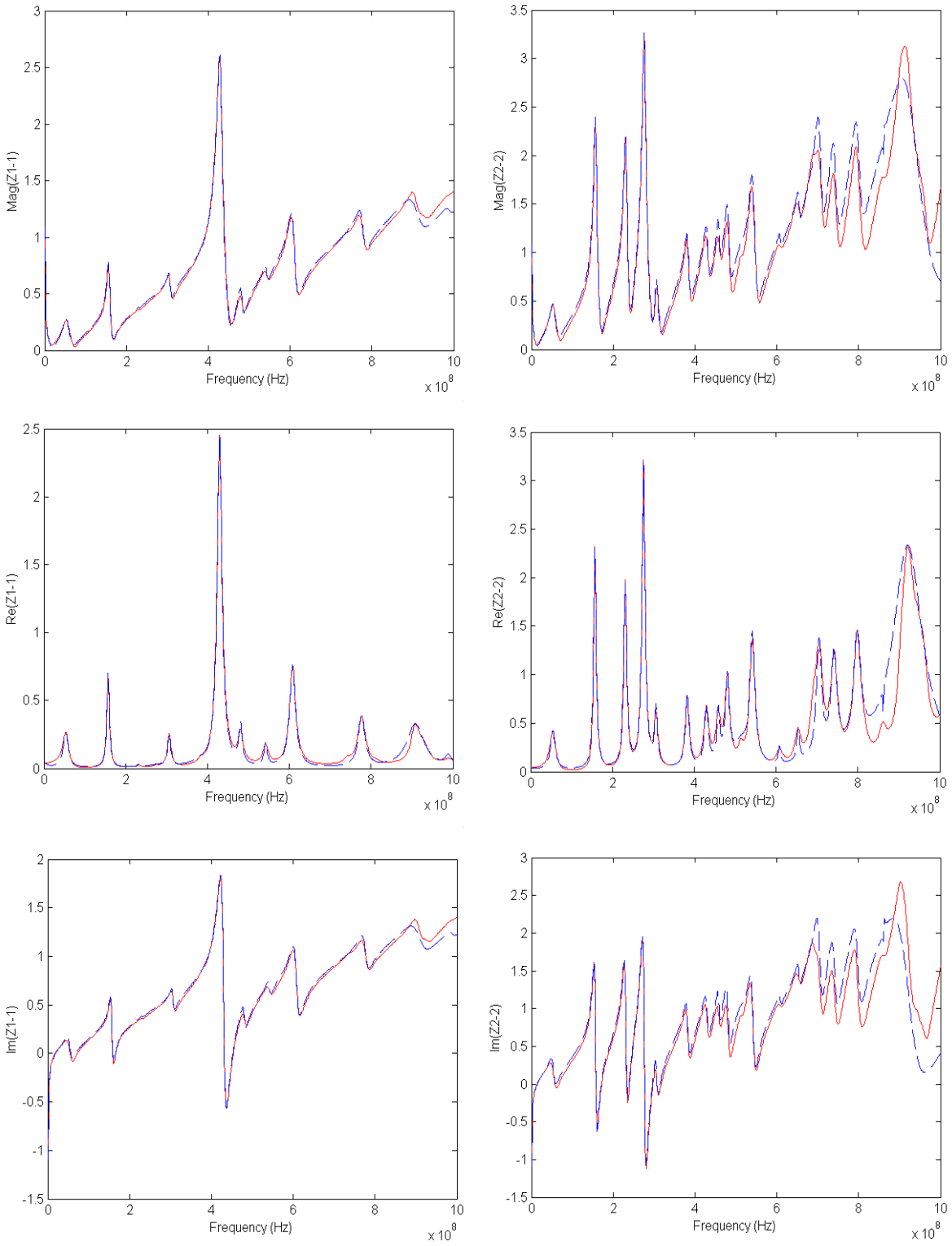
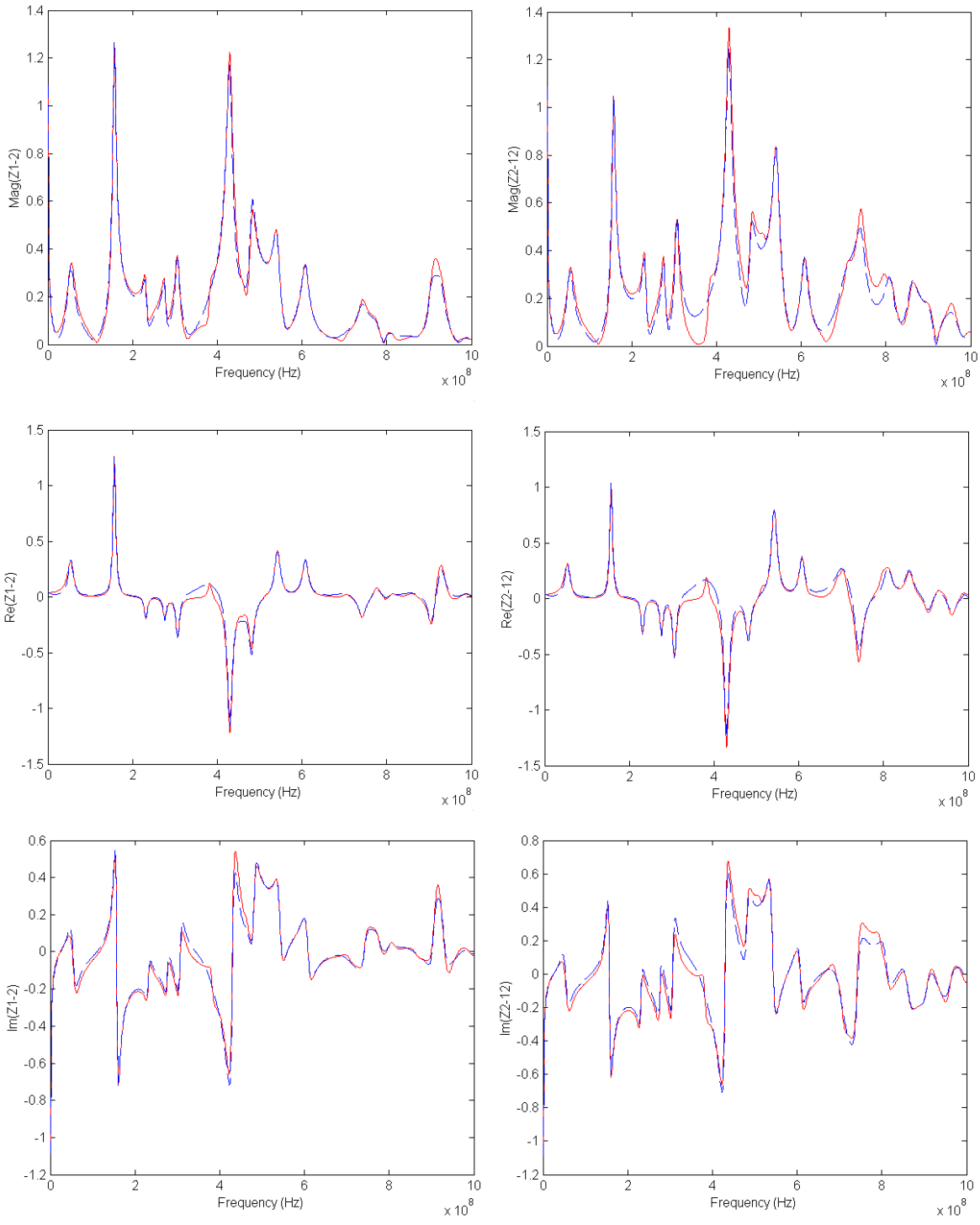


Fig. 7.10 Top view of the geometry for 3.3 V power distribution network.

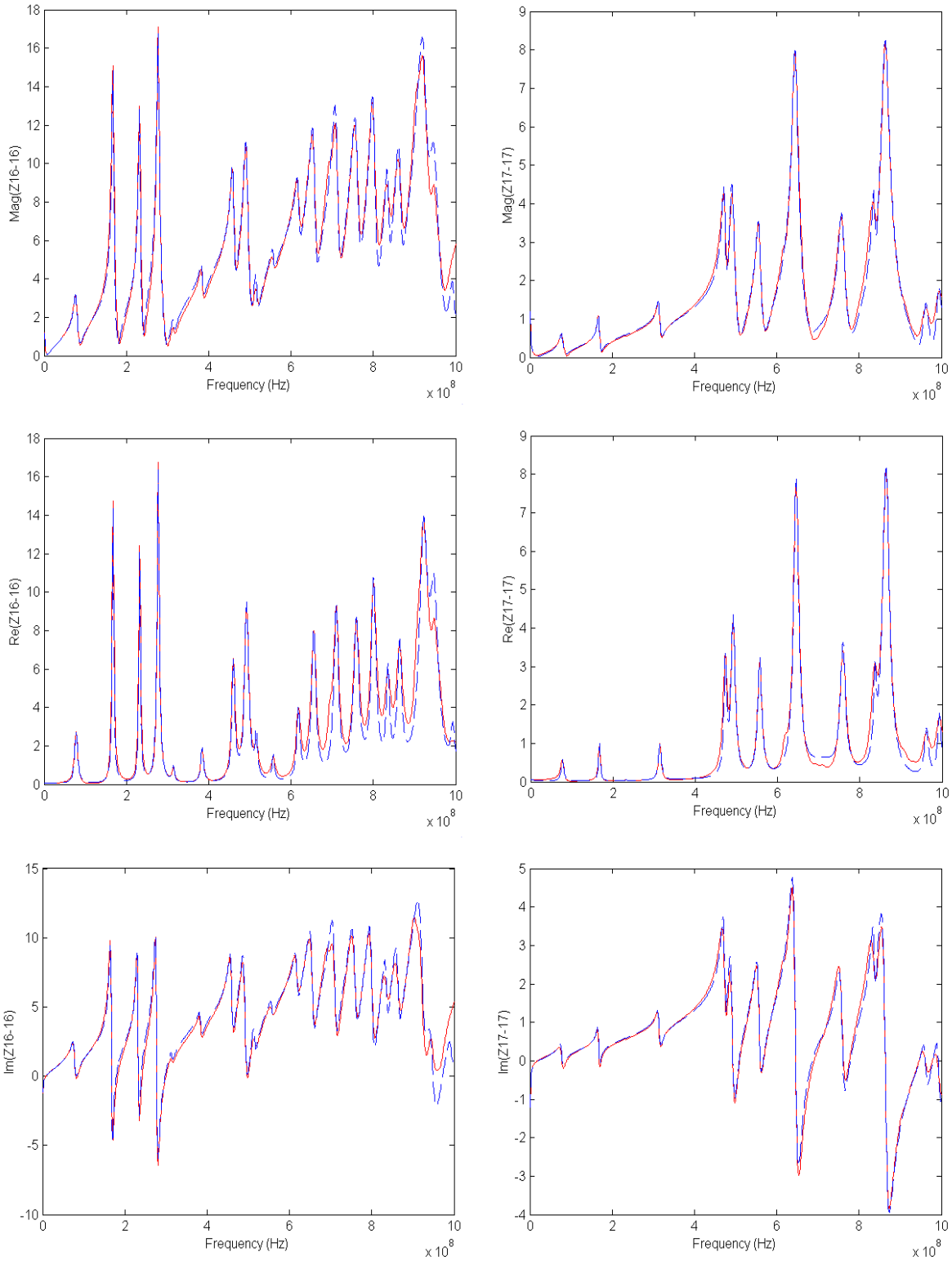


(a)

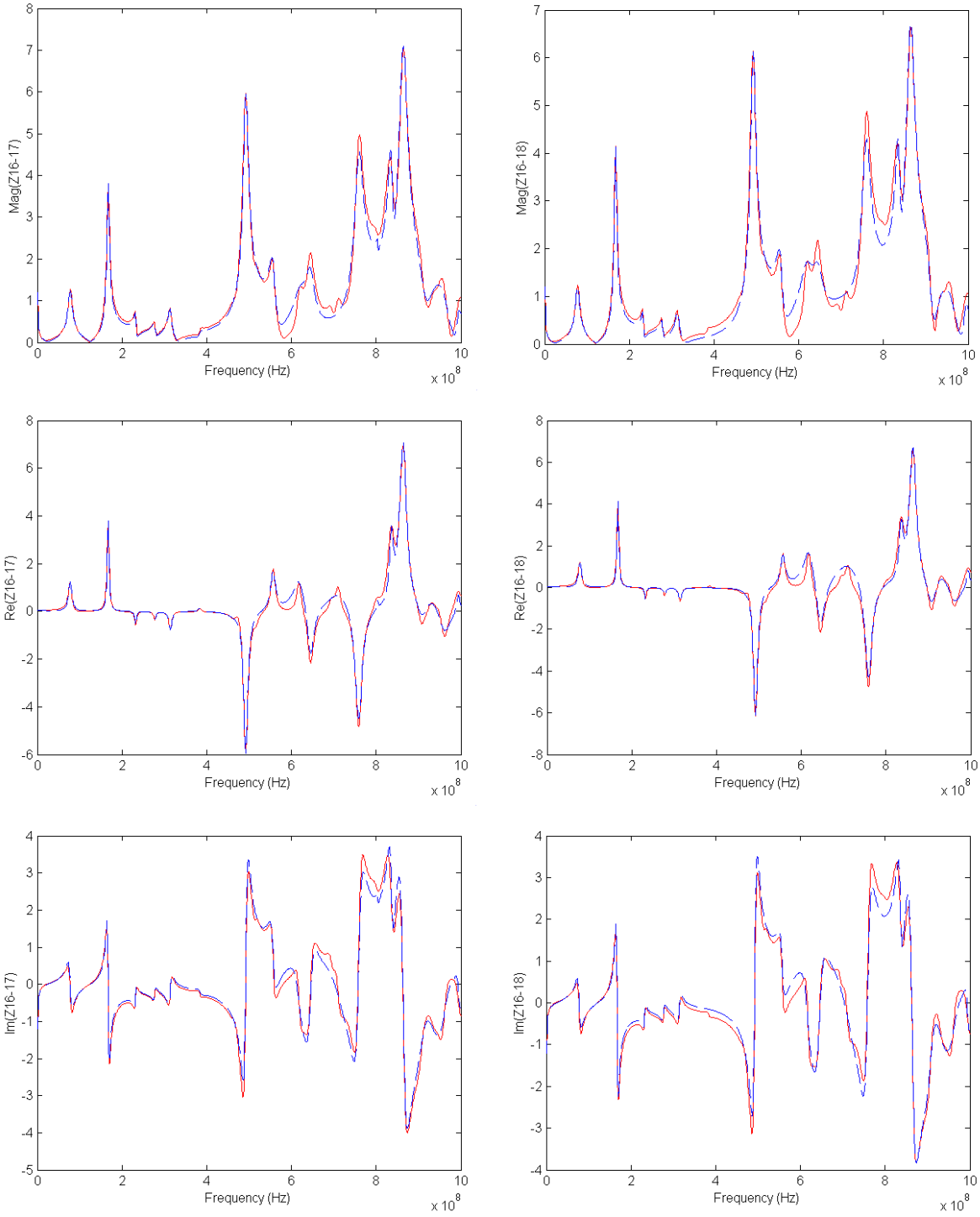


(b)

Fig. 7.11. Impedance response for 2.5 V power distribution network computed by transmission matrix method (solid) and Z-parameter based macro-modeling method (dashed): (a) self impedance at Ports 1 and 2 and (b) transfer impedance between Ports 1 and 2 and Ports 2 and 12.


Mag(Z16-16)
Mag(Z17-17)
Re(Z16-16)
Re(Z17-17)
Im(Z16-16)
Im(Z17-17)
Frequency (Hz)
x 10^8

(a)



(b)

Fig. 7.12. Impedance response for 3.3 V power distribution network computed by transmission matrix method (solid) and Z-parameter based macro-modeling method (dashed): (a) self impedance at Ports 16 and 17 and (b) transfer impedance between Ports 16 and 17 and Ports 16 and 18.

For computing simultaneous switching noise using SPICE, an equivalent circuit model was implemented as a 19-port system for all the package/board planes in the 2.5 V and 3.3 V power distribution networks. Based on the port description shown in Appendix D, a SPICE netlist for I/O drivers, transmission lines and DC sources was generated as in Appendix E. As shown in Appendix E, the 3.3 V power distribution network supplied power to 18 I/O drivers, with a 3.3 V DC source at Port 16. The outputs of the drivers were connected with 50-ohm transmission lines using lossless T lines in SPICE. All the transmission lines were referenced to the 2.5 V power distribution network, where a 2.5 V DC source was attached to Port 3.

The goal of this analysis was to capture the ground bounce in the 2.5 V power distribution network due to return currents generated by the 3.3 V transmission lines. Fig. 7.13 shows the modeling result for the transmission lines with no termination, where the signal of the drivers has a period of 20 ns with rise time of 700 ps and fall time of 300 ps. In the figure, the signal output of the 7^{th} transmission line (T7: shown in Appendix E) was captured at the driver output on the package and at the end of the transmission line on the board, and noise voltage at Port 1 and Port 2 were computed, named C31 and C16 sites in Appendix C, respectively. While Port 2 (C16) was on the edge of the board in the vicinity of the 2.5 V DC source, Port 1 (C31) was beneath the drivers, which were driven in the center area of the package. As a result, the I/O switching noise at Port 1 (C31) is larger than that at Port 2 (C16), as shown in Fig. 7.13. In addition, while the noise shown in Fig. 7.9 mostly occurred during the high to low transition of the drivers, the noise shown in Fig. 7.13 was generated over the entire time period, which is the sum of the noise generated by each I/O driver. The charge and delay time of a signal varies with its

physical length and characteristic impedance. As shown in Appendix E, since the transmission lines had different physical lengths, waves generated due to the return currents propagated with different time delays between the power/ground planes. In addition, due to the physical separation between the output port and the reference ports, the noise was generated over the entire time period.

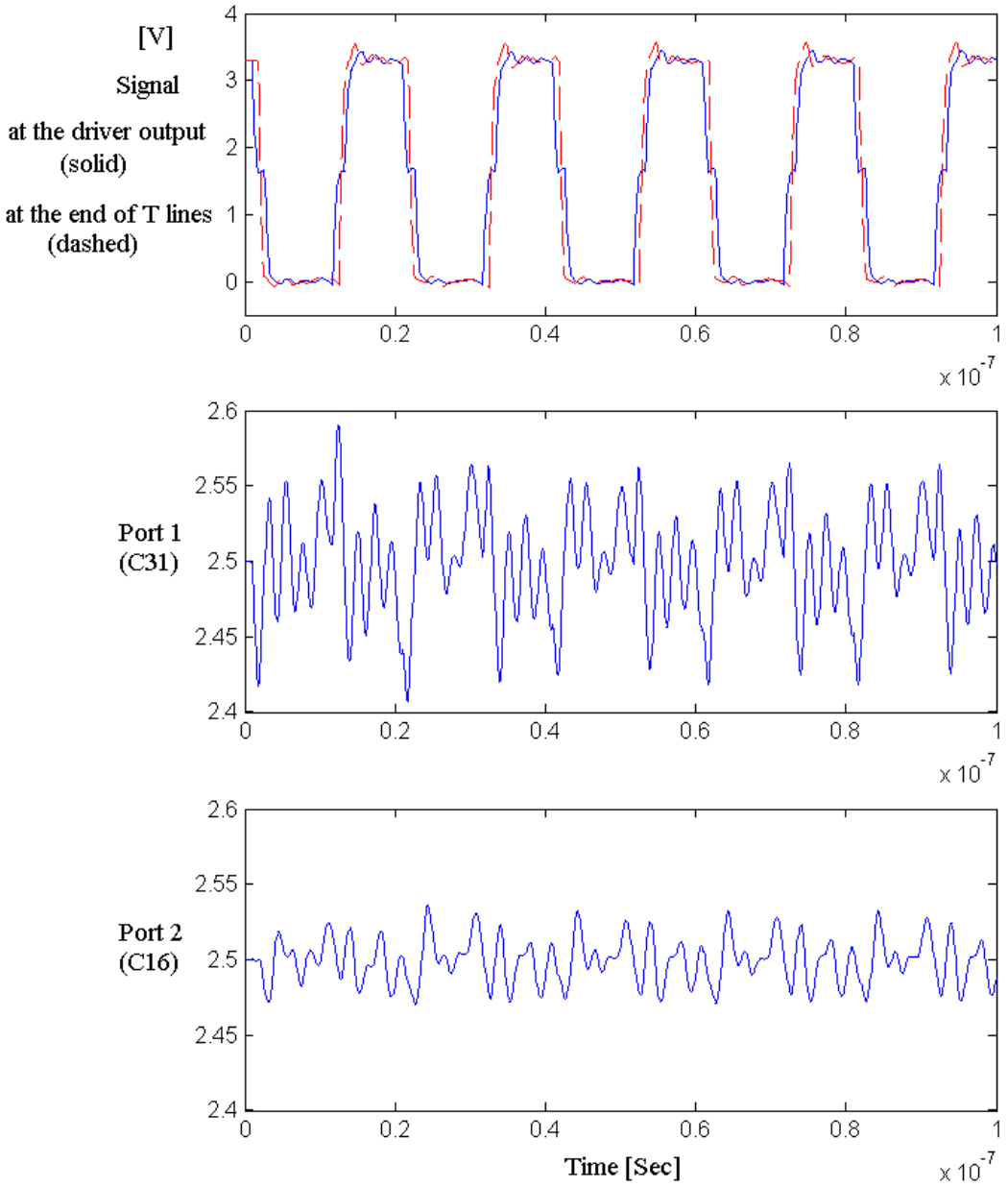


Fig. 7.13 Simultaneous switching noise generated by the modeling method.

Using the measurement result obtained in [38], the noise voltage at Port 2 (C16) was compared, as shown in Fig. 14. Fig. 14 shows one period of the noise voltage. Even though the waveforms between modeling and measurement are not identical, peak-to-peak voltages are well matched. The discrepancy between modeling and measurement in the time domain could be due to unknown parasitics in the HyperBGA package, due to the driver model used or due to the small error in the macro-modeling method at higher frequencies.

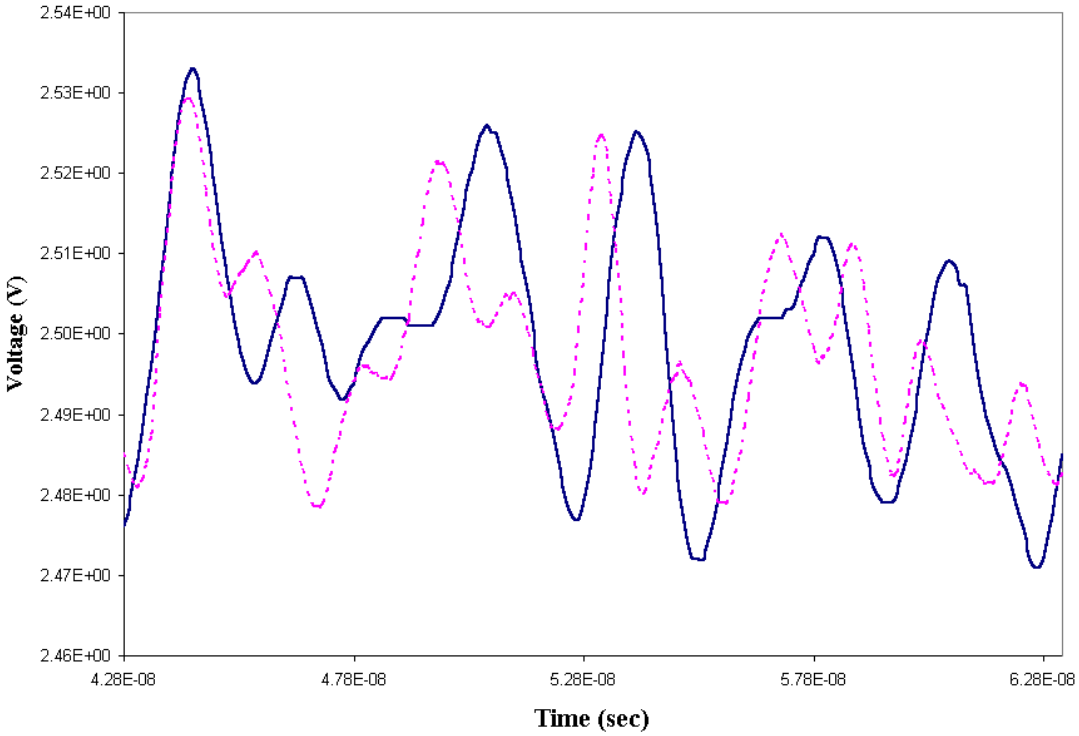


Fig. 7.14 Simultaneous switching noise at Port 2 (C16): measurement (dashed) result and modeling (solid) result.

To examine the negative feedback effect of nonlinear switching circuits, the noise voltage at Port 2 (C16) shown in Fig. 7.13 was compared with the voltage computed using linear sources, as shown in Fig. 7.15. Totally, 18 current outputs were measured in SPICE, between the drivers and the port connections on the 2.5 V power distribution

network. With the short termination at the port containing the 2.5 V DC source, the impedance matrix was recomputed. Then, using the IDFT described in Chapter 3 and summing the voltage generated by each current source, the noise voltage at Port 2 (C16) was computed. Comparing Figs. 7.13 and 7.15, the noise voltage with linear drivers is larger than the voltage generated using the nonlinear drivers even though the waveforms are similar. As mentioned in Chapter 1, linearity of noise is not preserved beyond a certain number of switching drivers due to the negative feedback. As a result, when noise becomes excessive, it slows down the drivers by reducing the current output of the drivers.

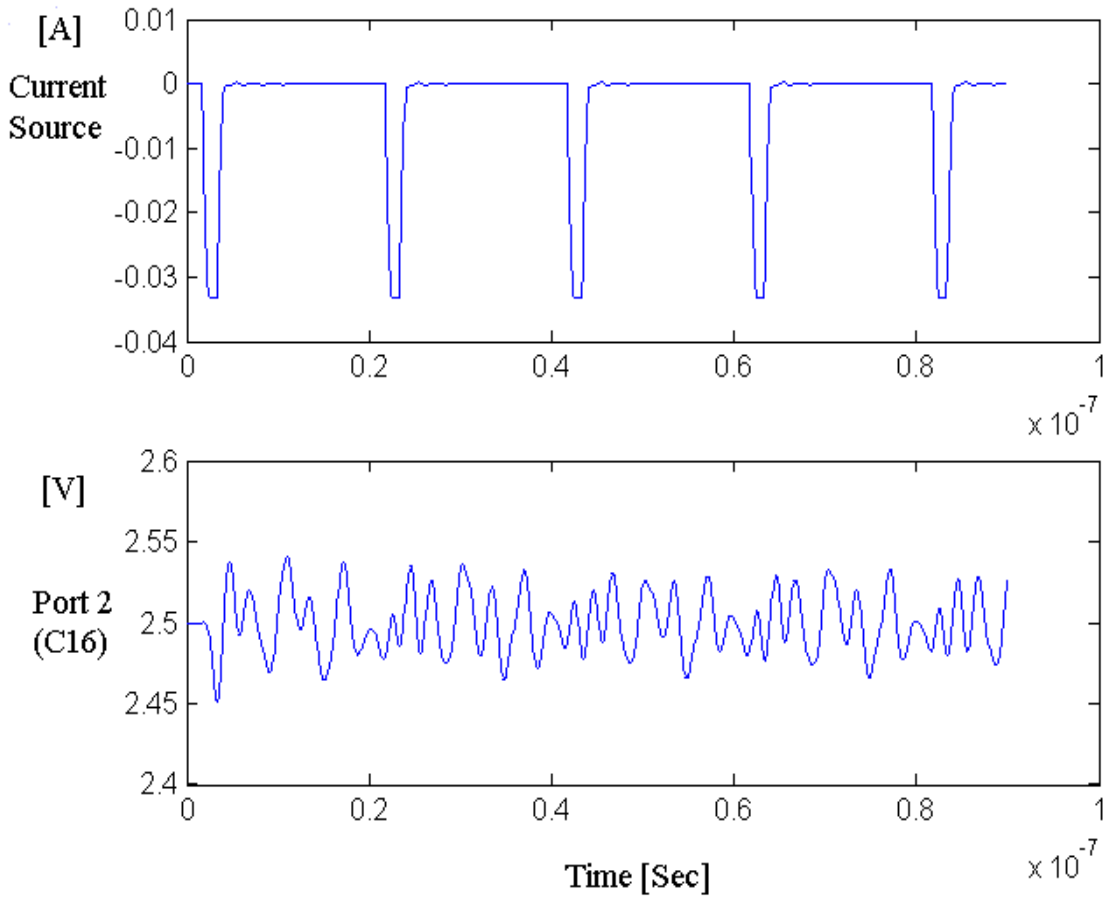


Fig. 7.15 Simultaneous switching noise at Port 2 (C16) using linear current sources.

7.4 Summary

In this chapter, a Z-parameter based macro-modeling method for generating rational functions was discussed. The rational functions were computed using direct mapping based on the data at four specific frequencies, which enables four unknown coefficients (P_i, P_r, a and b) to be computed. Compared with the method of least squares approximation, the method is very fast and can be applied for an electrically large system consisting of multiple resonances and requiring a large number of ports. However, the implementation of the equivalent circuits is not the most efficient solution. In addition, the computation of P_r is an approximation, and parameters a and b are computed based on the approximation of P_r. As a result, the accuracy of this method can depend on the value of the parameter P_r. More research is therefore necessary to increase the accuracy for calculating P_r. As future work, an iterative method to minimize the average error can be developed.

In this chapter, to compute simultaneous switching noise in complex structures such as Sun Microsystems' test vehicle and IBM's test vehicle, the macro-models based on the Z parameters have been simulated with nonlinear switching circuits and I/O interconnects. Based on model to hardware correlation in the frequency domain, which was shown in the previous chapter, the transient response in the time domain was obtained using macro-models and nonlinear drivers.

CHAPTER 8

Conclusion and Future Work

In this dissertation, modeling methods have been presented for analyzing multi-layered arbitrary shaped power distribution networks both in the frequency and time domain. Since realistic power distribution networks in the package and board are electrically large structures containing numerous discontinuities and components, the analysis of the entire power distribution network demands large memory requirements and a considerable CPU run time on the most powerful computers. As a result, there has been a clear need for more efficient modeling methods to accurately model such large networks. Based on these issues, modeling methods have been developed and applied for a high-speed digital system requiring high-performance packages. In this dissertation, two methods have been discussed for frequency and transient simulations; namely, the transmission matrix method for the frequency simulation and the macro-modeling method based on Y and Z parameters for transient simulation.

The transmission matrix method has been developed to compute the frequency response at specific ports in the network. The advantage of this method is its ability to analyze electrically large and complicated structures with minimum computational time and small memory requirements. The method has shown good agreement with measurements and other simulators such as SPICE, an analytical solution and the cavity resonator model. The method was tested on test vehicles from IBM and Sun Microsystems, and products from Sun Microsystems and Kodak.

Based on the frequency response computed using the transmission matrix method, a method using an IDFT and convolution was used for analyzing core switching nose. However, its use is limited to linear sources. For analyzing I/O switching noise, power distribution networks need to be analyzed in the presence of interconnects and non-linear drivers. For such system level simulation, the need for improved circuit analysis is required. This is possible through macro-models. In this dissertation, two macro-models have been developed; namely, a Y-parameter based macro-model using a weighted least squares approximation by solving an eigenvalue problem and a Z-parameter based macro-model using direct mapping. A Y-parameter based macro-model is limited to networks requiring a small number of ports while its equivalent circuit implementation is efficient compared with those of other parameters. For an electrically large system consisting of multiple resonances and requiring a large number of ports, a Z-parameter based macro-model is preferred.

All the methods described above have been verified using several simulations and measurements. Finally, the methods described have been applied for the simulation of simultaneous switching noise on the test vehicles from Sun Microsystems and IBM. Based on the model to hardware correlation in the frequency domain using the transmission matrix method, the macro-models were constructed and simulated in HSPICE. By combining the two methods, an electrically large and complex structure can be analyzed efficiently.

As an extension to the methods described in this dissertation, the following areas of research are appropriate:

1. **Analysis of on-chip power distribution networks:** For accurately analyzing substrate noise, a fine gridded mesh is required in silicon substrates. On-chip power distribution networks can also be represented as distributed and repeated resistive, capacitive and inductive circuit elements. The use of the transmission matrix method for such networks can be a useful study.
2. **Evaluation and calculation of partial self and mutual inductances for vias:** As stated previously, there are thousands of via connections in realistic power distribution networks. Currently, FastHenry has been used to compute the via inductances. However, the use of FastHenry is cumbersome since FastHenry was developed for analyzing generic structures and therefore requires a large amount of CPU time for computation. Hence, a more direct computational method is required to compute the self and mutual inductances for the via connections. Using the numerical expressions developed as part of the partial element equivalent circuit (PEEC) method, a method can be developed for computing the via inductances for incorporation into the transmission matrix method.
3. **Simulation of nonlinear drivers using the IDFT and convolution:** Using an equivalent circuit model based on Z parameters, power distribution networks were simulated in the presence of non-linear drivers in SPICE. However, this is also limited for networks consisting of around 20,000 circuit elements due to the limitation of SPICE. In addition, it is not easy to avoid internal time step errors in SPICE for networks simulated with non-linear drivers. In this dissertation, independent linear sources were used using the IDFT and convolution. Based on

the I/V characteristics of CMOS inverters, non-linear circuits can be used which include the negative feedback effect of the switching circuits.

Appendix A. Locations of Decoupling Capacitors for L-Shaped Geometry

#	x (cm)	y (cm)	C (F)	ESL (H)	ESR (Ω)
1	8.1788	2.1082	1.00E-07	4.70E-10	0.0391
2	10.5918	2.1082	1.00E-07	4.70E-10	0.0391
3	12.2174	4.1783	1.00E-07	4.70E-10	0.0391
4	12.2174	5.6515	1.00E-07	4.70E-10	0.0391
5	12.2555	6.3881	1.00E-07	4.70E-10	0.0391
6	9.8044	8.5471	1.00E-07	4.70E-10	0.0391
7	7.366	9.2329	1.00E-07	4.70E-10	0.0391
8	6.223	5.1181	1.00E-07	4.70E-10	0.0391
9	6.223	3.4163	1.00E-07	4.70E-10	0.0391
10	6.223	7.6073	1.00E-07	4.70E-10	0.0391
11	6.223	3.6195	1.00E-08	4.70E-10	0.1
12	6.223	5.1181	1.00E-08	4.70E-10	0.1
13	7.4422	2.4384	1.00E-08	4.70E-10	0.1
14	9.2456	2.1082	1.00E-08	4.70E-10	0.1
15	12.2174	4.1783	1.00E-08	4.70E-10	0.1
16	12.2174	5.6515	1.00E-08	4.70E-10	0.1
17	7.5692	9.2329	1.00E-08	4.70E-10	0.1
18	10.795	9.2329	1.00E-08	4.70E-10	0.1
19	6.223	7.6073	1.00E-08	4.70E-10	0.1
20	12.2174	9.0043	1.00E-08	4.70E-10	0.1
21	5.842	3.937	1.00E-06	7.47E-10	0.0158
22	5.842	5.1562	1.00E-06	7.47E-10	0.0158
23	5.842	6.4262	1.00E-06	7.47E-10	0.0158
24	5.842	7.6962	1.00E-06	7.47E-10	0.0158
25	5.842	8.9662	1.00E-06	7.47E-10	0.0158
26	6.5786	1.7653	1.00E-06	7.47E-10	0.0158
27	7.7343	1.778	1.00E-06	4.70E-10	0.0158
28	8.8773	1.7653	1.00E-06	4.70E-10	0.0158
29	10.0584	1.7653	1.00E-06	4.70E-10	0.0158

#	X (cm)	Y (cm)	C (F)	ESL (H)	ESR (Ω)
30	11.4427	2.1463	1.00E-06	4.70E-10	0.0158
31	12.2555	4.0132	1.00E-06	4.70E-10	0.0158
32	12.2555	5.2832	1.00E-06	4.70E-10	0.0158
33	11.8745	2.1463	1.00E-06	4.70E-10	0.0158
34	12.2555	7.874	1.00E-06	4.70E-10	0.0158
35	12.2555	2.6416	1.00E-06	4.70E-10	0.0158
36	10.9855	2.1463	1.00E-06	4.70E-10	0.0158
37	10.0584	1.7653	1.00E-06	4.70E-10	0.0158
38	8.8773	1.7653	1.00E-06	4.70E-10	0.0158
39	7.7343	1.778	1.00E-06	4.70E-10	0.0158
40	6.5786	1.7653	1.00E-06	4.70E-10	0.0158
41	5.842	3.937	1.00E-06	7.47E-10	0.0158
42	5.842	5.1562	1.00E-06	7.47E-10	0.0158
43	5.842	6.4262	1.00E-06	7.47E-10	0.0158
44	5.842	7.6962	1.00E-06	7.47E-10	0.0158
45	5.842	8.9662	1.00E-06	7.47E-10	0.0158
46	12.2555	7.874	1.00E-06	4.70E-10	0.0158
47	7.1501	1.4732	1.00E-06	4.70E-10	0.0158
48	12.2555	5.2832	1.00E-06	4.70E-10	0.0158
49	12.2555	4.0132	1.00E-06	4.70E-10	0.0158
50	12.2555	2.6416	1.00E-06	4.70E-10	0.0158
51	9.4615	9.6012	1.00E-06	7.47E-10	0.0158
52	8.1915	9.6012	1.00E-06	7.47E-10	0.0158
53	10.0203	9.6012	1.00E-06	7.47E-10	0.0158
54	11.938	9.6012	1.00E-06	7.47E-10	0.0158
55	6.1595	9.5377	1.00E-06	7.47E-10	0.0158
56	3.6957	1.5367	1.00E-06	7.47E-10	0.0158
57	8.2931	1.4732	1.00E-06	4.70E-10	0.0158
58	6.1595	2.9845	1.00E-06	7.47E-10	0.0158
59	12.2555	9.144	1.00E-06	4.70E-10	0.0158
60	12.2174	9.2329	1.00E-06	4.70E-10	0.0158
61	7.1501	1.778	1.00E-05	1.10E-09	0.006
62	8.2931	1.778	1.00E-05	1.10E-09	0.006
63	11.3157	9.6012	1.00E-05	1.10E-09	0.006
64	9.9695	1.4986	1.00E-05	1.10E-09	0.006

#	X (cm)	Y (cm)	C (F)	ESL (H)	ESR (Ω)
65	11.9507	2.6416	1.00E-05	1.10E-09	0.006
66	12.2555	3.4036	1.00E-05	1.10E-09	0.006
67	12.2555	4.6736	1.00E-05	1.10E-09	0.006
68	6.096	1.4859	1.00E-05	1.10E-09	0.006
69	11.8745	8.7122	1.00E-05	1.10E-09	0.006
70	12.2555	8.509	1.00E-05	1.10E-09	0.006
71	5.842	8.3312	1.00E-05	1.10E-09	0.006
72	5.842	7.0612	1.00E-05	1.10E-09	0.006
73	9.4615	1.4732	1.00E-05	1.10E-09	0.006
74	5.842	3.2512	1.00E-05	1.10E-09	0.006
75	5.842	4.5212	1.00E-05	1.10E-09	0.006
76	7.1501	1.778	1.00E-05	1.10E-09	0.006
77	8.2931	1.778	1.00E-05	1.10E-09	0.006
78	5.4381	1.4884	1.00E-05	1.10E-09	0.006
79	10.6426	1.7526	1.00E-05	1.10E-09	0.006
80	11.5951	1.7526	1.00E-05	1.10E-09	0.006
81	12.2555	3.4036	1.00E-05	1.10E-09	0.006
82	12.2555	4.6736	1.00E-05	1.10E-09	0.006
83	6.7945	9.6012	1.00E-05	1.10E-09	0.006
84	6.604	2.1717	1.00E-05	7.80E-10	0.006
85	12.2555	8.509	1.00E-05	1.10E-09	0.006
86	5.842	8.3312	1.00E-05	1.10E-09	0.006
87	5.842	7.0612	1.00E-05	1.10E-09	0.006
88	12.2555	2.0447	1.00E-05	1.10E-09	0.006
89	5.842	4.5212	1.00E-05	1.10E-09	0.006
90	5.842	3.2512	1.00E-05	1.10E-09	0.006
91	1.4097	0.8255	1.50E-03	7.81E-09	0.0078
92	2.5654	0.8255	1.50E-03	7.81E-09	0.0078
93	2.7686	2.0066	1.50E-03	7.81E-09	0.0078
94	1.6256	1.9812	1.50E-03	7.81E-09	0.0078
95	3.9243	2.1844	1.50E-03	7.81E-09	0.0078
96	5.0902	2.1869	1.50E-03	7.81E-09	0.0078
97	0.508	1.7145	1.50E-03	7.81E-09	0.0078

Appendix B. Locations of Via Holes for Kodak Power Distribution Network

Via #	x (cm)	y (cm)	Via #	x (cm)	y (cm)	Via #	x (cm)	y (cm)
1	2.963	1.1868	35	3.09	1.3138	69	3.09	1.4408
2	0.423	1.4408	36	2.455	1.0598	70	2.7115	3.0918
3	3.471	1.5678	37	2.4728	2.7591	71	2.582	1.4408
4	1.3145	1.4383	38	2.455	1.1868	72	3.0214	3.7116
5	3.344	1.5678	39	2.328	1.1868	73	2.2315	3.4957
6	1.378	1.5881	40	2.328	1.0598	74	1.947	1.1868
7	3.598	1.5678	41	2.996	3.483	75	3.0265	3.2137
8	3.598	1.4408	42	2.201	1.4408	76	2.836	1.0598
9	3.344	1.9488	43	2.643	1.6161	77	0.931	1.0598
10	3.598	1.3138	44	2.201	1.1868	78	1.947	1.0598
11	3.725	1.3138	45	2.135	2.345	79	0.804	1.6948
12	3.598	1.0598	46	2.201	1.0598	80	0.55	1.5678
13	3.725	1.0598	47	1.9775	3.7014	81	3.598	1.6948
14	3.471	1.0598	48	1.82	1.0598	82	3.471	1.9488
15	2.582	1.1868	49	1.82	1.1868	83	0.55	4.3618
16	1.2917	3.0156	50	1.693	1.0598	84	0.423	4.3618
17	2.709	1.0598	51	2.8614	1.6161	85	0.423	4.2348
18	5.5106	0.689	52	1.693	1.1868	86	3.598	2.2028
19	2.963	1.0598	53	1.6397	2.4035	87	3.598	2.0758
20	3.09	1.0598	54	1.566	1.4408	88	3.725	1.6948
21	2.8589	2.7895	55	1.566	1.3138	89	3.598	1.9488
22	2.836	1.1868	56	1.566	1.0598	90	3.725	1.5678
23	4.0095	2.6321	57	1.7768	1.9539	91	0.55	1.9488
24	2.643	2.566	58	1.8708	3.5871	92	0.423	2.0758
25	2.4093	1.9971	59	1.566	1.1868	93	4.1111	1.8574
26	2.582	1.0598	60	1.5609	3.0664	94	0.677	2.0758
27	3.344	1.1868	61	1.439	1.1868	95	1.185	4.3618
28	3.344	1.0598	62	2.709	1.3138	96	2.836	4.2348
29	5.5767	0.7728	63	1.312	1.0598	97	0.804	2.2028
30	3.217	1.4408	64	3.725	2.2028	98	1.5558	2.8048
31	3.217	1.1868	65	3.09	4.2348	99	0.423	2.3298
32	3.1687	1.8167	66	0.423	1.5678	100	0.55	2.3298
33	3.217	1.0598	67	3.725	1.1868	101	2.3661	3.2696
34	2.0664	1.0395	68	3.0468	1.8421	102	0.55	2.5838

Via #	x (cm)	y (cm)	Via #	x (cm)	y (cm)	Via #	x (cm)	y (cm)
103	0.423	2.5838	143	3.598	4.1078	183	0.931	4.3618
104	1.025	2.6575	144	3.344	3.9808	184	0.931	4.2348
105	0.804	2.8378	145	3.598	3.9808	185	2.582	4.1078
106	1.1342	3.7039	146	3.598	3.8538	186	2.582	4.2348
107	0.55	2.9648	147	3.344	3.7268	187	0.804	4.3618
108	0.55	3.0918	148	3.471	3.7268	188	0.362	3.7928
109	1.1698	3.229	149	3.598	3.5998	189	0.804	4.2348
110	0.9513	2.7895	150	1.0732	3.3814	190	2.582	4.3618
111	0.55	3.2188	151	1.9318	3.2747	191	1.1799	3.8335
112	0.55	3.3458	152	3.471	3.3458	192	2.7293	3.6963
113	0.677	2.2028	153	3.1052	3.6608	193	2.709	4.3618
114	0.55	2.2028	154	3.725	3.3458	194	0.55	1.8218
115	1.058	3.5033	155	3.598	3.2188	195	0.423	1.6948
116	0.55	2.4568	156	3.725	3.0918	196	0.677	1.6948
117	0.423	2.4568	157	3.725	2.8378	197	2.836	4.3618
118	0.804	2.5838	158	3.598	2.8378	198	1.058	4.3618
119	0.55	2.8378	159	3.725	2.4568	199	2.201	3.9808
120	1.6397	2.8607	160	0.423	3.3458	200	4.0933	2.8378
121	0.423	2.8378	161	0.677	3.4728	201	1.312	4.2348
122	0.423	2.9648	162	0.423	3.4728	202	1.312	4.3618
123	0.423	3.0918	163	0.423	3.5998	203	1.439	4.1078
124	0.423	3.2188	164	0.423	3.7268	204	1.566	3.9808
125	3.344	2.3298	165	0.55	3.8538	205	0.55	1.3138
126	2.7725	2.2663	166	3.598	4.3618	206	0.55	1.4408
127	0.677	4.2348	167	3.725	4.3618	207	3.471	4.2348
128	2.836	4.1078	168	3.725	4.1078	208	3.344	4.2348
129	0.677	4.3618	169	3.725	3.9808	209	0.423	3.9808
130	2.201	4.2348	170	3.725	3.8538	210	0.55	3.9808
131	3.725	1.4408	171	3.725	3.7268	211	3.217	4.2348
132	1.185	3.9808	172	3.725	3.5998	212	2.963	3.9808
133	0.55	3.4728	173	3.344	3.5998	213	0.55	4.1078
134	1.0656	3.5998	174	3.725	3.4728	214	0.423	4.1078
135	0.804	3.5998	175	3.598	3.4728	215	3.598	2.3298
136	0.55	3.5998	176	3.725	3.2188	216	3.598	2.5838
137	0.55	3.7268	177	3.344	3.2188	217	3.9104	1.0598
138	0.423	3.8538	178	3.725	2.9648	218	3.725	1.8218
139	0.804	3.8538	179	3.598	3.0918	219	3.725	1.9488
140	2.6887	3.2493	180	3.598	2.9648	220	3.9155	1.8726
141	3.217	3.9808	181	3.1179	3.3255	221	3.725	2.0758
142	3.725	4.2348	182	3.725	2.5838	222	0.804	1.5678

Via #	x (cm)	y (cm)	Via #	x (cm)	y (cm)	Via #	x (cm)	y (cm)
223	3.852	1.6999	263	1.439	1.4408	303	2.4169	2.3552
224	1.058	1.1868	264	1.947	4.1078	304	2.8614	3.7014
225	1.185	1.1868	265	2.328	3.9808	305	2.582	3.7141
226	3.471	4.3618	266	0.55	1.1868	306	1.5914	1.7202
227	0.423	1.8218	267	0.55	1.6948	307	2.582	1.7202
228	0.804	2.0758	268	0.55	4.2348	308	2.8614	1.7202
229	3.471	2.2028	269	0.55	2.0758	309	2.7725	2.7489
230	3.9917	2.0758	270	1.693	1.3138	310	2.4169	3.0664
231	3.344	2.2028	271	1.82	1.4408	311	1.7311	3.0664
232	3.9917	2.4568	272	2.201	1.3138	312	3.217	4.1078
233	0.423	1.3138	273	2.455	4.1078	313	3.344	3.3458
234	0.2452	0.7804	274	2.328	1.4408	314	3.344	3.8538
235	1.185	4.2348	275	2.455	1.3138	315	3.471	3.2188
236	4.0806	1.3773	276	2.709	1.1868	316	0.677	3.5998
237	3.598	1.8218	277	2.836	1.3138	317	0.677	3.8538
238	0.677	1.5678	278	2.709	3.9808	318	0.677	4.1078
239	3.344	4.3618	279	3.09	3.9808	319	0.677	2.4568
240	1.058	1.0598	280	3.09	1.1868	320	0.677	2.8378
241	3.344	2.5838	281	3.344	4.1078	321	3.344	1.8218
242	2.963	4.2348	282	3.344	1.3138	322	0.804	1.4408
243	2.963	4.3618	283	3.344	1.6948	323	0.804	1.8218
244	3.217	4.3618	284	3.344	2.0758	324	3.344	2.8378
245	1.82	3.9808	285	3.344	2.4568	325	2.328	1.3138
246	0.677	3.9808	286	3.344	2.9648	326	1.947	1.3138
247	0.677	1.4408	287	3.471	3.9808	327	1.693	1.4408
248	0.677	1.9488	288	3.471	3.4728	328	1.185	1.3138
249	0.677	2.3298	289	3.471	1.4408	329	0.931	1.3138
250	0.677	2.5838	290	3.471	2.3298	330	0.677	1.8218
251	0.677	3.0918	291	3.471	2.8378	331	0.677	1.3138
252	0.804	3.3458	292	3.471	3.0918	332	3.471	2.5838
253	0.804	3.7268	293	3.598	3.3458	333	3.471	1.8218
254	0.804	4.1078	294	3.598	3.7268	334	3.471	1.3138
255	0.804	1.3138	295	3.598	4.2348	335	3.471	4.1078
256	0.804	2.4568	296	3.598	1.1868	336	3.471	3.8538
257	0.804	2.9648	297	4.487	2.279	337	3.217	1.3138
258	1.058	1.4408	298	4.487	1.9107	338	2.963	1.3138
259	1.058	4.2348	299	1.312	3.7014	339	2.709	1.4408
260	1.693	4.1078	300	1.5914	3.7014	340	2.582	1.3138
261	1.439	4.2348	301	1.312	1.7202	341	2.963	1.4408
262	1.312	4.1078	302	1.7311	2.3552	342	1.947	1.4408

Via #	x (cm)	y (cm)	Via #	x (cm)	y (cm)	Via #	x (cm)	y (cm)
343	1.185	1.4408	352	1.439	3.9808	361	3.471	3.5998
344	0.677	3.2188	353	1.566	4.1078	362	3.344	1.4408
345	0.804	3.4728	354	1.82	4.1078	363	4.5886	1.0598
346	0.804	3.0918	355	1.947	3.9808	364	1.7311	2.8632
347	0.804	3.2188	356	2.201	4.1078	365	2.4169	2.5584
348	0.931	3.9808	357	2.455	3.9808	366	1.7311	2.5584
349	0.931	4.1078	358	2.582	3.9808	367	2.4169	2.8632
350	3.471	2.9648	359	2.836	3.9808	368	4.614	1.7837
351	1.185	4.1078	360	2.963	4.1078			

Appendix C. Port Locations for Decoupling Capacitors on V2 (Gnd)/V4 Planes

Port	Capacitance (μF)	x (cm)	y (cm)
C43	0.01	31.2420	16.0655
C35	0.01	28.1305	15.8115
C39	0.01	30.7975	12.1285
C37	0.01	38.3540	28.9560
C41	0.01	39.1160	28.9560
C44	0.01	28.1305	13.3985
C46	0.01	32.0675	14.7955
C13	0.47	30.7340	16.0655
C10	0.47	28.1305	15.3035
C1	0.47	30.7975	11.9380
C7	0.47	39.1160	28.7020
C4	0.47	28.1305	12.8905
C23	20	31.3055	16.3830
C29	20	27.8130	15.5575
C13	20	31.4325	12.0650
C21	20	38.3540	28.4480
C27	20	39.1160	28.4480
C31	20	32.3850	14.6685
C25	20	27.8130	13.0175
C19	0.47	32.0675	14.2875
C16	0.47	38.3540	28.7020

Appendix D. Port Locations for Macro-models

2.5 V Power Distribution Network

Port#	x(cm)	y(cm)	Layers
1	32.385	14.669	V4/V2(Gnd)
2	38.354	28.702	V4/V2(Gnd)
3	38.100	29.337	V4/V2(Gnd)
4	26.670	25.019	V4/V2(Gnd)
5	42.037	19.050	V4/V2(Gnd)
6	40.005	19.050	V4/V2(Gnd)
7	40.513	10.922	V4/V2(Gnd)
8	42.545	10.922	V4/V2(Gnd)
9	32.131	10.351	V4/V2(Gnd)
10	28.638	12.954	V4/V2(Gnd)
11	31.115	14.796	V4/V2(Gnd)
12	31.178	13.335	V4/V2(Gnd)
13	29.691	13.957	V1/Gnd
14	30.611	14.351	V1/Gnd
15	30.611	13.647	V1/Gnd

3.3 V Power Distribution Network

Port#	x(cm)	y(cm)	Layers
16	36.576	29.337	V8/V2(Gnd)
17	29.691	13.957	V2(split)/Gnd
18	30.611	14.351	V2(split)/Gnd
19	30.611	13.647	V2(split)/Gnd

Appendix E. SPICE Netlist for Macro-models

Test vehicle from Sun Microsystems

```
rsh26  p2     p4     1e-5
rsh24  p2     p6     1e-5
lpv dv p11 2.8n
lpg dg 0   2.8n


.include 'driver.inc'  * file name for dirvers
.subckt (driver) v g o   s_rise=0.5n s_per=10n ov=0
<subckt for macromodel>

* Driver output: in1, in2, in3, in4
xdrv1 dv dg in1 (driver) m=1 s_per=200ns s_rise=10ns ov=0.3
xdrv2 dv dg in2 (driver) m=1 s_per=200ns s_rise=10ns ov=0.3
xdrv3 dv dg in3 (driver) m=1 s_per=200ns s_rise=10ns ov=0.3
xdrv4 dv dg in4 (driver) m=1 s_per=200ns s_rise=10ns ov=0.3


* reference for a vdd1/gnd1 plane pair
wline1 n=1 in1  p1  out1  p2  rlgcfile=sig.rlc   l='20/39.37'
wline2 n=1 in2  p1  out2  p2  rlgcfile=sig.rlc   l='20/39.37'
wline3 n=1 in3  p1  out3  p2  rlgcfile=sig.rlc   l='20/39.37'
wline4 n=1 in4  p1  out4  p2  rlgcfile=sig.rlc   l='20/39.37'


* reference for a vdd2/gnd1 plane pair
tline1u  in1  p5  out1  p66   z0=1508   td=1.5n
tline2u  in2  p5  out2  p66   z0=1508   td=1.5n
tline3u  in3  p5  out3  p66   z0=1508   td=1.5n
tline4u  in4  p5  out4  p66   z0=1508   td=1.5n


* reference for a vdd2/gnd2 plane pair
tline1d  in1  p3  out1  p44   z0=1508   td=1.5n
tline2d  in2  p3  out2  p44   z0=1508   td=1.5n
tline3d  in3  p3  out3  p44   z0=1508   td=1.5n
tline4d  in4  p3  out4  p44   z0=1508   td=1.5n


rsource p2 ps 0.01   * source resistor
vdc ps 0  5.0
```

Test vehicle from IBM

.include 'res_drvn.inc' * file name for dirvers
<subckt for macromodel>

* Ports #: P1, P2, ….., P19
* Driver output: SP1, SP2, ….., SS18
xdrv1 P17 gnd SP1 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv2 P18 gnd SP2 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv3 P18 gnd SP3 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv4 P18 gnd SP4 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv5 P18 gnd SP5 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv6 P18 gnd SP6 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv7 P18 gnd SP7 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv8 P18 gnd SP8 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv9 P18 gnd SP9 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv10 P18 gnd SP10 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv11 P18 gnd SP11 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv12 P18 gnd SP12 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv13 P19 gnd SP13 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv14 P19 gnd SP14 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv15 P19 gnd SP15 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv16 P19 gnd SP16 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv17 P19 gnd SP17 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50
xdrv18 P19 gnd SP18 (res_drvn) s_per=20ns s_rise=700ps s_fall=300ps drvres=50

Tline1p SP1 P13 EP1 P10 Z0=53.3785 TD=79.642ps
Tline2p SP2 P14 EP2 P11 Z0=53.3785 TD=45.305ps
Tline3p SP3 P14 EP3 P11 Z0=53.3785 TD=16.728ps
Tline4p SP4 P14 EP4 P11 Z0=53.3785 TD=51.628ps
Tline5p SP5 P14 EP5 P11 Z0=53.3785 TD=35.066ps
Tline6p SP6 P14 EP6 P11 Z0=53.3785 TD=69.395ps
Tline7p SP7 P14 EP7 P11 Z0=53.3785 TD=25.730ps
Tline8p SP8 P14 EP8 P11 Z0=53.3785 TD=40.092ps
Tline9p SP9 P14 EP9 P12 Z0=53.3785 TD=38.242ps
Tline10p SP10 P14 EP10 P12 Z0=53.3785 TD=29.2ps
Tline11p SP11 P14 EP11 P12 Z0=53.3785 TD=49.272ps
Tline12p SP12 P14 EP12 P12 Z0=53.3785 TD=25.589ps
Tline13p SP13 P15 EP13 P12 Z0=53.3785 TD=50.827ps
Tline14p SP14 P15 EP14 P12 Z0=53.3785 TD=16.462ps
Tline15p SP15 P15 EP15 P12 Z0=53.3785 TD=27.489ps
Tline16p SP16 P15 EP16 P12 Z0=53.3785 TD=35.481ps
Tline17p SP17 P15 EP17 P12 Z0=53.3785 TD=58.359ps

```
Tline18p SP18  P15 EP18  P12  Z0=53.3785  TD=50.356ps

Rpb1   EP1   SB1   5e-6
Rpb2   EP2   SB2   5e-6
Rpb3   EP3   SB3   5e-6
Rpb4   EP4   SB4   5e-6
Rpb5   EP5   SB5   5e-6
Rpb6   EP6   SB6   5e-6
Rpb7   EP7   SB7   5e-6
Rpb8   EP8   SB8   5e-6
Rpb9   EP9   SB9   5e-6
Rpb10  EP10  SB10  5e-6
Rpb11  EP11  SB11  5e-6
Rpb12  EP12  SB12  5e-6
Rpb13  EP13  SB13  5e-6
Rpb14  EP14  SB14  5e-6
Rpb15  EP15  SB15  5e-6
Rpb16  EP16  SB16  5e-6
Rpb17  EP17  SB17  5e-6
Rpb18  EP18  SB18  5e-6


Tline1b   SB1   P10 EB1   P4  Z0=49.06673  TD=873.96ps
Tline2b   SB2   P11 EB2   P6  Z0=49.06673  TD=725.52ps
Tline3b   SB3   P11 EB3   P5  Z0=49.06673  TD=880.1ps
Tline4b   SB4   P11 EB4   P5  Z0=49.06673  TD=850.68ps
Tline5b   SB5   P11 EB5   P6  Z0=49.06673  TD=754.1ps
Tline6b   SB6   P11 EB6   P6  Z0=49.06673  TD=662.06ps
Tline7b   SB7   P11 EB7   P6  Z0=49.06673  TD=793.42ps
Tline8b   SB8   P11 EB8   P5  Z0=49.06673  TD=800.66ps
Tline9b   SB9   P12 EB9   P7  Z0=49.06673  TD=718.37ps
Tline10b SB10  P12 EB10  P8  Z0=49.06673  TD=801.58ps
Tline11b SB11  P12 EB11  P7  Z0=49.06673  TD=666.62ps
Tline12b SB12  P12 EB12  P7  Z0=49.06673  TD=717.12ps
Tline13b SB13  P12 EB13  P8  Z0=49.06673  TD=784ps
Tline14b SB14  P12 EB14  P7  Z0=49.06673  TD=695.31ps
Tline15b SB15  P12 EB15  P8  Z0=49.06673  TD=854.82ps
Tline16b SB16  P12 EB16  P8  Z0=49.06673  TD=812.97ps
Tline17b SB17  P12 EB17  P8  Z0=49.06673  TD=874.7ps
Tline18b SB18  P12 EB18  P9  Z0=49.06673  TD=187.18ps


Vdc25 P3 gnd  2.5     * DC source for 2.5 V power distribution network
Vdc33 P16 gnd  3.3    * DC source for 3.3 V power distribution network
```

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Awards / Patents

1. Student Best Paper Award at the 9th Topical Meeting on Electrical Performance of Electronic Packaging, Phoenix, Arizona, Oct'00.

2. 1st Place, Poster Contest, Annual NSF-PRC Meeting, Georgia Tech, 2000.

3. Invention Disclosure:
   Inventors: **Joong-Ho Kim** and Madhavan Swaminathan
   Title: Modeling of Arbitrarily Shaped Power Distribution Systems
   ID #: 2368
   Date: September 8, 2000
   Provisional patent application has been filed.

VITA

Joong-Ho Kim was born in Korea, on Feb. 8, 1969. He graduated from Kyung-Bock High School, Seoul, Korea, in 1987. He received the B.S.ECE degree in electrical and computer engineering in 1998 from Ohio State University, Columbus, Ohio and the M.S.ECE in 2000 and Ph.D degrees in 2002 from Georgia Institute of Technology, Atlanta, Georgia.

To pursue his Ph.D in electrical and computer engineering, Kim began his research in 1999 and has been a Graduate Research Assistant in the Packaging Research Center. He has contributed to several publications in the signal and power integrity area. His current research interests are the modeling and simulation of power distribution networks. He was awarded 1st Place (Poster Contest) at the Annual NSF-PRC Meeting, Georgia Tech, 2000 and received the Best Student Paper Award at Topical Meeting on Electrical Performance of Electronic Packaging (EPEP), Phoenix, Arizona, 2000.

In 2002, Kim joined the packaging group for signal/power integrity in Intel, Phoenix, Arizona to work on signal and power integrity.

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