

Modeling and Simulation of Planes in Electronic Packages

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Modeling and Simulation of Planes in Electronic Packages

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CHAPTER 1

Introduction

As clock frequency and chip integration levels increase in a digital system, simultaneous switching noise (SSN) generated on the power distribution network of packages is becoming a serious problem. This causes various signal integrity concerns in high speed digital systems. This problem continues to grow, limiting the system performance as microprocessor speeds increase. These speeds almost double with each new microprocessor generation. Simultaneous switching noise needs to be suppressed for packages and modules, especially in large scale and high performance CMOS systems. Such high performance systems have many fast output drivers that switch simultaneously to transfer data between processor and memory in a short time duration. A large voltage spike generated by the active output drivers can propagate to quiet drivers or internal logic circuits, and can cause logic errors during the operation of digital systems. Similarly the internal logic circuits switching simultaneously within a microprocessor can cause fluctuation on the power supply rails of the chip. Simultaneous switching noise and methods for noise reduction have been investigated over the years for designing high performance chips. These methods involved the development of equivalent circuit models for simulating the noise in a circuit simulator such as SPICE.

1.1 Switching Noise in Power Distribution Networks

Simultaneous switching noise, also called ground bounce or ΔI noise, is a complex

phenomena that deteriorates the system performance, causing voltage fluctuations on the power supply. The switching noise combined with coupled noise can be transmitted to signal lines or quiet drivers, as shown in Fig. 1.1. This can cause waveform distortion in the time domain and serious signal delays for off-chip drivers. Due to this, the overall system performance deteriorates limiting the system cycle time [1],[2]. If the distortion occurs below the receiver's threshold, then increased delay (order of a few hundred picoseconds) will be present on every line that emanates from the cluster of switching drivers. A negative noise generated by the off-chip drivers in Fig.1 causes a spurious signal to propagate through the quiet driver and the transmission line, ultimately appearing at the quiet receiver's input. When this noise exceeds the receiver's noise tolerance, the receiver's output will be greater than its input. As a result, the noise travels through the logic circuits that the receiver is connected to, growing in amplitude, until it finally sets a down stream latch into a wrong state, causing a system datum error.

Modern CMOS microprocessors and ASICs have millions of circuits consisting of many internal circuits and hundreds of external drivers all switching within one time cycle. As will be shown later, the switching noise is directly proportional to each driver's current slew rate and so all of this simultaneous switching can cause hundreds or even thousands of millivolts (mV) of noise between the power supply rails (V_{dd} or GND) of the chip [3]-[7]. When the amplitude of this noise approaches one-half of the CMOS signal swing (VDD), which is the approximate noise tolerance of a static CMOS circuit, a signal error can occur. This noise becomes a major problem with advances in CMOS technology that results in faster device speeds.

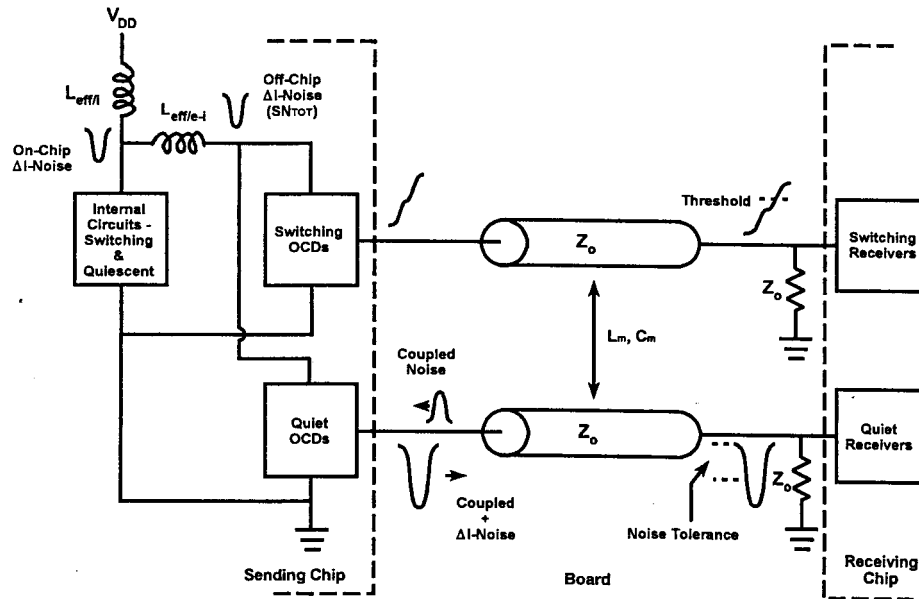


Fig. 1.1 Switching and coupled noise on signal Lines [1]

Fig. 1.2 shows the measured noise on a quiet line as a function of the number of switching drivers for two types of slew rates in a CMOS ASIC chip [3]. In Fig. 1.2, the noise increases linearly with the number of switching drivers and ultimately saturates due to excessive noise on the power supply rails. Fig. 1.3 shows the ground bounce waveforms measured for a multichip module by varying the number of switching drivers [4].

1.2 Effect of Switching Noise on Signal Integrity and Performance

The reference voltage fluctuation due to the ground bounce also brings several other signal integrity issues such as signal delay and clock skew.

Let V_{DD} and V_{dd} be the desired reference power and a new power level shrunk due to the switching noise as in Fig. 1.4a, respectively.

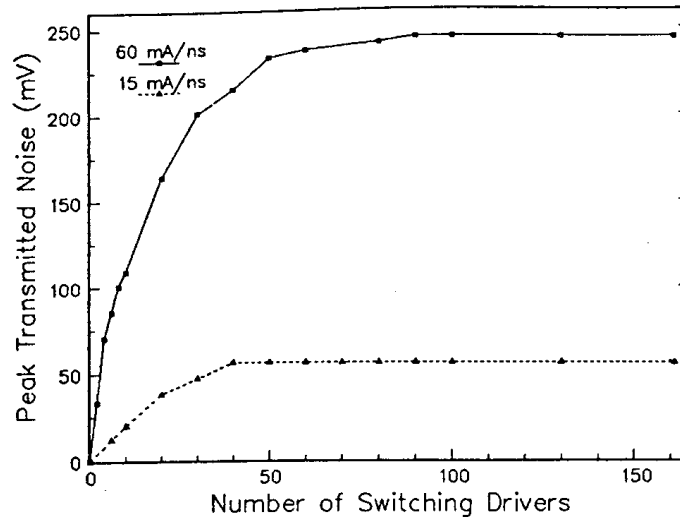


Fig. 1.2 Quiet line peak transmitted noise measured as a function of the number of switching drivers in a CMOS ASIC chip [3]

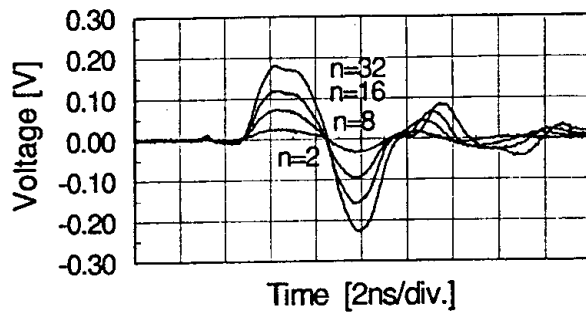


Fig. 1.3 Ground noise waveforms measured on a MCM-C substrate [4]

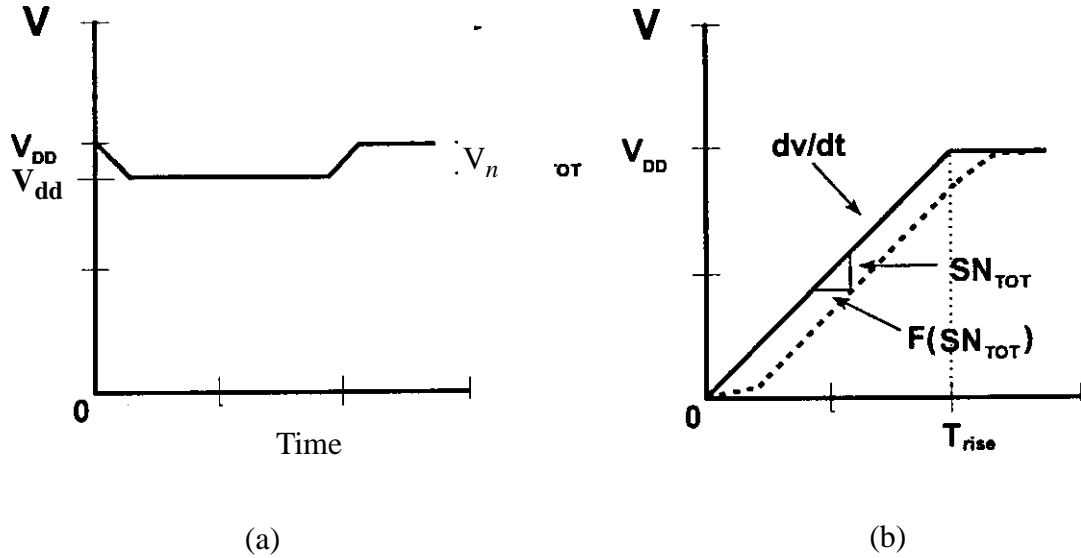


Fig. 1.4 (a) Power supply shrink and (b) signal delay due to switching noise

The signal waveform can be represented as

$$V(t) = V_{dd}(1 - e^{-t/\tau}) \quad (1.1)$$

where $V_{dd} = V_{DD} - \Delta V$ and τ is the time constant. The voltage slew rate of the signal can be computed as [8]

$$\left. \frac{dV}{dt} \right|_{t=0} = \frac{V_{dd}}{\tau} \quad (1.2)$$

In (1.2), since $V_{dd} < V_{DD}$, the signal slows down as illustrated in Fig. 1.4.

Gate delays of a CMOS circuit can be computed as [9]

$$T_d = 0.7 \cdot \frac{L/W}{\mu \cdot C_{ox}(V_{DD} - V_T)} \cdot C_L \quad (1.3)$$

where μ is the mobility, L is the channel length, W is the channel width, C_{ox} is the gate oxide capacitance, C_L is the load capacitance and V_T is the threshold voltage. When V_{DD} is reduced due to power supply noise, the delay of the circuit increases.

The voltage fluctuation on the chip power supply rails due to switching noise also affects the clock distribution network causing clock skews in the systems as illustrated in Fig. 1.5.

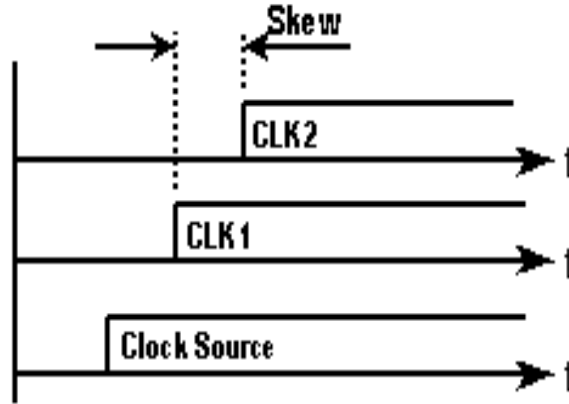


Fig. 1.5 Clock skew [9]

The clock skew can be derived as [9]

$$T_{ClockSkew} = 0.7R_{tr}C_L \left(\frac{V_{DD}}{V_{DD} - V_T} \right) \left(\frac{V_{DD} - V_{dd}}{V_{DD}} \right) \quad (1.4)$$

where R_{tr} is the source-drain resistance of the driver. Any reduction in the power supply voltage causes the clock skew to increase.

1.3 Effective Inductance

Simultaneous switching noise in the past has been attributed to the increase in the total current slew rate of the output buffers and the effective inductance of the power distribution network of the package, as discussed in [1]

$$V_{\Delta I} = N L_{eff} \frac{di}{dt} \quad (1.5)$$

where

di/dt = Current slew rate of a single driver

L_{eff} = Effective inductance of the power distribution system

N = Number of simultaneously switching drivers

$V_{\Delta I}$ = Voltage variation

L_{eff} accounts for all the parasitic inductances along the current path in the package. This includes the current path for the internal circuits on the chip, the external off-chip current loop and chip to module or module to module connections. However, L_{eff} is only meaningful as a figure of merit and as an approximation that can be used for estimating ΔI noise because at high frequencies the package is too complex to be represented by a single lumped inductor. In reality, the package is a multi port pole-zero network [1][5].

To properly model SSN, all the parasitic inductances, resistances and capacitances along the power distribution path including planes and wires at each package level should

be considered. L_{eff} in (1) can vary based on the current path in the package. Current distribution in the package can vary based on the position of the signal conductor with reference to the ground planes, locations of the sink and source points, vias, and the switch direction of the drivers. Hence the effective inductance for a package is not unique and can vary as shown in Fig. 1.6, where a strong image current is formed underneath the signal line, which travels back to the source point and completes the current loop at the ground pin. This is the shortest path to the ground pin which results in an increase in the inductance of the ground plane as compared to the case where the sink point would have been located close to the signal source point.

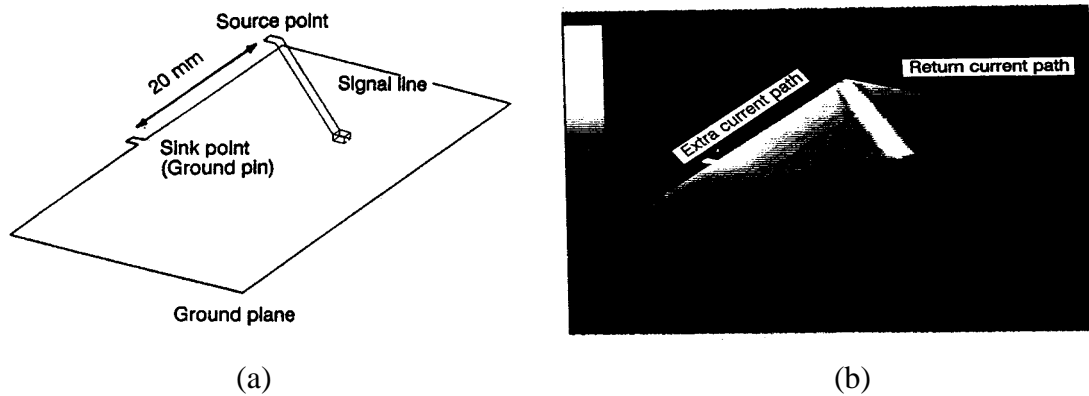


Fig. 1.6 (a) Physical structure of the interconnect above a ground plane and (b) the simulated result showing the current density on the plane.

1.4 Plane Modeling in Power Distribution Networks

Accurate prediction of SSN and its effects on the circuit behavior is possible through appropriate modeling of the power distribution network and simulation of their electrical behavior. Simulation of the electrical behavior in the package should take into account

interactions between the components and the electromagnetic behavior of the package. With the ever increasing need for electromagnetic (EM) modeling of high-speed digital circuits and packages, various transient electromagnetic field solvers have been used to model packages. These include the Finite Difference Time Domain (FDTD) method, the Partial Element Equivalent Circuit (PEEC) method and Method of Moments (MoM), to name a few. These methods have been used successfully for the electromagnetic simulation of simple structures such as a few interconnects over a small section of a plane. Package structures, such as planes, however, are electrically large and can contain numerous vias. Even with significant advances in numerical techniques for the electromagnetic modeling of packages, the analysis of an entire package often becomes computationally prohibitive due to severe demands on memory and CPU time.

In the past, the power distribution network was either modeled as a lumped inductor or as an inductive network which is suitable for lead frame packages such as QFPs and DIPs [5][6]. In packages supporting high speed microprocessors or ASICs, planes are used to distribute power to the chip as shown in Fig. 1.7. Hence planes form an integral part of the power distribution network in modern packages.

At high frequencies the power distribution network supports wave propagation and the planes behave as cavity resonators supporting radial waves that propagate between the plane pairs. The reflection of these waves at the plane edges causes resonances in the package in the steady state. This behavior can be captured by computing the impedance of the power distribution system which includes the wave propagation effects. While designing planes in a package, the input impedance seen by the chip and the trans-impedance between the chip and other parts of the power distribution network have to be controlled,

over a large frequency spectrum up to 1 GHz and above, to control the noise levels, as discussed in [10].

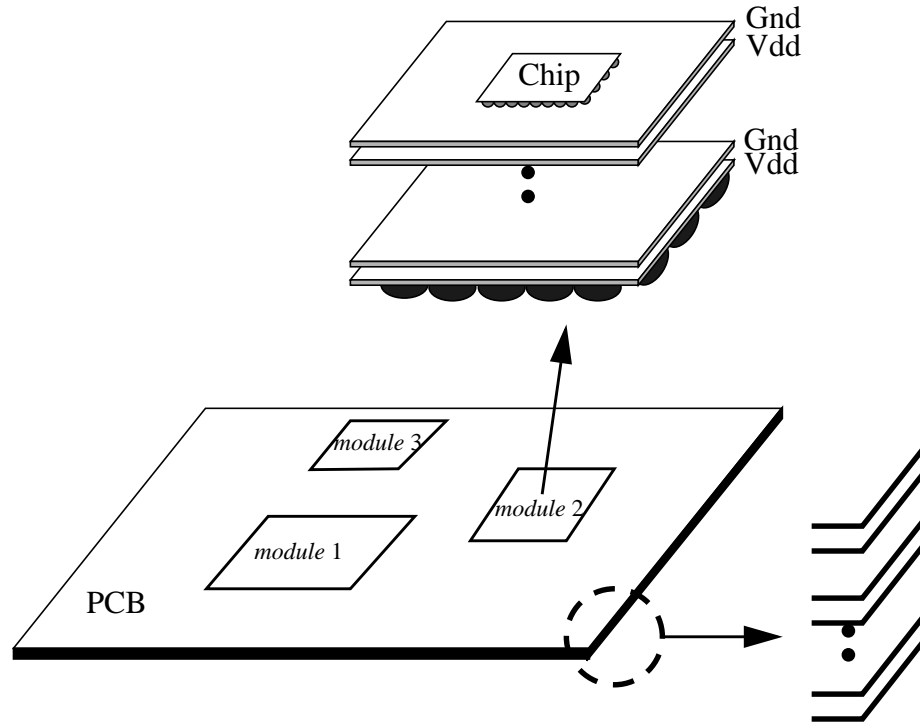


Fig. 1.7 Multi-layered high frequency package

Fig. 1.8 illustrates a method for modeling such a multi-layered package as an inductance network [11]. Propagation of waves in a medium requires the presence of both inductance and capacitance in the network. In addition, the wave attenuation requires the presence of resistance in the network. Hence a pure inductance network for modeling power distribution is inaccurate at high frequencies. Since planes perform a critical function, their response has to be accurately predicted, simulated and understood for designing high speed systems [12]. Some of the methods that have been used in the past for modeling planes are a) Partial Element Equivalent Circuit [13] b) Method of Moments [14] c)

Finite Difference Time Domain [15] and d) Transmission Line approach [16]. The first three are numerical methods that solve Maxwell's equation over an enclosed volume or a surface. Since planes are electrically large, these methods are often computationally expensive.

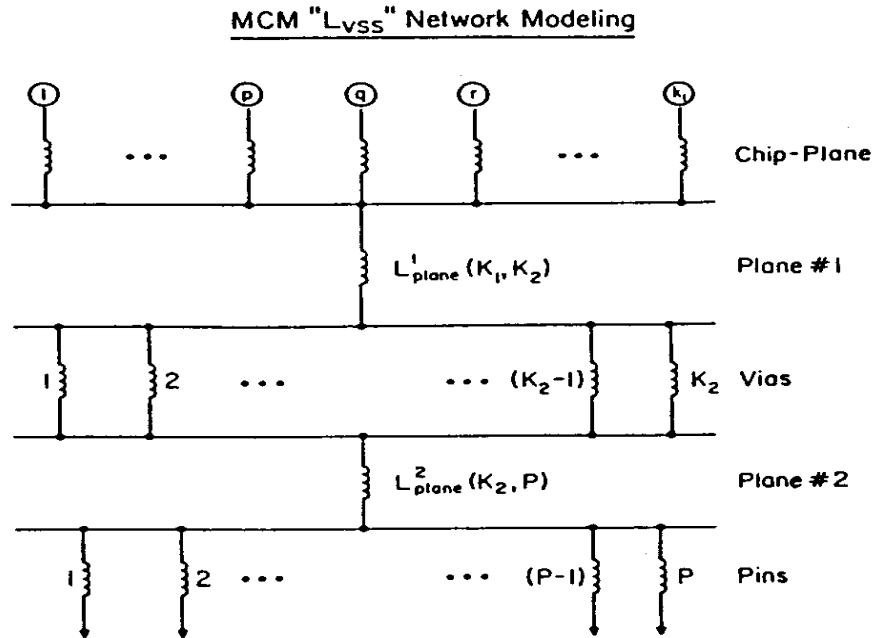


Fig. 1.8 Inductance network for a multi-layered structure

The transmission line approach uses an array of transmission lines for analyzing the structure as shown in Fig. 1.9. The method uses a finite fixed grid with the grid spacing defined by the highest frequency content of the signal. This approach can lead to large simulation time, especially when packages are mounted on printed circuit boards due to the granularity required.

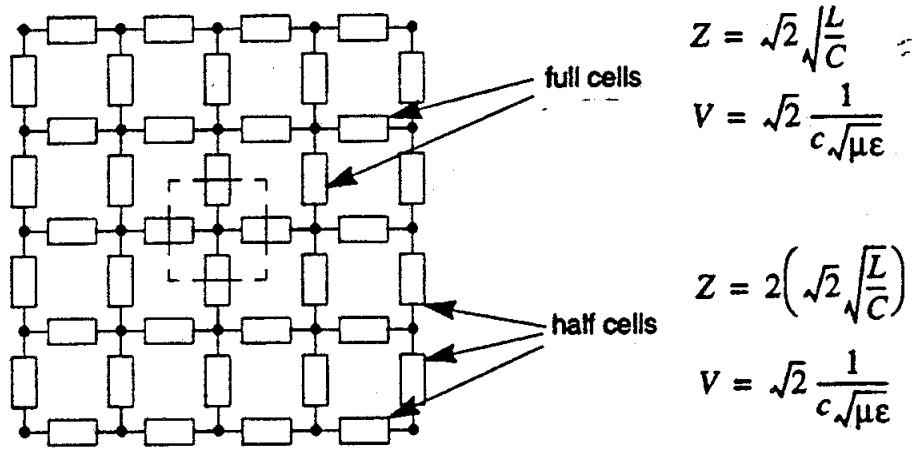


Fig. 1.9 Transmission line modeling for a plane structure [16]

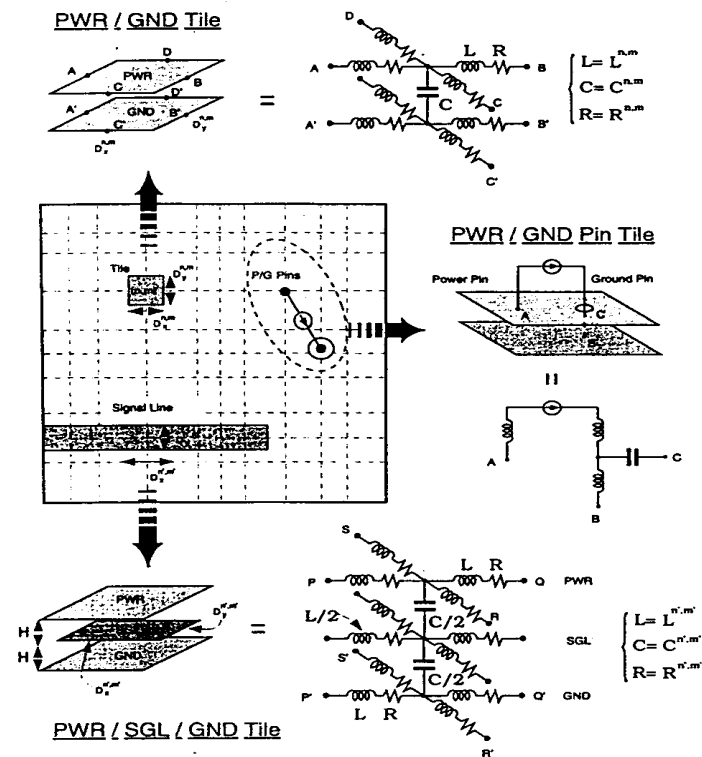


Fig. 1.10 Distributed network modeling for a plane structure [17]

Another approach in SPICE uses a distributed RLC network to model the plane structures as shown in Fig. 1.10 [17]. This method uses a nonuniform gridding algorithm according to the discontinuities involved and lumped circuit elements are derived using full-wave electromagnetic field simulations. In both transmission line approach and distributed network approach the electrical dimensions of the partitioned cells must be less than a tenth of a wavelength at the highest frequency of the signal. This can lead to large networks and prohibitively large simulation time.

Hence, there is a clear need for more efficient and accurate modeling methods for modeling planes in high performance packages that capture the high frequency behavior. Some important issues for modeling planes are:

- Inductance network which is the most commonly used cannot capture the complex behavior of multi pole-zero system response involving plane resonances in packages.
- Since structures are electrically large and need to be analyzed over a large spectrum of frequency, full wave EM modeling methods or the methods that partition structures may not be computationally efficient.
- Equivalent circuits with reduced order are required for simulation with other circuit components to estimate overall performance.
- Sometimes planes in power distribution networks are designed as irregular shapes based on space availability or for isolation of propagated noise. These structures also need to be analysed accurately.
- The modeling method should be extendable for analyzing multi-layered packages and boards with multiple plane stack-ups.

- Decoupling capacitors form an integral part of power distribution networks. Hence the modeling method should be capable of analyzing planes with decoupling capacitors to understand issues such as placement, parasitics, etc..
- Core switching noise estimation requires the analysis of the whole system. Hence, the modeling method should capture all the above effects for investigating the noise on any component of the circuit in both the frequency and time domain.

1.5 Proposed Research and Dissertation Outline

Based on the issues for analyzing switching noise in high performance systems, the following research is proposed:

1. Development of an analytical method for modeling planes in electronic packages. For the accurate prediction of simultaneous switching noise and for noise reduction, power distribution networks in packages need to be electrically modeled and analyzed. The complex behavior of planes at high frequencies need to be predicted accurately through modeling and simulation.
2. Development of model order reduction methods for generating compact, efficient and passive models. The analytical solution proposed for planes includes infinite number of modes, which is not computationally efficient. A method to reduce the model order is therefore desired for simulation, that provides accurate results over the frequency band of interest. An algorithm has been developed to determine the minimum number of modes that are required for computing the response.

3. A method is proposed for incorporating decoupling capacitors. This method could be used for the optimum placement of decoupling capacitors to suppress noise in a system.
4. Transient Measurements and verification of the modeling method. A test vehicle has been designed and fabricated for transient measurements. The methods developed have been verified through correlation with measured data.
5. Development of S-parameter based equivalent circuits using macromodels for power distribution networks. S-parameters are suitable for modeling microwave circuits in the frequency domain. They enable a further reduction in the model size by eliminating the internal nodes in the network. The method proposed enables the incorporation of reduced S-parameter models into SPICE using rational functions.
6. Enforcement of the passivity condition for macromodels. Macromodeling in 5 doesn't guarantee the passivity of the network response during simulation. The conditions for ensuring passive system behavior during simulation are studied in this research. The goal is to develop a method for ensuring the passivity of circuits and synthesizing equivalent circuits.
7. Development of methods for modeling irregular geometries. In particular, the goal of this research is to develop algorithms that account for large cut-outs on package planes. These algorithms will be used to develop SPICE circuit models.
8. Application of the research items 1 to 7 for modeling the core noise in a test system.

The remainder of this thesis is organized as follows. Chapter 2 presents impedance computation of plane pairs and implementation of equivalent circuits based on a model

order reduction method. In Chapter 3, transient measurements on a test vehicle and simulation results are discussed to verify the modeling method discussed in Chapter 2. In Chapter 4, impedance computation of irregular shaped planes using the segmentation method is discussed. In Chapter 5, decoupling capacitors are incorporated into the plane model and the impedance of the decoupled structure is computed. A method for generating reduced order models (macromodels) using rational functions is discussed in Chapter 6. Macromodels developed in Chapter 6 are not guaranteed to be passive even though the original network is passive. In Chapter 7, methods to preserve the passivity of the impedance macromodels are discussed for one-port and two-port systems. In Chapter 8, various simulations of core switching noise have been conducted for the CMOS5L test vehicle supplied by IBM. These simulations are based on the modeling method described in this dissertation. The conclusion and recommendation for future work are provided in Chapter 9.

CHAPTER 2

Modeling of Planes

The impedance at the ports on regular shaped plane pairs can be solved analytically from Maxwell's equations and represented as the sum of infinite number of wave modes as discussed in [18] and [19]. By using the analytical solution, ports can be placed at arbitrary locations on the plane and the frequency response of the ports can be computed. Each wave mode in the nonlinear solution for the impedance can be represented as a parallel resonator circuit through linearization, as discussed in [23]. Then the equivalent circuit for the port response can be implemented directly from the equations using resonant circuits and transformers [23]. Since the equivalent circuit consists of passive lumped elements, the circuit is guaranteed to be passive. In this chapter, the analytical solution for the impedance of solid plane pairs is briefly reviewed and a model order reduction method is developed to implement a low order equivalent circuit.

2.1 Impedance Computation

Consider a plane structure as shown in Fig. 2.1 which consists of two planes of dimensions axb , separated by a dielectric of thickness ' d ' and permittivity ' ϵ '. Since $a,b \gg d$ where $d \ll \lambda$ (the wavelength), the major field components are E_z , H_x and H_y where ' E ' is the electric field, ' H ' the magnetic field and the subscripts represent the field directions.

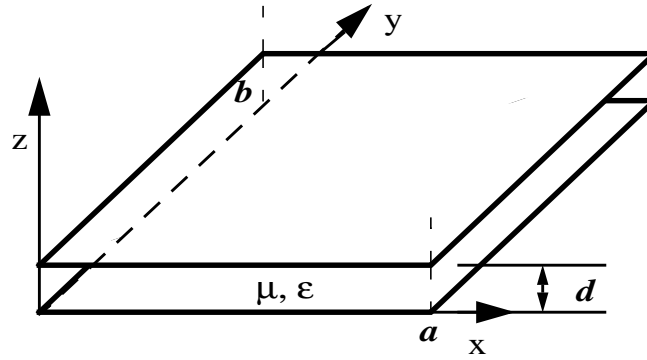


Fig. 2.1 Physical structure of a plane pair

Since the edges in Fig. 2.1 represent a magnetic wall, the impedance matrix at arbitrary ports on the plane can be computed for a low loss structure as[18],[19]:

$$Z_{ij}(\omega) = j\omega\mu d \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{\epsilon_n^2 \epsilon_m^2}{(k_{mn}^2 - k^2)ab} f(x_i, y_i, x_j, y_j) \quad (2.1)$$

where

$$f(x_i, y_i, x_j, y_j) = \cos \frac{m\pi x_i}{a} \sin c \frac{m\pi y_i}{2a} \cos \frac{n\pi x_j}{b} \sin c \frac{n\pi y_j}{2b} \cos \frac{m\pi x_j}{a} \sin c \frac{m\pi y_j}{2a} \cos \frac{n\pi x_i}{b} \sin c \frac{n\pi y_i}{2b}$$

$$k = k' - jk'' \text{ with } k' = \omega\sqrt{\epsilon\mu} \text{ and } k'' = \omega\sqrt{\epsilon\mu}(\tan\delta + r/d)/2,$$

$$k_{mn}^2 = (m\pi/a)^2 + (n\pi/b)^2,$$

$$r = 1/\sqrt{\pi f \mu \sigma} \text{ the skin depth,}$$

δ the dielectric loss angle,

ϵ the permittivity

μ the permeability

$$\epsilon_m, \epsilon_n = 1 \text{ for } m, n=0 \text{ and } \sqrt{2}, \text{ otherwise,}$$

m, n the propagating modes,

$(x_i, y_i), (x_j, y_j)$ the co-ordinates of the port locations,

and $(t_{xi}, t_{yi}), (t_{xj}, t_{yj})$ the dimensions of the ports.

(2.1) is the solution for a radial wave propagating between the planes. The accuracy of (2.1) has been discussed for 1 port in [19] up to 8 GHz. Various measurements for a test board, the data of which are available in [20], have been conducted to examine the accuracy of the solution [21]. The test board consists of a plane pair of 12" x 10" size with a spacing of 8 mils and 15 ports connected to SMA connectors for S-parameter measurement, as shown in Fig. 2.2. The Z parameters have been calculated for 15 ports using (2.1) and converted to S parameters using the transformation:

$$S = (Z + [Z_o])^{-1}(Z - [Z_o]) \quad (2.2)$$

where $[Z_o]$ is the characteristic impedance matrix at the ports:

$$[Z_o] = \begin{bmatrix} Z_{o1} & & & & \\ & Z_{o2} & & & \\ & & \cdot & & \\ & & & \cdot & \\ & & & & Z_{on} \end{bmatrix}$$

S parameters between ports 8 and 3 and also between ports 8 and 10 were computed from (2.1) and (2.2). Results are shown in Figs 2.3, 2.4 and 2.5. Figs 2.3 and 2.4 show reflection (S11) at port 8 and transmission (S12) for the 2 port structure between ports 8 and 3. Fig. 2.5 shows the transmission between ports 8 and 10. The results agree well with the measured data shown in [20]. It is important to note that these results were computed without the effect of the SMA connectors.

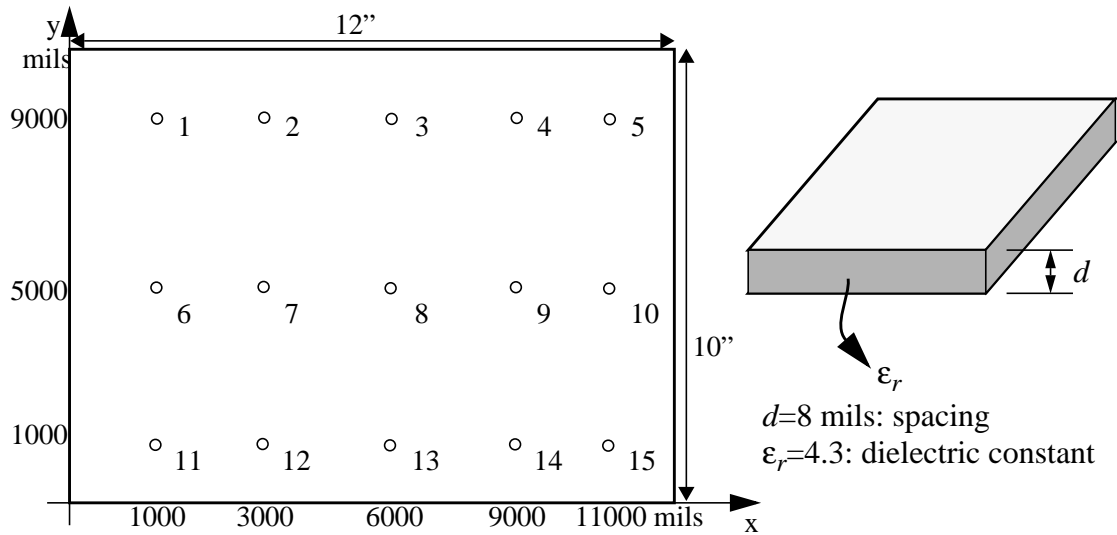


Fig. 2.2 The board structure in [20] for S-parameter simulation (Refer to Fig. 3 in [20])

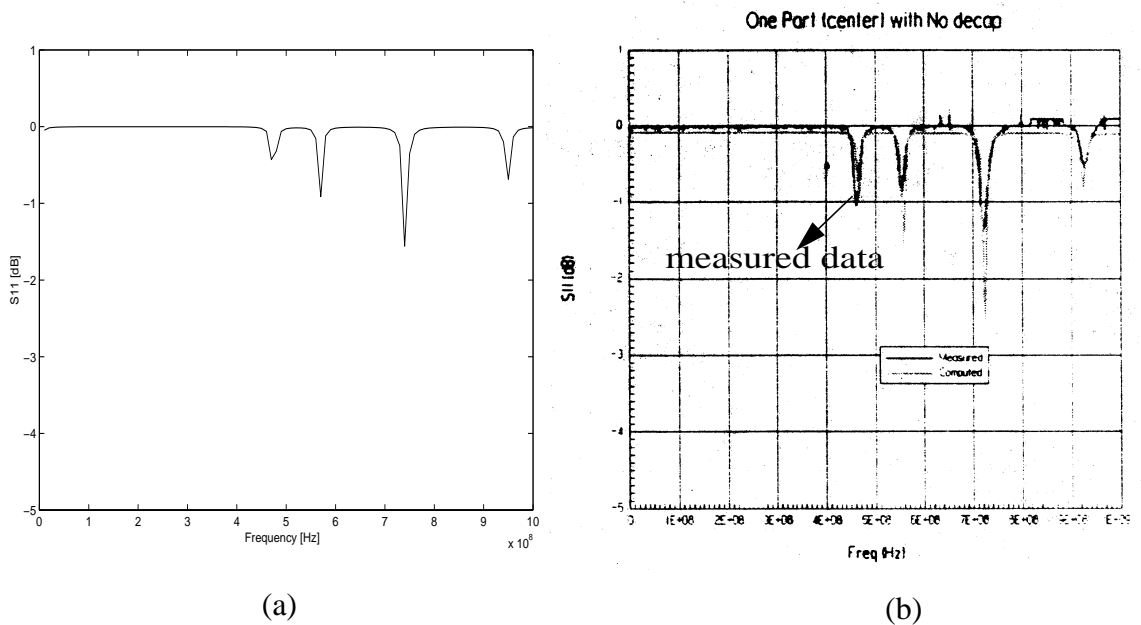


Fig. 2.3 Reflection(S_{11}) at port 8 with 2 port structure between ports 8 and 3:
 (a) computation from (21) and (2.2), (b) measured data[20]

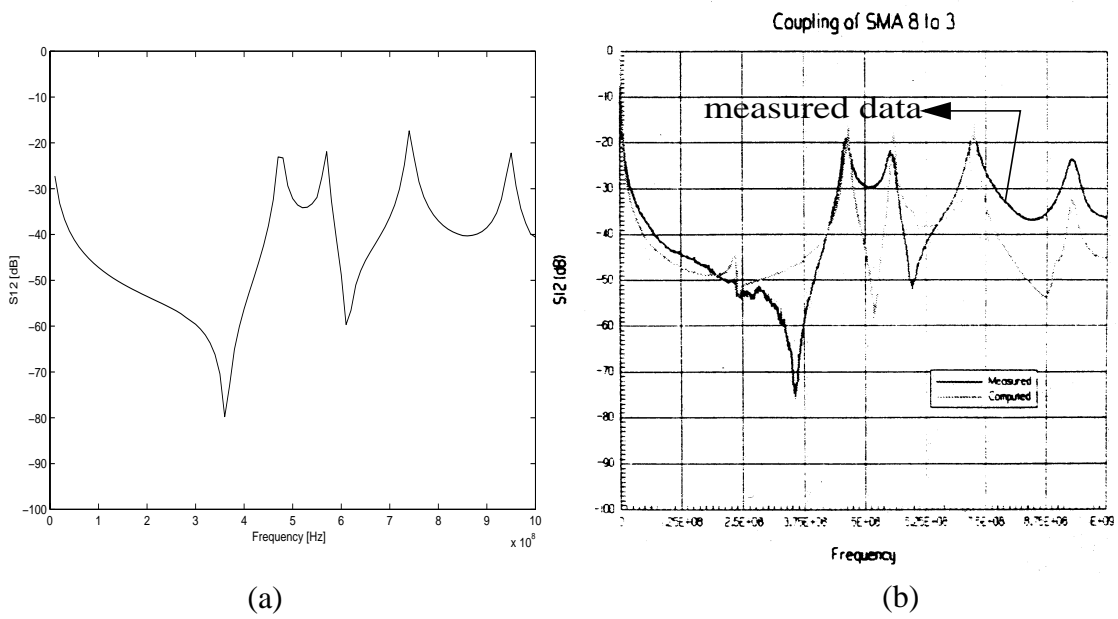


Fig. 2.4 S_{12} with two-port structure between ports 8 and 3:
 (a) computation from (2.1) and (2.2), (b) measured data[20]

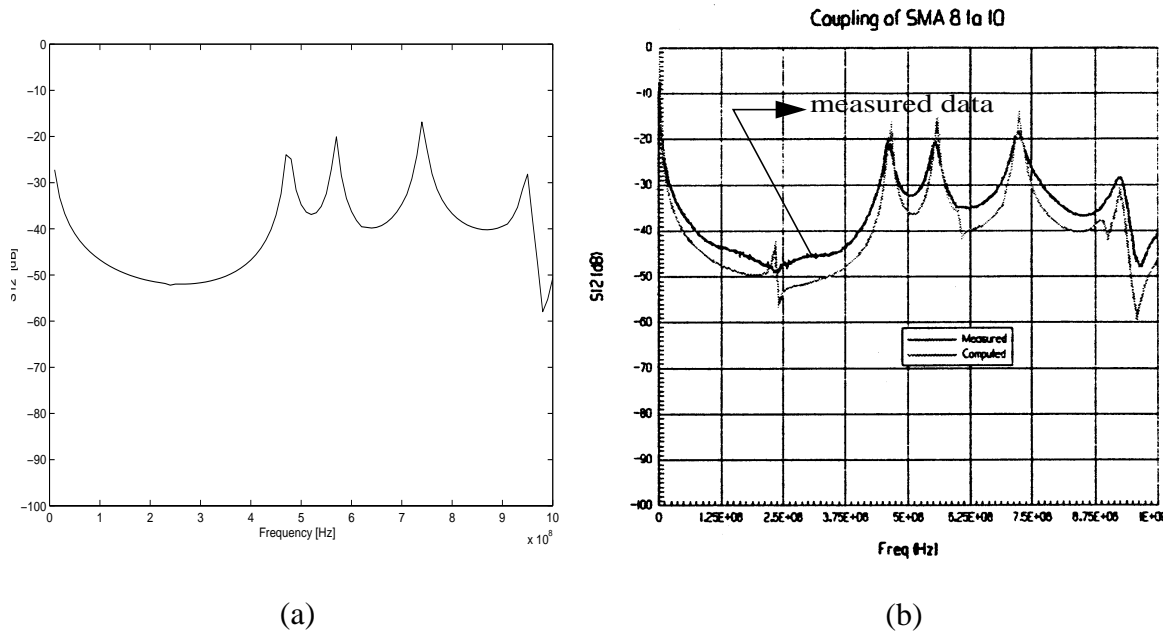


Fig. 2.5 S_{12} with two-port structure between ports 8 and 10:
 (a) computation from (2.1) and (2.2), (b) measured data [20]

During computation, the mode numbers used were $m=0$ to 20 and $n=0$ to 20. These numbers will be used as a reference for generating reduced order models in the next section on model order reduction.

2.2 Model Order Reduction

From (2.1), it can be seen that an infinite number of modes are required to obtain the response for two planes. It is not computationally efficient to construct the circuit with an arbitrarily large number of modes since this can lead to prohibitively large simulation time. In this section, effects of the modes on the response are investigated and a guide is suggested to find the minimum set of mode numbers to obtain accurate results.

Consider the test structure shown in Fig. 2.2 which consists of 2 planes of 12" x 10" with the separation of 8 mils between the planes (dielectric thickness) and a relative dielectric constant of 4.3. In the previous section, good correlation between (2.1) and measurements was demonstrated for the transmission between ports 8 and 3 with $m,n=0$ to 20 modes. In this section, these results will be used as a reference to develop an algorithm to determine the minimum number of modes that are required.

Assuming $k' \gg k''$, k^2 in (2.1) is approximated as:

$$\begin{aligned} k^2 &= \omega^2 \epsilon \mu \left(1 - j \left(\tan \delta + \frac{1}{d \sqrt{\pi f \mu \sigma}} \right) \right) \\ &= \omega^2 \epsilon \mu \left(1 - j \left(\tan \delta + \frac{\sqrt{2}}{d \sqrt{\omega \mu \sigma}} \right) \right) \end{aligned} \quad (2.3)$$

Since the resonant frequency of the structure in Fig. 2.1 for the ' mn ' mode is [18],[22]

$$f_{mn} = \frac{\sqrt{(m/a)^2 + (n/b)^2}}{2\sqrt{\epsilon\mu}} \quad (2.4)$$

k_{mn} in (2.1) is written as

$$k_{mn} = 2\pi f_{mn}\sqrt{\epsilon\mu} = \omega_{mn}\sqrt{\epsilon\mu} \quad (2.5)$$

Using (2.3) and (2.5) the impedance equation in (2.1) can be rewritten as:

$$\begin{aligned} Z_{ij}(\omega) &= \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{j\omega}{\omega_{mn}^2 - \omega^2 + j\omega^2(\tan\delta + (\sqrt{2}/\omega\mu\sigma)/d)} \Gamma_{ijmn} \\ &= \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{j\omega}{\omega_{mn}^2 + (j\omega)^2 + j\omega \cdot \omega(\tan\delta + (\sqrt{2}/\omega\mu\sigma)/d)} \Gamma_{ijmn} \end{aligned} \quad (2.6)$$

where

$$\Gamma_{ijmn} = \frac{d}{ab\epsilon} \epsilon_n^2 \epsilon_m^2 \cos\frac{m\pi x_i}{a} \operatorname{sinc}\frac{m\pi t_{xi}}{2a} \cos\frac{n\pi y_i}{b} \operatorname{sinc}\frac{n\pi t_{yi}}{2b} \cos\frac{m\pi x_j}{a} \operatorname{sinc}\frac{m\pi t_{xj}}{2a} \cos\frac{n\pi y_j}{b} \operatorname{sinc}\frac{n\pi t_{yj}}{2b}$$

Assuming low dielectric loss ($\tan\delta \ll r/d$) and approximating the loss in the third term of the denominator near the resonant frequencies [18],[23], equation (2.6) is further simplified as:

$$Z_{ij}(\omega) = \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{j\omega}{\omega_{mn}^2 + (j\omega)^2 + j\omega \cdot \omega_{mn}(\sqrt{2}/\omega_{mn}\mu\sigma)/d} \Gamma_{ijmn} \quad (2.7)$$

Fig. 2.6 shows a plot of the pole locations of the modes for the structure in Fig. 2.2 on the complex σ - $j\omega$ plane. In Fig. 2.6, (m,n) represent the mode number. As expected, the attenuation of each mode increases as the resonant frequency of that mode moves farther

to the left on the complex $(\sigma, j\omega)$ plane. The distribution of the poles can be used to determine the minimum set of modes that are required to obtain the response over the frequency band of interest.

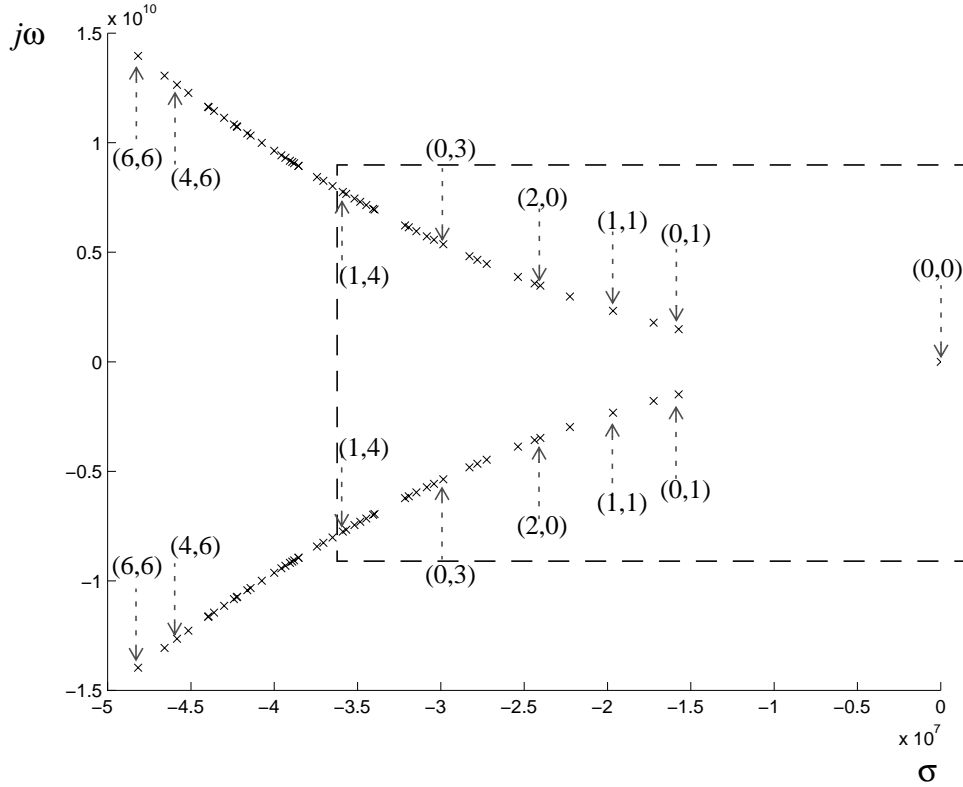


Fig. 2.6 Pole locations of the structure in Fig. 2.2: $s=\sigma+j\omega$

To determine the minimum set of modes, two separate test cases will be considered namely, the trans-impedance between ports 8, 3 and the self-impedance at port 8 in Fig. 2.2. For the trans-impedance computation, the maximum frequency f_{max} over which the response is desired is first used to determine the modes that need to be considered. Suppose that the structure in Fig. 2.2 is analyzed up to 1 GHz, that is, $\omega_{max}=2\pi f_{max}=6.28 \times 10^9$ rad/sec. The block in Fig. 2.6 indicates the dominant modes that need to be considered.

Since $f_{max} \geq \sqrt{(m_k/a)^2 + (n_k/b)^2} / 2\sqrt{\epsilon\mu}$ where (m_k, n_k) 's are the modes with the resonant frequencies within f_{max} , the highest mode numbers for m_k and n_k are the integers which satisfy the following conditions:

$$M_m \leq 2af_{max}\sqrt{\epsilon\mu} < M_m + 1 \quad (2.8)$$

and

$$M_n \leq 2bf_{max}\sqrt{\epsilon\mu} < M_n + 1 \quad (2.9)$$

Then (m_k, n_k) 's are found using the relation

$$0 \leq m_k \leq a\sqrt{4\epsilon\mu f_{max}^2 - (n_k/b)^2} \quad n_k=0, 1, \dots, M_n \quad (2.10)$$

This has been discussed in [24] for the mode numbers required to obtain an accurate response. Though the modes from (2.10) give the response near the resonant frequencies of the structure, the computation at lower frequencies as well as high frequencies can lead to large error while computing the input impedance, as has been discussed in [25]. Using (2.8), (2.9), (2.10), the number of modes required to compute the impedance for the structure in Fig. 2.2 was found to be $M_m=4$ and $M_n=3$. The trans-impedance between port 3 and port 8 computed with 20 modes based on the above criterion is compared to the one computed with 441 modes in Fig. 2.7, showing the accuracy of the minimized model. In reality, only 5 modes out of 20 modes indicated in Fig. 2.7 are sufficient to obtain the same response. This results in a further reduction in the model size, which will be discussed later in this section.

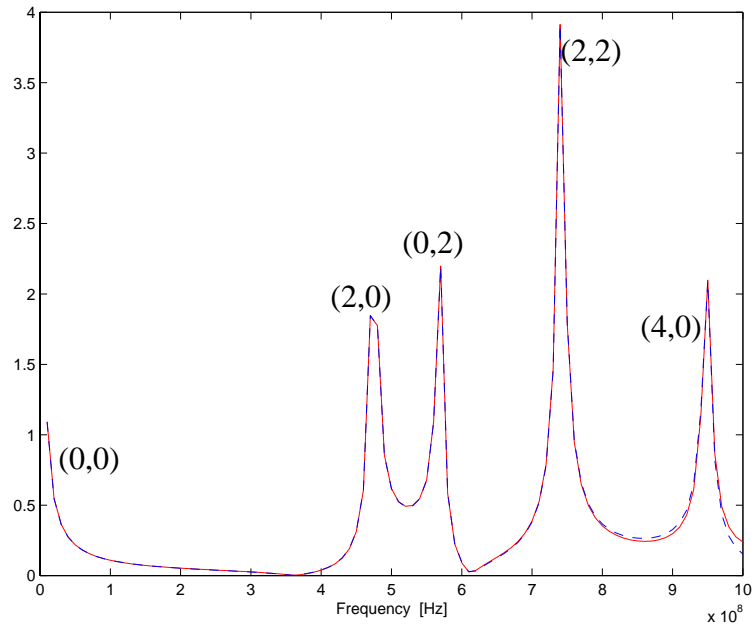


Fig. 2.7 Trans-impedance between ports 3 and 8: Computation with $m=0$ to 20 and $n=0$ to 20 (solid line) and with $m=0$ to 4 and $n=0$ to 3 (dashed line)

In contrast, the computation of the self-impedance, Z_{ii} , requires the inclusion of modes above f_{max} to ensure nulls at the appropriate frequencies in the response. This can be attributed to the evanescent wave modes that impact the self impedance at a port but decays by the time they reach the remote ports. The input impedance at port 8 was computed and compared in Fig. 2.8 using the same number of modes used in Fig. 2.7. As can be seen in Fig. 2.8, though the poles match exactly for both the 441 modes and 20 modes test cases, the nulls are shifted resulting in a deviation in the response. This can cause errors when the noise voltages are computed using the reduced order model. The error occurs mostly in the imaginary part rather than in the real part as shown in Fig. 2.9.

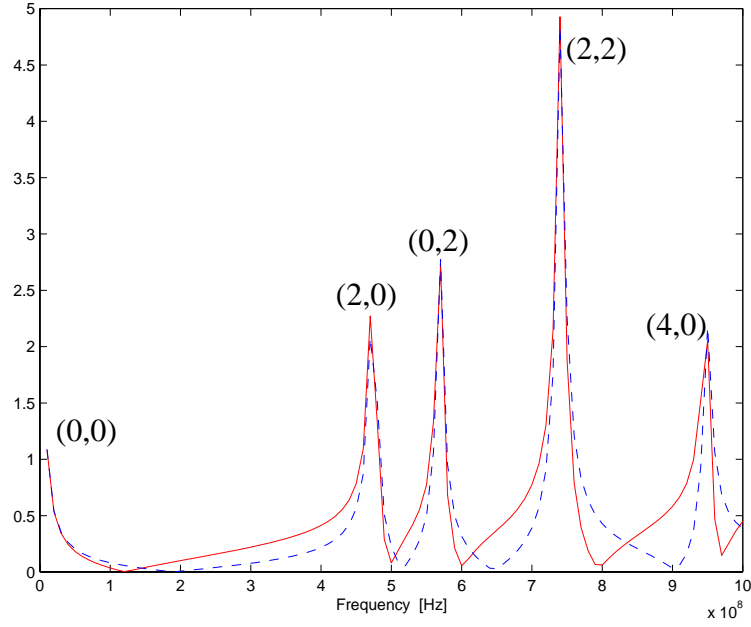


Fig. 2.8 Input impedance at port 8: Computation with $m=0$ to 20 and $n=0$ to 20 (solid line) and with $m=0$ to 4 and $n=0$ to 3 (dashed line)

This can be seen from (2.7) which can be rearranged in terms of the real and imaginary parts as:

$$Z_{ij}(\omega) = \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \left[\frac{\sqrt{\frac{2\omega_{mn}}{\mu\sigma d^2}}}{\frac{2\omega_{mn}}{\mu\sigma d^2} + \omega^2 \left(\left(\frac{\omega_{mn}}{\omega} \right)^2 - 1 \right)^2} + j \frac{\omega \left(\left(\frac{\omega_{mn}}{\omega} \right)^2 - 1 \right)}{\frac{2\omega_{mn}}{\mu\sigma d^2} + \omega^2 \left(\left(\frac{\omega_{mn}}{\omega} \right)^2 - 1 \right)^2} \right] \Gamma_{ijmn} \quad (2.11)$$

where

$$\Gamma_{ijmn} = \frac{d}{ab\epsilon} \epsilon_n^2 \epsilon_m^2 \cos \frac{m\pi x_i}{a} \operatorname{sinc} \frac{m\pi t_{xi}}{2a} \cos \frac{n\pi y_i}{b} \operatorname{sinc} \frac{n\pi t_{yi}}{2b} \cos \frac{m\pi x_j}{a} \operatorname{sinc} \frac{m\pi t_{xj}}{2a} \cos \frac{n\pi y_j}{b} \operatorname{sinc} \frac{n\pi t_{yj}}{2b}$$

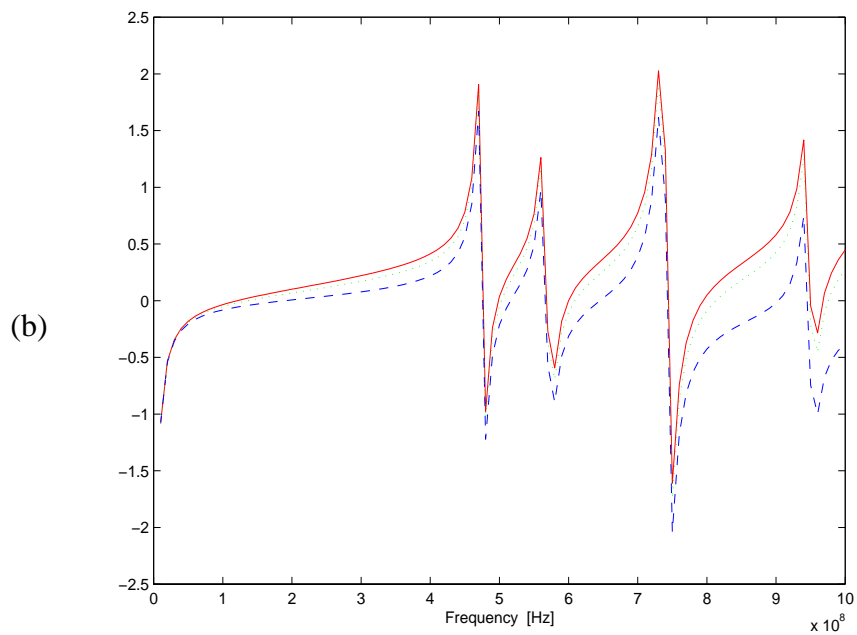
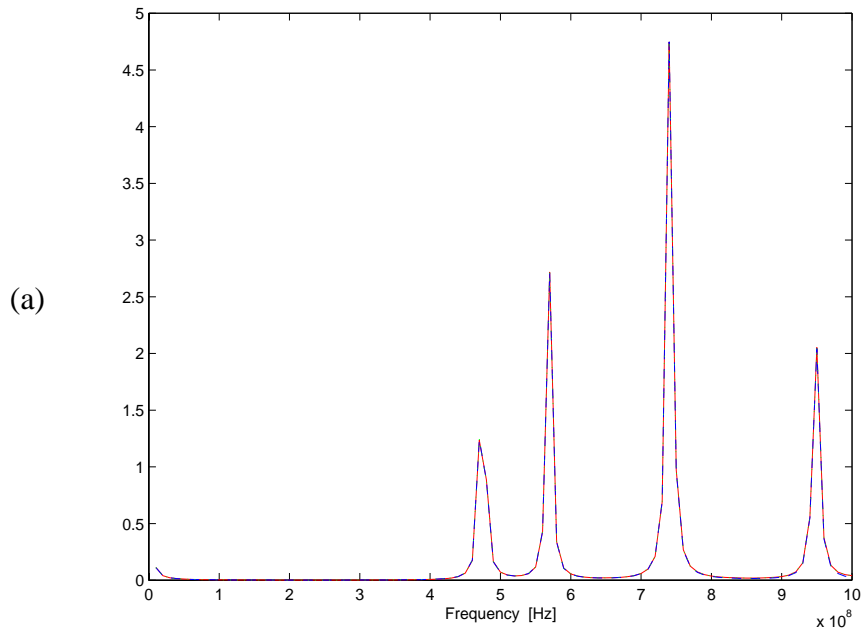


Fig. 2.9 Input impedance at port 8, (a) real part and (b) imaginary part: Computation with $m=0$ to 20 and $n=0$ to 20 (solid line), with $m=0$ to 4 and $n=0$ to 3 (dashed line) and with $m=0$ to 10 and $n=0$ to 10 (dotted line)

Consider the modal response of the input impedance for ‘ mn ’ mode.

$$Z_{ii, mn}(\omega) = \left[\frac{\sqrt{\frac{2\omega_{mn}}{\mu\sigma d^2}}}{\frac{2\omega_{mn}}{\mu\sigma d^2} + \omega^2 \left(\left(\frac{\omega_{mn}}{\omega} \right)^2 - 1 \right)^2} + j \frac{\omega \left(\left(\frac{\omega_{mn}}{\omega} \right)^2 - 1 \right)}{\frac{2\omega_{mn}}{\mu\sigma d^2} + \omega^2 \left(\left(\frac{\omega_{mn}}{\omega} \right)^2 - 1 \right)^2} \right] \Gamma_{iimn} \quad (2.12)$$

where

$$\Gamma_{iimn} = \frac{d}{ab\epsilon} \epsilon_n^2 \epsilon_m^2 \left(\cos \frac{m\pi x_i}{a} \sin c \frac{m\pi t_{xi}}{2a} \cos \frac{n\pi y_i}{b} \sin c \frac{n\pi t_{yi}}{2b} \right)^2$$

(2.12) reveals how higher order modes affect the response at lower frequencies. Since $\Gamma_{iimn} \geq 0$, the reactance in the imaginary part changes from inductive to capacitive nature at ω_{mn} as shown in Fig. 2.10 while the resistance of the real part is always positive. To obtain the response at the minima in Fig. 2.8, the effect of the resonant modes for $\omega > \omega_{max}$ on the response for $\omega < \omega_{max}$ needs to be understood. As shown in Fig. 2.10 and from (2.12), the effect of the higher order modes on the real part of Z_{ii} is minimal since the variable ‘ ω ’ shows up in the denominator. However, the reactance term in (2.12) contains the frequency factor in the numerator and therefore the response is significantly affected by the higher order modes. Since the maximum error in the imaginary part of Z_{ii} (reactance of the circuit) occurs at f_{max} with less error at lower frequencies, the error at f_{max} has been used as a criterion to determine the modes required to implement the resonator circuits. The required modes are determined such that the error of the reactance of Z_{ii} at f_{max} is minimized when higher order modes are added to the modes in (2.10). In Fig. 2.9(b), the maximum error of the response at 1 GHz (f_{max}) was reduced by adding the modes up to

$m, n=10$. The resulting error was 20% of the original error when using the modes (m_k, n_k) 's in (2.10).

The mode numbers can be further reduced according to port locations by investigating the residue terms Γ_{iimm} 's in (2.12) which contain information on the port locations [24]. Γ_{iimm} vanishes at $x \cong (a/2m)k$ or $y \cong (b/2n)k$ where k is an odd number, 1,3,5.. since $\cos(k\pi/2) = 0$. Therefore, the resonator circuits corresponding to those modes can be suppressed whenever $m \cong (a/2x)k$ or $n \cong (b/2y)k$ where k is an odd number. For example, at port 8, all odd modes of m and n are removed since the port is located at the center of the board and so the cosine factors and hence Γ_{iimm} 's vanish for those modes.

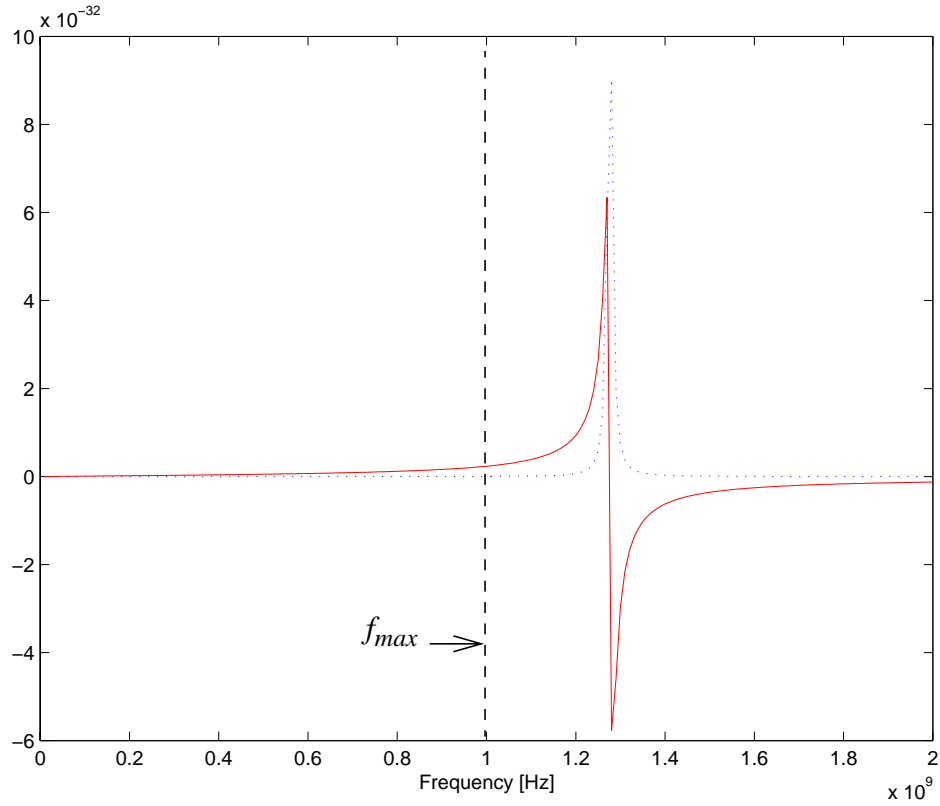


Fig. 2.10 Modal input impedance $Z_{ii,mm}$ computed at port 8 with $m=4$ and $n=3$
Real part (dotted line) and imaginary part (solid line)

By separating port-specific terms and physically constant terms, Γ_{iimm} is written as $\Gamma_{iimm} = (d/ab\epsilon)N_{mni}^2$. Table 2.1 shows N_{mni} 's for port 8 for $m=0$ to 4 and $n=0$ to 3. Only 6 modes (0,0), (0,2), (2,0), (2,2), (4,0), and (4,2) have significant values contributing to the response. Other modes within f_{max} do not affect the results as shown in Figs 2.7, 2.8, 2.9. The largest suppression of modes occurs for the ports located at the center of the board and the minimum suppression occurs for the ports located close to the periphery. For example, the maximum modes are required when input impedance needs to be computed for ports located near the periphery, as shown in Fig. 2.11 for port 5.

Table 2.1 N_{mn8}

m \ n	0	1	2	3
0	1	0	-1.4142	0
1	0	0	0	0
2	-1.4142	0	2.0	0
3	0	0	0	0
4	1.4142	0	-2.0	0

For a structure with a large number of ports, some ports can be described with a few modes and others with more modes depending on the port locations. The response for the planes should therefore include all the modes defined by the port locations for both the self-impedance and trans-impedance computation. Therefore, the number of modes required is determined largely by the input impedance for a port close to the periphery rather than ports removed from the periphery.

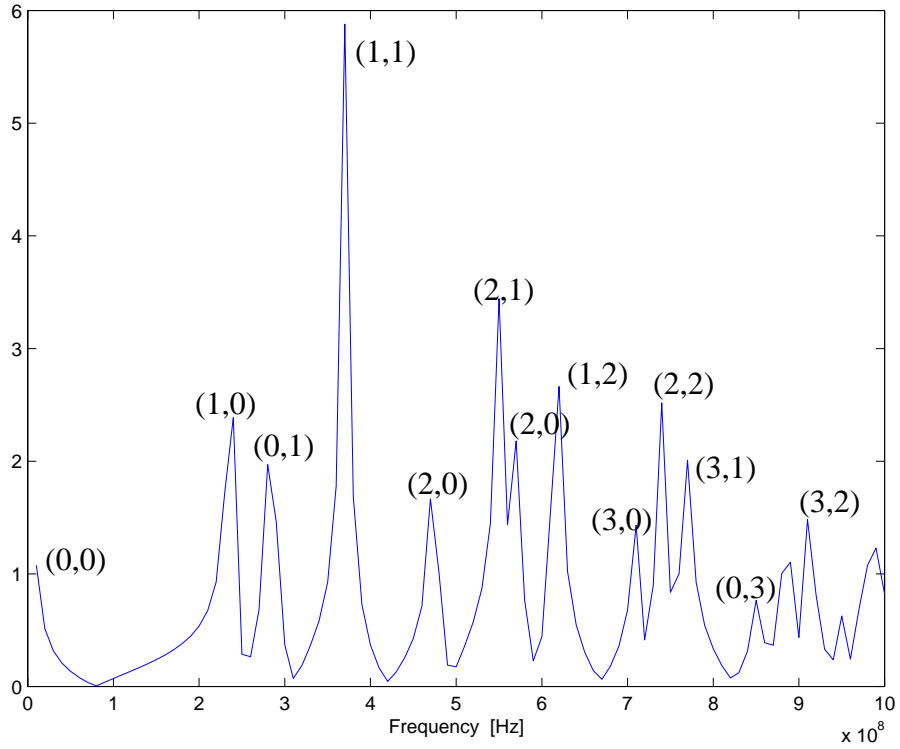


Fig. 2.11 Magnitude of the input impedance at port 5.

2.3 Equivalent Circuit using Wave Resonator Models

Equivalent circuits are implemented using the method discussed in [18] and [23] where the passive network of lumped elements is synthesized directly from (2.1). By dividing the numerator and denominator of (2.7) by $j\omega$ and linearizing as in (2.13), the impedance in (2.7) can be rewritten as [23]:

$$Z_{ij}(\omega) = \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{N_{mni} N_{mnj}}{1/j\omega L_{mn} + j\omega C_{mn} + G_{mn}} \quad (2.13)$$

where $L_{mn} = d/(\omega_{mn} ab\epsilon)$,

$$C_{mn} = ab\epsilon/d,$$

$$G_{mn} = (ab\epsilon/d)\omega_{mn}(\tan\delta + (\sqrt{2/\omega_{mn}\mu\sigma})/d),$$

and $N_{mni} = \epsilon_n \epsilon_m \cos \frac{m\pi x_i}{a} \sin c \frac{m\pi t_{xi}}{2a} \cos \frac{n\pi y_i}{b} \sin c \frac{n\pi t_{yi}}{2b}$.

G_{mn} can be approximated as $G_{mn} = (ab\epsilon/d^2)\sqrt{2\omega_{mn}/\mu\sigma}$ for low dielectric loss ($\tan\delta \ll r/d$).

Each mode of (2.13) represents a parallel resonator circuit and the equivalent circuit is implemented using the passive lumped elements and ideal transformers as discussed in [23] with the number of modes determined using the model order reduction method described in the previous section.

Fig. 2.12 shows the equivalent circuit diagram for N ports with up to ‘ pq ’ modes. $E_{mn,i}$ in each block of Fig. 2.12 represents a transformer circuit for port- i which delivers the energy from the parallel resonator corresponding to the ‘ mn ’ mode. The parallel resonator circuit of each mode consists of the circuit components L_{mn} , G_{mn} and C_{mn} in (2.13). Since each mode resonator circuit contains mode-dependent component values around the mode resonance frequency, the whole circuit naturally reflects the frequency-dependent behavior, which has been captured using lumped passive elements.

Each resonator requires 3 lumped elements and the number of resonators in the equivalent circuit is the number of required modes independent of the number of ports. The number of transformers increases as the number of ports increases. However, the number of transformers can be reduced significantly depending on the port locations.

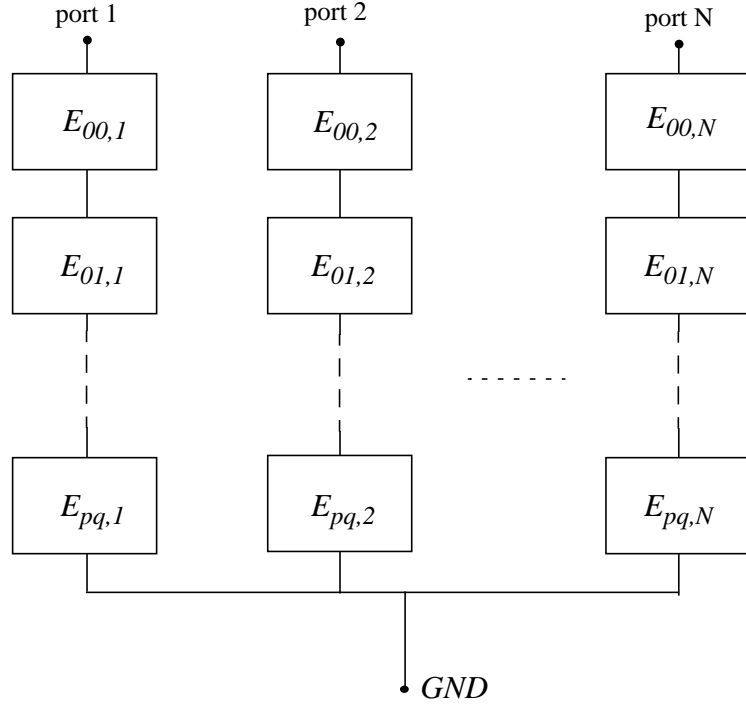


Fig. 2.12 Circuit implementation using resonator models for ‘N’ ports

Each port requires transformers of, at most, the number of resonators or less depending on the port locations. Using this method, the equivalent circuit for the planes is implemented using the minimum number of components. The number of components required is given by

$$\mathfrak{N}_t = 3 \times \mathfrak{N}_{\mathfrak{R}} + \sum_{i=1}^N \mathfrak{N}_{Ti} \quad (2.14)$$

where \mathfrak{N}_t is the total number of components in the circuit, $\mathfrak{N}_{\mathfrak{R}}$ is the number of the mode resonators used, \mathfrak{N}_{Ti} is the number of the transformers which are determined by the modes required at each port ($\mathfrak{N}_{Ti} \leq \mathfrak{N}_{\mathfrak{R}}$) and N is the # of ports.

The complexity of the developed model is a function of the number of ports and the number of components between ports. Using the model order reduction methods described in the previous section, the complexity of the model between ports can be minimized. Since each via represents a port, the number of ports can be minimized by either combining adjacent vias into a single port based on the highest frequency or by eliminating selected quiet vias. This can further reduce the size of the model.

2.4 Summary

In this chapter, a method for modeling plane pairs has been presented which uses the analytical solution to compute the impedance for the ports on a plane pair. Equivalent circuits can be implemented directly from the equation using wave resonator models. A model order reduction method has been developed to generate low order simulation models. Wave mode numbers necessary for computing the accurate response of the model are determined such that the model error in the imaginary part of the self-impedance is minimized at the highest frequency of interest. Since some wave modes vanish based on port locations, the model order is further reduced by eliminating the corresponding resonator circuits. By using the modeling method discussed in this chapter, the responses for the ports located at any location on the plane can be computed accurately and the plane pair can be represented as a low order circuit for efficient simulation.

The next chapter discusses measurements on a test vehicle to verify the accuracy of the modeling method described in this chapter.

CHAPTER 3

Model to Hardware Correlation

In the previous chapter, a modeling method for plane pairs was discussed. This chapter discusses some measurements on a test vehicle and correlation between measurements and simulation results using the modeling method described in Chapter 2.

3.1 Test Vehicle Design and Fabrication

Test boards were designed and fabricated to check the accuracy of the modeling approach in the time domain. Fig. 3.1 shows the layer structure and port locations on the top plane which are used for measurements and verification of the plane modeling method.

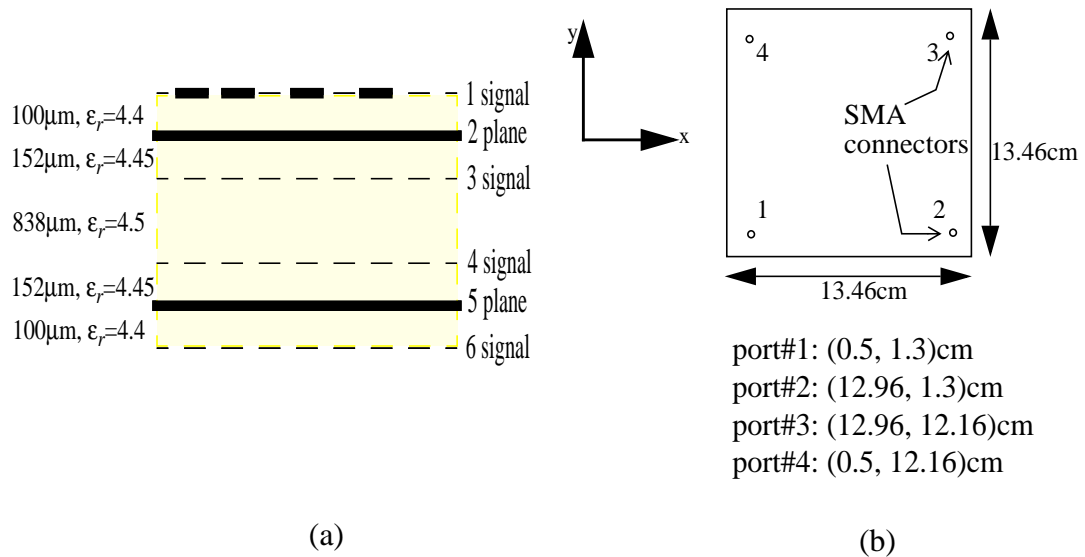


Fig. 3.1 Test Vehicle: (a) layer stack-up and (b) top view

The plane size is 13.46 cm by 13.46 cm and the dielectric constants are 4.4~4.5 at 1 MHz and 4.1~4.2 at 100 MHz. The thicknesses of the planes, P1 and P2, are 35 μ m. P2 (the 5th layer) was used as the ground reference for all the probe points.

3.2 Transient Measurements and Simulation

The transient response of the planes was measured using a digital sampling oscilloscope Tektronix 11801B as shown in Fig. 3.2. The SD-24 sampling head in the measurement setup generated a step pulse with 35ps rise time and 500 mV amplitude. The source impedance of the oscilloscope is 50 Ω . Since the characteristic impedance of the coaxial cables used in Fig. 3.2 is 50 Ω , the incident pulse launched on the plane is 250 mV. The signal lines in Fig. 3.1 are not activated in the measurement.

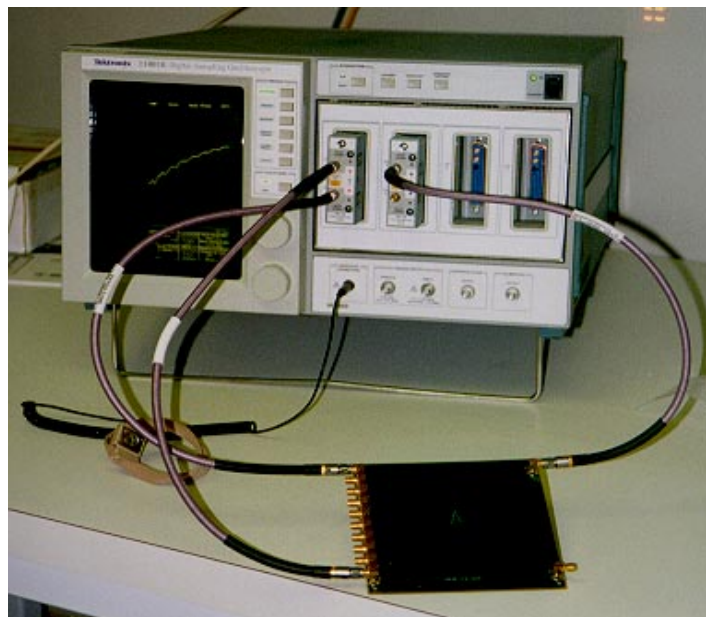


Fig. 3.2 Measurement setup

Pulse transients on the plane P1 were measured with the pulse source. Based on (2.8)-(2.10) and the analysis method described in Sec. 2.2, for a frequency band of 1 GHz, the minimum required modes were 4 with $M_m = 1$ and $M_n = 1$. This translates to the (0,0), (1,0), (0,1) and (1,1) modes. Fig. 3.3 and Fig. 3.4 show the input impedance at port 1 and the trans-impedance between port 1 and port 3, respectively, computed with more than 400 modes, with 9 modes ($m=0$ to 2, $n=0$ to 2) and with 25 modes ($m=0$ to 4, $n=0$ to 4). Since the structure is square, resonances for (m,n) and (n,m) modes occur at the same frequency, i.e., $f_{mn}=f_{nm}$. Due to this, the first peak resulted from the sum of the two modes (0,1) and (1,0). Two test cases were used to simulate the transient response and compared with measurements.

As a first test case, the pulse was injected into port 1 and measured at port 3. Fig. 3.5 shows the equivalent circuit representation of the measurement setup including the plane equivalent circuit. Fig. 3.6 shows the simulated transient response which has been correlated with the measured data. The simulation result shows good agreement with the measurements.

As a second test case, 3 pulses were injected at ports 1, 2 and 4 simultaneously and the transmitted wave was measured at port 3. The number of modes considered were 25 ($m=0$ to 4 and $n=0$ to 4) for the construction of the 4 port equivalent circuit. The simulation result shows good agreement with the measured data as shown in Fig. 3.7. Though the small glitch due to a spurious oscillation in the initial time period of the simulation is negligible in amplitude, it can be removed by including higher order modes for accurately modeling the delay.

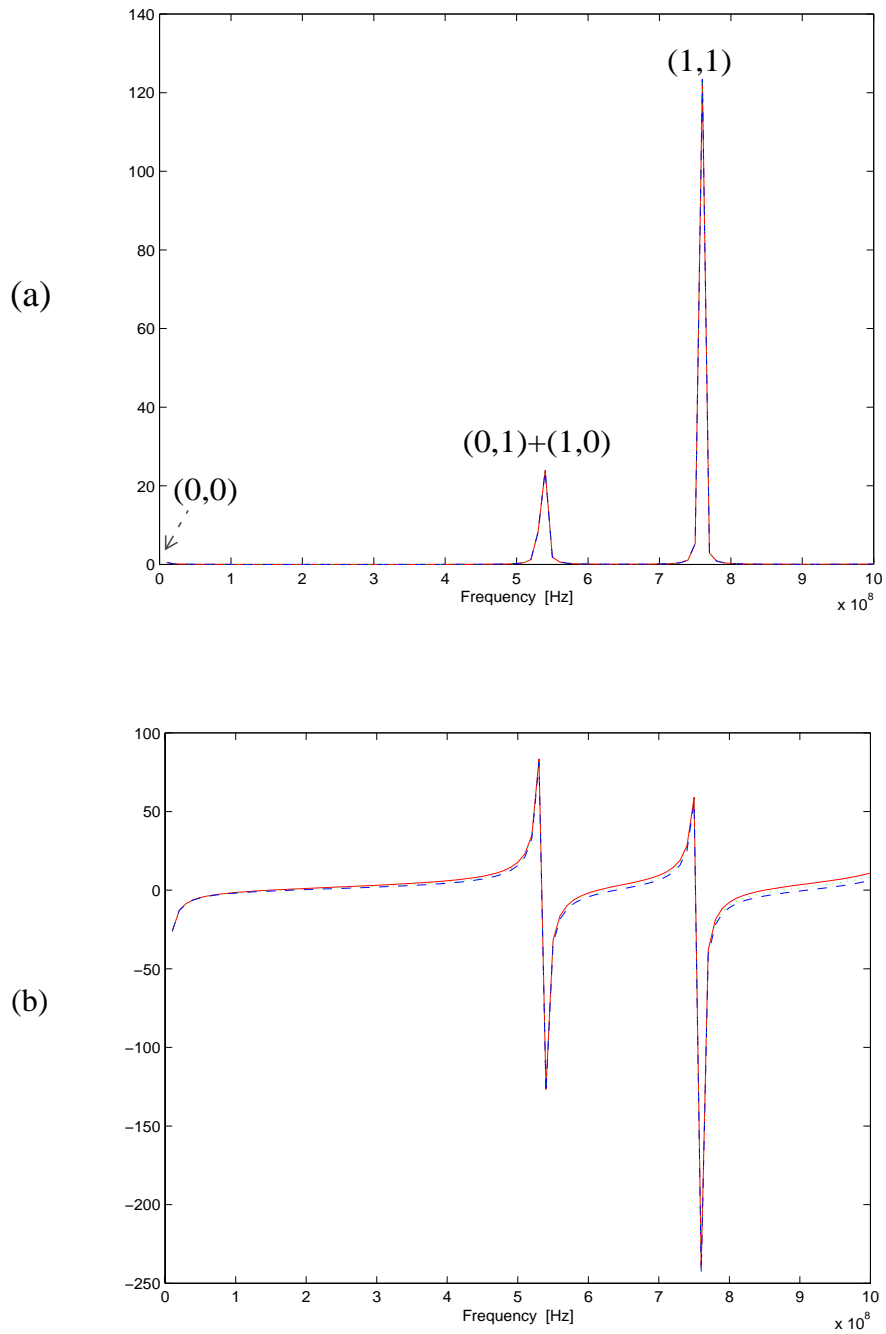


Fig. 3.3 Input impedance at port 1 (a) real and (b) imaginary part 441 modes with $m=0$ to 20 and $n=0$ to 20 (solid), 9 modes with $m=0$ to 2 and $n=0$ to 2 (dashed) and 25 modes of $m=0$ to 4 and $n=0$ to 4 (dotted)

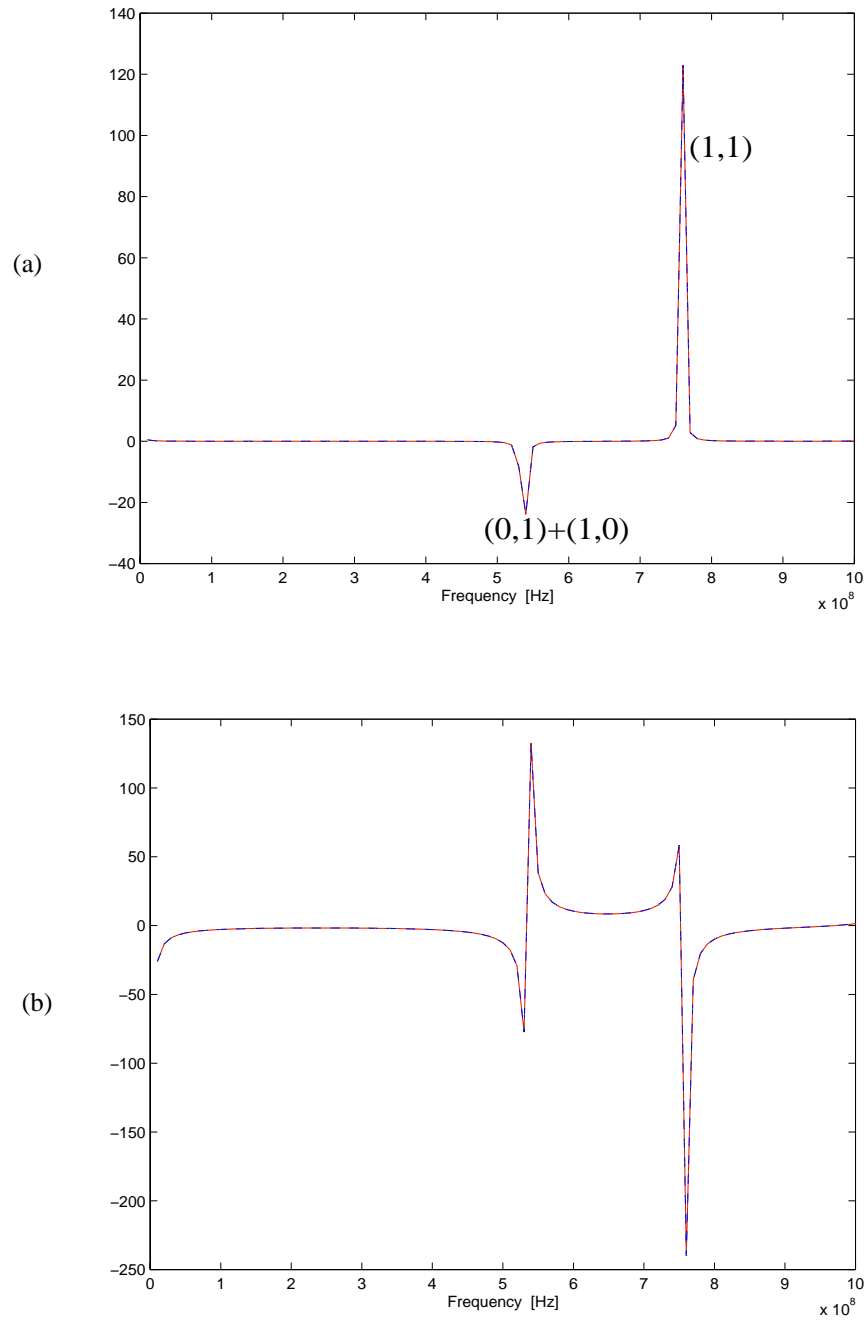
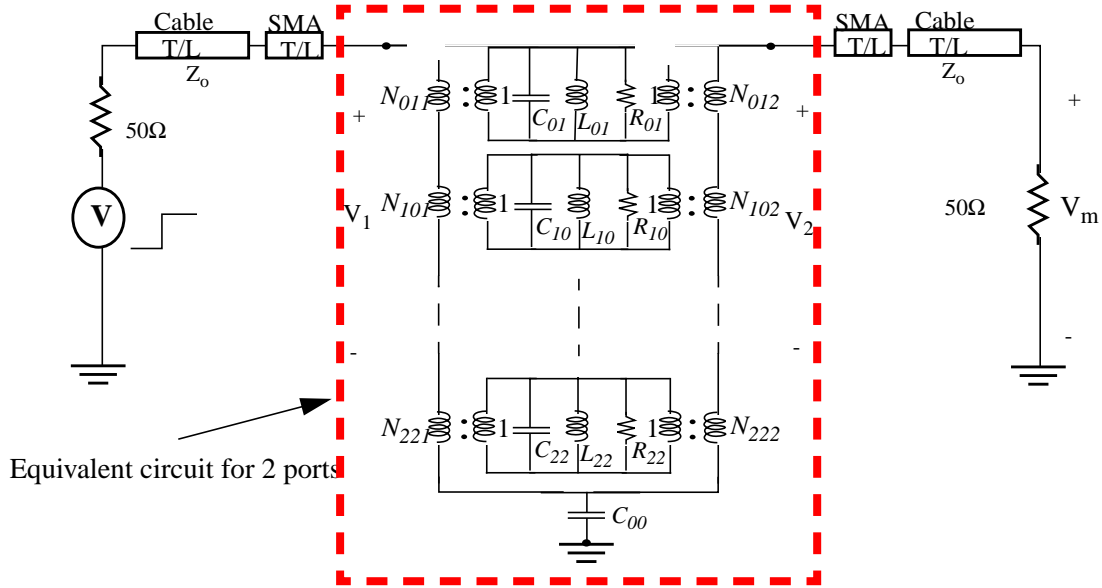


Fig. 3.4 Trans-impedance between ports 1 and 3 (a) real and (b) imaginary parts 441 modes with $m=0$ to 20 and $n=0$ to 20 (solid), 9 modes with $m=0$ to 2 and $n=0$ to 2 (dashed) and 25 modes with $m=0$ to 4 and $n=0$ to 4 (dotted)

Both Figs 3.6 and 3.7 show initial glitches in the response caused by the resonances in the structure followed by the charging of the planes in the steady state. Since the models show good correlation with measurements both in the transient and steady states, these models represent large bandwidth models which are often required for noise computation in high frequency packages.



$C_{01}=6.05711\text{e-}10\text{F}$, $L_{01}=1.45404\text{e-}10\text{H}$, $R_{01}=1.96072\text{e+}02\Omega$, $N_{01I}=1.3574$, $N_{012}=-1.3526$
 $C_{10}=6.05711\text{e-}10\text{F}$, $L_{10}=1.45404\text{e-}10\text{H}$, $R_{10}=1.96072\text{e+}02\Omega$, $N_{10I}=1.4079$, $N_{102}=-1.4079$
 $C_{11}=6.05711\text{e-}10\text{F}$, $L_{11}=7.27020\text{e-}11\text{H}$, $R_{11}=1.64876\text{e+}02\Omega$, $N_{11I}=1.9110$, $N_{112}=1.9042$
 $C_{02}=6.05711\text{e-}10\text{F}$, $L_{02}=3.63510\text{e-}11\text{H}$, $R_{02}=1.38644\text{e+}02\Omega$, $N_{02I}=1.1914$, $N_{022}=1.1730$
 $C_{20}=6.05711\text{e-}10\text{F}$, $L_{20}=3.63510\text{e-}11\text{H}$, $R_{20}=1.38644\text{e+}02\Omega$, $N_{20I}=1.3888$, $N_{202}=1.3888$
 $C_{12}=6.05711\text{e-}10\text{F}$, $L_{12}=2.90808\text{e-}11\text{H}$, $R_{12}=1.31121\text{e+}02\Omega$, $N_{12I}=1.6773$, $N_{122}=-1.6514$
 $C_{21}=6.05711\text{e-}10\text{F}$, $L_{21}=2.90808\text{e-}11\text{H}$, $R_{21}=1.31121\text{e+}02\Omega$, $N_{21I}=1.8852$, $N_{212}=-1.8785$
 $C_{22}=6.05711\text{e-}10\text{F}$, $L_{22}=1.81755\text{e-}11\text{H}$, $R_{22}=1.16585\text{e+}02\Omega$, $N_{22I}=1.6546$, $N_{222}=1.6291$

Fig. 3.5 Equivalent circuit for the measurement setup

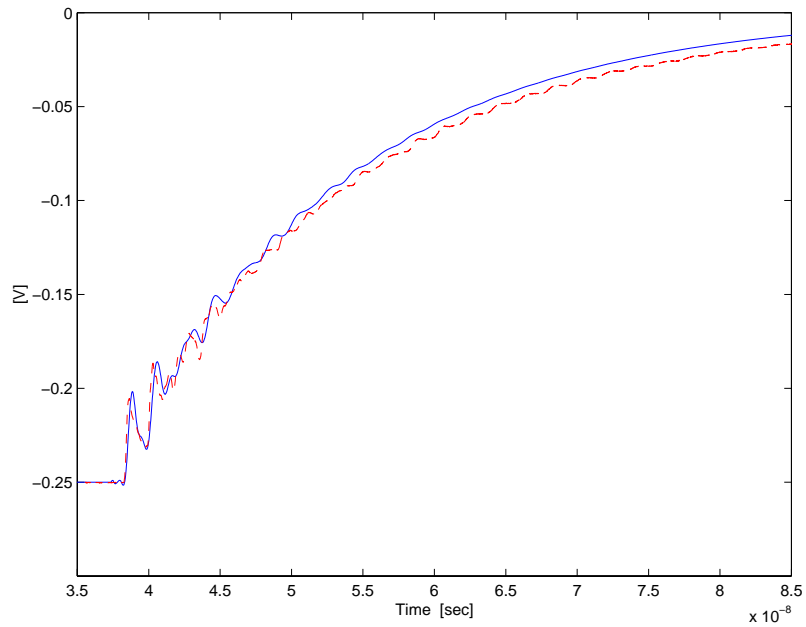


Fig. 3.6 Transient response at port 3 with port 1 excited:
Simulation (solid line) and measured data (dashed line)

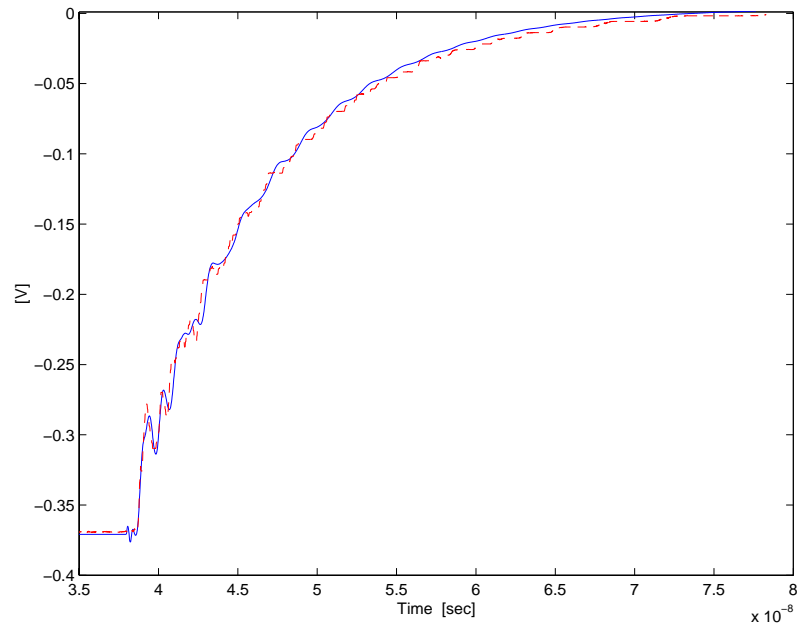


Fig. 3.7 Transient response at port 3 with ports 1, 2 and 4 simultaneously excited:
Simulation (solid line) and measured data (dashed line)

3.3 Summary

In this chapter, time domain measurements on a test vehicle have been discussed. The test structure which consists of a plane pair has been modeled using the method described in Chapter 2 and the simulation results were compared with measurements. The equivalent circuits were constructed using the modes $m=0$ to 2 and $n=0$ to 2. The transient response shows that although the plane behaves basically as a parallel plate capacitor in the steady state with the input pulse charging the structure, large oscillatory glitches occur in the initial time period due to wave reflection from the boundaries. It was shown from the simulation results that the model captured the plane resonances in the initial time period accurately.

In the next chapter, the modeling method described in chapter 2 for rectangular geometries has been extended for irregular geometries.

CHAPTER 4

Modeling of Irregular Planes

Some applications contain irregular power distribution planes. Examples are pagers, cellular phones and certain digital systems, to name a few. These power distribution networks can be analyzed as composites of simpler configurations. Examples of package planes with large cut-outs or L-shaped planes are shown in Fig. 4.1.

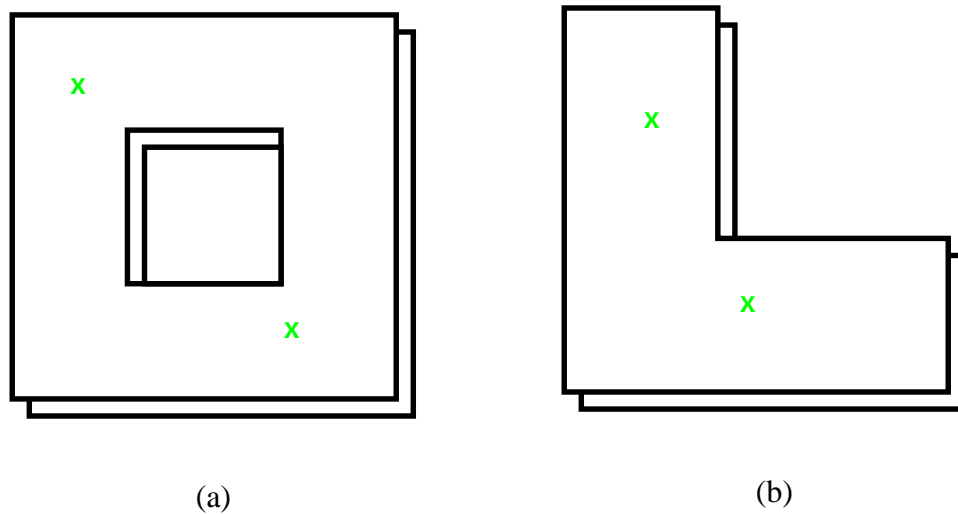


Fig. 4.1 Practical examples of irregular geometries of planes in power distribution network: (a) rectangular geometry with a large cut-out and (b) L-shaped geometry

The analytical solution in (2.1) are no longer valid for these irregular structures. However, an irregular structure such as those in Fig. 4.1 can be decomposed into regular rectangular shapes which can be recombined using the method of segmentation [26],[27]. Using segmentation, an irregular structure can be divided into rectangular regions sharing a common interface, where each region is bounded by either electric or magnetic walls.

Using the solution for a rectangular geometry, each region is first characterized using the analytical solution in (2.1) and recombined by enforcing the continuity of the tangential components of the electric and magnetic fields at the interface. The underlying basis of the segmentation approach is the transformation of the field matching along the interface between two regions into an equivalent network connection problem. Matching of the tangential component of the magnetic field is accomplished by the current continuity condition enforced by Kirchoff's current law. The continuity of the tangential component of electric field is ensured by enforcing equivalence of voltages at the connected ports. Thus the electromagnetic field matching problem is solved as an equivalent network interconnection problem. An alternate way of solving the problem for these structures is by using the desegmentation method. This method is applicable in cases where the addition of one or more simpler shapes to the original irregular shape to be analyzed yields another simple shape. The segment added to the original structure and the augmented structure which are regular are characterized using the solution in (2.1). Then the response of the original irregular structure is solved by enforcing the boundary conditions at the common interface as in the segmentation method. In this chapter, the segmentation method will be used to obtain the response of a structure with a large cut-out, as shown in Fig. 4.1.

4.1 Segmentation Method

To review the segmentation method, consider the structure in Fig. 4.2 where the structure 'G' is the composite of the structures 'A' and 'B'. The responses of 'A' and 'B' are known and the response of 'G' needs to be obtained between ports p and q. The structures 'A' and 'B' are connected together through the connection ports c_i 's and d_i 's.

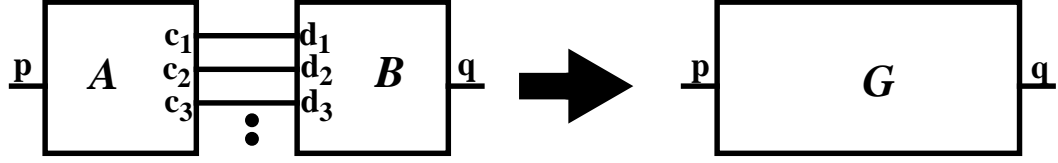


Fig. 4.2 Segmentation method

The boundary conditions enforced for current continuity at the interface are

$$\begin{aligned} V_{ci} &= V_{di} \\ I_{ci} &= -I_{di} \end{aligned} \quad (4.1)$$

and

where V_{ci} , V_{di} are the voltages at the c_i and d_i ports and I_{ci} , I_{di} are the currents flowing into the c_i and d_i ports.

Let the structures A, B and G be represented as

$$\begin{bmatrix} V_p \\ V_c \end{bmatrix} = \begin{bmatrix} Z_{pp\alpha} & Z_{pc} \\ Z_{cp} & Z_{cc\alpha} \end{bmatrix} \begin{bmatrix} I_p \\ I_c \end{bmatrix} = Z_A \begin{bmatrix} I_p \\ I_c \end{bmatrix} \quad (4.2a)$$

and

$$\begin{bmatrix} V_q \\ V_d \end{bmatrix} = \begin{bmatrix} Z_{qq\beta} & Z_{qd} \\ Z_{dq} & Z_{dd\beta} \end{bmatrix} \begin{bmatrix} I_q \\ I_d \end{bmatrix} = Z_B \begin{bmatrix} I_q \\ I_d \end{bmatrix} \quad (4.2b)$$

where $V_c = [V_{c1} \ V_{c2} \ \dots \ V_{cn}]$, $I_c = [I_{c1} \ I_{c2} \ \dots \ I_{cn}]$, $V_d = [V_{d1} \ V_{d2} \ \dots \ V_{dn}]$ and $I_d = [I_{d1} \ I_{d2} \ \dots \ I_{dn}]$ for n connections. Using the boundary conditions in (4.1), the voltage-current relation between ports p and q can be derived as:

$$\begin{bmatrix} V_p \\ V_q \end{bmatrix} = \left(\begin{bmatrix} Z_{pp\alpha} & 0 \\ 0 & Z_{qq\beta} \end{bmatrix} + \begin{bmatrix} Z_{pc} \\ -Z_{qd} \end{bmatrix} (Z_{cc\alpha} + Z_{dd\beta})^{-1} \begin{bmatrix} -Z_{cp} & Z_{dq} \end{bmatrix} \right) \begin{bmatrix} I_p \\ I_q \end{bmatrix} = Z_G \begin{bmatrix} I_p \\ I_q \end{bmatrix} \quad (4.3)$$

If the impedance matrices Z_A and Z_B in (4.2) are known, the impedance for the structure G , Z_G , can be obtained using (4.3).

As an example, consider the rectangular plane G in Fig. 4.3 measuring $6\text{cm} \times 2\text{cm}$ with a dielectric thickness of $1142\mu\text{m}$ and relative permittivity of 4.5. This structure can be decomposed into two planes of dimension $3\text{cm} \times 2\text{cm}$ and combined using connection ports, as illustrated in Fig. 4.3. In Fig. 4.3, ports 1 and 2 are located at $(1.0, 1.5)$ and $(5.0, 0.5)$, respectively. The planes A and B were individually analyzed using (2.1) to compute the impedance. The impedance matrix which included the trans-impedance matrix

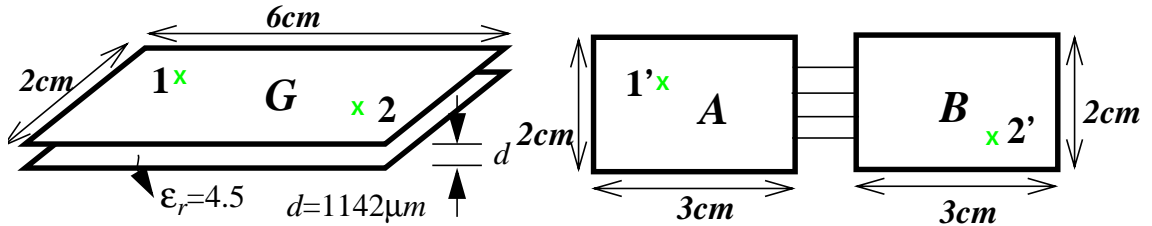


Fig. 4.3 Plane G decomposed into planes A and B

between ports 1, 2 and the connection ports was computed using $m=0$ to 20 and $n=0$ to 20 wave modes for each plane. Using (4.3), the planes A and B were combined and the response between ports 1 and 2 was computed. This was compared with the solution obtained by analyzing plane G directly using (2.1) and $m=0$ to 20 and $n=0$ to 20 wave

modes. The results are shown in Fig. 4.4 for varying number of connection ports. In Fig. 4.4, the result converges for 11 connection ports, indicating appropriate matching at the boundary between planes *A* and *B*. The disagreement in magnitude at the resonant frequency between the computation with $k=11$ and the analytical solution is due to the finite number of connection ports used. This leads to a slight shift of the resonant frequency since the responses were computed at discrete frequencies with a finite frequency step of 10MHz.

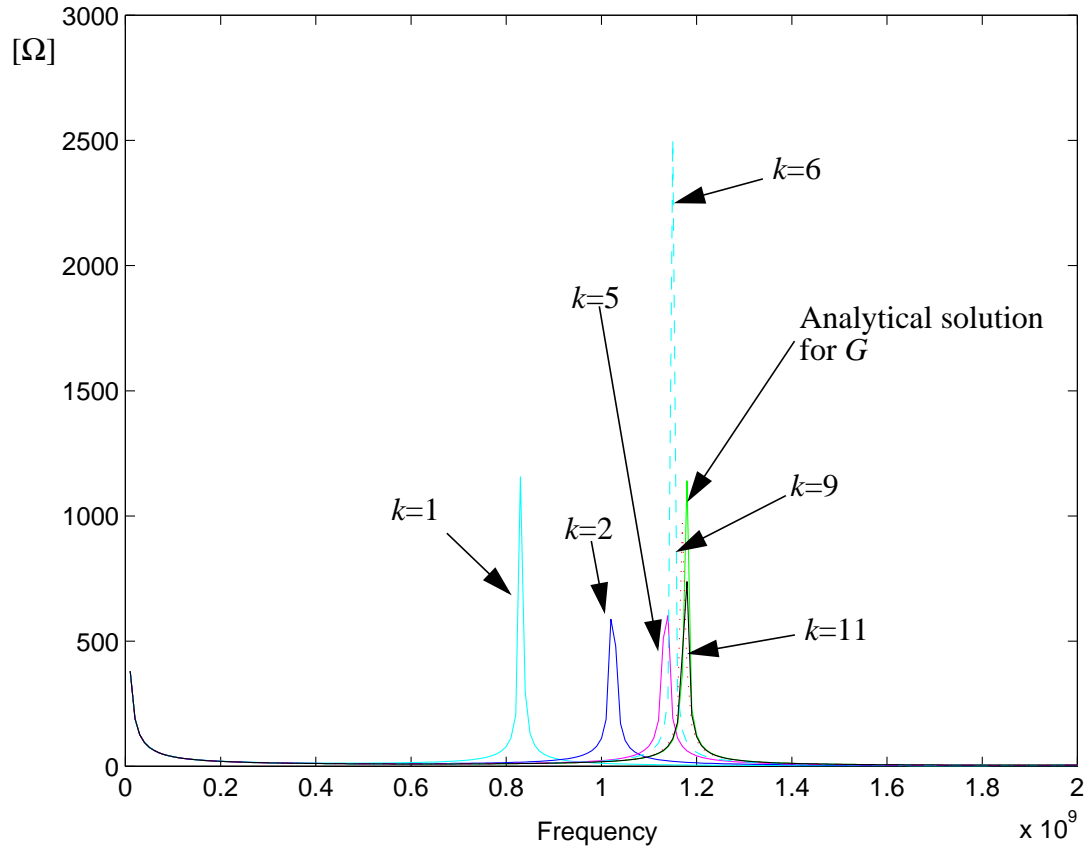


Fig. 4.4a Z_{12} magnitude computed using segmentation method with different numbers of connection ports

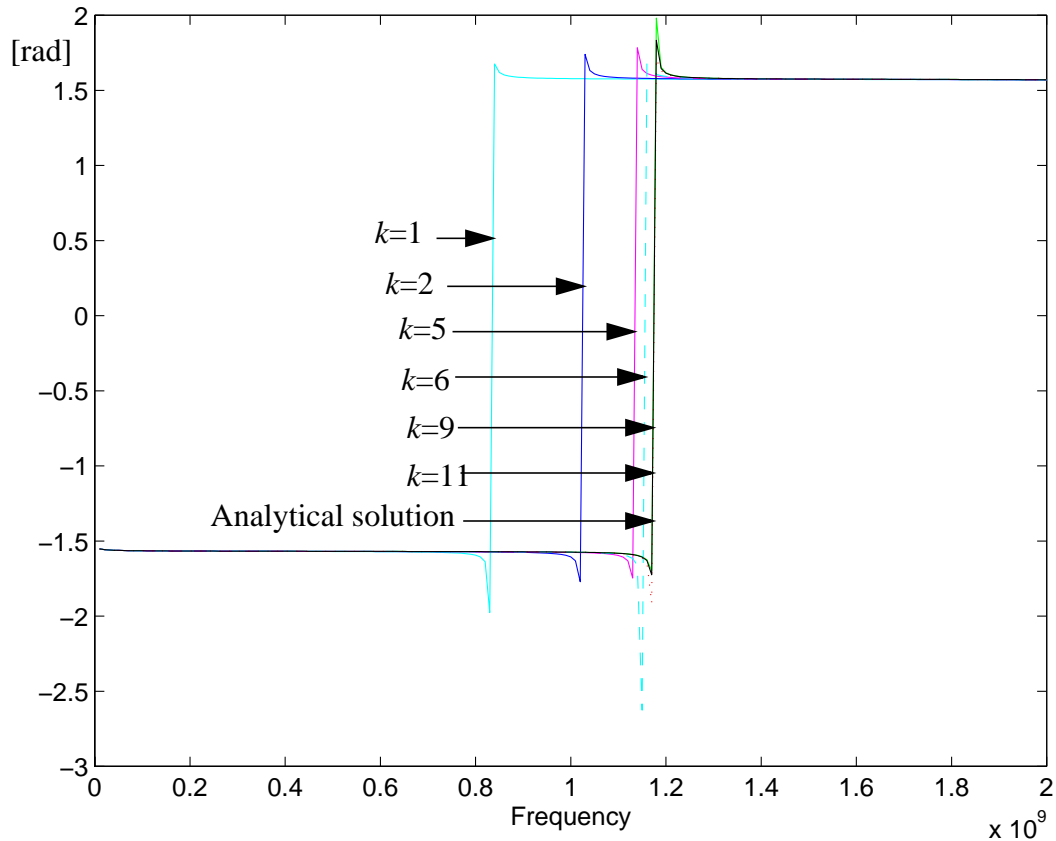


Fig. 4.4b Z_{12} phase computed using segmentation method with different number of connection ports

4.2 L-shaped Planes

In the previous section, the accuracy of the segmentation method for a certain number of connection ports has been demonstrated using a rectangular plane structure. In this section, an L-shaped structure with dimensions $12.26\text{cm} \times 9.60\text{cm}$, as shown in Fig. 4.5a, has been analyzed. The dielectric thickness is $25.4\mu\text{m}$ with a relative permittivity of 4.0 and the metal conductivity is $5.8 \times 10^5 \text{mho/cm}$. The external ports are located at port 1 (2.26cm , 6.81cm) and port 2 (3.38cm , 5.92cm) on P2. This structure has previously been analyzed

using the transmission line matrix method [28]. In this section, the structure has been analyzed using the segmentation method. The L-shaped structure is first decomposed into two rectangular structures as shown in Fig. 4.5b.

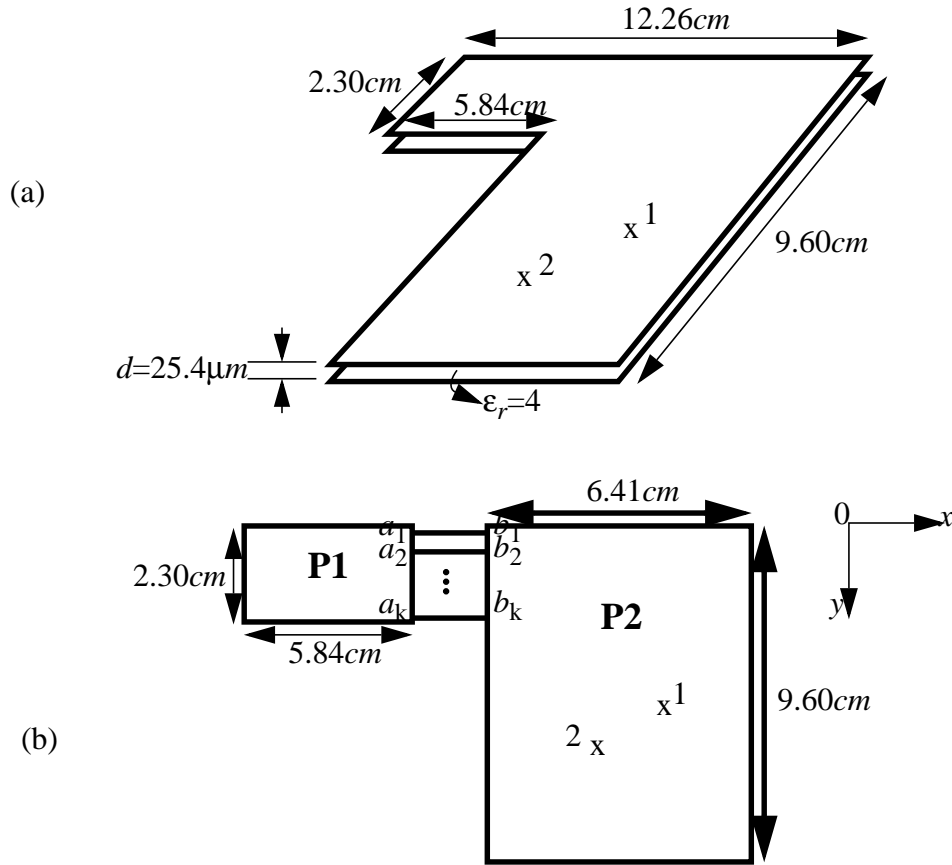


Fig. 4.5 Decomposition of the L-shape structure into rectangular structures for solving the port response using the segmentation method

The frequency response at the external ports 1 and 2 and the connection ports a_i 's and b_i 's were computed for P1 and P2 separately using the analytical solution with the wave modes $m=0$ to 60 and $n=0$ to 60. The results were then combined at the connection ports using the segmentation method. The self-impedance at port 1 computed with different number of connection ports is compared with the computation using the transmission line matrix method [28] in Fig. 4.6. In [28], the structure was partitioned into unit cells of

dimension $0.508\text{cm} \times 0.508\text{cm}$ and the total response was computed using the transmission line matrix method. In Fig. 4.6, the segmentation method agrees with the transmission line matrix method for 12 connection ports over a bandwidth of 2 GHz. This translates to a spacing of $\lambda/40$ between the connection ports at 2GHz which indicates the fine granularity that is required.

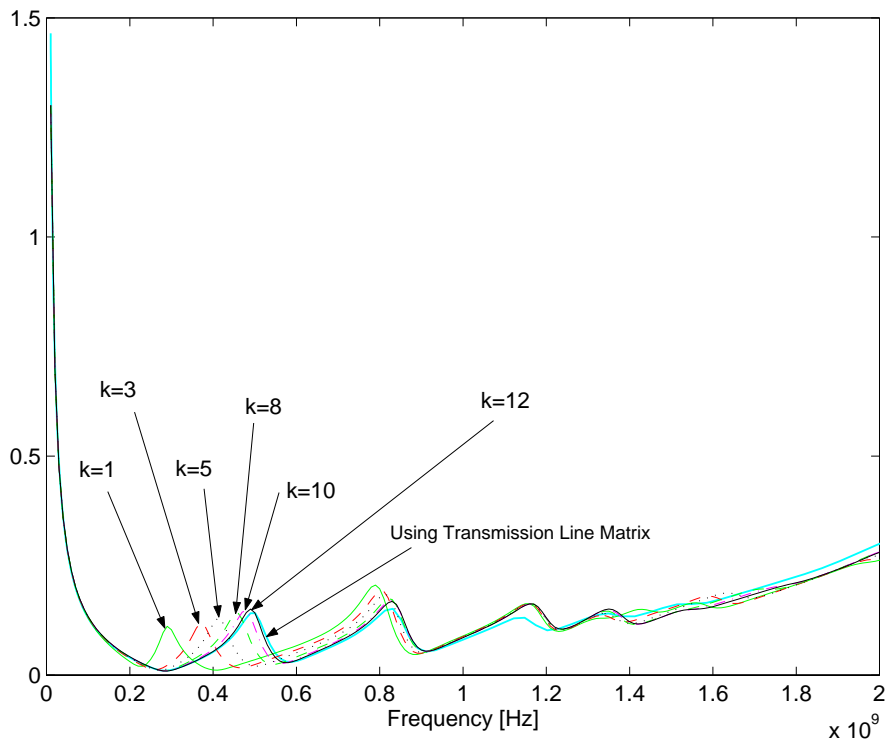


Fig. 4.6 Self-impedance of the L-shape structure at port 1 computed using the segmentation method with different number of connection ports and using the transmission matrix method.

4.3 Planes with Cut-outs

In the previous sections, the accuracy of the segmentation method has been demonstrated for a rectangular structure and L-shaped structure. In this section, an irregular

plane structure with dimension $3.2\text{cm} \times 3.2\text{cm}$ and a cut-out of $1\text{cm} \times 1\text{cm}$ as shown in Fig. 4.7a has been analyzed. The dielectric thickness is $300\mu\text{m}$ with a relative permittivity of 9.5 and the metal resistivity is $10.5\mu\Omega\text{-cm}$. The structure is decomposed first into two L-shaped planes. Each L-shaped plane is then divided into rectangular planes, as shown in Fig. 4.7c. The rectangular planes can be analyzed using the analytical solutions described earlier. The responses of the rectangular planes in Fig. 4.7c were computed using (2.1) with wave mode numbers $m=0$ to 10 and $n=0$ to 10.

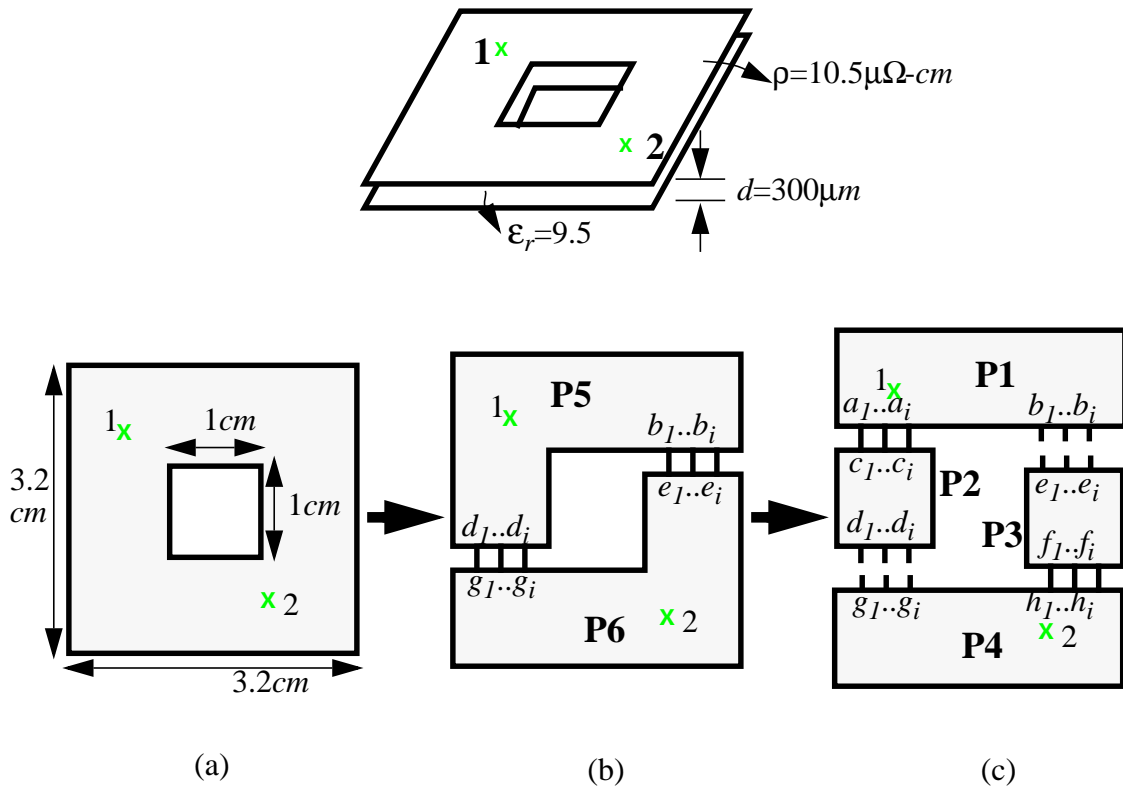


Fig. 4.7 Decomposition of the structure with a cut-out into regular structures for solving the port response using segmentation method

The response at the ports in Fig. 4.7a, which are located at port 1 (0.5cm , 2.7cm) and port 2 (2.7cm , 0.5cm), has been solved using the two-step segmentation process: first for each L-shaped plane and then for the whole structure by combining two L-shaped planes.

The responses on planes P1 and P2 were first computed at the connection ports a_i 's, c_i 's and the external ports 1, b_i 's, d_i 's as shown in Fig. 4.5c using the analytical solution as

$$Z_{P1} = \begin{bmatrix} Z_{11} & Z_{1b} & Z_{1a} \\ Z_{b1} & Z_{bb} & Z_{ba} \\ Z_{a1} & Z_{ab} & Z_{aa} \end{bmatrix} \quad Z_{P2} = \begin{bmatrix} Z_{dd} & Z_{dc} \\ Z_{cd} & Z_{dd} \end{bmatrix} \quad (4.4)$$

Using the segmentation method, the response on P5 in Fig. 4.7b was computed at port 1 and the connection ports b_i 's and d_i 's by combining the two matrices in (4.4) as

$$Z_{P5} = \begin{bmatrix} Z_{11} & Z_{1b} & Z_{1d} \\ Z_{b1} & Z_{bb} & Z_{bd} \\ Z_{d1} & Z_{db} & Z_{dd} \end{bmatrix} \quad (4.5)$$

Similarly, the response on P6 in Fig. 4.7b was computed at port 2 and the connection ports e_i 's and g_i 's by combining the impedance matrices of planes P3 and P4 as

$$Z_{P6} = \begin{bmatrix} Z_{22} & Z_{2e} & Z_{2g} \\ Z_{e2} & Z_{ee} & Z_{eg} \\ Z_{g2} & Z_{ge} & Z_{gg} \end{bmatrix} \quad (4.6)$$

Finally, the response of the entire structure at ports 1 and 2 in Fig. 4.7a was computed using the segmentation method by combining the results in (4.5) and (4.6) as

$$Z_T = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \quad (4.7)$$

Figs 4.8a and 4.8b show the computation results with different number of connection ports. It can be seen that the result converges with 28~32 connection ports. The rectangular structure of dimension $3.2\text{cm} \times 3.2\text{cm}$ with the same port locations but without a cut-out was also computed using the analytical solution to analyze the effect of the cut-out. The imaginary part of the trans-impedance for the rectangular structure is shown in Fig. 4.9. While the first resonance of the rectangular structure without the cut-out occurred at $\sim 1.5\text{GHz}$, that of the structure with the cut-out was shifted to a lower frequency of $\sim 650\text{MHz}$. This can be attributed to the wave taking a longer path to communicate between the ports due to the presence of the cut-out.

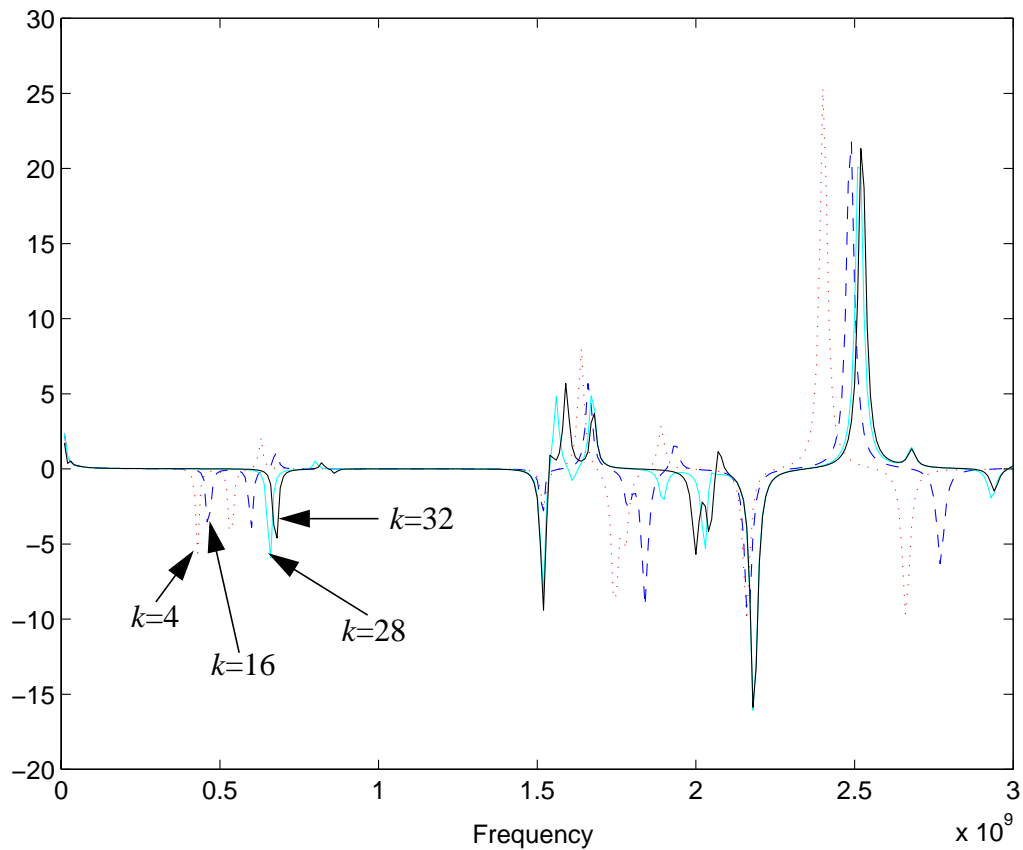


Fig. 4.8a $\text{Real}(Z_{12})$ computed for the structure in Fig. 4.5a using segmentation with different number of connection ports ($=k$)

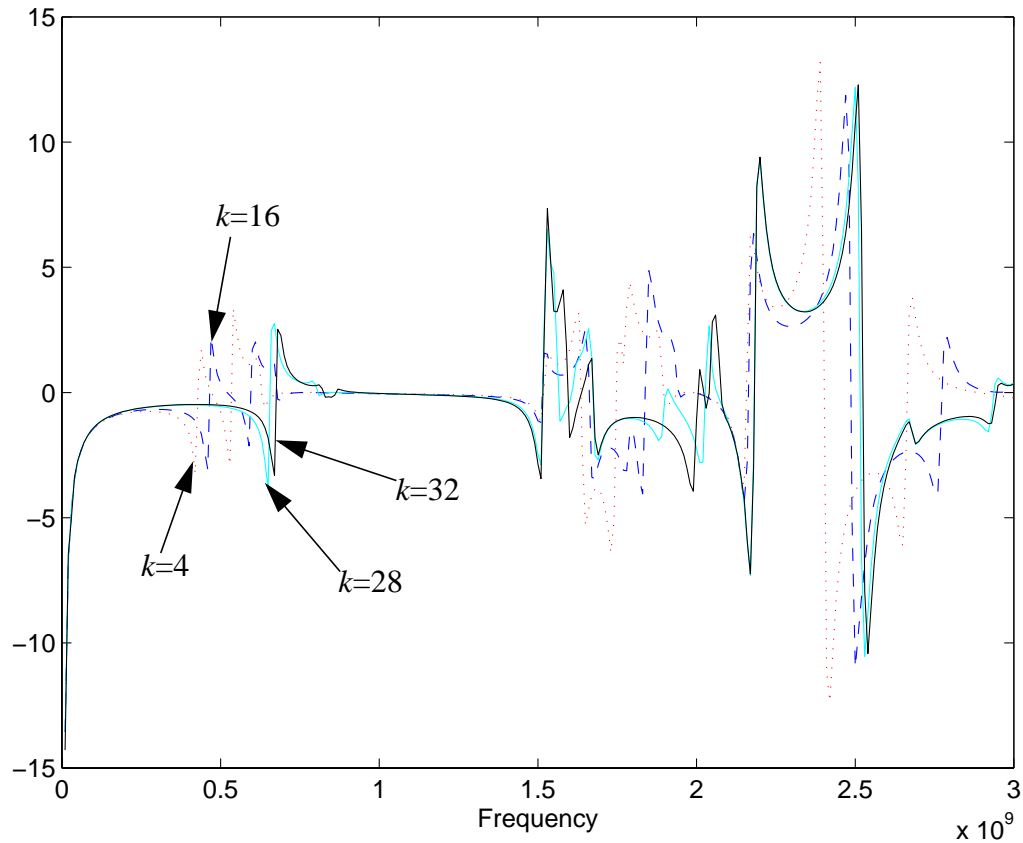


Fig. 4.8b $\text{Imag}(Z_{12})$ computed for the structure in Fig. 4.5a using segmentation with different number of connection ports ($=k$)

4.4 Summary

In this chapter, a method for analyzing irregular plane structures has been discussed. Irregular structures are first decomposed into regular structures and re-combined for computing the response of the original irregular structure using the method of segmentation.

Using this method, an L-shaped plane structure and a rectangular structure with a large cut-out have been analyzed. The computation result of the L-shaped plane structure using the segmentation method has been compared with the response computed using the trans-

mission line matrix method. Good correlation with 12 connection ports was obtained over a bandwidth of 2GHz.

The rectangular structure with a cut-out was analyzed using a two-step segmentation process by decomposing the structure first into L-shaped plane structures and then into rectangular structures. The response computed using the segmentation method converged with 32 connection ports. The results were compared with the response of a rectangular plane of the same size with no cut-out. The first resonance of the structure with a cut-out shifted to a lower frequency of ~650MHz as compared to ~1.5GHz for the rectangular plane.

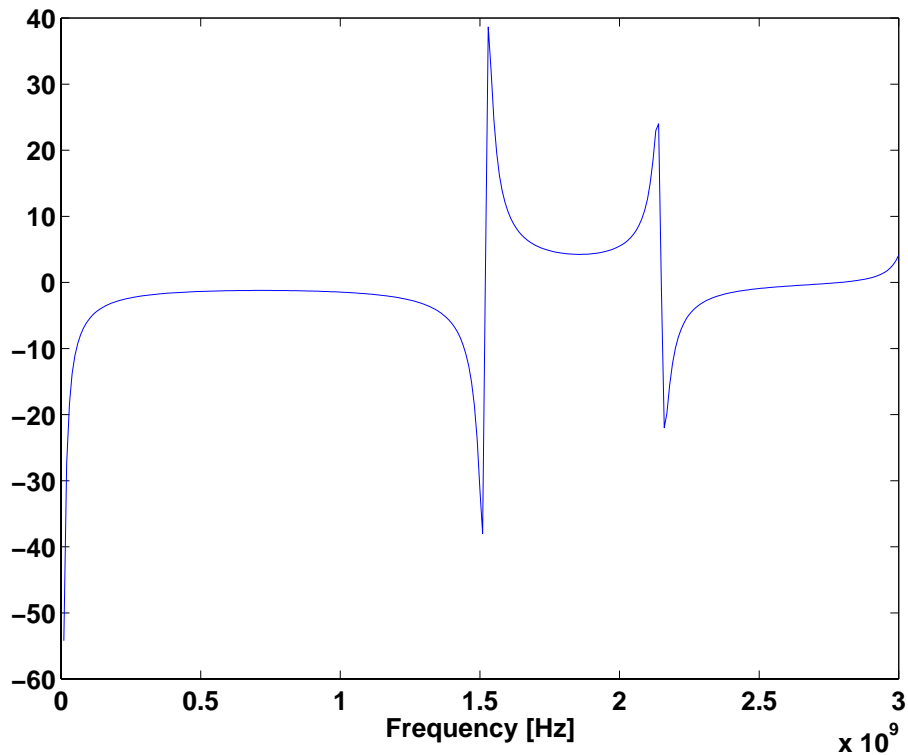


Fig. 4.9 $\text{Imag}(Z_{12})$ computed for the solid regular structure (no cut-out, 3.2cmX3.2cm) using (2.1)

Through various examples it has been shown that the response of irregular planes can be computed efficiently and accurately by using the analytical solution in Chapter 2 and the segmentation method. In Chapter 2, the rectangular planes were modeled as resonator circuits constructed directly from the solution. Since the response of irregular structures computed using the segmentation method discussed in this chapter are purely numerical, equivalent circuits need to be constructed based on the frequency response computed. A macromodeling method is discussed in Chapter 6 to model the response as rational functions.

CHAPTER 5

Decoupling Capacitors

The accurate computation of the power distribution impedance in a package is important since it helps to estimate the ground bounce and electromagnetic interference in a digital system. An important component of the power distribution network are decoupling capacitors, whose presence alters the impedance. Depending on the manner in which the capacitors alter the power distribution impedance, the ground bounce in the system may or may not be suppressed. Hence a critical sizing activity for a designer is to understand the effect of the decoupling capacitor parasitics, namely, series equivalent resistance (R_E) and inductance (L_E) on the power distribution system as well as the noise suppression obtained based on the decoupling capacitor placement.

5.1 Modeling Method

In this section, a method which incorporates decoupling capacitors into the plane solution in (2.1) is discussed. Fig. 5.1 illustrates a plane structure with a decoupling capacitor at an arbitrary port location. The impedance of the capacitor includes its parasitic inductance (L_E) and resistance (R_E). The current-voltage relationship at the ports containing the decoupling capacitors is illustrated in Fig. 5.1 using which the impedance matrix of the planes can be updated.

Let a decoupling capacitor be connected to port i , as shown in Fig. 5.1, where the current flowing into the i -th port, i_i' , is divided between the plane and the capacitor. Let the plane structure without decoupling capacitors be represented as

$$V = ZI \quad (5.1)$$

where $V = [v_1 \ v_2 \ \dots \ v_n]^T$, $I = [i_1 \ i_2 \ \dots \ i_n]^T$ are the voltage and current vectors, respectively.

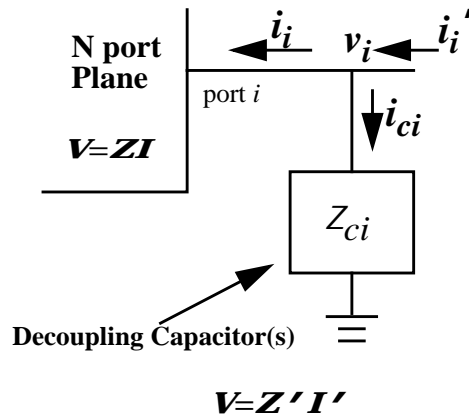


Fig. 5.1 Planes with decoupling capacitors

From Fig. 5.1, the voltages at the ports can be written as:

$$V = \begin{bmatrix} v_1 \\ v_2 \\ \dots \\ v_n \end{bmatrix} = \begin{bmatrix} z_{c1} i_{c1} \\ z_{c2} i_{c2} \\ \dots \\ z_{cn} i_{cn} \end{bmatrix} = \begin{bmatrix} z_{c1} & & & 0 \\ & z_{c2} & & \\ & & \dots & \\ 0 & & & z_{cn} \end{bmatrix} \begin{bmatrix} i_{c1} \\ i_{c2} \\ \dots \\ i_{cn} \end{bmatrix} = Z_C I_C \quad (5.2)$$

where $Z_{ci} = j\omega L_{Ei} + R_{Ei} + 1/j\omega C_i$ is the impedance of the decoupling capacitor. When multiple capacitors are connected to a port, the impedance Z_{ci} is the parallel combination of

the capacitors. Using the current relation $\mathbf{I}' = \mathbf{I} + \mathbf{I}_C$, \mathbf{V} in (5.2) can be written in terms of \mathbf{I}' as:

$$\begin{aligned} \mathbf{V} &= \mathbf{Z}(\mathbf{Z} + \mathbf{Z}_C)^{-1} \mathbf{Z}_C \mathbf{I}' \\ &= (\mathbf{Z}_C^{-1} + \mathbf{Z}^{-1})^{-1} \mathbf{I}' \\ &= \mathbf{Z}' \mathbf{I}' \end{aligned} \quad (5.3)$$

where the updated impedance matrix becomes

$$\mathbf{Z}' = (\mathbf{Z} + \mathbf{Z}_C)^{-1} \quad (5.4)$$

where \mathbf{Z}_C is the diagonal matrix containing the impedance of the decoupling capacitors and \mathbf{Z}' represents the new impedance matrix of the planes.

In (5.4), the location of each capacitor is treated as a port. The impedance matrix without capacitors is first computed at all the port locations. The capacitors are then included and the impedance matrix is updated as shown in (5.4). It is important to note that the parasitics of the capacitor include the inductance of the leads and the losses of the capacitor. Using this method, algorithms can be developed for the optimal placement of decoupling capacitors.

5.2 Test Structure

Consider a plane of size 5cm x 5cm separated by a 150 μ m thick insulator with relative dielectric constant 9.5. The resistivity of the metallization is 10.5 $\mu\Omega$ -cm. Fig. 5.2 shows the port locations where port p3 indicates the port location for a decoupling capacitor.

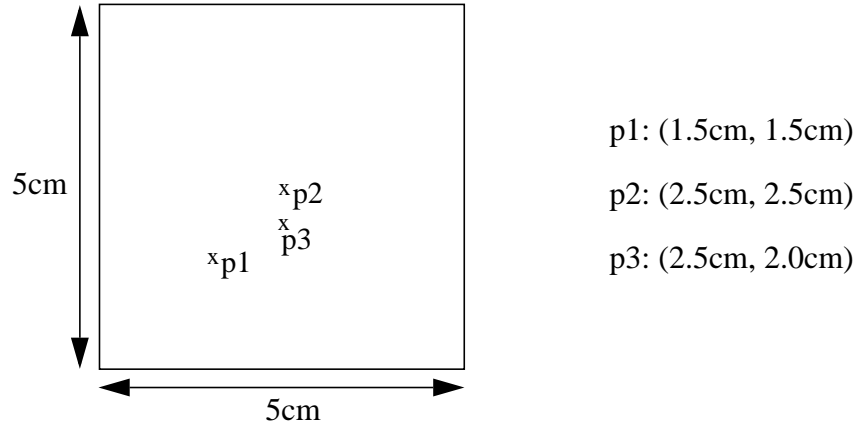


Fig. 5.2 A plane structure with a decoupling capacitor

The decoupling capacitor used has capacitance of 32nF, series inductance of 60 pH and series resistance of 50mΩ and therefore the admittance of the decoupling capacitor is

$$y_c = z_c^{-1} = \frac{1}{\frac{1}{j2\pi f x 32 \times 10^{-9}} + j2\pi f x 60 \times 10^{-12} + 0.05} \quad (5.5)$$

Hence the admittance matrix for the decoupling capacitors in (5.4) is as follows:

$$Y_C = Z_C^{-1} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & y_c \end{bmatrix} \quad (5.6)$$

The admittance matrix for the bare plane with no decoupling capacitors is computed from (2.1) as:

$$Y = Z^{-1} = \begin{bmatrix} y_{11} & y_{12} & y_{13} \\ y_{21} & y_{22} & y_{23} \\ y_{31} & y_{32} & y_{33} \end{bmatrix} \quad (5.7)$$

The updated new impedance matrix containing the decoupling capacitor in (5.4) is

$$Z' = (Y + Y_C)^{-1} = \begin{bmatrix} y_{11} & y_{12} & y_{13} \\ y_{21} & y_{22} & y_{23} \\ y_{31} & y_{32} & (y_{33} + y_c) \end{bmatrix}^{-1} \quad (5.8)$$

Figs 5.3 and 5.4 show the trans-impedance between ports p1 and p2 and self-impedance at port p2 in Fig. 5.2, respectively. The self-impedance at port p2 with a decoupling capacitor with different parasitics was computed and the performance of the decoupling capacitor was compared in Fig. 5.5. Three more decoupling capacitors of 32nF, $L_E=60\text{nH}$ and $R_E=50\text{m}\Omega$ were added to the plane at (3.0cm, 2.5cm), (2.5cm, 3.0cm) and (2.0cm, 2.5cm). The self-impedance with four decoupling capacitors was compared with the response with one decoupling capacitor in Fig. 5.6. As seen in Figs. 5.3 to 5.6, the impedance decreases over the frequency range with a new resonant frequency occurring at a lower frequency when the decoupling capacitors were added. It can be also seen that a smaller parasitic inductance L_E reduces the impedance and helps in shifting the resonance to a higher frequency. Consider the plane pair as a parallel plate capacitor of 1.4nF ($C = \epsilon A/d$). The response of the plane represented as a capacitor is compared with the plane response computed using the analytical solution in (2.1) in Fig. 5.7a. In Fig. 5.7b, a decoupling capacitor of 32nF, $L_E=60\text{nH}$ and $R_E=50\text{m}\Omega$ was added to the plane represented as a capacitor in

parallel and its response was compared with the plane response computed using (2.1) and (5.8) with the decoupling capacitor attached at port p3. It can be seen that the response of the plane represented as a capacitor agrees with the response computed using (2.1) and (5.8) only at very low frequencies up to 100MHz, indicating the importance of treating the plane as a cavity resonator and not just a lumped capacitor.

5.3 Summary

In this chapter, a method for incorporating decoupling capacitors into the plane solution has been discussed. It has been demonstrated that the presence of decoupling capacitors decreases the plane impedance at high frequency. In addition, decoupling capacitors shift the resonance frequencies of the unpopulated plane to lower frequencies with much smaller impedance. The effect of parasitics of the decoupling capacitors on the impedance of the plane was also analyzed using a test structure.

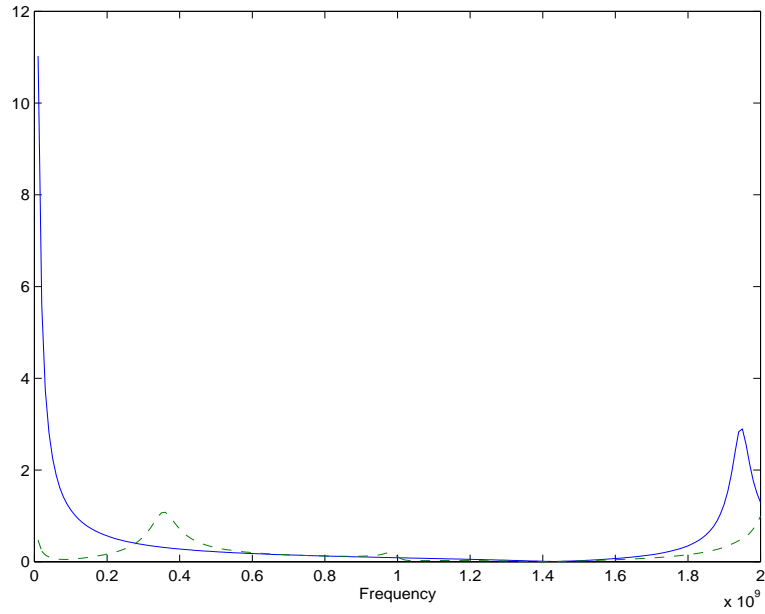


Fig. 5.3 Trans-impedance between ports p1 and p2 with a decoupling capacitor of 32nF, $R_E=50m\Omega$ and $L_E=60nH$ at port p3 (dashed) and with no decoupling capacitor (solid)

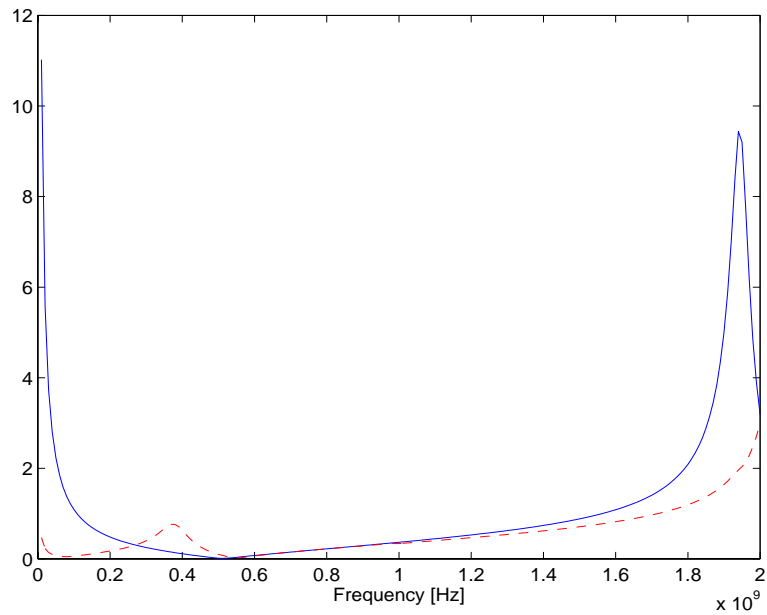


Fig. 5.4 Self-impedance at port p2 with a decoupling capacitor of 32nF, $R_E=50m\Omega$ and $L_E=60nH$ at port p3 (dashed) and with no decoupling capacitor (solid)

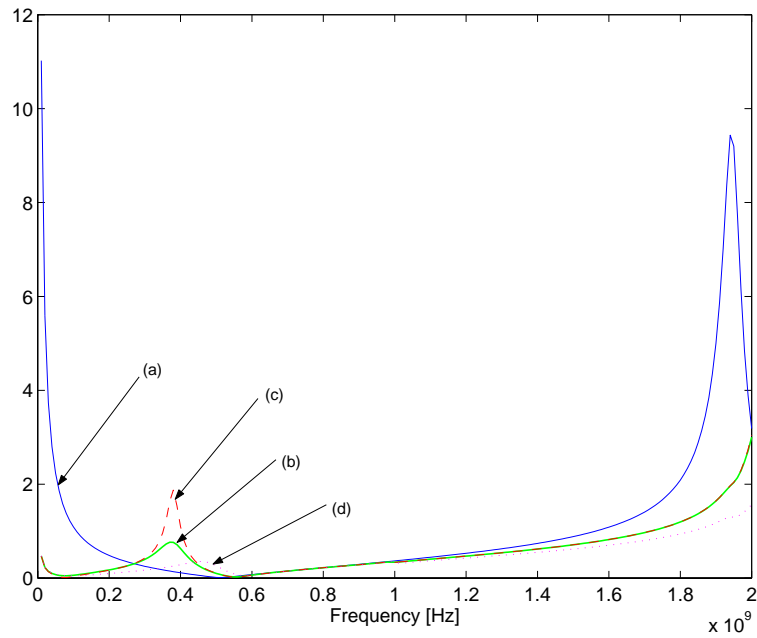


Fig. 5.5 Self-impedance at port p2 (a) with no decoupling capacitor, (b) with a decoupling capacitor of 32nF, $R_E=50\text{m}\Omega$ and $L_E=60\text{nH}$, (c) with 32nF, $R_E=10\text{m}\Omega$ and $L_E=60\text{nH}$ and (d) with 32nF, $R_E=50\text{m}\Omega$ and $L_E=10\text{nH}$ placed at port p3.

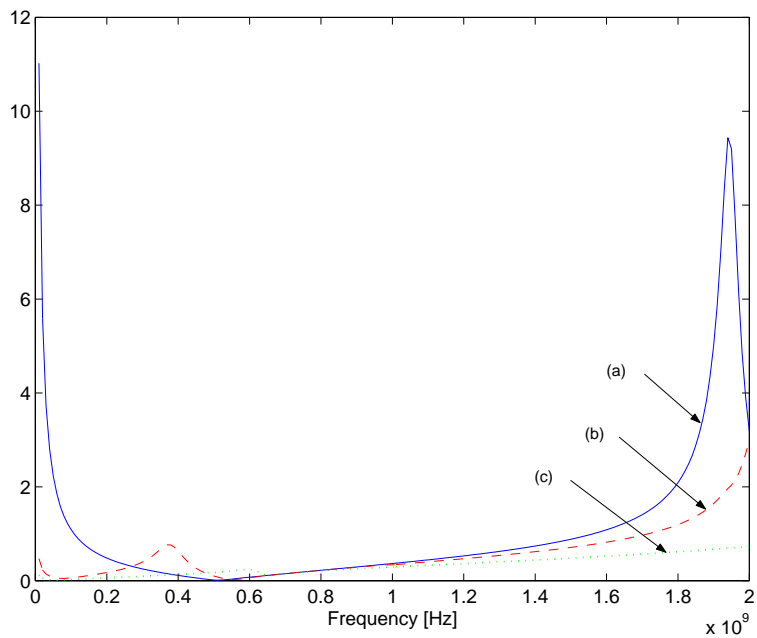


Fig. 5.6 Self-impedance at port p2 (a) with no decoupling capacitor, (b) with one decoupling capacitor of 32nF, $R_E=50\text{m}\Omega$ and $L_E=60\text{nH}$ and (c) with four decoupling capacitors of 32nF, $R_E=50\text{m}\Omega$ and $L_E=60\text{nH}$ placed at port p3.

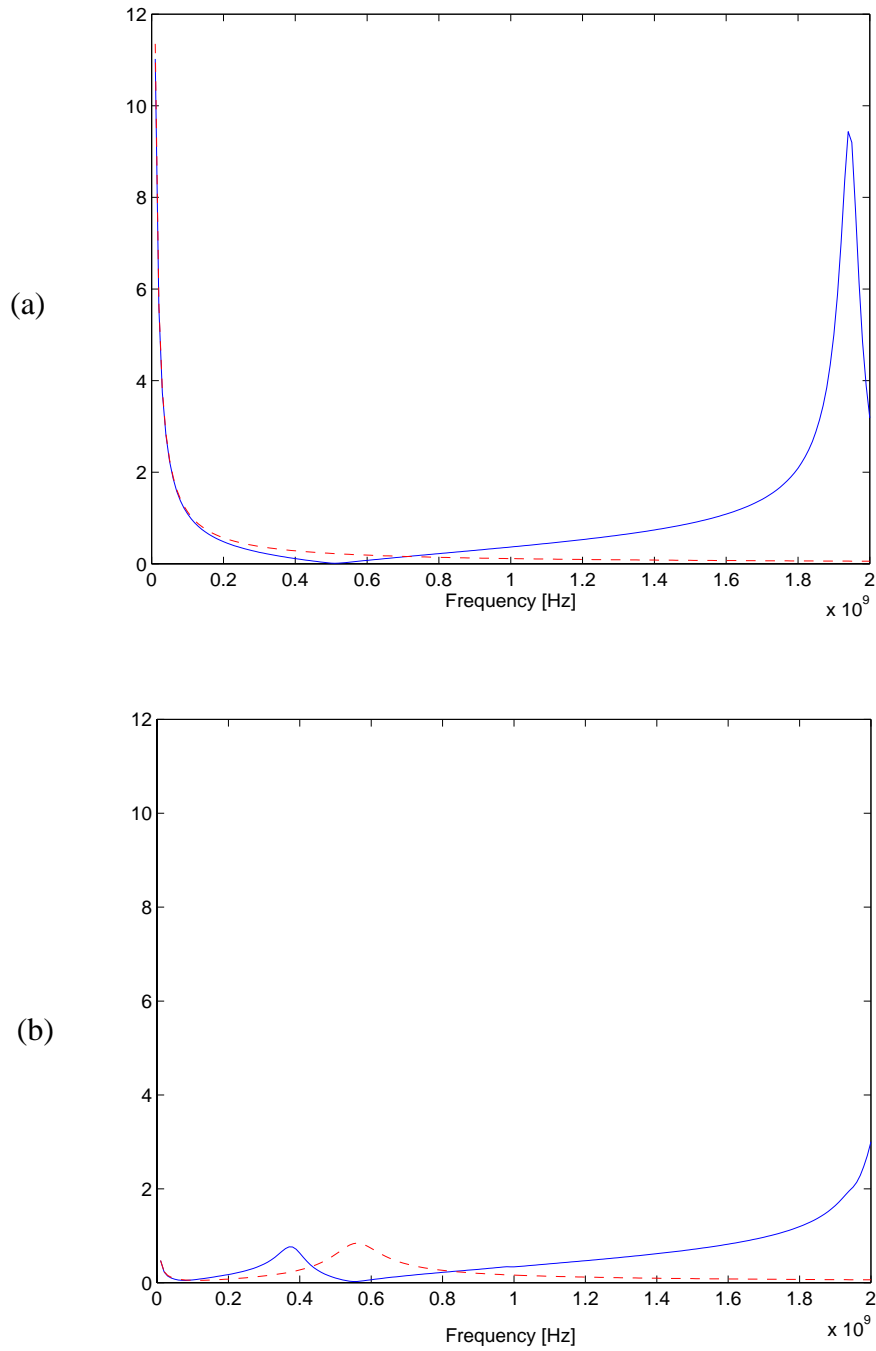


Fig. 5.7 (a) Plane response at port p2 with no decoupling capacitor at port p3, computed using (2.1) (solid) and treated as a capacitor (dashed), and (b) Plane response at port p2 with a decoupling capacitor of 32 nF, $L_E = 60$ pH and $R_E = 50$ m Ω connected at port p3, computed using (2.1) (solid) and treated as a capacitor (dashed)

CHAPTER 6

Macromodeling using Rational Functions

The previous chapters enable the analysis of irregular shaped planes and planes with decoupling capacitors. Using the methods described, the frequency response at port location can be computed. However, this data needs to be included as part of a larger network for simulation with non-linear devices. This is possible through macromodels, details of which are discussed in this chapter. The advantage of using macromodels are the following: a) a complex network can be represented by using a reduced order model by eliminating the internal nodes and b) they reduce the computational complexity of the convolution integral to $O(N)$ operations for an N step transient simulation [29].

When the frequency response of a device is available as a look-up table, the device can be modeled using rational functions called macromodels. The high frequency features of the system can be captured through equivalent circuits using circuit parameters, Z (impedance), Y (admittance) or S (scattering), represented as rational functions. Using macromodeling, the dominant poles of the system can be captured using reduced order models. This enables the representation of systems through simple models. In this chapter, the macromodeling method discussed in [30],[31] is described and the issues associated with the macromodeling for complex systems are discussed.

6.1 Eigenvalue Problem

Assuming the frequency response of the device is known as a look-up table, the data can be captured using a rational function of the form:

$$H(s) = \frac{a_0 + a_1s + \dots + a_p s^p}{b_0 + b_1s + \dots + b_q s^q} \quad (6.1)$$

where $s = j\omega$, $H(s)$ is the available data at discrete frequencies and a_i, b_i are unknown coefficients to be computed. (6.1) is rewritten as

$$a_0 + a_1s + \dots + a_p s^p - b_0H(s) - b_1sH(s) - \dots - b_q s^q H(s) = 0 \quad (6.2)$$

(6.2) is next rearranged as a matrix equation as in (6.3) where ‘A’ is a known matrix and ‘X’ is the solution vector to be found.

$$\underbrace{\begin{bmatrix} 1 & s_1 & s_1^2 & \dots & s_1^p & -H(s_1) & -s_1H(s_1) & \dots & -s_1^q H(s_1) \\ 1 & s_2 & s_2^2 & \dots & s_2^p & -H(s_2) & -s_2H(s_2) & \dots & -s_2^q H(s_2) \\ & & & \dots & & & & & \\ & & & & & & & & \\ & & & & & & & & \\ 1 & s_n & s_n^2 & \dots & s_n^p & -H(s_n) & -s_nH(s_n) & \dots & -s_n^q H(s_n) \end{bmatrix}}_{\mathbf{A}} \underbrace{\begin{bmatrix} a_0 \\ a_1 \\ \cdot \\ a_p \\ b_0 \\ b_1 \\ \cdot \\ b_q \end{bmatrix}}_{\mathbf{X}} = \mathbf{0} \quad (6.3)$$

The coefficients in X of (6.3) are found by solving the eigenvectors and eigenvalues of the equation [32],[33]:

$$A^H A X = \lambda_{min} X \quad (6.4)$$

where A^H is the complex conjugate transpose of the matrix A . The solution is the eigenvector corresponding to the minimum eigenvalue (λ_{min}) closest to zero. Since the matrix $A^H A$ is complex, the eigenvectors are complex. For the rational function in (6.1) to be realizable, the condition that all the coefficients in (6.1) are real is enforced. Since X is a real vector with the enforced condition and the eigenvalues of a Hermitian matrix $A^H A$ are real, the term on the right side of the equation in (6.4) is a real vector and hence (6.4) can be written as

$$Re(A^H A) X = \lambda_{min} X \quad (6.5)$$

Hence, the solution is obtained by solving the eigenvector of $Re(A^H A)$ corresponding to the minimum eigenvalue. In (6.5), the frequencies are normalized with a scaling factor for a numerically stable result during computation.

This macromodeling method has been successfully used for modeling electrically small and lossy structures in [30] and [34] for which stable models have been constructed. As the system gets complex, ensuring the passivity of the macromodels is critical for transient simulations. The issues related to passivity will be discussed in the next chapter.

When a large number of ports in an electrically large system are modeled, a huge matrix in (6.3) needs to be solved and this can be a problem due to limited computer resources and due to the ill-conditioned matrix 'A' in (6.3).

In [30] and [34], all the rational functions for the multi-port response were obtained simultaneously with common denominator polynomials, i.e., common poles. A phenomena observed in modeling an electrically large system is that the effects of some poles are cancelled based on the port locations, as discussed in Sec. 2.2 on model order reduction, i.e., a pole observed at a port may not occur at another port. Solving the eigenvalue problem simultaneously for all the ports with different poles can cause matrix 'A' in (6.3) to be ill-conditioned. Also, the number of ports which can be solved simultaneously is limited by the computer memory. To avoid this problem, each port is solved separately by computing the eigenvectors for each circuit parameter (S , Y or Z), to generate individual rational functions with different poles.

Consider the plane structure in Fig. 2.2. The scattering parameters (S) for the 15 ports on the structure were computed using (2.1) and (2.2) and modeled as rational functions. Each parameter was modeled as described above. The macromodeling results for the reflection at port 1 and transmission between ports 7 and 8 are shown in Fig. 6.1.

S_{11} was captured using a rational function with $p=11$ and $q=12$ model orders while S_{78} was captured using model orders $p=2$ and $q=3$. Further results on S parameters and macromodels are available in the appendix. The minimum model orders required are found by either investigating the eigenvalues as a function of the polynomial orders as shown in Fig. 6.2 or by counting the number of resonant frequencies present in the table for highly resonant systems. In Fig. 6.2, the minimum eigenvalue converges close to zero near the appropriate model order, which can be used for determining the order of the rational functions.

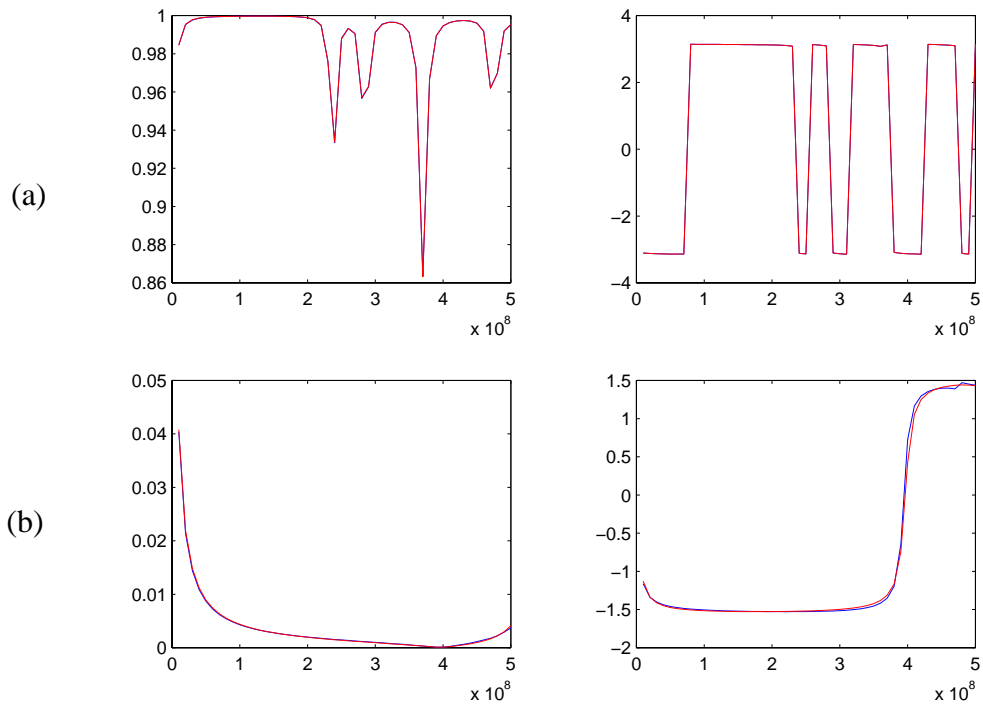


Fig. 6.1 Response of rational functions (a) S_{11} magnitude and phase and (b) S_{78} magnitude and phase

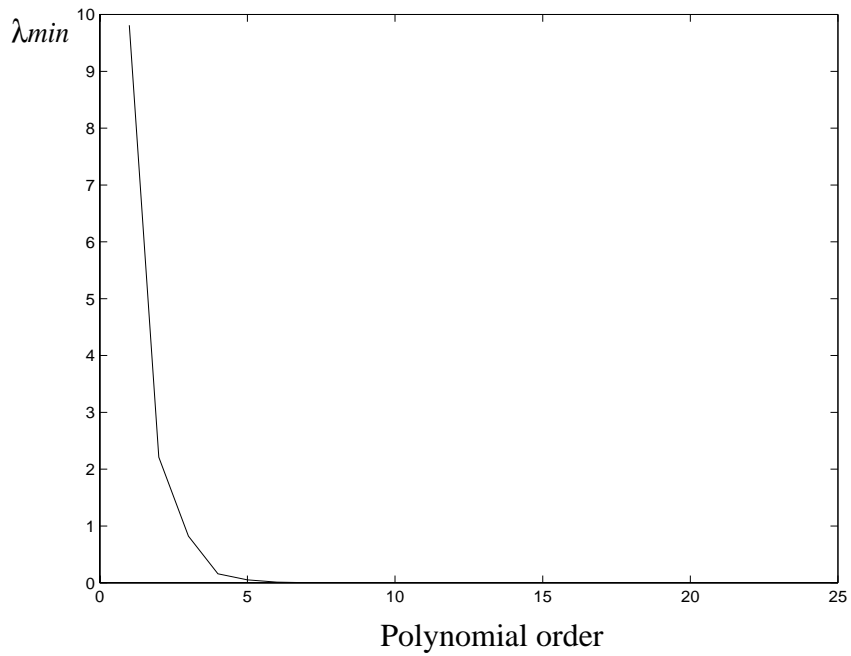


Fig. 6.2 Minimum eigenvalue convergence for generating macromodels.

In [31], macromodeling has been applied to electrically small and simple devices for which stable macromodels with small orders were found. However, for an electrically large system with a complex response, the macromodeling method in [31] does not guarantee a passive model.

In the following sections, methods have been presented for constructing equivalent circuits based on various circuit parameters. Enforcement of the passivity of circuits will be discussed in the next chapter.

6.2 Equivalent Circuit Based on S-parameters

The rational functions developed using macromodels in Sec. 6.1 can be used to implement equivalent circuits using dependent current or voltage sources. In this section, some examples of equivalent circuits using macromodels based on Y and Z parameters are introduced with HSPICE functions. Also the circuit using S parameter-based macromodels is developed for highly resonant systems. A circuit using Y-parameters can be represented as

$$I_i = \sum_j Y_{ij}(s)V_j \quad (6.6)$$

(6.6) can be implemented in HSPICE using dependent voltage sources as shown in Fig. 6.3. Similarly, a circuit using Z-parameters can be represented as

$$V_i = \sum_j Z_{ij}(s)I_j \quad (6.7)$$

Since dependent current sources are not available for rational functions in HSPICE, the circuit is formed using dependent voltage sources as in Fig. 6.4. These circuits using Y or Z parameters have been used successfully for simulating lossy and electrically small structures such as resistors and capacitors [31],[34].

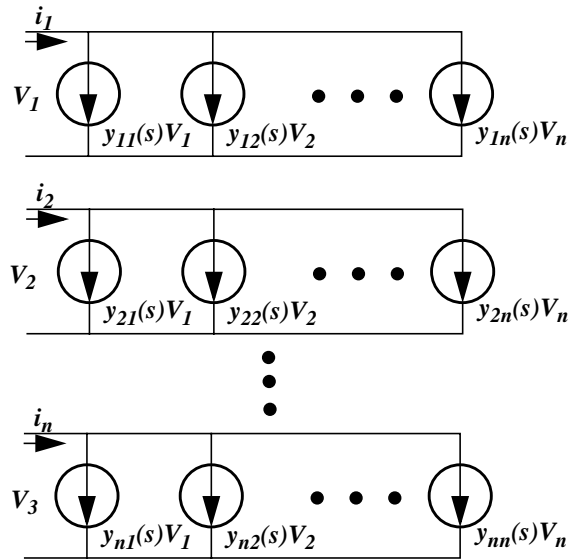


Fig. 6.3 Circuit implementation using Y-parameter macromodels

However, for resonant circuits such as power distribution networks, the Y and Z parameter networks can introduce errors during transient simulation. This is because the frequency response has large variations in amplitude making it difficult to capture its behavior at both DC and high frequencies using rational functions. S parameter macromodels can be used to avoid these errors in modeling systems with multiple resonances. Since S parameters of passive systems are bounded in value ($|S(s)| \leq 1$), macromodels using S parameters can capture both the DC and high frequency characteristics well.

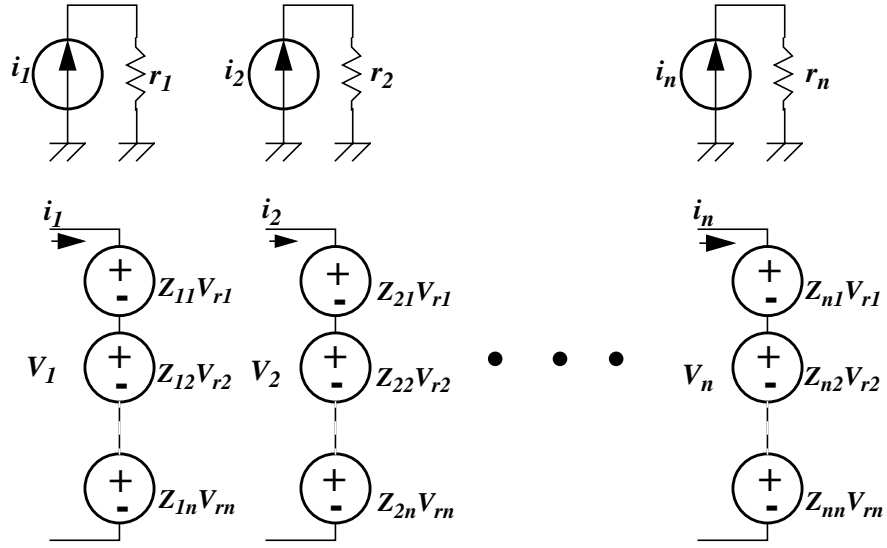


Fig. 6.4 Circuit implementation using Z-parameter macromodels

A technique for developing equivalent circuits using S-parameters for microwave circuits has been discussed in [35], which can be represented in the form:

$$V_i = Z_o \frac{1 + S_{ii}}{1 - S_{ii}} I_i + \sum_{j=1}^N \frac{S_{ij}}{1 - S_{ii}} [V_j + Z_o I_j] \quad i, j = 1, \dots, N, i \neq j \quad (6.8)$$

where Z_o is the port characteristic impedance. In [35] the circuit in (6.5) was implemented using a look-up table containing S-parameters as a function of frequency. By implementing the circuit using macromodels, the circuit can be simulated faster and more accurately. This is because rational functions enable recursion for computing the transient response and provide a good interpolation between frequency points. Macromodels can be constructed for the functions $(1+S_{ii})/(1-S_{ii})$ and $S_{ij}/(1-S_{ii})$. By placing a small resistor in series

with the ports and expressing the current terms in (6.8) by the voltage across the resistor, all terms can be implemented using voltage controlled voltage sources. An alternate equivalent circuit can also be obtained by multiplying both sides in (6.8) by $(1-S_{ii})$ and rearranging it as follows [36]:

$$V_i = S_{ii}V_i + Z_o(1 + S_{ii})I_i + \sum_{j=1}^N S_{ij}[V_j + Z_oI_j] \quad i,j = 1, \dots, N, i \neq j \quad (6.9)$$

which can be implemented using dependent sources. In (6.9) macromodels can be developed for the S-parameters directly without any transformation. Fig. 6.5 shows the circuit diagram using (6.9). The resistors r_1 - r_n in Fig. 6.5 are for sensing the currents at each port in (6.9) and realizing the circuit using voltage-controlled voltage sources, since the current-controlled voltage sources are not available in HSPICE.

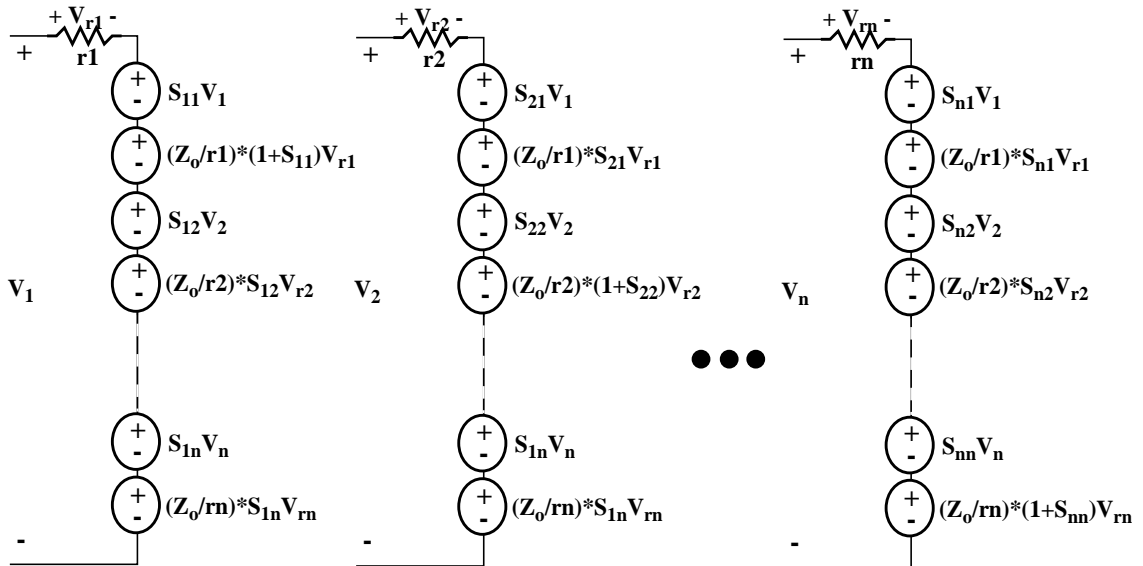


Fig. 6.5 Circuit implementation using S-parameter macromodels

Scattering parameters are used to capture the reflection and transmission characteristics of microwave circuits. In the next section, methods have been developed to capture the behavior of interconnects and planes using S-parameter macromodels.

6.3 Test Cases

6.3.1 Test Case 1: Modeling of a Transmission Line

Transmission lines are often described as a distributed network which is represented as a large network of passive lumped elements. These transmission lines can be represented using a reduced order model over the frequency range of interest. As an example, consider a 4 mm-long transmission line consisting of a distributed network of 40 cascaded segments as shown in Fig. 6.6. Each segment consists of $L=55.5\text{pH}$, $C=8.3\text{fF}$ and $R=1\text{e-}5\Omega$ (~loss-less) and L and R are divided by 2 to form a symmetric network. The frequency response of the two port system has been modeled as a rational function using macromodels.

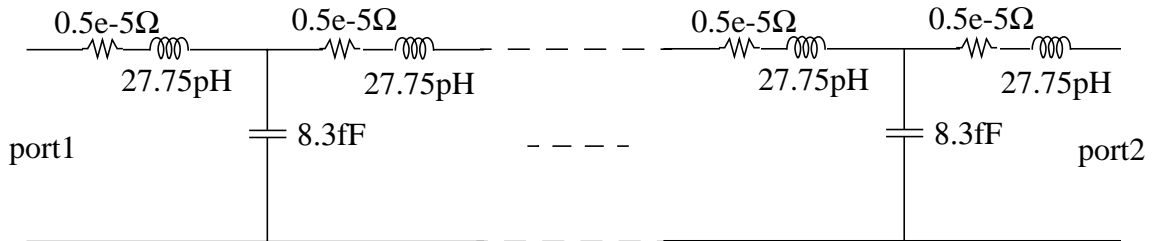


Fig. 6.6 Transmission line represented as a network of R, L and C

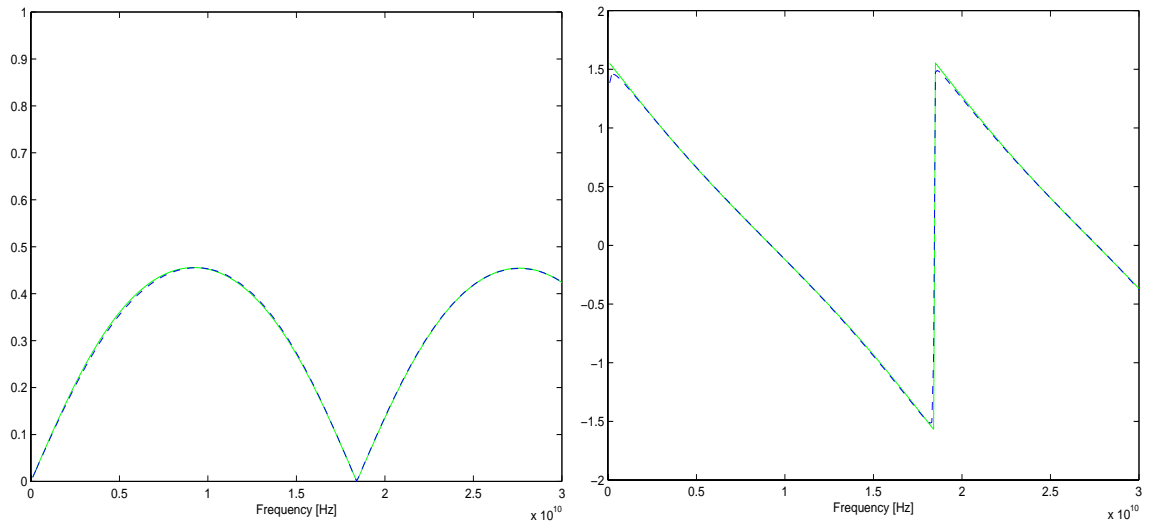
The S-parameters for the network containing 40 segments were extracted using HSPICE simulation. The macromodels for the S-parameters based on the data up to 30GHz were generated with $p=6$ (numerator) and $q=6$ (denominator) orders as in (6.10).

$$S_{11}(s) = \frac{a_0 + a_1s + \dots + a_6s^6}{d_0 + d_1s + \dots + d_6s^6} \quad S_{12}(s) = \frac{b_0 + b_1s + \dots + b_6s^6}{d_0 + d_1s + \dots + d_6s^6} \quad (6.10)$$

where

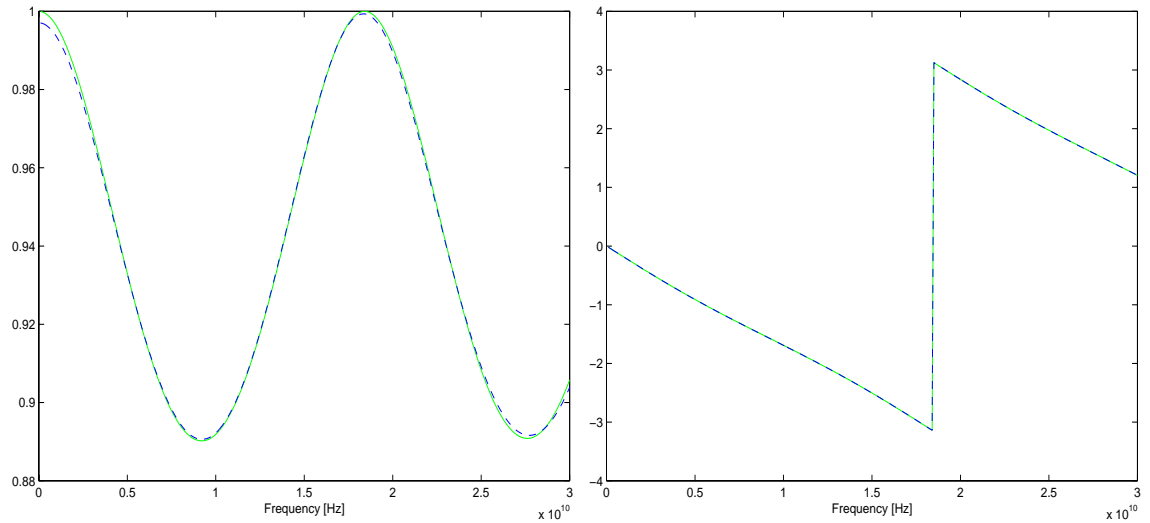
$a_0 = 9.9972\text{e-}04$	$b_0 = 6.8692\text{e-}01$	$d_0 = 6.8896\text{e-}01$
$a_1 = 9.3481\text{e-}12$	$b_1 = -2.2185\text{e-}12$	$d_1 = 1.8755\text{e-}11$
$a_2 = -2.7293\text{e-}23$	$b_2 = -1.3173\text{e-}23$	$d_2 = 1.7525\text{e-}22$
$a_3 = 8.8979\text{e-}34$	$b_3 = -2.8583\text{e-}36$	$d_3 = 1.3647\text{e-}33$
$a_4 = -2.4981\text{e-}45$	$b_4 = 7.1356\text{e-}46$	$d_4 = 3.8429\text{e-}45$
$a_5 = 1.4286\text{e-}56$	$b_5 = -4.2665\text{e-}57$	$d_5 = 1.3749\text{e-}56$
$a_6 = -3.3597\text{e-}68$	$b_6 = 7.5387\text{e-}69$	$d_6 = 2.1797\text{e-}69$

Thus the transmission line consisting of 40 RLC sections has been represented as a 6th order model. In this model, the poles occurred at frequencies 0, 18.2GHz and 38.4GHz. The frequency response using the cascaded model and macromodels are shown in Fig. 6.7. A pulse was injected onto the transmission line from one terminal with the other terminal open-ended, as shown in Fig. 6.8, for a transient simulation. Fig. 6.9 shows the transient response of the test setup in Fig. 6.8, using the cascaded model and macromodels. The transient simulation of the cascaded network took 1 min. 8 sec. and the simulation with the macromodel took 45 seconds on a SUN Ultra Sparc workstation. This time can be further reduced by using recursive convolution [29]. A transmission line can be modeled as a frequency-dependent model using this method and could be used to simulate the noise over bouncing planes.



(a)

(b)



(c)

(d)

Fig. 6.7 Response of the transmission line: raw data (solid line) and macromodeling result (dashed), (a) S_{11} magnitude, (b) S_{11} phase, (c) S_{12} magnitude and (d) S_{12} phase

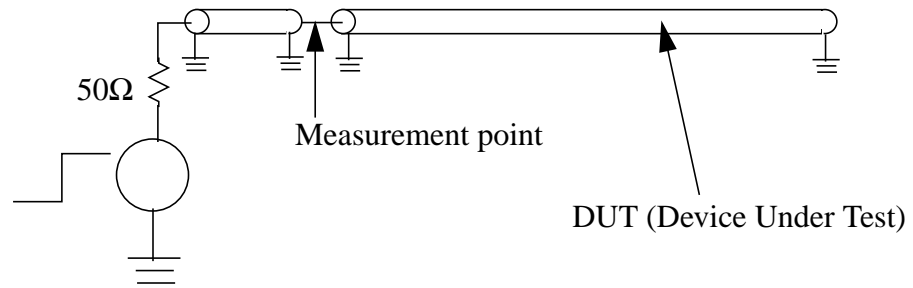


Fig. 6.8 Transmission line with a pulse injected onto one terminal and the other terminal open-ended for transient simulation

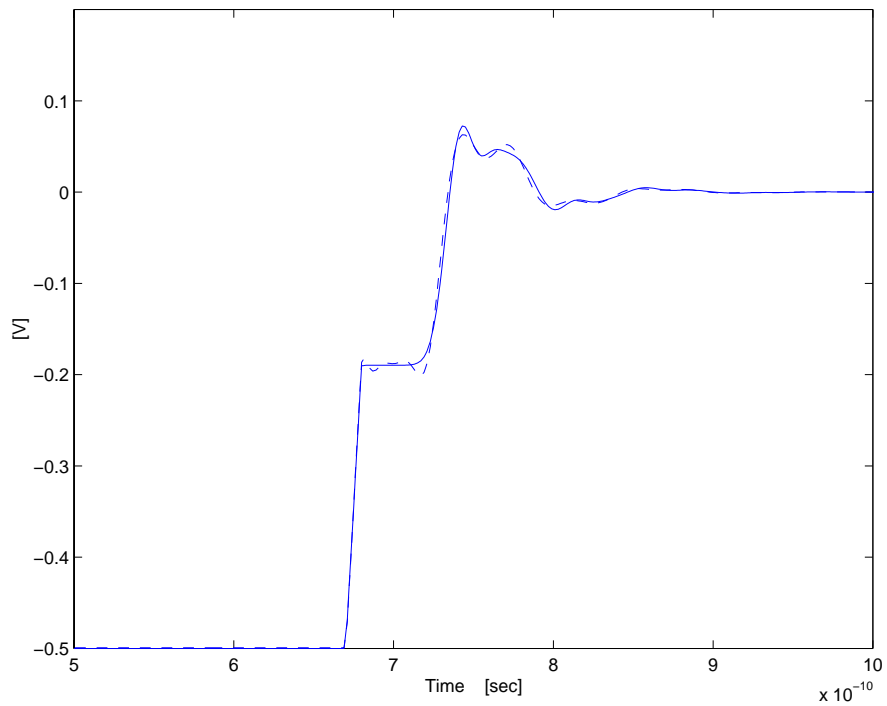


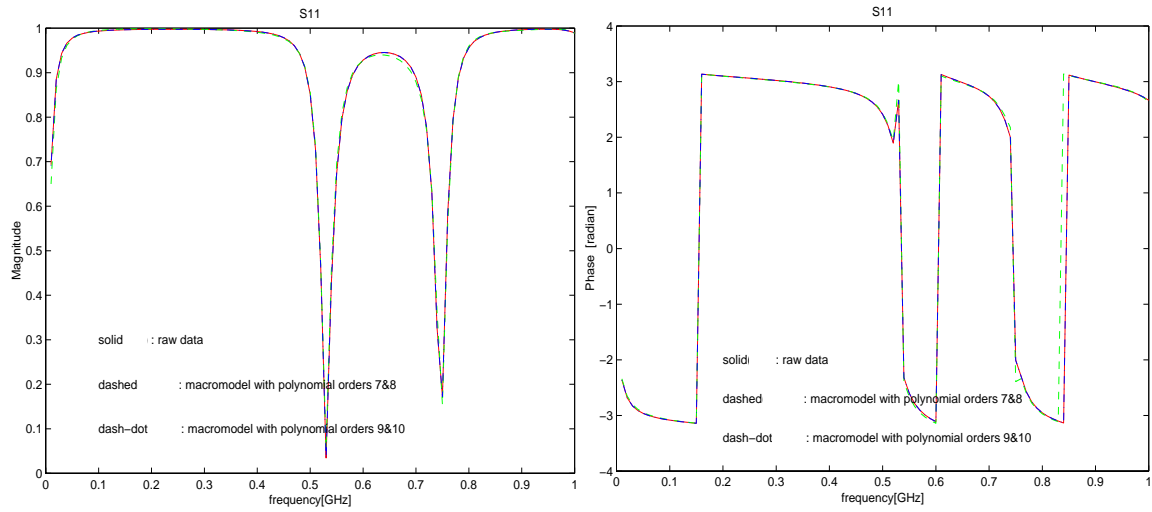
Fig. 6.9 Transient response of the transmission line with a pulse injected into one terminal and the other terminal open-ended: distributed network (solid) and macromodel (dashed)

6.3.2 Test Case 2: Modeling of Planes

As another example, the test vehicle in Fig. 3.1 was simulated using the macromodeling method. The test vehicle in Fig. 3.1 is electrically large and showed multiple resonances over the frequency bandwidth of interest. Two macromodels with different polynomial orders were generated based on the computed data from 0 to 1 GHz for the response between ports 1 and 3 on the plane. The first macromodel was generated with $p=7$ and $q=8$ for numerator and denominator orders in (6.1) by capturing the poles at 528.8MHz, 749.7MHz and 1.0471GHz. A second model was generated with $p=9$ and $q=10$ by capturing the poles at 528.8MHz, 748.1MHz, 1.0493GHz and 1.1898GHz. The macromodeling result is shown in Fig. 6.10. Fig. 6.11 shows the comparison of the transient simulation results using the two macromodels.

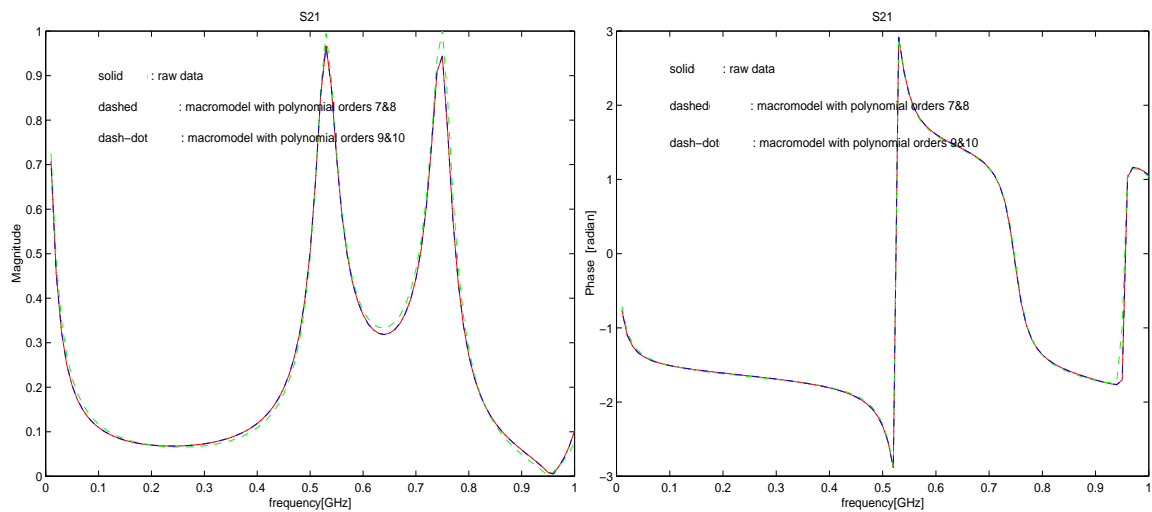
Since the response with the higher order model does not improve the accuracy much compared to the lower order model, the lower order model is desirable due to the smaller simulation time required. However, the lower order model shows spurious oscillations as compared to the higher order model. Therefore, the modeling order needs to be high enough to account for the delay accurately.

When the frequency response is available as a table, the package structures can be modeled using a reduced order model through the S-parameter equivalent circuits, as described in the two test cases.



(a)

(b)



(c)

(d)

Fig. 6.10 Macromodeling with the data over 0 to 1GHz : S_{11} (a) magnitude and (b) phase, and S_{21} (c) magnitude and (d) phase between ports 1 and 3, computed raw data (solid), model with 7&8th orders (dashed), model with 9&10 th orders (dash-dot)

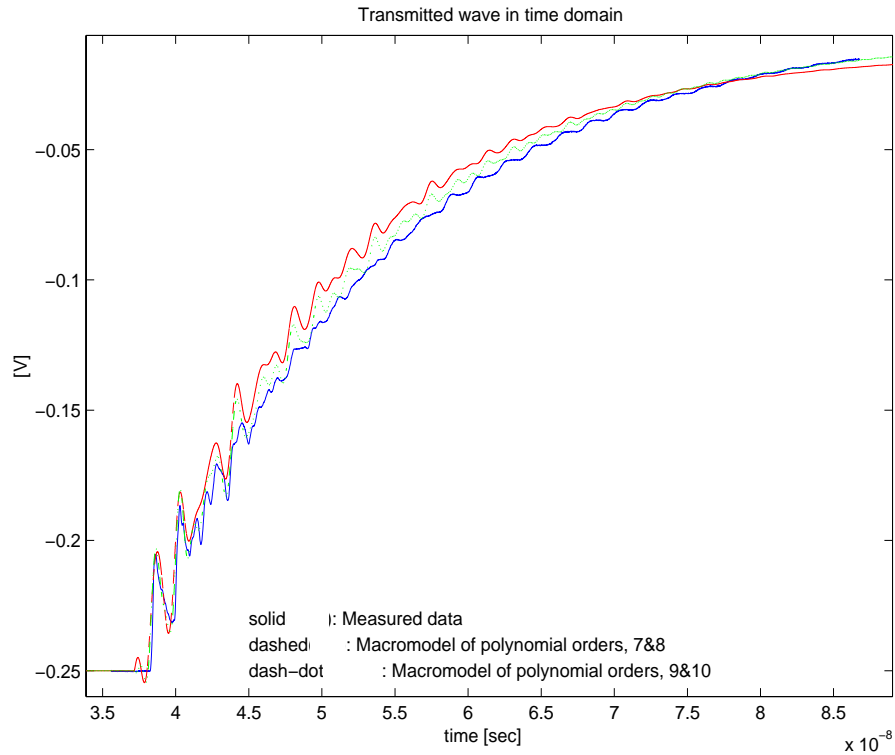


Fig. 6.11 Transient response with the two different macromodels

6.3.3 Modeling of a Split Plane Structure

In this section, a split plane structure populated with decoupling capacitors as shown in Fig. 6.12 was modeled [37]. The physical dimension of the plane pair is $12\text{cm} \times 30\text{cm}$ and the top plane is split with a gap of 5mm while the bottom plane is continuous. The split planes P1 and P2 are connected together with a parallel circuit with 0.15pF , 95Ω and 0.17nH components. The dielectric thickness is $700\mu\text{m}$ with a relative permittivity of 4. The metal conductivity is $5.8 \times 10^5 \text{mho/cm}$. The squares and slashes which form a uniform grid indicate the locations of the decoupling capacitors of 220nF with $R_E = 0.1\Omega$ and

$L_E=2\text{nH}$ and 10nF with $R_E=0.1\Omega$ and $L_E=2\text{nH}$, respectively. In Fig. 6.12, ‘S’ indicates the source port and ‘M1’, ‘M2’ the measurement ports.

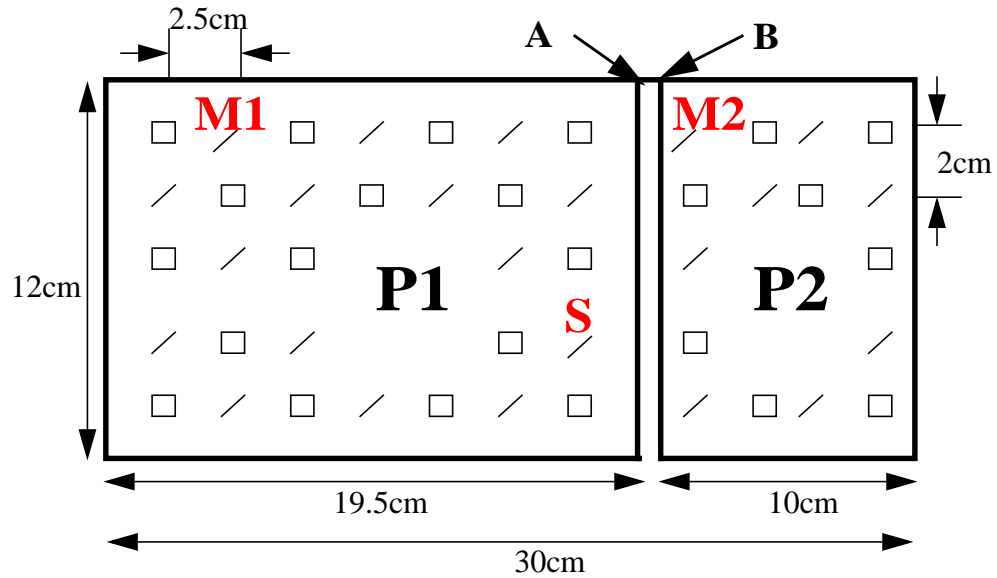


Fig. 6.12 A split plane structure with decoupling capacitors, 10nF with $R_E=0.1\Omega$ and $L_E=2\text{nH}(\diagup)$ and 220pF with $R_E=0.1\Omega$ and $L_E=2\text{nH}(\square)$. The circuit between A and B consists of 0.15pF , 95Ω and 0.17nH in parallel.

The structure can be represented as a reduced order model between the ports by first computing the frequency response using the methods described in the previous chapters. This requires a three step process namely,

- 1) Computing the frequency response of the bare planes using (2.1)
- 2) Updating the impedance matrix by including decoupling capacitors using (5.4)
- 3) Applying the method of segmentation to connect planes P1 and P2 together using the circuit element between points A and B [37].

This approach assumes that the two plane pairs are isolated and the only interaction that can occur between the plane pairs is through the circuit element at A,B. The fre-

quency response of each plane pair was first computed using (2.1) up to 1 GHz. The locations of the decoupling capacitors were represented as ports. Ports S, M1 and M2 were defined at the decoupling capacitor locations and ports A and B were defined as additional ports. Therefore the frequency response of P1 was computed at 36 ports including port A and the frequency response of P2 at 21 ports including port B. The computed impedance matrix was updated for each plane pair by including the frequency response of the decoupling capacitors, as described in Chapter 5, as follows:

$$\begin{aligned} Z1 &= (Z_{C1}^{-1} + Z_{P1}^{-1})^{-1} \\ &= (Y_{C1} + Y_{P1})^{-1} \end{aligned} \quad (6.11a)$$

and

$$\begin{aligned} Z2 &= (Z_{C2}^{-1} + Z_{P2}^{-1})^{-1} \\ &= (Y_{C2} + Y_{P2})^{-1} \end{aligned} \quad (6.11b)$$

where Z_{P_i} and Y_{P_i} are the impedance and admittance matrices of the bare plane pairs without decoupling capacitors and Z_{C_i} and Y_{C_i} are the diagonal matrices representing the decoupling capacitors. For example, the matrix Y_{C_i} is

$$Y_{C_i} = \begin{bmatrix} y_{c1} & & & & \\ & y_{c2} & & & \\ & & \mathbf{0} & & \\ & & & \cdots & \\ \mathbf{0} & & & & y_{cn} \end{bmatrix} \quad (6.12)$$

where y_{ci} represents the admittance of the decoupling capacitors at each port defined by

$$y_{ci} = \frac{1}{1/sC + R_E + sL_E} \quad (6.13)$$

where C is 10nF or 220pF, R_E is 0.1Ω and L_E is 2nH.

By separating the ports for the decoupling capacitors from the other ports ‘S’, ‘M1’ and ‘A’, the impedance matrix for plane pair P1 can be partitioned as follows:

$$Z_{\alpha} = \left(Z_{C\alpha}^{-1} + Z_{B\alpha} \right)^{-1} = \begin{bmatrix} Z_{aa} & Z_{ap} \\ Z_{pa} & Z_{pp} \end{bmatrix} \quad (6.14)$$

where $Z_{B\alpha}$ is the impedance of the bare plane pair without capacitors and $Z_{C\alpha}$ is the impedance matrix for the capacitors as described in (6.11) and (6.12). In (6.14), Z_{aa} is a submatrix containing the three ports ‘S’, ‘M1’, ‘A’ on P1 and Z_{pp} is a submatrix for the decoupling capacitors. The response of P2 is obtained in a similar way as:

$$Z_{\beta} = \left(Z_{C\beta}^{-1} + Z_{B\beta} \right)^{-1} = \begin{bmatrix} Z_{bb} & Z_{bq} \\ Z_{qb} & Z_{qq} \end{bmatrix} \quad (6.15)$$

where β and q indicates the ports for ‘M2’ and ‘B’, respectively.

Since only the frequency response at the ports ‘S’, ‘M1’ and ‘M2’ are desired, the submatrices Z_{aa} and Z_{bb} are used for computing the frequency response at the ports of interest. Matrices Z_{aa} and Z_{bb} can be written as:

$$Z_{aa} = \begin{bmatrix} Z_{11a} & Z_{12a} & Z_{13a} \\ Z_{21a} & Z_{22a} & Z_{23a} \\ Z_{31a} & Z_{32a} & Z_{33a} \end{bmatrix} \quad Z_{bb} = \begin{bmatrix} Z_{11b} & Z_{12b} \\ Z_{21b} & Z_{22b} \end{bmatrix} \quad (6.17)$$

where $1a$, $2a$ and $3a$ represent the ports 'S', 'M1', 'A' on P1 and $1b$ and $2b$ represent the ports 'M2' and 'B' on P2, respectively.

Using the current-voltage relation at 'B' and using the method of segmentation described in Chapter 4, the frequency response of the whole system at the desired ports can be computed as

$$Z_T = \begin{bmatrix} Z_{S,S} & Z_{S,M1} & Z_{S,M2} \\ Z_{M1,S} & Z_{M1,M1} & Z_{M1,M2} \\ Z_{M2,S} & Z_{M2,M1} & Z_{M2,M2} \end{bmatrix} \quad (6.18)$$

$$= \begin{bmatrix} Z_{11a} & Z_{12a} & 0 \\ Z_{21a} & Z_{22a} & 0 \\ 0 & 0 & Z_{11b} \end{bmatrix} + \begin{bmatrix} Z_{13a} \\ Z_{23a} \\ -Z_{12b} \end{bmatrix} \left(Z'_{33a} + Z_{22b} \right)^{-1} \begin{bmatrix} -Z_{31a} & -Z_{32a} & Z_{21b} \end{bmatrix}$$

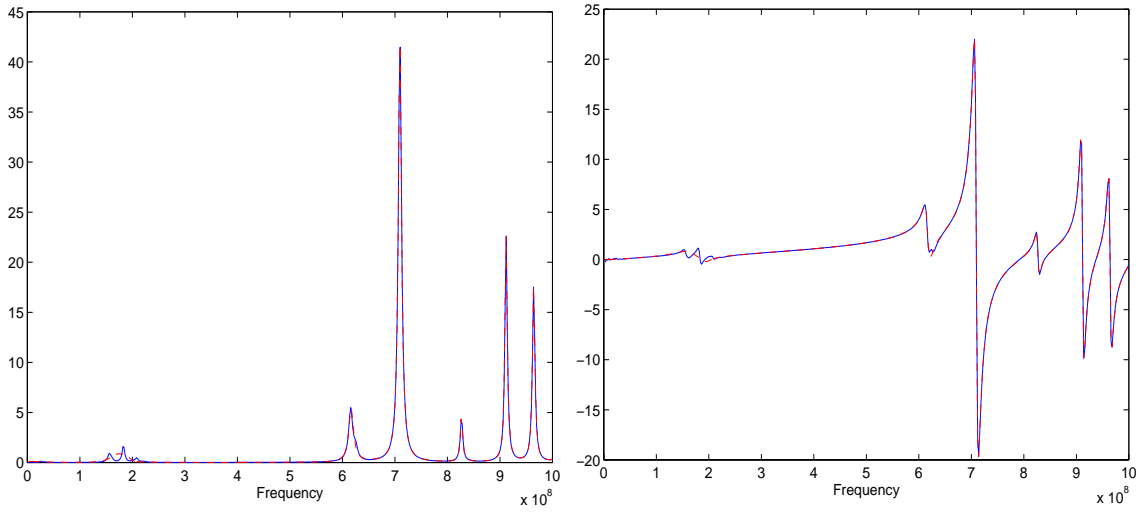
where $Z'_{33a} = Z_{33a} + Z_{AB}$ and Z_{AB} is the impedance for the circuit element between 'A' and 'B':

$$Z_{AB} = \frac{1}{j\omega \times 1.5 \times 10^{-13}} + 95 + j\omega \times 1.7 \times 10^{-10} \quad (6.19)$$

After computing the frequency response, the macromodels at each port were generated using

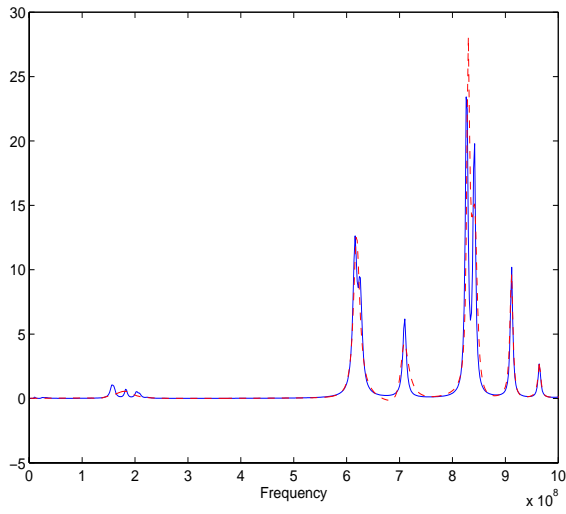
$$Z_{ij}(s) = \frac{a_0 + a_1s + \dots + a_p s^p}{b_0 + b_1s + \dots + b_q s^q} \quad (6.20)$$

by solving the eigenvalue problem described in Sec. 6.1. The order of the macromodels were $p=18, q=18$ for $Z_{S,S}$, $p=17, q=17$ for $Z_{S,M1}$, $p=19, q=20$ for $Z_{M1,M1}$, $p=17, q=17$ for $Z_{S,M2}$ and $p=17, q=17$ for $Z_{M2,M2}$. Fig. 6.13 shows the comparison between the frequency response of the macromodels and raw data. In Fig. 6.13, the real part of $Z_{M2,M2}(s)$ shows negative values around 680MHz, which violates the passivity condition. This example will therefore be used for enforcing passivity in the next chapter.

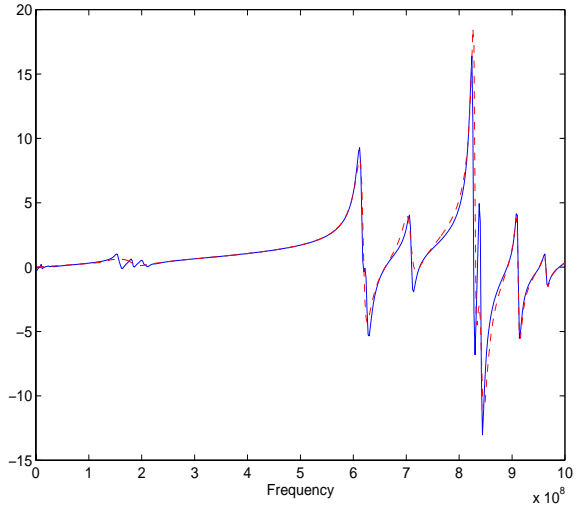


(a)

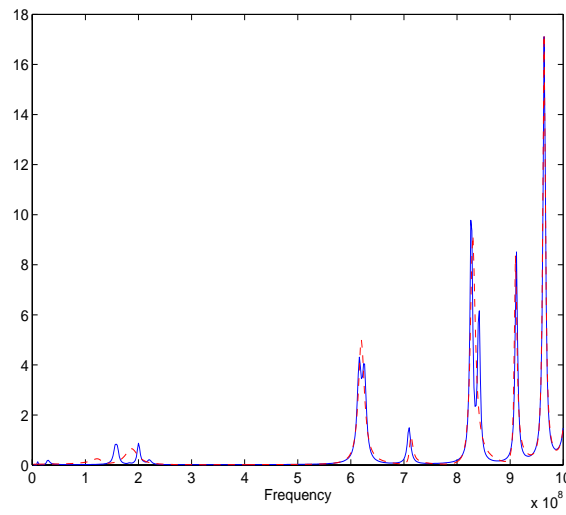
(b)



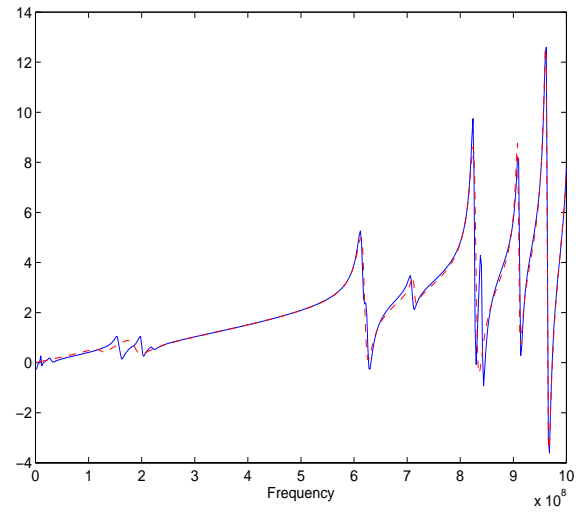
(c)



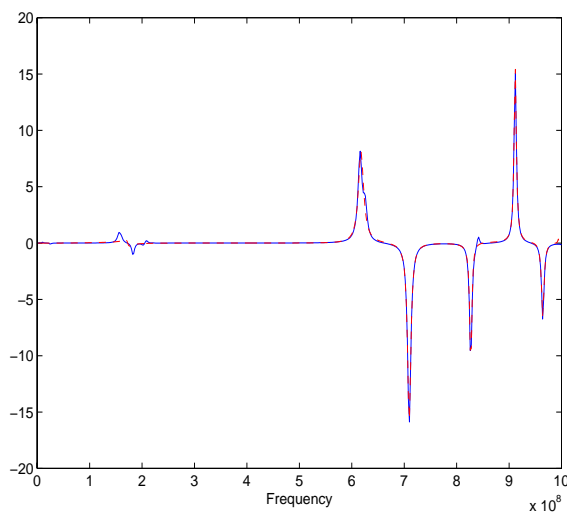
(d)



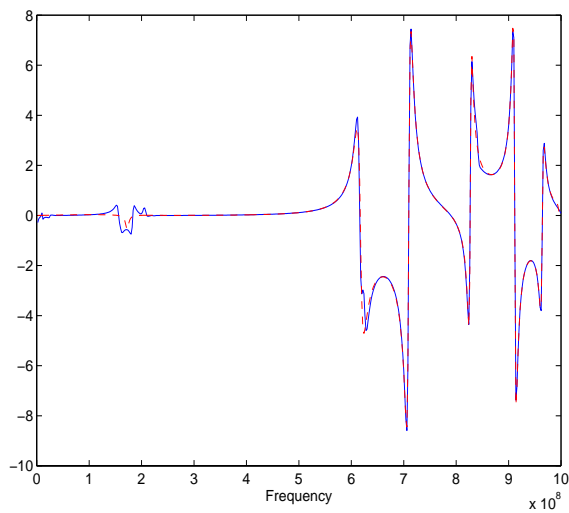
(e)



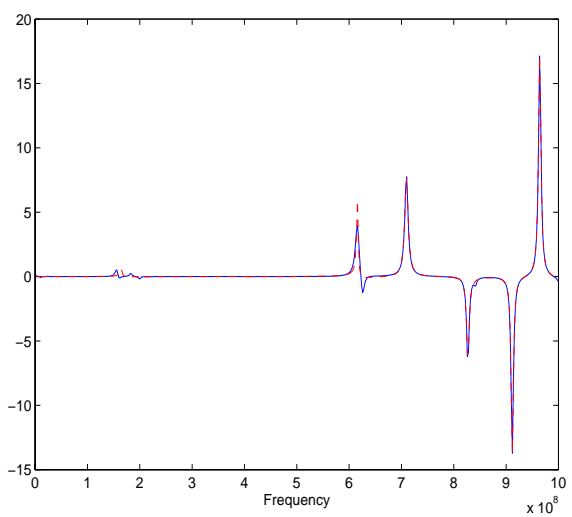
(f)



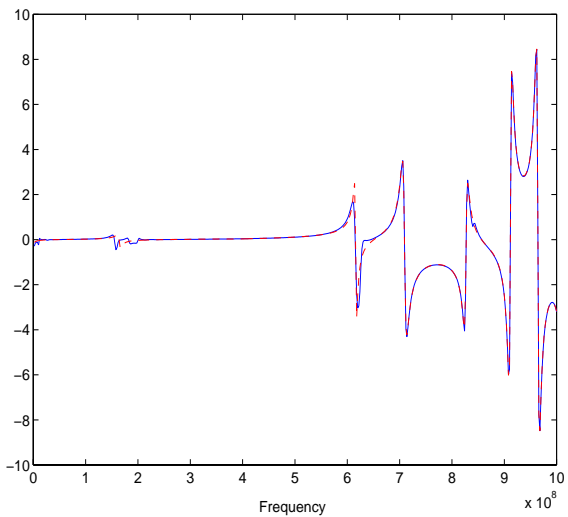
(g)



(h)



(i)



(j)

Fig. 6.13 (a) $\text{Real}(Z_{S,S})$, (b) $\text{Imag}(Z_{S,S})$, (c) $\text{real}(Z_{M1,M1})$, (d) $\text{Imag}(Z_{M1,M1})$, (e) $\text{Real}(Z_{M2,M2})$, (f) $\text{Imag}(Z_{M2,M2})$, (g) $\text{Real}(Z_{S,M1})$, (h) $\text{Imag}(Z_{S,M1})$, (i) $\text{Real}(Z_{S,M2})$, and (j) $\text{Imag}(Z_{S,M2})$: Raw data (solid) and Macromodel (dashed)

6.4 Summary

In this chapter, a macromodeling method for generating rational functions by solving an eigenvalue problem was discussed. The rational functions were used to construct equivalent circuits for transient simulations. S parameter-based equivalent circuits using macromodels were developed since S-parameter macromodels captured the response of highly resonant systems well. A 4 *mm*-long transmission line was modeled over 30 GHz using S-parameter rational functions with a 6th order rational functions. This model was formed to simulate faster than a distributed network model in SPICE. The plane pair which was modeled earlier using resonator circuits in Chapter 2 was modeled using S-parameter macromodels with two different orders. It was observed that a higher order model was desired for simulating accurate delays while a lower order model could be used if this was not important. A low order model is attractive since it reduces simulation time.

The rational functions generated using the macromodeling method discussed in this chapter are not always guaranteed to be passive, resulting in erroneous transient response. A split plane structure populated with a large number of decoupling capacitors was modeled using Z-parameters. The rational functions generated revealed the violation of the passivity condition at certain frequencies. In Chapter 7, a method for enforcing the passivity of macromodels is discussed.

CHAPTER 7

Enforcing Passivity for Macromodels

Power distribution networks are resonant structures which are passive circuits. Hence, they cannot create energy. In the last chapter, a method was discussed for generating rational functions based on the frequency response of power distribution networks. However, these rational functions are not guaranteed to be passive. In this chapter, methods have been developed to modify the rational functions such that they do not violate any passivity conditions.

7.1 Definition of Passivity

Some networks have the property of absorbing and/or storing energy. They can return their previously stored energy to an external network, but never more than the amount stored. Such networks are called *passive networks*.

Let $E(t)$ be the energy delivered to a network having a pair of terminals from an external source up to time t . The power delivered to the network is

$$p(t) = v(t)i(t) \tag{7.1}$$

where $v(t)$ and $i(t)$ are the load voltage and current at the terminals, respectively. Therefore, the network is defined to be passive if, for all t ,

$$E(t) = \int_{-\infty}^t v(x)i(x)dx \geq 0 \quad (7.2)$$

Similarly, a multiport network is passive if, for all t,

$$E(t) = \int_{-\infty}^t \mathbf{v}^T(x)\mathbf{i}(x)dx \geq 0 \quad (7.3)$$

where $\mathbf{v}(t) = [v_k(t)]$, $\mathbf{i}(t) = [i_k(t)]$ are the port voltages and currents, respectively.

7.2 Passivity Properties and Test for One-port Networks

Driving point functions (impedance/admittance) of passive one-port networks are positive real. By definition, a positive real rational function $F(s)$ where $s=\sigma+j\omega$ possesses the following properties [38],[39]:

- (a) $F(\sigma)$ is real
- (b) $\text{Re}[F(s)] \geq 0$ for all $\sigma \geq 0$

A given rational function with real coefficients can therefore be tested for positive realness through the above conditions.

Let $F(s)$ be a rational function represented as $N(s) / D(s)$ where $N(s)$ and $D(s)$ are polynomials with p -th and q -th orders, respectively. The necessary conditions for passivity of $F(s)$ are [31],[39],[40],[41]:

1. The coefficients in the polynomials $N(s)$ and $D(s)$ must be real and positive.
2. Complex poles and zeros must occur in complex conjugate pairs.
3. The real part of all poles and zeros must be negative or zero. In addition, if the real part is zero, then that pole or zero must be simple and the residue at such a pole must be real and positive.
4. The polynomials $N(s)$ and $D(s)$ should not have missing terms between the highest and lowest degree, unless all even or all odd terms are missing.
5. The degree of $N(s)$ and $D(s)$ may differ by either zero or one only.
6. $\text{Re}[F(j\omega)] \geq 0$ for $-\infty < \omega < \infty$

The conditions 1 to 5 can be checked from the generated rational functions. These conditions are necessary for rational functions to be passive at all frequencies but are not sufficient conditions. Condition 6 is obtained directly from the properties described in (a) and (b) which cannot be extracted directly from the coefficients of the rational function. Therefore, the rational functions which satisfy conditions 1 to 5 are first generated and then condition 6 is tested at all frequencies.

7.3 Passivity Properties and Test of Multiport Networks [38],[42],[43]

In the previous section, the important properties of driving point functions for passive one port networks were discussed. This section discusses the conditions for passive multiport networks, in particular, two port networks. The impedance and admittance matrices of

a passive multiport network are positive real matrices. As an example, consider a two-port impedance matrix:

$$Z(s) = \begin{bmatrix} z_{11}(s) & z_{12}(s) \\ z_{21}(s) & z_{22}(s) \end{bmatrix} \quad (7.4)$$

where $z_{ij}(s)$ is a real rational function. It is required that each driving point function, $z_{11}(s)$ and $z_{22}(s)$, in the matrix must still satisfy the passivity properties described in the previous section. In addition, the matrix must be also positive, semi-definite. Hence, for any arbitrary real vector X

$$X^T \cdot \text{Re}[Z(s)] \cdot X \geq 0 \quad (7.5)$$

where $X = [x_1 \ x_2]^T$ and x_1, x_2 are arbitrary real numbers. From the above inequality, an important and necessary condition for a passive, reciprocal two-port network can be derived. The residues corresponding to the poles on the $j\omega$ -axis must satisfy the following condition, called the *residue condition*, in addition to the conditions for one-port networks described in Sec. 7.2 [38],[39]:

$$k_{11}k_{22} - k_{12}^2 \geq 0 \quad (7.6)$$

where k_{ij} 's are the residues corresponding to the poles on the $j\omega$ -axis for a lossless network represented as

$$\begin{aligned}
h_{11}(s) &= \frac{k_{11}^{(o)}}{s} + \frac{2k_{11}^{(1)}s}{s^2 + \omega_1^2} + \dots + \frac{2k_{11}^{(m)}s}{s^2 + \omega_m^2} + k_{11}^{(\infty)}s \\
h_{12}(s) &= \frac{k_{12}^{(o)}}{s} + \frac{2k_{12}^{(1)}s}{s^2 + \omega_1^2} + \dots + \frac{2k_{12}^{(m)}s}{s^2 + \omega_m^2} + k_{12}^{(\infty)}s \\
h_{22}(s) &= \frac{k_{22}^{(o)}}{s} + \frac{2k_{22}^{(1)}s}{s^2 + \omega_1^2} + \dots + \frac{2k_{22}^{(m)}s}{s^2 + \omega_m^2} + k_{22}^{(\infty)}s
\end{aligned}$$

where $h(s)$ can be impedance or admittance. For lossy networks, complex poles and residues occur in complex conjugate pairs. The residue condition in (7.6) describes the test condition for lossless networks.

By definition, positive realness is linked with the real part of a function. Let the real part of $Z(s)$ in (7.3) be

$$\operatorname{Re}(Z(s)) = \begin{bmatrix} r_{11} & r_{12} \\ r_{21} & r_{22} \end{bmatrix} \quad (7.7)$$

Similar to the condition for residues in (7.6), it follows for $\operatorname{Re} s \geq 0$ that [38]

$$r_{11} \geq 0, r_{22} \geq 0 \quad (7.8)$$

and

$$r_{11}r_{22} - r_{12}^2 \geq 0 \quad (7.9)$$

for reciprocal two-port networks which can be extended to multi-port networks. The above conditions apply to admittance matrices in a similar way. The condition in (7.8) has already been explored in the previous section since z_{11} and z_{22} are driving point functions and hence positive real. The condition in (7.9) is called as the *real part condition*. This real part condition alone is a sufficient condition for Z to be a positive real matrix. The stronger statement for passivity is that *the necessary and sufficient conditions for a real symmetric matrix to be nonnegative definite is that all its eigenvalues have to be positive* [42]. Therefore, this condition along with the real part condition in (7.9) will be applied in this chapter to check the passivity of rational functions generated using the macromodeling technique described in the last chapter.

7.4 Passivity Enforcement Algorithm

7.4.1 One-port Network

The rational functions, called macromodels, are first generated with real coefficients which provide a good fit to the raw data. The first step of passivity preservation for driving point functions is to check the new model against each condition of 1 through 5 in Sec. 7.2. If any of those conditions is violated, the model is discarded. Next, the response of the macromodel is computed over the extended frequency range beyond the maximum frequency of interest. The condition 6 is tested for the real part of the macromodel at each frequency over the extended frequency range. In most cases, a well-fitting model satisfying all the conditions 1 to 6 can be found. However, a small error in the models for highly resonant systems which are generated satisfying conditions 1 to 5 can cause the violation of condition 6. In these models, the real part can be slightly negative at the frequencies

where the real part of the input data is close to zero, which violates the passivity condition. These models can be modified through compensation by using the method described in [43].

In this section, the macromodels generated for the split plane structure in Sec. 6.3.3 are considered for passivity compensation. $Z_{M1,M1}(s)$ was generated as in (7.10) and its poles and zeros are shown in Table 7.1. The model was generated based on 1GHz data and the frequency response of the model extended up to 3GHz is shown in Fig. 7.1. This is necessary since the violation of the passivity condition may occur just beyond the maximum frequency used to generate the rational function. As shown in (7.10) and Table 7.1, the model was created with all positive coefficients with no missing term and with all negative real parts of poles and zeros satisfying the conditions 1 to 5 in Table 7.1. However, the model still reveals a negative region in the real part around 680MHz as shown in Fig. 6.13 and Fig. 7.1.

$$Z_{M1, M1}(s) = \frac{a_0 + a_1s + \dots + a_{19}s^{19}}{b_0 + b_1s + \dots + b_{20}s^{20}} \quad (7.10)$$

where

a0 = 4.1453e-04	b0 = 1.8706e-02
a1 = 8.2930e-12	b1 = 8.6909e-12
a2 = 4.1350e-21	b2 = 4.6472e-20
a3 = 1.9169e-29	b3 = 1.3299e-29
a4 = 4.8028e-39	b4 = 3.3051e-38
a5 = 1.2042e-47	b5 = 4.9783e-48
a6 = 1.5557e-57	b6 = 7.8542e-57
a7 = 2.5666e-66	b7 = 8.1862e-67

$a_8 = 2.2109e-76$
 $a_9 = 2.7396e-85$
 $a_{10} = 1.6773e-95$
 $a_{11} = 1.6846e-104$
 $a_{12} = 7.3265e-115$
 $a_{13} = 6.2580e-124$
 $a_{14} = 1.8517e-134$
 $a_{15} = 1.3898e-143$
 $a_{16} = 2.5196e-154$
 $a_{17} = 1.7009e-163$
 $a_{18} = 1.4296e-174$
 $a_{19} = 8.8319e-184$

$b_8 = 9.4021e-76$
 $b_9 = 7.3291e-86$
 $b_{10} = 6.5855e-95$
 $b_{11} = 3.9072e-105$
 $b_{12} = 2.8639e-114$
 $b_{13} = 1.2756e-124$
 $b_{14} = 7.8141e-134$
 $b_{15} = 2.4992e-144$
 $b_{16} = 1.2944e-153$
 $b_{17} = 2.6921e-164$
 $b_{18} = 1.1786e-173$
 $b_{19} = 1.2211e-184$
 $b_{20} = 4.4529e-194$

Table 7.1: Poles and zeros of the model in (7.10)

Poles	Zeros
$p_1 = -5.4608e+08 + 8.9852e+09i$	$z_1 = -1.7472e+07 + 6.2105e+09i$
$p_2 = -5.4608e+08 - 8.9852e+09i$	$z_2 = -1.7472e+07 - 6.2105e+09i$
$p_3 = -2.2159e+07 + 6.0600e+09i$	$z_3 = -1.7490e+07 + 5.9720e+09i$
$p_4 = -2.2159e+07 - 6.0600e+09i$	$z_4 = -1.7490e+07 - 5.9720e+09i$
$p_5 = -2.1336e+07 + 5.7288e+09i$	$z_5 = -1.5856e+07 + 5.5999e+09i$
$p_6 = -2.1336e+07 - 5.7288e+09i$	$z_6 = -1.5856e+07 - 5.5999e+09i$
$p_7 = -3.9754e+07 + 5.2957e+09i$	$z_7 = -3.8645e+07 + 5.2496e+09i$
$p_8 = -3.9754e+07 - 5.2957e+09i$	$z_8 = -3.8645e+07 - 5.2496e+09i$
$p_9 = -2.1004e+07 + 5.2120e+09i$	$z_9 = -4.7908e+07 + 4.5915e+09i$
$p_{10} = -2.1004e+07 - 5.2120e+09i$	$z_{10} = -4.7908e+07 - 4.5915e+09i$
$p_{11} = -4.1800e+08 + 4.3608e+09i$	$z_{11} = -4.6572e+08 + 4.2025e+09i$
$p_{12} = -4.1800e+08 - 4.3608e+09i$	$z_{12} = -4.6572e+08 - 4.2025e+09i$
$p_{13} = -5.7998e+07 + 4.4476e+09i$	$z_{13} = -1.4880e+07 + 4.1532e+09i$
$p_{14} = -5.7998e+07 - 4.4476e+09i$	$z_{14} = -1.4880e+07 - 4.1532e+09i$
$p_{15} = -4.4490e+07 + 3.8859e+09i$	$z_{15} = -8.7029e+07 + 1.2910e+09i$
$p_{16} = -4.4490e+07 - 3.8859e+09i$	$z_{16} = -8.7029e+07 - 1.2910e+09i$
$p_{17} = -1.2704e+08 + 1.1474e+09i$	$z_{17} = -7.8835e+07 + 8.3972e+08i$
$p_{18} = -1.2704e+08 - 1.1474e+09i$	$z_{18} = -7.8835e+07 - 8.3972e+08i$
$p_{19} = -7.3240e+07 + 8.5641e+08i$	$z_{19} = -5.0979e+07$
$p_{20} = -7.3240e+07 - 8.5641e+08i$	

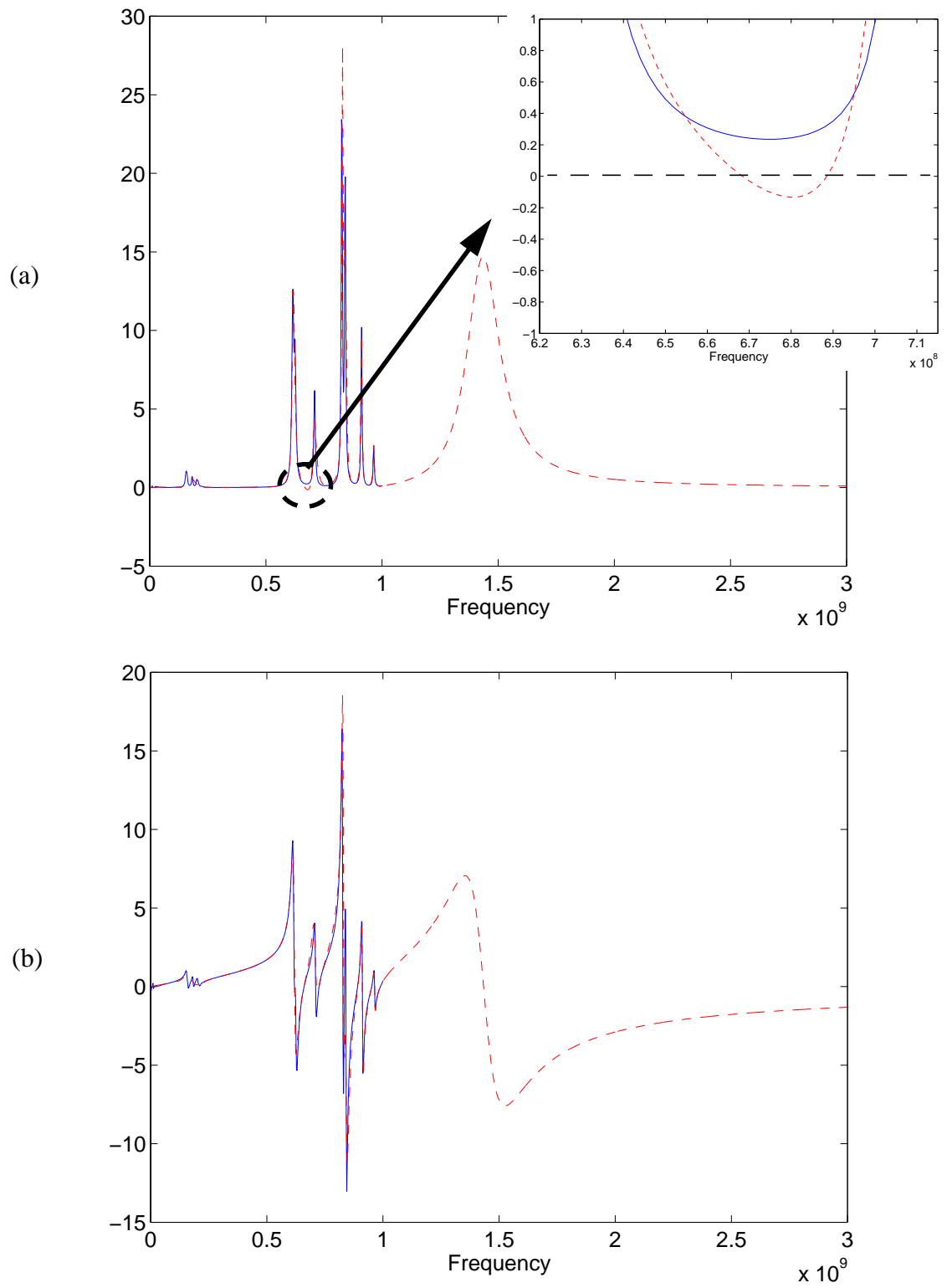


Fig. 7.1 Macromodeling result based on 1 GHz data for $Z_{M1, M1}$ with $p=19$ and $q=20$: (a) real part and (b) imaginary part. Macromodel(dashed) and raw data(solid)

To compensate the negative response of the model around 680MHz, a rational function with a conjugate pole pair over the negative real region was constructed and added to the model [43]. Let $U(s)$ be represented by the pole, $p_{1,2} = -\alpha \pm j\beta$ and residue

$$k_{1,2} = d_1 \pm jd_2 :$$

$$\begin{aligned} U(s) &= \frac{d_1 + jd_2}{s + \alpha - j\beta} + \frac{d_1 - jd_2}{s + \alpha + j\beta} \\ &= \frac{2d_1s + 2(d_1\alpha - d_2\beta)}{s^2 + 2\alpha s + \alpha^2 + \beta^2} \end{aligned} \quad (7.11)$$

$p_{1,2}$ and $k_{1,2}$ are determined such that $U(s)$ is guaranteed to be passive, for which the real part of $U(s)$ is always positive over the extended range of frequency while the response of $U(s)$ does not affect the overall response at other frequencies. Equation (7.11) gives the restrictions for $U(s)$ to be passive:

1. d_1 and α must be positive.
2. $d_1\alpha \geq d_2\beta$

The negative real region of the model is redrawn in Fig. 7.2. The frequency of the pole β is determined by the frequency at which the negative maximum occurs as shown in Fig. 7.2 and d_1 , d_2 and α are determined such that the response of $U(s)$ offsets all negative values at those frequencies.

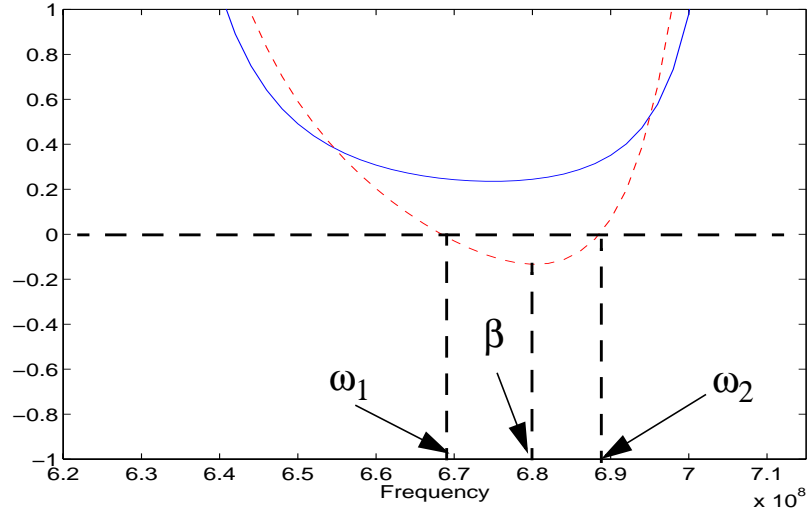


Fig. 7.2 Negative real region of the model. β is determined at the frequency where the maximum negative value occurs

The real part response of $U(s)$ needs to be greater than the absolute values of the real part of the model at the frequencies between ω_1 and ω_2 to guarantee the positiveness of the updated model. This is done by making the real part response of $U(s)$ at its pole slightly greater than the maximum negative value of the model real part at the same frequency, and also by setting the bandwidth of the response of $U(s)$ to $\omega_2 - \omega_1$. Since the bandwidth of $U(s)$ is 2α from (7.11), α is determined as [41]

$$\alpha = \frac{\omega_2 - \omega_1}{2} \quad (7.12)$$

Practically, α is chosen to be slightly larger than determined in (7.12) such that the bandwidth of $U(s)$ covers all the negative real region of the macromodel.

The real part response of $U(s)$ is expressed as

$$Re[U(\omega)] = \frac{2(d_1\alpha - d_2\beta)(\alpha^2 + \beta^2) + 2(d_1\alpha + d_2\beta)\omega^2}{(\alpha^2 + \beta^2 - \omega^2)^2 + (2\alpha\omega)^2} \quad (7.13)$$

Let the maximum negative real part value of the model be r_{max} , that is, $r_{max} = Real(Z_{M1,M1}(j\beta))$. Then it follows that

$$Re[U(\beta)] = \frac{2(d_1\alpha - d_2\beta)\alpha^2 + 4d_1\alpha\beta^2}{\alpha^4 + 4\alpha^2\beta^2} \geq |r_{max}| \quad (7.14)$$

Since α and β have been already determined, d_1 and d_2 can be determined considering the parameter condition 2 mentioned previously and (7.14). To make the problem easier, d_2 can be set to 0 and only d_1 needs to be determined from (7.14).

$$d_1 = k|r_{max}| \frac{\alpha^3 + 4\alpha\beta^2}{2\alpha^2 + 4\beta^2} \quad (7.15)$$

where $k = 1 \sim 2$.

To compensate the negative real part of the model in (7.10), $U(s)$ is constructed with $\alpha=6.9115e+07$, $\beta=4.2726e+09$ and $d_1=9.9318e+06$ using the above conditions and the response of $U(s)$ is shown in Fig. 7.3. Then the macromodel for $Z_{M1,M1}(s)$ is updated as

$$\begin{aligned} \tilde{Z}_{M1,M1}(s) &= Z_{M1,M1}(s) + U(s) \\ &= \frac{\mathbf{a}_0 + \mathbf{a}_1s + \dots + \mathbf{a}_{21}s^{21}}{\mathbf{b}_0 + \mathbf{b}_1s + \dots + \mathbf{b}_{22}s^{22}} \end{aligned} \quad (7.16)$$

where

a0 = 7.5948e+15	b0 = 3.4157e+17
a1 = 1.5187e+08	b1 = 1.6128e+08
a2 = 7.7300e-02	b2 = 8.6846e-01
a3 = 3.5982e-10	b3 = 2.5795e-10
a4 = 9.4792e-20	b4 = 6.5180e-19
a5 = 2.4038e-28	b5 = 1.0877e-28
a6 = 3.4984e-38	b6 = 1.7715e-37
a7 = 5.9279e-47	b7 = 2.1012e-47
a8 = 5.9651e-57	b8 = 2.5135e-56
a9 = 7.6183e-66	b9 = 2.2868e-66
a10 = 5.6678e-76	b10 = 2.1528e-75
a11 = 5.8519e-85	b11 = 1.5374e-85
a12 = 3.2561e-95	b12 = 1.1869e-94
a13 = 2.8431e-104	b13 = 6.6322e-105
a14 = 1.1599e-114	b14 = 4.3083e-114
a15 = 8.8369e-124	b15 = 1.8399e-124
a16 = 2.5091e-134	b16 = 1.0212e-133
a17 = 1.7065e-143	b17 = 3.1697e-144
a18 = 3.0213e-154	b18 = 1.5133e-153
a19 = 1.8665e-163	b19 = 3.0780e-164
a20 = 1.5542e-174	b20 = 1.2616e-173
a21 = 8.8408e-184	b21 = 1.2826e-184
	b22 = 4.4529e-194

The updated macromodel is compared with the original data in Fig. 7.4.

The following procedure shows the steps to obtain a one-port macromodel with its passivity preserved:

1. Generate the macromodel which satisfies the conditions 1 to 5 in Sec. 7.2.
2. Compute the response of the macromodel over the extended frequency range and test the real part of the model for condition 6.
3. If the passivity is violated in 2, construct $U(s)$ in (7.11) as follows:
 - 3.1. Determine β at the frequency where the maximum negative real value occurs.

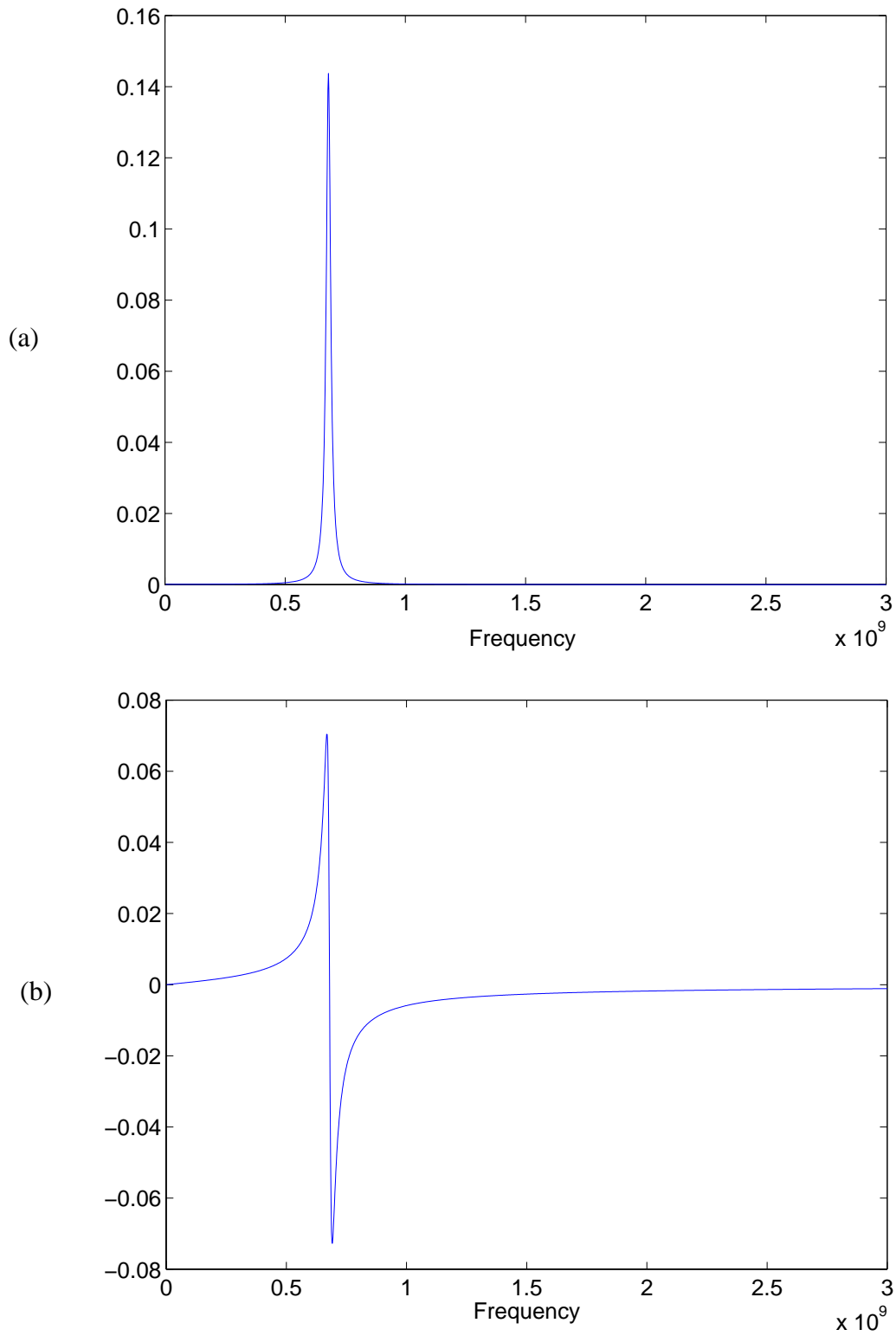


Fig. 7.3 Frequency response of $U(s)$: (a) real part and (b) imaginary part

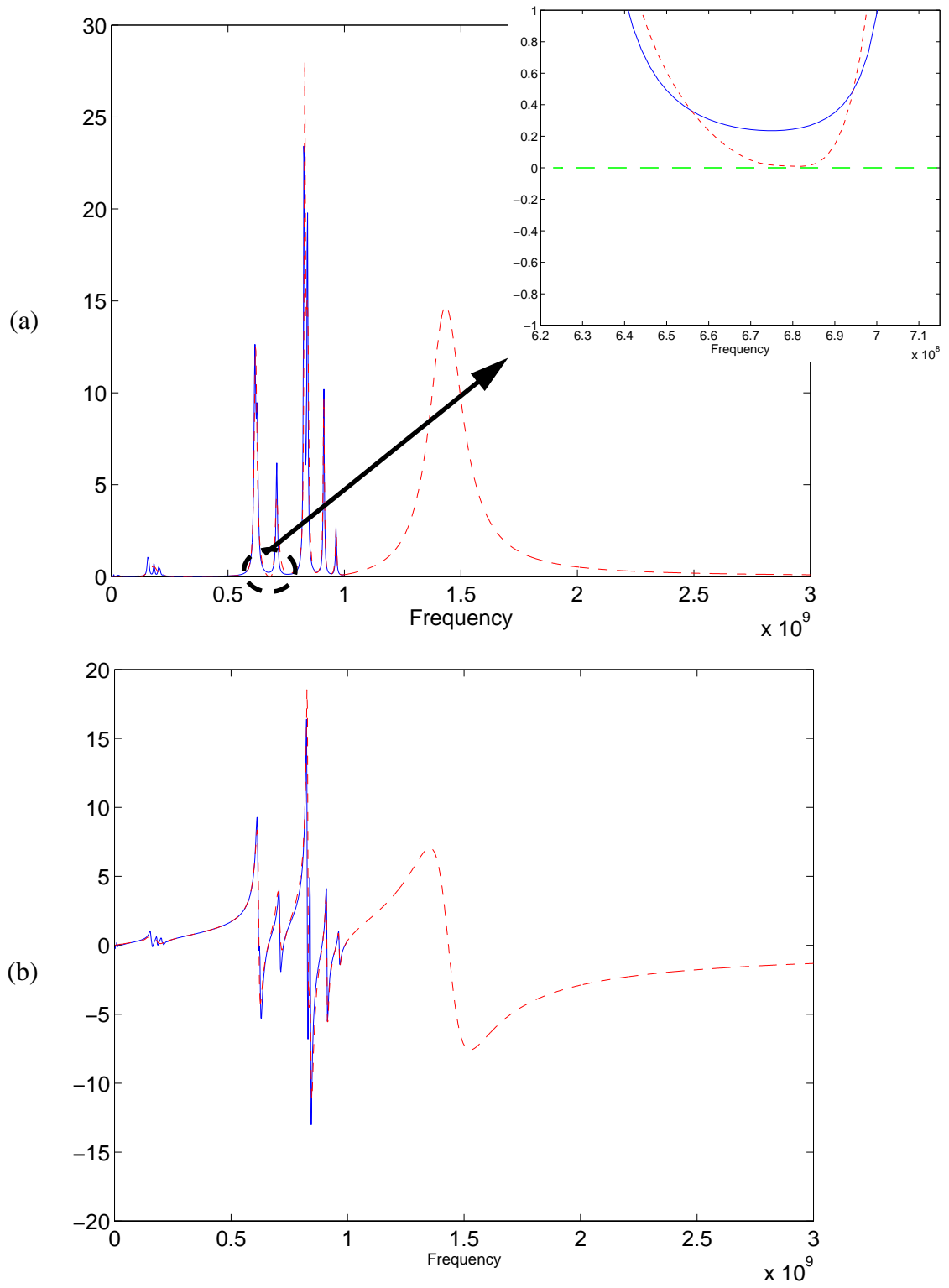


Fig. 7.4 New model of $Z_{MI,MI}$ with passivity compensated: (a) real part and (b) imaginary part. Macromodel(dashed) and raw data(solid)

3.2 Determine α as in (7.12) so that the bandwidth of $U(s)$ covers the negative real region of the macromodel.

3.3 Determine d_1 as in (7.15).

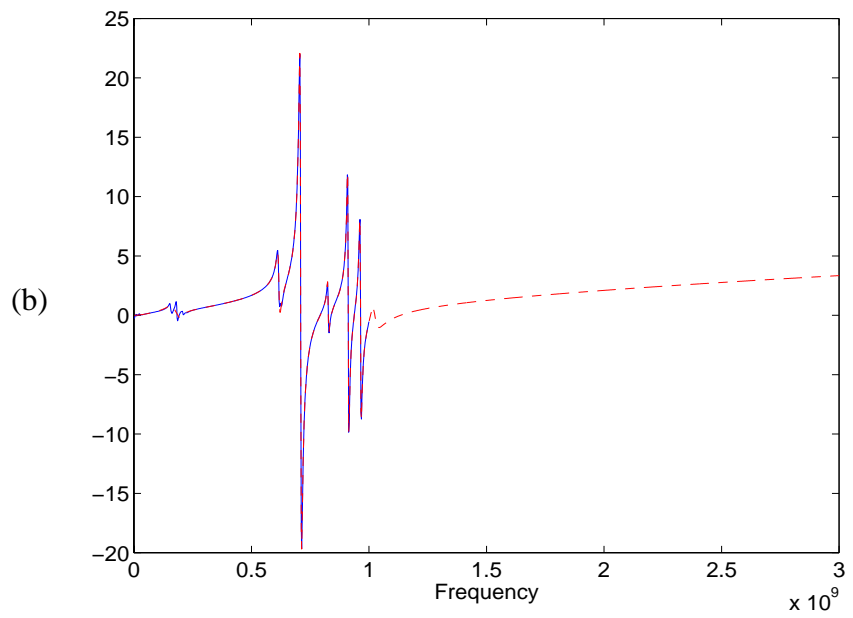
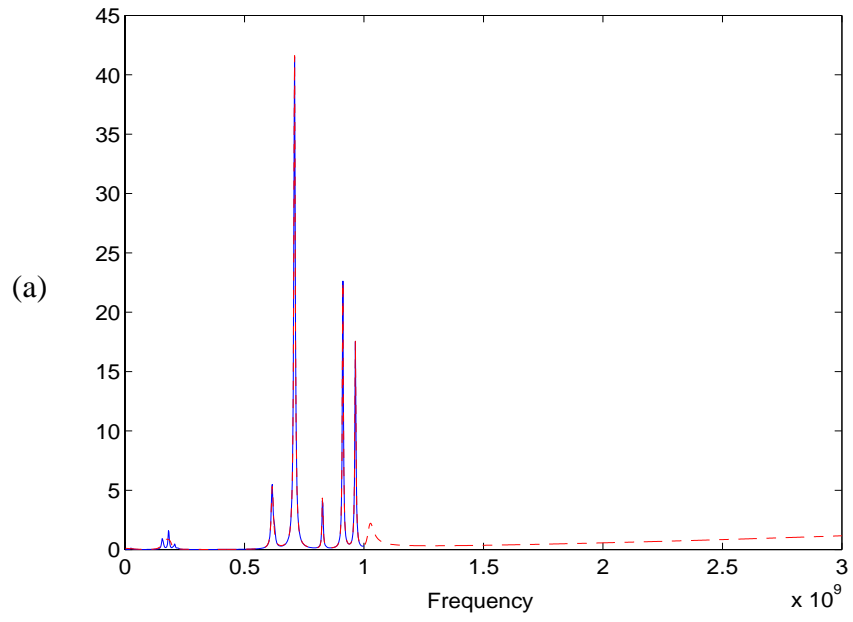
4. Update the macromodel as in (7.16)

7.4.2 Two-port network

Each driving point function needs to be modeled first such that the passivity is guaranteed for one-port, as described in the previous section. The only condition that needs to be enforced in modeling the trans-impedance/admittance functions are stable poles in the generated transfer functions. The real part conditions or eigenvalue conditions for the real part of the two-port matrix described in (7.3) through (7.9) are then tested at each frequency to ensure passivity of the solution.

To illustrate the procedure, consider two ports in Fig. 6.11, say source port ‘S’ and measurement port ‘M1’. A passive macromodel for $Z_{M1,M1}(=Z_{22})$ was developed in the previous section using pole compensation. The macromodels for $Z_{S,S}(=Z_{11})$ and $Z_{S,M1}(=Z_{12})$ have also been generated as shown in Fig. 7.5 with the passivity of Z_{11} guaranteed with stable poles for Z_{12} . All models were generated based on data up to 1 GHz and the responses were computed over the extended frequency range up to 3 GHz to check the passivity of the model beyond the maximum frequency of interest. In addition the passivity of the models were tested within the frequency range of interest.

Although the driving point functions Z_{11} and Z_{22} were generated to be passive and Z_{12} was generated with all stable poles, the real part condition or eigenvalue condition for the two-port circuit was violated at the frequencies shown in Table 7.2.



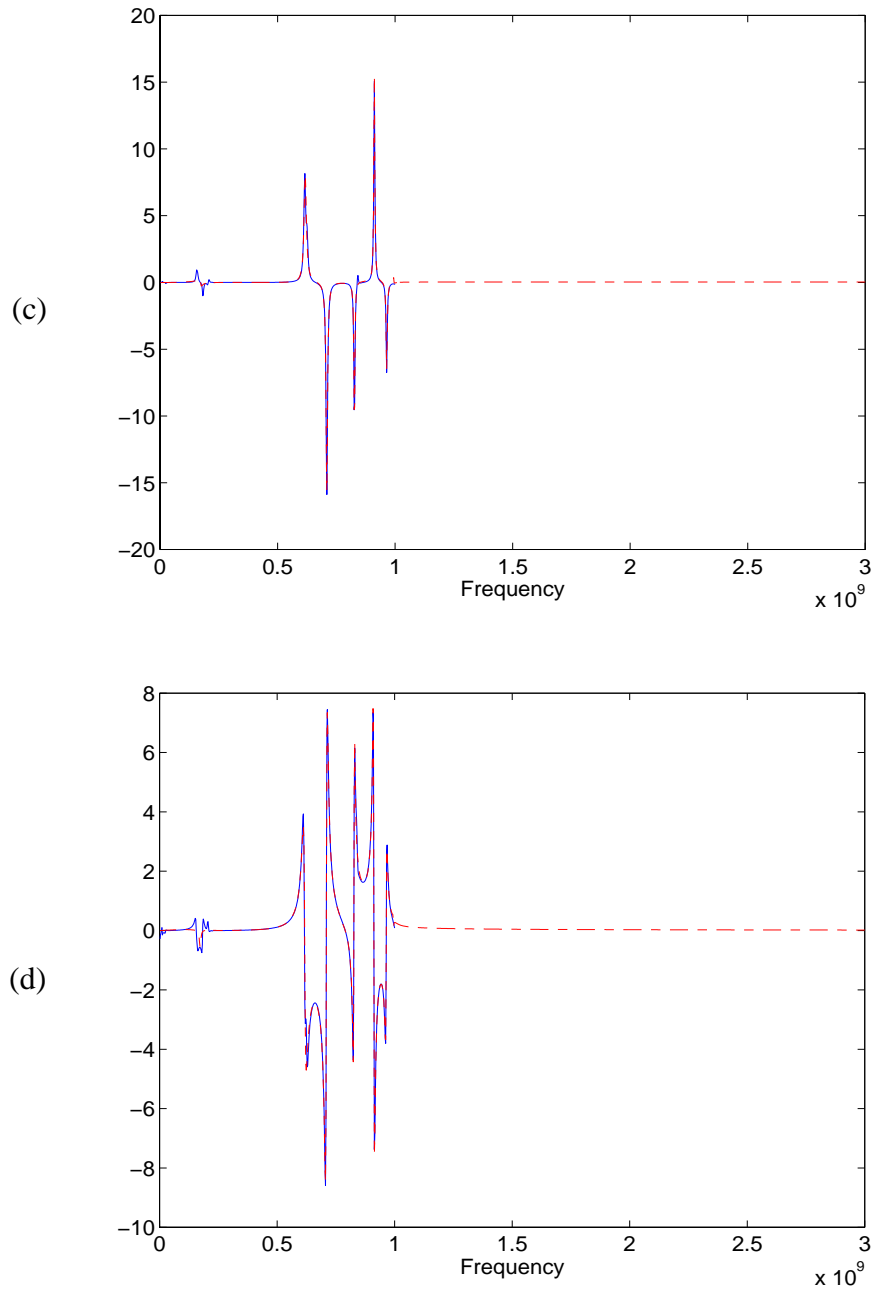


Fig. 7.5 Macromodel (dashed) and raw data (solid): (a) $\text{real}(Z_{11})$, (b) $\text{imag}(Z_{11})$, (c) $\text{real}(Z_{12})$, and (d) $\text{imag}(Z_{12})$

Table 7.2: Frequency with passivity violation of the two-port model

Region	Frequencies with passivity violation
1	96 MHz - 138MHz
2	616MHz - 620MHz
3	676MHz - 692MHz
4	708MHz - 712MHz
5	822MHz - 828MHz
6	912MHz
7	994MHz

To ensure passivity, each region was compensated with a conjugate pole response $U_i(s)$ using the algorithm described for the one-port case. Then $U(s)$ was constructed as the sum of the responses over all regions:

$$U(s) = \sum_{i=1}^7 U_i(s) \quad (7.17)$$

Consider the compensation function $U_1(s)$ for region 1. The parameter β was found at the frequency where the maximum negative eigenvalue occurred in region 1 [37]. The parameter α was determined such that $(\omega_2 - \omega_1)$ in (7.12) covers the frequency region where the eigenvalues of the matrix are negative. $U_1(s)$ was constructed such that the real part of $U_1(s)$ offsets any negative response of $X^T Re[Z]X$ in region 1 where $X=[x_1 \ x_2]$ is an arbitrary real vector. Therefore, (7.14) was modified to find d_1 such that

$$X^T Re \begin{bmatrix} U_i(\beta) & 0 \\ 0 & U_i(\beta) \end{bmatrix} X = (x_1^2 + x_2^2) \frac{2(d_1\alpha - d_2\beta)\alpha^2 + 4d_1\alpha\beta^2}{\alpha^4 + 4\alpha^2\beta^2} \geq R_{max} \quad (7.18)$$

where $R_{max} = \text{Max}\{X | -X^T Re[Z(j\beta)]X\}$.

Let $Re[Z(j\beta)]$ be

$$Re[Z(j\beta)] = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \quad (7.19)$$

Then,

$$\begin{aligned} X^T Re[Z(j\beta)]X &= a_{11}x_1^2 + a_{12}x_1x_2 + a_{21}x_1x_2 + a_{22}x_2^2 \\ &= a_{11}x_1^2 + 2a_{12}x_1x_2 + a_{22}x_2^2 \end{aligned} \quad (7.20)$$

By solving $a_{11}x_1^2 + 2a_{12}x_1x_2 + a_{22}x_2^2 = 0$ for x_1 , a set of $X_M = [x_{1M} \ x_{2M}]$ causes $X^T Re[Z(j\beta)]X$ to become a negative maximum is found. This leads to the relation:

$$x_{1M} = -\frac{a_{12}}{a_{11}}x_{2M} \quad (7.21)$$

which results in R_{max} to be

$$R_{max} = -X_M^T Re[Z]X_M = -(a_{11}x_{1M}^2 + 2a_{12}x_{1M}x_{2M} + a_{22}x_{2M}^2) \quad (7.22)$$

From (7.18), d_1 is determined as

$$d_1 = kR_{max} \frac{\alpha^3 + 4\alpha\beta^2}{(2\alpha^2 + 4\beta^2)(x_1^2 + x_2^2)} \quad (7.23)$$

All $U_i(s)$'s are determined in a similar manner for the seven regions where the passivity was violated. Fig. 7.6 shows the response of $U(s)$ which is the sum of $U_i(s)|_{i=1,\dots,7}$.

Finally, the two-port impedance matrix was updated as in (7.24):

$$\begin{aligned} \tilde{Z}(s) &= Z(s) + \begin{bmatrix} U(s) & 0 \\ 0 & U(s) \end{bmatrix} \\ &= \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} + \begin{bmatrix} U(s) & 0 \\ 0 & U(s) \end{bmatrix} \end{aligned} \quad (7.24)$$

The passivity-compensated model is compared with the input data in Fig. 7.7, showing negligible error in the interpolated response.

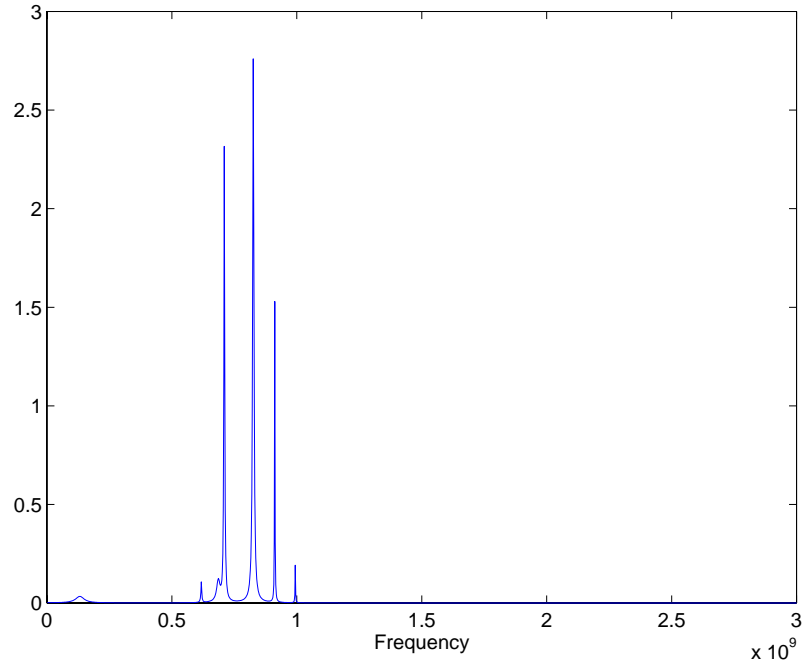


Fig. 7.6 Compensation function $U(s)$ of the two-port(S,M1) system

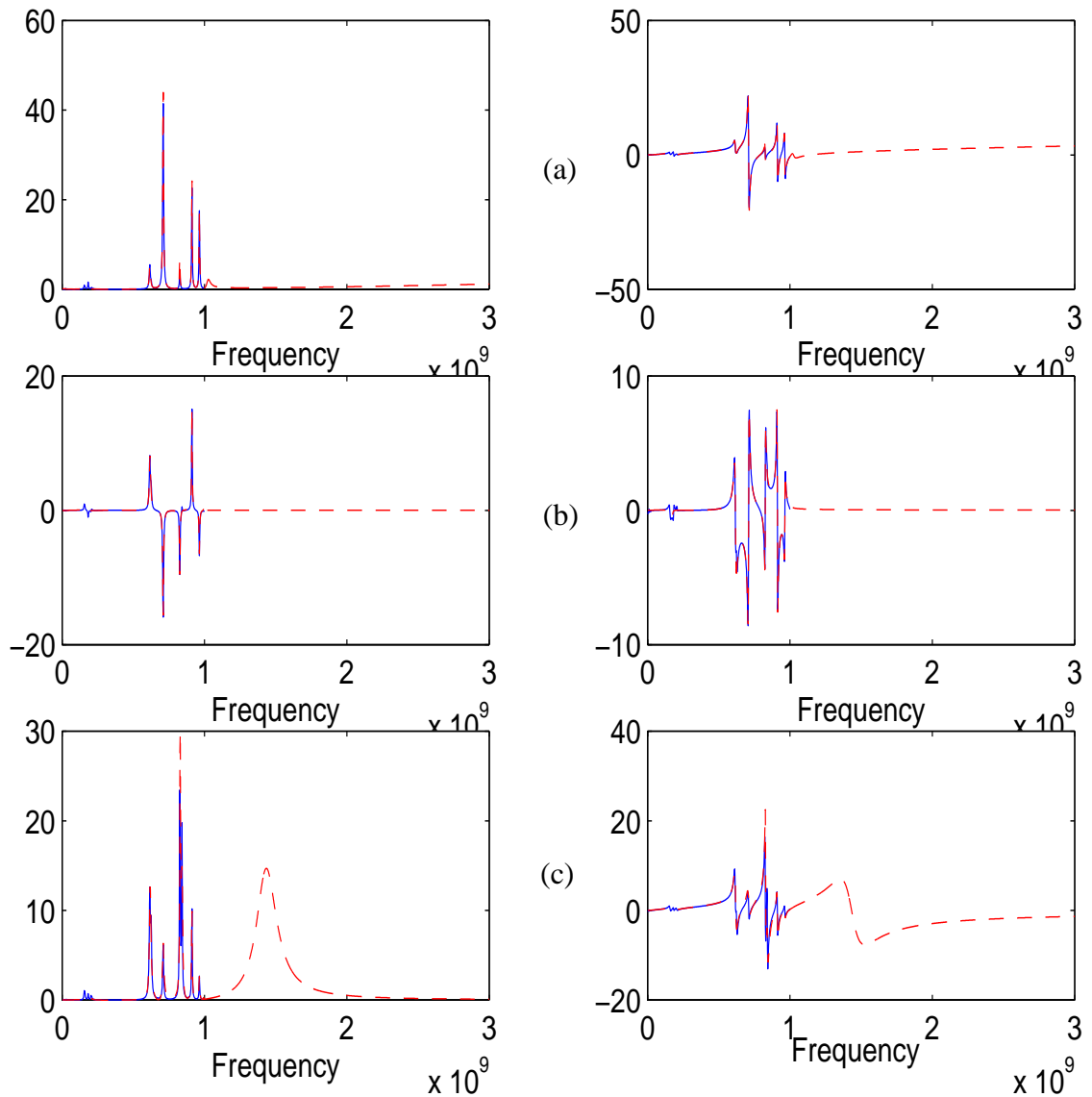


Fig. 7.7 Passivity-compensated macromodel(dashed) and raw data(solid): (a) Z_{11} real and imaginary parts, (b) Z_{12} real and imaginary parts and (c) Z_{22} real and imaginary parts

As another example, the two-port system with source port ‘S’ and ‘M2’ in Fig. 6.11 was modeled. First, the rational functions for each driving point impedance function $Z_{S,S}$ and $Z_{M2,M2}$ were generated such that all the passivity conditions were satisfied, as in the

previous example. The trans-impedance $Z_{S,M2}$ was next generated with stable poles. The models were generated using raw data up to 1 GHz. The passivity condition for the eigenvalues of the two-port impedance matrix was then tested at each frequency up to 3 GHz. The passivity condition was violated in 9 regions as shown in Table 7.3. Figs 7.8 and 7.9 show the compensation function $U(s)$ and the macromodeling result with the passivity compensated, respectively. In Fig. 9, the interpolated response and the raw data show good agreement.

Table 7.3: Frequency regions with passivity violation of the two-port model

Region	Frequencies with passivity violation
1	1MHz
2	81MHz - 83MHz
3	308MHz
4	346MHz - 356MHz
5	411MHz - 414MHz
6	448MHz - 450MHz
7	456MHz - 457MHz
8	486MHz
9	503MHz - 509MHz

Based on the two examples, the procedure for obtaining a passive model for two ports is as follows:

1. Obtain the macromodels for the driving point functions as described in 7.4.1.
2. Obtain the macromodels for trans-impedance/admittance functions with stable poles.
3. Compute the response of the macromodels over the extended frequency range.

4. Find the frequency regions where the real part eigenvalue conditions of the two port matrix in (7.9) violate passivity.
5. Determine a compensation function $U_i(s)$ for each negative real region:
 - 5.1 Determine β at the frequency where the maximum negative eigenvalue of the real part matrix occurs in the i -th region.
 - 5.2 Determine α such that the bandwidth of $U_i(s)$, $(\omega_2 - \omega_1)$, covers the negative eigenvalue region of the real part matrix.
 - 5.3 Determine d_1 as in (7.23).
6. Determine the compensation function $U(s)$ for the entire frequency range as in (7.17).
7. Update the impedance matrix as in (7.24).

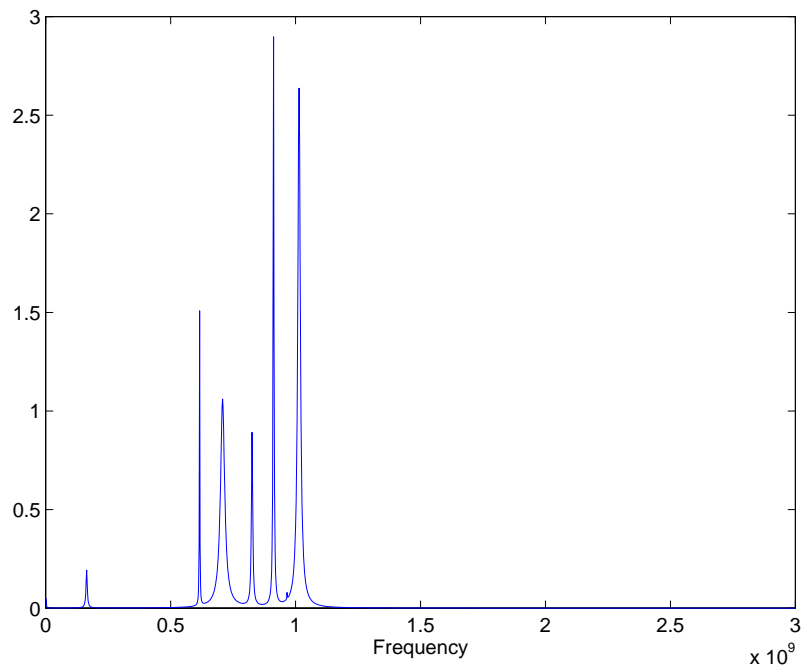


Fig. 7.8 Compensation function $U(s)$ of the two-port (S,M2) system

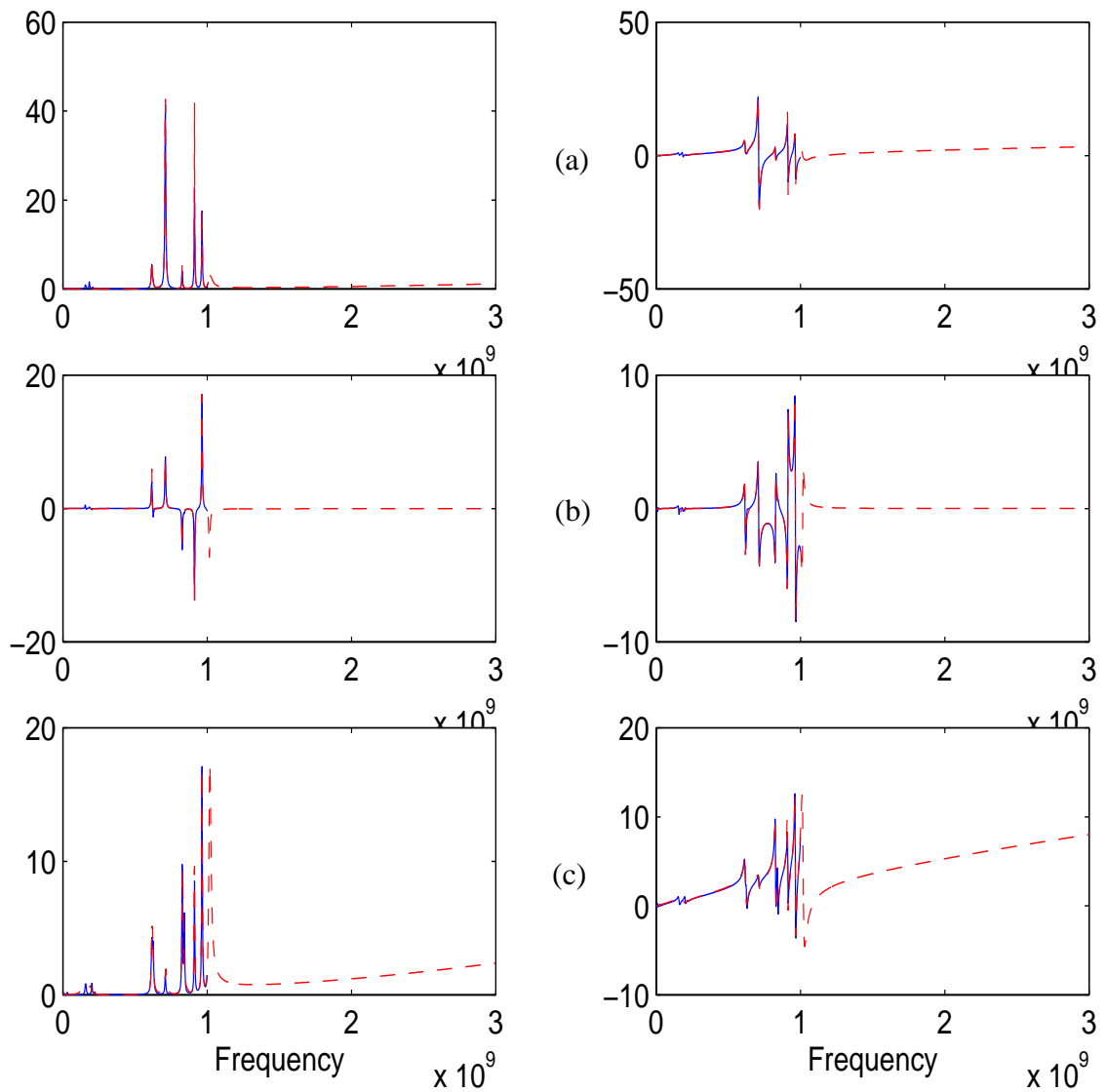


Fig. 7.9 Passivity-compensated macromodel (dashed) and raw data (solid): (a) Z_{11} real and imaginary parts, (b) Z_{12} real and imaginary parts and (c) Z_{22} real and imaginary parts

7.5 Summary

In this chapter, methods have been developed to modify the rational functions generated in Chapter 6 such that the passivity of the models is preserved. The algorithms

enforcing the passivity for one-port and two-port systems have been demonstrated for a split plane structure.

CHAPTER 8

Simulation of Switching Noise

As discussed in Chapter 1, simultaneous switching noise for high speed digital systems needs to be analyzed and predicted through accurate modeling of the power distribution network. In the previous chapters, methods for modeling planes in power distribution networks containing decoupling capacitors have been discussed. In this chapter, these methods have been applied for the simulation of switching noise for various test cases. Noise effects due to core switching have been analyzed and the effects of decoupling capacitors on noise reduction have been examined with placement on the board, package and on chip.

8.1 Switching Noise in a Mixed Signal Module

In this section, a computer module is simulated to analyze ground bounce and the effect of decoupling capacitors using the methods developed in the earlier sections. Consider a computer module as shown in Fig. 8.1 consisting of a plane pair of size $32mm \times 32mm$ separated by a $150\mu m$ thick insulator with dielectric constant of 9.5. The resistivity of the metallization is $10.5\mu\Omega\text{-}cm$. The voltage source with $V_{dd} = 3.3$ volts is injected at location $(0.5cm, 2.7cm)$ and a digital chip and an analog filter are located at locations $(1cm, 1cm)$ and $(2.5cm, 2.5cm)$, respectively. C1 through C4 indicate the positions for attaching

decoupling capacitors on the module. Each decoupling capacitor has a capacitance of 2nF , series equivalent inductance of 60pH and series equivalent resistance of $50\text{m}\Omega$.

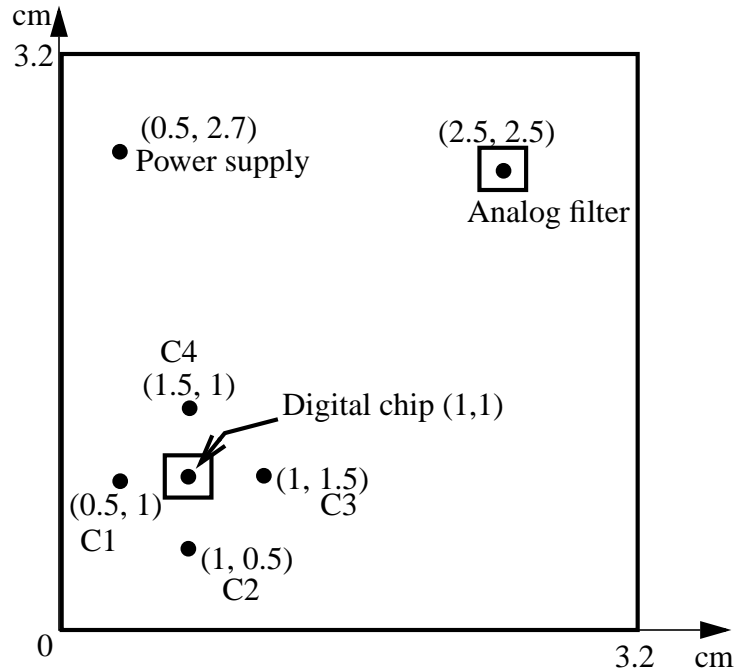


Fig. 8.1 Mixed signal module with a digital chip, analog filter and decoupling capacitors

A current source as shown in Fig. 8.2 is used to emulate a fast driver with a current slew rate of 60mA/ns in the digital chip. The effect of decoupling capacitors for noise reduction is observed in the trans-impedance and transmission coefficient in Fig. 8.3, which were computed using (5.4). It can be seen that the trans-impedance and transmission coefficient between the ports for the digital chip and the analog filter decrease by a large amount when the decoupling capacitors are connected to the planes, which causes better noise isolation between the digital chip and the analog filter. Fig. 8.4a shows the transient response on the plane in the vicinity of the analog filter. A noise voltage of $\pm 30\text{mV}$ is observed with one driver switching when the planes do not contain decoupling

capacitors. This noise is reduced $\pm 2\text{mV}$ when the decoupling capacitors are attached to the planes, as shown in Fig. 8.4b. This is because the decoupling capacitors act as a large reservoir and supply the necessary current to the switching driver, thus reducing the oscillation on the power supply.

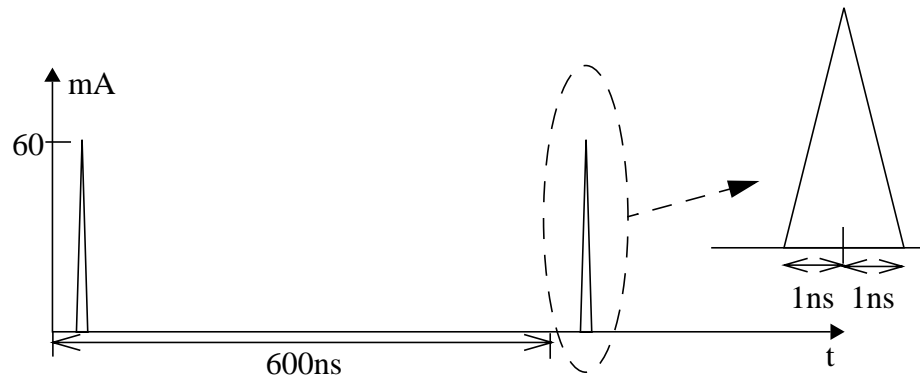
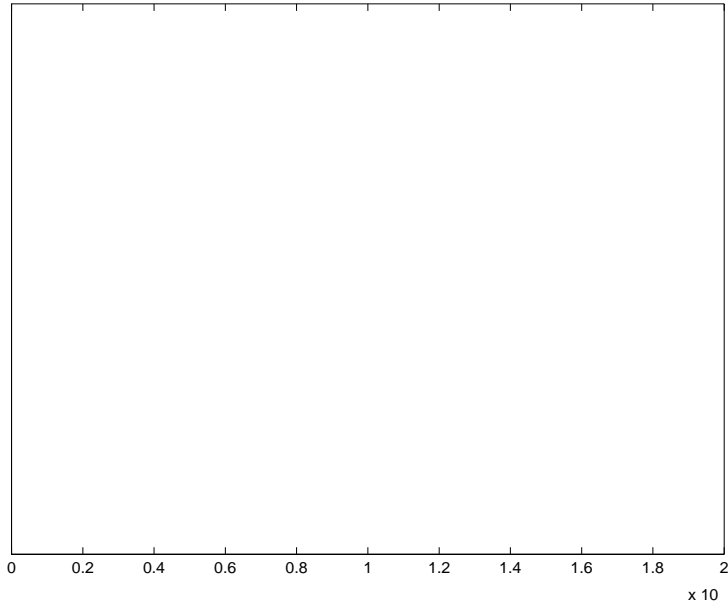
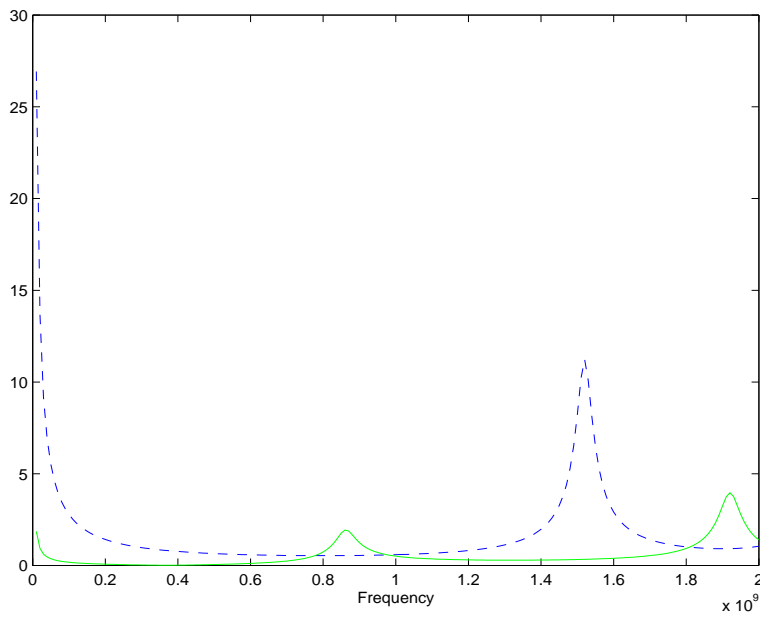


Fig. 8.2 Current profile for the digital chip in Fig. 8.1



x21-46650.8 x20.8 x61 -6910.2 x64

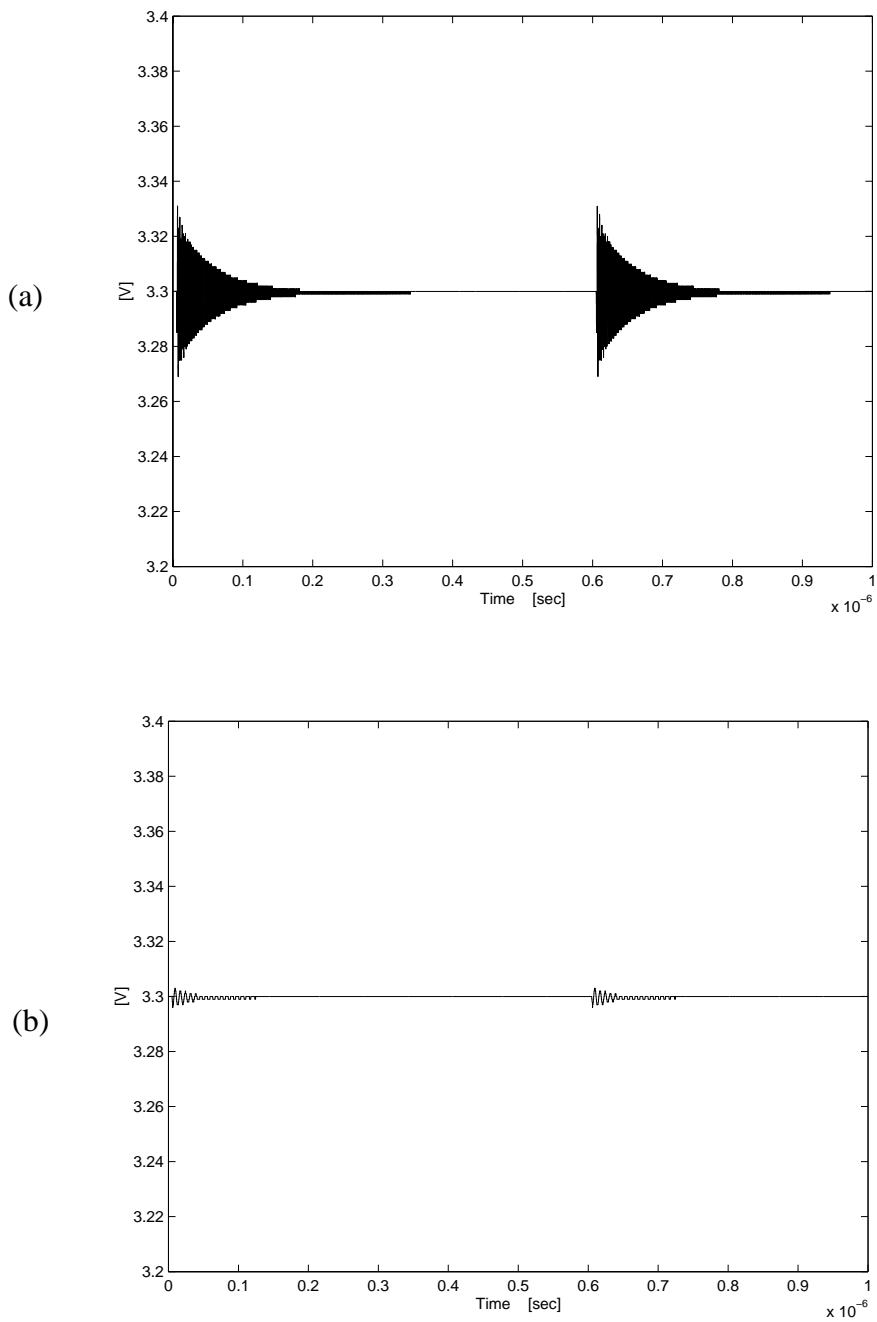


Fig. 8.4 Induced voltage fluctuation at the analog filter power supply when the drivers of the digital chip is switching with (a) no decoupling capacitor and (b) with decoupling capacitors

8.2 Core Switching Noise Analysis for a CMOS Test Chip

This section discusses various simulation results of core switching noise for a CMOS ASIC test chip mounted on a Ceramic Ball Grid Array (CBGA) package attached to a printed circuit board (PCB), as shown in Fig. 8.5.

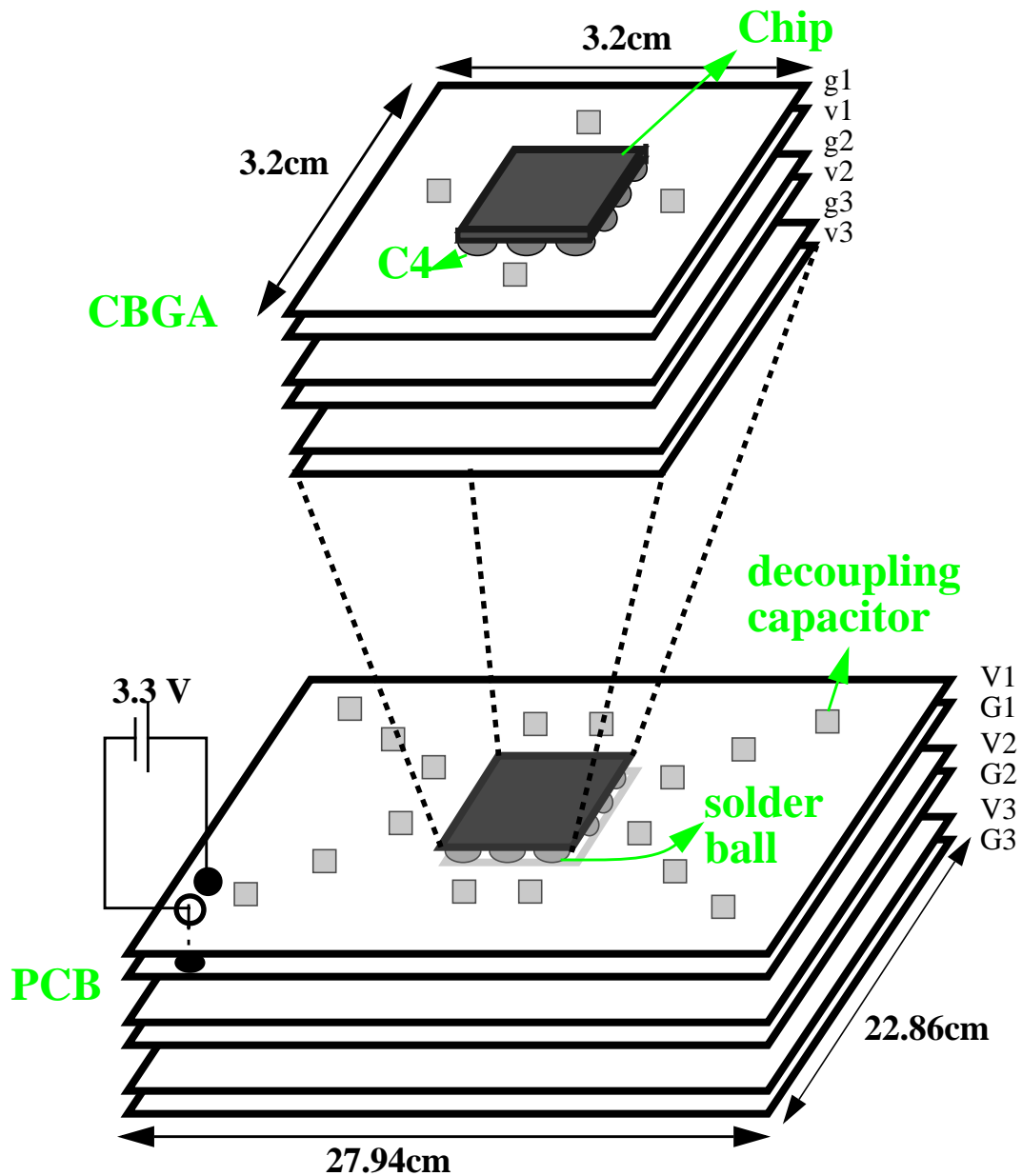


Fig. 8.5 Test setup for core switching noise

The test structure consists of multiple planes in both the package and PCB, as shown in Fig. 8.5. The CBGA package consists of three plane pairs and so does the PCB. The regulated power is supplied to the board and package from a corner of the PCB. The board is populated with 32 decoupling capacitors and the package is populated with 4 decoupling capacitors as described later. The CMOS chip was mounted on the package through C4 connections and the CBGA package was attached to the board through solder bumps. The test structure used for modeling in this section is based on the CBGA package and test card described in [3]. This test structure was modeled previously using an inductance network in [3] as shown in Fig. 8.6 where only lateral inductance of the planes were considered.

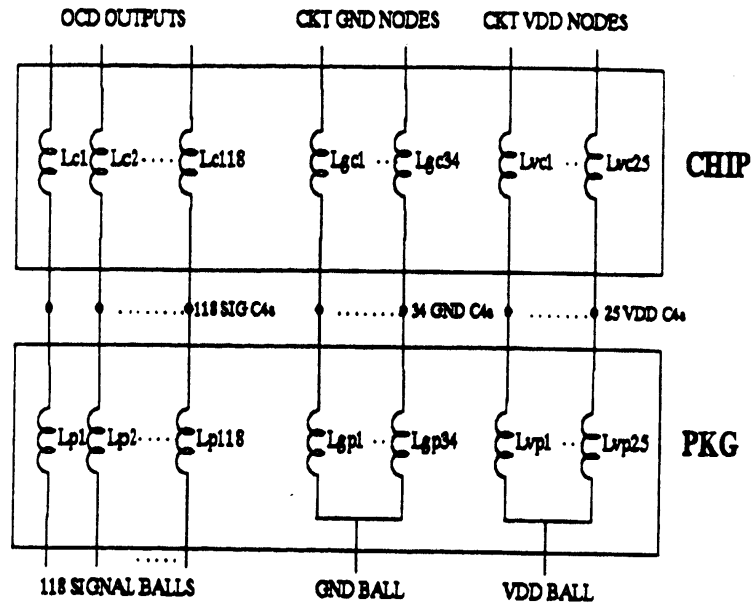


Fig. 8.6 Inductance network previously modeled for the structure in Fig. 8.5

In this section, the entire structure was modeled using the methods described in the previous chapters by accounting for all wave propagation effects. A method for modeling a single plane pair using wave resonator circuits with reduced order was described in Chapter 2. Since the test structure in Fig. 8.5 is multi-layered, the single plane pair model was extended to model multiple plane pairs using the methods described in [23], [45]. This is based on a skin effect approximation where the plane pairs are assumed to be capacitively coupled. Both the frequency and time domain results have been obtained using HSPICE.

The plane dimensions are shown in Table 8.1. The dielectric constants of the CBGA package and the PCB are 9.5 and 4.5, respectively. Each plane pair in Fig. 8.5 was modeled separately as in Table 8.1 and combined together in SPICE for a multi-layer stack-up. Simulations of the core switching noise were conducted first on the package (CBGA) alone in Sec. 8.2.1 and later the whole structure, including the package and test board in Sec. 8.2.2. In Table 8.1, g1 to g3 and v1 to v3 are the plane layers in the CBGA package and G1 to G3 and V1 to V3 in the PCB.

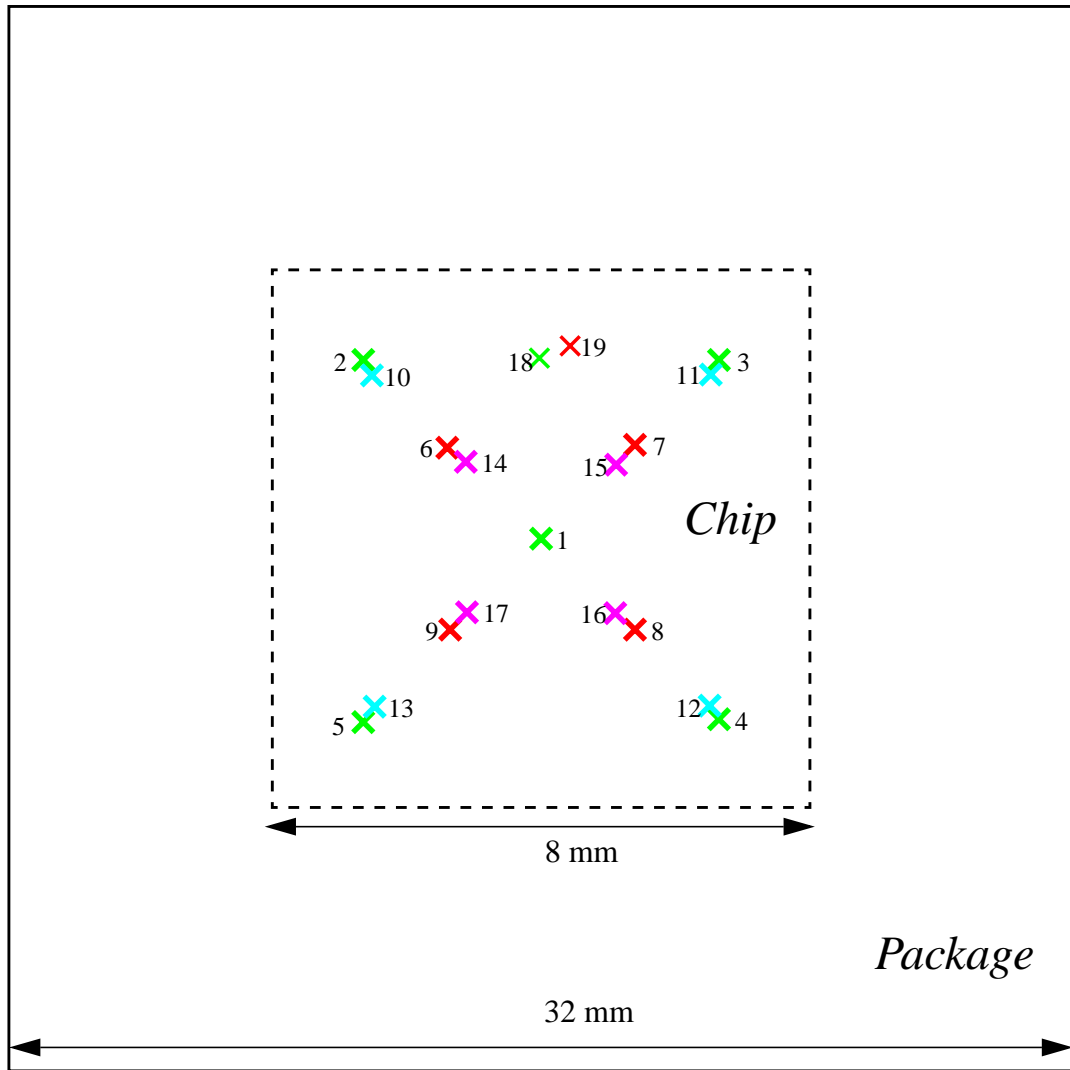
Table 8.1 Plane Pairs Modeled

plane layers	plane size	layer thickness	subcircuit element
g1-v1	0.8 cm x 0.8 cm	150 μm	Xplane1, planeSN
v1-g2	0.8 cm x 0.8 cm	300 μm	Xplane2, planeSK
g2-v2	3.2 cm x 3.2 cm	300 μm	Xplane3, planeLK
v2-g3	3.2 cm x 3.2 cm	300 μm	Xplane4, planeLK
g3-v3	3.2 cm x 3.2 cm	150 μm	Xplane5, planeLN
G1-V1	27.94 x 22.86	109.22 μm	Xplane6, planeTC1

plane layers	plane size	layer thickness	subcircuit element
V1-G2	27.94 x 22.86	337.82 μ m	Xplane7, planeTC2
G2-V2	27.94 x 22.86	109.22 μ m	Xplane8, planeTC1
V2-G3	27.94 x 22.86	337.82 μ m	Xplane9, planeTC2
G3-V3	27.94 x 22.86	109.22 μ m	Xplane10, planeTC1

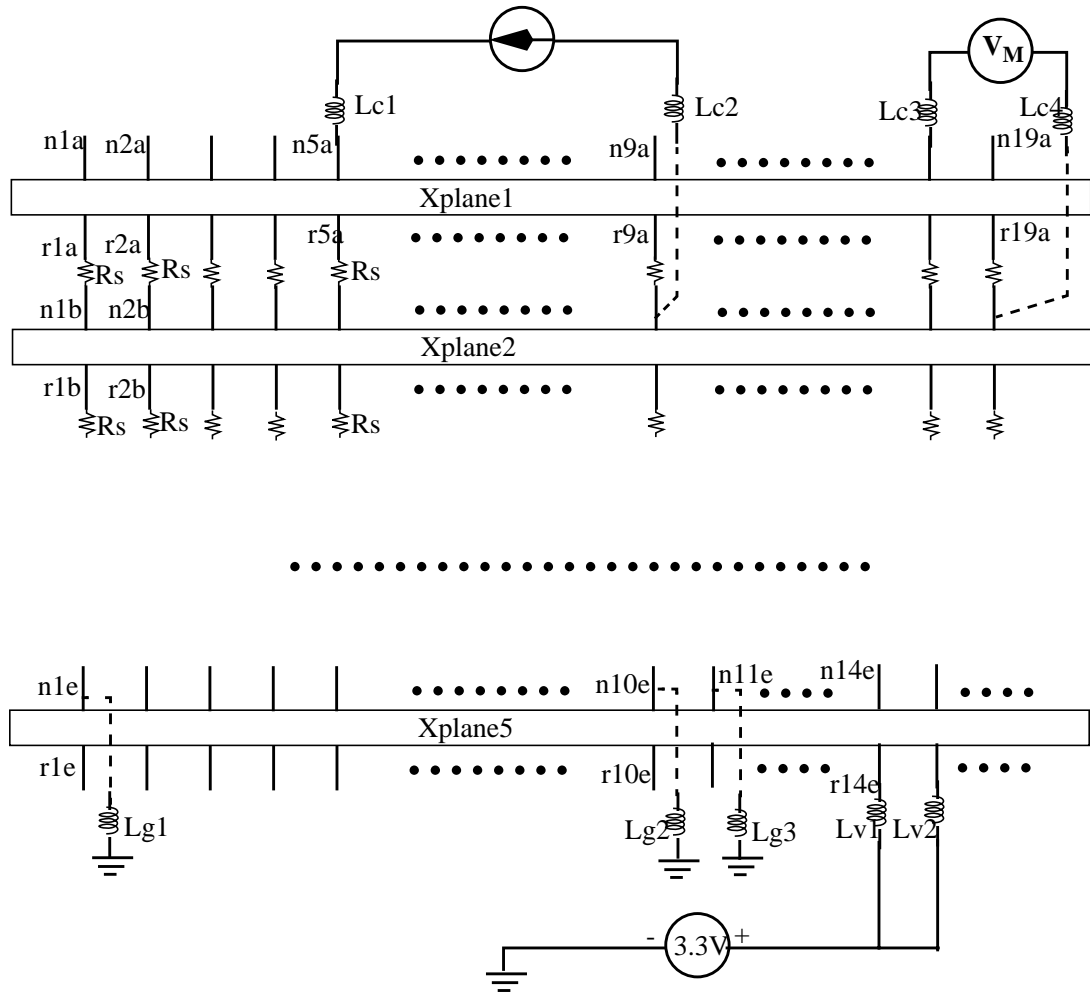
8.2.1 Simulation of core switching noise with the package only

In this section, the package alone is modeled and simulated to see the effect of the package planes on the switching noise. The ports were defined as shown in Fig. 8.7. Five ports for ground and four ports for Vdd were defined in the core area of the chip, as shown in Fig. 8.7. The same number of grounds and Vdds were defined for the vias connecting from the planes to the solder balls. The chip was powered at the bottom of the package, as shown in Fig. 8.8. The circuit diagram for the layer stack-up and connections for C4 and solder balls is also shown in Fig. 8.8. The current source emulating the active circuits is connected between ports 5 and 9 in Fig. 8.7 and the fluctuation on the power supply is observed between ports 18 and 19. The port locations are shown in the appendix. The vias are not shown in Fig. 8.8. Two kinds of current sources as shown in Fig. 8.9 were used to emulate on-chip switching activity. Several simulation results are shown in Figs 8.10 to 8.13 for the cases without inductance added, with inductances for vias only, with inductances for C4s and solder balls only, and with inductances for vias, C4s and solder balls. (a) and (b) of each figure represent the simulation results using the current source (a) and (b) in Fig. 8.9, respectively. Small resistances of $10^{-5} \sim 10^{-6} \Omega$ such as Rs in Fig. 8.8 were used in SPICE to avoid the error ‘source voltage/inductance loop’ in the simulations.



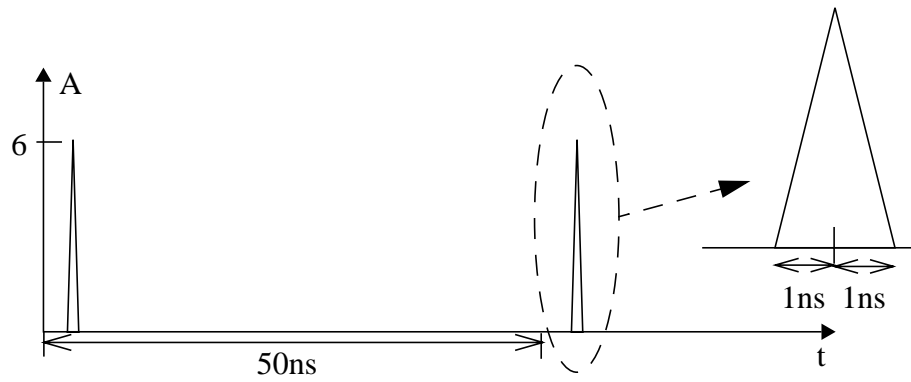
- 1 - 5: ports for ground vias connected between C4s and g1 through g3
- 6 - 9: ports for Vdd vias connected between C4s and v1 through v3
- 1, 10 - 13: ports for ground vias connected between solder balls and g3
- 14 - 17: ports for Vdd vias connected between solder balls and v3
- 18, 19: ports for differential voltage measurement, ground on g1 and Vdd on v1

Fig. 8.7 Port locations of the package defined in the core area for simulation

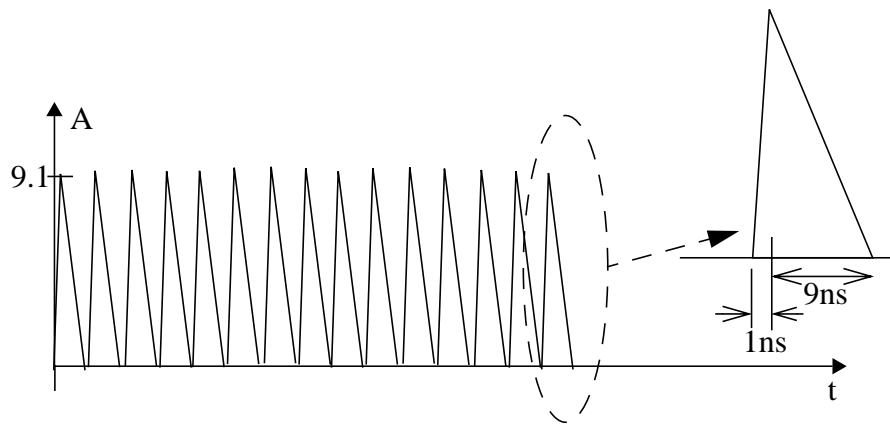


nxx, rxx: plane ports
Lcx: C4 inductance
Lgx, Lvx: solder ball inductance

Fig. 8.8 SPICE circuit diagram for the CBGA package



(a)



(b)

Fig. 8.9 Current profile used for on-chip switching activity

(1) Simulation I: Noise due to the package planes only

Vias, C4s, and solder balls were not modeled in this simulation. Vias were shorted with small resistances of $10^{-5}\Omega$. In Fig. 8.10, the noise voltage is very small indicating that the source does not excite electromagnetic waves of sufficient energy to cause the voltage to fluctuate.

(2) Simulation II: Noise due to via inductances

The differential voltage at the same location, between ports 18 and 19 was observed **with via inductance of 15pH added** for each via. The result is shown in Fig. 8.11.

(3) Simulation III: Noise due to C4 and solder ball inductances

The differential voltage at the same location, between ports 18 and 19 was simulated **with inductance for C4s and solder balls added**. The inductance values for each C4 and solder ball were given as 10pH and 20pH, respectively. The results are shown in Fig. 8.12.

(4) Simulation IV: Noise due to inductances of vias, solder balls and C4s

The differential voltage at the same location, between ports 18 and 19 was observed **with inductance for vias, C4s, and solder balls added**. The inductance values for each C4 and solder ball were given as 10pH. The results are shown in Fig. 8.13.

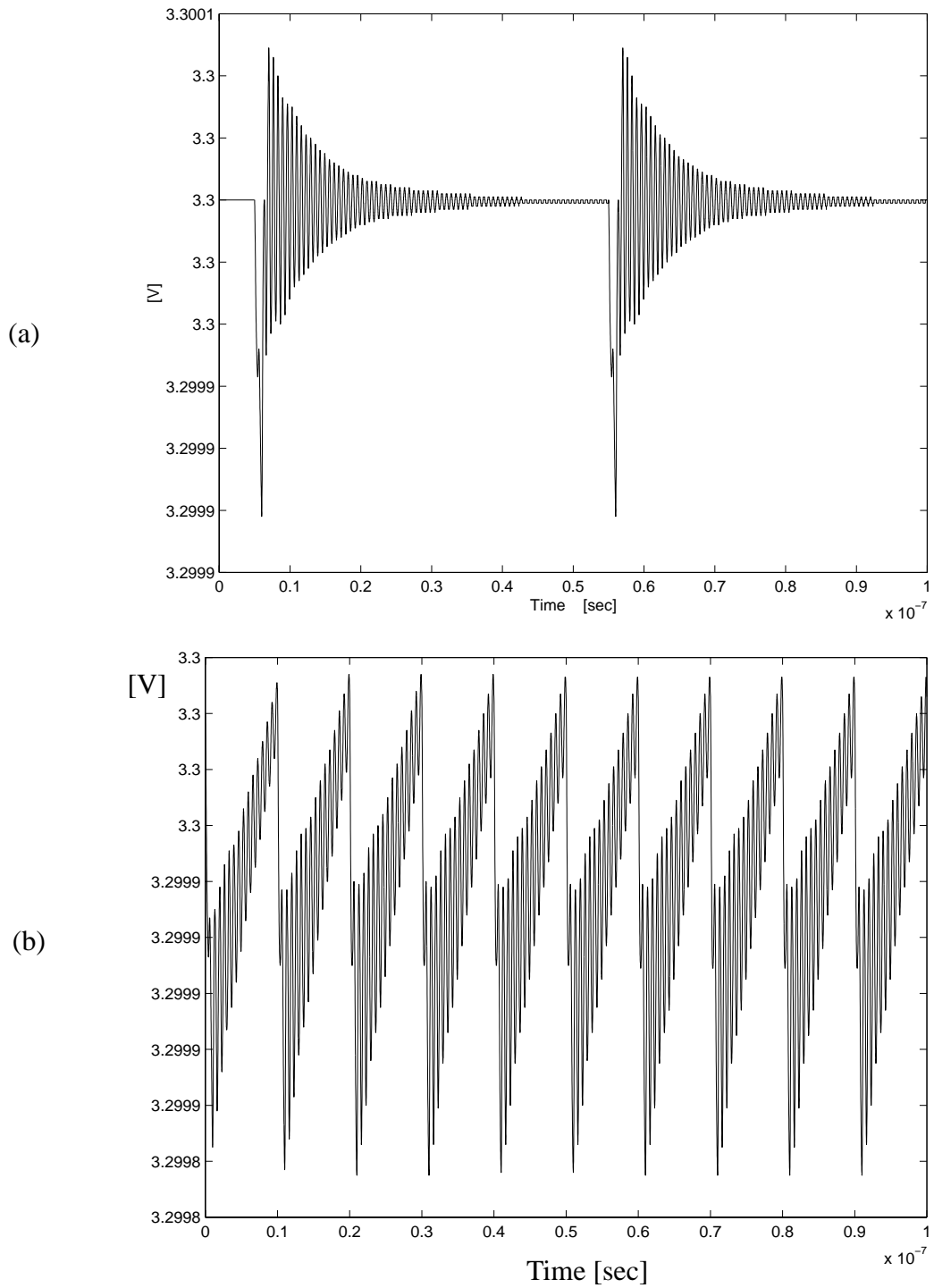


Fig. 8.10 Simulations of differential voltage (a) with the current source in Fig. 8.9a and (b) with the current source in Fig. 8.9b. The simulation model includes *no inductance* for vias, C4s, and solder balls.

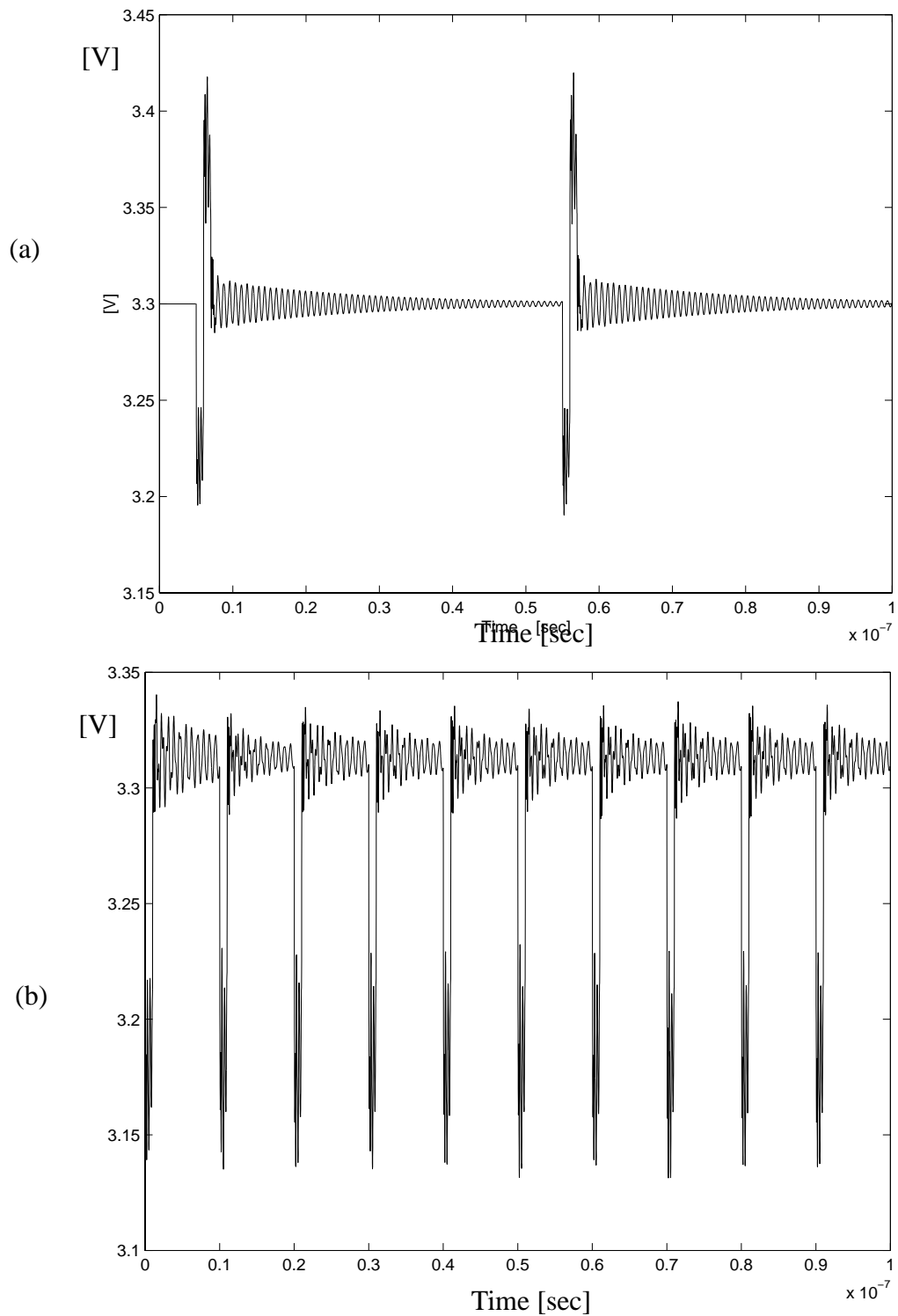


Fig. 8.11 Simulations of differential voltage (a) with the current source in Fig. 8.9a and (b) with the current source in Fig. 8.9b. The simulation model includes *inductances for vias only*

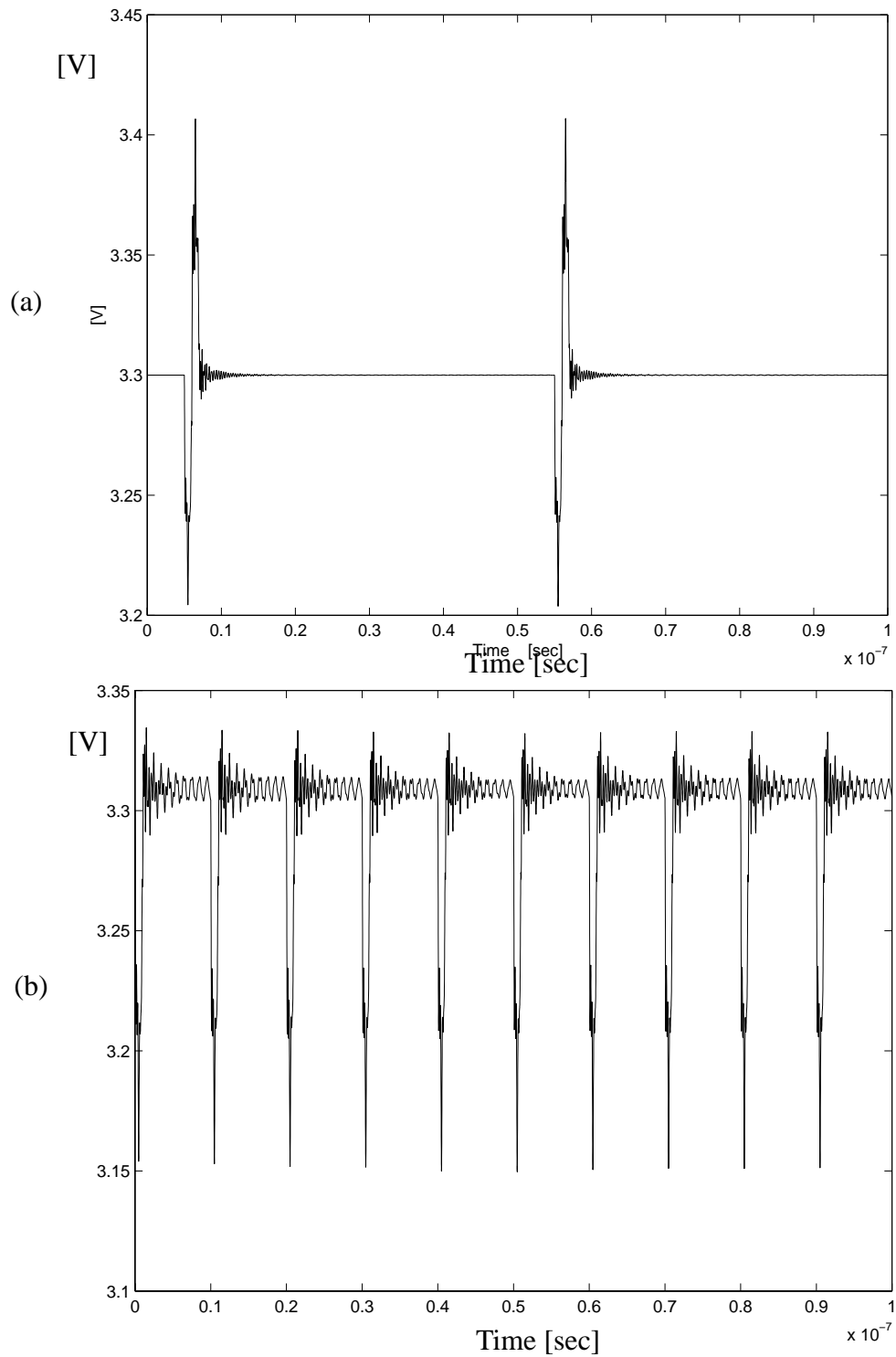


Fig. 8.12 Simulations of differential voltage (a) with the current source in Fig. 8.9a and (b) with the current source in Fig. 8.9b. The simulation model includes *inductances for C4s and solder balls only*.

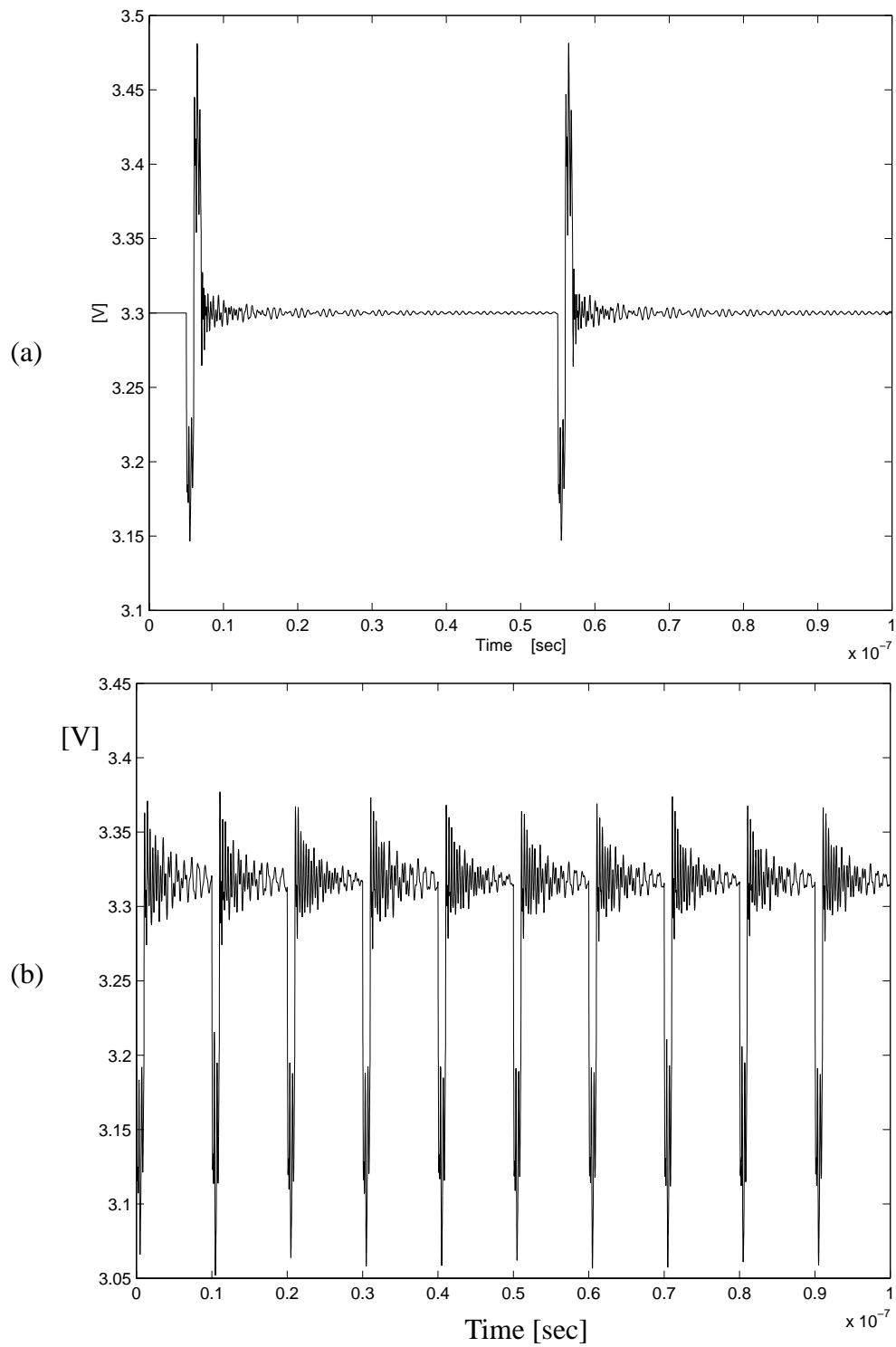
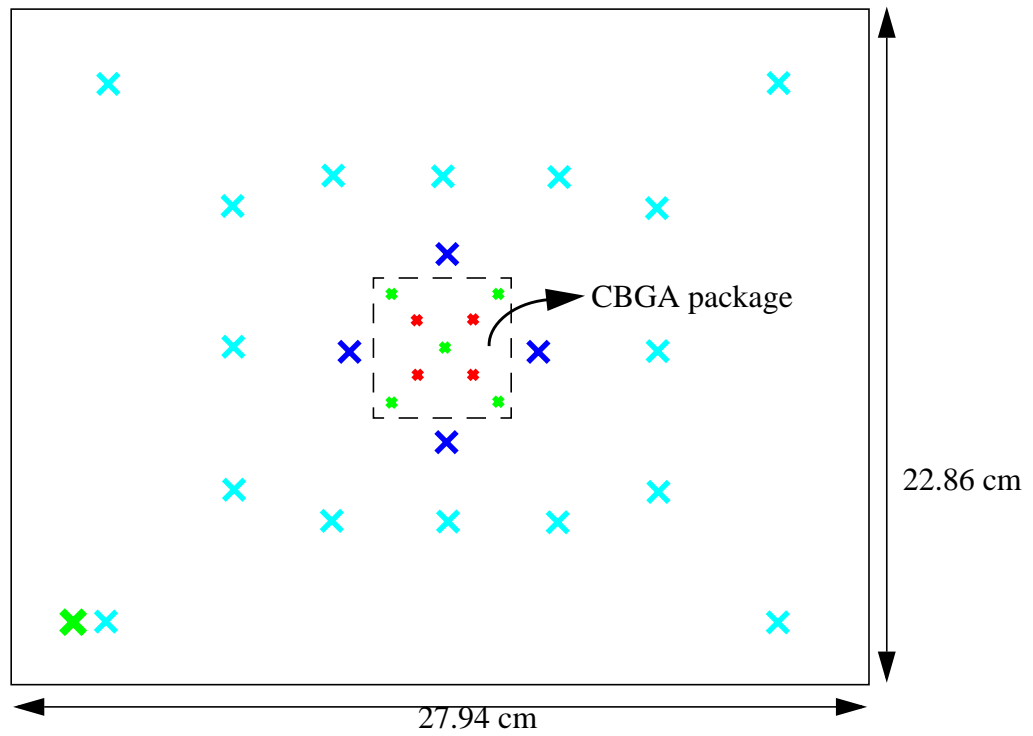


Fig. 8.13 Simulations of differential voltage (a) with the current source in Fig. 8.9a and (b) with the current source in Fig. 8.9b. The simulation model includes *inductance for vias, C4s and solder balls*.

From Figs 8.10-8.13, it is clear that the dominant noise is generated by the inductance and not by the planes when only the package is considered. This is a clear demonstration that the frequency content of the source may or may not excite the electromagnetic wave in the planes, causing them to bounce.

8.2.2 Simulation of Core Switching Noise with the test board included

In this section the previous simulation has been repeated by observing the voltage variation between ports 18 and 19 by including the test board in the model. Fig. 8.14 shows the test board dimension and port locations for the ideal power connection, decoupling capacitors and solder balls. Three kinds of decoupling capacitors were used, 47 nF with $R_E=0.1\Omega$ and $L_E=1\text{nH}$, 10 nF with $R_E=0.1\Omega$ and $L_E=1\text{nH}$, and 20 μF with $R_E=1\Omega$ and $L_E=10\text{nH}$. The CBGA package in Fig. 8.7 was connected to the board through solder balls within the dashed square area shown in Fig. 8.14. Inductances for vias and solder balls were not included in the simulation. The current source of Fig. 8.9 (a) was used for the simulation. First, the board was modeled with only one plane pair (G1 and V1). Fig. 8.15 and Fig. 8.16 show the voltage variation at ports 18 and 19, which are the C4 locations on the top layer of the CBGA package, without and with decoupling capacitors on the board, respectively. In the simulation of Fig. 8.16, ideal decoupling capacitors without parasitics were used.



- ✕ Port for the ideal power connection
- ✕ Ports for the decoupling capacitors of 114nF(2x47nF + 2x10nF)
- ✕ Ports for the decoupling capacitors of 20uF
- * Ports for Vdd (solder ball locations at the core area)
- * Ports for ground (solder ball locations at the core area)

Fig. 8.14 Port locations for the decoupling capacitors on the board

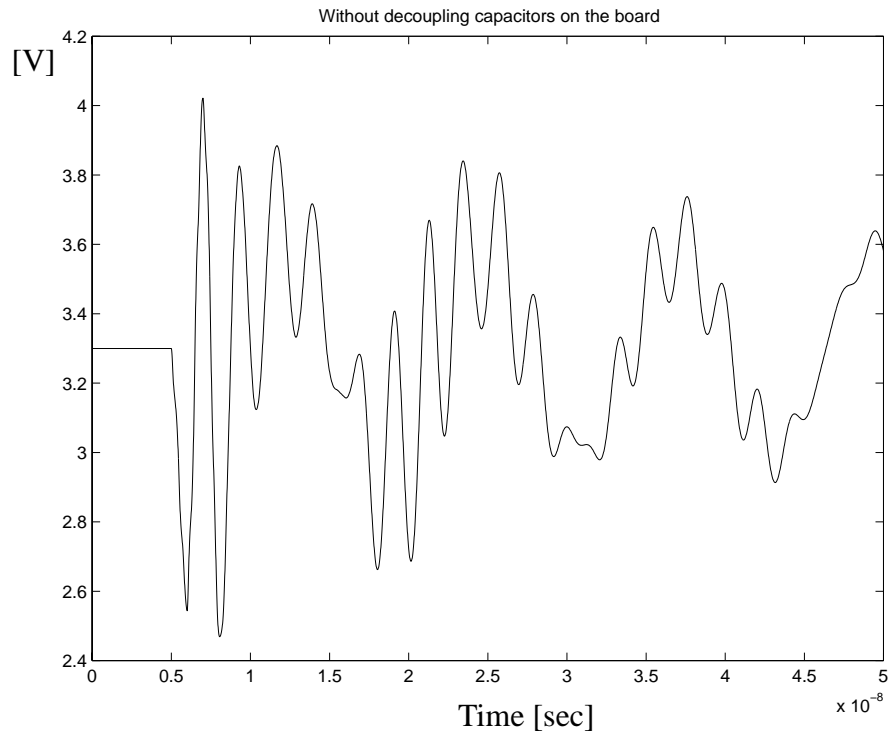


Fig. 8.15 Simulation with no capacitor on the board. The board model included only one plane pair.

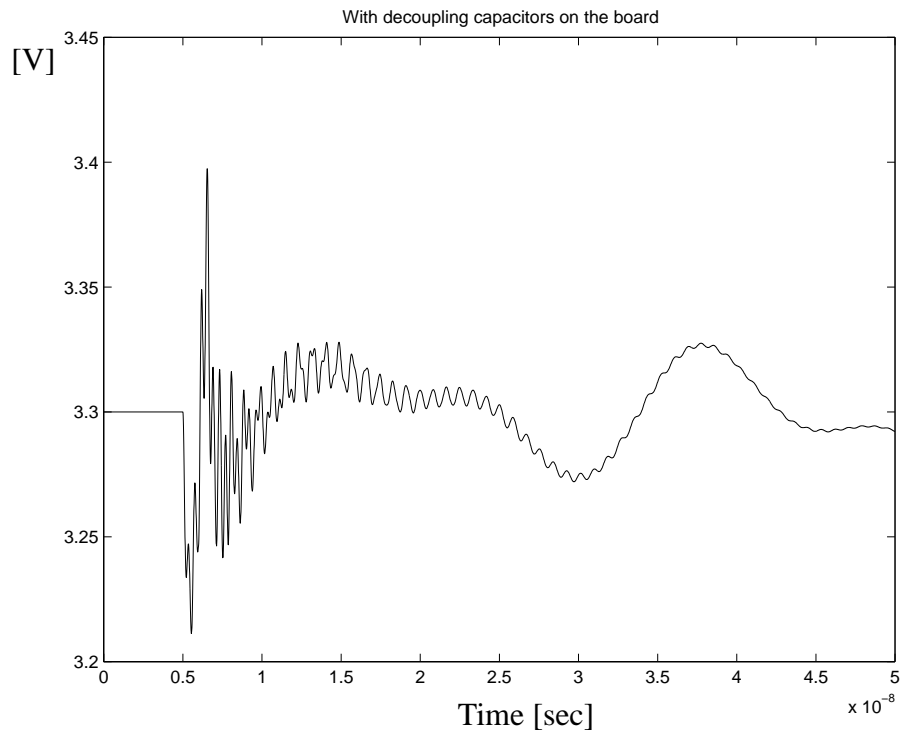


Fig. 8.16 Simulation with the decoupling capacitors on the board. The board model included only one plane pair.

Finally, the board was modeled with all three plane pairs and the simulation results for the differential voltage variation between ports 18 and 19 are shown in Fig. 8.17.

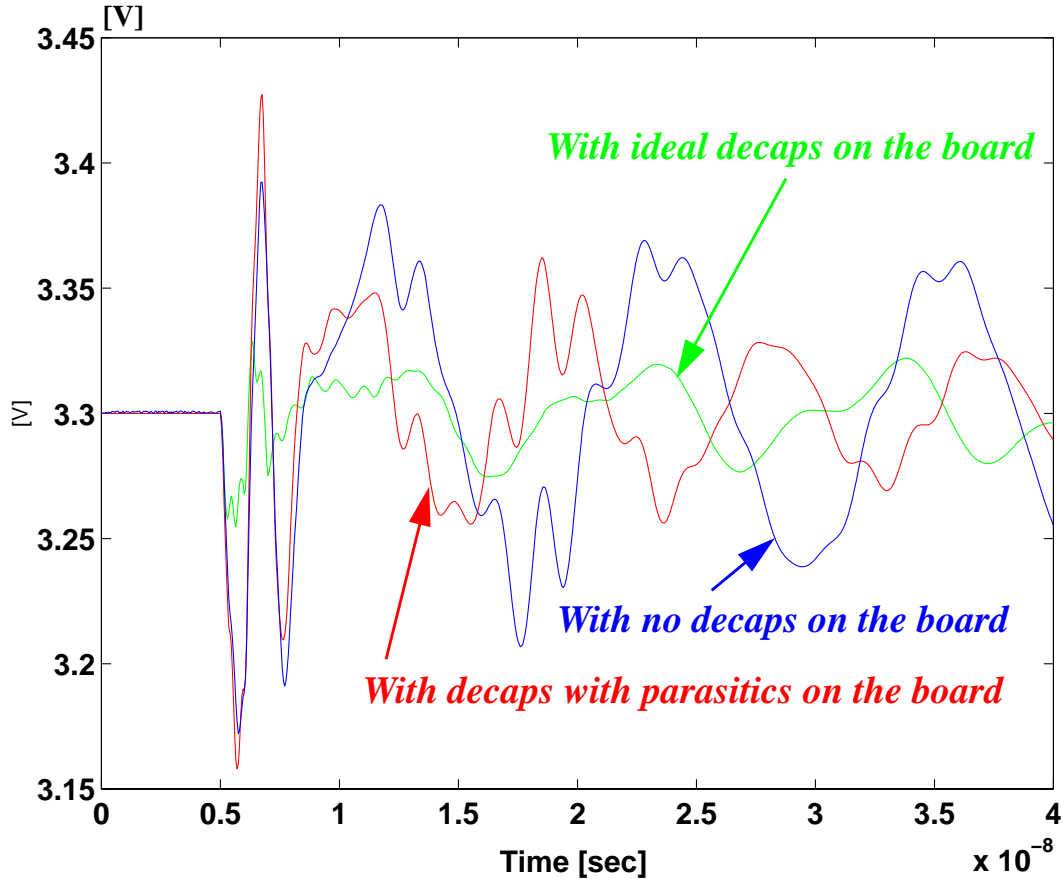


Fig. 8.17 Simulation with all plane layers included in the board model

A clear demonstration of the importance of the board plane layers is shown in Figs 8.15, 8.16 and 8.17. In the figures, the oscillatory waveforms are produced due to the plane resonance in the board. The 800 mV noise in Fig. 8.15 is lowered to 100 mV through decoupling capacitors in Fig. 8.16. In Fig. 8.16, the ideal decoupling capacitors with no parasitics were used. The additional capacitance and lower inductance obtained through the addition of the remaining plane pairs lowers the 100 mV noise to 40 mV. Fig. 8.17

shows the simulation results with all the plane layers on the board included. In Fig. 8.17, the Vdd planes and ground planes have been shorted together using ideal vias at the decoupling capacitor locations. It can be seen that the parasitics of the capacitors degrade the performance of the decoupling capacitors. It can also be seen that the steady state noise attenuates faster compared to the case with no decoupling capacitors. It is clear from sections 8.2.1 and 8.2.2 that the plane resonances can be ignored for the package but is significant for the board, assuming the current sources used. However, the scenario could change for faster sources as described in 8.2.4.

8.2.3 Simulation of Core Switching Noise with On-chip Capacitance

Next, an on-chip decoupling capacitor of 32 nF with a series resistance of 6.3 m Ω was connected between ports 5 and 9 and the same simulation was repeated with and without the module decoupling capacitors. In this simulation, the parasitics of on-board decoupling capacitors were included in the model. The four module capacitors of 32 nF with $R_E=0.1\Omega$ and $L_E=1\text{nH}$ were tied to the large package planes outside the die area about 5mm away from the die edge, one on each side of the die. The results are shown in Fig. 8.18. From the figure, it can be seen that the on-chip decoupling capacitor decreases the 140 mV power supply noise to 80 mV. However, the module decoupling capacitors had little effect on noise reduction. This can be attributed to the large lateral inductance of the planes from the capacitor to the chip.

The frequency response of the entire system is shown in Fig. 8.19 and Fig. 8.20. Both figures show three curves namely, i) the response of only on-chip capacitor, ii) the response without the on-chip capacitor and iii) the response of the entire system. In Fig.

8.19 which represents the self-impedance frequency response, the second peak is caused by the chip -package resonance. The resonance occurs due to the interaction between the capacitance of the chip and the inductance of the package. The frequency at which this occurs is the intersection point between curves i) and ii), as shown in Fig. 8.19. Beyond 500 MHz, the on-chip capacitance dominates the frequency response and hence completely suppresses all the plane resonances. Therefore, it can be concluded that the bandwidth that needs to be supported on the package and board is ~500 MHz.

The self-impedance frequency response for various on-chip capacitors is shown in Fig. 8.21. The chip-package resonance can be clearly seen in all the cases where the resonance shifts to a lower frequency as the on-chip capacitance is increased.

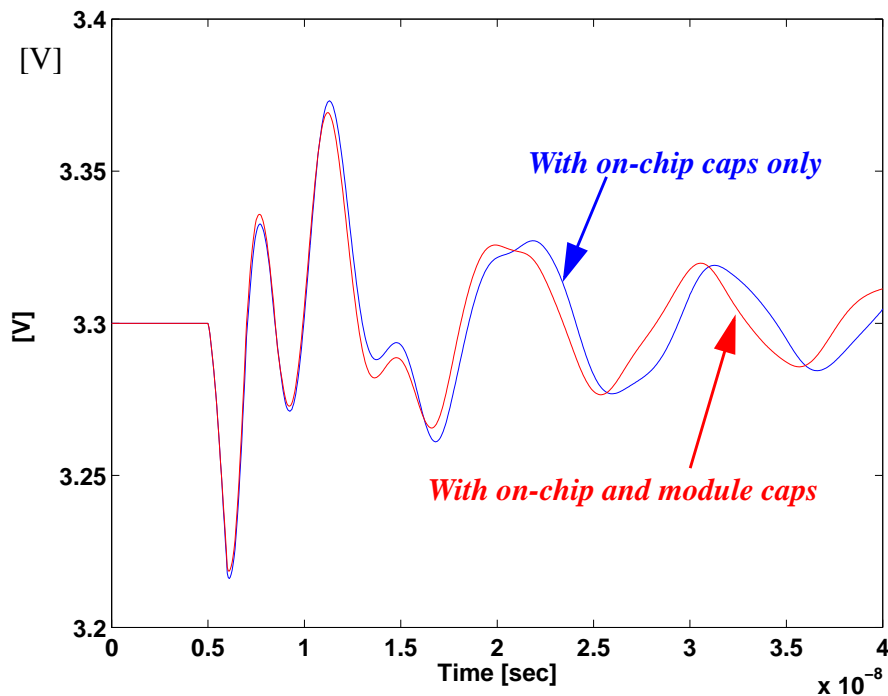


Fig. 8.18 Simulation with all plane layers and on-board decoupling capacitors and on-chip and module decoupling capacitors included in the model

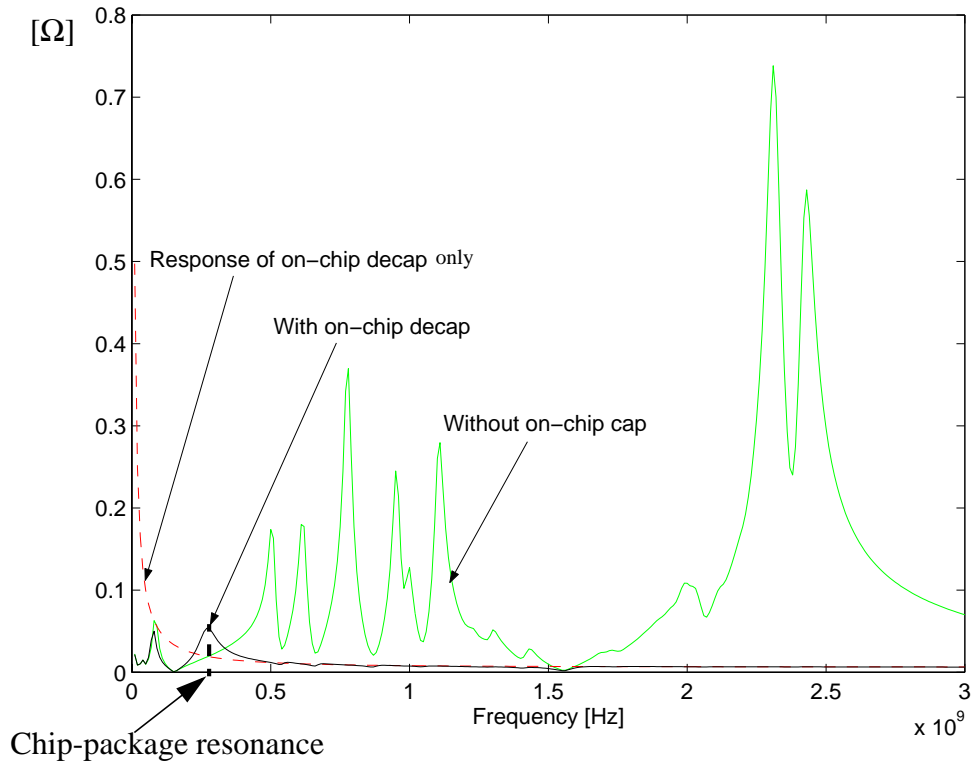


Fig. 8.19 Self-impedance seen from the chip (switching side)

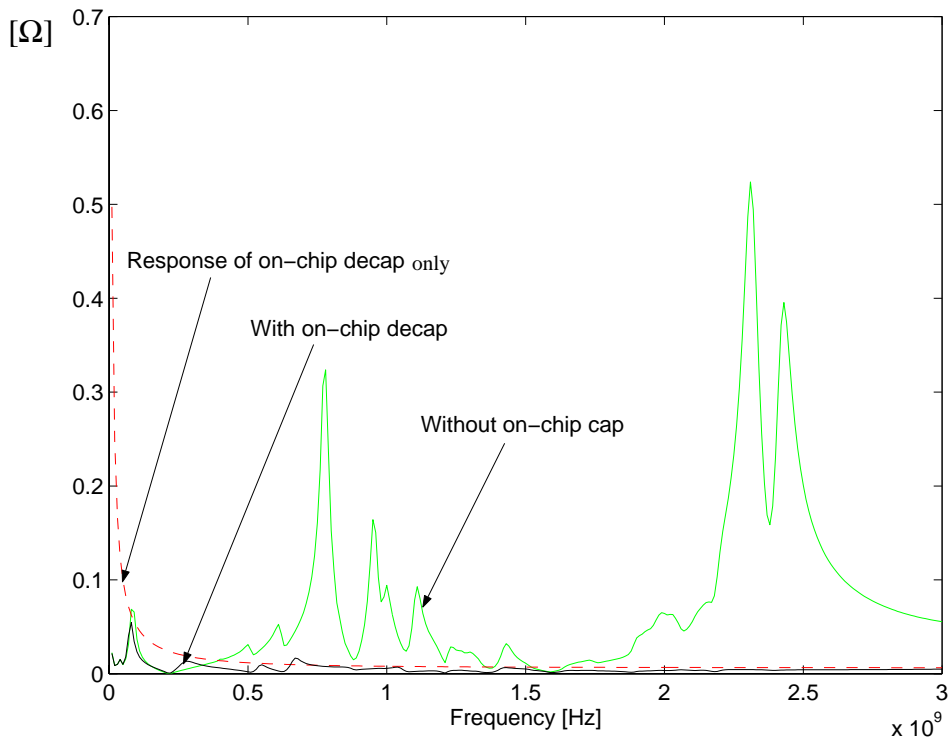


Fig. 8.20 Trans-impedance seen between the switching driver and quiet driver

For an on-chip capacitance of 500nF, the chip-package resonance occurs at a very low frequency. In addition, the impedance is minimized indicating that the bandwidth to be supported in the package and board is $\sim 190\text{MHz}$. The on-chip capacitance as a function of the resonance frequency is shown in Fig. 8.22.

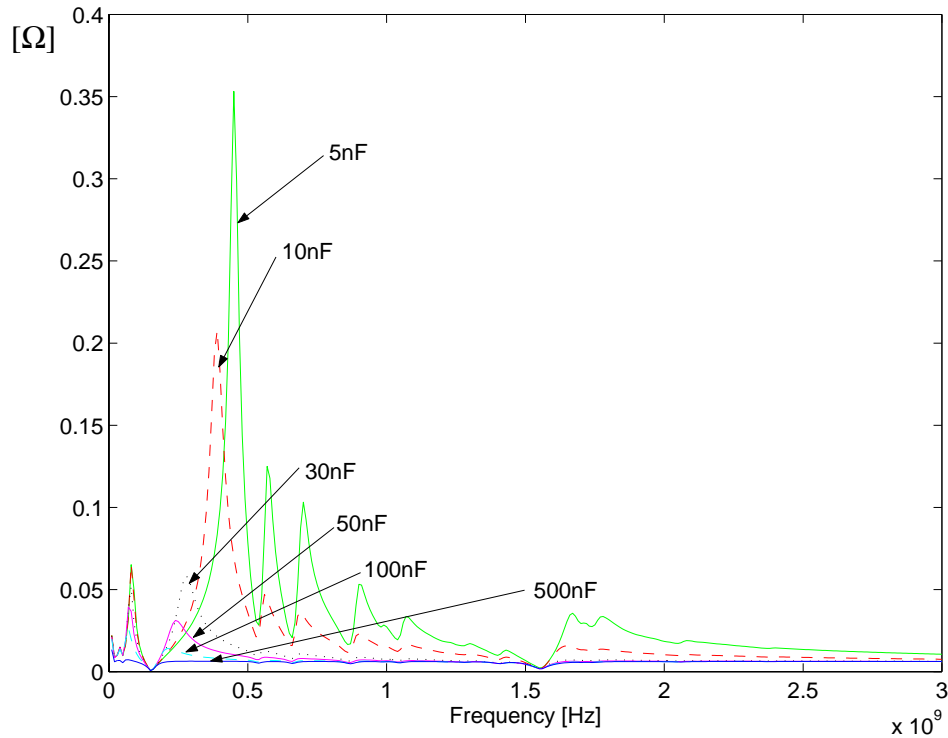


Fig. 8.21 Self-impedance seen from the chip with different on-chip capacitance values

8.2.4 Simulation of Core Switching Noise with Fast Current Sources

In this section, the results of the simulations in 8.2.1 (4), which is shown in Fig. 8.13b, using current sources with different rise times have been compared. First, the current source with 1ns rise time and 9ns fall time as in Fig. 8.9 (b) was used and the result is shown in Fig. 8.23 (a).

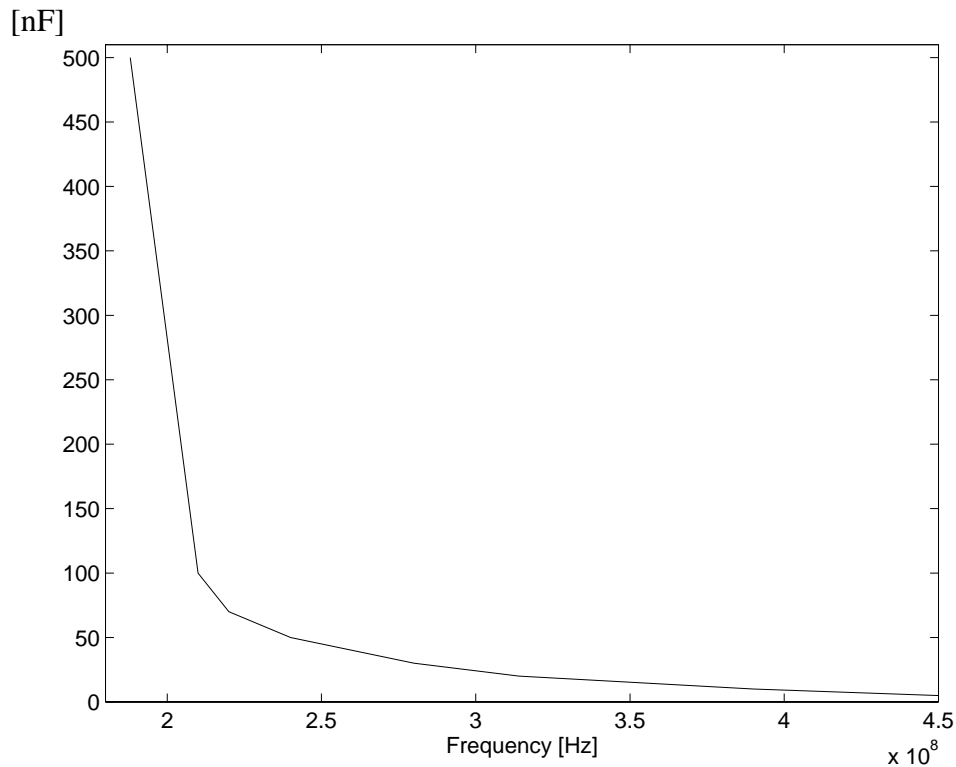


Fig. 8.22 On-chip capacitance vs. chip-package resonant frequency

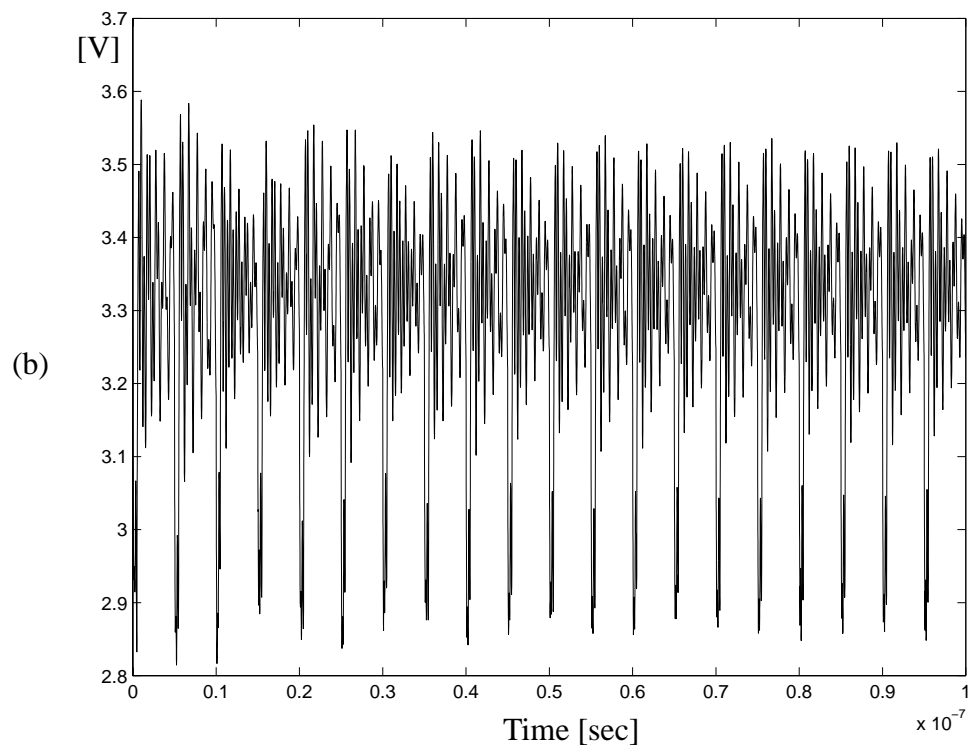
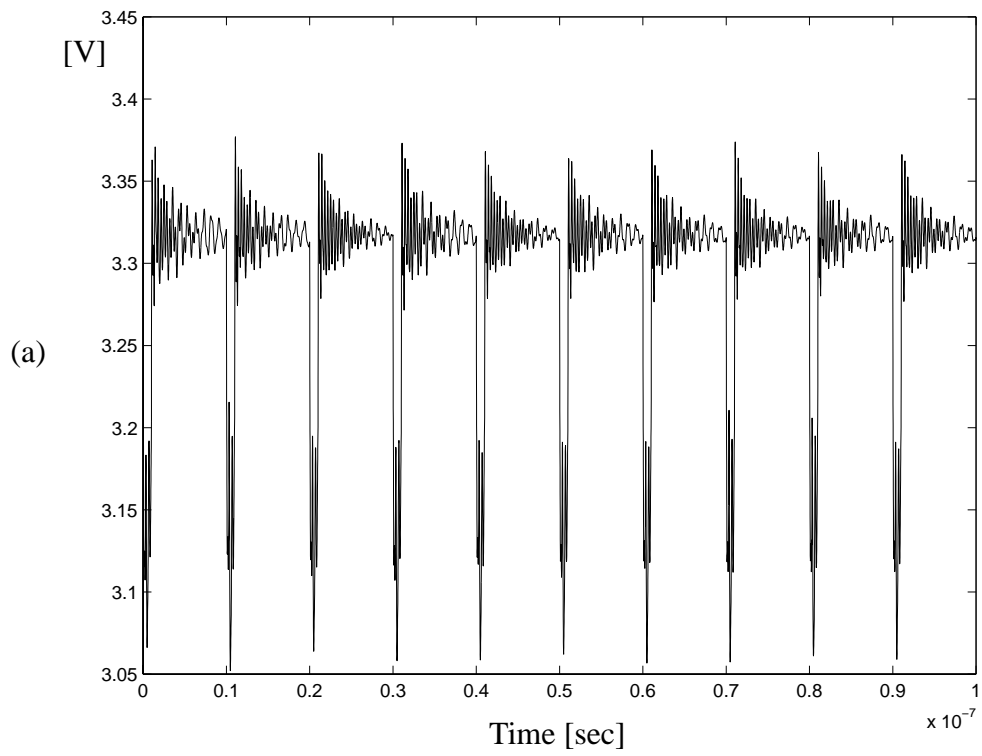
In the second simulation, the current source with 0.5ns rise time and 4.5ns fall time was used and the result is shown in Fig. 8.23 (b). In the third simulation, the current source with 0.1ns rise time and 0.9ns fall time was used and the result is shown in Fig. 8.23 (c). In all three cases, only the package models were used with the inductances of vias and C4s and no decoupling capacitors included. The oscillatory waveforms in Figs 8.23 (a), (b) and (c) are produced by the package plane resonances. The noise contribution due to the plane increases as the rise time falls, suggesting that the source excites the plane resonances. In Fig. 8.23 (c), the plane contribution is almost equal to the inductive contribution, suggesting the critical role that planes play in the generation of power supply fluctuation at the

chip. Clearly the CMOS5L Test Vehicle cannot support a 100 ps edge rate. The last simulation shown in Fig. 8.24 was conducted with the on-chip decoupling capacitor included for the case of Fig. 8.23c. The on-chip capacitance decreases the noise substantially. However, around ± 25 mV of noise exists in the package in the steady state due to plane resonances. This noise can increase with larger current sources.

8.3 Summary

In this chapter a mixed signal module and a CBGA package on test board were simulated for computing the core switching noise. Initially, the core noise produced by the CBGA package alone was investigated. It was observed that the inductance of vias, C4s and solder bumps contributes the maximum towards core noise and the effect of the planes is insignificant. Next, the entire test vehicle including the package (CBGA) and the board was modeled and the effect of decoupling capacitors on the noise was investigated. Noise with a maximum amplitude of 800 mV was observed with a single plane pair. The noise decreased to a maximum of 100 mV when decoupling capacitors were included. The noise decreased further to 40 mV when all the board layers were included. Finally, the CBGA package was simulated with faster current sources. From the results, it was observed that the package planes contribute to the noise more than the vias, when faster rise times were used.

In summary, it is clear that the plane resonances have a large contribution towards the power supply fluctuation, when the core switches. This effect will become pronounced as the frequency of the processor increases in future generations and is largely dependent on the on-chip capacitance.



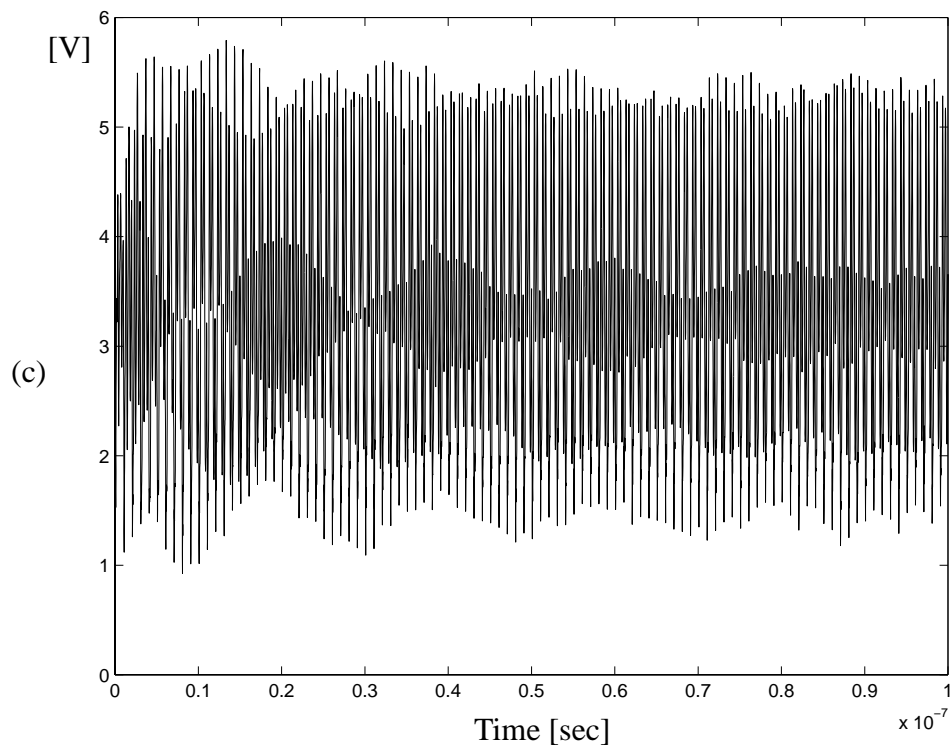


Fig. 8.23 Simulation results with current sources of different rise times (a) $t_r = 1\text{ns}$, $t_f = 9\text{ns}$ (b) $t_r = 0.5\text{ns}$, $t_f = 4.5\text{ns}$ (c) $t_r = 0.1\text{ns}$, $t_f = 0.9\text{ns}$

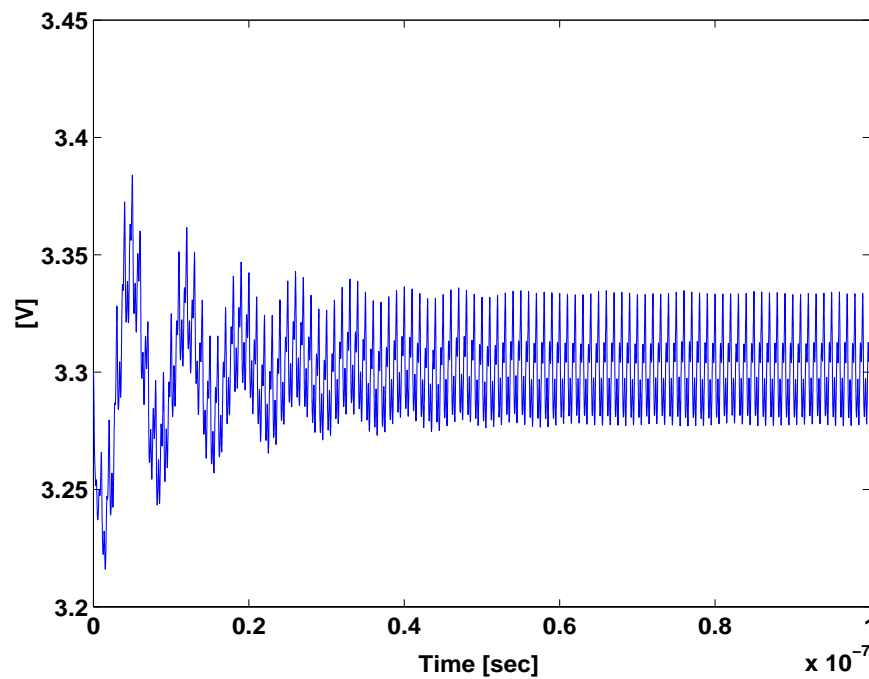


Fig. 8.24 Simulation result with the current source of $t_r = 0.1\text{ns}$, $t_f = 0.9\text{ns}$ and on-chip decoupling capacitor included

CHAPTER 9

Conclusion and Future Work

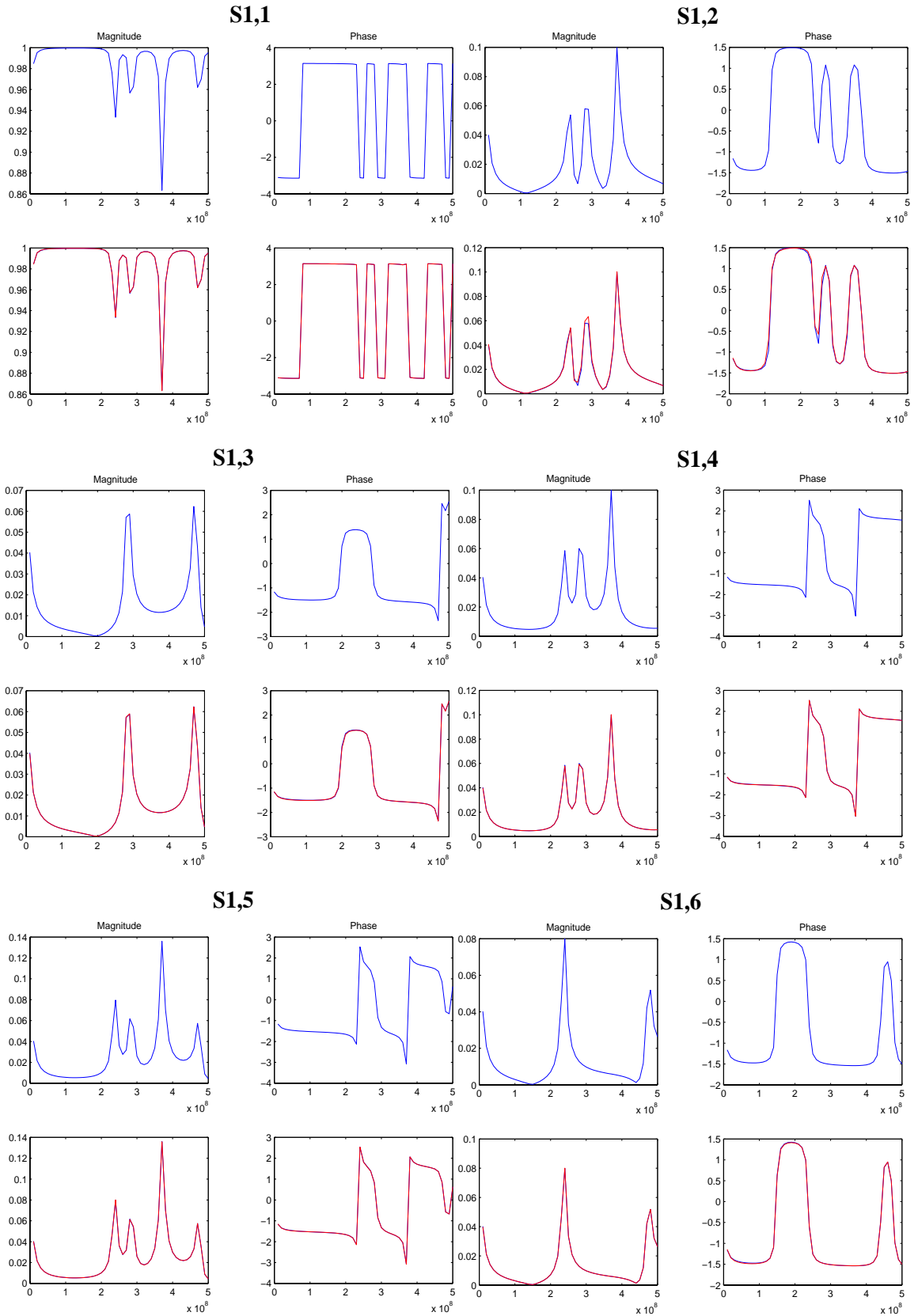
In this dissertation, modeling methods have been presented to accurately model planes in electronic packages for both regular and irregular structures. Methods have been developed to generate equivalent circuits using resonators for rectangular planes and macromodels for irregular planes. Since the plane pairs are highly resonant structures, modeling of these structures requires high order macromodels. A model order reduction method for rectangular planes has been developed to determine the optimum wave mode numbers for efficient simulation. Macromodels have been used to implement equivalent circuits where numerical solutions are available, such as in irregular planes and planes with decoupling capacitors. For highly resonant systems, S-parameter macromodel-based equivalent circuit was found to be accurate. While wave resonator models for rectangular planes are guaranteed to be passive, macromodels developed using an eigenvalue solution does not guarantee passivity. This can create a problem for transient simulations. In this dissertation, a method to preserve the passivity of the macromodels has been discussed for one-port and two-port power distribution networks, which can be extended for multi-port systems. All the methods described above have been verified using several simulations and measurements. Finally, the methods described have been applied for the simulation of core switching noise for a mixed signal module and a CMOS5L test vehicle from IBM. Effects of plane resonance and decoupling capacitors on switching noise have been investigated in

detail through numerous simulations. Through these simulations the importance of the accurate modeling of planes has been demonstrated.

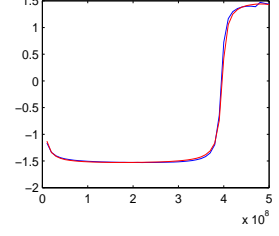
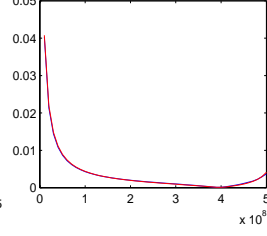
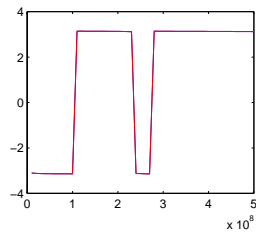
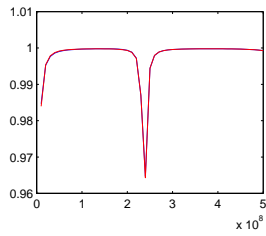
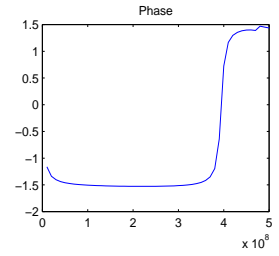
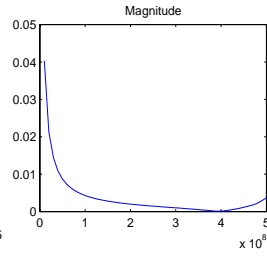
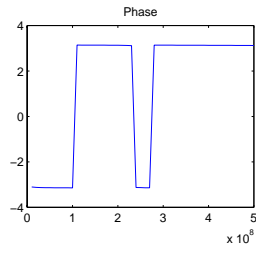
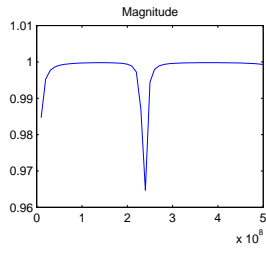
As an extension to the methods described in this dissertation, the following areas of focus may be appropriate:

- Inclusion of via inductance in the plane models. These can be achieved using PEEC models generated from Fast Henry, an inductance extraction program developed at MIT.
- Methods to assure the passivity of S-parameter macromodels.
- Application of iterative methods such as the Conjugate Gradient method to speed-up simulations.

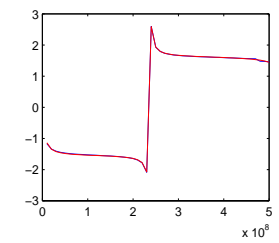
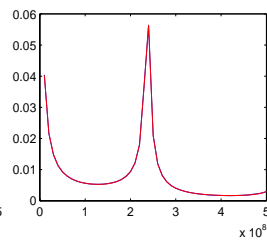
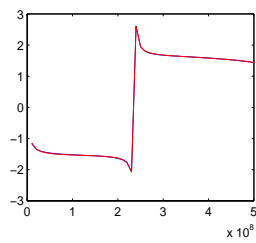
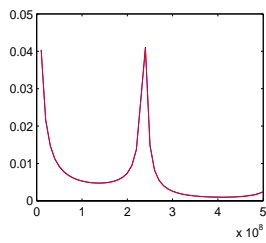
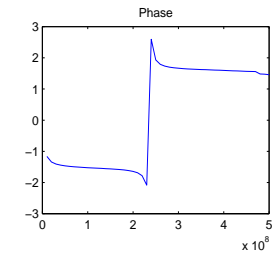
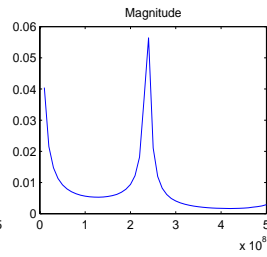
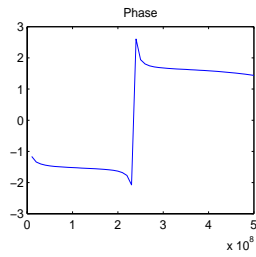
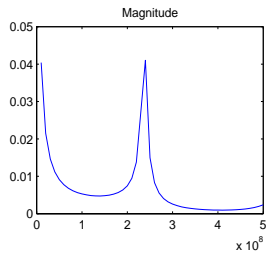
Appendix A. Macromodeling of 15 ports in Fig. 2.2



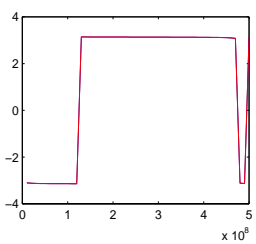
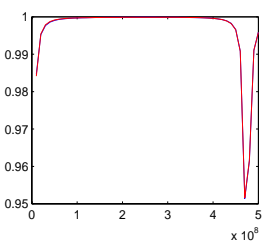
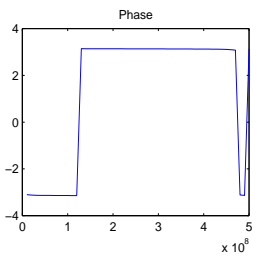
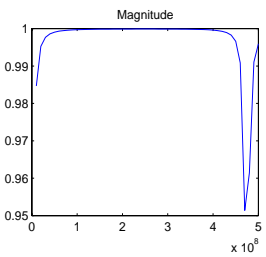
S7,7



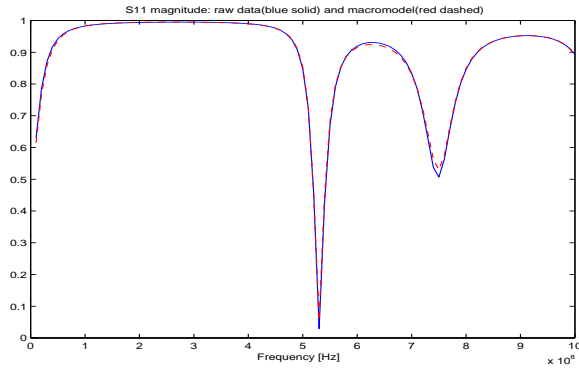
S7,9



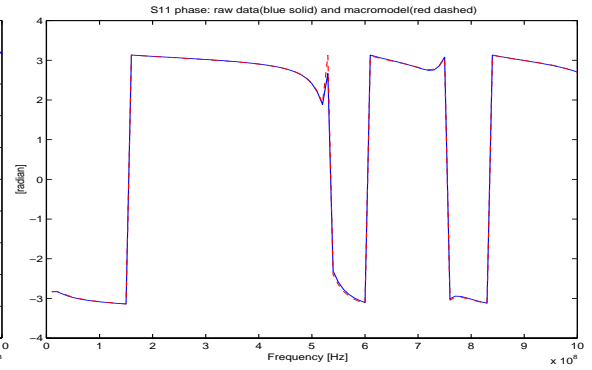
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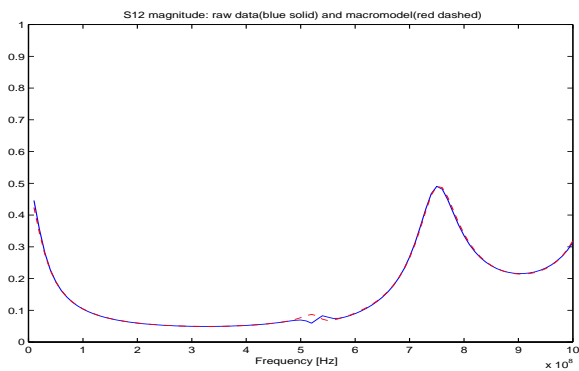
Appendix B. 4-port Macromodeling of TV2



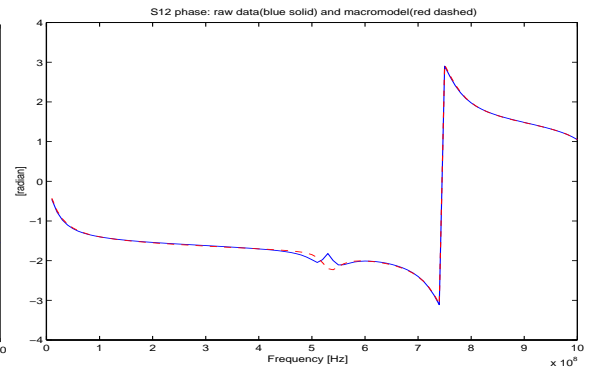
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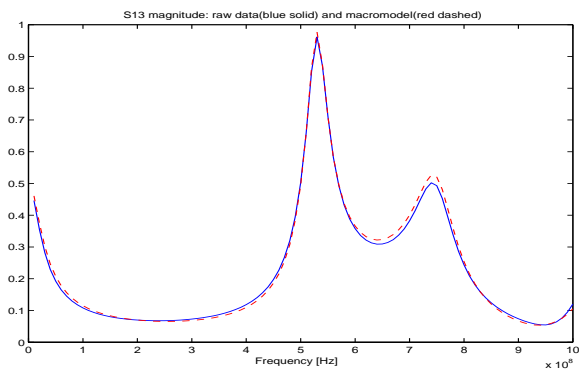
S11phase



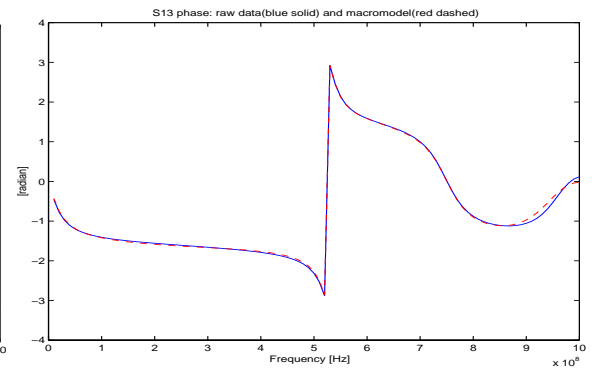
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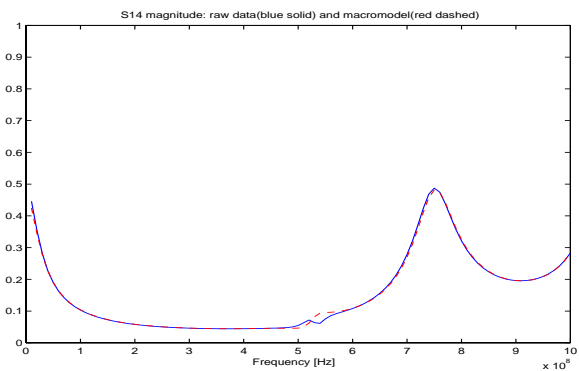
S12phase



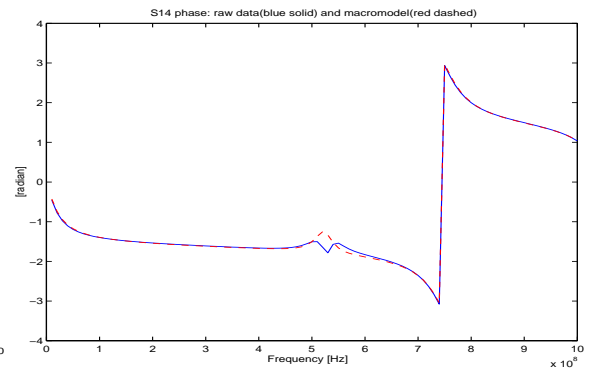
S13magnitude



S13phase



S14magnitude



S14phase

Appendix C. Port locations in Figs 8.7 and 8.14

Table A1: Port locations on the plane pair of 0.8 cm x 0.8 cm

port#	x [cm]	y [cm]	port#	x [cm]	y [cm]
1	0.4	0.4	11	0.654	0.654
2	0.124	0.676	12	0.654	0.146
3	0.676	0.676	13	0.146	0.146
4	0.676	0.124	14	0.285	0.515
5	0.124	0.124	15	0.515	0.515
6	0.262	0.538	16	0.515	0.285
7	0.538	0.538	17	0.285	0.285
8	0.538	0.262	18	0.4	0.676
9	0.262	0.262	19	0.446	0.7
10	0.146	0.654			

Table A2: Port locations on the plane pair of 3.2 cm x 3.2 cm

port#	x [cm]	y [cm]	port#	x [cm]	y [cm]
1	1.6	1.6	11	1.85	1.85
2	1.32	1.88	12	1.85	1.35
3	1.88	1.88	13	1.35	1.35
4	1.88	1.32	14	1.48	1.72
5	1.32	1.32	15	1.72	1.72
6	1.46	1.74	16	1.72	1.48
7	1.74	1.74	17	1.48	1.48
8	1.74	1.46	18	1.6	1.88
9	1.46	1.46	19	1.65	1.9
10	1.35	1.85			

Table A3: Port locations for the plane pair of dimension 27.94 cm x 22.86 cm

port#	x [cm]	y [cm]	port#	x [cm]	y [cm]
1	13.97	11.43	16	24.94	2
2	13.716	11.684	17	24.94	20.86
3	14.224	11.684	18	3	20.86
4	14.224	11.176	19	10	2
5	13.716	11.176	20	13.97	2
6	13.8548	11.5452	21	17.94	2
7	14.0852	11.5452	22	22.94	10
8	14.0852	11.3148	23	22.94	11.43
9	13.8548	11.3148	24	22.94	12.86
10	2	2	25	17.94	20.86
11	10	11.43	26	13.97	20.86
12	13.97	12.86	27	10	20.86
13	17.94	11.43	28	5	12.86
14	13.97	10	29	5	11.43
15	3	2	30	5	10

1-5:ground on g3, 6-9:Vdd on v3, 10:Global Vdd&gnd, 11-14:2X57nF, 15-30:20uF

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