Methodologies for Modeling Simultaneous Switching Noise in Multi-Layered Packages and Boards

A Thesis

Presented to
The Faculty of the Division of Graduate Studies

by

Sungjun Chun

In Partial Fulfillment of the Requirements for the Degree
Doctor of Philosophy
in the School of Electrical and Computer Engineering

Georgia Institute of Technology
Atlanta, Georgia
April 2002

Methodologies for Modeling Simultaneous Switching Noise in Multi-Layered Packages and Boards

Approved:

Dr. Andrew F. Peterson, Reading Committee

Dr. David C. Keezer, Reading Committee

Dr. Abhijit Chatterjee, Committee

Dr. Suresh K. Sitaraman, Committee

Dr. Madhavan Swaminathan, Chairman

Date Approved April 9, 2002

To my dearly beloved daughter Jeana, my wife Eunkyung,
my parents, and my sisters

ACKNOWLEDGEMENTS

It is a great pleasure to express my sincere appreciation and deepest gratitude to my thesis advisor, Dr. Madhavan Swaminathan, for his invaluable guidance, consistent support, and inspiration throughout all the stages of my graduate studies. His vast professional experience and knowledge has motivated me in my research, enriched and expanded my knowledge, and contributed significantly to this thesis. I also am indebted to the members of the thesis review committee, Dr. Andrew F. Peterson, Dr. David C. Keezer, Dr. Abhijit Chatterjee of the School of Electrical and Computer Engineering, and Dr. Suresh K. Sitaraman of the School of Mechanical Engineering for their valuable contributions in reviewing my thesis manuscript.

I would like to acknowledge the support received from Sun Microsystems, who provided the test vehicles and functioning computer systems required for the switching noise analysis. Specifically, I would like to thank Mr. Larry Smith at Sun Microsystems. The valuable discussions that I had with him, along with all the help that he provided, were instrumental in the successful completion of this research.

As I complete this thesis, it is also apparent that I owe special thanks to many other people who supported and helped me during my journey through my graduate studies and research at Georgia Tech. First among these is Dr. W. Marshall Leach of the School of Electrical and Computer Engineering for his helpful technical discussions and

encouragement. I am grateful to Dr. Mahadevan K. Iyer of the Department of Advanced Packaging at the Institute of Microelectronics in Singapore for his support of my research during my stay as a summer intern.

I also want to acknowledge my fellow students and a research engineer in the group for their help and for making my stay at Georgia Tech a pleasant one. My sincere thanks to Bhyrav, Erdem, Jifeng, Jinseong, Jinwoo, Joe, Joong-Ho, Kamal, Martin, Rohan, Sidharth, Sunghwan, Vinu, Woopoung and Dr. Lixi Wan. The journey would not have been possible without their support.

Finally, I gratefully thank my wife Eunkyung for the love and support that she has given me ever since we met. With her my dreams came true. I am thankful that my daughter Jeana is growing up into a beautiful girl. I see the reason I exist and love of God in her. I also gratefully thank my parents and sisters for all the sacrifice they have made for me.

Above all, praise, glory, and thanks to God!

Table of Contents

List of Tables

List of Figures

CHAPTER 1

Introduction

Current CMOS microprocessors and application-specific integrated circuits (ASICs) have hundreds of I/Os switching within one cycle time. When the noise produced by all the simultaneous switching circuits approaches the noise tolerance of a static CMOS circuit, the integrity of the output signal is degraded [1]. Therefore, proper prediction of the level of simultaneous switching noise (SSN) in a packaged electronics system has become one of the most important issues in high frequency digital design. As electronic packaging has progressed from traditional lead frame packages to packages that have power and ground planes, the SSN problem has shifted from a lead frame inductance problem to a power plane inductance problem. In addition, the planes behave as cavity resonators at high frequencies, which require the inclusion of both capacitance and resistance [2], [3]. As inductances become smaller for future packaging technologies, it is believed that the power plane contribution to SSN will dominate as compared to all vertical inductive effects. Thus computing the response of planes in the presence of interconnects represents the core of the SSN modeling problem, for future systems.

1.1 Power Distribution System

With increasing clock speeds and decreasing supply voltages in computing devices, the design of the power distribution system (PDS) is becoming an increasingly difficult challenge for modern CMOS technology.

The purpose of the PDS is to supply a constant, noise-free voltage to the integrated circuits in a system. To achieve this, the PDS must exhibit a very low impedance over a large frequency bandwidth where the noise voltages exist. A desirable impedance (Z) plot for the PDS, looking from the circuit load into the package and printed circuit board (PCB), is shown in Figure 1.1 [1].

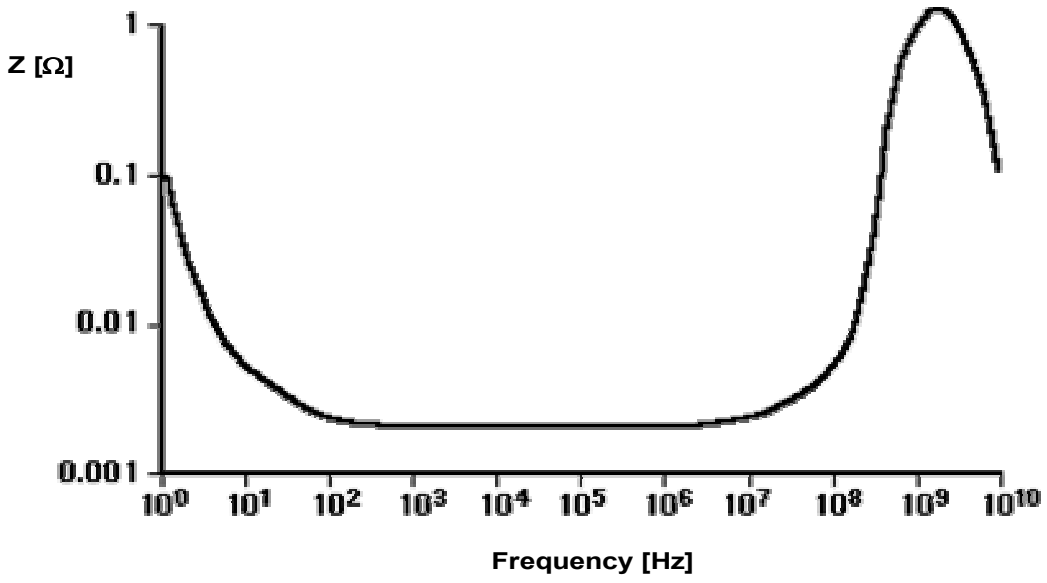


Figure 1.1 Output Impedance (Z) verses Frequency for a Typical Power Distribution System [1]

At very low frequencies, the power distribution network acts as a capacitor while, at high frequencies, it is primarily inductive. In the mid-frequency range, a good PDS should behave as a transmission line with a very low characteristic impedance, with the latter being orders of magnitude lower than the impedance of the total circuit load. As the frequency continues to increase beyond the inductive region, resonances can occur at the higher frequencies in a CMOS system. The goal is therefore to design the PDS such that its impedance is small throughout the frequency range desired as dictated by the operating speed of the electronic system.

In the PDS, noise voltages are generated by the intermittent current demands of loads, especially in CMOS circuits. When many of the drivers switch from low to high or high to low at the same time, very large transient currents must be delivered by the PDS. Even a small inductance in the PDS will generate a noise voltage, which could cause false triggering of other gates, which is commonly known as the SSN problem.

Figure 1.2 shows a simplified digital circuit consisting of four gates [4]. As an example, consider the circuit in Figure 1.2 when the output of gate 1 switches from high to low. Before gate 1 switches, its output is high, and the stray capacitance of the wiring between gates 1 and 2 is charged to the supply voltage. When gate 1 switches, the stray capacitance must be discharged before the low voltage can be transmitted to gate 3. Therefore, a large transient current flows through the ground system to discharge this stray capacitance. As a result of ground inductance, this current spike produces a noise voltage pulse at the ground terminals of gates 1 and 2, causing the compression of the power supply voltage. If the output of gate 2 is low, this noise pulse will be coupled to

the input of gate 4, as shown in Figure 1.2, causing gate 4 to switch states. The magnitude of this noise must therefore be below the noise tolerance of the logic family used in order to avoid having this noise cause intermittent logic errors during the operation of the digital circuitry [5].

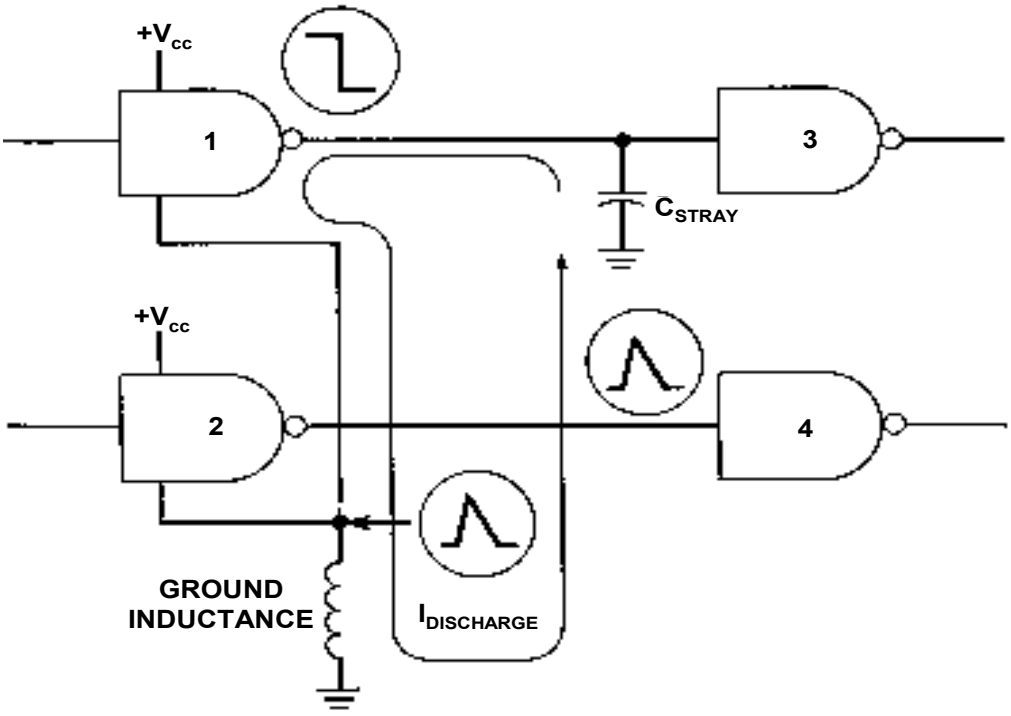


Figure 1.2 Noise Generation when Output of Gate 1 Switches from High to Low [4]

In a realistic system, the noise voltage generated by the simultaneous switching of N output drivers is given as [6]

$$\Delta V = NL_{eff}\frac{\Delta i}{\Delta t} \qquad (1.1)$$

where L_{eff} is the effective inductance of the power distribution system which accounts for all the parasitic inductance along the current path in the package, $\Delta i/\Delta t$ is the peak rate of change of current, Δi is the current required by each driver during the switching event, and Δt is the rise or fall time of the signal. Thus, the magnitude of the SSN is proportional to the total power supply current slew rate of the driver and the effective inductance of the power supply path.

Since reducing the current slew rate of the driver ultimately degrades the switching speed of a digital system, a reduction in the effective inductance of the package is one method for reducing SSN. This can be achieved by changing the package from a lead frame package to a ball grid array (BGA) package, as shown in Figure 1.3 (a), (b), [6] respectively.

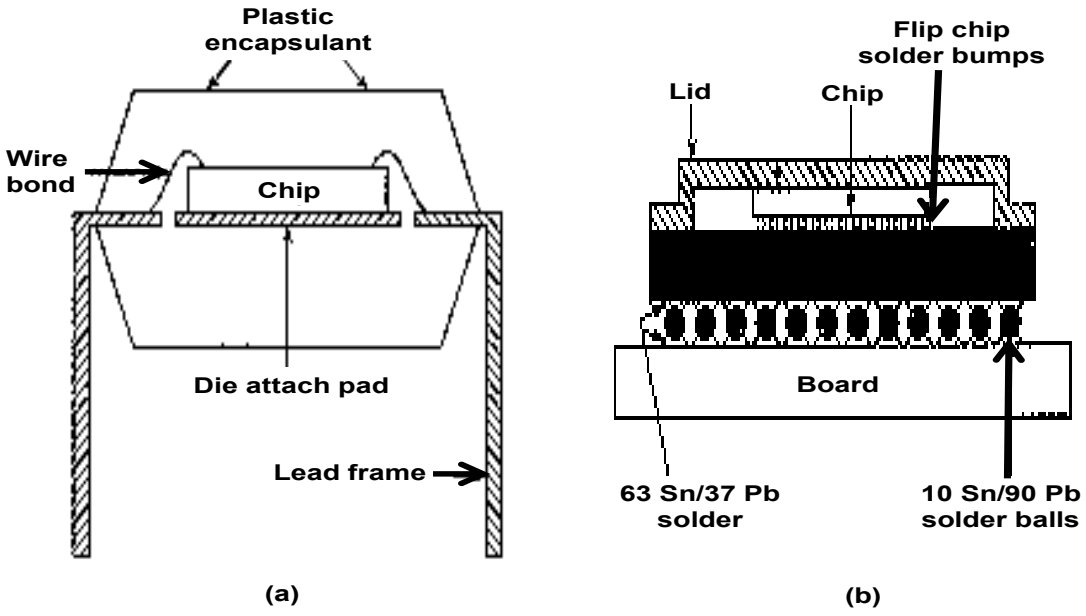


Figure 1.3 (a) Lead Frame Package (b) Ball Grid Array (BGA) [6]

All parasitics associated with the package are minimized in the BGA package due to the small inductances associated with the vertical current path consisting of vias, solder bumps and solder balls.

To meet the low inductance requirements, conducting planes, which have the least inductance and resistance amongst power distribution structures, are used for supplying power and ground in BGA packages. In [7], mesh and solid planes have been compared with regard to coupled noise, SSN, and shielding effectiveness. It has been shown that as the plane-to-plane separation decreases, the effective sheet inductance of the mesh plane increased to as much as five times that of the solid plane. Thus, the most effective way to reduce the inductance of the PDS would be the use of solid planes for power/ground, which makes the solid planes an important part of the PDS.

The behavior of the solid planes has been modeled using lumped element equivalent circuits for high speed digital multi-chip module applications in [8]. However, the accuracy of this model is limited since the rise time is much longer than the propagation time across the plane. Since the size of the power/ground planes in printed circuit boards (PCB) is not negligible compared to the wavelength of the highest frequency of interest, the transmission line effects of the planes must be considered. Thus, only a distributed circuit can accurately model the effects of high frequency noise coupled into the planes. Distributed models of the planes have been used in [9]. However, only the current flow parallel to a signal trace has been considered. The application of the transmission line model, which includes the distributed effects, has also been studied in [10]. The disadvantage of this model is that, it requires numerous transmission lines for

obtaining accuracy due to the spatial granularity of the transmission line grid, which in turn increases computation time. A numerical approach based on the finite difference time domain (FDTD) method for modeling planes has been discussed in [11]. However, this method requires a large computation time for obtaining a steady state solution in the frequency domain. Therefore, it is important to develop a method that would allow the accurate modeling of solid planes, which is compatible with the rest of the power supply hierarchy in a circuit simulator such as SPICE.

1.2 Simultaneous Switching Noise Impact on Microprocessor Performance and Signal Integrity

Simultaneous switching noise (SSN) has a large effect on microprocessor performance. The maximum operating frequency of a microprocessor FMAX is given by [12],

$$FMAX \propto \frac{\mu \cdot V_{cc}}{2 \cdot N \cdot L^2} \tag{1.2}$$

where μ is the mobility, V_{cc} is the power supply level, N is the number of inverters, and L is the channel length. The above relationship shows that a higher V_{cc} power supply voltage results in a higher FMAX. Figure 1.4 shows the FMAX of a microprocessor operating at a specific V_{cc} voltage based on the relationship in (1.2).

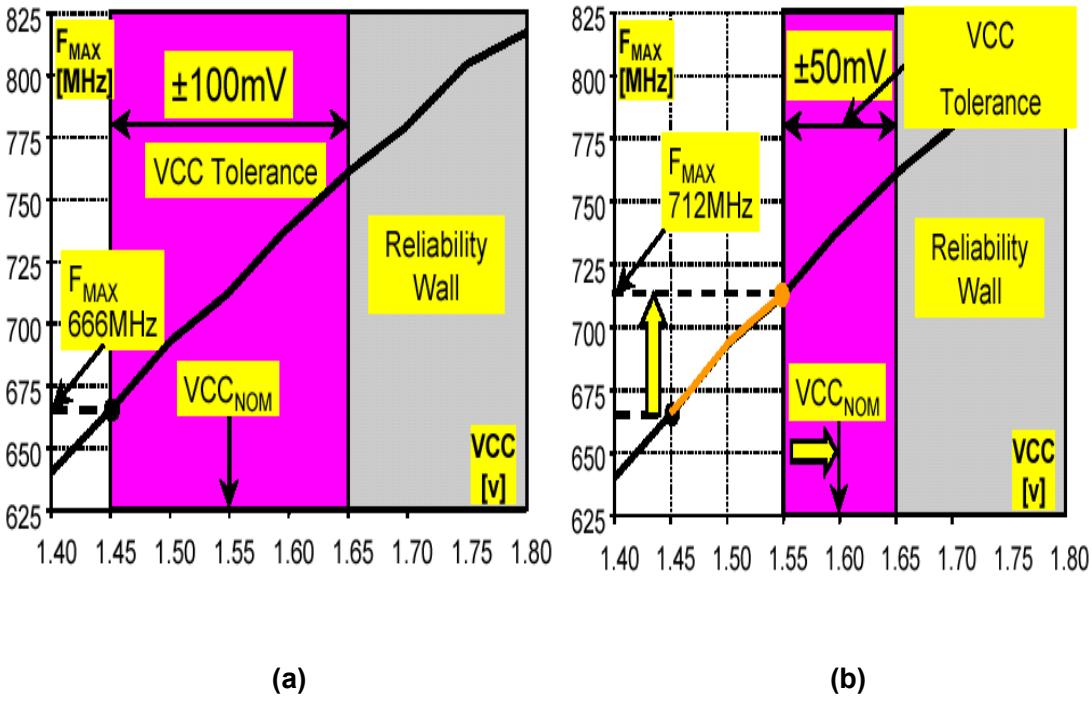


Figure 1.4 (a) FMAX vs. Vcc with Voltage Tolerance of ±100 mV (b) FMAX vs. Vcc with Voltage Tolerance of ±50 mV [12]

In the figures, the regions beneath the graph are the possible operating frequencies while operation in areas above the graph will result in functional failures. Figure 1.4 (a) shows the FMAX when the V_{cc} voltage tolerance is ±100 mV, which is determined by the stability and impedance of the power supply as well as the microprocessor current consumption. The minimum FMAX based on a ±100 mV voltage tolerance for this microprocessor is 666 MHz, as shown in Figure 1.4 (a). Figure 1.4 (b) shows the FMAX when the V_{cc} voltage tolerance is reduced to ±50 mV. It can be seen from the figure that the resultant FMAX has shifted from 666 MHz to 712 MHz when the V_{cc} voltage tolerance is reduced to ±50 mV from ±100 mV. Thus, a smaller supply voltage tolerance

due to reduced SSN enables a higher V_{cc} voltage, and therefore, the microprocessor can operate at a higher FMAX frequency.

SSN also has a profound effect on signal integrity of clock signals resulting in excessive clock skew. Figure 1.5 (a) shows a symmetric H-tree clock distribution network with n=4, which is the number of H-tree levels. At the end of the 4th level, drivers are implemented to feed the clock signal to all registers in the sub-blocks. Clock skew, by definition, is the time difference between the maximum and minimum delays, as shown in Figure 1.5 (b).

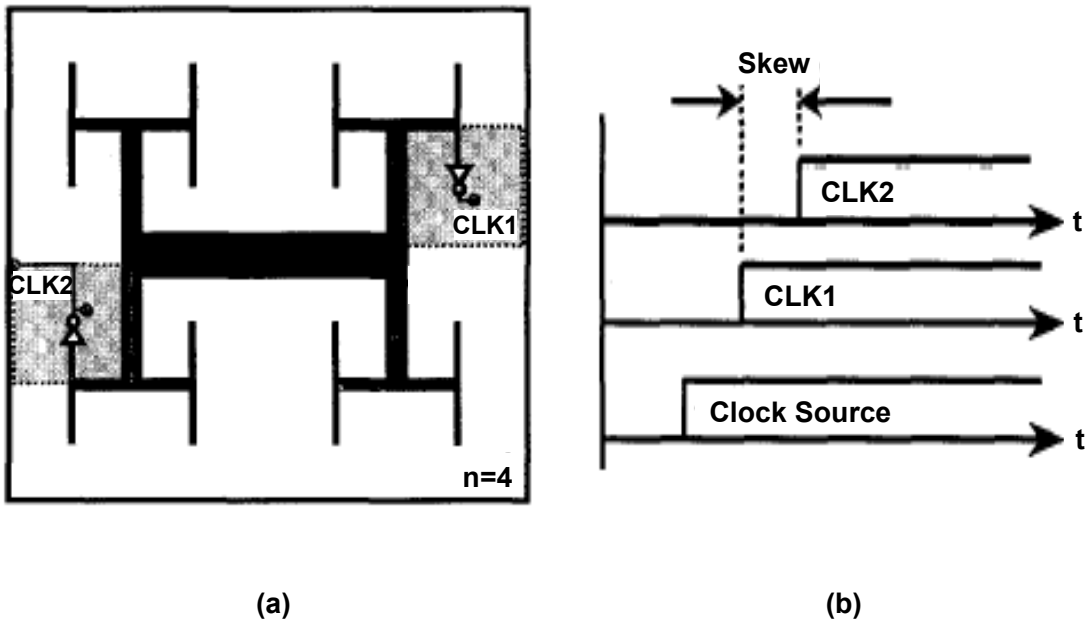


Figure 1.5 (a) Symmetric H-tree Structure (b) Clock Skew between the two points CLK1 and CLK2 [13]

The clock skew, T_{CLK}, can be expressed as [13],

$$T_{CLK}(V_{cc}) = 0.7 R_{tr} C_L \left(\frac{V_{cc}}{V_{cc} - V_T}\right) \cdot \left(\frac{\Delta V_{cc}}{V_{cc}}\right) \qquad (1.3)$$

where R_{tr} is the source-drain resistance of the driver, C_L is the load capacitance, V_T is the threshold voltage, and ΔV_{cc} is the power supply voltage variation. As can be seen from equation (1.3), a large power supply voltage fluctuation due to SSN results in increased clock skew, thus causing signal integrity problems.

1.3 Simultaneous Switching Noise due to Plane Bounce

All high frequency packages contain planes, which are used to supply power to the chips. A plane pair, which consists of two planes (say Vdd and Gnd) separated by an insulator, behaves as a cavity resonator at high frequencies. When circuits such as output drivers switch, they deposit a time varying charge on the Vdd and Gnd planes, which result in a displacement current source in the cavity. This current source excites radial electromagnetic waves in the cavity that reflect from the edges of the planes, causing multiple resonances in the cavity. Depending on the frequency response of the cavity, which can contain multiple resonances, the planes can bounce causing voltage fluctuations on the power supply rails of the chip. Plane bounce represents the variation of the potential difference between the voltage and ground nodes across the surface of the planes. This voltage variation is equivalent to the planes bouncing with time as compared to the DC level. This effect has been described in [3] where circuits in a microprocessor

core switch simultaneously. A method for modeling the simultaneous switching noise for output drivers driving transmission lines in a multi-layered package or board containing planes has been described in this dissertation.

In [14], the SSN in the package has been modeled by extracting an effective inductance L_{eff} for the power distribution. This approach is valid when SSN is dominated by the vertical inductance in the power distribution network. However, this modeling method can give erroneous results in future systems since it does not capture the distributed effects associated with planes. In [15], SSN has been modeled by an approach which models the vertical inductances. However, this method does not account for the reflection of the electromagnetic wave from the plane edges. Other approaches such as the one used in [16] model a quadrant of a chip, which once again neglects the reflection from the plane edges.

Since the planes support wave propagation by behaving as cavity resonators at high frequencies, both inductance and capacitance are necessary to model the propagation of waves between plane pairs. In addition, resistance needs to be included to account for the attenuation of propagating waves in the dielectric medium.

Thus, it is clearly necessary to develop an accurate and efficient modeling method, which can simulate SSN due to the reflection of electromagnetic waves from the plane edges by capturing the distributed effects associated with planes. Important issues for modeling SSN in high speed systems include the following:

- Planes play a critical role in modern power distribution systems (PDS) and therefore need to be modeled accurately to capture all the distributed effects.

- SSN needs to be simulated in the presence of non-linear drivers that drive transmission lines and other circuit components of the systems. Therefore, creating a circuit interface to planes is desired for simulation of simultaneous switching noise (SSN).

- The modeling method needs to demonstrate the stacking of planes and interconnects for modeling of high performance systems containing multi-layered planes in packages and boards.

- Return current of signal transmission lines has a dominant effect on SSN in high speed systems. Hence, return currents need to be analyzed correctly and accurately.

- SSN is also caused by discontinuities such as vias and splits on the planes. Their effects on SSN need to be captured, quantified and included for modeling SSN.

- The modeling method should be extendable to complex and realistic systems.

- Discrete decoupling capacitors are important components in a power distribution network. Their value, type and placement need to be optimized to enable the design of resonance free PDS.

- Various methods to reduce SSN need to be studied.

1.4 Proposed Research and Dissertation Outline

Based on the issues for modeling of SSN in high speed systems, the following research has been proposed in this dissertation.

1. Development of equivalent circuit models for solid plane pairs behaving as cavity resonators. In [17], [18], an analytical expression, which is a non-linear equation, has been used for modeling planes. This expression is good for numerical calculations, but is not well suited for circuit simulation where the planes have to be simulated with the rest of the electronics in a circuit simulator such as SPICE. For circuit simulations, a macromodel representing the plane behavior was used in [17]. An important issue in using macromodels is passivity, which can be difficult to guarantee for complex networks. Hence, in this dissertation a synthesis approach has been used for extracting an equivalent circuit directly from the analytical solution in [18]. The non-linear equation in [17], [18] has been linearized for this purpose, which requires the approximation of the losses in the circuit. The accuracy of the derived circuit model for planes has been evaluated by comparison with the analytical equation and its operation in the time domain has been studied. The circuit model has been expanded for the multi-port power/ground planes. The advantage of this circuit model is that it enables direct SPICE simulation of planes with other circuit components such as drivers, transmission lines, connectors, and vias, which is necessary for simulating SSN in a system.

2. Demonstration of an approach that enables the stacking of planes and interconnections under the assumption of no field penetration. Skin effect approximation has been employed and validated for the construction of circuit models for the multi-layered structure. The accuracy of the circuit model for the multi-layered planes has been verified by measurements in the frequency domain. This has been extended for attaching interconnections to planes. Using the circuit model developed for the multi-layered

planes, the voltage at port locations on the plane is allowed to vary with time, which is extremely important for the modeling of signal transmission lines over noisy reference planes.

3. Connection of non-linear driver models to the circuit models in SPICE for simulation of the waveforms and correlation with measurements on an active test vehicle. Transmission lines have been incorporated into the circuit models for the planes, to account for the return current effects. The SSN measured on the test vehicle has been analyzed in detail and the noise mechanism has been studied. It has been shown that SSN due to plane bounce is caused by the return currents on the planes. The propagation of energy into the lower layers even though the plane pairs are isolated through skin effect has been studied and quantified. The simulations of the quiet embedded stripline transmission lines have been used to show the amount of noise coupled to a quiet stripline that is referenced to a noisy power plane.

4. Effects of discontinuities on the planes and their role in SSN have been studied. Vias have a pronounced effect on SSN. A vertical current source due to the via transition can excite electromagnetic waves between planes. It has been shown that the return currents are responsible for plane bounce when signal lines, referenced to different planes, transition through a via. A method for including via effects in modeling SSN has been discussed. The modeling approach has been correlated with measurements, showing the validity of the method.

SSN caused by split planes, which are used in mixed signal systems, has been studied in detail. Split power planes with transmission lines traversing across the split

have been measured for SSN. Return current on planes generated by a transmission line crossing the split excites radial waves between the planes. This wave generates SSN on the split planes, which have been simulated and compared to measurements. In [19], a FDTD method has been used to analyze the voltage disturbance when a transmission line traverses a split. Though this method captures the slot line modes generated across the split, the method presented in this dissertation is more appropriate for modeling noise at the system's level.

5. Application of the modeling method to large systems. The modeling method presented in this dissertation has been extended and applied to large size systems containing packages on a printed circuit board. The SSN at all levels of assembly, i.e. chip/package/PCB structure, has been observed using the modeling method. It has been demonstrated that using the modeling method, a system can be modeled to simulate plane bounce and its effect on driver and receiver switching. It has also been demonstrated that an increase in the number of power balls results in less noise due to the smaller inductive path for the return currents.

6. Model to hardware correlation in a functioning system. A twenty-layered high speed CPU board from Sun Microsystems has been used for evaluating both core noise and I/O switching noise. The PDS for the core circuitry includes two 750 MHz microprocessors, heat sinks, a pair of core vdd/gnd planes and 195 decoupling capacitors attached to the core vdd/gnd planes. The PDS for the I/O driver circuitry includes 402 drivers, 402 transmission lines in eight layers, three pairs of I/O vdd/gnd planes and 178 decoupling capacitors attached to the I/O vdd/gnd planes. The transfer impedance of each

PDS has been measured in the frequency domain and the noise voltages on the functioning system have been measured both in the frequency and time domain. The modeling methods described earlier have been applied for the model to hardware correlation of these noise waveforms.

7. Placement and optimization of decoupling capacitors. The use of discrete decoupling capacitors enables the reduction of SSN. Thus, its location, value, and quantity need to be determined such that the overall impedance of the system meets the target impedance in the frequency domain, which will ensure the minimization of noise in the time domain. The goal of this research is to develop a methodology for the efficient placement and optimization of decoupling capacitor locations. The frequency characteristics of the PDS have been simulated using the modeling method described earlier to identify the resonant peaks in the impedance profiles. Two different types of resonances in the PDS have been discussed and optimum methods for selecting the decoupling capacitor locations have been discussed.

8. Suppression of SSN using discrete/embedded decoupling capacitors have been simulated and studied. The roles of discrete capacitor and embedded capacitor have been discussed and the noise reduction has been demonstrated through simulations on a test vehicle and functioning board. The importance of loss tangent has been studied and simulations have been conducted for different values of loss tangent to understand its effect on plane resonances.

The organization for the remainder of this dissertation is as follows. Chapter 2 describes the development of circuit models for planes and interconnects. In Chapter 3, the return current effects on SSN have been studied through the measurements on a test vehicle. The modeling method discussed in Chapter 2 has been correlated with measurements to show the validity of the method. In Chapter 4, SSN caused by via transitions and splits on planes has been measured on a test vehicle and modeled by using the modeling method discussed in Chapters 2 and 3. In Chapter 5, simulation of SSN in systems containing drivers and receivers has been presented. In Chapter 6, the modeling methodology has been applied to model the noise in a functioning computer system provided by Sun Microsystems. In Chapter 7, optimal locations for discrete decoupling capacitors on planes have been studied. In Chapter 8, the suppression of SSN using discrete/embedded decoupling capacitors have been studied. Finally, Chapter 9 provides the conclusions and future work for the continuation of this dissertation.

CHAPTER 2

Modeling of Planes and Transmission Lines

At high frequencies, conducting planes, which form an integral part of the power distribution system (PDS), support radial wave propagation. This is caused by the distributed effects of the planes which behave as transmission lines. In addition, when the vertical inductance effects are minimized, SSN is dominated by the return currents of the signal transmission lines, which flow on the planes [2], [21]. Hence, planes need to be modeled accurately. To enable the simulation of planes with the rest of the electronics in a system, interfaces to a circuit simulator are desired. Since high performance packages and boards are multi-layered, the models for planes should be extendable to multiple layers.

In this chapter, planes have been modeled by developing equivalent circuit models. Since the equivalent circuit is derived from an analytical solution that is positive definite, the circuit is guaranteed to be passive. The circuit models that have been developed have been extended for modeling of multi-layered structures. Models for the interconnects have been incorporated into the model for the planes to account for return currents. Using the circuit model developed for the multi-layered planes, the voltage at

port locations on the plane is allowed to vary with time, which enables the modeling of signal transmission lines over noisy reference planes.

2.1 Resonant Circuit for a Plane Pair

Figure 2.1 shows the structure of a plane pair which consists of two planes of dimensions *a* x *b*, separated by a dielectric of thickness '*d*' and permittivity 'ε'.

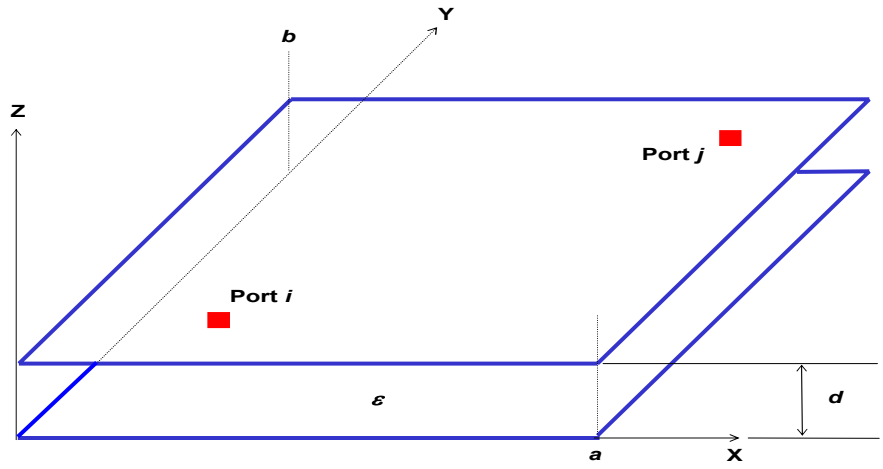


Figure 2.1 Plane Pair Structure [17]

With the assumption that $a,b >> d$ where $d << \lambda$ (the wavelength), which is true in all electronic packages including single chip and multi-chip modules, the impedance matrix Z at port locations on the plane can be derived as [17]

$$Z_{ij}(\omega) = j\omega\mu d \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} \frac{\varepsilon_n^2 \varepsilon_m^2}{(k_{mn}^2 - k^2)ab} f(x_i, y_i, x_j, y_j) \qquad (2.1)$$

where $$f(x_i, y_i, x_j, y_j) = (\cos\frac{m\pi x_i}{a}\sin c\frac{m\pi t_{xi}}{2a})\cdot(\cos\frac{n\pi y_i}{b}\sin c\frac{n\pi t_{yi}}{2b})$$

$$\cdot(\cos\frac{m\pi x_j}{a}\sin c\frac{m\pi t_{xj}}{2a})\cdot(\cos\frac{n\pi y_j}{b}\sin c\frac{n\pi t_{yj}}{2b})$$

In equation (2.1), (x_i,y_i) and (x_j,y_j) are the co-ordinates of the port locations, (t_{xi},t_{yi}) and (t_{xj},t_{yj}) are the dimensions of the ports with $k_{mn}^2 = (m\pi/a)^2 + (n\pi/b)^2$ where m, n are the propagating modes on the planes. The loss is included as a perturbation with the wavenumber k given by

$$k = k' - jk'', (k' >> k'') \qquad (2.2)$$

where

$$k' = \omega\sqrt{\varepsilon\mu}\,,$$

$$k'' = \omega\sqrt{\varepsilon\mu}(\tan\delta + \gamma/d)/2\,,$$

which is valid for low loss structures. Here '$\tan\delta$' is the loss tangent of the dielectric material and 'γ' is the skin depth for the conductors used in the circuit.

The analytical expression described in equation (2.1) is good for numerical calculations, but not well suited for circuit simulation where the planes have to be simulated with the rest of the electronics. For circuit simulations, a macromodel has been used in [17]. An important issue in using macromodels is passivity, which can be difficult to guarantee for complex networks. A method, that is compatible with the modeling methods for the rest of the power supply hierarchy and the device - namely, SPICE - has been used in this dissertation. To achieve this, an attempt to extract an equivalent circuit

directly from equation (2.1) has been made in this section. Substitution of equation (2.2) into equation (2.1) for k and assuming $k' >> k''$ results in the impedance equation (2.3) shown below [20], [21].

$$Z_{ij}(\omega) = \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} \frac{N_{mni} N_{mnj}}{j\omega C_{mn} + 1/j\omega L_{mn} + G_{mn}} \tag{2.3}$$

where

$$N_{mni} = \varepsilon_m \varepsilon_n \cos\frac{m\pi x_i}{a} \sin c\frac{m\pi t_{xi}}{2a} \cos\frac{n\pi y_i}{b} \sin c\frac{n\pi t_{yi}}{2b}$$

$$N_{mnj} = \varepsilon_m \varepsilon_n \cos\frac{m\pi x_j}{a} \sin c\frac{m\pi t_{xj}}{2a} \cos\frac{n\pi y_j}{b} \sin c\frac{n\pi t_{yj}}{2b}$$

$$C_{mn} = \frac{\varepsilon ab}{d}$$

$$L_{mn} = \frac{d}{\varepsilon ab(2\pi f_{mn})^2}$$

$$f_{mn} = \frac{\sqrt{(m/a)^2 + (n/b)^2}}{2\sqrt{\varepsilon\mu}}$$

$$G_{mn} = \frac{2\pi f C_{mn}}{Q}$$

$$Q = \frac{d\sqrt{\pi f \mu\sigma}}{1 + d\tan\delta\sqrt{\pi f\mu\sigma}}$$

Here f_{mn} is the resonance frequency of the structure and Q is the quality factor, which contains the dielectric loss and the conductor loss in the structure.

The above equation for the conductance G_{mn} is non-linear and dependent on the natural-frequency of the cavity. This equation for G_{mn} has been linearized by using the resonant frequency instead of the natural-frequency of the cavity to enable circuit synthesis, as shown below.

$$G_{mn} = \frac{2\pi f_{mn} C_{mn}}{Q_{mn}} \tag{2.4}$$

$$Q_{mn} = \frac{d\sqrt{\pi f_{mn} \mu\sigma}}{1 + d\tan\delta\sqrt{\pi f_{mn} \mu\sigma}} \tag{2.5}$$

The linearity in the variable 'f' has been obtained by assuming that the losses can be described by a tank circuit at resonance. Thus, based on the equation (2.3) with the linearized G_{mn}, the equivalent circuit can be implemented by using parallel resonant circuits and ideal transformers as shown in Figure 2.2.

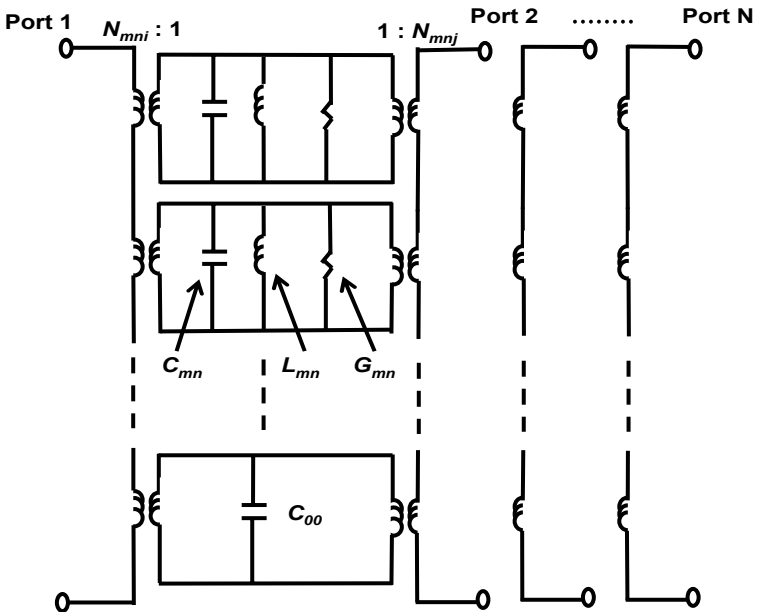


Figure 2.2 Equivalent Circuit for a Plane Pair

It is important to note that since each modal impedance in equation (2.3) is a representation of a passive circuit consisting of passive component, R, L and C in parallel, and the equivalent circuit in Figure 2.2 is constructed as a direct realization of this representation, the passivity in the original passive circuit response has been preserved.

This circuit model in Figure 2.2 is based on waveguide theory for the planes where the circuit characteristics in the vicinity of a resonant frequency can be expressed in terms of C, L and G parameters. Since the planes act as cavity resonators, the capacitor 'C' is used for storage of electric energy and the inductor 'L' for storage of magnetic energy, whereby at the resonant frequency, there is an exchange of energy between the two elements. The conductance 'G' is used to account for the losses in the circuit. Here, with m=n=0, the tank circuit is reduced to C_{00} which corresponds to the charging and discharging of the static capacitance of the planes. This mode can be called the zero-frequency resonant mode or electrostatic mode. Thus C_{00} represents the electrostatic capacitance of the structure. The information on the "port" is captured by N_{mni} and N_{mnj} which are the ideal transformer turn ratio for the port i and j, respectively. By connecting further external ports in parallel across the resonant circuit, the equivalent circuit for the multi-port structure can be represented as shown in Figure 2.2. The equivalent circuit in Figure 2.2 can be used to model the plane pair as a waveguide coupled to the various natural modes of the resonators through transformers.

To check the validity of the circuit model in Figure 2.2, a plane pair with length 20 inches and width 0.3 inch, as shown in Figure 2.3, has been modeled using the

equivalent circuit in Figure 2.2. The model uses a linearized representation for G_{mn} which has been simulated in SPICE for impedance calculations. The simulation results have been compared with the results from equation (2.1). The modes used for both calculations were $0 \leq m \leq 8$ and $n=0$. The insulator used was FR4 with a dielectric constant of 4.7 and a dielectric thickness of 4 mils. Figure 2.4 and Figure 2.5 show the input impedance at port 1 and transfer impedance between port 1 and port 2, respectively.

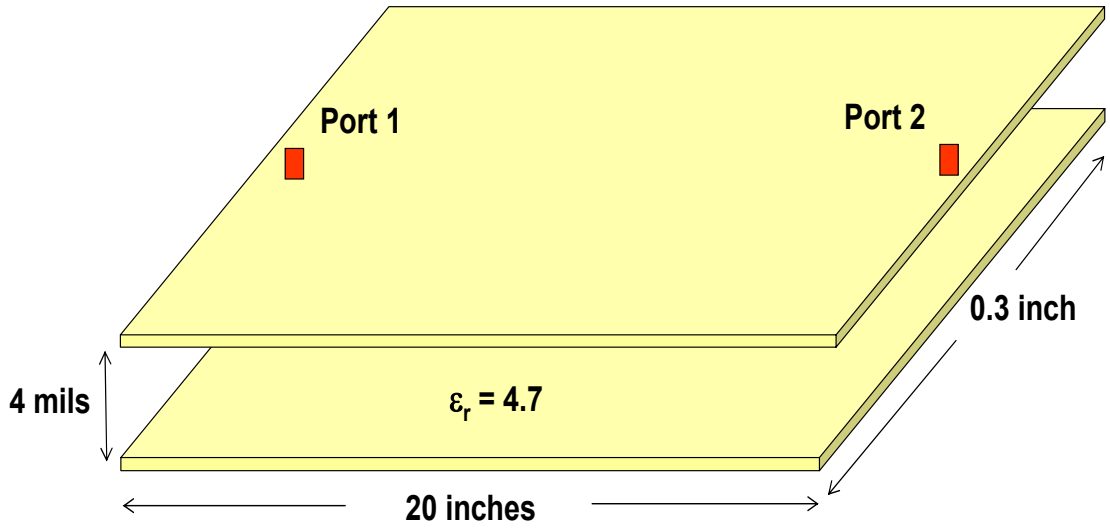
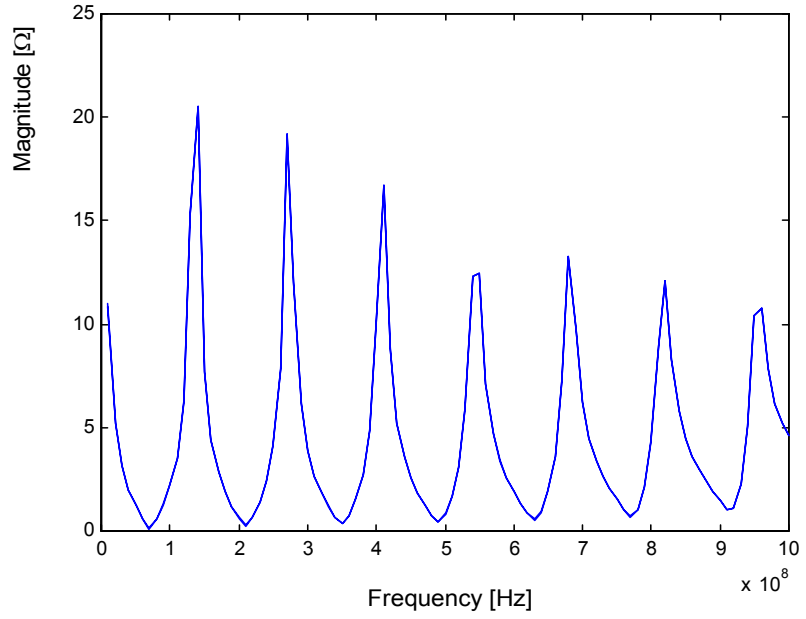
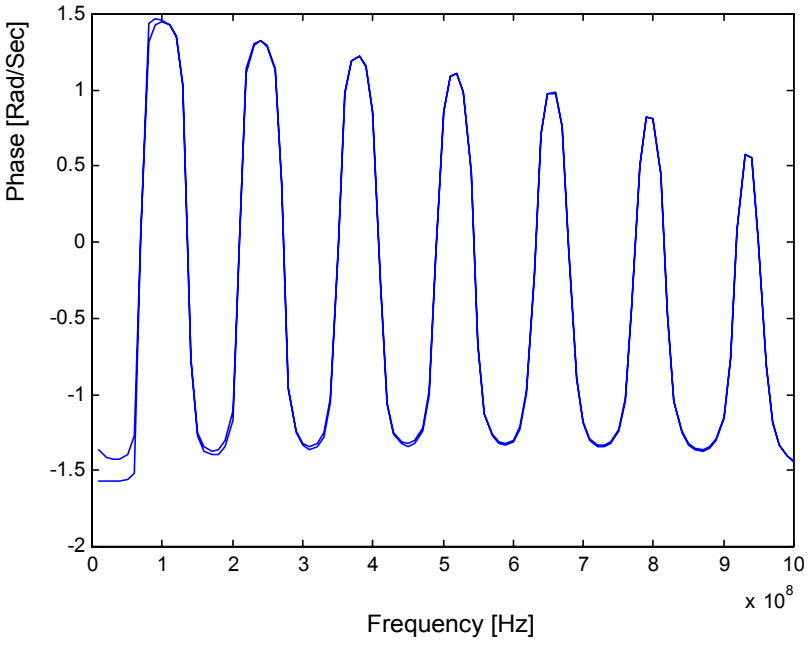


Figure 2.3 Plane Pair with Two Ports

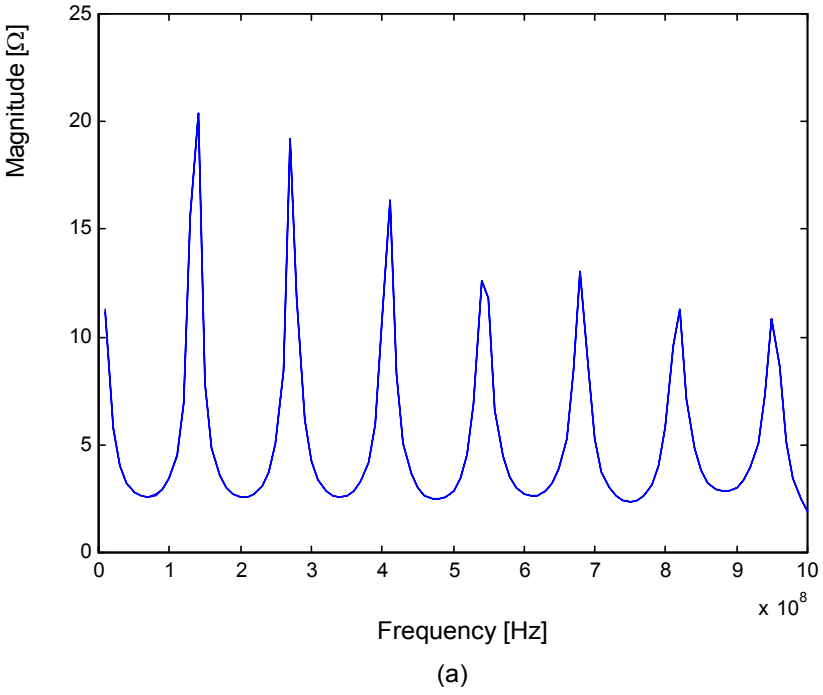


(a)

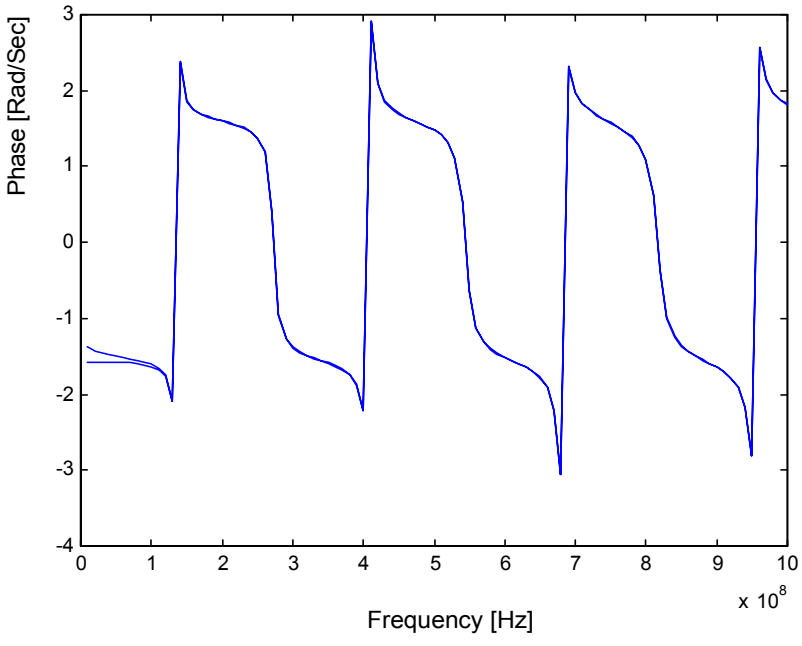


(b)

Figure 2.4 Input Impedance at Port 1, (a) Magnitude (b) Phase: Result from Equation (2.1) (Solid Line), SPICE Result using Circuit in Figure 2.2 (Dashed Line)



(a)

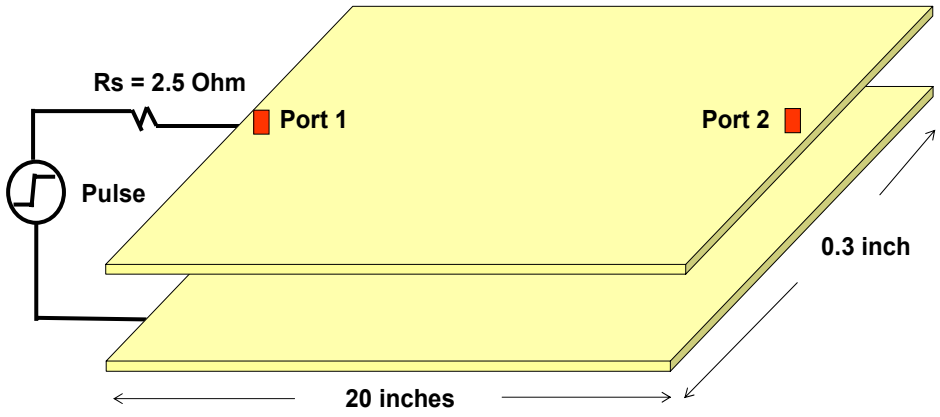


(b)

Figure 2.5 Transfer Impedance between Port 1 and Port 2, (a) Magnitude (b) Phase: Result from Equation (2.1) (Solid Line), SPICE Result using Circuit in Figure 2.2 (Dashed Line)

As shown in Figure 2.4 and Figure 2.5, the equivalent circuit in Figure 2.2 can be successfully used instead of equation (2.1). The small discrepancy in the phase at low frequencies is due to the absence of G_{00} in the circuit due to the linearization of equation (2.1). The importance of this resonant circuit model is that it enables the direct SPICE simulation of planes with other circuit components such as drivers, transmission lines, connectors, vias, etc, which is necessary for simulating noise in systems.

To better understand the operation of the circuit model in the time domain, a pulse voltage source of 1 ns rise time with a series 2.5 ohm resistor was applied to the structure in Figure 2.3, as shown in Figure 2.6 (a). The far end of the plane pair was left unterminated. Figure 2.6 (b) is the equivalent circuit for the structure.



(a)

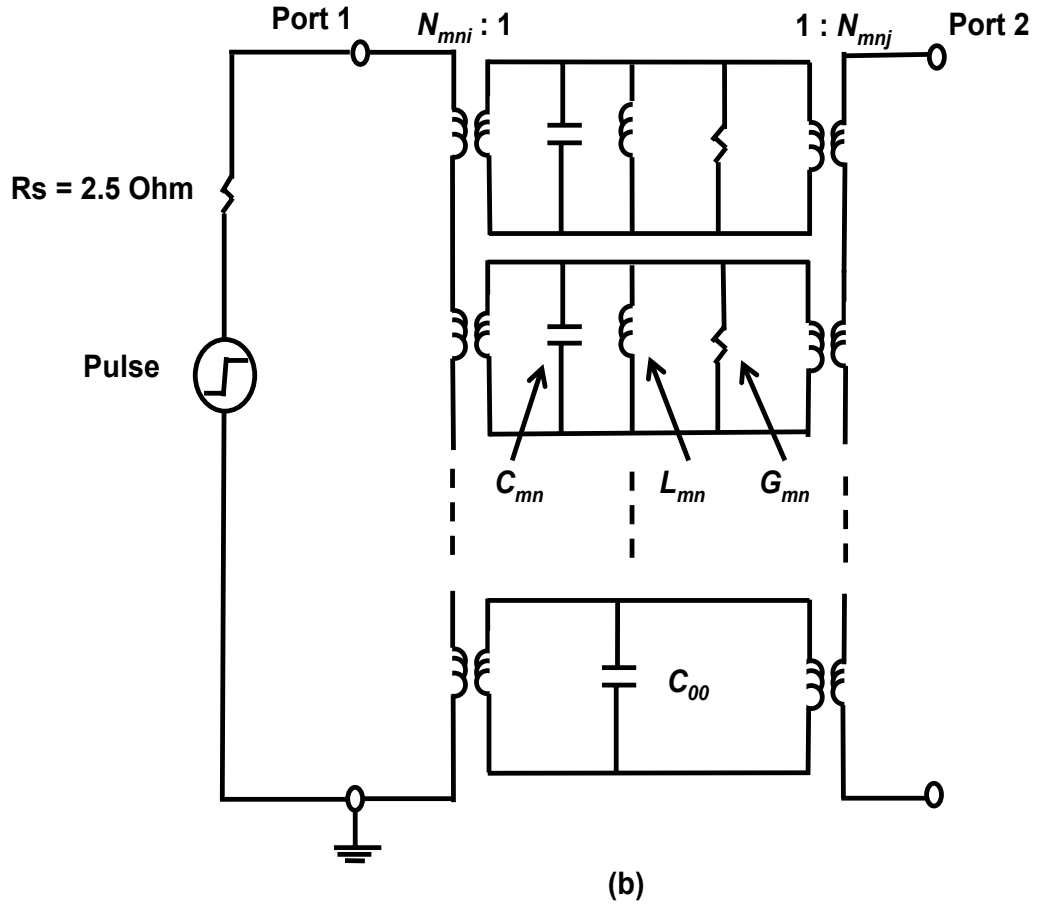
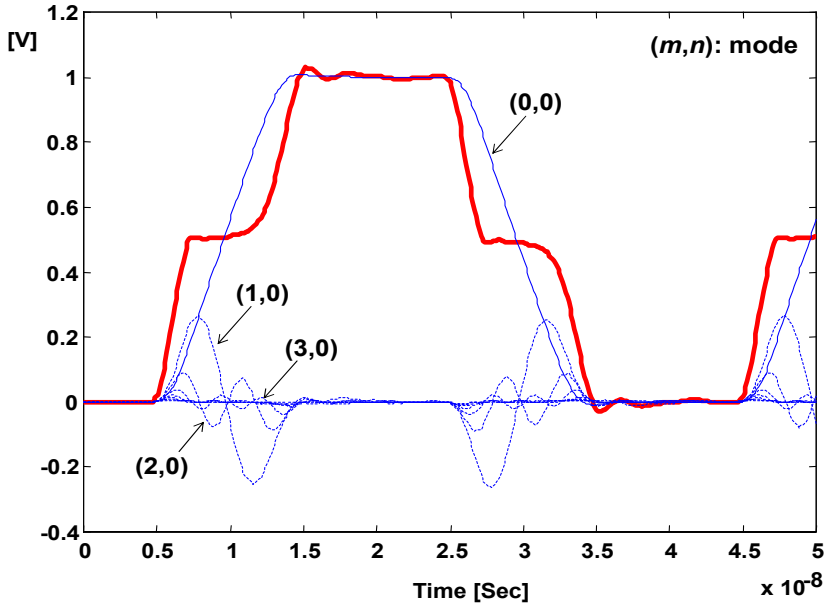
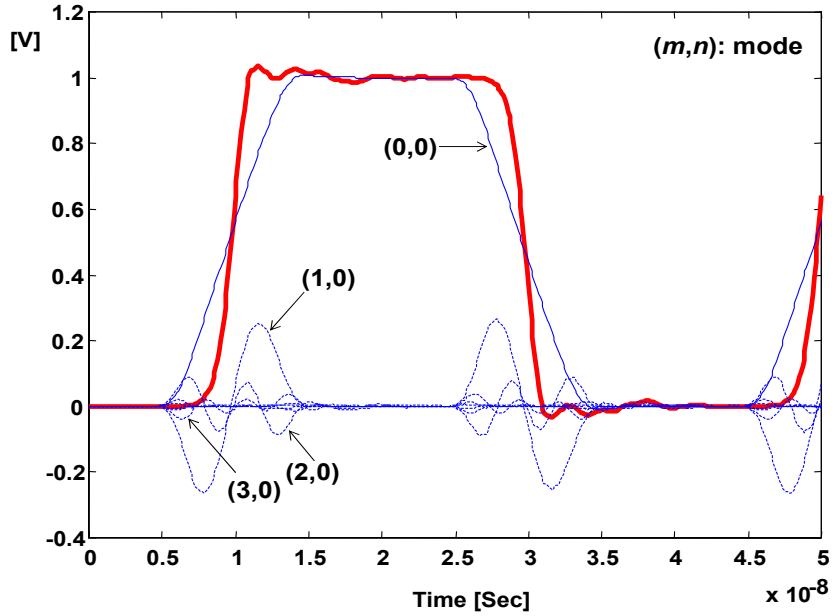


Figure 2.6 (a) Plane Pair with Pulse Source (b) Equivalent Circuit

Figure 2.7 (a), (b) are the SPICE simulation results for the near and far end waveforms of the plane pair. In addition, the voltages across each section of the transformer outputs have been displayed in Figure 2.7.



(a)



(b)

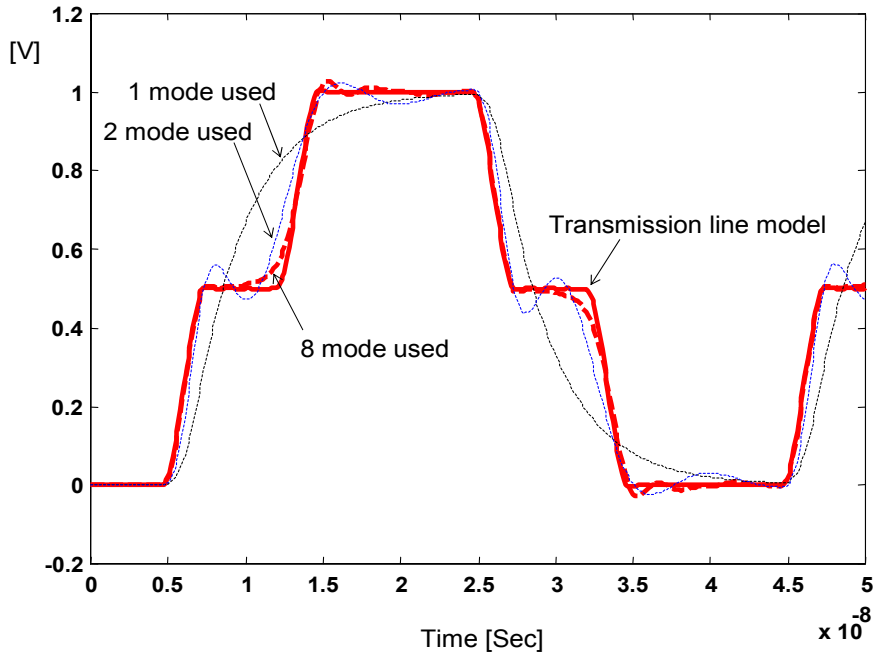
Figure 2.7 (a) Near End Waveforms: At Port 1 (Thick Solid Line), Transformer Output for Fundamental Mode (Thin Solid Line), Transformer Outputs for Other Modes (Dashed Line) (b) Far End Waveforms: At Port 2 (Thick Solid Line), Transformer Output for Fundamental Mode (Thin Solid Line), Transformer Outputs for Other Modes (Dashed Line)

The transformers are defined using the turn ratio 'N_{mni}' and 'N_{mnj}' in equation (2.3). These transformers are used to couple energy between ports. The transformers in series at any port is used to sum the voltages produced by the resonator circuit. The frequency of oscillation is defined by each resonator and the corresponding amplitude is accounted for by the transformer turn ratio. In Figure 2.7 (a), (b), the Fourier frequency components that are added together to form the near and far end port waveforms are very apparent. Hence, Figure 2.2 is equivalent to a circuit that simulates the transient response by summing the various Fourier components of the transient signal.

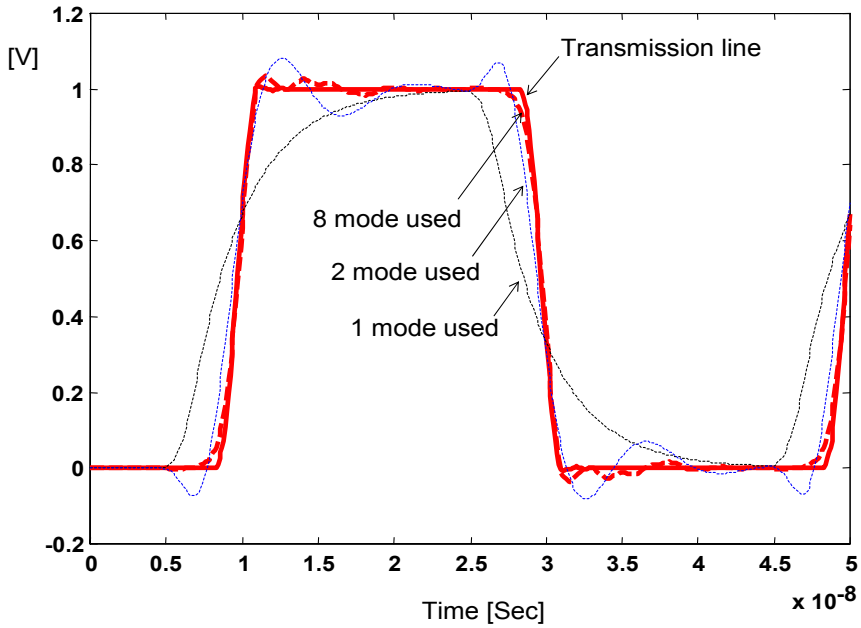
The plane structure in Figure 2.6 (a) behaves like a one-dimensional transmission line due to its long length and short width. The plane pair was modeled as a transmission line with characteristic impedance (Z_0) of 2.5 ohms and time delay of 3.671 ns. The circuit in Figure 2.6 (a) was simulated using the transmission line model in SPICE and compared with that of the resonant circuit model in Figure 2.8. The two simulations show good agreement. It is important to note that the resonant circuit model converges to the transmission line model as the number of modes are increased. It is also important to note that the resonant circuit model is guaranteed to be stable and passive.

2.2 Resonant Circuit for Multi-Layered Planes

In this section, a method is described that enables the stacking of planes for a multi-layered structure.



(a)



(b)

Figure 2.8 (a) Near End Waveforms at Port 1: Resonant Circuit Model (Thick Dashed Line), Transmission Line Model (Thick Solid Line) (b) Far End Waveforms at Port 2: Resonant Circuit Model (Thick Dashed Line), Transmission Line Model (Thick Solid Line)

Once the plane models are constructed, the interconnections and driver models can be connected to the planes using superposition, which has been explained in the next section. This method therefore combines electromagnetic theory with network theory to capture the ground bounce phenomena that occurs when output drivers switch simultaneously.

The stacking of planes is based on a skin effect approximation, which has been described in [3]. As an example, the skin depth for copper as a function of frequency is shown in Figure 2.9. As can be seen from the figure, the skin depth decreases as the frequency increases, with a depth of 2.1 microns at 1 GHz. As has been discussed in [22], [23], the waves that propagate between planes induce current densities on the planes that decay exponentially as they penetrate through the conductor. If the plane thickness 't' is larger than 3 γ, where γ is the skin depth (= $1/\sqrt{\pi f \mu \sigma}$), the plane layers can be completely decoupled by assuming small magnetic field penetration through the planes.

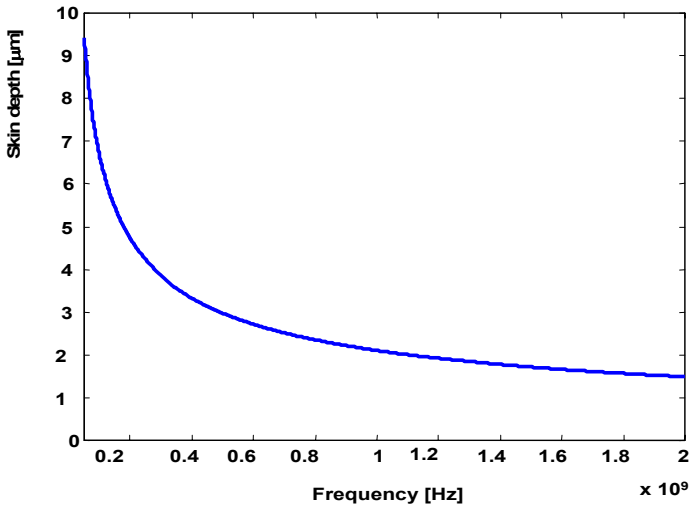
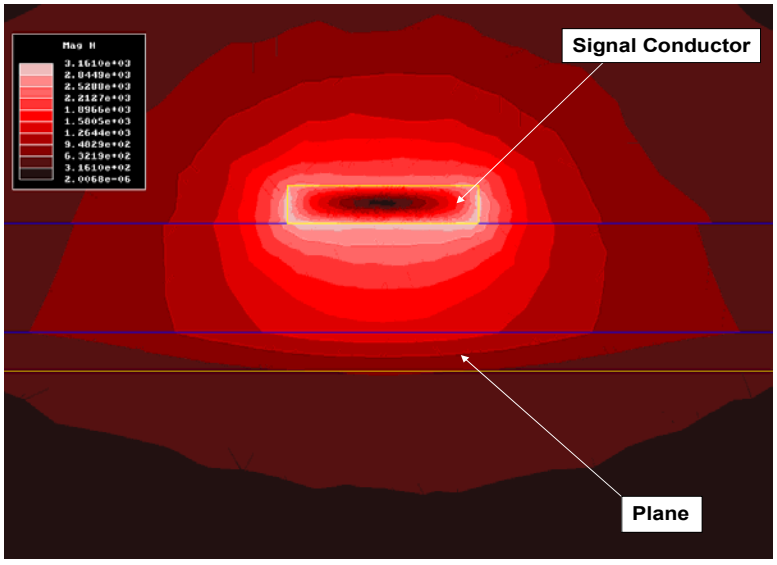
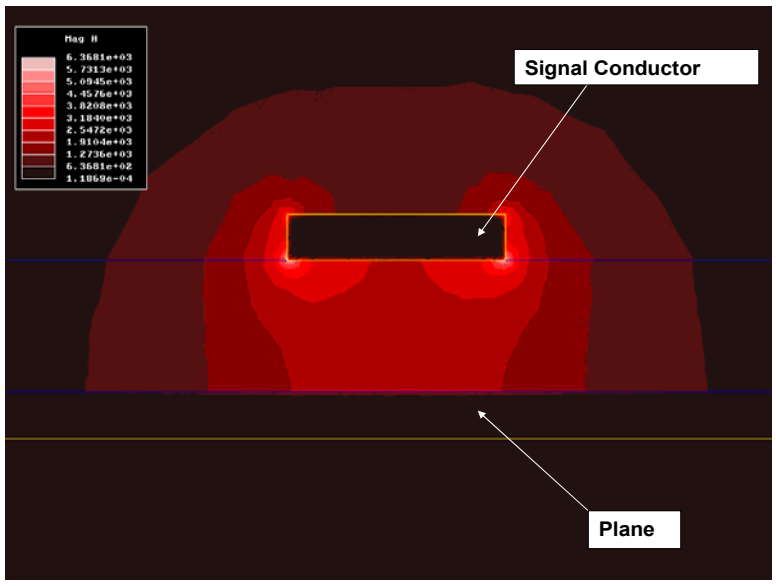


Figure 2.9 Skin Depth for Copper [22]

A microstrip transmission line structure was simulated using Ansoft software to see the effects of magnetic field penetration through the layers, as shown in Figure 2.10.



(a)



(b)

Figure 2.10 Magnetic Field Penetration: (a) f = 1KHz (b) f = 500 MHz

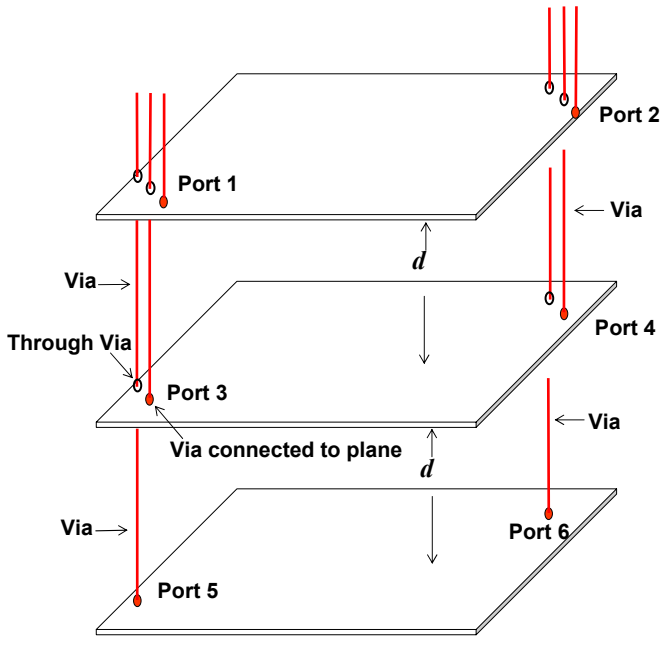
In the figures, the distribution and magnitude of the magnetic field over the cross-section of the structure is shown for the metal with thickness of 35 μm. Figure 2.10 (a) is for f = 1 KHz where the corresponding skin depth is 2087 μm. Since the plane thickness of 35 μm is much smaller than the skin depth, there is penetration of the magnetic field throughout the cross-section of the plane. This causes coupling between the plane layers through the solid metal conductor. For f = 500 MHz, the plane thickness of 35 μm is more than 10 times larger than the skin depth, which is 2.95 μm. Thus, the magnetic field penetrates only a small depth into the plane, as shown in Figure 2.10 (b). Hence, the coupling between plane layers is negligible at this frequency.

In addition, magnetic field penetration is a steady state effect that becomes dominant after many cycles for thin metallization layers. For thin metal layers, the maximum field penetration through the conductor occurs when the planes resonate, as described in [23]. This effect can be safely ignored if the thickness of the conductor is large compared to the skin depth at resonance and for transient simulations where the window of interest is around the rise time of the pulse.

Since SSN is a phenomenon occurring due to the transient switching of the drivers, the rise time is the parameter that has been used to evaluate the validity of the skin effect approximation. For the test vehicle used in this dissertation, the rise time is tr=12 ns. Using f_{3dB} = 0.35/tr, which corresponds to the 3 dB frequency, the corresponding skin depth is 12.237 microns at f=29.167 MHz. Since the copper thickness used was t=35 microns, which is ≈ 3γ, the skin effect approximation is valid. Based on this approximation, the plane layers and interconnection layers can be decoupled and

stacked using superposition. In high speed systems with very fast rise times, the skin effect approximation will be increasingly valid for thick conductors.

It is important to understand the flow of charge at a port where a via makes contact to a plane. For a good conductor, the electric field across the two surfaces of the conductor has to be zero. This is equivalent to having an instantaneous flow of charge through the plane cross-section where a via makes contact to the plane surface. Hence, based on this assumption, for the plane structure in Figure 2.11 (a), an equivalent circuit as shown in Figure 2.11 (b) can be constructed where a short-circuit has been used to connect the two plane surfaces at any port. In Figure 2.11 (b), the inductance of the via has been ignored, which can be included if necessary. This model can be readily extended to many layers.



(a)

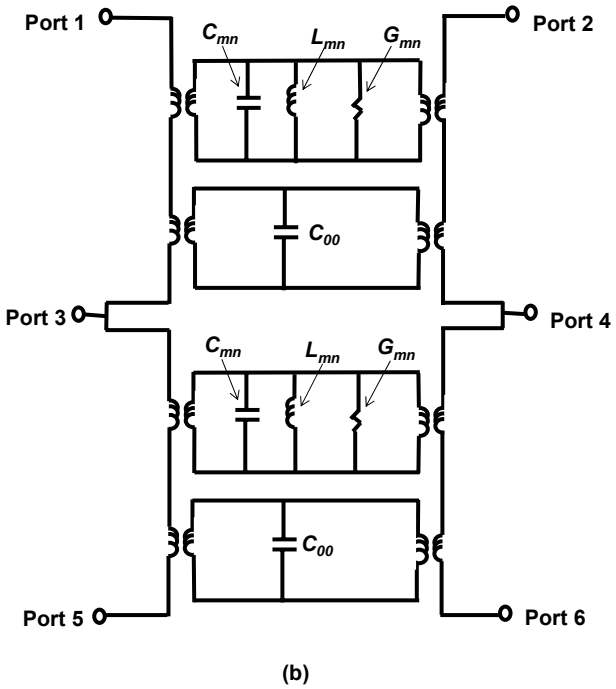


Figure 2.11 (a) Multi-Layered Plane Structure (b) Equivalent Circuit

In [3], equation (2.1) was used to compute the response of a multi-layered plane structure under the assumption that skin effect was dominant. The results were correlated with the coupled transmission line model (CTL) described in [24]. In this dissertation, since equation (2.1) has been linearized to equation (2.3) for constructing an equivalent circuit, the circuit model in Figure 2.11 (b) has been compared with [24] to verify accuracy.

The test structure consists of 3 planes with dimensions of 6 in x 4 in as shown in Figure 2.12.

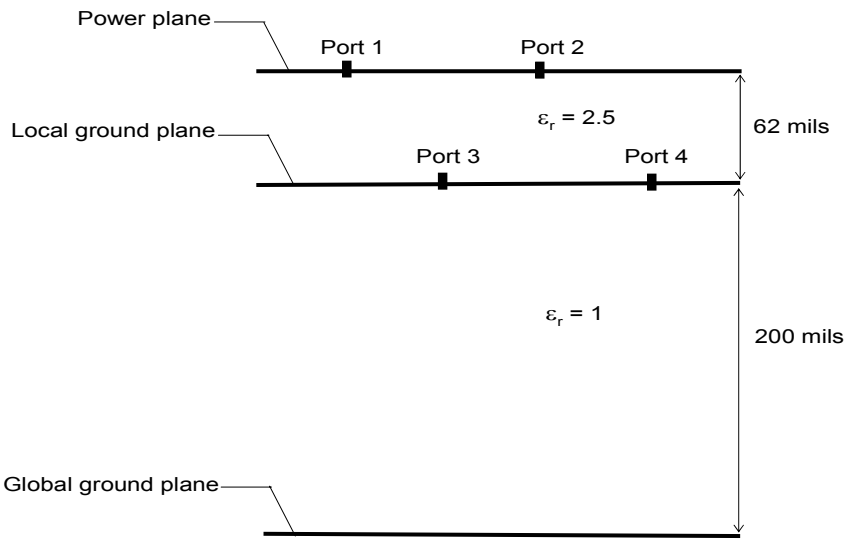


Figure 2.12 Test Vehicle from [24]

The separation between the power plane and the local ground plane is 62 mils with a relative dielectric constant $\varepsilon_r = 2.5$, and the separation between the local ground plane and the global ground plane is 200 mils with a relative dielectric constant $\varepsilon_r = 1$. Ports 1 and 2 are located at (x = 1 in, y = 3 in) and (x = 5 in, y = 1 in), respectively, on the power plane. Ports 3 and 4 are located at (x = 1 in, y = 1 in) and (x = 5 in, y = 3 in), respectively, on the local ground plane. Using the equivalent circuit in Figure 2.11 (b), and assuming two virtual ports on the local ground plane beneath port 1 and port 2 [3], the test structure can be modeled as shown in Figure 2.13. The comparison of the results between the model in Figure 2.13 and the measurement is shown in Figure 2.14 (a) and (b), demonstrating the validity of the equivalent circuit in Figure 2.11 (b) for modeling multiple layers. In Figure 2.14, the small discrepancy between the results can be attributed to the non-inclusion of via effects.

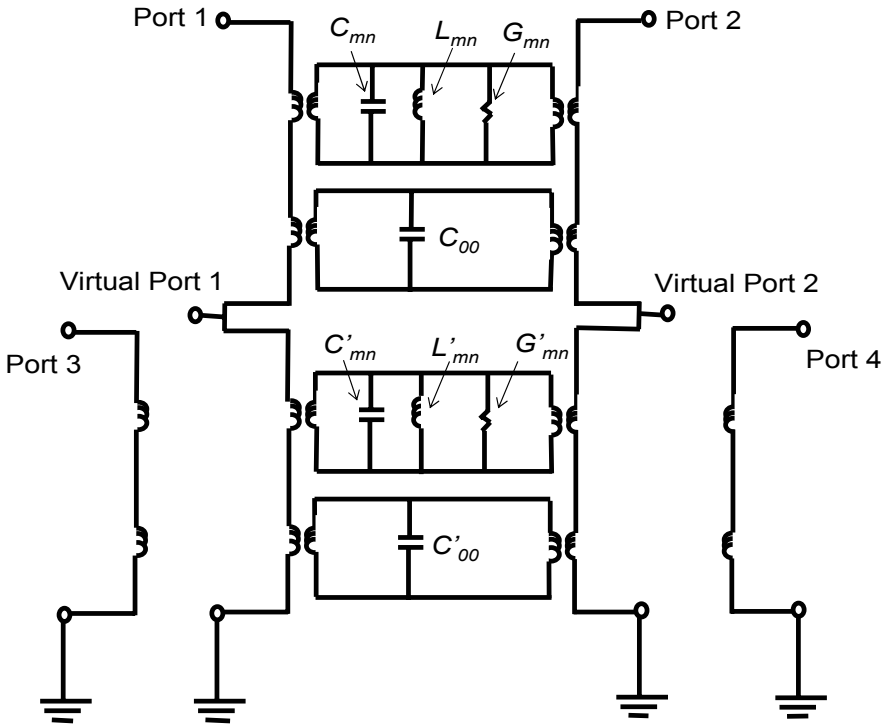
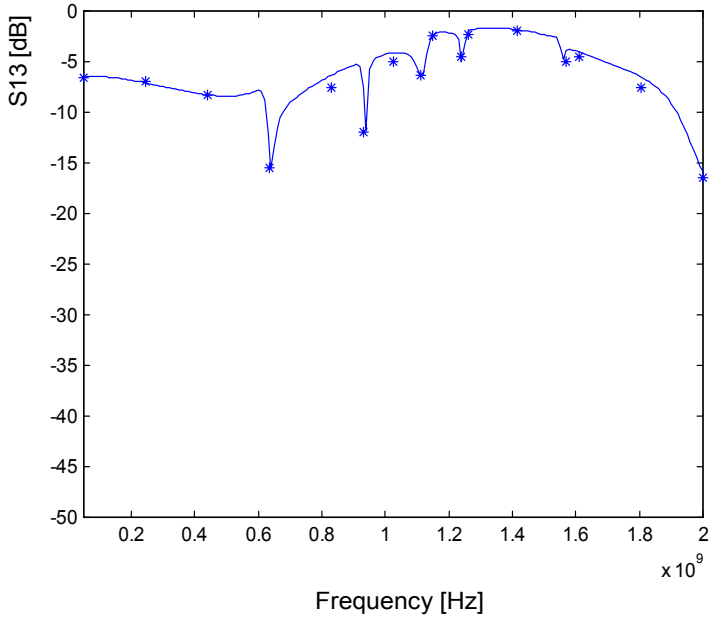
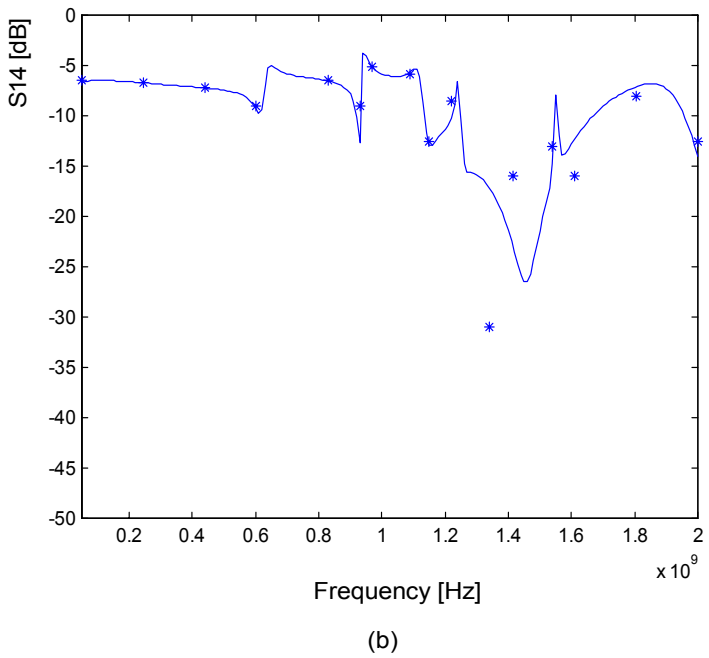


Figure 2.13 Model of the Test Structure in Figure 2.12



(a)



(b)

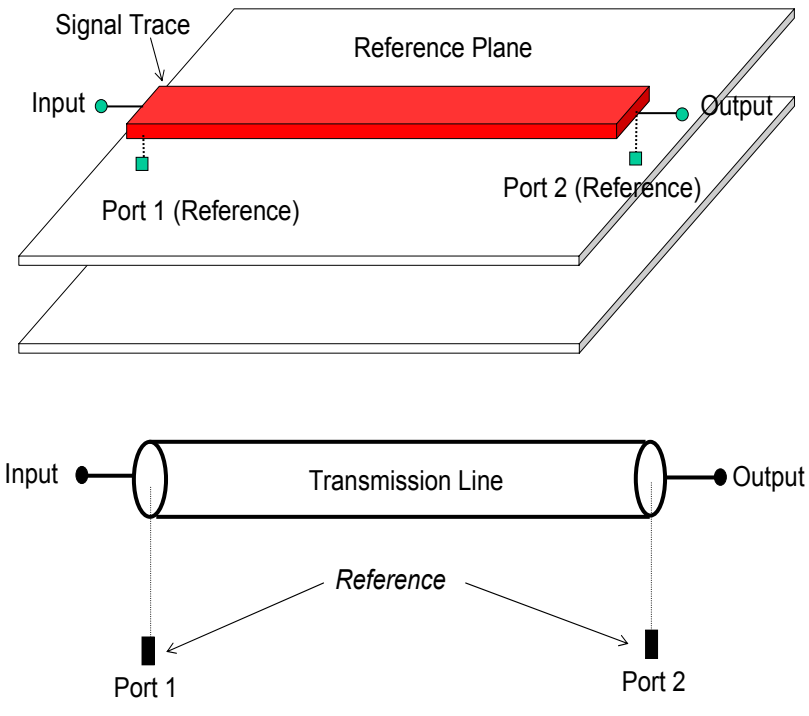
Figure 2.14 (a) Comparison of S13 between Result from Figure 2.13 (Solid Line) and Result from Measurement (*), (b) Comparison of S14 between Result from Figure 2.13 (Solid Line) and Result from Measurement (*)

2.3 Return Current

Return currents on planes cause the planes to bounce. When the signal transmission lines are incorporated into the plane models, the return current which occurs on the reference planes for the signal transmission line needs to be accounted for, correctly. The reference planes are not perfect and they bounce as return current accumulates and charges the parallel plate capacitance, causing waves to propagate between power and ground planes. In packages containing planes, the return current is on a reference plane that is in close proximity to the signal transmission line. This is because

at high speed, the return currents follow the path of least inductance, not the path of least resistance. The lowest inductance return path lies directly under a signal conductor, minimizing the total loop area between the outgoing and returning current paths [25].

To account for the return currents and using the skin effect approximation which is still valid for signal conductors, microstrip and un-symmetric stripline transmission lines can be modeled as in Figure 2.15 (a), (b), where the reference for the transmission line is the closest plane.



(a)

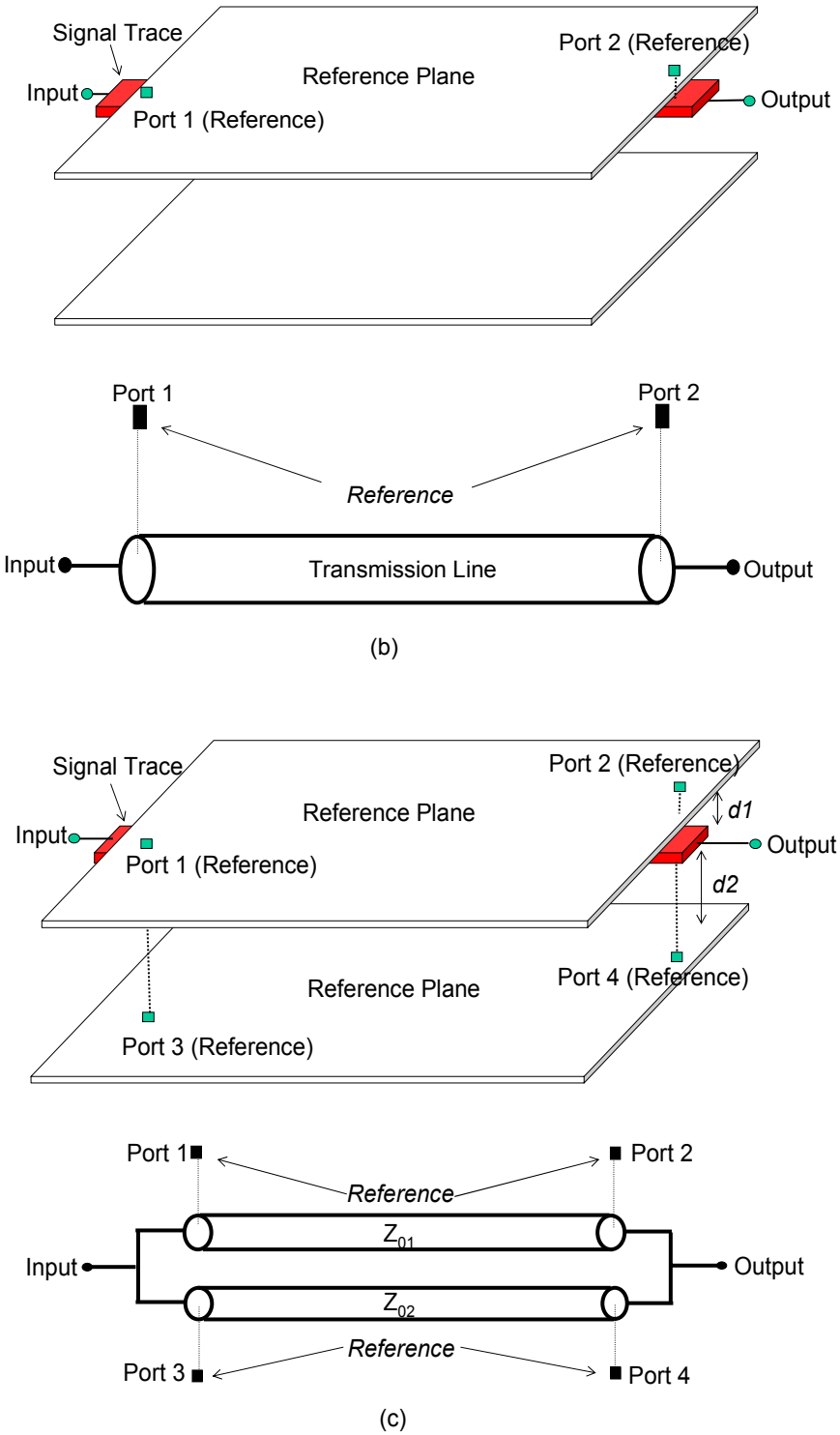


Figure 2.15 Transmission Line and Equivalent Circuit: (a) Microstrip Configuration (b) Un-symmetric Stripline Configuration-I (c) Un-symmetric Stripline Configuration-II

For a symmetric stripline, a similar approximation can be used by using two transmission lines in parallel, each with twice the impedance, referenced to the top and bottom planes. Figure 2.15 (b) is a case where the transmission line is very close to the top plane. Thus, the current on the signal trace makes reference to the nearest plane as shown in Figure 2.15 (b). The general case of an un-symmetric stripline transmission line with characteristic impedance of Z_0 is shown in Figure 2.15 (c). In the figure, *d1* is the distance between signal trace and top plane and *d2* is the distance between signal trace and bottom plane. Two transmission lines in parallel, each with a different impedance, can be used for referencing the top and bottom planes for the structure in Figure 2.15 (c). The characteristic impedances of the transmission lines are given by:

$$Z_{01} = Z_0 \frac{d1 + d2}{d2} \qquad (2.6.a)$$

$$Z_{02} = Z_0 \frac{d1 + d2}{d1} \qquad (2.6.b)$$

The model used in Figure 2.15 (a), (b), (c) ensures that the magnetic field produced by the signal line is contained between the transmission line and the corresponding plane, which is valid at high frequencies. Based on the structures in Figure 2.15 (a), (b), (c), the only information that is required to incorporate transmission lines into the plane models is a model for the transmission line and the position of the input and output reference ports on the planes obtained from the physical layout of the package or board. Irrespective of the physical routing of the interconnect, the only parameters needed for the transmission lines are its characteristic impedance, delay and frequency

dependent losses. The W-element model in HSPICE, which accounts for both the conductor and dielectric loss, has been used to model the transmission lines.

2.4 Superposition of Models with Planes and Interconnects

After constructing the models for multi-layered planes and interconnects, superposition theory based on the skin effect approximation can be used for combining the two models together. Models for other circuit components such as drivers, vias, and power supply can be incorporated into the models as shown in Figure 2.16, enabling the system level simulation of the noise waveforms in SPICE.

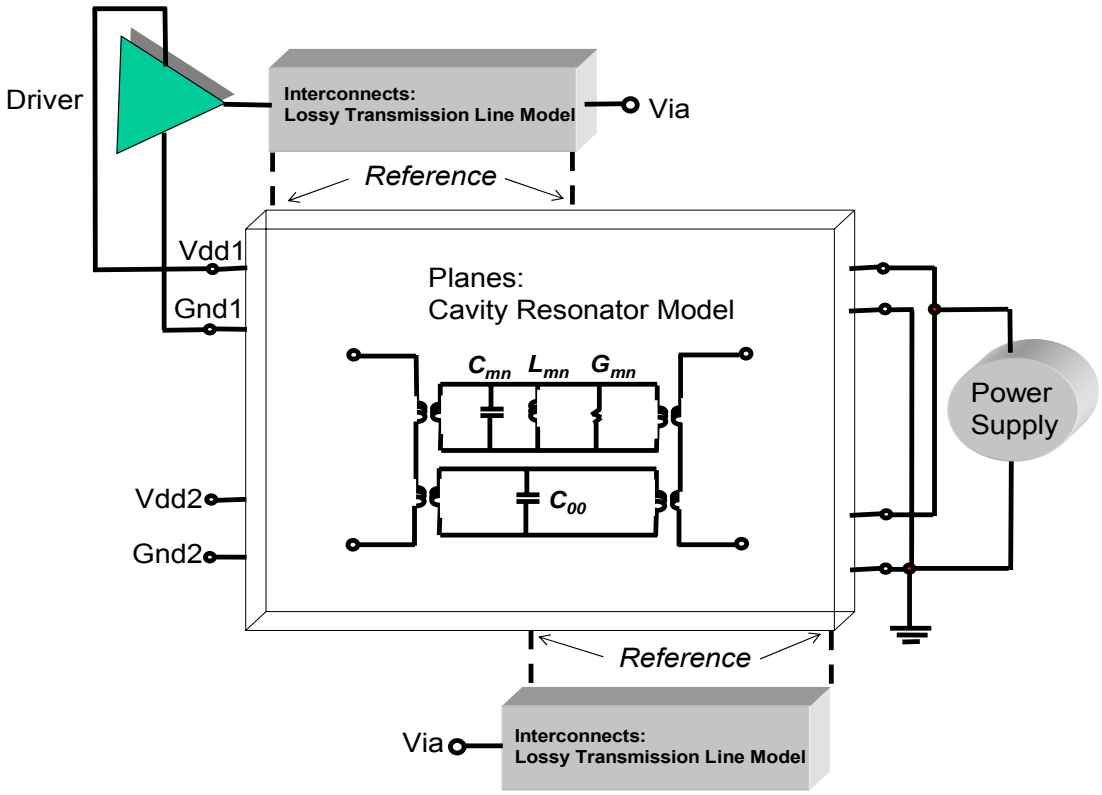


Figure 2.16 Superposition of the Circuit Models

2.5 Summary

In this chapter, equivalent circuit models for planes have been developed using a synthesis approach. The circuit model includes both inductance and capacitance for the modeling of wave propagation and resistance for the modeling of wave attenuation due to the losses in the medium. The circuit model for a single plane pair has been extended for the modeling of multi-port, multi-layered power/ground planes. The accuracy of the circuit model has been verified by comparison with measured data for multi-layered structures. The model for the interconnects has been incorporated into the model for the planes using superposition based on the skin effect approximation. By using the modeling method discussed in this chapter, the voltage at port locations on the plane is allowed to vary with time. Hence, signal transmission lines referenced to noisy power/ground planes can be modeled accurately, using the method discussed in this chapter.

CHAPTER 3

Plane Bounce from Return Currents

SSN has become a major bottleneck in high speed digital design. For future systems, modeling SSN can be complex due to the thousands of interconnects that need to be analyzed. This is because a system level modeling approach is necessary that combines the chip, package, and board level interactions. The major problem with simultaneous switching noise in high speed systems is the managing of return currents that flow on the reference planes. The return currents of the signal transmission lines flow on the reference planes, which are not perfect, causing the planes to bounce. Plane bounce represents the variation of the potential difference between the voltage and ground nodes across the surface of the planes, which is equivalent to the planes bouncing with time as compared to the DC level. This effect could become very important in high speed systems for estimating the fluctuations on the chip power supply. The modeling methods for planes and interconnections described in Chapter 2 can be used for modeling plane bounce since it accounts for the return current on the planes accurately.

In this chapter, return current effects on SSN has been analyzed through experiments on an active board. Simulations using the modeling method discussed in Chapter 2 have been correlated with measurements.

3.1 Test Vehicle

A test vehicle was designed and measured to verify the validity of the modeling method discussed in the previous chapter. Figure 3.1 shows the test vehicle consisting of planes, transmission lines and non-linear drivers.

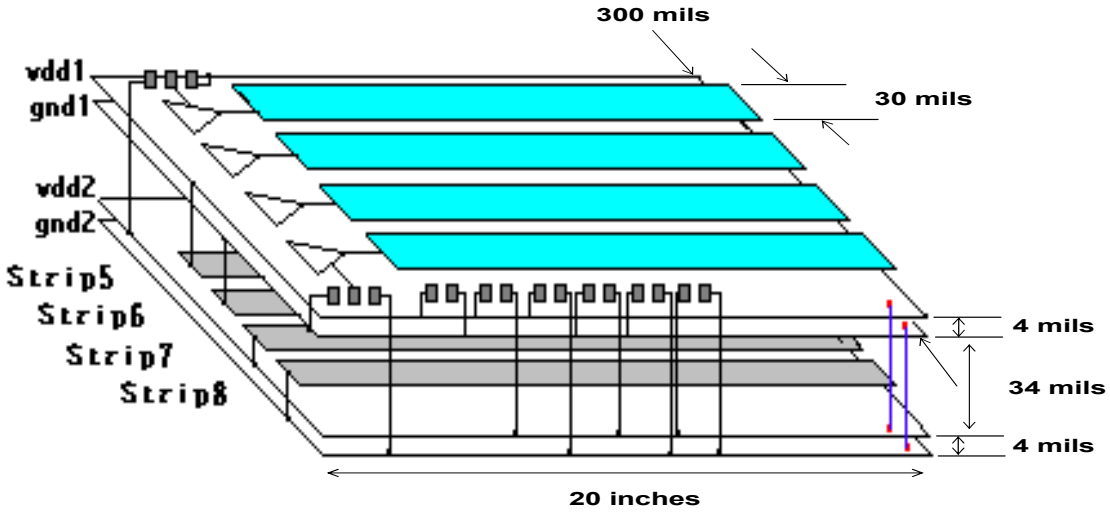


Figure 3.1 Test Vehicle for SSN Measurement

The test vehicle in Figure 3.1 is a seven-layered board with interconnections consisting of four very wide microstrip transmission lines with characteristic impedance Z_0 = 22 ohms. They are about 20 inches (50 cm) long and driven by a Texas Instruments ABT244 buffer driver. The power and ground planes are 0.3 inch (7.6 mm) wide and similar in length to the transmission lines. The stackup of the test vehicle includes 4 power planes and 3 signal layers in the order: sig1/Vdd1/Gnd1/sig2/sig3/Vdd2/Gnd2. The separation is 4 mils of FR4 material between all copper layers except sig2 and sig3 where the separation is 24 mils. Four silicon drivers are located on the left side of the test vehicle in a 20 pin DIP package. They were powered from Vdd1 and Gnd1 planes, using

vias. Two sets of 50 ohm stripline transmission lines were embedded between Gnd1 plane and Vdd2 plane. Layer sig2 is one set of striplines which is closer to the Gnd1 plane and layer sig3 is the other set (designated Strip5, Strip6, Strip7, Strip8), which is closer to the Vdd2 plane. The two power planes and two ground planes were not connected on the left side of the test vehicle, which enables independent voltage measurements between the 4 planes. Both Vdd planes and Gnd planes were connected together on the right side of the test vehicle.

A power supply of 5 volts was applied at the right side of the test vehicle to power up the structure and the noise was monitored in the vicinity of the driver, when the drivers transitioned. The measurement was done for two experimental conditions, namely, 1) when the far end of the microstrip transmission lines were open and 2) when the far end of the microstrip transmission lines were terminated to both Vdd and Gnd planes using 43 ohm resistors. The power supply noise measured at the driver was captured using a TDS 794D oscilloscope. Figure 3.2 shows the measurement setup.

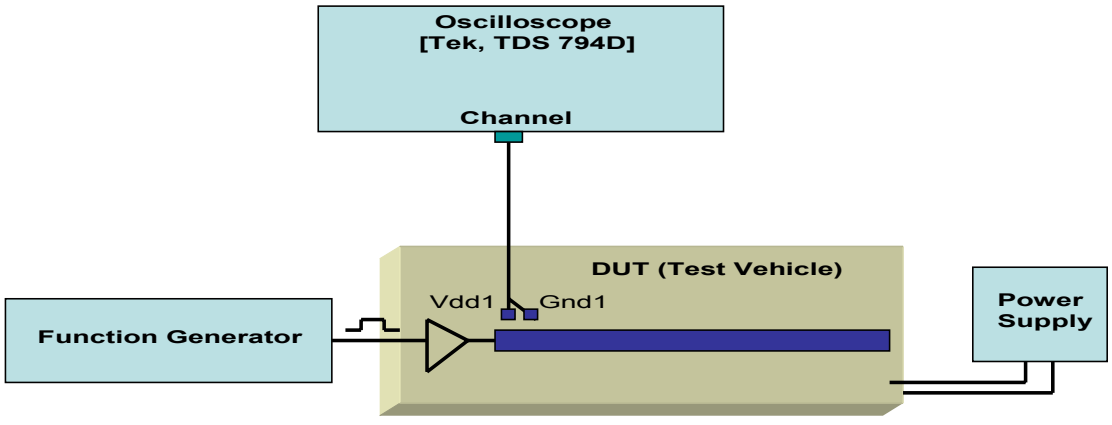


Figure 3.2 Measurement Setup

The noise voltages measured near the drivers were 1) voltage between Vdd1 and Gnd1 (differential voltage PP1), 2) voltage between Vdd2 and Gnd1 (differential voltage PP2), 3) voltage between Vdd2 and Gnd2 (differential voltage PP3). The voltage at the far end of the embedded stripline transmission lines was also simulated. These striplines were connected to each of the power planes on the left side of the board to monitor the propagated noise. Strip1 through Strip4 were right below Gnd1 plane and they were connected to each of the power planes on the left side of the board, i.e. Strip1 to Vdd1 plane, Strip2 to Gnd1 plane, Strip3 to Vdd2 plane, and Strip4 to Gnd2 plane. Strip5 through Strip8 were right above Vdd2 plane and they were also connected to each of the power planes on the left side of the board, i.e. Strip5 to Vdd1 plane, Strip6 to Gnd1 plane, Strip7 to Vdd2 plane, and Strip8 to Gnd2 plane. They were terminated to Gnd planes with 50 ohm resistors on the right side of the board. The purpose of these striplines was to sense the voltage of the power plane on the left side of the board and propagate that signal to the right side of the board. These striplines carry signals with respect to the nearest power plane. The amount of noise coupled to quiet striplines that are referenced to noisy power planes can be measured using this structure.

As stated in [2], [21], the SSN problem has shifted from an inductance problem to a plane bounce cavity problem. For multi-layered structures containing planes, the return current from the transmission lines on the planes contributes significantly to the plane bounce. This effect has been captured in the test vehicle and has been described in later sections.

3.2 Plane Bounce with Microstrip Transmission Line Unterminated

Consider the waveform in Figure 3.3 which was measured when the microstrip transmission lines were unterminated.

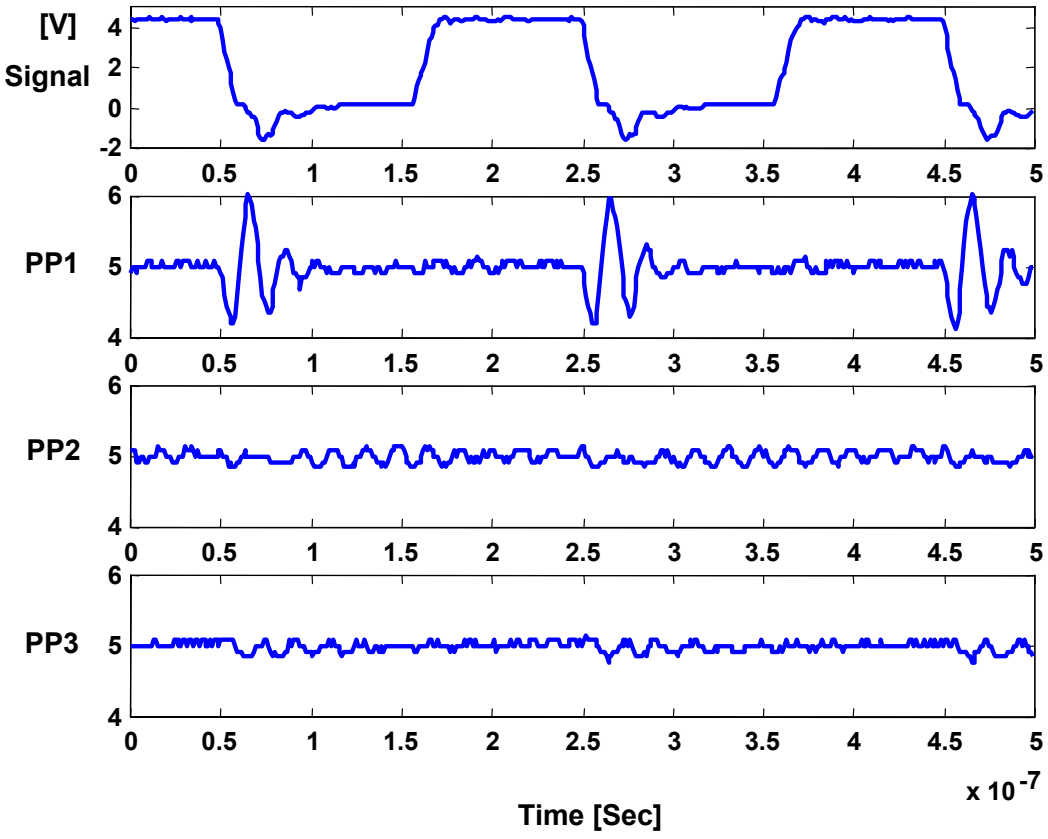


Figure 3.3 Measurement Results: No Termination PP1: Voltage Difference between Vdd1 and Gnd1, PP2: Voltage Difference between Vdd2 and Gnd1, PP3: Voltage Difference between Vdd2 and Gnd2

The noise occurs during the high to low transition of the drivers and very little noise occurs during the low to high transition. This can be explained based on the return

currents. When the transition is from low to high, the driver connects the Vdd1 plane to the transmission line through a small resistor R_{on1} in Figure 3.4.

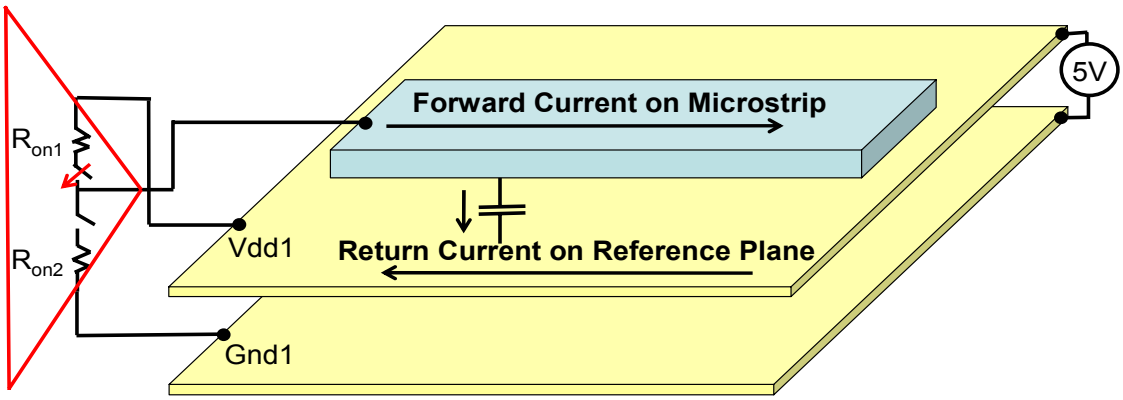


Figure 3.4 Low-to-High Transition: No Termination

Current flows into the transmission line and the return current flows on the Vdd1 plane. The current loop is completed through the Vdd1 plane, the driver resistance, the transmission line and the capacitance between the transmission line and the Vdd1 plane, as shown in Figure 3.4. Since the Gnd1 plane is not a part of the current loop, this does not excite any wave between the Vdd1-Gnd1 planes. However, when the transition is from high to low, the driver connects the transmission line to Gnd1 plane through a low impedance path R_{on2} in Figure 3.5.

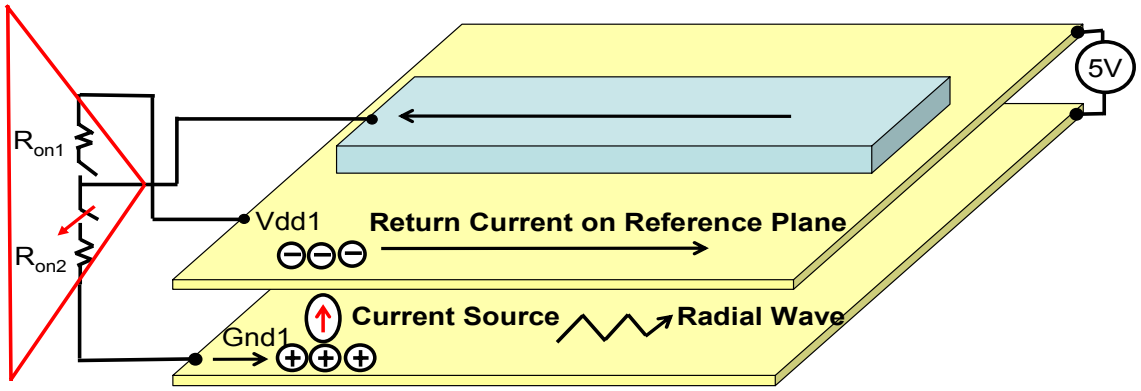


Figure 3.5 High-to-Low Transition: No Termination

Since the transmission line is initially charged to Vdd1 potential, the signal current flows out of the transmission lines through the driver and into the Gnd1 plane, causing a deposition of positive charge. On the Vdd1 plane, the current leaves the vicinity of the driver as return current, leaving behind negative charge, as shown in Figure 3.5. This causes the accumulation of charges with opposite polarities on the planes in the vicinity of the driver. Since the charges vary with time, they are equivalent to a displacement current source, as shown in Figure 3.5. The current source excites a radial wave between the planes that bounces off the edges of the planes, causing the planes to bounce.

3.3 Plane Bounce with Microstrip Transmission Line Terminated

Consider the test case when the microstrip transmission lines are terminated with two 43 ohm resistors connected to both Vdd and Gnd planes on the right side of the test vehicle. This results in a different waveform, as shown in Figure 3.6.

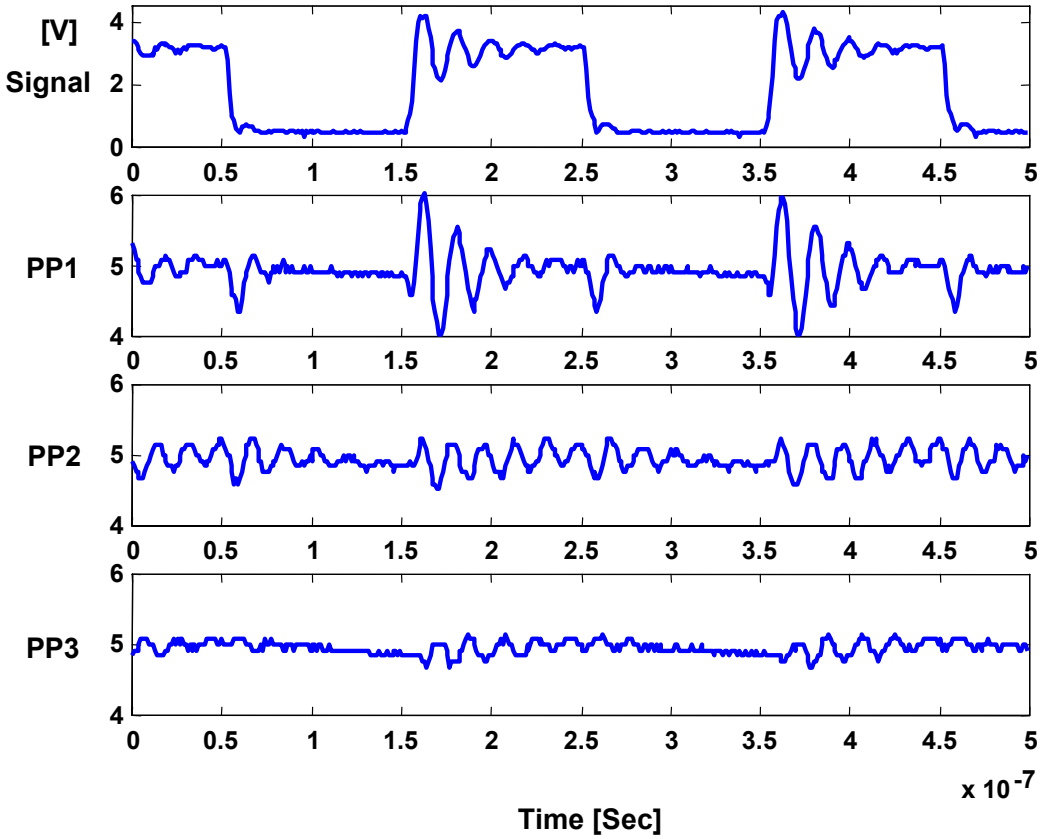


Figure 3.6 Measurement Results: With Termination PP1: Voltage Difference between Vdd1 and Gnd1, PP2: Voltage Difference between Vdd2 and Gnd1, PP3: Voltage Difference between Vdd2 and Gnd2

The maximum noise now occurs during the low to high transition instead of the high to low transition. This is due to the initial conditions on the transmission lines. Consider the initial condition when the driver is in the low state. Through the 43 ohm

resistors, the current flows from the power supply on the right side of the test vehicle and down the 22 ohm microstrip transmission line. The pull-down device in the driver conducts the current to the local ground where it is returned back to the right side of the test vehicle through the Gnd1 plane, as shown in Figure 3.7.

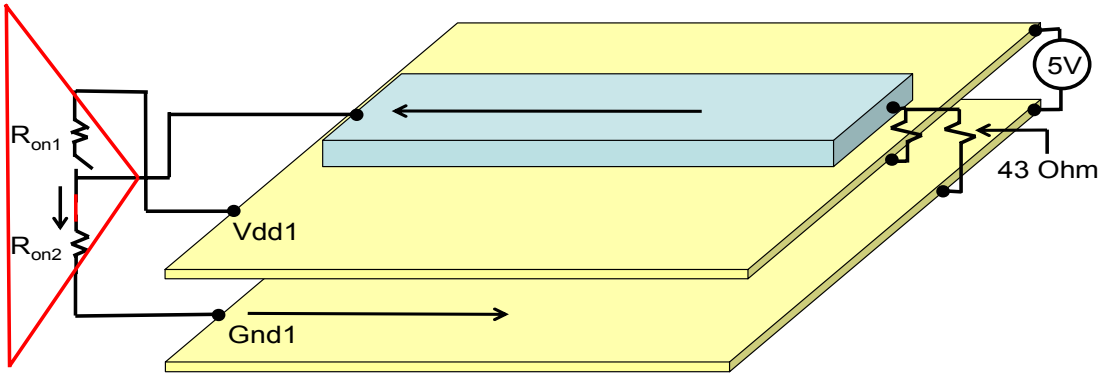


Figure 3.7 Initial Condition prior to Low-to-High Transition: With Termination

The Vdd1-Gnd1 planes are charged with the ground current. With these initial conditions, the driver makes a low to high transition. When the pull-down device in the driver becomes high impedance, the initial current loop is opened. The current continues to leave the ground node of the driver, leaving negative charge. Simultaneously the pull-up device connects the Vdd1 plane to the transmission line, causing the deposition of

positive charge on the Vdd1 plane near the Vdd node of the driver, as shown in Figure 3.8.

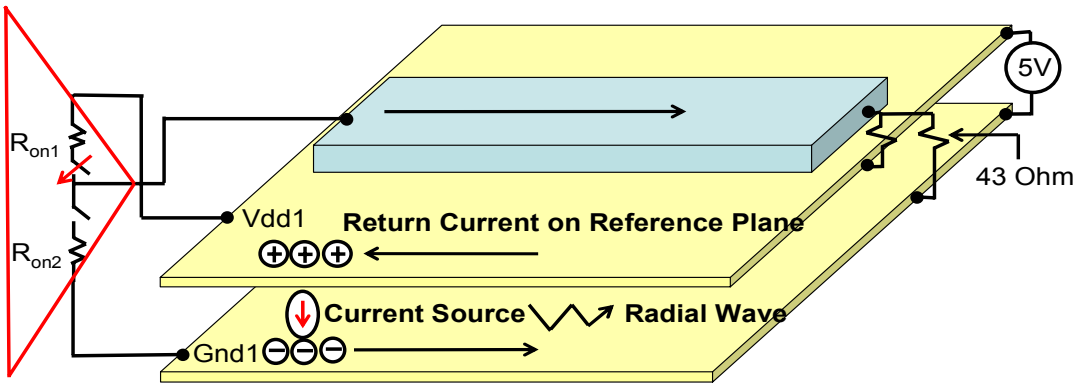


Figure 3.8 Low-to-High Transition: With Termination

The accumulation of charges near the driver acts like a displacement current source, exciting a disturbance between the Vdd1-Gnd1 plane, which causes the planes to bounce. It is important to note that the direction of the current source is opposite to the prior test case. This explains the opposite noise pattern for the two test cases. For the 22 ohm transmission line, since it is already pre-charged, no pull-up device is necessary in the driver for the first several ns. Current coming down the transmission line snaps the driver output high without any aid from the driver. When the transition is from high to

low, the phenomenon occurring is similar to the prior test case. Hence, similar noise waveforms are observed.

Both the measured results in Figure 3.3 and Figure 3.6 show that the noise occurs in the lower plane pairs, namely, Vdd2/Gnd1 and Vdd2/Gnd2 plane pairs. The time of flight along the length of the board is 3-4 ns. The noise on the lower plane pairs occurs immediately when the drivers switch, not one or two time of flight later. This is caused by the static capacitance between the planes. The capacitors behave as a voltage divider circuit causing the instantaneous propagation of energy into the layers below. The propagation of energy into the bottom plane pairs causes the excitation of radial waves, resulting in plane bounce.

In the next section, the simultaneous switching noise was simulated by modeling the power planes and transmission lines using the equivalent circuits described in the earlier sections and the correlation with measurements have been demonstrated.

3.4 Model to Hardware Correlation

Based on the discussion in the previous sections, the test vehicle was modeled as shown in Figure 3.9. In the figure, only the microstrip transmission lines are shown and the striplines have been excluded for clarity.

In the circuit, the microstrip transmission line is referenced to the planes as described in Figure 2.15 (a). The circuit model in Figure 3.9 has been simulated in HSPICE by attaching non-linear drivers and compared to measured results.

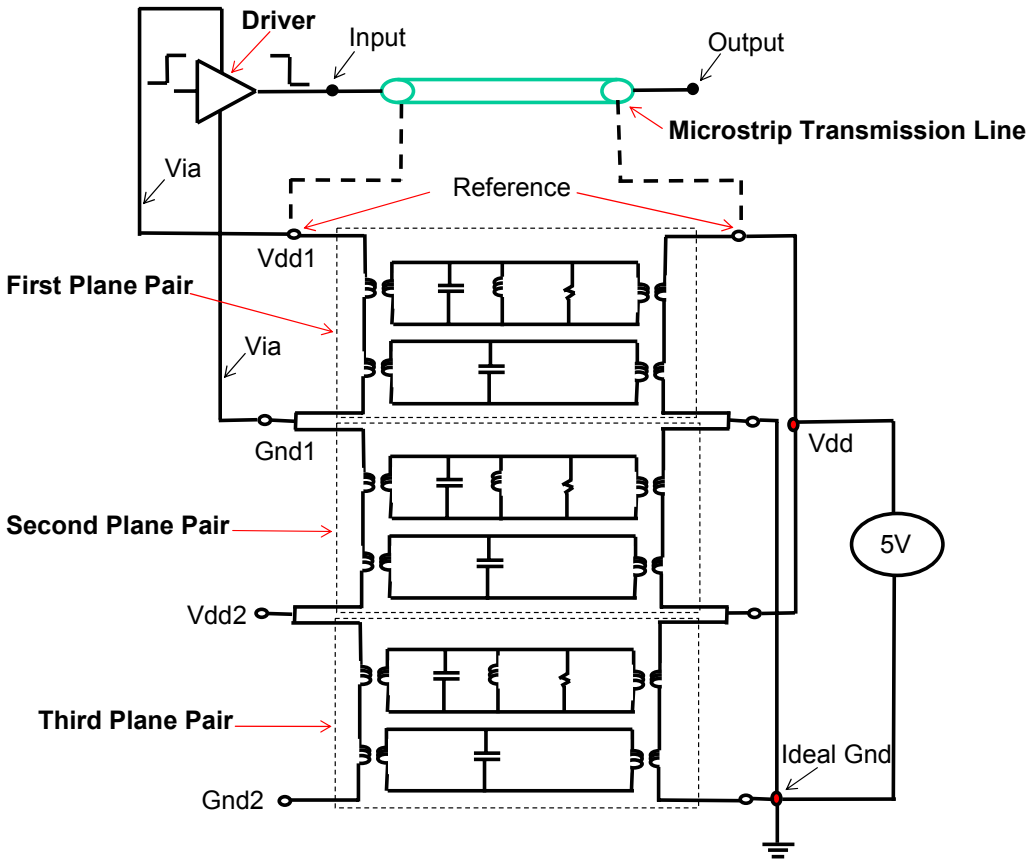


Figure 3.9 Circuit Model for the Test Vehicle

In the equivalent circuit for the test vehicle shown in Figure 3.9, the modes used for the planes were $0 \leq m \leq 8$ and $n=0$. Since the planes in the test vehicle are very long as compared to their width, the planes behave as one-dimensional transmission lines. Hence the zeroth mode was used for '*n*'. Figure 3.10 shows the modeling and measurement result for the microstrip transmission lines with no termination.

The voltage fluctuations across the power supply of the driver are caused by electromagnetic waves reflecting from the edge of the planes. The amplitude of the bounce is a function of the impedance profile of the planes and the frequency spectrum of

the driver signal. Simulation results show that the circuit in Figure 3.9 captures the power supply bounce on the planes. It is important to note that the driver models were constructed from measurements and contain a small discrepancy in the amplitude of the noise waveforms. It is also important to note that a port specified on a plane pair should be continued through the cross-section of the models to enable the propagation of noise to lower layers in the board.

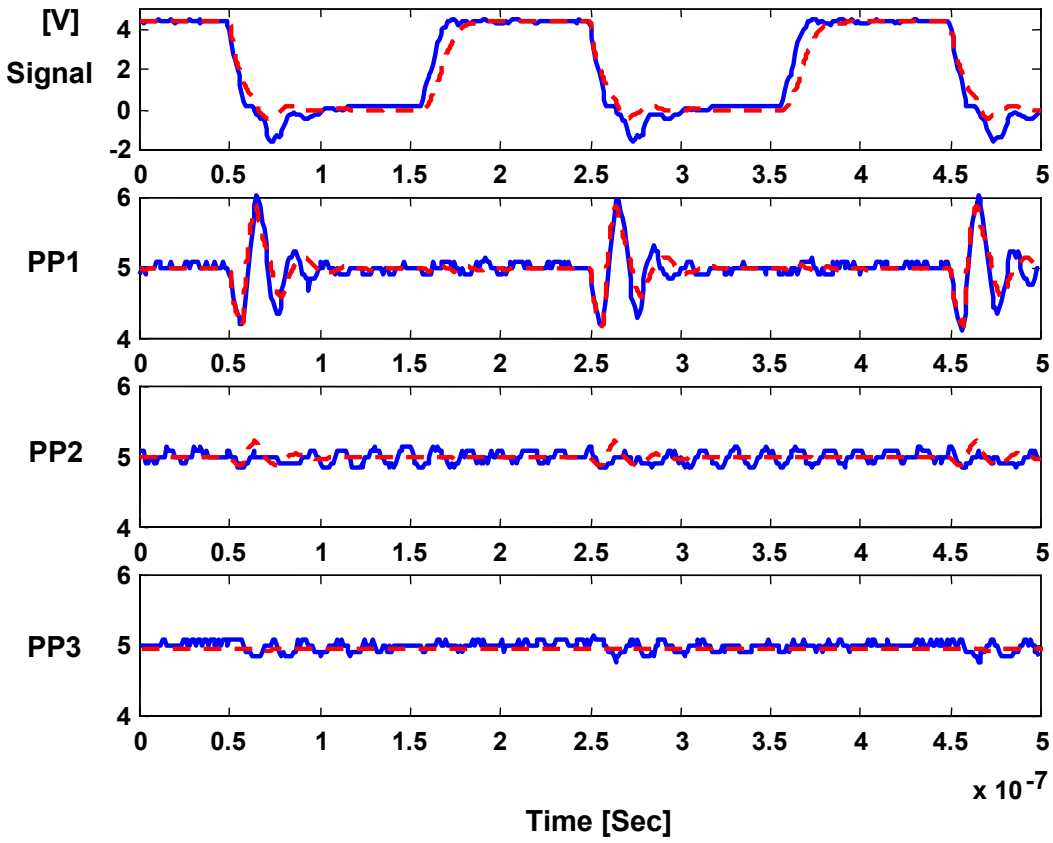


Figure 3.10 Measurement Results (Solid Line) and Modeling Results (Dashed Line): No Termination

Figure 3.11 shows the case where the microstrip transmission lines are terminated to both Vdd and Gnd planes on the right side of the test vehicle with 43 ohm resistors.

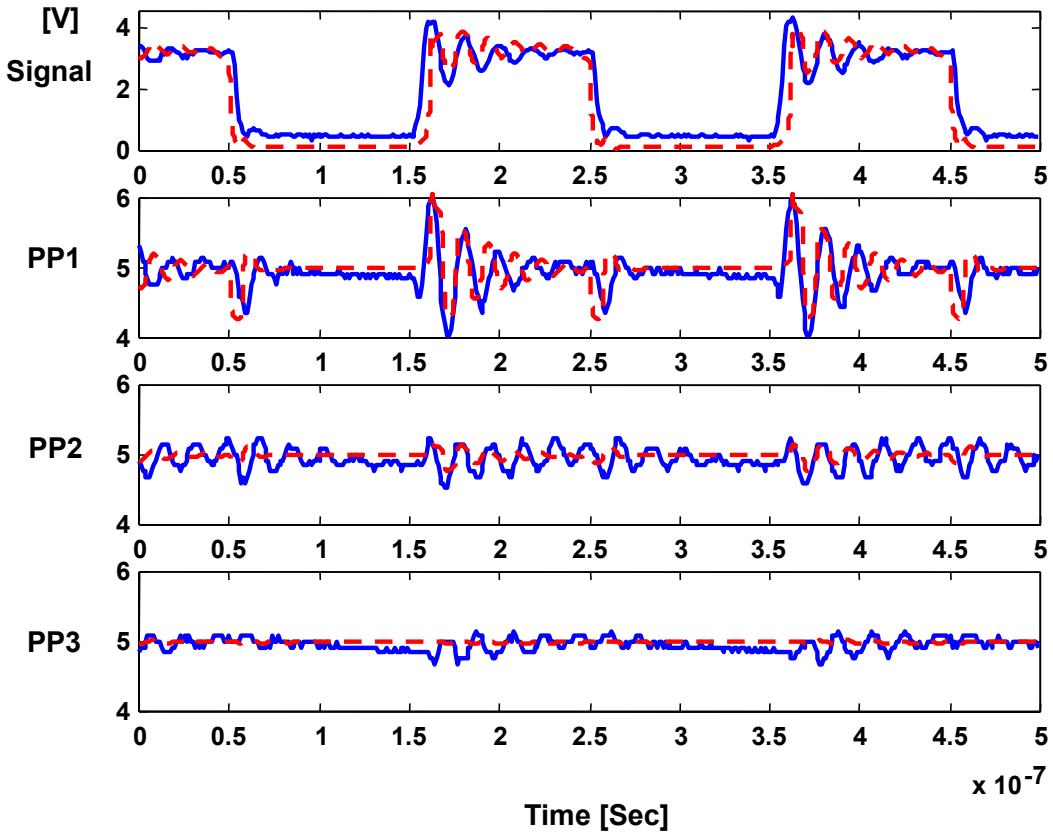
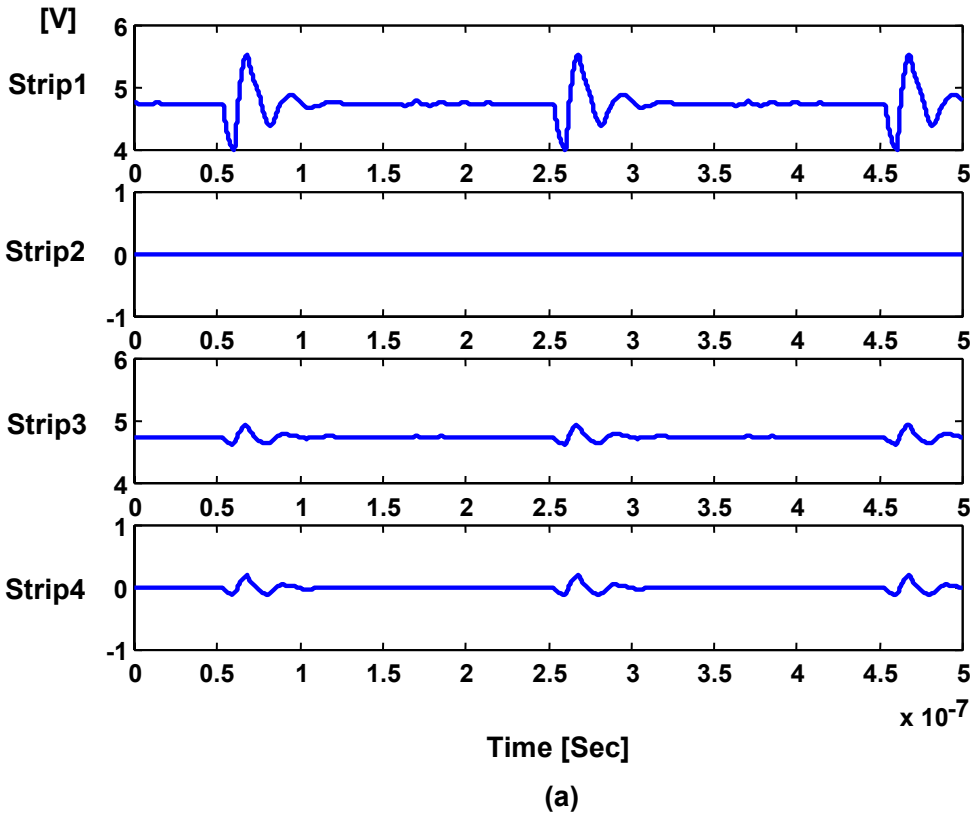


Figure 3.11 Measurement Results (Solid Line) and Modeling Results (Dashed Line): With Termination

Figure 3.12 shows the stripline simulation results for no termination. Strip1 to Strip4 make reference to Gnd1 plane while Strip5 to Strip8 make reference to Vdd2 plane. The voltage at the far end of Strip1, which is connected to the Vdd1 plane at the near end, shows the 3 or 4 ns of time delay of PP1, the voltage between Vdd1 and Gnd1 near the drivers. This time delay is due to the time of flight required for the wave to

propagate on the stripline to reach the far end of Strip1. An interesting phenomenon can be observed in Strip4 in Figure 3.12 (a), where the near end is connected to Gnd2 plane. Since Strip4 carries the signal of the Gnd2 plane with respect to Gnd1 plane at the far end of the board, the result represents the amount of noise coupled to a quiet stripline that is referenced to a noisy power plane. In a similar manner, the noise coupled to a quiet stripline (Strip 6) that propagates the Gnd1 plane signal referenced to a noisy power plane (Vdd 2 plane) is shown in Figure 3.12 (b).



(a)

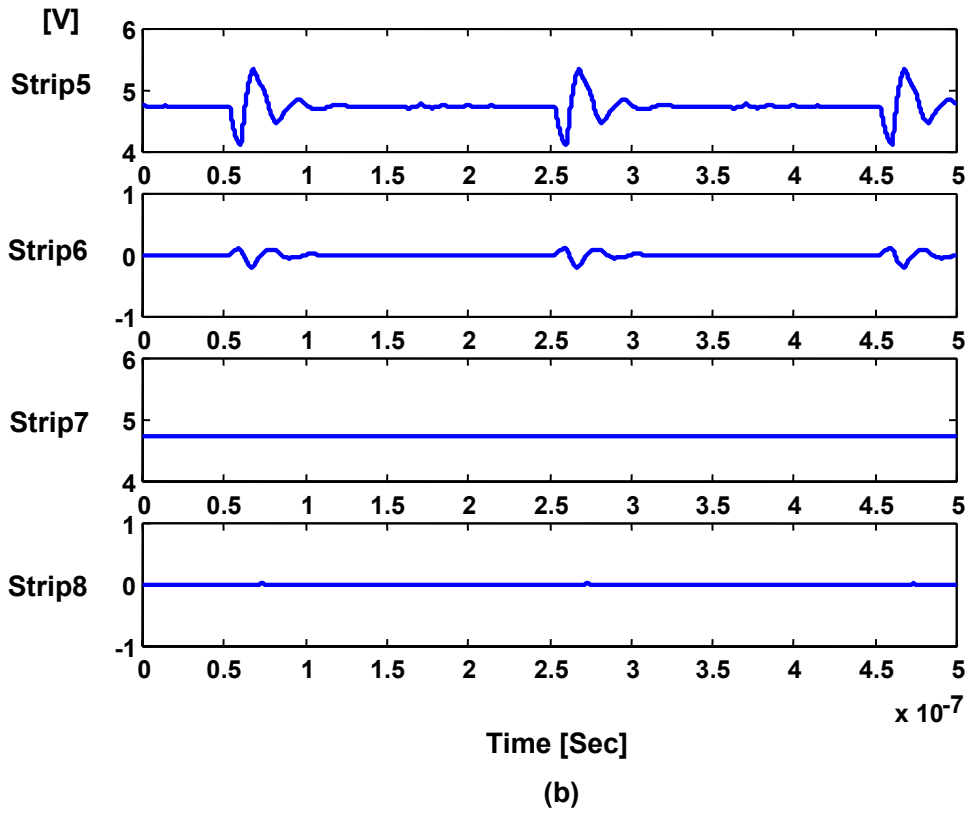


Figure 3.12 Waveforms at the Far End of Striplines for No Termination: (a) Strip1-Strip4 (b) Strip5-Strip8

3.5 Summary

In this chapter, a test vehicle was measured to obtain the plane-to-plane noise waveforms. Through measurements, it has been shown that simultaneous switching noise (SSN) due to plane bounce is caused by the return currents on the reference planes. The return current accumulates time-varying charges on the planes, which act like a displacement current source. The electromagnetic radial wave excited by this current source propagates between the planes and bounces off the edges of the planes, causing

the phenomena we call “bounce.” Non-linear driver models were connected to the circuit models for the planes and transmission lines, as described in Chapter 2, for simulation in SPICE. Simulation results, which account for the return currents correctly, were compared with measurements, verifying the validity of the method. The modeling method was also used to simulate the noise coupled to a quiet stripline, when referenced to noisy power planes.

CHAPTER 4

Plane Bounce caused by Discontinuities

It was shown in Chapter 3 that the return current on planes is responsible for plane bounce. Planes also bounce when there are discontinuities along the return current path. Signal vias and splits on the planes act as discontinuities in the path of the return currents, causing the simultaneous switching noise. The transmission lines carrying the signal need to reference proper planes to model the return current effect when vias transition. In order to capture the effect of a discontinuity due to the split planes, the impedance of the signal transmission lines traversing the split need to be determined by considering proper references.

In this chapter, active boards designed with vias and split planes have been measured for power supply voltage fluctuations. Test vehicles have been modeled and simulated by using the method described in this chapter, which is an extension of the method described in the previous chapters. The purpose of this chapter is to study the effects of vias and split planes and to capture these effects in SSN simulation. Model to hardware correlation has been done to demonstrate the validity of the method. Coupling between two isolated planes has also been simulated to quantify the energy transferred across the split planes.

4.1 Plane Bounce caused by Via Transitions

Vias have a pronounced effect on SSN. In the context of timing and signal integrity analysis, vias can be modeled as discontinuities by extracting their equivalent circuit [26]-[31]. However, these models may not capture the bounce on the power planes due to via transitions, especially if they do not excite the planes. In this section, via effects have been modeled by accounting for the return currents on the planes and the effects of via transitions on SSN have been studied.

Figure 4.1 shows a test board, which consists of drivers, transmission lines, vias, and planes [32].

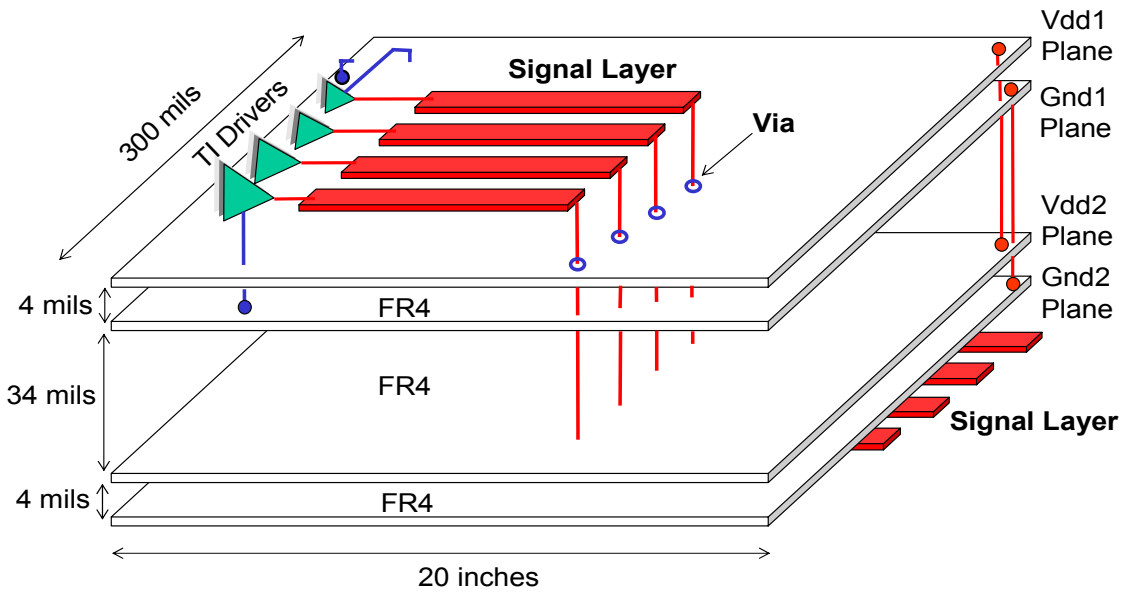


Figure 4.1 Test Vehicle with Via Transitions

It is a six-layered board. Half the length of the microstrip transmission lines with length 10 inches (25 cm) are on the top layer, above Vdd1 plane, and the other half are on the bottom layer, below Gnd2 plane. The microstrip transmission lines were unterminated. Consider the scenario when the microstrip transmission lines are being charged, as shown in Figure 4.2. The transmission lines on the top layer reference the adjacent plane, namely the Vdd1 plane, when they carry the signal from the drivers. Thus, the return currents for these transmission lines flow on the Vdd1 plane, leaving behind time-varying negative charges at via locations on the Vdd1 plane, as shown in Figure 4.2. The transmission lines on the bottom layer, however, reference the Gnd2 plane, causing the accumulation of time-varying positive charges at via locations on the Gnd2 plane, due to the flow of return currents caused by the charging of the transmission lines.

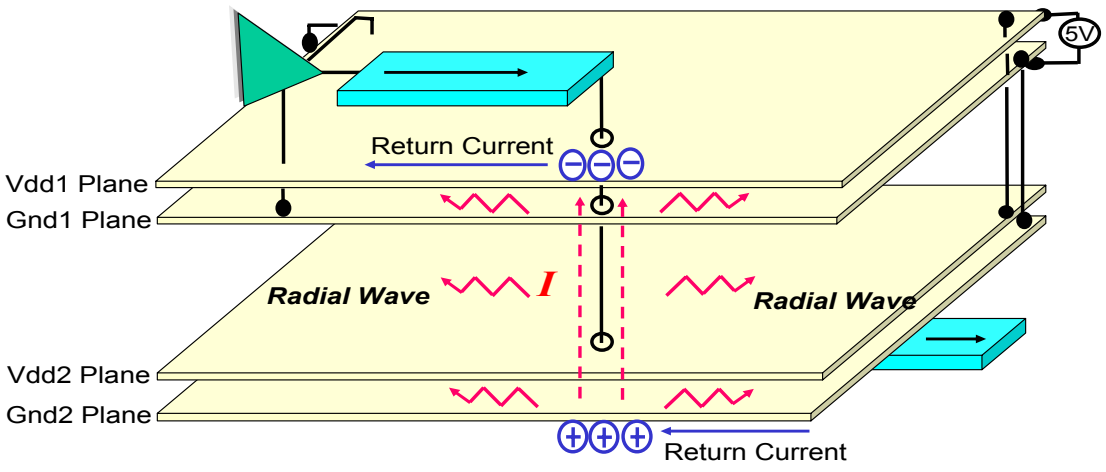


Figure 4.2 Plane Bounce due to Via Transitions

Thus, the vias, which connect the top and bottom transmission lines, generate the current source, *I*, which exists along the vertical cross-section of the test vehicle, as shown in Figure 4.2. This vertical current source excites electromagnetic waves that reflect from the edges of the planes causing planes to bounce. The plane bounce results in voltage fluctuations on the power supply rails of the drivers.

Based on the discussion in the previous section, the test vehicle can be modeled, as shown in Figure 4.3.

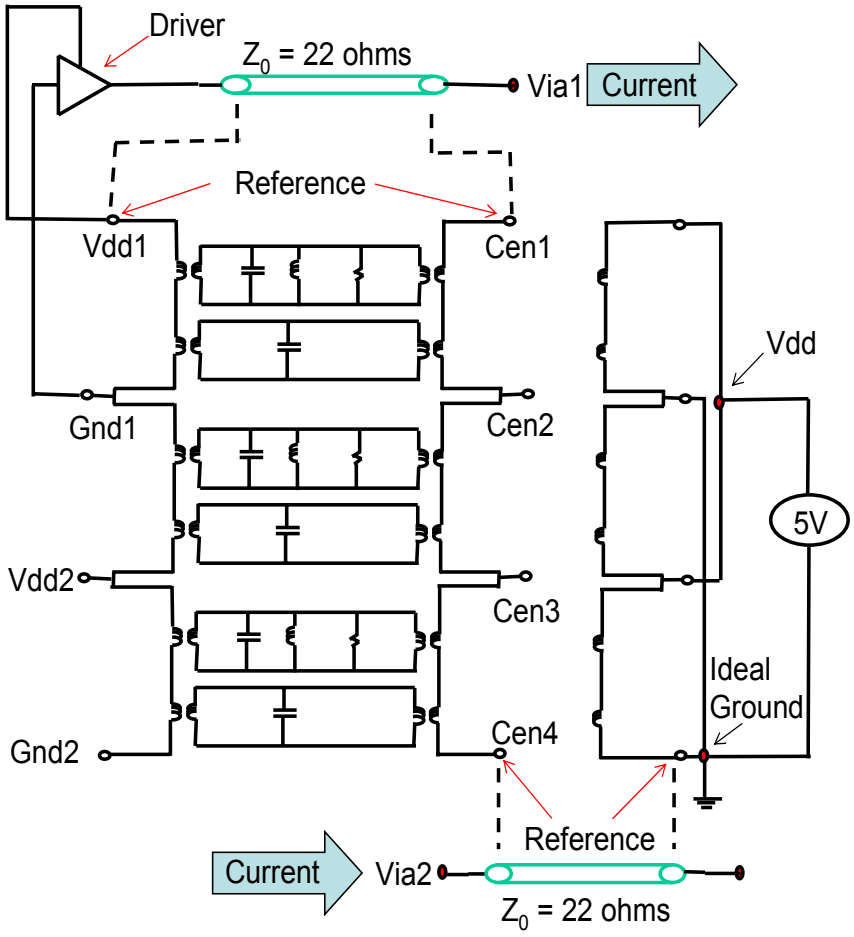


Figure 4.3 Circuit Model for the Test Vehicle with Via Transitions

The via in Figure 4.3 has been modeled with inductances and capacitances to account for the impedance mismatch at the via location. Sonnet software, which is an electromagnetic field solver based on method of moments, was used to obtain the values of capacitance (C) and time delay (Td) for the via. The inductance (L) of the via was calculated from,

$$L = \frac{Td^2}{C} \tag{4.1}$$

Figure 4.4 shows the circuit model for the via, which has been incorporated into the circuit in Figure 4.3 for plane bounce simulation in HSPICE.

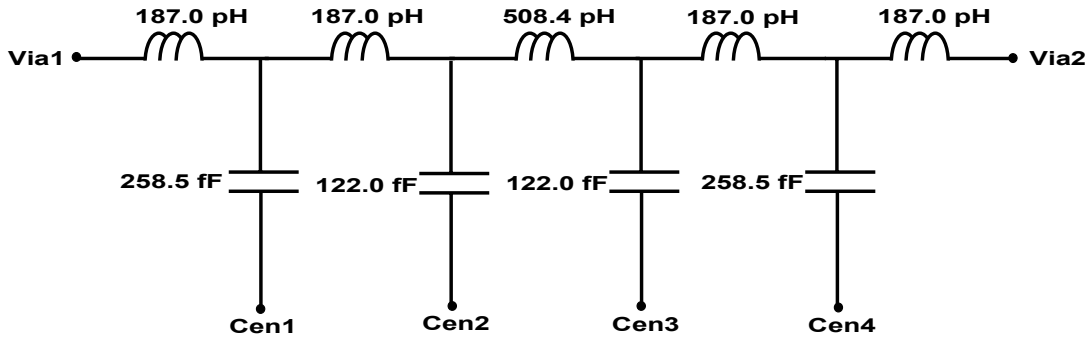


Figure 4.4 Circuit Model for Via

The primary hypothesis in this chapter is that the return currents are responsible for plane bounce when signal lines are referenced to different planes. Hence, the

discontinuity is the via which causes different paths for the return currents, causing planes to bounce. If this is true, then the simple circuit model in Figure 4.3 should capture the voltage fluctuation on the planes.

Figure 4.5 shows a comparison between measurement and modeling results, when the far ends of the microstrip transmission lines are unterminated. The results show reasonably good agreement.

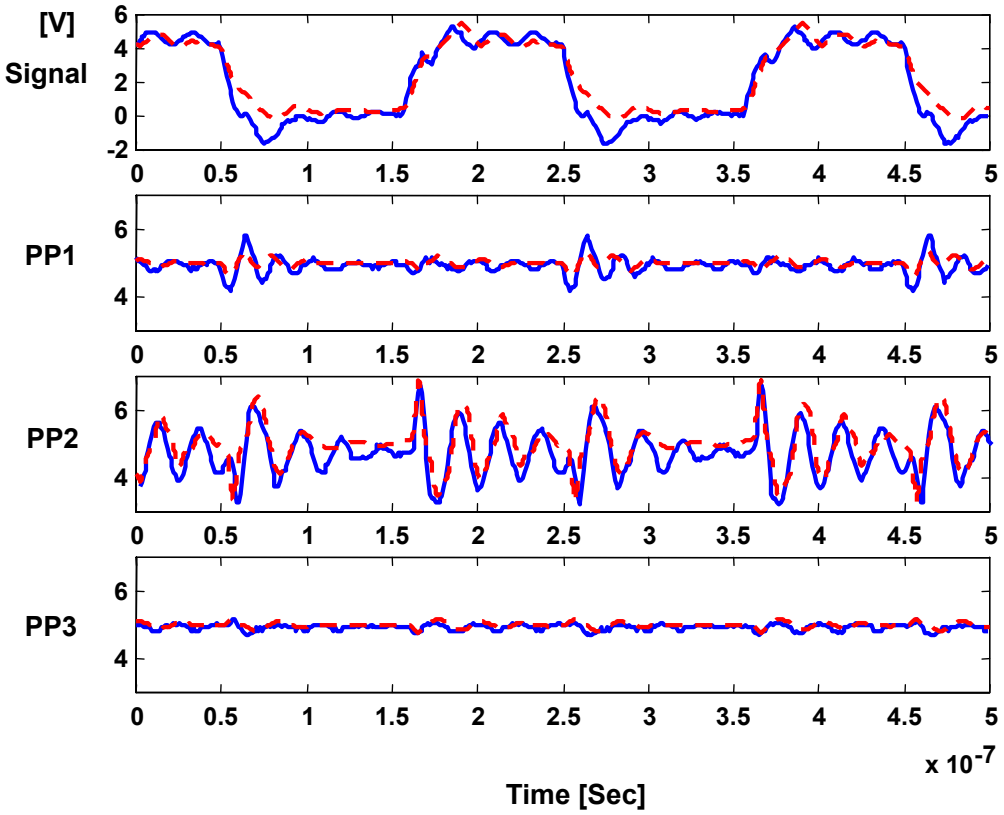


Figure 4.5 Measurement Results (Solid Line) and Modeling Results (Dashed Line) PP1: Voltage Difference between Vdd1 and Gnd1, PP2: Voltage Difference between Vdd2 and Gnd1, PP3: Voltage Difference between Vdd2 and Gnd2

It is important to note that the maximum noise voltage occurs on the second layer, which is the Gnd1/Vdd2 plane pair although the driver was supplied with power from the

first layer, which is Vdd1/Gnd1 plane pair. With a width of 0.3 inches and separation of 4 mils, the impedance of Vdd1/Gnd1 and Vdd2/Gnd2 plane pair is ~2.3 ohms for FR4 dielectric material. With a separation of 34 mils between Gnd1 and Vdd2 plane, the impedance is ~20 ohms for the Gnd1/Vdd2 plane pair. Hence, when the vertical current source due to the via transition excites the electromagnetic wave, the differential voltage between Gnd1/Vdd2 plane pair is larger due to a larger impedance, as shown in the measurement. The modeling result captures this effect very well.

4.2 Plane Bounce caused by Split Planes

In multi-layered printed circuit board (PCB), split power and ground planes are sometimes used. A power plane divided into several areas can be used to distribute multiple power supply voltages. In addition, separating a power/ground plane from the rest of the power distribution network can isolate a noisy or sensitive circuit from other circuits [19]. However, interconnects carrying the signal sometimes need to cross the split to communicate between different components located in different areas of the PCB.

In [33], the ground bounce with a slot in the ground and power plane was simulated using the Finite Difference Time Domain (FDTD) method, but the structure does not include signal transmission lines. In [34], the signal integrity issues at a split power/ground have been explained by mode conversion between the microstrip and slot lines, whose characteristic impedances are calculated by pre-determined formulae, as discussed in [35], [36], [37]. However, the plane bounce between the power and ground

planes have been neglected in most of the analysis available in the literature. In this section, the plane bounce caused by split power/ground planes when signal transmission lines traverse the split has been studied. Figure 4.6 shows the structure that was measured, modeled and studied.

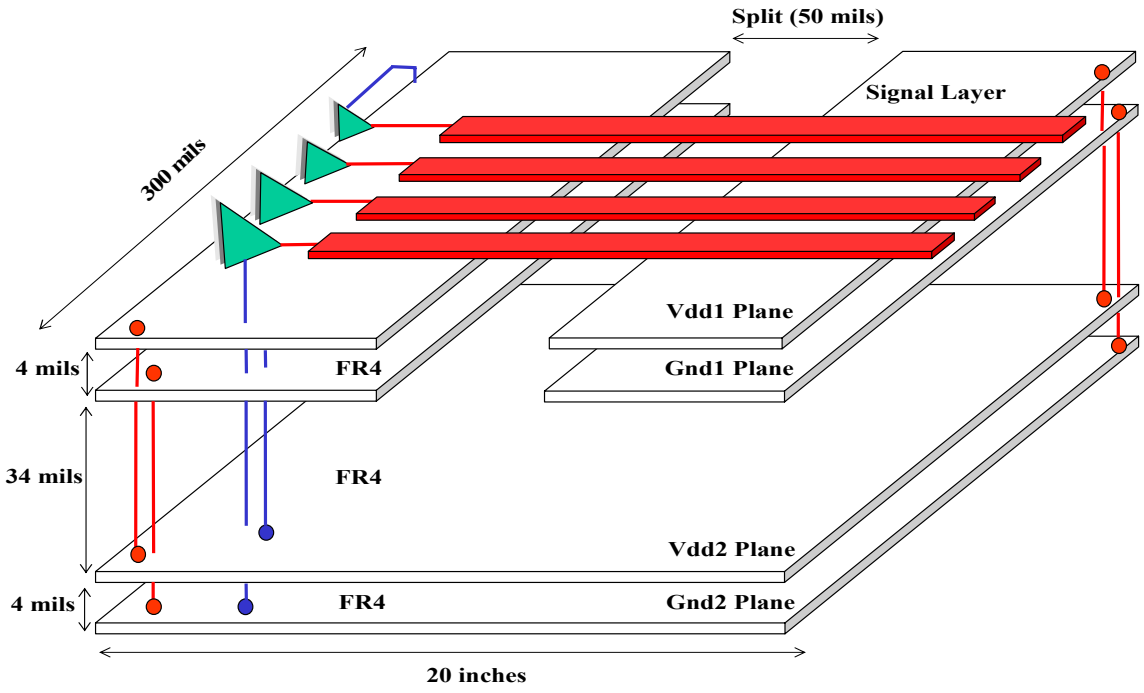


Figure 4.6 Test Vehicle with Split Planes

As shown in Figure 4.6, the Vdd1 and Gnd1 planes were split at the center and separated into two isolated planes. The drivers were powered from the Vdd2/Gnd2 plane pair which was continuous, as shown in Figure 4.6. The four microstrip transmission lines driven by the drivers cross the split on the Vdd1 and Gnd1 planes. The transmission lines were left unterminated. When the transmission lines carry the signal, the return currents flow on the adjacent planes near the vicinity of the transmission lines. Consider the scenario when the microstrip transmission lines are being charged and carry the

forward current, as shown in Figure 4.7. The return currents for the right section of the transmission lines flow on the right split Vdd1 plane, depositing positive charges at A on the plane, as shown in Figure 4.7. Similarly, the return currents for the left section of the transmission lines flow on the left split Vdd1 plane, leaving behind negative charges at B on the plane. At the split, the return currents for the transmission lines flow on the Vdd2 plane, just below the transmission lines, as shown in Figure 4.7. Thus, the split in the planes causes a discontinuity in the path of the return currents on the planes. Since the current has to be continuous, the current continues to flow through the displacement current *I*, as shown in Figure 4.7. This displacement current acts as a vertical current source, causing radial waves, which results in plane bounce.

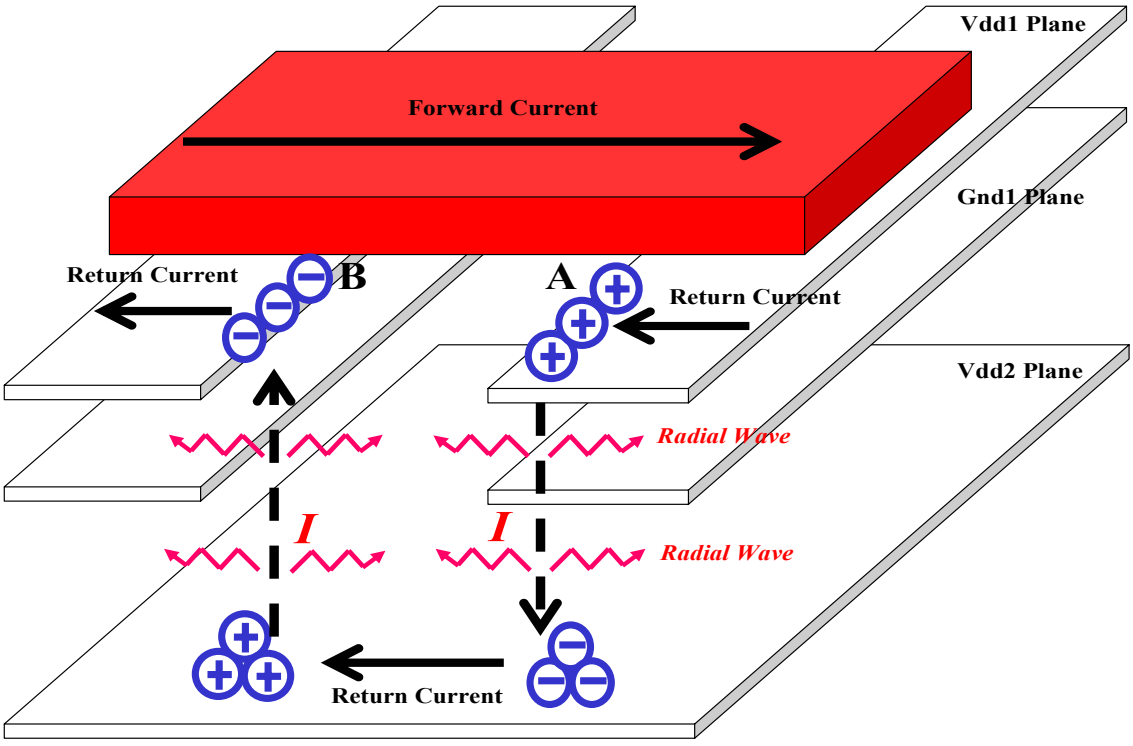


Figure 4.7 Plane Bounce due to Split

To capture the plane bounce due to the split, the microstrip transmission lines need to be modeled such that they are appropriately referenced to the planes. Although the microstrip transmission line in the test vehicle has a continuous signal conductor, it needs to be modeled as a series of transmission lines with different impedances since the reference plane is not continuous. When the signal flows on the microstrip transmission line, as shown in Figure 4.7, it initially sees an impedance of 22 ohms, corresponding to the distance of 4 mils between the signal conductor and the reference plane. For this section of the transmission line, the reference plane is the Vdd1 plane. As the microstrip line traverses the split region, it sees a new impedance, corresponding to the distance (d) of 42 mils between the signal conductor and the reference plane. For this section of the transmission line, the reference is the Vdd2 plane. The impedance, Z_0, for this transmission line has been calculated using the effective dielectric constant (ε_e) and signal conductor width (w), as shown below [38].

$$Z_0 = \frac{60}{\sqrt{\varepsilon_e}} \ln\left(\frac{8d}{w} + \frac{w}{4d}\right) = 80.5 \text{ ohms} \qquad (4.2)$$

where

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} * \frac{1}{\sqrt{1 + 12d/w}} \qquad (4.3)$$

Equation (4.2) is valid when $w/d \leq 1$, which is true for the test vehicle structure. After the split, the microstrip line once again has an impedance of 22 ohms since the reference plane is the Vdd1 plane.

Thus, the microstrip transmission line can be modeled as a series of three transmission line sections, as shown in Figure 4.8.

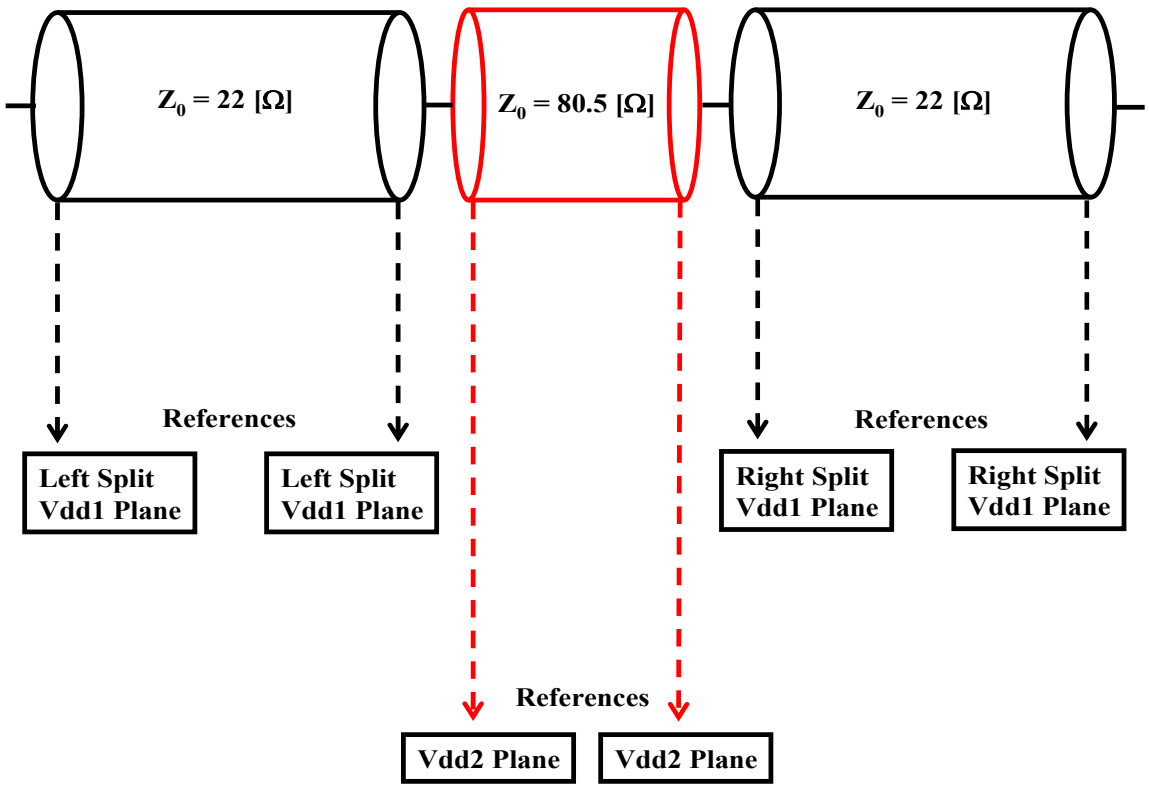


Figure 4.8 Modeling of Microstrip Transmission Lines Passing Over a Split Plane

The references in Figure 4.8 are the ports on the planes. The four planes, i.e. Vdd1, Gnd1, Vdd2 and Gnd2, are split into two plane pairs and modeled using the resonator circuit model, described in the previous sections. The circuit model for the microstrip transmission lines in Figure 4.8 has been incorporated into the circuit model for the planes by referencing the transmission lines to the appropriate ports on the planes, as shown in Figure 4.9.

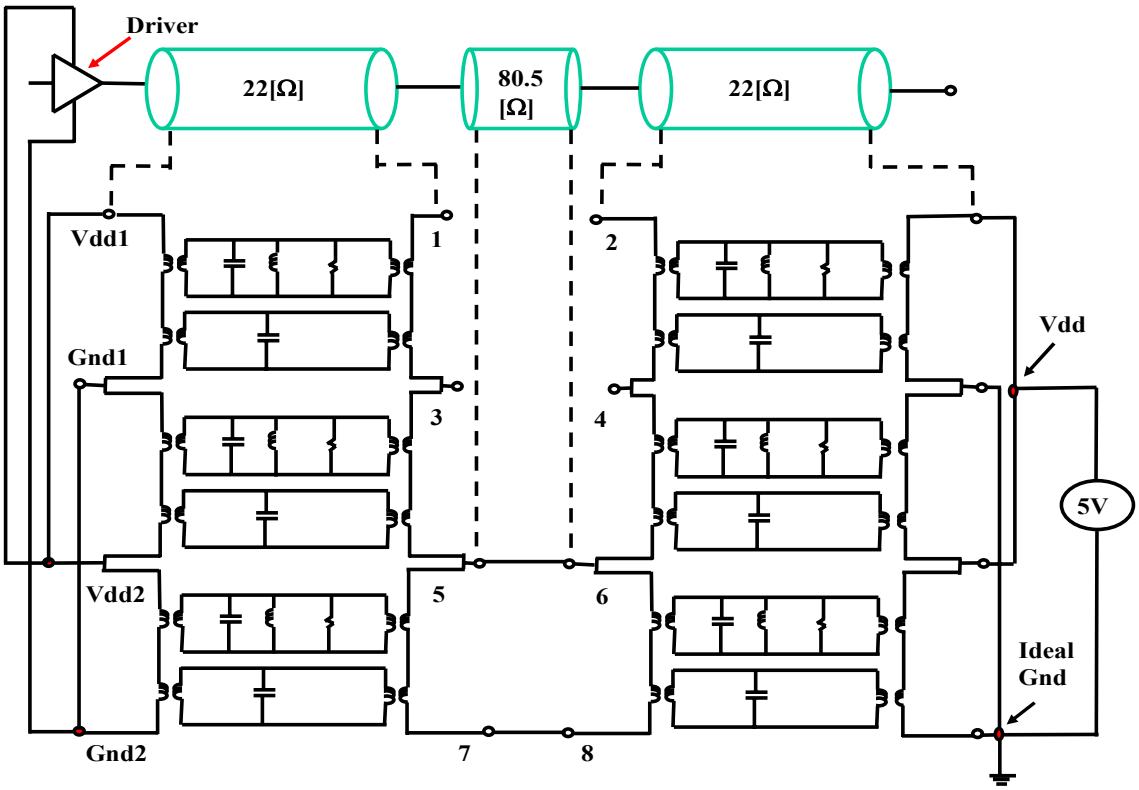


Figure 4.9 Modeling of the Test Vehicle with Split Planes

The circuit in Figure 4.9 has been simulated in HSPICE and the voltage waveforms near the split have been compared with measurements, as shown in Figure 4.10. Figure 4.10 (a) is the driver output signal with respect to the local Gnd2 plane. The noise voltages measured near the split were 1) voltage between right Vdd1 plane and Gnd2 plane, as shown in Figure 4.10 (b) 2) voltage between left Vdd1 plane and Gnd2 plane, as shown in 4.10 (c) 3) voltage between right Gnd1 plane and Vdd2 plane, as shown in Figure 4.10 (d). The opposite polarity in the noise pattern in Figure 4.10 (c) as compared to Figure 4.10 (b) is due to the opposite direction of the displacement current source, *I*, as the return current crosses the split, as illustrated in Figure 4.7. As can be seen in Figure 4.10, the modeling results capture the noise waveforms very well.

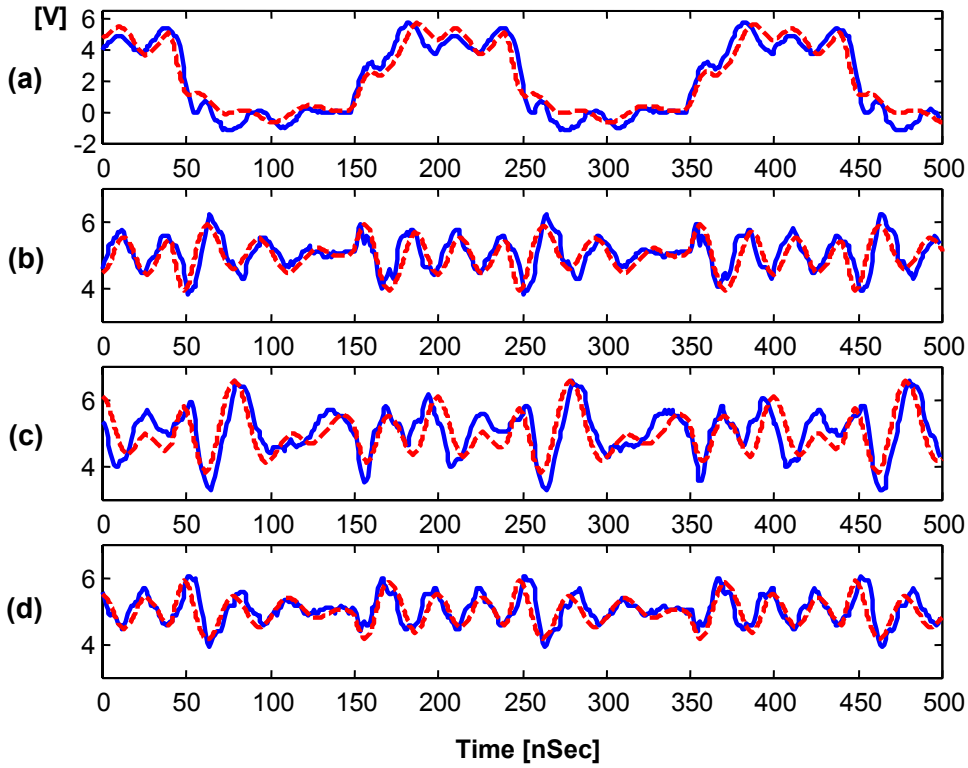


Figure 4.10 (a) Driver Output Signal (b) Voltage between Right Vdd1 Plane and Gnd2 Plane (c) Voltage between Left Vdd1 Plane and Gnd2 Plane (d) Voltage between Right Gnd1 Plane and Vdd2 Plane; Measurement (Solid Line), Modeling (Dashed Line)

4.3 Coupling through Split Planes

The power plane structure that has been analyzed in this section is shown in Figure 4.11 [39]. The purpose of modeling this structure was to calculate the coupling between two isolated planes connected through a ferrite core [40]. This structure was provided as a benchmark to test various modeling methods at the 9th Topical Meeting on Electrical Performance of Electronic Packaging held in Scottsdale, Arizona from October 23-25, 2000.

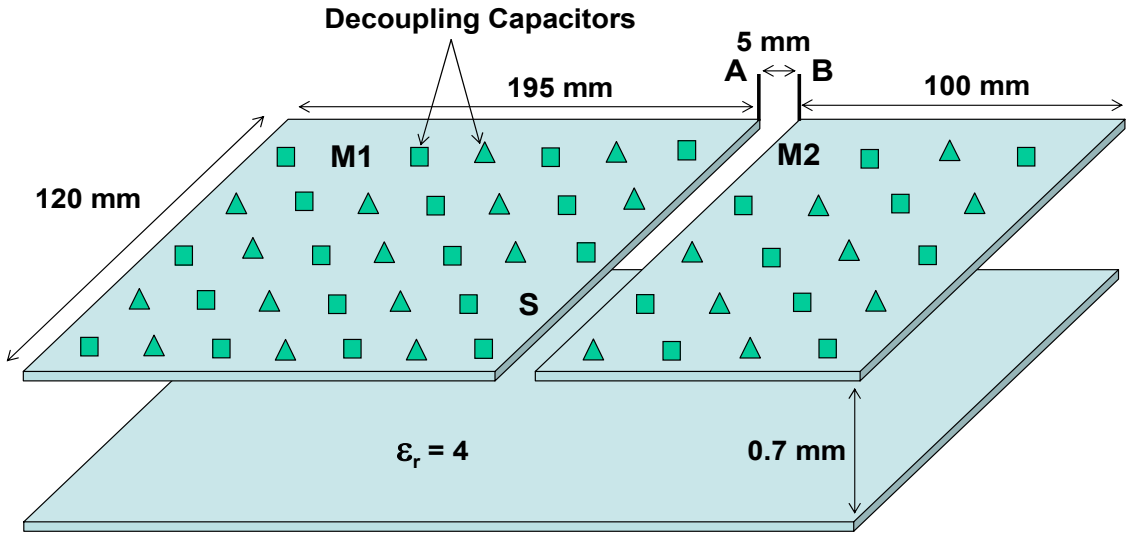


Figure 4.11 Plane Structure with Split

The power plane structure consisted of two planes separated by a dielectric. The bottom plane was continuous while the top plane was split into two planes. The two planes were connected together using a circuit between A and B which represents the ferrite core. The ferrite core was represented as a parallel combination of 0.15 pF, 95 ohms and 0.17 nH circuit elements. Each plane pair contained decoupling capacitors which were attached to the planes, as shown in Figure 4.11. Two types of decoupling capacitors were used. The first decoupling capacitor was a 10000 pF capacitor with an equivalent series resistance (ESR) of 0.1 ohms and an equivalent series inductance (ESL) of 2 nH and the second capacitor was a 220 pF capacitor with ESR=0.1 ohms and ESL=2

nH. Since, the modeling method used in this dissertation assumes a magnetic wall at the edges of the planes, including at the split, the fringing capacitance across the split has been ignored.

The plane structure was modeled using the method described in the previous sections. The equivalent circuit of the split plane is shown in Figure 4.12. As mentioned earlier, the synthesized equivalent circuit guarantees stability and passivity. Since the approach is gridless, it enables the simulation of structures where capacitors and probe points can be arbitrarily placed.

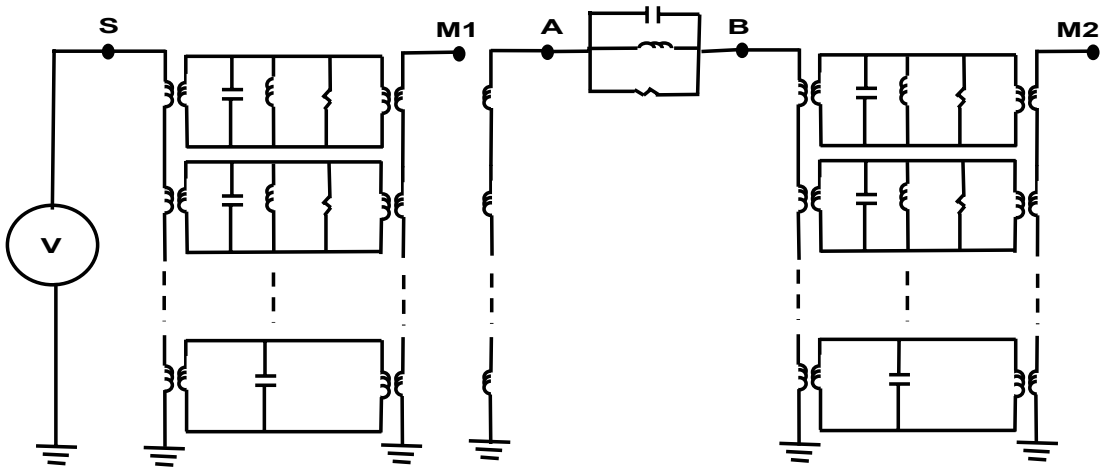


Figure 4.12 Equivalent Circuit for the Structure

In Figure 4.11, a major assumption is that the only coupling between the two isolated planes is through the circuit between nodes A and B. The transfer impedance between port ‘S’ and port ‘M2’ with decoupling capacitors was computed using the equivalent circuit in Figure 4.12. Table 4.1 shows the CPU time for different number of modes and the accuracy has been compared in Figure 4.13.

Modes (m,n)	CPU Time
(5,5)	28.94 Sec
(7,7)	188.68 Sec
(8,8)	403.49 Sec

Table 4.1 CPU Time for Different Number of Modes

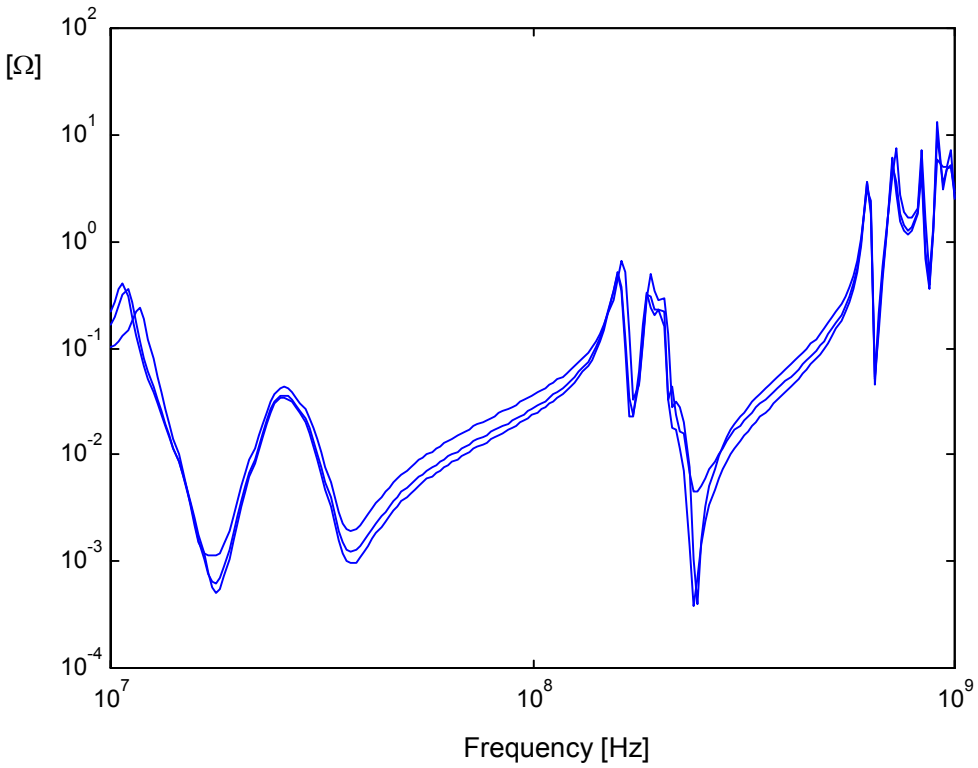


Figure 4.13 Transfer Impedance between Port 'S' and Port 'M2' with Decoupling Capacitors: (5,5) modes (Solid Line), (7,7) modes (Dashed Dot Line), (8,8) modes (Dashed Line)

Figure 4.14 and 4.15 show the comparison with other modeling methods. Figure 4.14 is the comparison with the analytical expression in equation (2.1), when (m,n) = (10,10) was used for both the equivalent circuit and the analytical expression. Figure 4.15 shows the comparison with the method using the transmission matrix (T-matrix) method [41].

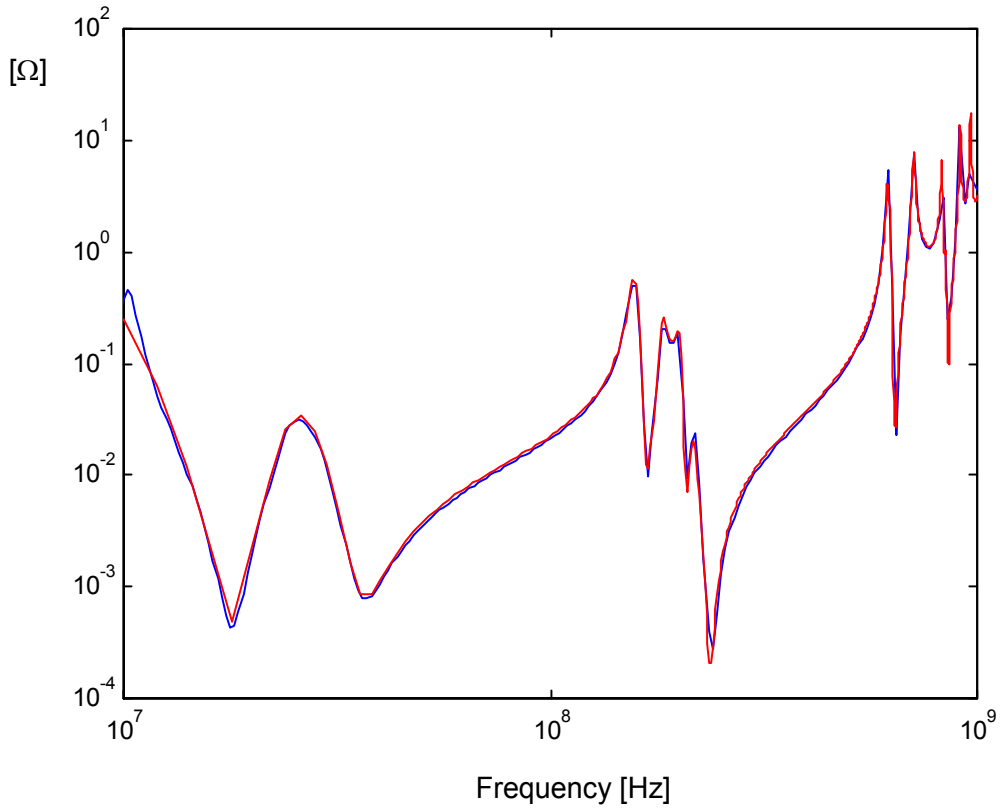


Figure 4.14 Comparison with Analytical Expression: Equivalent Circuit (Solid Line) and Analytical Expression (Dashed Line)

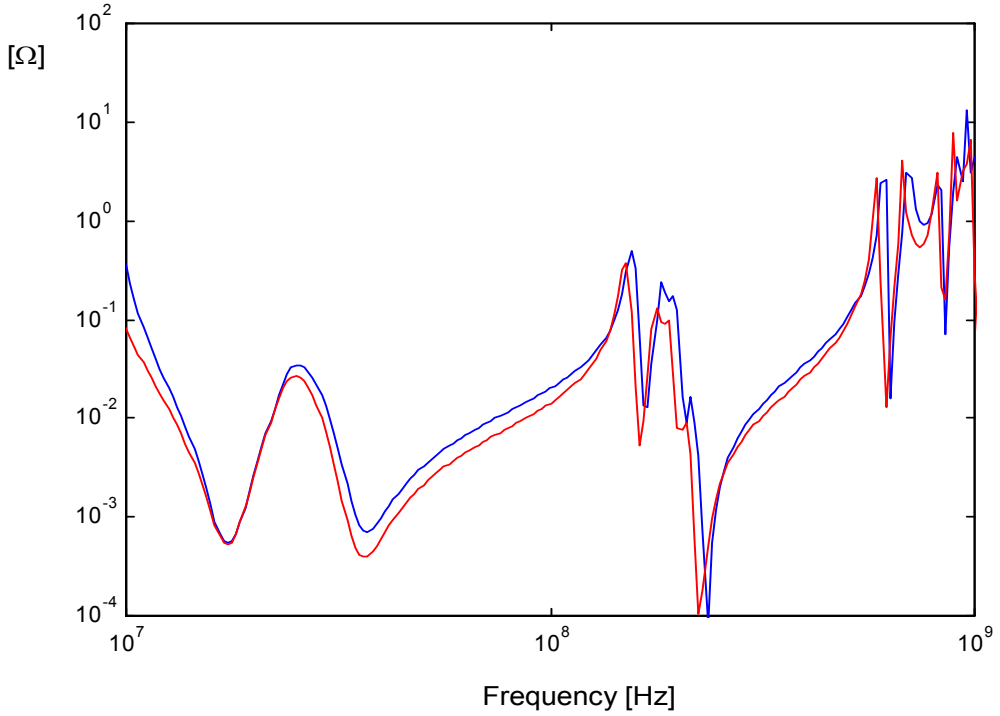


Figure 4.15 Comparison with T-matrix Method: Equivalent Circuit with m=n=15 (Solid Line) and T-matrix Method (Dashed Line)

The small discrepancy in Figure 4.15 can be improved by increasing the number of modes used in the equivalent circuit.

4.4 Summary

In this chapter, simultaneous switching noise (SSN) generated on a test vehicle containing vias was measured. It was shown that vias act as discontinuities causing different paths for the return currents, resulting in plane bounce. A method for including via effects in the simulation of SSN was discussed in this chapter. Simulation results have

been correlated with measurements, showing the validity of the modeling method. SSN caused by split planes has also been studied in detail in this chapter. Split power planes with transmission lines traversing the split have been measured for power supply noise. It has been shown that the split in the planes causes a discontinuity in the path of the return currents on the planes, generating a vertical current source, when the signal traverses the split. Radial waves caused by this current source results in plane bounce. These effects have been captured in the model by using transmission lines, referenced to the appropriate planes. Simulation results show good agreement with measurements, verifying the validity of the model. Using the modeling method, coupling between two split planes has also been simulated and the results have been compared with other modeling techniques.

CHAPTER 5

Extension to Large Systems

In the previous chapters, a method was presented for simulating the power supply noise on a test board. It consisted of separate models for the planes and interconnections, which were then combined in a circuit simulator like SPICE to account for the return currents. In this chapter, the method has been extended for modeling a system containing packages on a printed circuit board. In the system that has been simulated, the driver chips and receiver chips communicate with each other through transmission lines. These transmission lines are located between power and ground planes in the package and PCB, which is a typical cross-section in high speed systems. When the circuits switch, the return currents from the transmission lines flow both on the power and ground planes. The return currents cause voltage fluctuations on the power supply rails of the drivers and receivers, which can reduce the speed of the system.

In this chapter, the voltage fluctuations caused by the switching transmission lines have been modeled. The purpose of this chapter is to demonstrate the extension of the modeling method described earlier to realistic systems.

5.1 System - I

The system is shown in Figure 5.1, which consists of chips and packages mounted on a PCB.

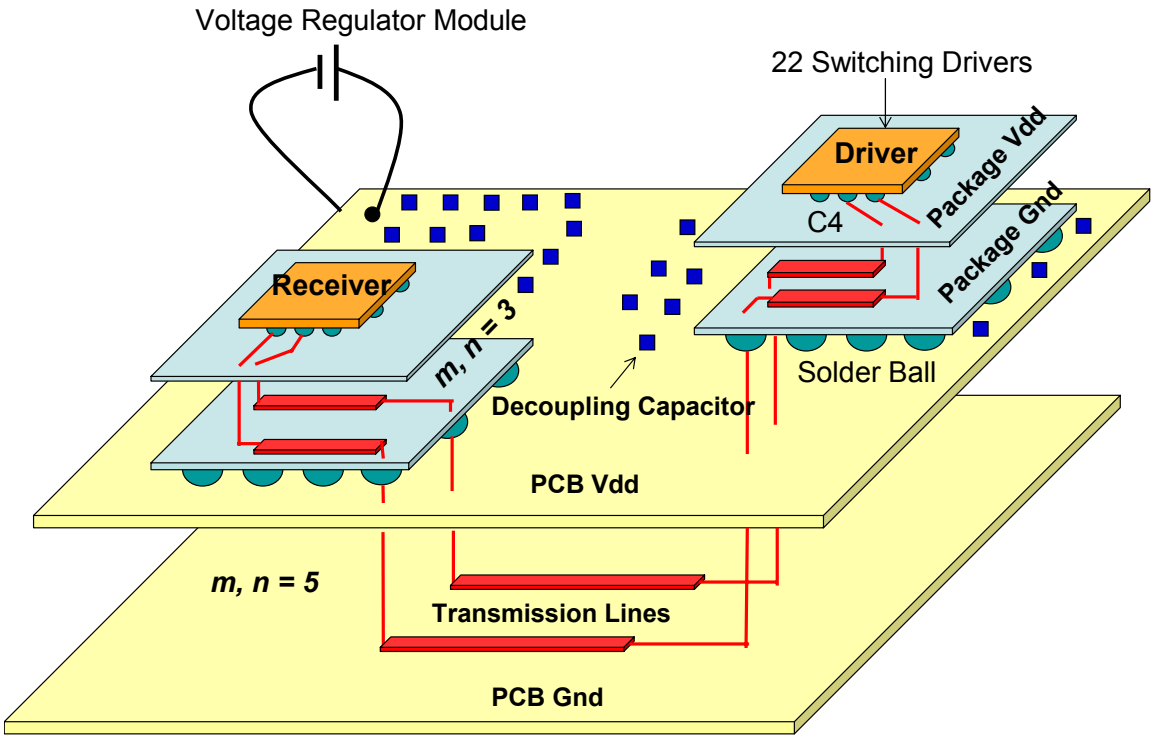


Figure 5.1 Packaged System with Driver and Receiver

The package consists of two planes (Vdd and Gnd) which measure 1.5" x 1.5" with a dielectric thickness of 4 mils. The insulator used was ceramic with a dielectric constant of 9. The PCB consists of two planes (Vdd and Gnd) with size 4" x 4" and a dielectric thickness of 4 mils. The insulator used was FR4 with a dielectric constant of 4. The PCB contains 69 decoupling capacitors which were distributed over the board at

arbitrary locations near the packages. Nine commercially available decoupling capacitors were used on the PCB. The capacitors were represented as a series RLC circuit where 'R' and 'L' are the equivalent series resistance and inductance of the capacitor, respectively. Table 5.1 shows the values of ‘R’, ‘L’ and ‘C’ used in the simulation. The PCB was powered using a 1.5 V supply at the upper left corner, as shown in Figure 5.1.

	R	L	C
A	0.11 Ohm	0.7 nH	3.3 nF
B	0.22 Ohm	0.52 nH	1 nF
C	0.17 Ohm	0.52 nH	1.5 nF
D	0.02 Ohm	7 nH	10 mF
E	0.22 Ohmn	0.52 nH	10 nF
F	0.002 Ohm	0.7 nH	22 μF
G	0.005 Ohm	5 nH	100 μF
H	0.015 Ohm	0.52 nH	1 μF
I	0.007 Ohm	0.7 nH	2.2 μF

Table 5.1 Series Equivalent Resistance and Inductance of the Capacitor

The two chips were connected using 6 transmission lines as shown in Figure 5.1. These transmission lines were connected to 22 active drivers with rise time of 100 ps, which were switched simultaneously. Three transmission lines were referenced to the Vdd plane and the remaining three were referenced to the Gnd plane, both on the package and PCB. Chip C4s with inductance of 0.05 nH were used to connect the chip to the package. Similarly, solder balls with inductance of 0.25 nH were used to connect the

package to the PCB. The planes in the package and PCB were connected together using solder balls with inductance of 0.25 nH. A total of 16 C4s and 16 solder balls were used for the transmission lines for the driver and receiver chips and 36 solder balls were used to connect between the package and PCB planes.

A total of 9 modes were used to model the package planes while 25 modes were used for modeling the PCB planes. Figure 5.2 shows the simulated driver and receiver signals with the planes modeled using the cavity resonator method. As a comparison, the system was simulated by modeling the planes using the transmission line method [42], as shown in Figure 5.2.

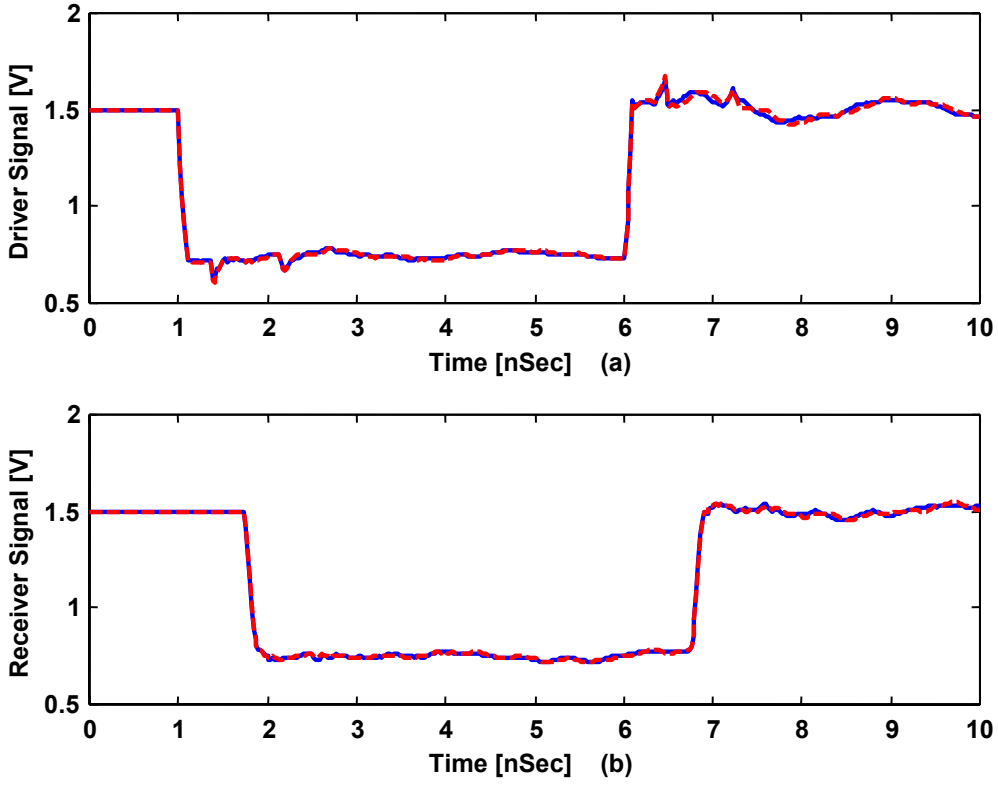


Figure 5.2 (a) Driver Signal (b) Receiver Signal; Resonator Model (Solid), Transmission Line Model (Dashed)

Figure 5.3 shows the noise simulated on the power supply planes. Figure 5.3 (a) is the noise simulated on the package planes in the vicinity of the driver. The noise simulated on the package planes in the vicinity of the receiver is shown in Figure 5.3 (b). Both figures show a distinct resonance in the waveforms due to the planes bouncing in the system. In addition, the noise on the receiver side is caused by the propagation of the electromagnetic wave through the PCB and package.

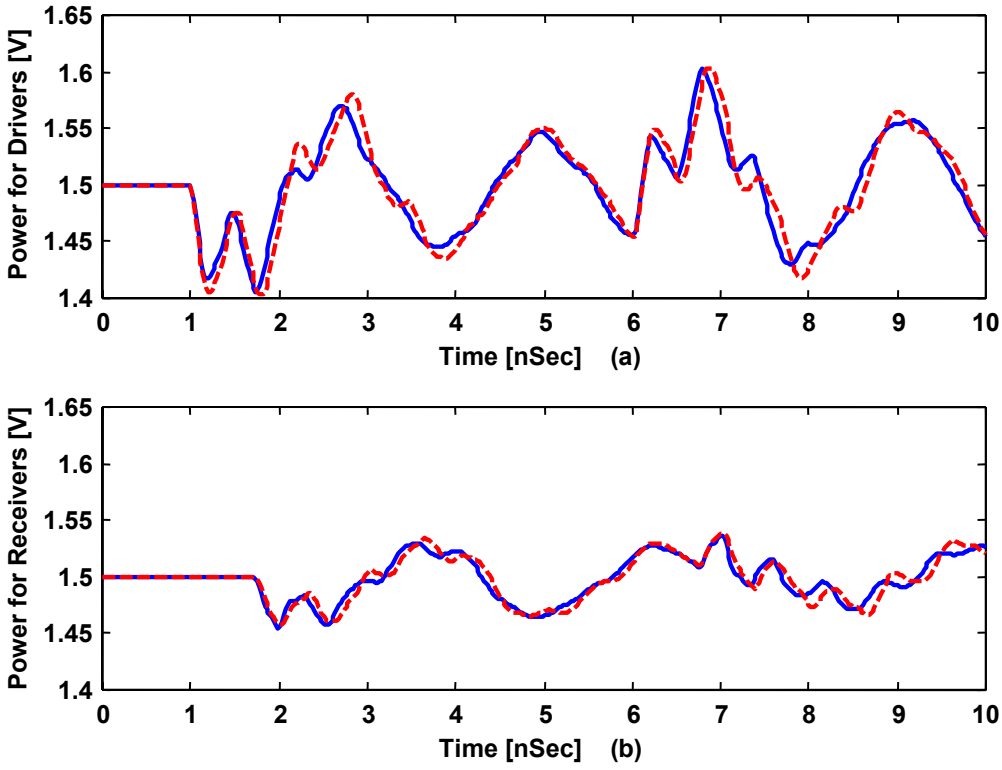


Figure 5.3 (a) Power Supply Voltage Fluctuation near Drivers (b) Power Supply Voltage Fluctuation near Receivers; Resonator Model (Solid), Transmission Line Model (Dashed)

Figure 5.4 shows the noise on the PCB power planes near receivers.

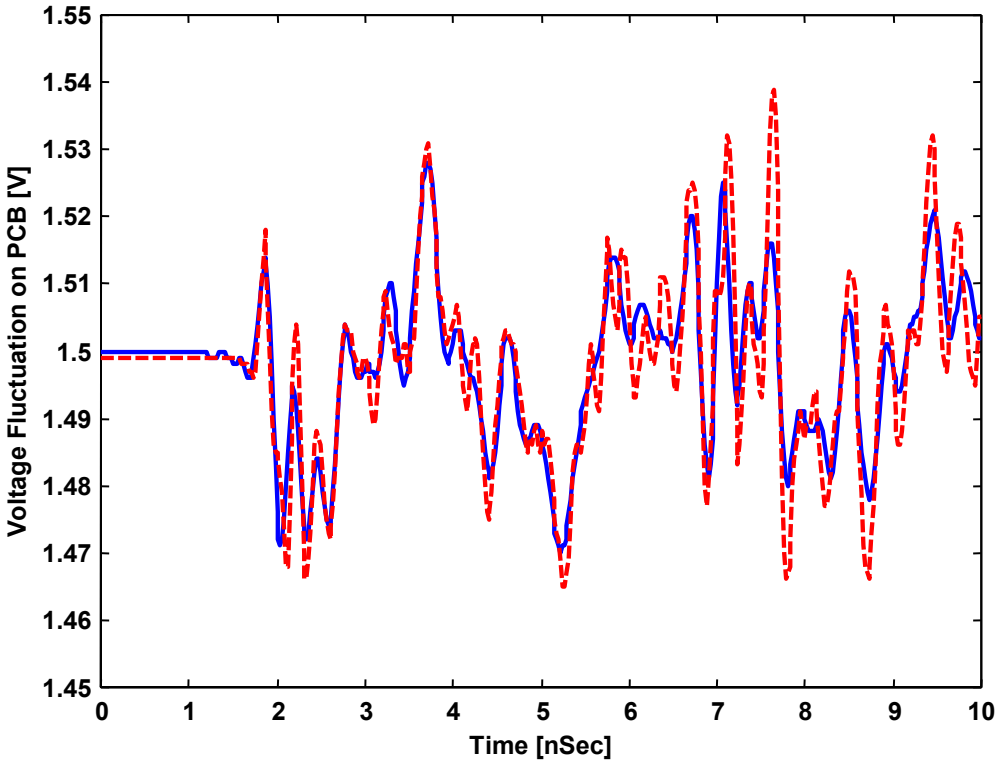


Figure 5.4 Power Supply Voltage Fluctuation on PCB; Resonator Model (Solid), Transmission Line Model (Dashed)

As shown in Figure 5.2, 5.3, and 5.4, the SSN at all levels of assembly, i.e. chip/package/PCB structure, can be observed using the modeling method. Table 5.2 shows the CPU time for two modeling methods. As shown in Table 5.2, the cavity resonator (CR) method requires a smaller CPU time than the transmission line (TL) method. This is because the CR method is based on a gridless approach, whereas the TL

method is based on the spatial granularity of the transmission line grid, which in turn increases computation time for obtaining accuracy.

Modeling Method	CPU Time
Cavity Resonator Model	258.79 Sec
Transmission Line Model	657.61 Sec

Table 5.2 CPU Time for Two Modeling Methods

5.2 System - II

The system in Figure 5.1 has been expanded for multi-layered packages in this section. Figure 5.5 shows the system. The package consists of four planes (Vdd1, Gnd1, Vdd2 and Gnd2). The two power planes can mimic different voltage levels with separate ground planes, which is typical in computer systems. Two Vdd (Vdd1 and Vdd2) and two Gnd (Gnd1 and Gnd2) planes are connected using a via with an inductance of 160 pH.

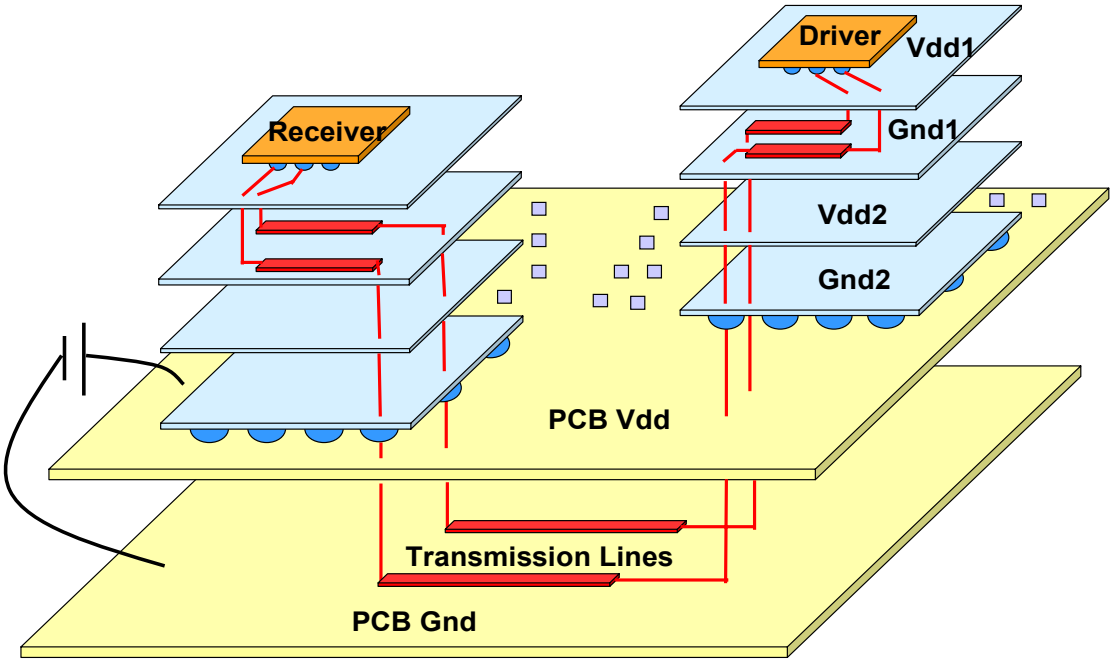


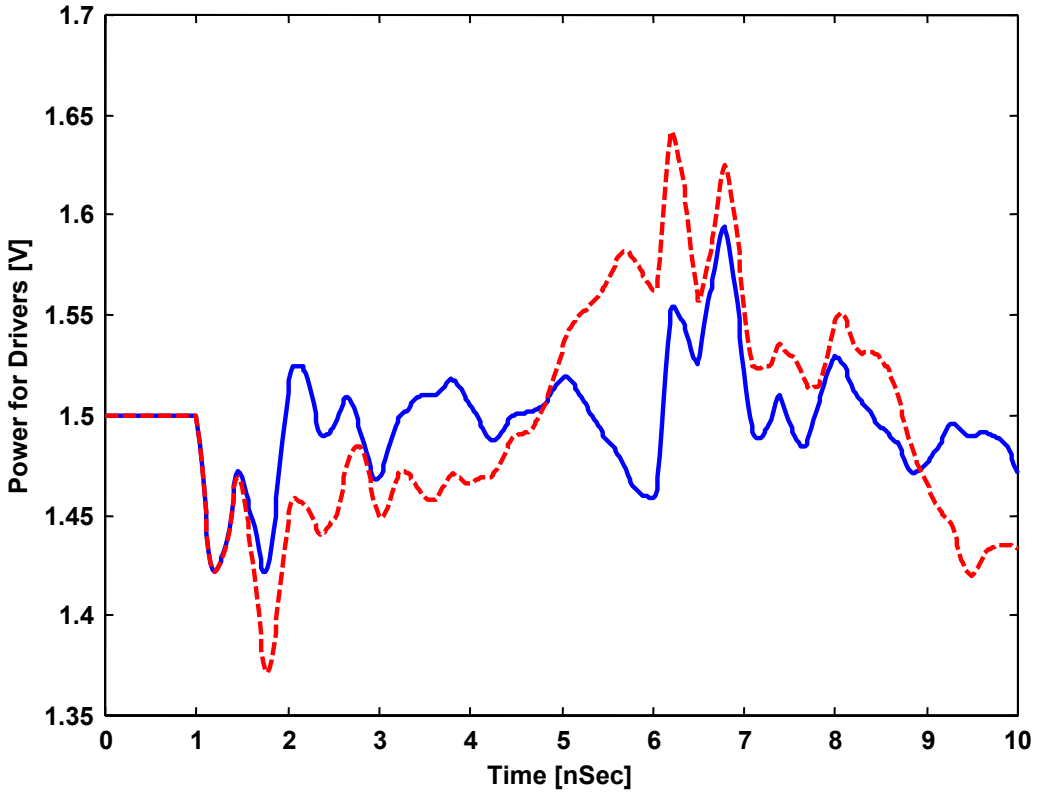
Figure 5.5 System with Multi-Layered Packages

The drivers were supplied with power from the Vdd2/Gnd2 plane pair in the package. A total of 32 solder balls were used to connect between the package and PCB planes.

Figure 5.6 shows the noise measured on the power supply planes. Figure 5.6 (a) is the noise measured on the package planes, i.e. between Vdd2 and Gnd2 planes, near the driver. The noise measured on the package planes, between Vdd2 and Gnd2 planes, near the receiver is shown in Figure 5.6 (b).

In Figure 5.6 (a) and 5.6 (b), the noise on the power supply is also shown when the number of solder balls is reduced from 32 to 4. As can be seen in Figure 5.6, a smaller

noise was observed for larger number of solder balls. The solder balls carry the return currents of the signal transmission lines. Hence, more solder balls translate to more return current paths, resulting in less noise due to a smaller inductance. The modeling technique used in this dissertation can therefore be used to optimize the signal : power : ground ratio for the solder balls for minimizing the simultaneous switching noise in the system.



(a)

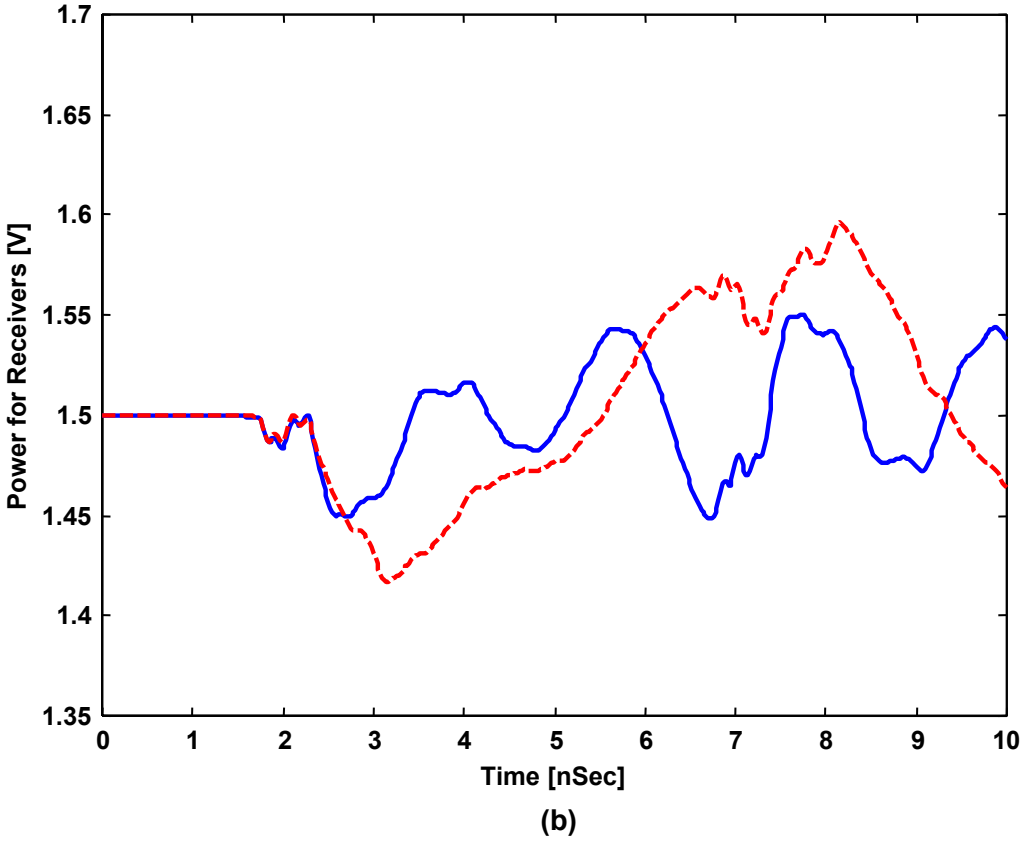


Figure 5.6 Power Supply Fluctuation for Different Number of Power Balls: (a) Near Driver (b) Near Receiver; 32 Power Balls (Solid), 4 Power Balls (Dashed)

5.3 Summary

In this chapter, an extension of the modeling method described in earlier chapters to large systems has been demonstrated. Systems containing chips on packages on board have been modeled to simulate plane bounce and its effect on driver and receiver switching. The packages and board in the systems contain conducting planes, which have been modeled using the cavity resonator method. The modeling results have been compared with the conventional transmission line method, demonstrating the smaller

CPU time required due to the absence of the grid in the cavity resonator method. It has been shown that by using the modeling method, the SSN at all levels of assembly, i.e. chip/package/PCB structure, can be observed, which enables the simulation of electronics in a system. It has also been shown from the simulation that smaller noise can be achieved by using a larger number of solder balls, which provides more return current paths for the signal transmission lines. Hence, the simulation technique can be used to optimize the signal : power ratio of the solder balls.

CHAPTER 6

Model to Hardware Correlation for a Functioning Computer System

In modern computer systems, the power distribution for core circuitry and I/O driver circuitry are separated to accommodate different power supply voltages. This chapter discusses measurement of noise in both the core and I/O driver power distribution system (PDS) for a high speed functioning computer system from Sun Microsystems, as shown in Figure 6.1. The PDS for core circuitry included two 750 MHz microprocessors, a heat sink, a pair of core vdd/gnd planes, and 195 decoupling capacitors between the core vdd/gnd planes. The PDS for the I/O driver circuitry included 402 drivers, 402 transmission lines in eight layers, three pairs of I/O vdd/gnd planes and 178 decoupling capacitors between the I/O vdd/gnd planes. The cross section of the system is shown in Figure 6.2. The characteristics of the noise waveforms on the two systems are different from each other. The transfer impedance of each PDS was measured and the noise on the PDS was also measured in both the frequency and time domain. The modeling methods described in the previous sections have been applied to model these noise waveforms.

The purpose of this chapter is to demonstrate that simple models described in the previous chapters can be applied to complex systems for modeling switching noise.

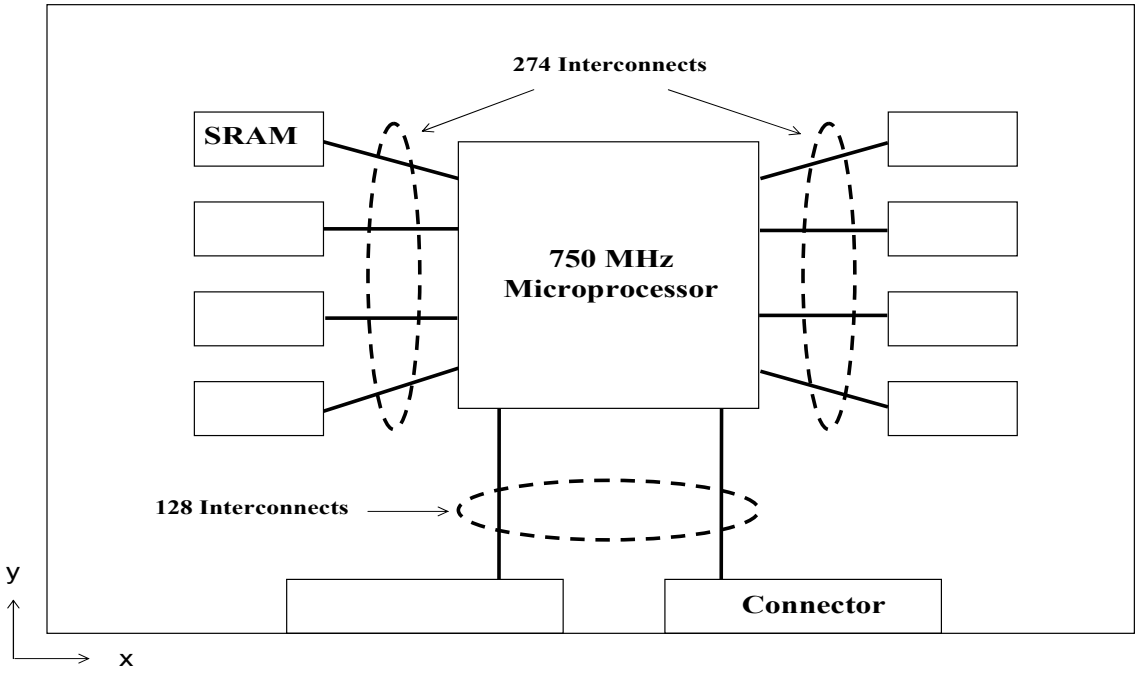


Figure 6.1 Top View of Functioning Board

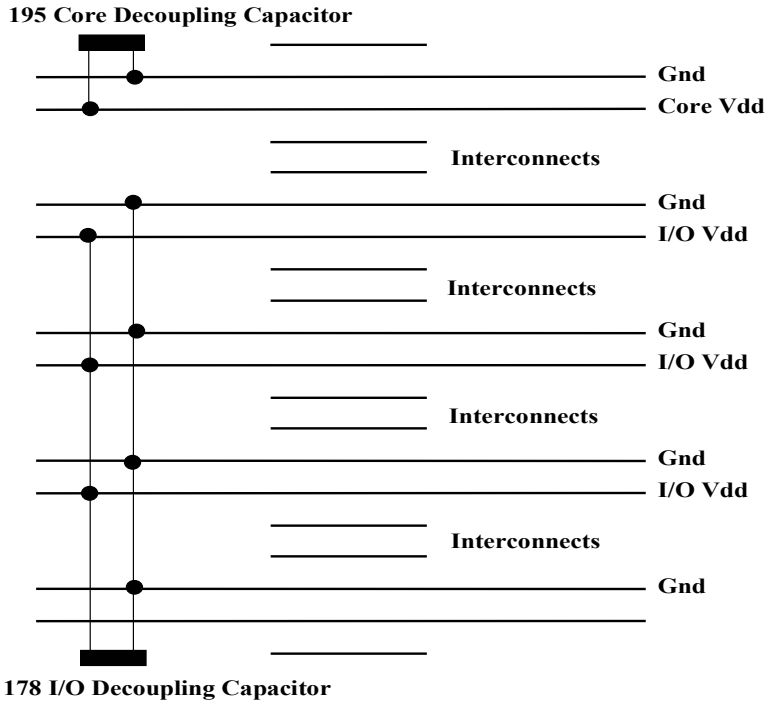


Figure 6.2 Cross Section of the Functioning Board

6.1 Core PDS Noise

The core PDS is used to supply clean power to the active circuit in the chip. Any voltage fluctuation on the core power supply rail, which exceeds the noise tolerance of the circuit, can cause the mal functioning of systems. In this section, characteristics of the noise waveforms in the core PDS have been investigated.

The impedance measurement was made with a vector network analyzer (VNA) as described in [43]. Figure 6.3 shows a diagram of the measurement details. The VNA was initially calibrated by soldering the 50 ohm coaxial transmission lines associated with Port 1 and Port 2 together with no device under test. This step was required for a "through" calibration, to set the reference level at 0 dB. The characteristic impedance of the parallel combination of the two coaxial transmission lines is 25 ohms, which is the reference impedance for the measurements. The transmission lines were then soldered to vias connected to the printed circuit board (PCB) power planes. The transmission coefficient from Port 1 to Port 2, S_{21}, was measured and the transfer impedance, Z_{trans}, was calculated from the magnitude of S_{21} (in dB) using the equation:

$$\left|S_{21}\right| = 20\log_{10}\frac{\left|Z_{trans}\right|}{25ohms} \tag{6.1}$$

$$\left|Z_{trans}\right| = 25\times 10^{\frac{\left|S_{21}\right|}{20}} \tag{6.2}$$

These equations are valid when the plane impedance is much less than 25 ohms.

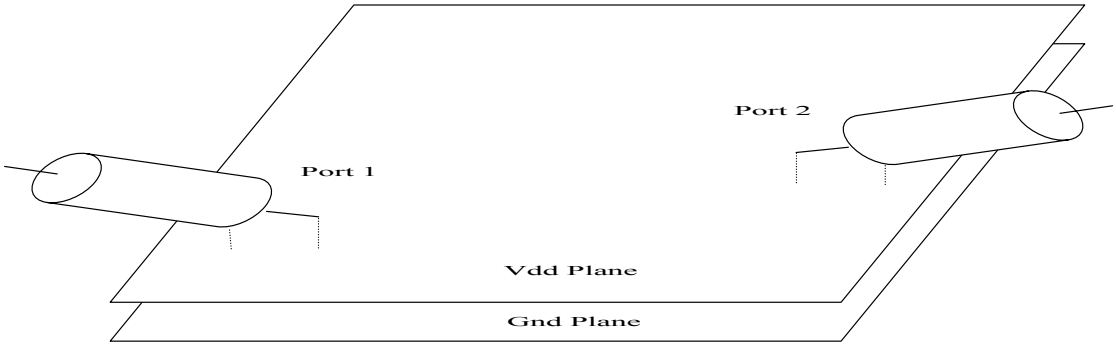


Figure 6.3 Measurement of PCB Power Planes

A resonator circuit model described in the previous section was constructed for modeling the planes. The modes used for the circuit model were $0 \leq m \leq 11$ and $0 \leq n \leq 4$. HSPICE simulations were performed by injecting 1 AC ampere of current into the power planes at one position, measuring the voltage at another position and dividing voltage by current to obtain the transfer impedance. Figure 6.4 shows the measured and simulated transfer impedance for a pair of 9.44 x 4.13 square inch power planes spaced 2 mils apart, which was used to power the core circuitry in Figure 6.2. Port 1 and 2 were located at (x=3.9 in, y=3.0 in) and (x=5.6 in, y=3.0 in), respectively, on the power planes. The dielectric was FR4 with a dielectric constant of 5.05 and loss tangent of 0.018. There were no components attached to the PCB planes; only the power planes were present in this measurement. PCB power planes are two parallel plates of conducting material, which form a parallel plate capacitor [44]. As can be seen in the measurement in Figure 6.4, the plane pair is capacitive at low frequencies, and then resonates above 100 MHz, as appropriate for the parallel plate dimensions. The circuit model used correctly simulates both the capacitance at low frequency and the cavity resonances at higher frequencies.

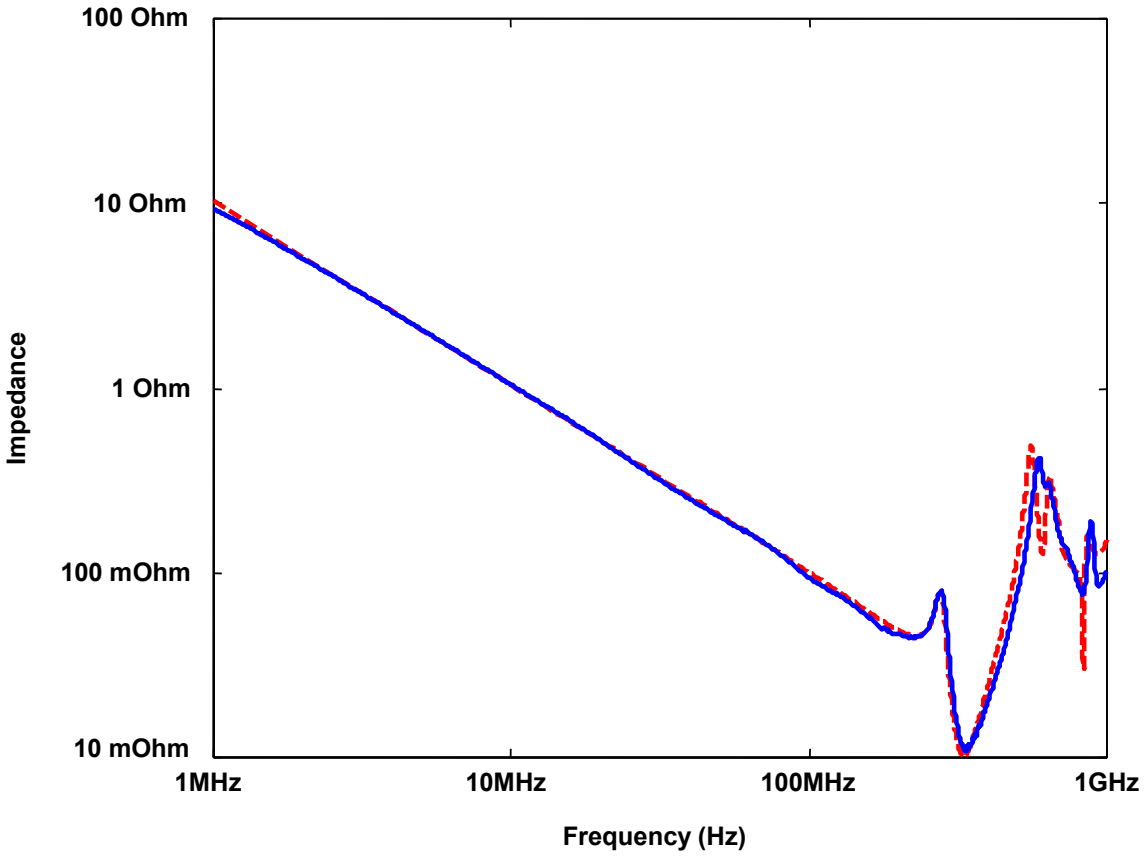


Figure 6.4 Model to Hardware Correlation for Transfer Impedance of Bare PCB Core Power Planes: Solid (Measurement), Dashed (Simulation)

The stuffed PCB core power planes were next measured using the VNA method described earlier. The core power planes were used to supply power to the 750 MHz microprocessors. The module was not biased for this measurement. Port 1 and 2 were located at (x=3.0 in, y=0.3 in) and (x=6.5 in, y=0.8 in), respectively for the measurement. A total of 195 decoupling capacitors were distributed between the core vdd and gnd planes. The 195 decoupling capacitors consisted of twenty-four different values of capacitors with varying equivalent series inductance (ESL) and equivalent series resistance (ESR). Table 6.1 shows the measured values for C, ESR, and ESL of the

capacitors used. The resonance frequencies for these decoupling capacitors varied from 332 KHz to 1.5 GHz.

	C	ESR (mOhms)	ESL (nH)
A	27 pF	850.0	0.4
B	33 pF	700.0	0.4
C	130 pF	373.4	0.458
D	174.4 pF	313.1	0.509
E	207.1 pF	243.1	0.468
F	304.7 pF	148.6	0.413
G	511.4 pF	139.8	0.4
H	595.8 pF	120.0	0.432
I	1.0 nF	75.0	0.370
J	2.2 nF	62.1	0.426
K	2.9 nF	203.8	0.533
L	4.2 nF	141.1	0.523

	C	ESR (mOhms)	ESL (nH)
M	8.2 nF	88.9	0.519
N	19.8 nF	44.3	0.572
O	41.1 nF	25.7	0.435
P	83 nF	19.9	0.416
Q	179 nF	15.9	0.548
R	379 nF	14.1	0.543
S	0.81 uF	9.8	0.485
T	1.93 uF	6.7	0.686
U	3.86 uF	4.8	0.703
V	7.87 uF	5.5	0.876
W	21.2 uF	2.7	1.628
X	81.2 uF	2.4	2.834

Table 6.1 Measured Values of C, ESR, and ESL

The resonator circuit model for the planes with 195 decoupling capacitors at the appropriate locations was constructed and simulated in HSPICE. The measured values of capacitance, ESL and ESR in Table 6.1 were used for the construction of series RLC circuit models for the discrete capacitors. Figure 6.5 shows the measured and simulated transfer impedance of the stuffed PCB core power planes.

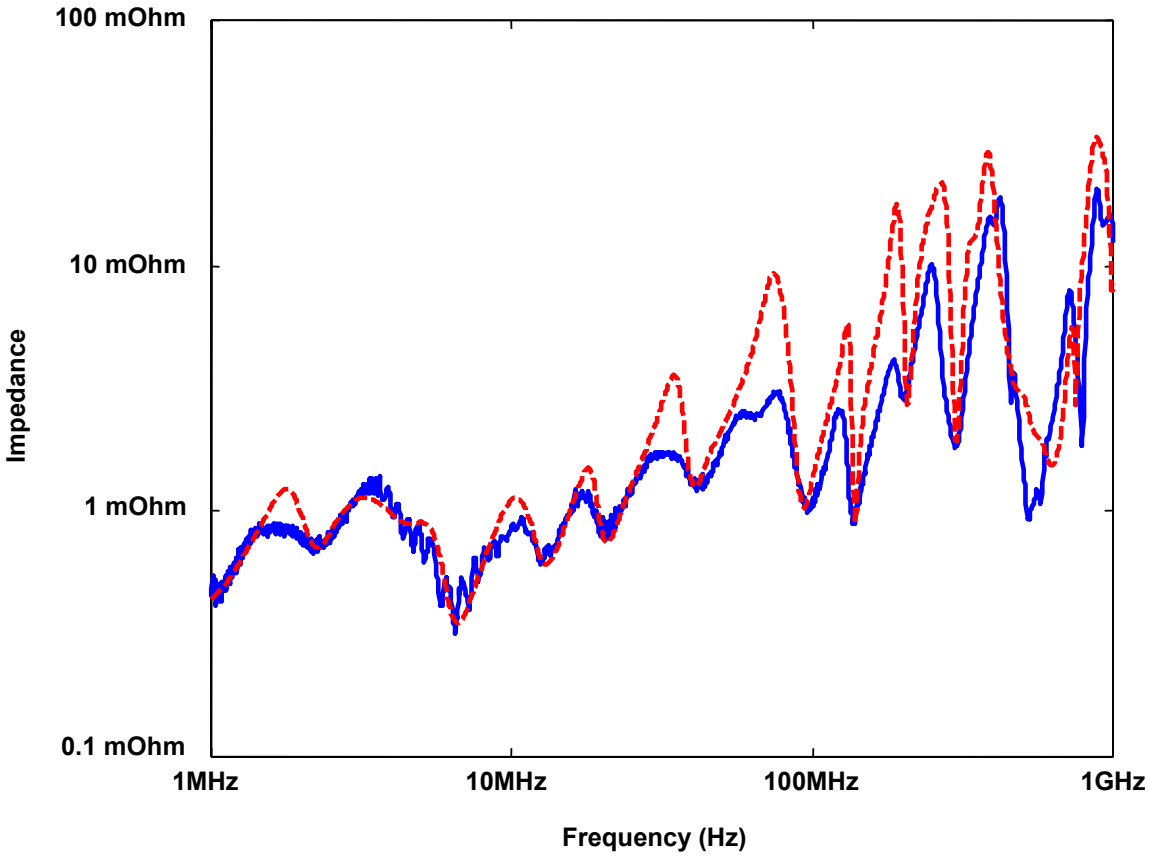


Figure 6.5 Model to Hardware Correlation for Transfer Impedance of Stuffed PCB Core Power Planes: Solid (Measurement), Dashed (Simulation)

As shown in Figure 6.5, 195 decoupling capacitors, connected in parallel to the core vdd/gnd planes, enable the power planes to maintain a transfer impedance less than 10 mOhm upto 350 MHz. Good model to hardware correlation was obtained at all frequencies except at some of the impedance peaks. These peaks are due to the inductance and capacitance of the 195 discrete decoupling capacitors. Distributed circuit models for the discrete decoupling capacitors are therefore required to obtain a better match at the impedance peaks [45].

Figure 6.6 shows a schematic of the system when it is powered with a voltage regulator module (VRM). The 750 MHz microprocessors are powered using the 1.8 V core vdd/gnd planes. Software compiling matrices of random orders was run on the microprocessors to ensure that the microprocessors were not idle. Two ports were defined, as shown in the schematic in Figure 6.6. Port 1 was located away from the microprocessors and Port 2 was located under the microprocessors, which was the closest point to the microprocessors on the PCB core power planes.

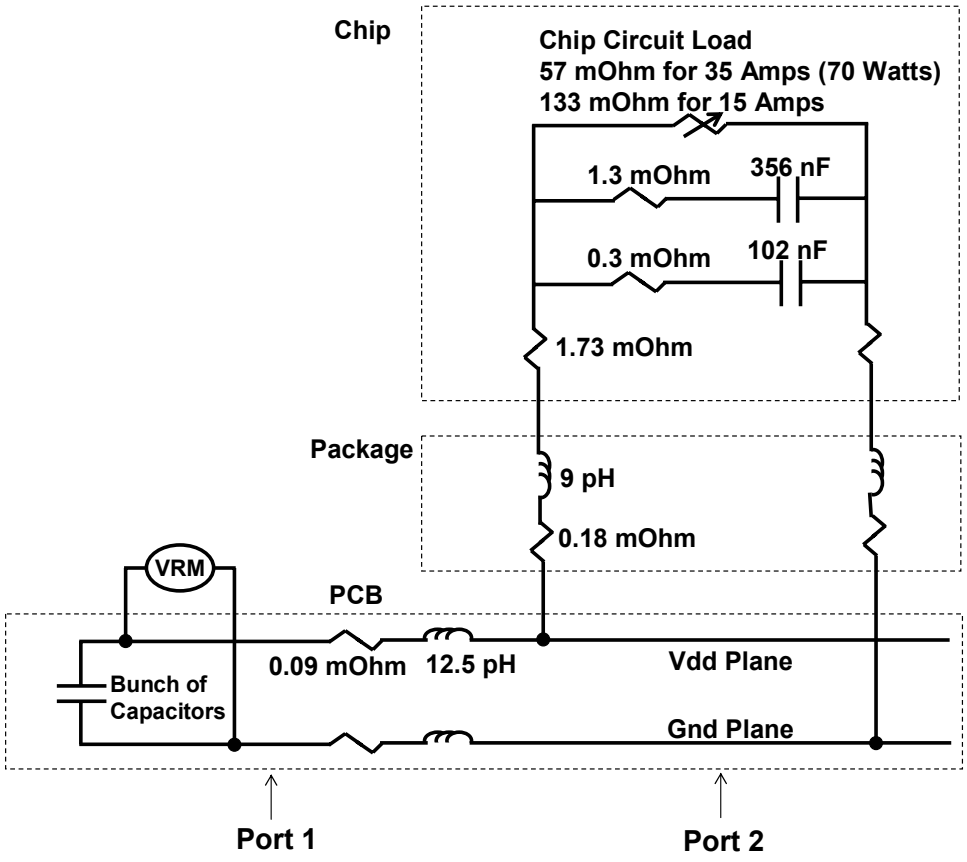
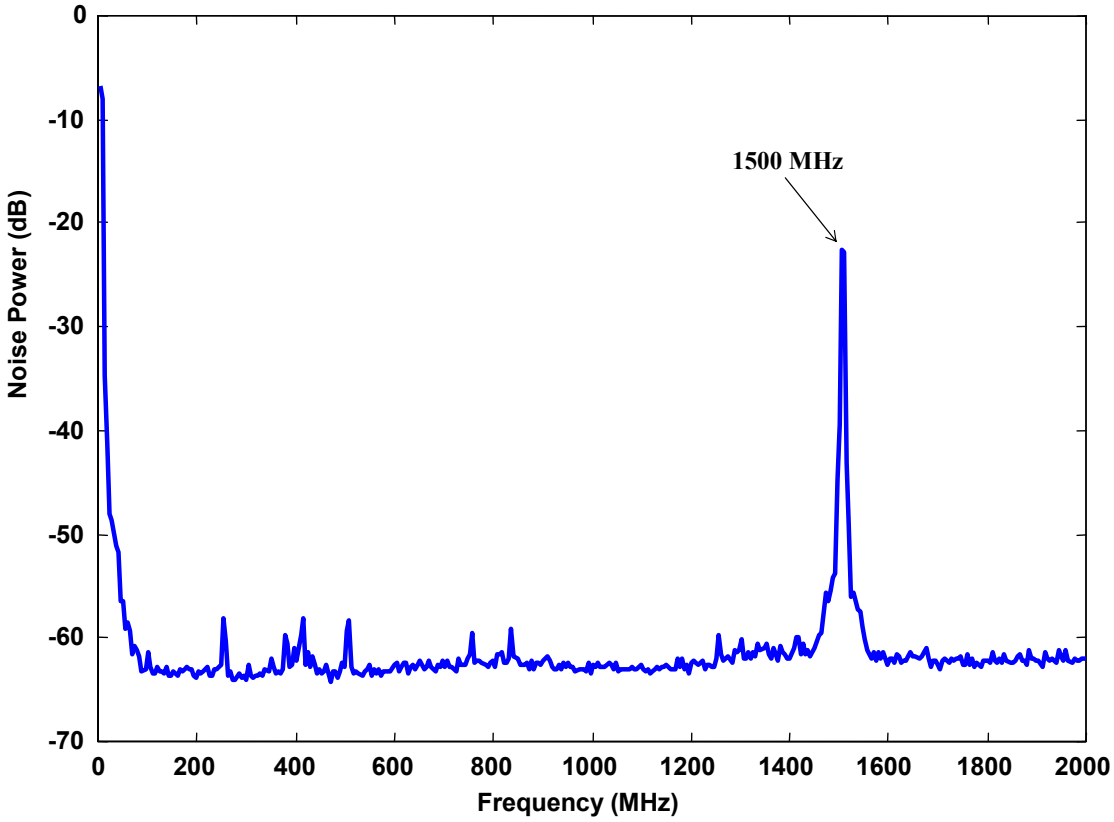
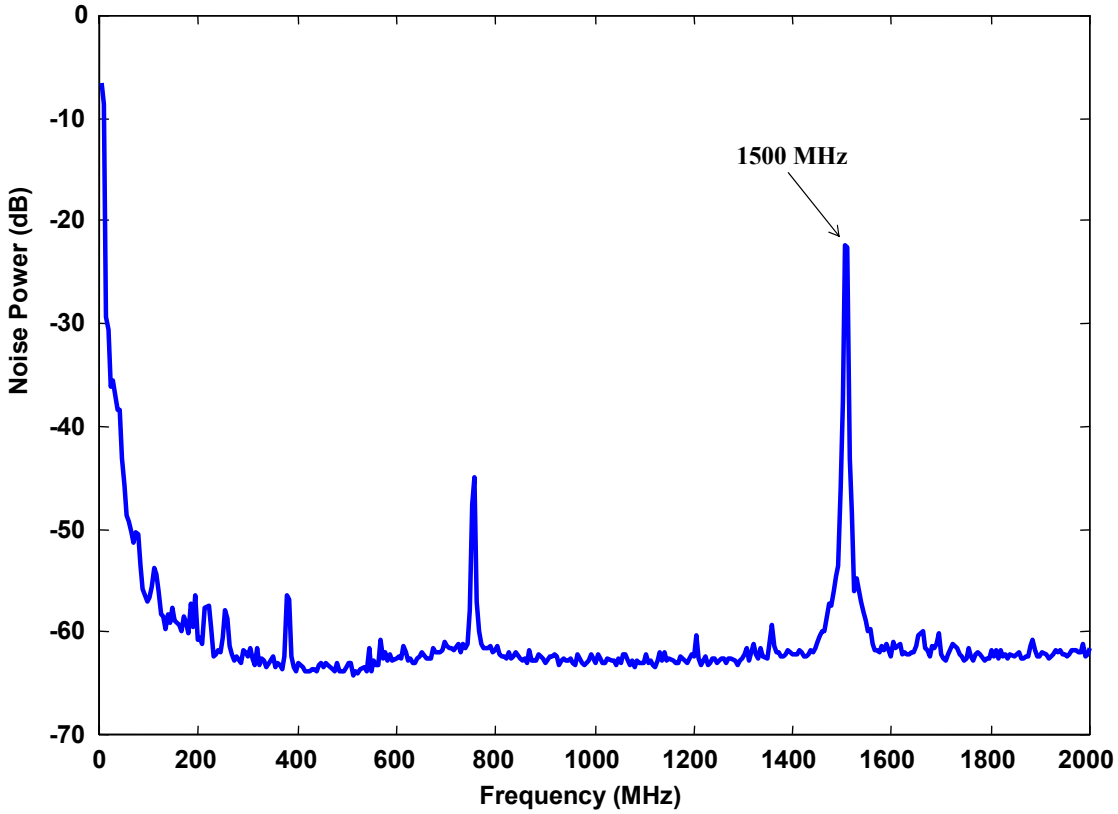


Figure 6.6 Circuit Schematic from Physical Structure

A spectrum analyzer was used to measure the noise on the functioning PCB core power planes in the frequency domain. The spectrum analyzer was set in "Max Hold" mode to record the maximum noise that occurred. The results at Port 1 and Port 2 are shown in Figure 6.7.



(a)



(b)

Figure 6.7 (a) Measured Core Noise of Functioning Board in the Frequency Domain at Port 1 (b) Measured Core Noise of Functioning Board in the Frequency Domain at Port 2

As can be seen in Figure 6.7, the maximum noise on the core PDS occurs at 1500 MHz, which is twice the clock frequency of the microprocessors. For the 750 MHz clock, the change in the current, drawn by the microprocessors, occurs both at its rising and falling edges, as shown in Figure 6.8. Hence, a 1500 MHz periodic change in the transient current causes the noise on the core PDS, as shown in Figure 6.7.

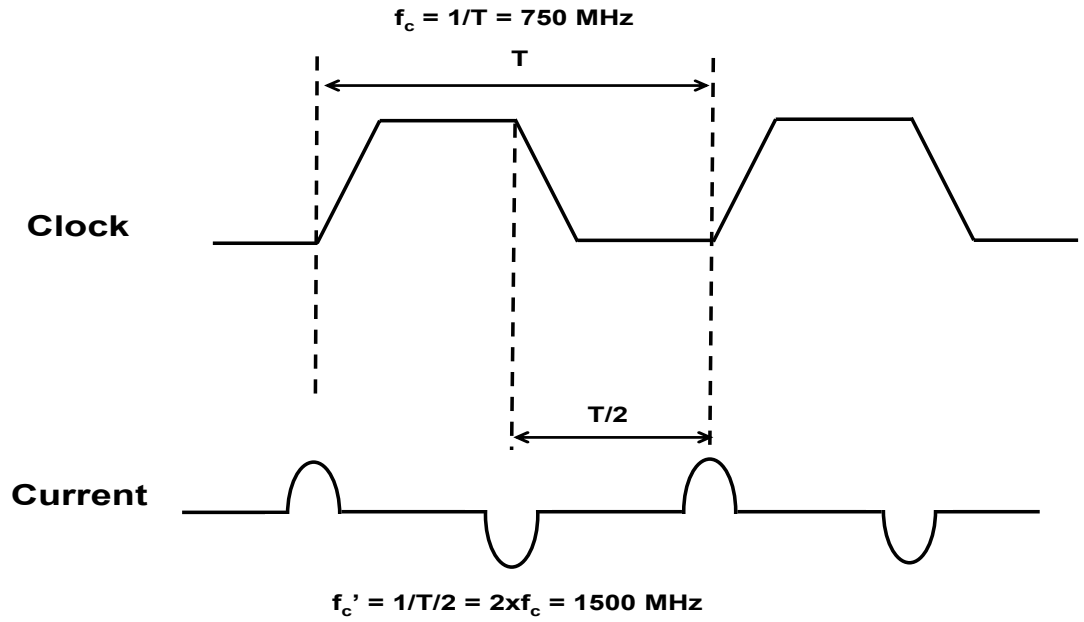
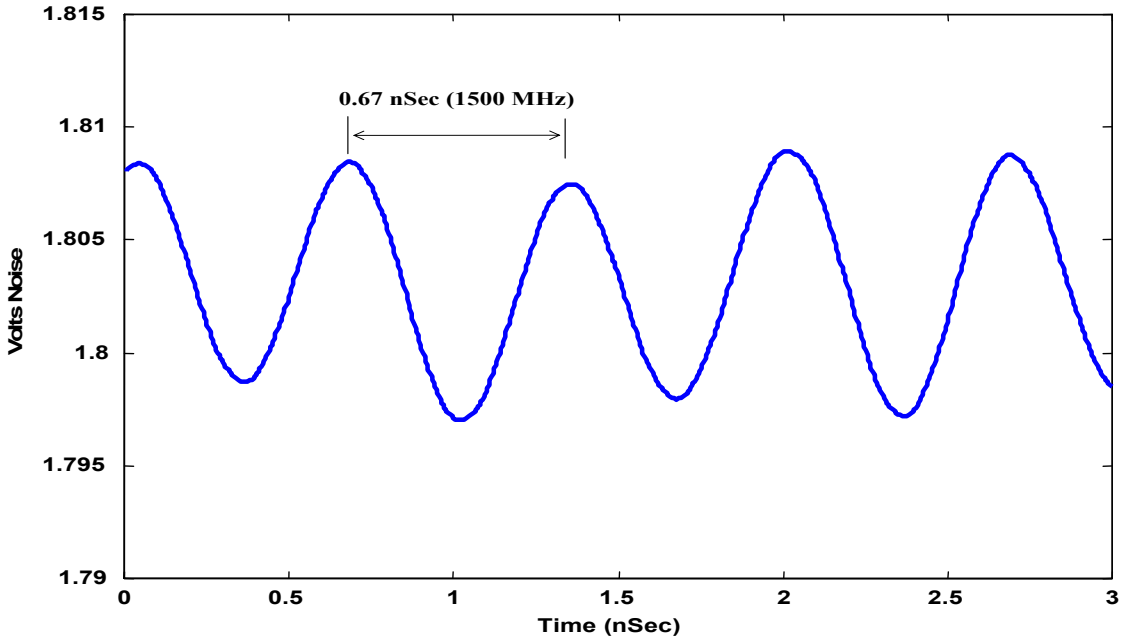
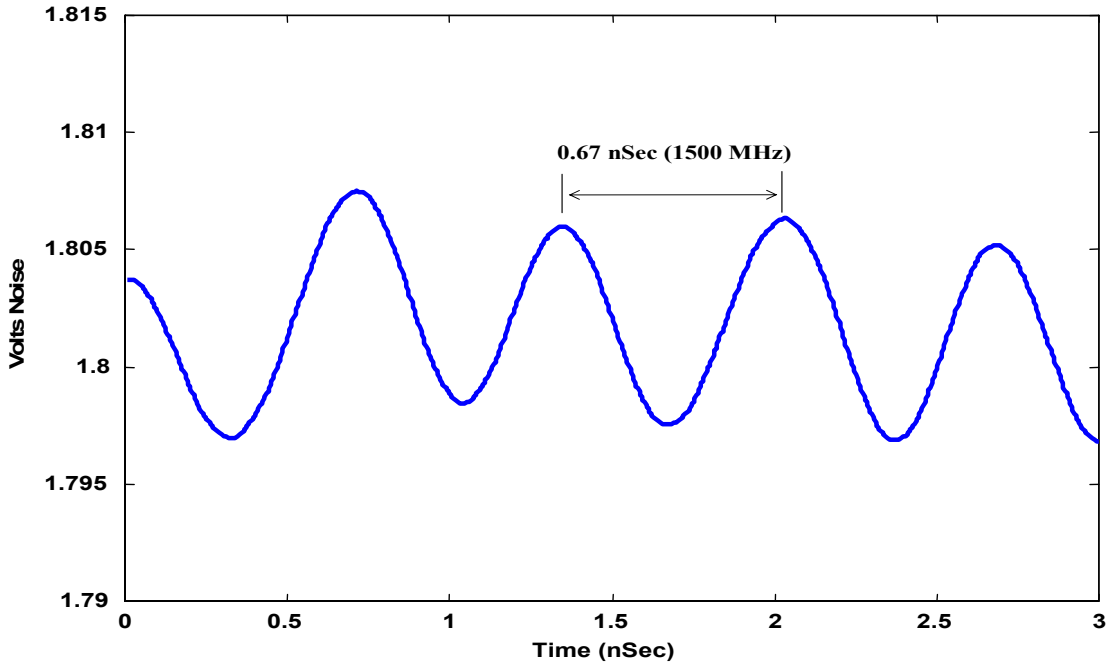


Figure 6.8 Change in the Current that Microprocessors are Drawing for 750 MHz Clock

The core PDS noise on the functioning board in the time domain was measured using an oscilloscope. Figure 6.9 shows the results.



(a)

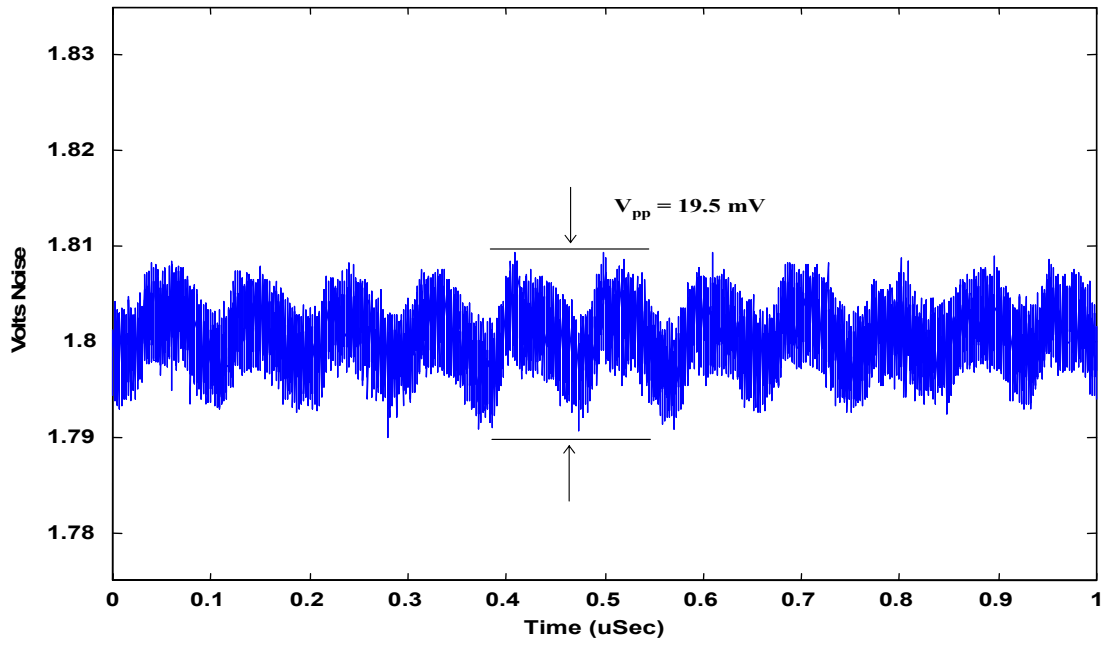


(b)

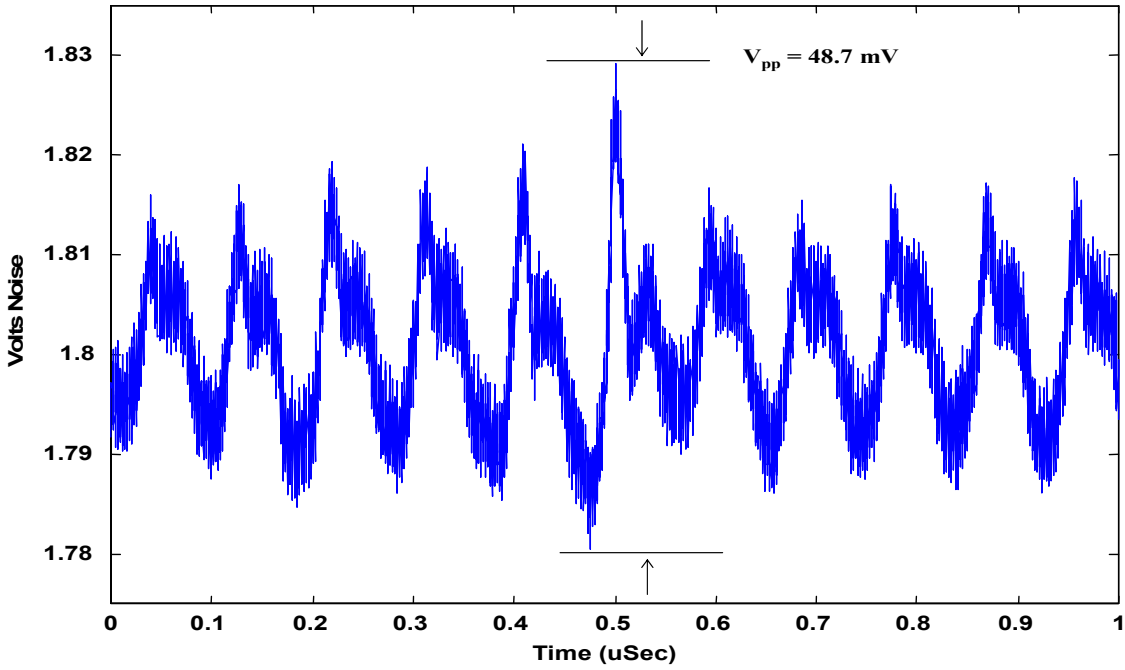
Figure 6.9 (a) Measured Core Noise of Functioning Board in the Time Domain at Port 1 (b) Measured Core Noise of Functioning Board in the Time Domain at Port 2

Both time domain measurements on Port 1 and Port 2 clearly show the 0.67 nSec periodic noise, which corresponds to a frequency of 1500 MHz. This represents twice the clock frequency of the microprocessors and is consistent with the measurements using the spectrum analyzer.

The maximum peak-to-peak noise (V_{pp}) voltage for the core PDS was measured using an oscilloscope, the results of which are shown in Figure 6.10. The maximum peak-to-peak noise of 19.5 mV was measured on the functioning core PDS away from the microprocessors and 48.7 mV was measured under the microprocessors. These noise voltages correspond to ±0.54 % and ±1.35 % of the 1.8 V core power supply, respectively.



(a)



(b)

Figure 6.10 (a) Measured Peak-to-Peak Core Noise of Functioning Board at Port 1:V_{pp} = 19.5 mV (b) Measured Peak-to-Peak Core Noise of Functioning Board at Port 2:V_{pp} = 48.7 mV

6.2 I/O PDS Noise

In high speed computer systems, the PDS for I/O drivers is often separated from that for the microprocessor core. This is to ensure isolation between the two power distribution networks. Simultaneous switching of hundreds of drivers causes noise on the PDS, which results in voltage fluctuation across the power supply rails of the circuits. This causes signal integrity problems affecting the data on the signal transmission lines. In this section, measurement and modeling of switching noise for output drivers driving transmission lines in a multi-layered functioning board containing planes have been described. The PDS for the driver I/Os in the system contained eight layers that were used for signal transmission lines. These transmission lines were driven by 402 drivers and included 274 transmission lines between the microprocessor and SRAMs and 128 transmission lines between the microprocessor and connectors, as shown in Figure 6.1. The cross-section of the board consisted of three vdd planes and three gnd plane, where all the vdd planes and gnd planes were connected together to have the same dc level, as shown in Figure 6.2. The dielectric used between the I/O power planes was FR4 with a thickness of 2 mils. A total of 178 decoupling capacitors were distributed between the I/O vdd and gnd planes.

The stuffed PCB I/O power planes were measured using a VNA. Port 1 and 2 were located at (x=4.1 in, y=0.3 in) and (x=5.3 in, y=3.9 in), respectively for the measurement. The resonator circuit model for the planes with 178 decoupling capacitors

at their corresponding locations was constructed and simulated in HSPICE. The equivalent thickness of n power plane pairs in parallel is given as [42]

$$t_{equivalent} = \frac{1}{\frac{1}{t_1} + \frac{1}{t_2} + ... + \frac{1}{t_n}} \tag{6.3}$$

Thus, three pairs of power planes with 2 mil thick dielectric in the I/O PDS system have been treated as one pair of power planes with 0.667 mil thick dielectric in the model to reduce the size of the circuit. This simple approach assumes that the dielectric constant is the same for the plane pairs and that many low inductance vias are used to connect the power plane pairs in parallel, minimizing the vertical inductance. Figure 6.11 shows the measured and simulated transfer impedance of the stuffed PCB I/O power planes.

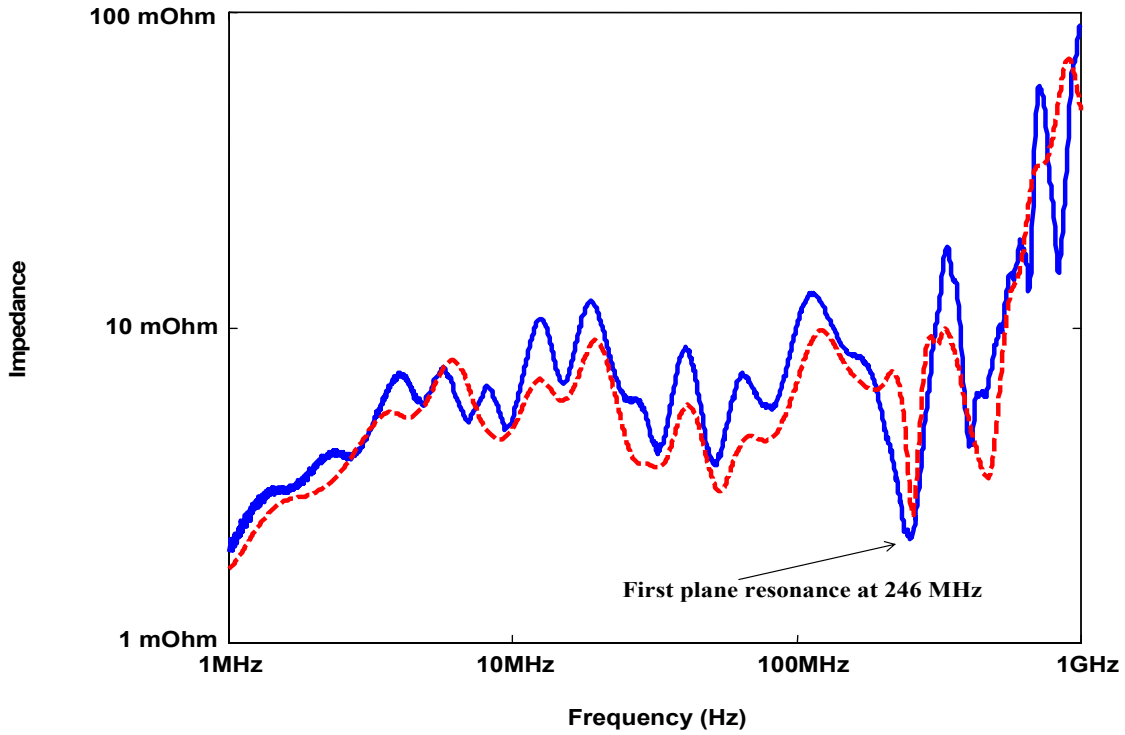


Figure 6.11 Model to Hardware Correlation for Transfer Impedance of Stuffed PCB I/O Power Planes: Solid (Measurement), Dashed (Simulation)

As shown in Figure 6.11, the first plane resonance occurs at 246 MHz. The resonances below that frequency are due to the inductance and capacitance of the discrete decoupling capacitors.

Measurements were conducted at Port 2 on the functioning I/O power distribution system (PDS). 402 drivers on the chip were powered by using the 1.5 V I/O vdd/gnd planes. Of these drivers, 274 were used for driving the transmission lines with a bus frequency of 250 MHz between the microprocessor and SRAMs. The remaining 128 drivers were driving the transmission lines with a bus frequency of 125 MHz between the microprocessor and connectors. These transmission lines were located between the I/O vdd and gnd planes.

Maximum noise that occurred on the functioning PCB I/O power planes was measured in the frequency domain using the spectrum analyzer, as shown in Figure 6.12.

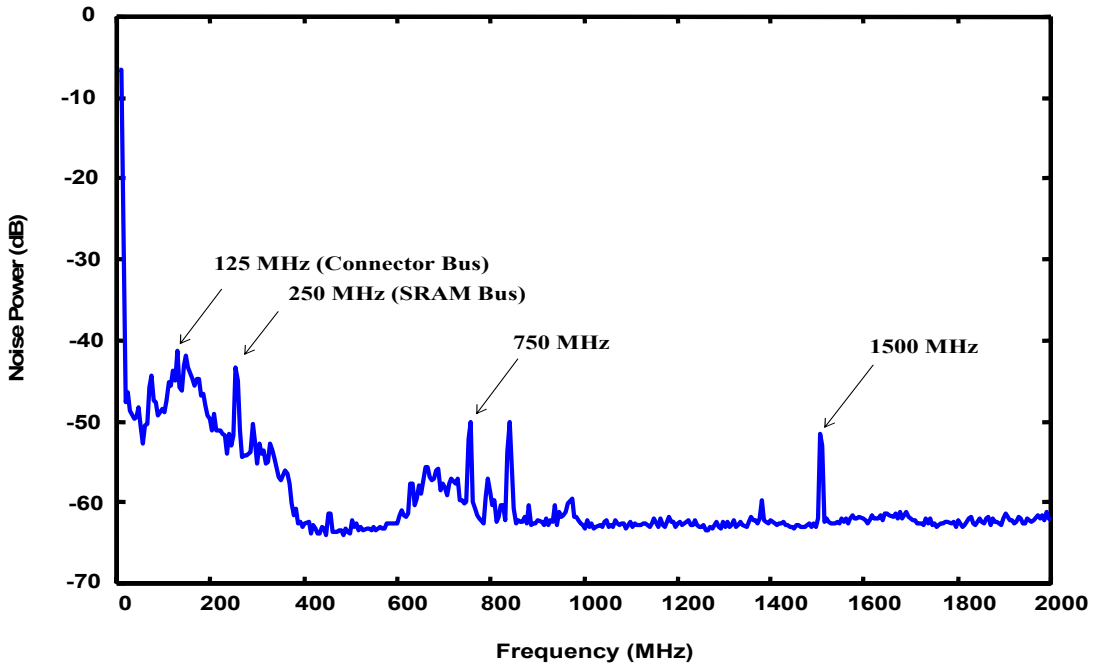


Figure 6.12 Measured I/O Noise of Functioning Board in the Frequency Domain at Port 2

As shown in Figure 6.12, there are noise peaks at 750 MHz, which corresponds to the clock frequency of the microprocessor and at 1500 MHz, which corresponds to twice the clock frequency of the microprocessor. However, the maximum noise occurred at 125 MHz and 250 MHz, which are the bus frequencies of the connector bus and SRAM bus, respectively.

At high speed, the return current is on a reference plane that is in close proximity to the signal transmission line, minimizing the total loop area between the outgoing and returning current paths, as explained in Chapter 2.3. Thus, the transmission lines, which were embedded between the I/O vdd and gnd planes, reference both vdd and gnd planes while carrying the signal. The reference planes of the transmission lines are not perfect and they bounce as return currents from the transmission lines accumulate and charge the parallel plate capacitance, causing waves to propagate between the vdd and gnd planes [2], [21]. This is the reason why the noise at the bus frequencies are dominant on the I/O vdd/gnd planes, as shown in Figure 6.12.

The power distribution induced I/O noise at port 2 was measured using an oscilloscope in the time domain. The model for the transmission line, described in Chapter 2.3, was constructed and incorporated using two transmission lines in parallel, each with twice the characteristic impedance of Z_0, for the signal transmission lines that were located between the I/O vdd and gnd planes. Twelve transmission lines, including 8 transmission lines from the SRAM buses and 4 transmission lines from the connector buses, were selected for simulation. The Z_0 of each transmission line was scaled down accordingly to ensure that the transient current in the reduced circuit matched the original

circuit. The modeling methodology for the functioning system employed the superposition of circuit models for planes and transmission lines as described earlier. This approximation is based on the skin depth approximation, which accounts for the return currents correctly. The models for the drivers and power supply were incorporated, and the entire circuit was simulated in the time domain. Figure 6.13 shows the measured and simulated results for the I/O PDS noise [46].

The return currents on the reference planes accumulate time-varying charges, which act as vertical current sources. The radial electromagnetic wave excited by these current sources cause the vdd/gnd planes to bounce, resulting in voltage fluctuations on the I/O vdd/gnd planes [2], [21], as shown in Figure 6.13. This effect has been captured well by the simplified circuit model.

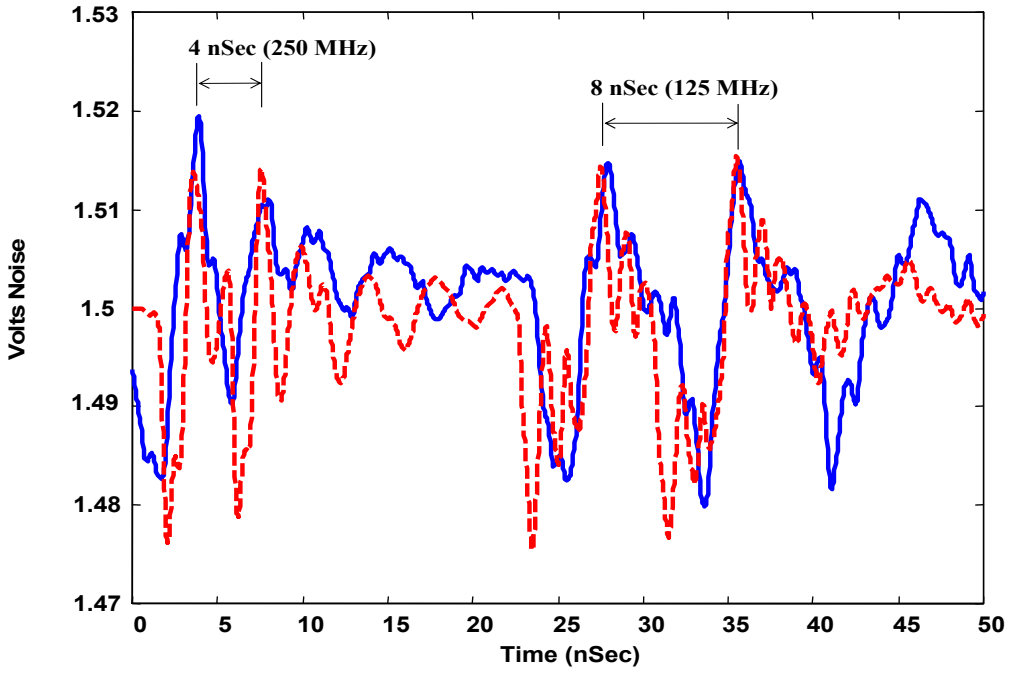


Figure 6.13 Model to Hardware Correlation for Power Distribution Induced I/O Noise: Solid (Measurement), Dashed (Simulation)

In the system, the maximum peak-to-peak noise (V_{pp}) voltage of 40 mV was measured when 402 drivers were switched simultaneously. It is obvious in Figure 6.13 that the 4 nSec periodic noise is due to the SRAM bus which carries the signal at 250 MHz and the 8 nSec periodic noise is due to the connector bus which carries the signal at 125 MHz. Considering that the measurements are on a functioning computer system (and not an experimental Test Vehicle), the simulation results show good model to hardware correlation. The CPU time required for the time domain simulation of the circuit in HSPICE was 124 Seconds with a 20 pSec time step for a 50 nSec duration.

6.3 Summary

Measurements conducted on a functioning power distribution system (PDS) with 750 MHz microprocessors were discussed in this chapter. For the core PDS, the noise at twice the clock frequency was the dominant noise both in the frequency and time domain. The transfer impedance of both the core and I/O PDS was simulated by using circuit model for the planes. The simulation results showed good agreement with measurements. For the I/O PDS, both frequency and time domain measurements indicated that I/O switching noise was caused by the return currents flowing on the I/O vdd/gnd planes. The methods described in earlier chapters were applied to model the I/O switching noise in a functioning system in the time domain, which accounted for the return currents correctly. The modeling results showed good agreement with measurements, demonstrating the

application of the methodology discussed in this dissertation for modeling complex and realistic systems.

CHAPTER 7

Placement and Optimization of Decoupling Capacitors

As mentioned earlier, high speed systems require a low power distribution impedance. To maintain a small power distribution system (PDS) impedance over a large frequency bandwidth, decoupling capacitors are required. The properties and usage of decoupling capacitors have been discussed in [47], [48], [49]. The placement of a decoupling capacitor has been discussed in [50] for several configurations, however all the configurations have been limited to the placement of one decoupling capacitor near the active device. High performance systems require thousands of decoupling capacitors to maintain a low power distribution impedance over a large bandwidth. Therefore, developing a methodology for selecting the decoupling capacitors and deciding their location across the entire printed circuit board (PCB) becomes very important.

Based on the previous chapters, decoupling capacitors should be chosen to suppress any resonance peaks in the power distribution impedance over the frequency range of interest. The frequency response of the PDS in modern computer systems show two kinds of resonances. The first resonance is caused by the capacitor inductance and

plane capacitance (LC resonance) and the second resonance is due to the cavity resonance of the planes.

In this chapter, methods for selecting decoupling capacitors have been discussed. In addition, choosing the locations for the decoupling capacitors on the printed circuit board power and ground planes has been described.

7.1 Target Impedance

Based on the allowed ripple on the power supply rails of the chip, the target impedance for the PDS can be calculated as [51]:

$$Z_{target} = \frac{(PowerSupplyVoltage) \times (AllowedRipple)}{Current} \tag{7.1}$$

Using the above equation, the target impedance for various product generations has been calculated in Table 7.1. In the table, a 5% ripple voltage has been assumed. In addition, only 50% of the switching current is assumed at each clock edge for a total of 100% switching current for an entire clock cycle. For example, for the Athalon microprocessor

$$Z_{target} = \frac{1.6 \times 5\%}{31 \times 50\%} = 5.1 m\Omega . \tag{7.2}$$

Year	Product Generation	Voltage (volts)	Power (watts)	Current (amperes)	Z_{target} (mohms)	Frequency (MHz)
1991	386	5	5	1	500	16
1993	486	3.3	10	3	109	66
1996	Pentium I	2.6	25	10	27	300
1999	Athalon	1.6	50	31	5.1	900
2002	Itanium	1.2	150	125	1.0	3000

Table 7.1 Power Distribution System Historical Trends
Courtesy: Larry Smith, Sun Microsystems, USA

The significance of the target impedance is that the power distribution impedance as seen from the microprocessor be less than Z_{target} over a frequency range defined by the operating frequency of the microprocessor. From Table 7.1, the target impedance has been falling ~5x every computer generation. Since computer systems are wideband systems where the microprocessor can run at sub-multiples of the maximum clock frequency, the PDS impedance should not exceed the target impedance from DC to multiple harmonics of the maximum clock frequency. This is illustrated in Figure 7.1 for a system with a target impedance of 2 mΩ. In Figure 7.1, it is assumed that the same power is dissipated at all frequencies. To satisfy the target impedance curve in Figure 7.1, decoupling capacitors have to be selected with care since they add additional resonances to the system, which can exceed the desired target impedance. In addition, when attached

to planes, the resonance between the capacitor inductance and the plane capacitance can shift the target impedance curve upwards.

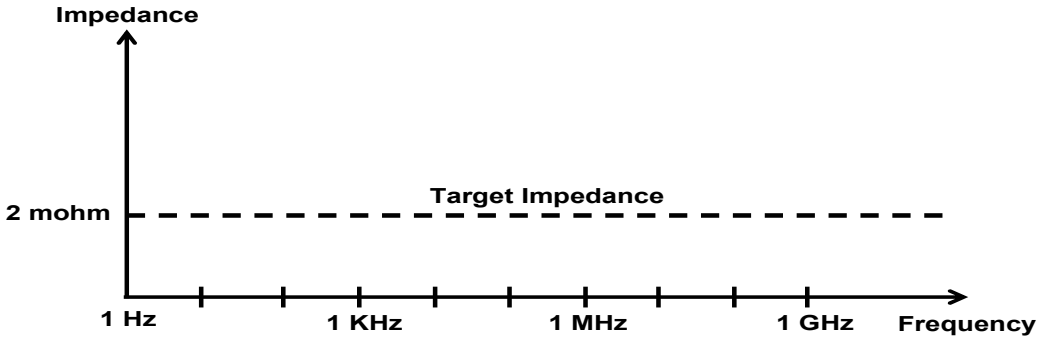


Figure 7.1 Target Impedance to be met over Frequency Range [51]

In this chapter, methods for choosing the decoupling capacitors and their placement on the power and ground planes are described. The analysis is limited to two planes (VDD and ground). However, this methodology can be extended to multi-layered planes.

7.2 LC Resonance

Consider a square plane pair measuring 11 inch x 11 inch with a dielectric thickness of 1mil, as shown in Figure 7.2. The relative dielectric constant (ε_r) and loss tangent are 4 and 0.018, respectively, which correspond to standard FR4 material. A

resonator circuit model with 64 ports, as described in Chapter 2, was constructed for this plane pair. The modes used were $0 \leq m \leq 6$ and $0 \leq n \leq 6$.

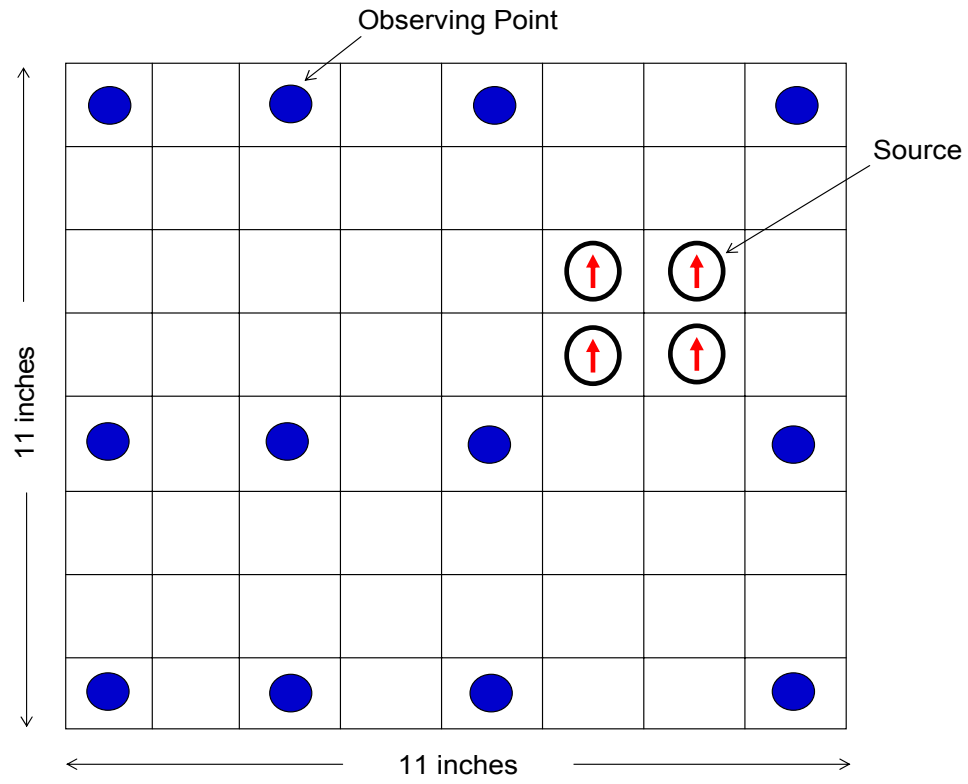


Figure 7.2 11x11 Square Inch Plane Pair

The plane pair was stimulated using four 0.25 ampere current sources, as shown in Figure 7.2. These current sources represent the switching circuits. Since the sum of the current sources is 1 ampere, the voltage measured at any port translates to the transfer impedance between the source point and the observation point. The plane was divided into an 8x8 array of nodes which was uniformly distributed, as shown in Figure 7.2. The simulated impedance was observed at 16 points across the planes which included the 4

current source locations, as shown in Figure 7.2. Figure 7.3 shows the plane impedance with no decoupling capacitors at the 16 observation points.

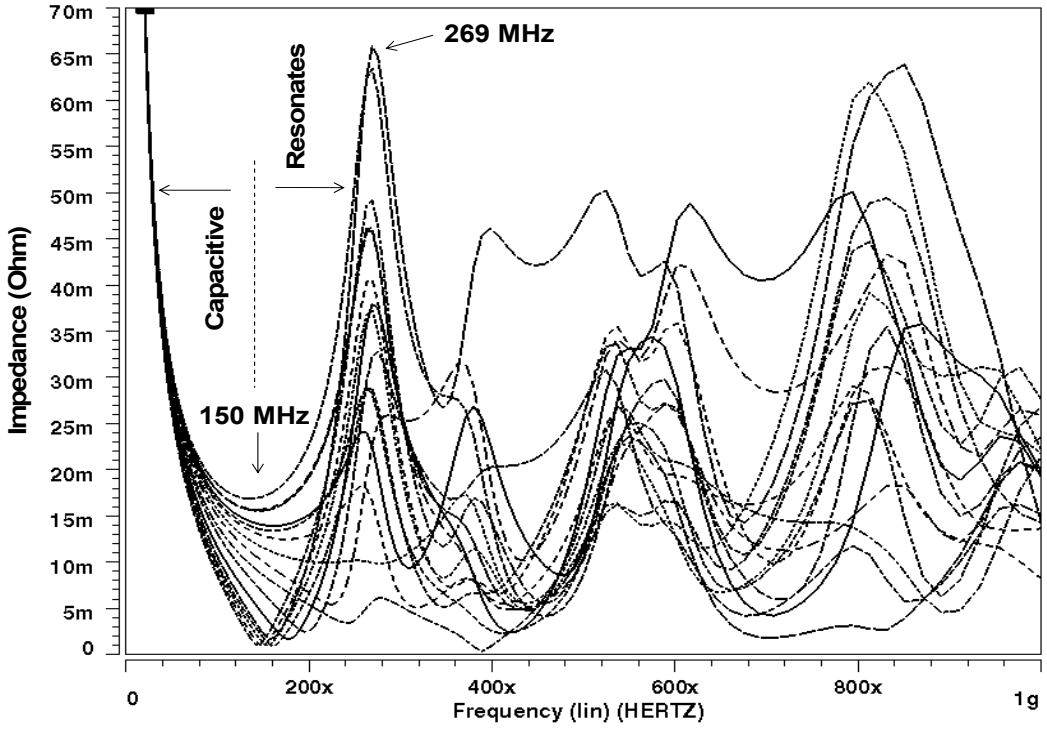


Figure 7.3 Plane Impedances with No Decoupling Capacitors at the 16 Locations

As can be seen in Figure 7.3, the impedance is capacitive at low frequencies, followed by resonances. The time delay across the 11 inch plane with ε_r of 4 is 1.863 ns. A one wavelength wave will stand in the cavity formed by the plane pair at 1/1.863 ns = 537 MHz. The impedance profile in Figure 7.3 shows that nearly all of the locations throughout the plane have impedance peaks at 269 MHz, which corresponds to the half-wavelength frequency. It can also be seen in Figure 7.3 that at frequencies well below the first resonant dip at 150 MHz, all points on the board are at the same impedance. At these low frequencies, components placed anywhere on the plane will see nearly the same

plane impedance. Therefore, if the decoupling capacitors are uniformly placed throughout the plane, then the impedances at all the points are reduced by the same amount [52]. This is equivalent to having all the decoupling capacitors in parallel with the static capacitance of the planes across a single voltage and ground node.

When decoupling capacitors are attached to planes, they exhibit a resonant peak due to the parallel combination of the plane capacitance (C_p) and decoupling capacitor inductance (L). The resonance frequency for this resonant peak is given as $f_0 = \frac{1}{2\pi\sqrt{C_p \cdot L}}$. The capacitor inductance includes the pad inductance on the printed circuit board for mounting the capacitors. It is important to note that the 'LC' resonance is in addition to the self resonant frequency of the decoupling capacitor.

As an example, assume that the decoupling capacitors are placed evenly across the board and ¼ of the plane is considered. Then the plane capacitance is ¼th its maximum value. Since only ¼th the capacitors are present in this area, the inductance of the decoupling capacitors is increased by 4 times. This is because capacitors are mounted in parallel, with the equivalent inductance corresponding to capacitor inductances in parallel. Therefore, the resonant peak for ¼th the plane is at $f_0 = \frac{1}{2\pi\sqrt{(C_p/4)\cdot(4L)}} = \frac{1}{2\pi\sqrt{C_p \cdot L}}$, which remains unchanged. Therefore, if the capacitors are distributed evenly, all sub planes resonate at the same frequency. This is the reason for distributing capacitors uniformly over the whole area of the board at a

frequency less than the first null resonant frequency of the planes. Thus, the capacitors added at each node lowers the impedance over the desired frequency range.

The number of capacitors can be decided based on the target impedance desired. As an example, let there be an impedance peak at frequency f_r, which exceeds the target impedance. Then the decoupling capacitors resonating at frequency f_r should be placed uniformly over the plane's area. Since the minimum impedance for the decoupling capacitor is at its equivalent series resistance (ESR) value which occurs at the self resonant frequency, the number of decoupling capacitors required to meet the target impedance can be calculated as:

$$\text{Number of Capacitors} = \frac{\text{ESR of Each Deoupling Capacitor}}{\text{Target Impedane Required}} \qquad (7.3)$$

Hence, based on the methodology described, the number and type of decoupling capacitors can be selected for suppressing LC resonance.

7.2.1 Results

To demonstrate the above methodology, decoupling capacitors were attached to the plane pair shown in Figure 7.2 to lower the impedance in Figure 7.3. Forty two decoupling capacitors that are effective up to 50 MHz were evenly distributed across the planes shown in Figure 7.2 and the impedance at each frequency was computed. Table

7.2 shows the values for 'C', 'ESL', 'ESR' and Self Resonant Frequency (f_r) for the capacitors used in the simulation.

C	ESL	ESR	f_r	Number
10 mF	1 nH	23.0 mohm	50.3 KHz	2
50 μF	1 nH	5.0 mohm	711.8 KHz	2
22 μF	1 nH	2.0 mohm	1.0 MHz	1
10 μF	1 nH	3.1 mohm	1.6 MHz	1
4.7 μF	1 nH	4.7 mohm	2.3 MHz	1
2.2 μF	1 nH	7.1 mohm	3.4 MHz	1
1.0 μF	1 nH	15.4 mohm	5.0 MHz	2
470 nF	1 nH	23.3 mohm	7.3 MHz	2
220 nF	1 nH	35.3 mohm	10.7 MHz	2
100 nF	1 nH	67.1 mohm	15.9 MHz	4
47 nF	1 nH	99.7 mohm	23.2 MHz	5
22 nF	1 nH	148.5 mohm	33.9 MHz	7
10 nF	1 nH	224.7 mohm	50.3 MHz	12
			Total	42

Table 7.2 Capacitors effective up to 50 MHz

Figure 7.4 shows the simulated plane impedance with 42 capacitors uniformly distributed, at the 16 observation points. The power plane capacitance was 109 nF for an 11 inch square board with spacing of 1mil. The inductance of the decoupling capacitors was 1 nH. The parallel resonance peak can be calculated as $f_0 = \frac{1}{2\pi\sqrt{(109nF)\cdot(1nH/42)}} = 99MHz$. This resonant peak is visible in the impedance profile in Figure 7.4 at 100 MHz. Figure 7.4 also shows that the first half-wavelength resonance of the planes has shifted to the right from 269 MHz to 290 MHz due to the added capacitors.

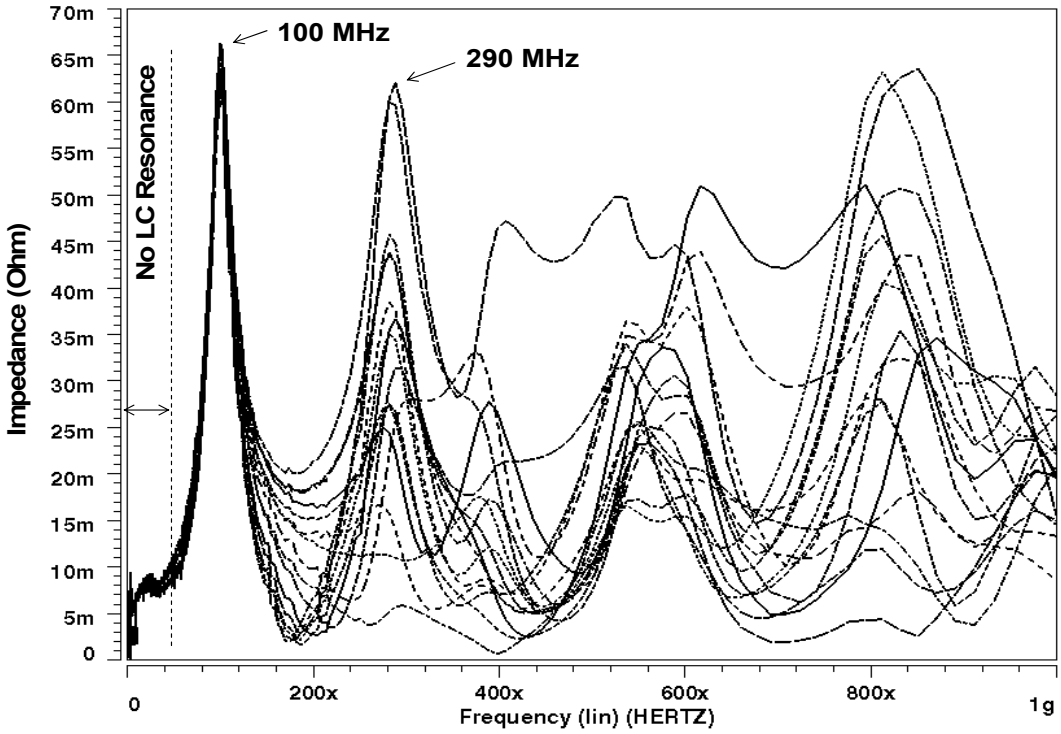


Figure 7.4 Plane Impedances with Decoupling Capacitors Effective up to 50 MHz

Figure 7.5 shows the impedance response with 73 uniformly distributed capacitors with an effective frequency range of 130 MHz. The LC resonance peak, where the capacitors resonates with the planes, has now increased to 160 MHz and has a lower magnitude. The first half-wavelength resonance for the planes has also increased to 300 MHz. Table 7.3 shows the values for 'C', 'ESL', 'ESR' and Self Resonant Frequency (f_r) for the capacitors used to lower the impedance up to 130 MHz. These capacitors are in addition to the 42 capacitors placed earlier.

C	ESL	ESR	f_r	Number
4.7 nF	1 nH	102.1 mohm	73.4 MHz	7
3.3 nF	1 nH	109.9 mohm	87.6 MHz	7
2.5 nF	1 nH	151.1 mohm	100.7 MHz	7
1.5 nF	1 nH	168.0mohm	130.0 MHz	10
			Total	31

Table 7.3 Capacitors effective up to 130 MHz

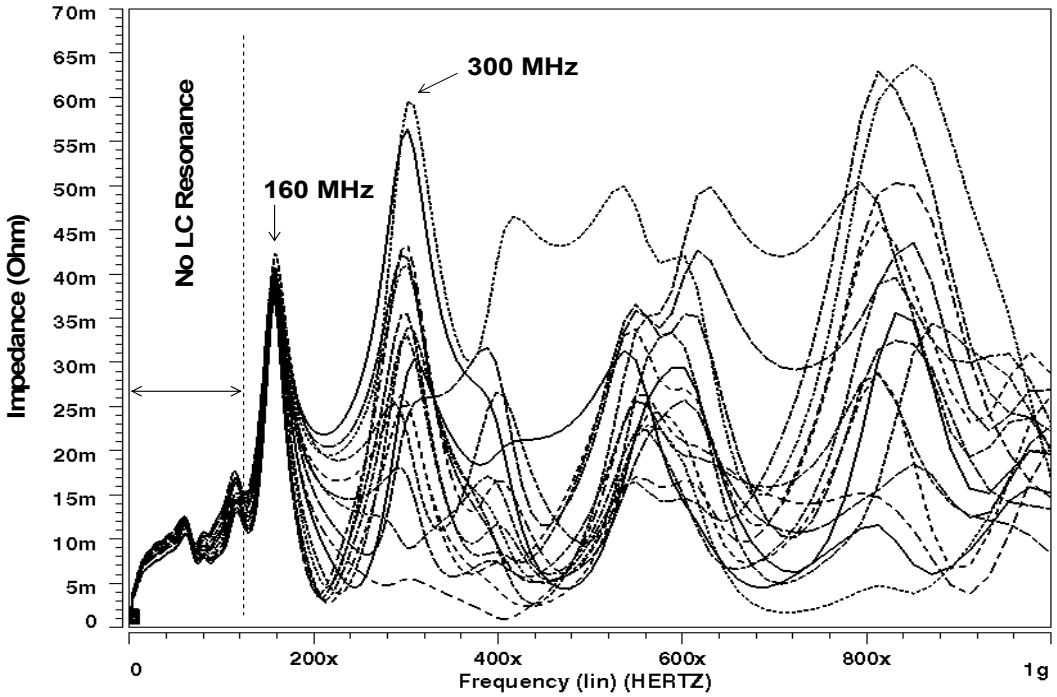


Figure 7.5 Plane Impedances with Decoupling Capacitors Effective up to 130 MHz

Figure 7.6 shows the plane impedance with 104 uniformly distributed capacitors that are effective up to 255 MHz. The LC resonance peaks have disappeared all together. The first plane half-wavelength resonance has increased further to 325 MHz. Table 7.4 shows the capacitors used in addition to the capacitors in Table 7.2 and Table 7.3.

C	ESL	ESR	f_r	*Number*
1.0 nF	1 nH	216.2 mohm	159.2 MHz	9
820 pF	1 nH	223.9 mohm	175.8 MHz	9
560 pF	1 nH	239.6 mohm	212.7 MHz	9
390 pF	1 nH	255.5 mohm	254.9 MHz	4
			Total	31

Table 7.4 Capacitors effective up to 255 MHz

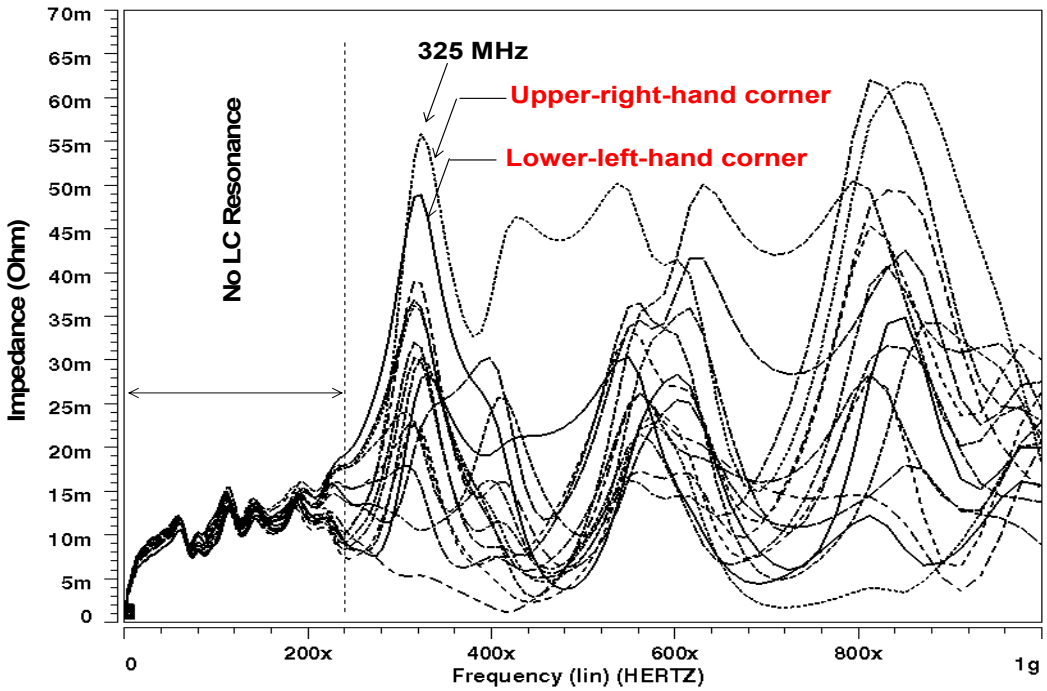


Figure 7.6 Plane Impedances with Decoupling Capacitors Effective up to 255 MHz

Using the methodology discussed in this section, with capacitors of different values, the LC resonance has been suppressed and the plane impedance has been significantly reduced. The focus is now on suppressing the cavity resonances.

7.3 Cavity Resonance

Once the LC resonances are suppressed, the next task is to manage the cavity resonances due to standing waves on the planes. The simulations in this section have been done with the 104 LC resonance-suppressing capacitors uniformly distributed on the planes, as described in the previous section.

Unlike 'LC' resonance, all the cavity resonances cannot be suppressed unless the physical structure or material properties of the planes are changed. This includes changing the plane dimensions, reducing the dielectric thickness, increasing the dielectric constant and increasing the loss-tangent of the FR-4 material. These are described in the next chapter. The purpose of this section is to reduce the cavity resonance peak at discrete frequencies using decoupling capacitors. The discrete frequencies are based on the operating frequency of the microprocessor.

As can be seen in Figure 7.6, there is a large resonance peak at 325 MHz due to a half-wavelength wave standing in the plane cavity. To confirm the importance of capacitor placement for suppressing cavity resonance, 14 capacitors consisting of 7 capacitors with f_r=325 MHz and 7 capacitors with f_r= 650 MHz were placed at the center of the board. Table 7.5 shows the values for 'C', 'ESL', 'ESR' and Self Resonant Frequency (f_r) for the capacitors used in the simulation.

C	ESL	ESR	f_r	*Number*
239.81 pF	1 nH	100 mohm	325 MHz	7
59.95 pF	1 nH	100 mohm	650 MHz	7
			Total	14

Table 7.5 Capacitors used in the Cavity Resonance Simulation

The frequency domain response is shown in Figure 7.7 which is identical to Figure 7.6. Hence, 14 capacitors placed at the center of the board did not change the impedance response. Thus, the location of the decoupling capacitors on the board for suppressing cavity resonance is very important and needs to be selected with care. This is the subject of this section.

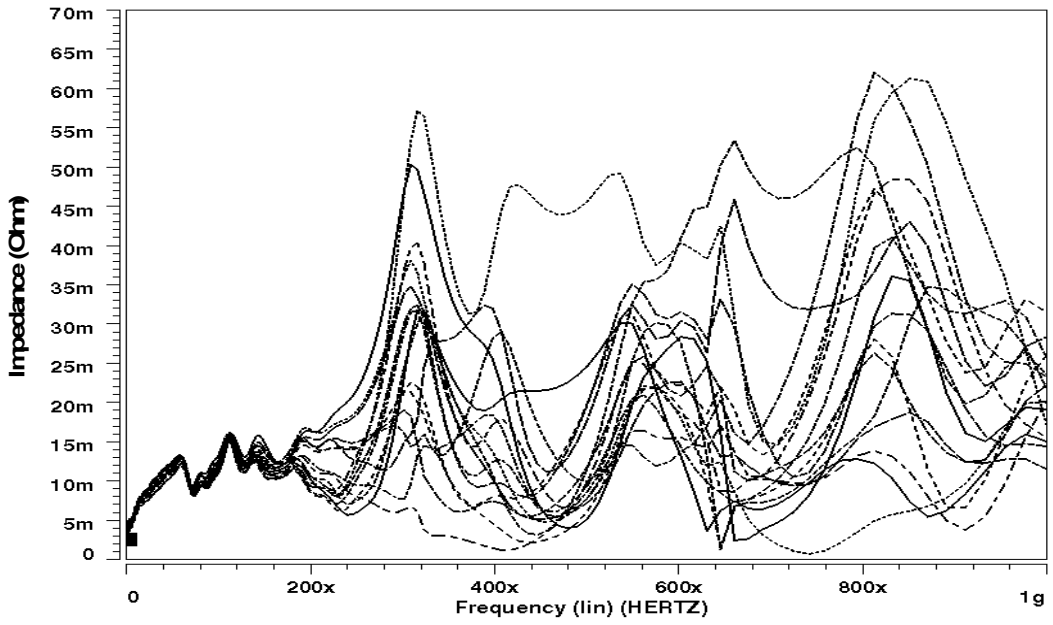


Figure 7.7 Plane Impedances with 14 Capacitors (f_r=325 MHz and f_r=650 MHz) placed at the Center of the Board

As an example, suppose that the microprocessor on the board has to run at 325 MHz, which exactly coincides with the frequency corresponding to the plane resonance. Figure 7.8 shows the simulation result in the time domain with the impedance response in Figure 7.6. Pulses with a period of 3.077 ns were used to represent the microprocessor drawing 10 ampere transient current at 325 MHz. The rise and fall time of the pulse used was 300 ps. In Figure 7.8, a maximum noise voltage of ±300 mV can be observed.

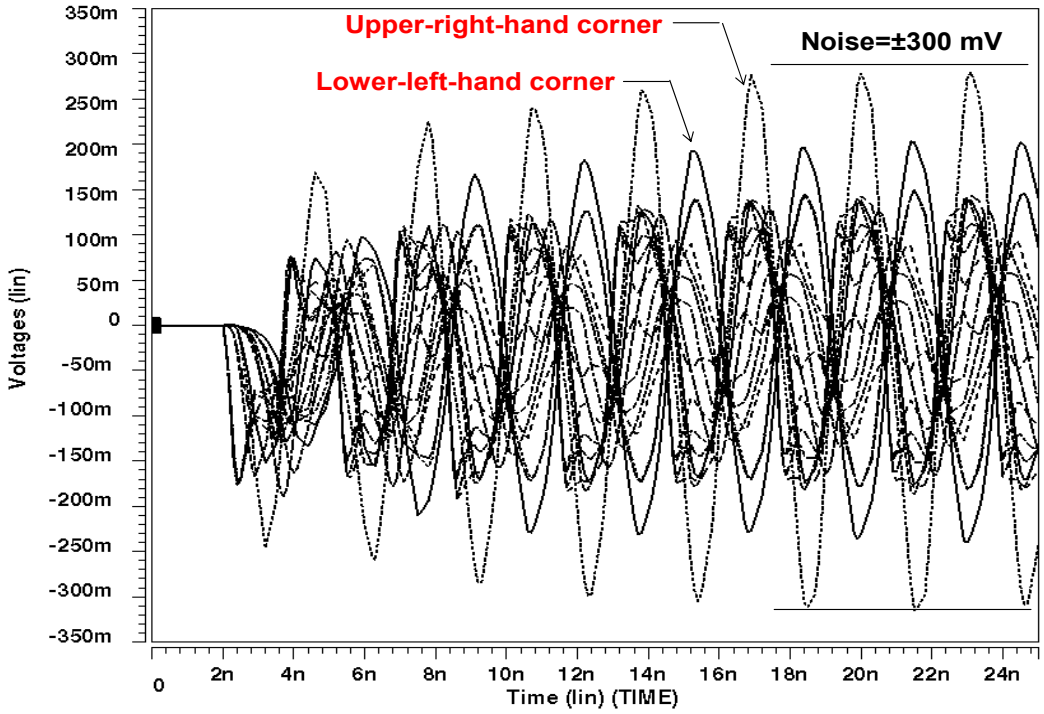


Figure 7.8 Noise Voltages on the Planes When Stimulated at 325 MHz

Since capacitors are a reservoir of charge, the ideal position for the decoupling capacitors is next to the microprocessors. The capacitors can then deliver charge at the clock and clock harmonic frequencies. The fourteen capacitors in Table 7.5 composed of

7 capacitors with f_r=325 MHz and 7 capacitors with f_r=650 MHz with resonant frequencies corresponding to the clock and twice the clock frequency, respectively, were added at the source locations. Figure 7.9 shows the plane impedance in the frequency domain.

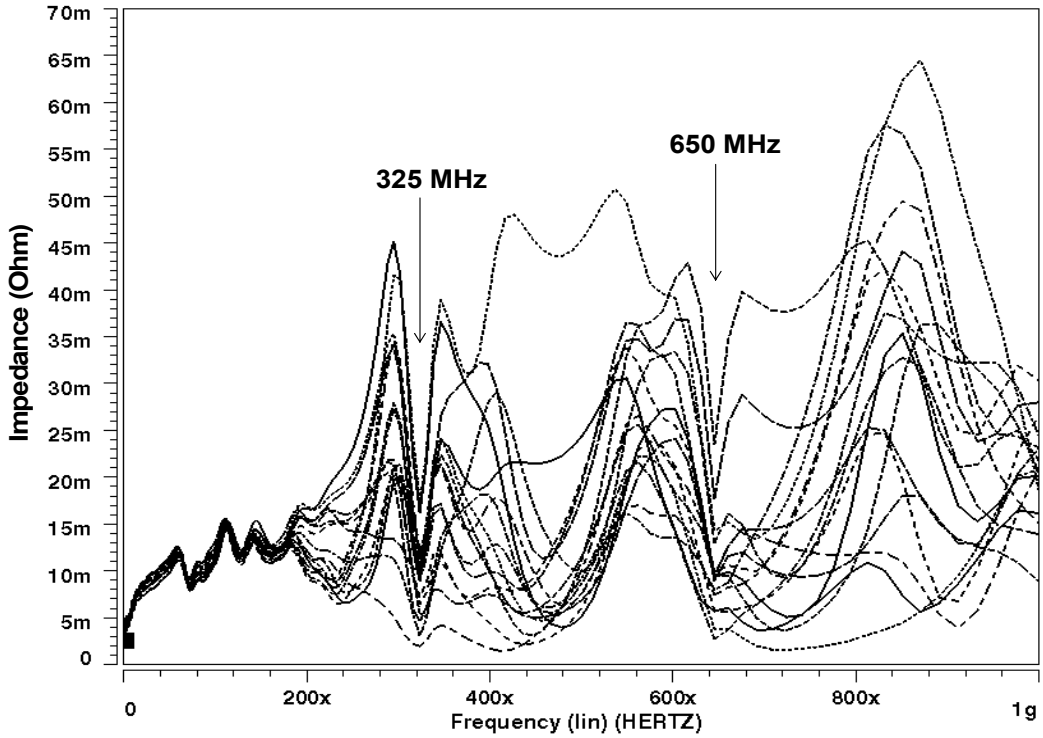


Figure 7.9 Plane Impedances with 14 Capacitors (f_r=325 MHz and f_r=650 MHz) placed at Current Sources

As can be seen in Figure 7.9, the cavity resonance peak at 325 MHz has been suppressed substantially to less than 20 mΩ. Figure 7.10 shows the corresponding time domain simulation with a 10 ampere pulse source with period 3.077 ns and rise/fall time of 300 ps. In Figure 7.10, the noise voltage has been reduced to ±200 mV.

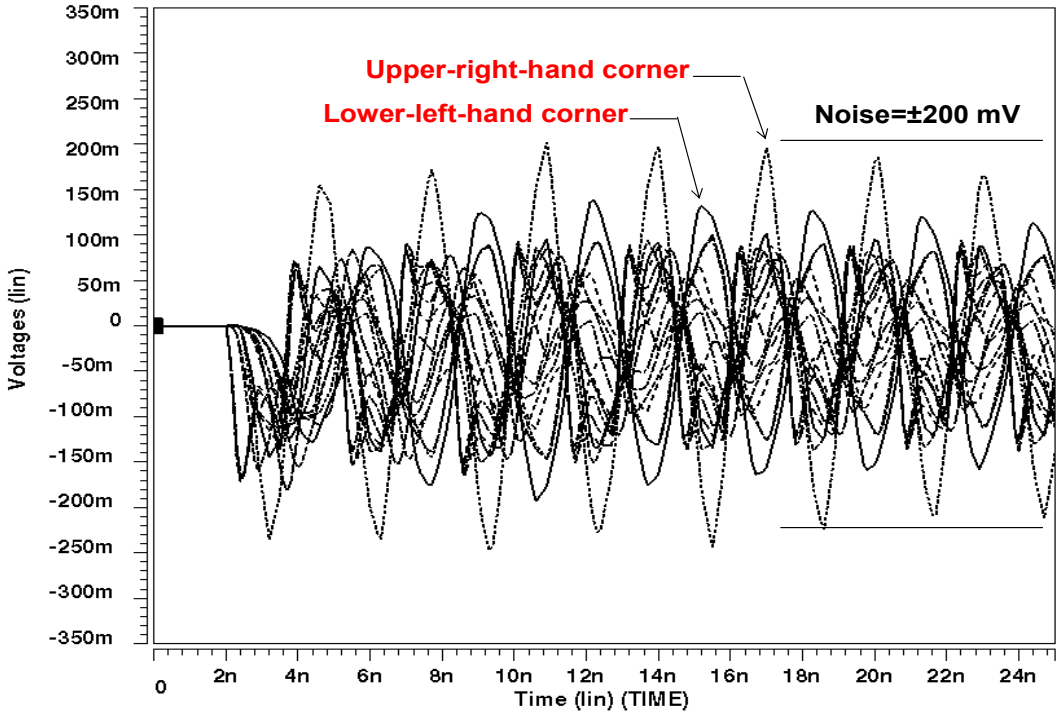


Figure 7.10 Noise Voltages with 14 Capacitors (f_r=325 MHz and f_r=650 MHz) placed at Current Sources

To better understand the response in Figure 7.10, consider the impedance response without the 14 high frequency capacitors, as shown in Figure 7.6. From Figure 7.6, the locations with the highest impedances at 325 MHz are located at opposite corners of the board; namely, the upper-right-hand and lower-left-hand corners, respectively. Identifying the appropriate locations with high impedances is required for managing the cavity resonance. Decoupling capacitors with 'f_r' at these frequencies, therefore, need to be placed at locations with high impedances [52].

Based on this methodology, the 14 capacitors in Table 7.5 were distributed non-uniformly on the planes. These included four capacitors with f_r=325 MHz at the source

locations, two capacitors with f_r=325 MHz at the upper-right-corner location, one capacitor with f_r=325 MHz at lower-left-corner location, and seven capacitors with f_r=650 MHz at the source locations. Figure 7.11 shows the result in the time domain, with the same current source as before. In Figure 7.11, the noises at opposite corners have been suppressed and smaller noise voltages can be observed over the entire area of the planes as compared with the result in Figure 7.10, where all 14 capacitors were located at the source locations. In Figure 7.11, the noise voltage has been further reduced to ±150 mV.

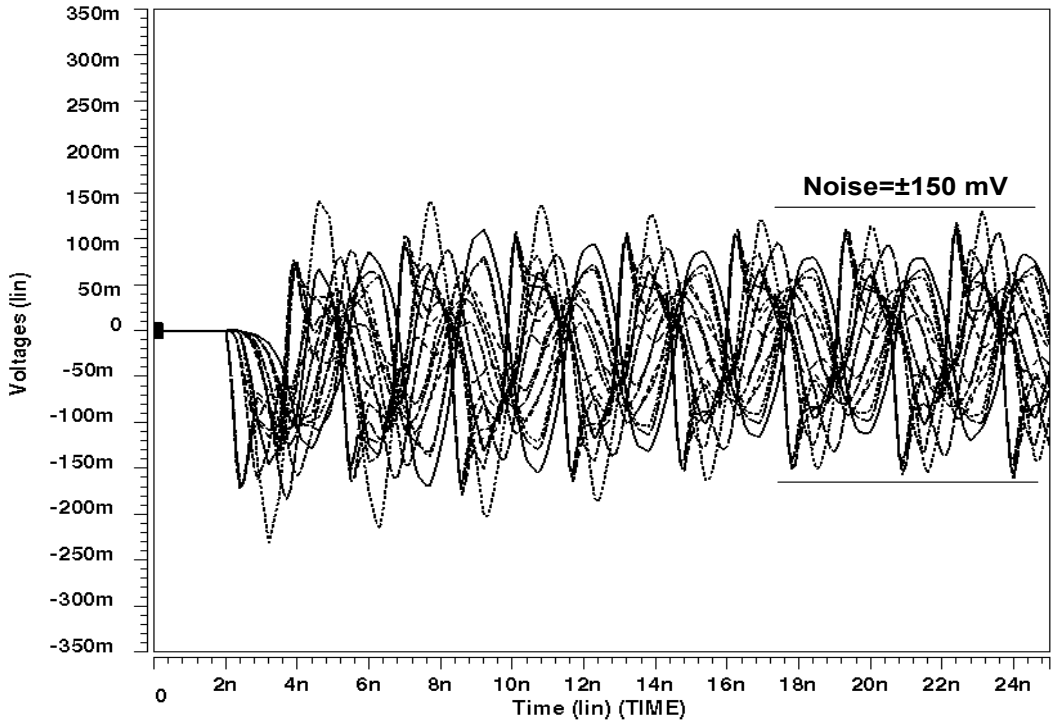


Figure 7.11 Noise Voltages with 14 Capacitors (f_r=325 MHz and f_r=650 MHz) placed at Current Sources and Upper-right-hand and Lower-left-hand Corners

Figure 7.12 shows the corresponding impedance response in the frequency domain. As can be seen in Figure 7.12, the cavity resonance peak at 325 MHz has been suppressed to less than 15 mΩ.

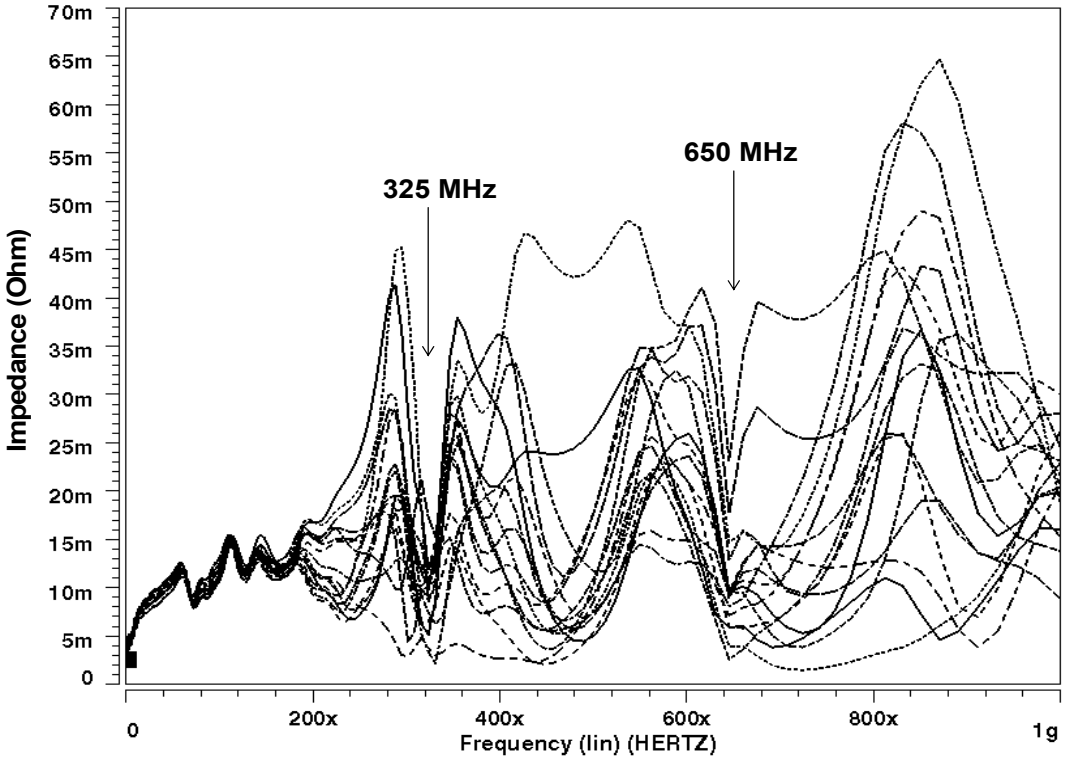


Figure 7.12 Plane Impedances with 14 Capacitors (f_r=325 MHz and f_r=650 MHz) placed at Current Sources and Upper-right-hand and Lower-left-hand Corners

After a group of decoupling capacitors are attached to the planes, another analysis can be performed and more capacitors can be placed at the high-impedance locations and re-analyzed in an iterative fashion until the resultant impedance response is less than or equal to the target impedance Z_{target}. This methodology has been described using an algorithm in the next section.

7.4 Algorithm for Decoupling Capacitor Selection and Placement

This section captures the methodology described in the previous sections in the form of an algorithm for implementing it as a computer code. This algorithm is based on the following assumptions which can be changed based on the computer resources [52].

1. The output from SPICE simulation is a linear array of 8x8 nodes with 100 frequency points at each node. This translates to 6400 values of impedance (Z) data.
2. At every frequency, the impedances at the 64 nodes are computed. Thus, the 6400 values of impedance data translate to 100 sets of data (one for each simulated frequency).
3. Each set consists of 64 data points that map to a specific location on the plane pair at each frequency.

Based on the above assumptions, a flow chart is shown in Figure 7.13 for suppressing 'LC' and cavity resonances.

7.5 Summary

In this chapter, a methodology for the placement and optimization of decoupling capacitors has been described. Two different types of resonances in the PDS were considered, namely, 'LC' resonance and cavity resonance.

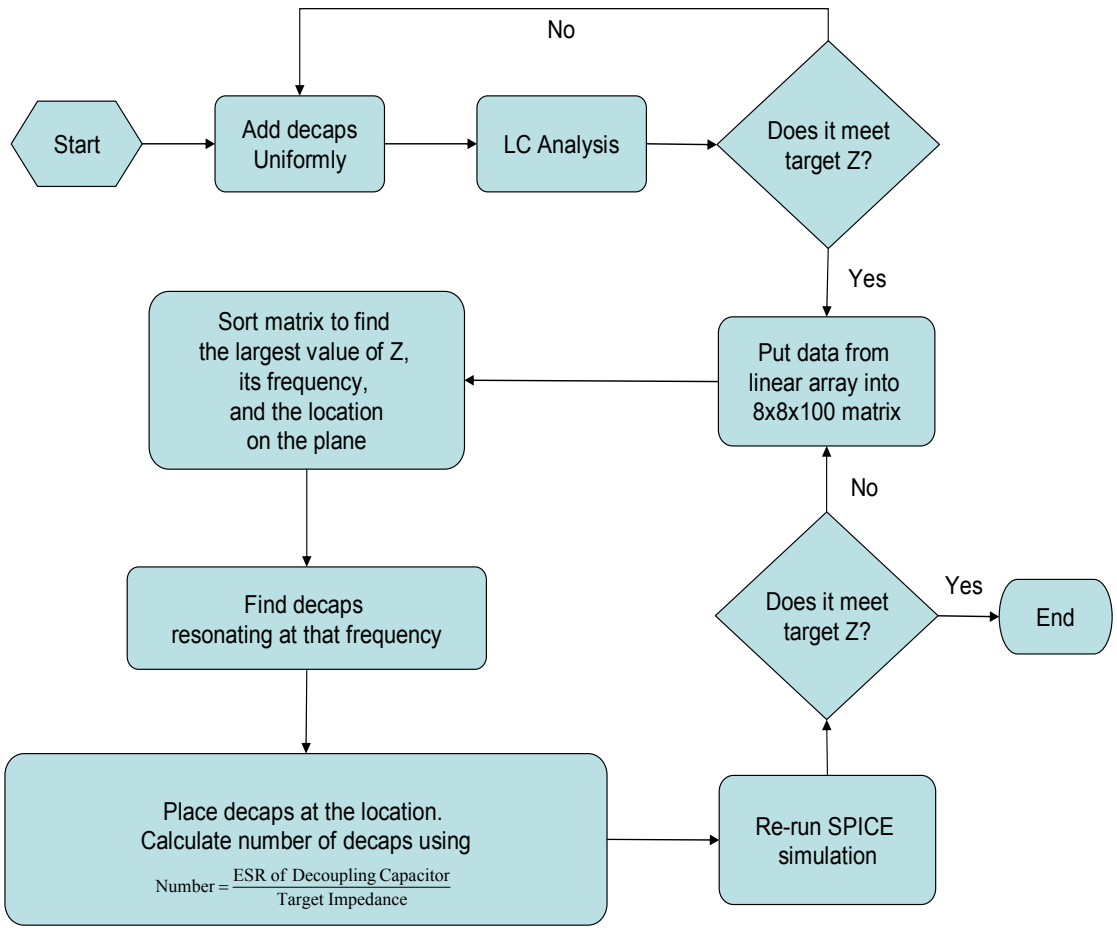


Figure 7.13 Flow Chart for the Placement of Decoupling Capacitors for Cavity Resonance

The 'LC' resonance caused by the capacitor inductance and power plane capacitance occurs in the low frequency range well below the first null resonant frequency of the planes. The capacitors were placed on the power plane uniformly to ensure that each small section of the plane had the same capacitance to minimize the resonant peak due to LC resonance. The resonance caused by standing waves in the cavity occurs at higher frequencies, above the first null resonant frequency of the planes. Simulations

demonstrated that the cavity resonance can be suppressed when the decoupling capacitors were placed at the locations that had high impedances. By using the algorithm proposed, which identify the frequencies and locations with high impedances on the plane, and by placing the decoupling capacitors resonating at these frequencies at the high-impedance locations, the cavity resonance can be minimized. Using this methodology, the target impedance for the microprocessor can be met over a large frequency range.

CHAPTER 8

Suppression of Simultaneous Switching Noise using New Technologies

---

In the previous chapters, SSN has been studied from a modeling and analysis aspect. The reduction of SSN is an important issue that has been discussed in this chapter. Discrete decoupling capacitors have been used in the PDS to minimize the tolerance on the power supply for CMOS circuits. This improves signal integrity and reduces radiated noise. For the modern PDS with continuous power and ground planes, the embedded capacitance between planes can be used to reduce SSN. In addition, increasing the loss in the dielectric can also be used as a mechanism for reducing SSN.

In this chapter, suppression of SSN using discrete/embedded decoupling capacitors is simulated and studied. The roles of discrete capacitor and embedded capacitor are discussed and the noise reduction is demonstrated through simulations on a test vehicle and functioning board. The importance of the dielectric loss tangent is also studied and simulations are conducted for different values of loss tangent to understand its effect on plane resonances.

8.1 Discrete Decoupling Capacitors

Discrete decoupling capacitors, placed between the power and ground planes, act as local sources of charge so that during the switching event, the current surge is drawn from these capacitors rather than the voltage regulator module (VRM). This mitigates momentary drops in the voltage supplied to the switching device due to the current surge passing through the inductance of the PDS, thus preventing the false switching of the logic circuits [53].

Figure 8.1 shows the current return loop and associated effective inductance for circuits driving interconnections in the package [47].

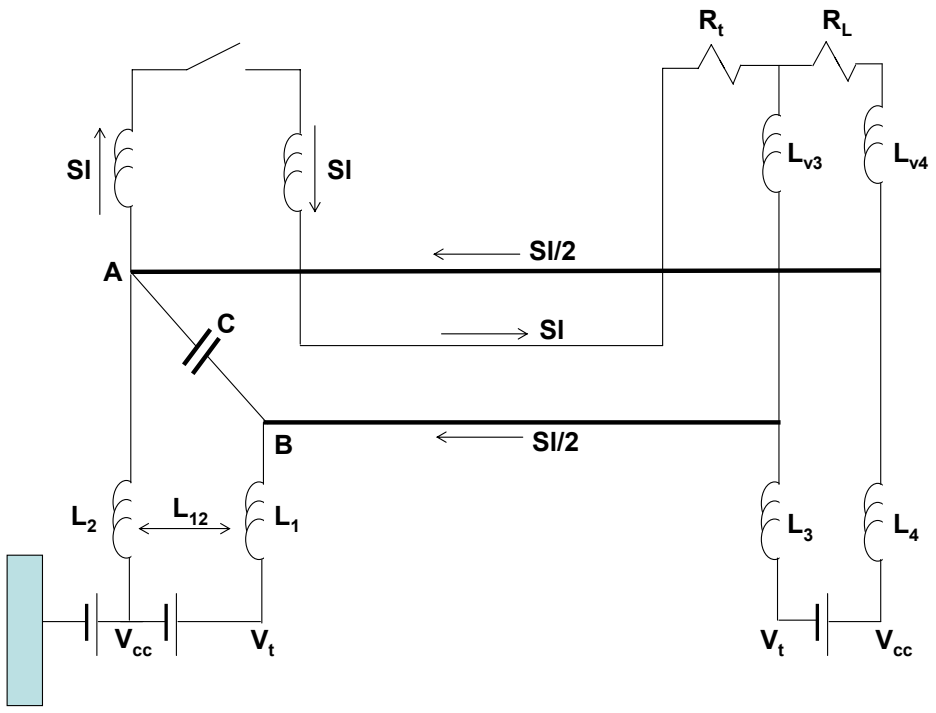
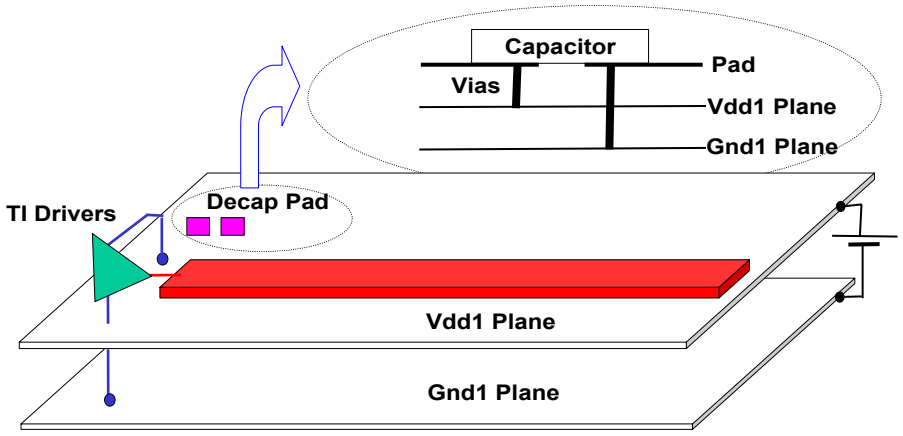


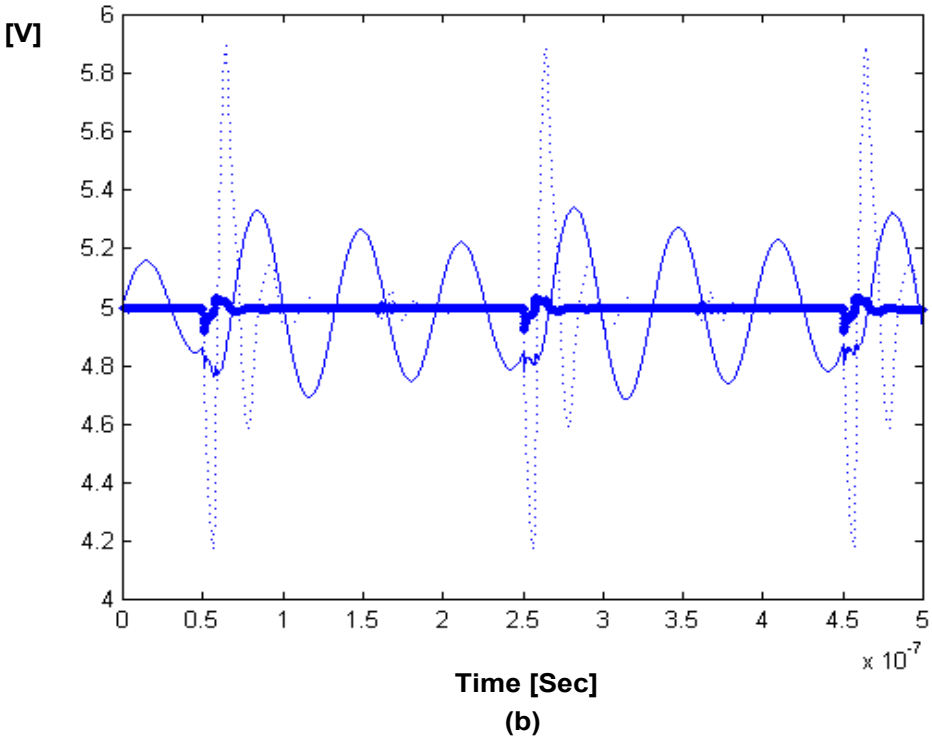
Figure 8.1 Conceptual Current Path for Switching Drivers [47]

In the figure, the driver is modeled as a switch that draws current from the V_{cc} supply and delivers it to another supply, V_t, through a signal line and a termination resistance R_t. One end of the resistor R_t is connected to the signal line and the other to the power supply V_t through the vias represented by L_{v3} and L_3. R_L is an equivalent impedance formed by the receiving chip. The signal line is in the middle of a V_{cc} and V_t power plane so that each carries a return current equal to 50 % of the current on the signal line. The return current loop is composed of the inductances L_1 and L_2. If a large enough capacitor C is connected between points A and B, then the current necessary for the switching driver can be supplied instantaneously by this capacitor instead of traversing the $L_1 - L_2$ path.

To see the effects of the discrete decoupling capacitors on SSN, the test vehicle in Section 3.2 with decoupling capacitors has been re-simulated in this chapter. In the simulation, capacitors were placed near the drivers as shown in Figure 8.2 (a). Figure 8.2 (a) also shows the cross-section of the decoupling capacitor mounted on the planes, where the vias connect the capacitor to the planes. Two types of decoupling capacitors were used in the simulation. The first capacitor had a capacitance of 1 μF with an ESR of 9.8 mohms and ESL of 0.485 nH, which corresponds to X5R_0603 capacitor. The second capacitor had a capacitance of 0.01 μF with an ESR of 9.8 mohms and ESL of 0.485 nH. The ESR and ESL of two capacitors were chosen the same for comparison of the effectiveness of the decoupling capacitor in terms of charge storage (C). Figure 8.2 (b) shows the simulation results for the first plane pair power supply fluctuation (PP1). These results have been compared with the case where no decoupling capacitors were used.



(a)



(b)

Figure 8.2 (a) Snapshot of the Test Vehicle with Discrete Decoupling Capacitor (b) First Layer Power Supply Fluctuations (PP1): No Decoupling Capacitor (Dotted Line), 0.01 μF Capacitor in Series with 9.8 mohms and 0.485 nH (Thin Solid Line), 1 μF Capacitor in Series with 9.8 mohms and 0.485 nH (Thick Solid Line)

As is obvious from Figure 8.2, decoupling capacitors reduce the simultaneous switching noise on the power planes. The charge necessary for the switching driver can be supplied by the decoupling capacitor, which reduces the voltage drop across the chip terminals by

$$dV = \frac{dI \cdot dt}{C} \qquad (7.1)$$

where dV is the voltage drop in the supply voltage caused by a current transient of dI occurring in time dt. C is the capacitance of the decoupling capacitor. In Figure 8.2, the 1 μF capacitor results in a larger noise suppression as compared to the 0.01 μF due to the larger charge storage, as expected. To enable the decoupling of the PDS, issues such as the determination of their values, quantities, and locations are required. These have been studied in Chapter 7 in detail.

8.2 Embedded Decoupling Capacitors

In the PDS where the planes are used for supplying power and ground, the SSN can be reduced if enough attenuation is provided to suppress plane resonances.

The attenuation in dB can be expressed as [54]

$$A^{dB} = 4.35\left(\frac{R_s}{Z_0} + G_d Z_0\right) \qquad (7.2)$$

where Z_0 is the characteristic impedance and R_s and G_d are the series resistance of the conductor and parallel conductance of the dielectric, respectively.

The above expression states that the same series resistance produces higher attenuation if the characteristic impedance is lower. The characteristic impedance of the plane pair is given as $Z_0 = \sqrt{L/C}$. Thus, with tightly spaced power planes, capacitance increases and inductance decreases. This results in a low characteristic impedance, which helps in suppressing the magnitude of plane resonances. Using high dielectric constant material also increases the capacitance, resulting in low plane impedance.

At the Packaging Research Center (PRC), the test vehicle in Section 3.2 has been re-designed using System-On-a-Package (SOP) technology with a cross-section as shown in Figure 8.3 [55]. The length of the transmission line is 10 inches. Varying spacings between planes and different dielectric materials have been used in the test vehicle, as shown in Table 8.1. The thin dielectric material acts as an embedded decoupling capacitor for suppressing noise.

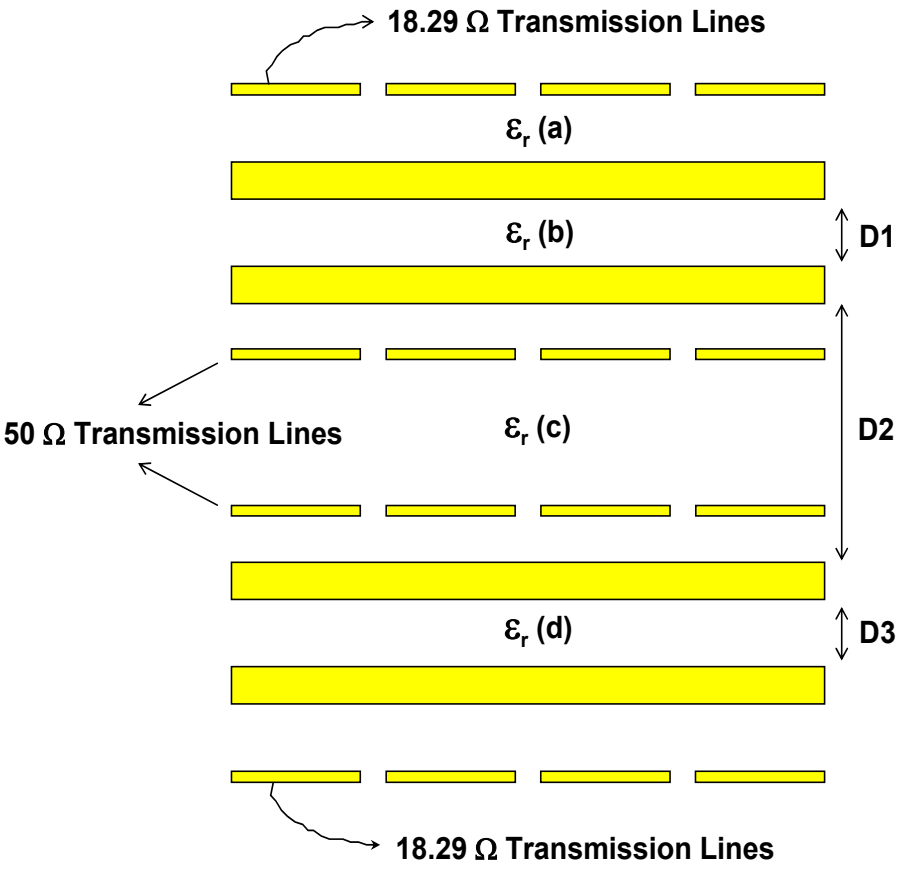


Figure 8.3 Cross-Section of the Test Board to be Implemented at PRC

	ε_r (a)	ε_r (b)	ε_r (c)	ε_r (d)	D1 [μm]	D2 [μm]	D3 [μm]
Standard	4.7	4.7	4.7	4.7	101.6	863.6	101.6
Low ε_r	3.9	3.9	3.9	3.9	10	825	10
Low ε_r + High ε_r	3.9	30	3.9	30	10	825	10

Table 8.1 Three Cases with Different Dielectric Constants and Spacings between Planes

The three cases shown in Table 8.1 have been simulated using the modeling method described in the previous chapters. The simulation results are shown in Figure 8.4. The results show that the use of thin dielectric material with high dielectric constant reduces the SSN significantly.

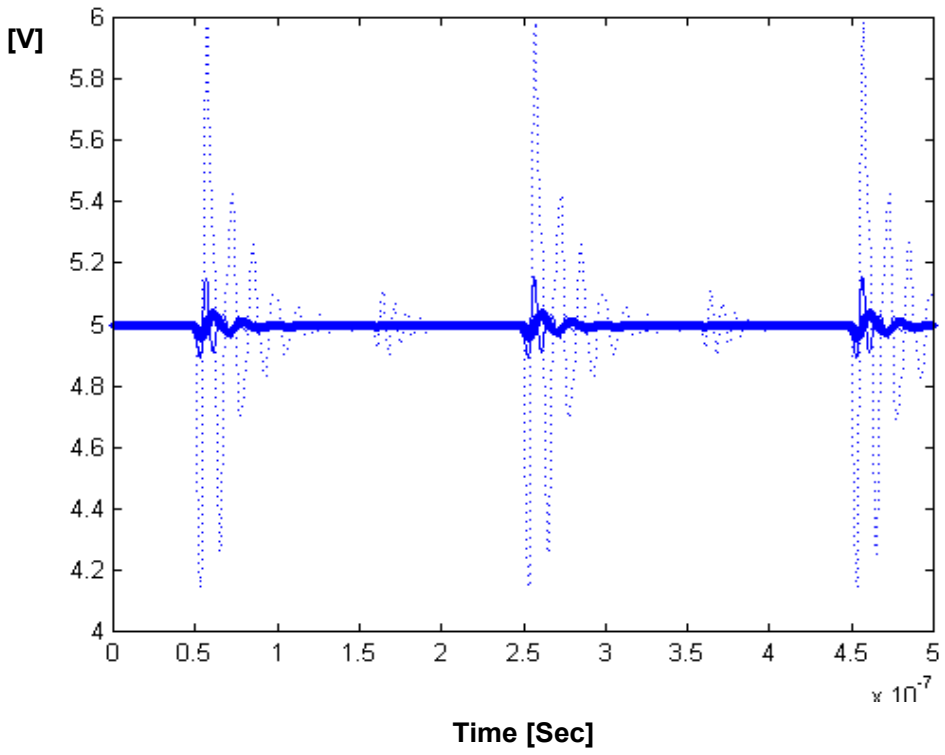


Figure 8.4 First Layer Power Supply Fluctuations for Three Cases in Table 3: Standard (Dotted Line), Low ε_r (Thin Solid Line), Low ε_r + High ε_r (Thick Solid Line)

Table 8.2 summarizes the results based on the SSN simulations with discrete/embedded capacitors.

Capacitors	Capacitance	Peak-to-Peak Noise
Discrete	0.01 μF	650 mV
Discrete	1 μF	115 mV
Embedded	6.68 nF	262 mV
Embedded	0.05 μF	83 mV

Table 8.2 Summary of Noise Simulations with Discrete/Embedded Capacitors

The performance of the discrete decoupling capacitor is limited by its parasitics, i.e. ESR and ESL. ESR is strong function of dielectric type and determines the null in the impedance curve, where the capacitance (C) of the capacitor resonates with the inductance (ESL) at $f_0 = \frac{1}{2\pi\sqrt{C \cdot ESL}}$. Thus, for the same amount of C, a larger ESL will lower f_0, above which the capacitor becomes inductive, causing the capacitor to perform poorly for decoupling.

Dielectric Thickness Variation

The functioning board discussed in Chapter 6 was also simulated with different dielectric thickness for reducing the switching noise. Figure 8.5 (a), (b), (c) shows simulation results with dielectric thickness of 2, 1 and 0.5 mils, demonstrating the effectiveness of thin dielectrics for reducing switching noise. The peak to peak noise (V_{pp}) was reduced from 39.9 mV to 15.8 mV by replacing 2 mil thick dielectric with 0.5 mil thick dielectric, as shown in Figure 8.5.

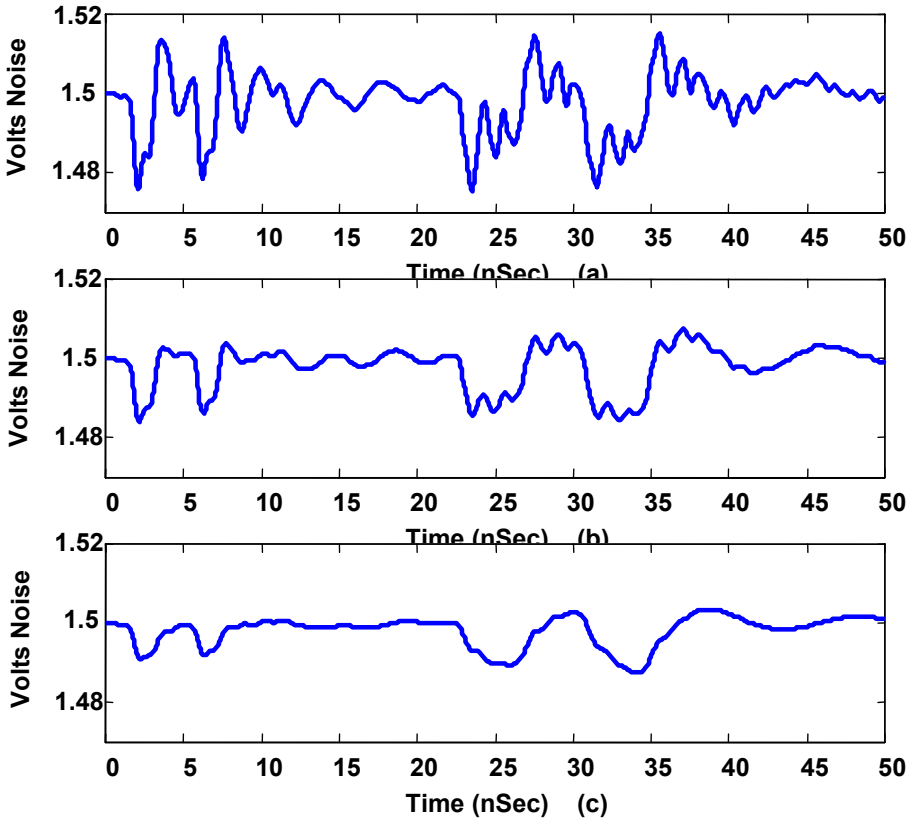


Figure 8.5 Simulated Switching Noise for Different Dielectric Thickness: (a) 2 mils: V_{pp}=39.9 mV (b) 1 mil: V_{pp}=23.4 mV (c) 0.5 mil: V_{pp}=15.8 mV

Loss Tangent

Another method for suppressing the amplitude of plane resonances is to increase the loss of the dielectric material used between the power/ground planes. The typical PCB materials have been optimized for low loss signal transmission, and because of this, they do not provide sufficient suppression of plane resonances. If used only between the power/ground planes, high dielectric loss materials can be used to suppress plane resonances [54].

To demonstrate the effect of dielectric loss on the plane resonances, the Vdd1/Gnd1 plane pair of the test vehicle in Section 3.2 was simulated with three dielectric loss tangent values: tanδ = 0, 0.03, 0.3, respectively. The magnitude of the self-impedance at the left side of the plane pair has been computed using equation (2.3), as shown in Figure 8.6.

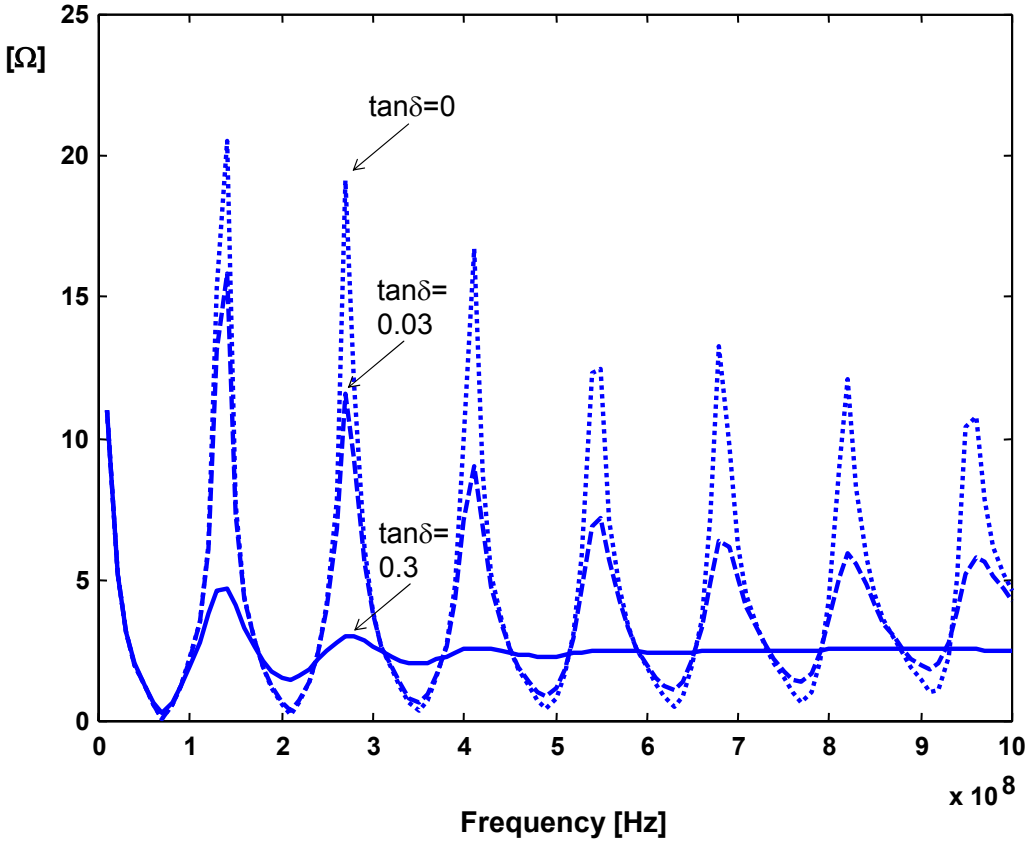


Figure 8.6 Self-Impedance: tanδ = 0 (Dotted Line), tanδ = 0.03 (Dashed Line), tanδ = 0.3 (Solid Line)

As shown in the figure, a dielectric material with loss tangent of 0.3 suppresses most of the plane resonances.

8.3 Summary

In this chapter, the suppression of SSN using discrete/embedded decoupling capacitors was discussed. Two types of discrete decoupling capacitors were used for the simulation of the test vehicle. Discrete decoupling capacitors supply the current necessary for the switching drivers and the simulations showed that the capacitors with larger capacitance resulted in a lower noise. This is expected due to the increased charge storage capacity of a larger capacitor. Test structures, utilizing the embedded capacitance of the solid plane pairs, have been designed at PRC and simulated for SSN evaluations. It was shown in the simulation that structures with thin dielectrics and high dielectric constants reduced SSN significantly by lowering the impedance of the planes. The functioning board discussed in Chapter 6 was re-simulated with thinner dielectric thickness, demonstrating its effect in reducing SSN. Simulations also showed that the loss tangent of the dielectric suppressed the resonant peaks of the power planes, when the loss was increased.

CHAPTER 9

Conclusions and Future Work

This dissertation described a methodology for modeling the simultaneous switching noise (SSN) in multi-layered packages and boards. The circuit models were first derived for the multi-port power/ground planes. These models were then expanded for multi-layered structures arising in packages and boards. Transmission lines were then incorporated into the models based on superposition theory to account for the return current effects.

A test vehicle was designed, fabricated and measured to quantify the plane-to-plane noise waveforms. It was shown that the SSN is caused by plane bounce, which is caused by the return currents of the signal transmission lines. Plane bounce represents the variation of the potential difference between the voltage and ground nodes across the surface of the planes. This voltage variation is equivalent to the planes bouncing with time as compared to the DC level. The modeling method was correlated with measurements, showing the validity of the modeling methodology.

The modeling methodology was then extended to account for via transitions and splits on planes by accounting for the return currents on the planes. It was demonstrated that using the methodology discussed in this dissertation, a system can be modeled to

simulate plane bounce and its effect on driver and receiver switching and the SSN at all levels of assembly, i.e. chip/package/PCB structure, can be computed.

To further validate the modeling methodology, core and I/O switching noise in a functioning computer system was measured. In the core power distribution system (PDS), the noise at twice the clock frequency was found to be the dominant noise. In the I/O PDS, the switching noise was caused by the return currents flowing on the I/O power planes. The modeling methodology was applied to the functioning system and showed good model to hardware correlation, demonstrating the application of the methodology for modeling complex and realistic systems.

Optimal locations for discrete decoupling capacitors were studied. For suppressing the LC resonance, it was found that the capacitors need to be placed on the power plane in a distributed manner over the plane's area. For suppressing the cavity resonance, the frequencies and locations that have high impedances were first identified using the algorithm proposed and the decoupling capacitors resonating at these frequencies were then placed at the high-impedance locations.

Both discrete and embedded decoupling capacitors were used in the simulations to understand their effects on reducing SSN. Based on simulations, it was demonstrated that switching noise can be reduced by using thin and lossy dielectric material, which provides sufficient attenuation for suppressing the plane resonances.

As a continuation of the work described in this dissertation, the following areas of study may be considered:

- Statistical analysis using the modeling methodology to map the physical manufacturing parameters to the electrical performance parameters, such as SSN.
- Modeling of on-chip PDS, which uses meshed power planes.
- Modeling of noise coupling between on-chip and off-chip PDS.

REFERENCES

[1] Rao R. Tummala, Eugene J. Rymaszewski, Alan G. Klopfenstein, Microelectronics Packaging Handbook, Technology Drivers, Part I, Chapter 3, Second Edition, Chapman & Hall, 1997.

[2] Larry Smith, "Simultaneous Switch Noise and Power Plane Bounce for CMOS Technology, "IEEE 8th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 163-166, San Diego, CA, October 1999.

[3] Nanju Na, Jinseong Choi, Sungjun Chun, Madhavan Swaminathan and Jegannathan Srinivasan, "Modeling and Transient Simulation of Planes in Electronic Packages," IEEE Transactions on Components, Packaging, and Manufacturing Technology - Advanced Packaging, Vol. 23, No. 3, pp. 340-352, August 2000.

[4] Henry W. Ott, Noise Reduction Techniques in Electronic Systems, Chapter 10, Second Edition, Wiley, 1988.

[5] G. A. Katopis, “Delta-I Noise Specification for a High-Performance Computing Machine,” Proc. IEEE, Vol. 73. No. 9, pp. 1405-1415, 1985.

[6] William D. Brown, Advanced Electronic Packaging, Chapter 3, IEEE Press, 1998.

[7] Barry J. Rubin, “Comparison of Mesh and Solid Planes for Use in Electrical Packaging,” IEEE 5th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 217-219, 1996.

[8] M. A. Schmidt, K. Lam, L. E. Mosley, G. Choksi, and B. K. Bhattacharyya, “Current distribution in power and ground planes of a multilayer pin grid package,” in Proc. Int. Elcectron. Packag. Soc., 1988, pp. 467-475.

[9] Abdul-Rahman Yaghmour and John L. Prince, “Effect of Mutual Coupling Between Signal Traces and Ground Planes on SSO Noise in Packages with Multiple Stacked Ground Planes,” Proceedings of 47th Electronic Components and Technology Conference, pp. 836-841, 1997.

[10] Keunmyung Lee, Alan Barber, “Modeling and analysis of Multichip Module Power Supply Planes,” IEEE Transactions on Components, Packaging, and Manufacturing Technology – Part B. Vol. 18, No. 4, pp. 628-639, November 1995.

[11] R. Mittra, S. Chebolu, and W. D. Becker, “Efficient Modeling of Power Planes in Computer Packages using the Finite Difference Time Domain Method,” IEEE Transactions on Microwave Theory and Technology, Vol. 42, No. 9, pp. 1791-1795, September 1994.

[12] A. Waizman, Chee-Yee Chung, “Package capacitors impact on microprocessor maximum operating frequency,” Proceeding of 51th Electronic Components and Technology Conference, pp. 118-122, May 2001.

[13] P. Zarkesh-Ha, T. Mule, J. D. Meindl, “Characterization and modeling of clock skew with process variations,” Proceedings of the IEEE Custom Integrated Circuits, pp. 441-444, 1999.

[14] Ramesh Senthinathan, Andreas C. Cangellaris and John L. Prince, "Reference Plane Parasitics Modeling and Their Contribution to the Power and Ground Path "Effective" Inductance as Seen by the Output Drivers," IEEE Transactions on Microwave Theory and Techniques, Vol. 42, No. 9, pp. 1765-1773, September 1994.

[15] W. Becker, B. McCredie, G. Wilkins and A. Iqbal, "Power Distribution Modeling of High Performance First Level Computer Packages," IEEE 2nd Topical Meeting on Electrical Performance of Electronic Packaging, pp. 202-205, October 1993.

[16] James P. Libous and Daniel P. O'Connor, "Measurements, Modeling, and Simulation of Flip-Chip CMOS ASIC Simultaneous Switching Noise on a Multilayer Ceramic BGA," IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 20, No 3, pp. 266-271, August 1997.

[17] Nanju Na, Madhavan Swaminathan, “Modeling and Simulation of Planes in Electronic Packages for GHz Systems,” IEEE 8th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 149-152, San Diego, October, 1999.

[18] Nanju Na, “Modeling and Simulation of Planes in Electronic Packages,” Ph.D. Thesis Presented to the Academic Faculty, School of Electrical and Computer Engineering, Georgia Institute of Technology, January 2001.

[19] Sheng-Mou Lin and Ruey-Beei Wu, “Composite Effects of Reflections and Ground Bounce for Signal Line through a Split Power Plane,” IEEE 10th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 89-92, Cambridge, October, 2001.

[20] T.Okoshi, Planar Circuits for Microwaves and Lightwaves, Chapter 2, Springer-Verlag, 1985.

[21] Sungjun Chun, Madhavan Swaminathan, Larry D. Smith, Jegannathan Srinivasan, Zhang Jin and Mahadevan K. Iyer, “Modeling of Simultaneous Switching Noise in High Speed Systems,” IEEE Transactions on Advanced Packaging, Vol. 24, No. 2, pp. 132-142, May 2001.

[22] Jinseong Choi and Madhavan Swaminathan, "Computation of the Frequency Response of Multiple Planes in Gigahertz Packages and Boards," IEEE 8th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 157-160, San Diego, October, 1999.

[23] Jifeng Mao, Jegannathan Srinivasan, Jinseong Choi, Nhon Do and Madhavan Swaminathan, "Computation and Effect of Field Penetration Through Planes in Multi-Layered Package Power Distribution Networks for Giga-Processors," IEEE 9th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 43-46, Scottsdale, Arizona, October 2000.

[24] Henry Hungjen Wu, Jeffrey W. Meyer, Keunmyung Lee and Alan Barber, "Accurate Power Supply and Ground Plane Pair Models," IEEE Transactions on Advanced Packaging, Vol. 22, No. 3, pp. 259-266, August 1999.

[25] Howard Johnson, Martin Graham, High-Speed Digital Design, Chapter 5, Prentice Hall, 1993.

[26] A. R. Djordjevic, T. K. Sarkar, “Computation of Inductance of Simple Vias Between Two Stripline Above a Ground Plane,” IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-33, pp. 265-269, March 1985.

[27] T. Wang, R. F. Harrington, J. R. Mautz, “The equivalent circuit of a via,” Trans. Soc. Comput. Simulation, Vol. 4, pp. 97-123, April 1987.

[28] T. Wang, R. F. Harrington, J. R. Mautz, “Quasi-Static Analysis of a Microstrip Via Through a Hole in a Ground Plane,” IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-36, pp. 1008-1013, June 1988.

[29] T. Wang, J. R. Mautz, R. F. Harrington, “The Excess Capacitance of a Microstrip Via in a Dielectric Substrate,” IEEE Transactions on Computer-aided Design, Vol. CAD-9, pp. 48-56, January 1990.

[30] P. Kok, D. De Zutter, “Capacitance of a circular symmetric model of a via hole including finite ground plane thickness,” IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-39, pp. 1229-1234, July 1991.

[31] K. Nabors, S. Kim, J. White, "Fast Capacitance Extraction of General Three-Dimensional Structure," IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-40, pp. 1496-1506, July 1992.

[32] Sungjun Chun, Jinseong Choi, Sidharth Dalmia, Woopoung Kim and Madhavan Swaminathan, "Capturing Via Effects in Simultaneous Switching Noise Simulation," IEEE International Symposium on Electromagnetic Compatibility, Vol. 2, pp. 1221-1226, August 2001.

[33] Daniel De Zutter, "The FDTD-method for EMC-problems with application to electrostatic discharge and delta-I noise calculations," IEEE International Symposium on Electromagnetic Compatibility, pp. 226-230.

[34] Haw-Jyh Liaw and Henri Merkelo, "Signal Integrity Issues at Split Ground and Power Planes," Proceedings of 46th Electronic Components and Technology Conference, pp. 752-755, 1996.

[35] K.C.Gupta, Ramesh Garg and I.J.Hahl, Microstrip Lines and Slotlines, Artech House, Dedham, MA, 1979.

[36] Ramesh Garg and K.C.Gupta, "Expressions for wave-length and impedance of a slotline," IEEE Trans. Microwave Theory & Tech., p.532, Aug, 1976.

[37] Minoru Maeda, "An analysis of gaps in microstrip transmission lines," IEEE Trans. Microwave Theory & Tech., pp. 390-396, June, 1972.

[38] David M. Pozar, Microwave Engineering, Chapter 3, Second Edition, John Wiley & Sons, 1998.

[39] Sungjun Chun, Joong-Ho Kim, Nanju Na and Madhavan Swaminathan, "Comparison of Methods for Modeling ALAN's Power Plane Structure," Proceeding of IEEE 9th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 247-250, October 2000.

[40] A. C. Cangellaris and A. E. Ruehli, "Model Order Reduction Techniques Applied to Electromagnetic Problems," Proceeding of IEEE 9th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 239-242, October 2000.

[41] Joong-Ho Kim and Madhavan Swaminathan, "Modeling of Irregular Shaped Power Distribution Networks Using Transmission Matrix Method," Proceedings of the 9th Topical Meeting on Electrical Performance of Electronic Packaging, pp.83-86, Oct.2000.

[42] Larry D. Smith, Raymond Anderson, Tanmoy Roy, "Power Plane SPICE Models and Simulated Performance for Materials and Geometries," IEEE Transactions on Advanced Packaging, Vol. 24, No. 3, pp. 277-287, August 2001.

[43] I. Novak, "Measuring Milliohms and PicoHenrys in Power Distribution Networks," Design Con, 2000.

[44] S. Pannala, J. Bandyopadhyay, M. Swaminathan, "Contribution of Resonance to Ground Bounce in Lossy Thin Film Planes," IEEE Transactions on Advanced Packaging, Vol. 22, No. 3, pp. 249-258, August 1999.

[45] Larry D. Smith, David Hockanson, "Distributed SPICE Circuit Model for Ceramic Capacitors," Proceeding of 51th Electronic Components and Technology Conference, pp. 523-528, Orlando, FL, 2001.

[46] Sungjun Chun, Larry Smith, Raymond Anderson and Madhavan Swaminathan, "Model to Hardware Correlation for Power Distribution Induced I/O Noise in a Functioning Computer System," To be published in Proceeding of 52th Electronic Components and Technology Conference, May 2002.

[47] R. Downing, P. Gebler, and George Katopis, "Decoupling Capacitor Effects on Switching Noise," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 16, No. 5, pp. 484-489, August 1993.

[48] J. Prymak, "Advanced Decoupling using Ceramic MLC Capacitors," 40th Electronic Components and Technology Conference, Vol. 2, pp. 1014-1023, 1990.

[49] T. Hubing, K. Drewniak, T. Van Doren, D. Hockanson, "Power Bus Decoupling on Multilayer Printed Circuit Boards," University of Missouri-Rolla, Rolla, MO 65401.

[50] Mark I. Montrose, Printed Circuit Board Design Techniques for EMC Compliance, Chapter 3, Second Edition, IEEE Press, 2000.

[51] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, T. Roy, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," IEEE Transactions on Advanced Packaging, Vol. 22, No. 3, pp. 284-291, 1999.

[52] Patent Disclosure entitled "A Methodology for the Placement and Optimization of Decoupling Capacitor Locations on Circuit Substrates," Larry Smith, Raymond Anderson, Sungjun Chun, Sun Microsystems Reference No: P6883.

[53] Clayton R. Paul, "Effectiveness of Multiple Decoupling Capacitor," IEEE Transactions on Electromagnetic Compatibility, Vol. 34, No. 2, pp. 130-133, May 1992.

[54] Istvan Novak, “Lossy Power Distribution Networks With Thin Dielectric Layers and/or Thin Conductive Layers,” IEEE Transactions on Advanced Packaging, Vol. 23, No. 3, pp. 353-360, August 2000.

[55] Joseph M. Hobbs, Hitesh Windlass, Venky Sundaram, Sungjun Chun, George E. White, Madhavan Swaminathan, Rao R. Tummala, “Simultaneous Switching Noise Suppression for High Speed Systems Using Embedded Decoupling,” Proceeding of 51th Electronic Components and Technology Conference, pp. 339-343, May 2001.

PUBLICATIONS

[1] **Sungjun Chun**, Madhavan Swaminathan, Larry D. Smith, Jegannathan Srinivasan, Zhang Jin and Mahadevan K. Iyer, "Modeling of Simultaneous Switching Noise in High Speed Systems," IEEE Transactions on Advanced Packaging, vol. 24, no. 2, pp. 132-142, May 2001.

[2] N.Na, J.Choi, **S.Chun**, M.Swaminathan, and J.Srinivasan, "Modeling and Transient Simulation of Planes in Electronic Package," IEEE Transactions on Components, Packaging, and Manufacturing Technology, vol. 23, no. 3, pp. 340-352, Aug. 2000.

[3] **Sungjun Chun**, Larry Smith, Raymond Anderson, Madhavan Swaminathan, "Model to Hardware Correlation for Power Distribution Induced I/O Noise in a Functioning Computer System," To be published in Proceeding of 52th Electronic Components and Technology Conference, San Diego, California, May 2002.

[4] **Sungjun Chun**, Jinseong Choi, Sidharth Dalmia, Woopoung Kim and Madhavan Swaminathan, "Capturing Via Effects in Simultaneous Switching Noise Simulation," IEEE International Symposium on Electromagnetic Compatibility, vol. 2, pp. 1221-1226, Montreal, Canada, Aug. 2001.

[5] **Sungjun Chun**, Joong-Ho Kim, Nanju Na and Madhavan Swaminathan, "Comparison of Methods for Modeling ALAN's Power Plane Structure," Proceeding of IEEE 9th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 247-250, Scottsdale, Arizona, Oct. 2000.

[6] **Sungjun Chun**, Madhavan Swaminathan, Larry D. Smith, Jegannathan Srinivasan, Zhang Jin and Mahadevan K. Iyer, "Physics Based Modeling of Simultaneous Switching Noise in High Speed Systems," Proceeding of 50th Electronic Components and Technology Conference, pp. 760-768, Las Vegas, Nevada, May 2000.

[7] J.Choi, **S.Chun**, N.Na, M.Swaminathan, and L.Smith, "A Methodology for the Placement and Optimization of Decoupling capacitors in Gigahertz Packages and Board," 13th International Conference on VLSI, pp. 156-161, Jan. 2000.

[8] Joseph M. Hobbs, Hitesh Windlass, Venky Sundaram, **Sungjun Chun**, George E. White, Madhavan Swaminathan, Rao R. Tummala, "Simultaneous Switching Noise Suppression for High Speed Systems Using Embedded Decoupling," Proceeding of 51th

Electronic Components and Technology Conference, pp. 339-343, Orlando, Florida, May 2001.

[9] M.Swaminathan, J.Choi, J-H.Kim, J.Choi, J.Mao and **S.Chun**, "Enabling Reliable System Through Ground Bounce Predictions," 2001 Mixed Signal Integrity Workshop, Atlanta, April 2001.

ACHIEVEMENTS

---

[1] Provisional Patent Application Filed by Georgia Tech
Inventors: **Sungjun Chun** and Madhavan Swaminathan
Title: Modeling of Simultaneous Switching Noise in High Speed Systems
Invention Disclosure No: 2408
Filing Date: 12/13/00

[2] Patent Disclosure Filed by Sun Microsystems
Inventors: Larry Smith, Raymond Anderson, **Sungjun Chun**
Title: A Methodology for the Placement and Optimization of Decoupling Capacitor Locations on Circuit Substrates
Sun Microsystems Reference File No: P6883
Filing Date: 3/21/02