Design Tradeoffs Among MCM-C, MCM-D and MCM-D/C Technologies

Asif Iqbal, Madhavan Swaminathan, Michael Nealon and Ahmed Omer

Abstract—The paper describes tradeoffs in electrical performance, wiring density and cost for MCM-C, MCM-D and MCM-D/C technologies. The thin and thick film interconnection media are compared with their associated pros and cons in terms of performance and cost.

I. INTRODUCTION

The improvements in the semiconductor device technology have afforded enormous increases in device speeds and density. The exponential growth in the on-chip device integration and performance has put severe demands on packaging in terms of wiring density, I/O escapes, signal fidelity, net delays and noise containment. To add to the challenge, the performance improvements in packaging are sought at an ever decreasing cost. Thus, computer packaging is seen increasingly as a key component limiting the machine performance. A good package design optimizes the system performance at the lowest cost for a given application. Several factors in computer packaging are motivating the use of MCM. The system designers find that the use of MCM results in significant performance, size, weight and reliability improvements. The increased chip I/O density is requiring a concomitant rise in the package wiring capacity to provide for optimal I/O escapes and inter connections from the chip. The major detractor in the widespread acceptance of MCM has been its high cost. The widespread acceptance of the MCM technology would be contingent on it providing an optimal solution to the system cost and performance objectives. Thus, the MCM technology should offer a portfolio of packaging options spanning a range of cost and performance enabling the system designer to optimize the architecture and machine organization at the design conception stage.

The present work describes design tradeoffs in electrical performance, wiring density and cost for MCM-C, MCM-D and MCM-D/C technologies. MCM-C includes cofired alumina (AlO) substrate using molybdenum metallization and cofired glass-ceramic (GC) substrate using copper metallization. MCM-D technology options include 2-level (coplanar) and a 4-level (triplate) structure utilizing copper in polyimide. MCM-D/C comprises the hybrid of the aforementioned thin and thick film technologies leading to 3, 4 and 5-level thin film (TF) options on top of cofired ceramic substrates. The thin film technologies presented in this work represent a range of ground rule complexity from 25 to 100 μm pitch and have been discussed to show the process/design tradeoffs.

II. PACKAGING TECHNOLOGIES

The wiring layers in the MCM-C technologies are designed in a stacked triplate configuration. The lines in the two adjacent signal layers run orthogonal to each other and are sandwiched between upper and lower reference mesh planes. The mesh planes have openings in a grid pattern to provide vertical interconnections for the substrate signal and power distribution systems. The triplate structure results in a controlled electromagnetic environment for the propagation of high speed pulses.

The 2-level (2-L) thin film structure is designed in a coplanar transmission line configuration with successive lines of power, signal and ground in one layer. The two levels provide X and Y directed wiring. The 4-level (4-L) and 5-level (5-L) thin film structures are designed with the triplate configuration. The difference between them lies in separating the capture pad layer from the lower reference mesh plane. The capture pad layer enables the finer grid thin film wiring (25 μm pitch) to connect to the coarser substrate grid (450 μm pitch). The separation of the capture pad layer from the voltage reference plane at the expense of increasing cost is warranted by noise considerations and will be elaborated in the subsequent section. The cross-section of the 2-level, 4-level and 5-level thin film technologies are shown in Fig. 1. Note that the presence of the capture pads is needed only in the MCM-D/C technology. The thin film technologies use a non-planar thin film process [11] (no planarization) in which the via and metal levels are defined using photosensitive polyimide (PSPI) and photoresist respectively. Laser ablation and reactive ion etching processes are alternative via patterning processes and were not considered in this paper due to the cost/groundrule complexity tradeoffs. Either electroplating or sputter deposition in conjunction with subetching could be used to pattern metal having the desired thickness. The process can handle via thickness in the range 4–20 μm with a double coat of polyimide required for thickness greater than 9 μm. The metal thickness varies depending on the process and the line pitch with the sputtering and electroplating handling thickness <2 μm and >2 μm respectively for as small as 25 μm pitch [2, 3]. For lower
wiring density applications, coarser ground rules may be used, namely, pitches <25 μm to lower the cost.

Among the thin film technologies, the 2-level structure affords the lowest cost, wiring density and performance whereas the 5-level design offers the highest performance and wiring density with the associated cost penalty. The physical parameters for the various technologies are listed in Table I.

## III. MODELING AND PROCESS INTERACTIONS

The electrical design of a high bandwidth MCM requires the choice of the appropriate geometric parameters, namely, signal line width (S), signal line thickness (T), dielectric thickness (D), signal line pitch (P), and the material properties such as conductor resistivity (ρ) and the dielectric constant (εr). Once the physical parameters are known, the electrical design consists of converting the geometric description into an equivalent electrical circuit using electromagnetic modeling. In this work, the electrical modeling was done by using an electromagnetic program [4] employing the spectral domain coupled with the moment method technique. The program involves the full-wave solution of Maxwell’s equations in the spectral domain and is general enough to handle structures commonly present in electronic packages that support non-TEM (transverse electric and magnetic) wave propagation. The non-uniform current distribution in the conductors at high frequencies due to skin effect were also included in the package models.

![Diagram of MCM-D (A), MCM D/C (B & C) Cross section.](image)

**Fig. 1. MCM-D (A), MCM D/C (B & C) Cross section.**

**Table I**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ALO</th>
<th>GC</th>
<th>2-L</th>
<th>4-L</th>
<th>5-L</th>
</tr>
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<tbody>
<tr>
<td>Signal Pitch P (μm)</td>
<td>450</td>
<td>450</td>
<td>50</td>
<td>25.50</td>
<td>25.50</td>
</tr>
<tr>
<td>Signal width W (μm)</td>
<td>100</td>
<td>75</td>
<td>12.5</td>
<td>10.15</td>
<td>10.15</td>
</tr>
<tr>
<td>Signal Thickness T (μm)</td>
<td>25</td>
<td>20</td>
<td>5</td>
<td>4.5,6</td>
<td>4.5,6</td>
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<tr>
<td>Dielectric Thickness D (μm)</td>
<td>75</td>
<td>65</td>
<td>4</td>
<td>5.5,9</td>
<td>5.5,9</td>
</tr>
<tr>
<td>Dielectric Constant(εr)</td>
<td>9.5</td>
<td>5.3</td>
<td>3.5</td>
<td>3.5</td>
<td>3.5</td>
</tr>
</tbody>
</table>

Though a range of thickness, width and pitch can be manufactured using the process, an optimum set of dimensions and layout are required, based on the design to meet the application requirements. The transmission line characteristics are dictated by six critical parameters. They are: characteristic impedance (Z0), delay (T0), capacitive and inductive coupling (C12 and L12 respectively) and resistance both DC and AC (Rdc and Rac) which are a function of the geometry and material properties. The capacitive and inductive coupling generate coupled noise in the system which for a pair of terminated coupled transmission lines can be written as

\[
NEN \approx Kb \times V_{in} \quad \text{for} \quad I > \frac{t_r}{2\tau}
\]

\[
FEN \approx \frac{\tau I \times Kf \times V_{in}}{t_r}
\]

where

\[
Kb = \frac{|C_{12}/C_{11} + L_{12}/L_{11}|}{4}
\]

\[
Kf = \frac{|C_{12}/C_{11} - L_{12}/L_{11}|}{4}
\]

In the above equation, NEN and FEN represent the saturated near end and unsaturated far end noise respectively on the quiet line for an excitation \(V_{in}\) with rise time \(t_r\) on the active line, \(l\) is the coupled length, \(\tau\) is the propagation delay and \(C_{11}\) and \(L_{11}\) are the self capacitance and inductance respectively. The mutual capacitance and inductance factor into the noise equations through the variables \(Kb\) and \(Kf\) which represent the backward and forward coupling coefficients, respectively. The equations assume that the transmission lines are lossless. Since the parameters \(Kb\) and \(Kf\) are proportional to coupled noise, they will henceforth be used as a variable in the parametric optimization and design tradeoff analysis. The DC and AC resistances have been differentiated for the tradeoff studies since Rdc relates to the dc voltage drop on the line as opposed to Rac which is a function of the current return paths on the transmission line. Typically \(Rac \gg Rdc\) and is a function of the frequency of operation.

The variation of the electrical parameters with physical dimensions is well known and will not be dealt with in detail here. As an example, the variation of Z0 and \(Kb\) as a function of the normalized physical dimensions for the 5 level thin film structure is shown in Figs. 2 and 3, where \(b\) is the total thickness from the top of level 2 (bottom mesh) to the bottom of level 5 (top mesh). Figs. 2 and 3 assume that all the lines are shielded using a parallel mesh layout (Fig. 4) and...
includes the capacitive loading effect of lines on the same and adjacent layers. In Fig. 3, $4*K_b$ represents the normalized near end noise generated (with respect to $V_{in}$) of a quiet line sandwiched between two active lines. Unterminated lines are typically used in thin film structures to maintain adequate signal levels through voltage doubling (due to high line resistance). Based on Figs. 2 and 3, a 10 $\mu$m wide line on a 25 $\mu$m pitch with $T = 5$ $\mu$m and $D = 5$ $\mu$m produces an impedance of $\sim 36\Omega$ and near end noise $\sim 10\%$.

The parallel mesh layout shown in Fig. 4 represents the optimum wiring layout [5] for the non-planar thin film process and has been used for the 4 and 5-level electrical characteristics in Table III. The layout is optimum since all the interconnections are perfectly shielded by the corresponding conductors in the mesh plane which leads to minimum non-planarity in the topography of the structure. Any variation to the layout in Fig. 4 either by shifting the position of the interconnects (to increase impedance) or by changing the mesh plane pattern could increase the interlevel shorts (process limitation) and produce variations in the electrical characteristics due to the changing dielectric thickness along the line length. Based on process and electrical interactions, the physical dimensions that represent the optimum dimensions from a process and design perspective are tabulated in Table I.

Though numerous papers are available depicting the variation of the line characteristics with physical dimensions, there is little information available on the mesh design which represents a critical part of any wiring structure. For example, this paper uses a parallel mesh as opposed to a diagonal mesh used by Shimada et al. [6] The change in the mesh design could have a large effect on the transmission line characteristics. As a comparison, consider two mesh plane designs namely parallel and diagonal mesh as depicted in Figs. 4 and 5 respectively. Both designs represent a triplate structure as in Fig. 1C (MCM D/C) with identical cross section ($T = 5$ $\mu$m and $D = 4$ $\mu$m), wiring pitch ($P = 25$ $\mu$m) and line width ($W = 12.5$ $\mu$m). The mesh plane conductors in Fig. 5 are oriented at a 45 degree angle as compared to the signal lines with a diagonal opening of 75 $\mu$m and conductor width of 18 $\mu$m (dimensions used to fit the layout into the modeling grid). This is in contrast to Fig. 4 where the lines and mesh conductors have a parallel orientation (with a mesh conductor width of 12.5 $\mu$m). The effect of the plane orientation and hole sizes on the line characteristics can be readily seen in Table II.
### Table II

<table>
<thead>
<tr>
<th>Variable</th>
<th>Parallel Mesh</th>
<th>Diagonal Mesh</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z0 (Ω)</td>
<td>28.6</td>
<td>40.4</td>
</tr>
<tr>
<td>T0 (ps/cm)</td>
<td>63.0</td>
<td>72.6</td>
</tr>
<tr>
<td>Kb (%)</td>
<td>3.2</td>
<td>8.9</td>
</tr>
<tr>
<td>Kf (%)</td>
<td>-0.19</td>
<td>-2.82</td>
</tr>
</tbody>
</table>

Z0: Characteristic Impedance  
T0: Time Delay  
Kb: Backward Coupling Coefficient  
Kf: Forward Coupling Coefficient

Kb = \frac{(K_{c} - K_{l})}{4}  
K_{c} = \frac{L_{11}}{C_{11}}  
K_{f} = \frac{L_{12}}{L_{11}}

As mentioned previously, the difference between the 4 and 5 level thin film wiring was the merging of the capture pad and reference levels. This results in the presence of capture pads and mesh on Level 1 in Fig. 1B which leads to a non-uniform bottom mesh layout. The physical non-uniformity translates into electrical line variations (such as impedance and noise increases) as a result of the presence of a non-uniform packaging environment for signal propagation on the interconnects [5]. The noise on the lines is further increased by the additional energy induced by the switching capture pads. The problems encountered by a 4-L design are schematically depicted in Fig. 6 for a signal propagating on the interconnects. The forward and return currents are shown for an even mode excitation. The larger current loop formed by the return currents due to the capture pads leads to increased self and mutual inductance of the lines with a corresponding increase in the near end and far end coupled noise. The larger self inductance leads to increased delays and impedance. The capacitance (both self and mutual) increases to a lesser degree as compared to the inductance. Fig. 6 also depicts the capacitive coupling introduced due to any voltage switching on the capture pads. An equivalent circuit to assess the effect of capture pad to line coupling is shown in Fig. 7 for the 4 level design.

Though the 4-L design reduces cost, one has to look at the application requirements to assess the effect of the impedance variation, noise increase and capture pad to line coupling on the system. Hence the reduction in one via level between the 4 and 5 level design is a trade-off between cost and application.
IV. PACKAGE SIMULATION

The electromagnetic modeling generates a set of electrical parameters which characterize the signal propagation and noise characteristics of the package structure. These electrical parameters are tabulated in Table III and may serve as one of the sources of guidance in matching a system application to the package type. Note that the coupling coefficients for MCM-C are given for horizontal, vertical and diagonal coupling because they contain multiple triplate wiring structures (multiple plane pairs). The attenuation constant taking into account the frequency dependent skin effect losses in signal lines is shown in Table III at 1 GHz indicating the differences in magnitude among the thin and thick film technologies. An ideal package would offer a characteristic impedance \( Z_0 \) to be near 50 \( \Omega \), while the signal propagation delay \( T_0 \), the attenuation constant \( \alpha \) and the coupling coefficients to be as small as technologically possible. The desire for the ideal performance notwithstanding, there are, still, many degrees of freedom available to the package designer to fit the package to the system needs while satisfying the economic and performance constraints. The circuit simulations were done to assess the net delay and crosstalk noise among the various interconnection media.

\[\begin{array}{cccc}
\text{Parameter} & \text{ALO} & \text{GC} & \text{2-L} \\
Z_0 (\Omega) & 51 & 50 & 44, 36.41, 36.41 \\
T_0 (\mu s/cm) & 110 & 80 & 79, 65, 65 \\
R_{dc} (\Omega /cm) & 0.3 & 0.2 & 3.2, 4.4, 2.2, 4.4, 2.2 \\
\delta (10^8 /cm) & 0.013 & 0.009 & 0.04, 0.06, 0.03, 0.06, 0.03 \\
K_{bh} (%) & 3.4 & 0.6 & 3.0, 3.17, 3.17 \\
K_{bd} (%) & 96 & 14 & - \\
K_{h} (%) & 49 & 52 & - \\
K_{h} (%) & 69 & 67 & -6, -65, -65 \\
K_{v} (%) & -36 & -46 & - \\
K_{D} (%) & -40 & -17 & - \\
\end{array}\]

**Table III**

**Fig. 7.** Equivalent Circuit for Pad to Line Coupling.

**A. Net Delay Comparison**

The internal IBM time domain circuit simulator (ASTAP) [7] was used to simulate the net delay from the driver input to the receiver input for each of the packaging media for relative comparison. A source terminated CMOS driver with a voltage slew rate of 2. 5 V/ns was used for the net delay simulations as a function of the package wiring length and the rising waveform delay was computed at the 50% levels of the voltage swing. The signal redistribution length from the chip terminal to the 1st package wiring plane was modeled as an RLC \( \pi \) network and the transmission line was loaded with a 3pF capacitor.

The comparative net delays for the three types of interconnection media are plotted in Fig. 8 as a function of the line length ranging from 10 to 200 mm. The lines in the alumina (ALO) and glass-ceramic (GC) substrate show a linear response due to the predominantly capacitive charging effects. There are two curves shown for the thin film medium to bound the delay for the line resistance. The low resistance thin film (TF-.2) line (0.2 \( \Omega/mm \)) shows a nearly linear response while the high resistance (TF-.6) line (0.6 \( \Omega/mm \)) exhibits a quadratic response owing to the RC charging effects. It is instructive to note that the thin film will not be the optimal medium to drive long transmission lines due to the significantly higher attenuation and distortion. Thus, the raw time of flight delay can be a misleading parameter to compare the signal delays in various package media and the use of the thin film medium must be based on a careful analysis that demonstrates its higher wireability benefits at the expense of additional cost and complexity.

**B. Crosstalk Noise Comparison**

The circuit simulations employing the IBM time domain circuit simulator (ASTAP) was done to compare the crosstalk noise in the signal lines among the various package structures. A CMOS driver with a voltage slew rate of 2.5 V/ns in a source terminated mode along with a quiescent driver in a 2-line configuration were used to simulate the near end (NEN) and far end (FEN) noise coupling. To account for the chip to package signal redistribution length, an RLC \( \pi \) network was used to model the space transformation from the chip terminal to the 1st wiring plane of the package.
The NEN values are plotted in Fig. 9 as a function of the coupled length. The relative crosstalk values must be balanced against the system noise margins. Thus, a high noise margin system may tolerate a noisy package availing the benefit of low cost.

The capture pad layer enable the melding of the thin film wiring with the thick film technology by connecting the thin film vias with the substrate vias. The pads are roughly 250 μm diameter or square to account for the substrate distortion and shrinkage in firing process while at the same time facilitating the thin film patterning process. The migration from the 4-level thin film to the 5-level structure was driven by the pad coupling noise and electrical variations in the interconnects. A switching net that uses the capture pad to go into the substrate would electromagnetically couple with the other thin film nets running over the capture pad causing unwanted noise. The 5-level structure places the bottom reference plane between the pad layer and the thin film wiring layer effectively shielding the thin film signal lines. The results of the modeling and simulations to compare the extent of the pad noise coupling using the circuit in Fig. 7 with a voltage slew rate of 2.5 V/ns and capture pad grid of 500 μm show the coupled noise to be about 3-5 mV per pad. The significance of this noise has to be viewed against the overall system noise budget and is dependent on the number of simultaneously switching nets and the number of the switching pads they pass over.

C. Power Distribution

The MCM power distribution design is critical to control the AC/DC voltage drops at the device level. The choice of the connector scheme for the 2nd level interconnection is a major design variable in controlling the DC drop. The use of edge connectors or cavity pin grid array (PGA) for the 2nd level interconnection in MCM-D and in some MCM-C results in high series resistance and inductance. MCM-C in standard PGA form provides a vertical power feed from the pin to the chip and its path resistance is a function of the number of ceramic layers, power vias and pins. It also offers the flexibility of adding more power planes to minimize the differential drop across all the chips in the MCM. The presence of the thin film power planes in MCM-D/C further minimizes the interchip DC drop.

The AC voltage drop is due to the inductive and capacitive nature of the power supply network. Decoupling capacitors are typically used to control the power supply noise to support the high simultaneously switching applications. The effectiveness of decoupling depends on the low path inductance from the capacitor to the device. The thin film power planes in MCM-D and MCM-D/C provide a low inductance path whereas the MCM-C technology provides decoupling through its top internal power planes using vias. The major differences in decoupling between the MCM-D and MCM-C are the via lengths and power plane separation affecting the series and mutual inductance of the decoupling path. The power supply decoupling efficiency of the MCM-C and MCM-D technology are best illustrated by means of an example as shown in Fig. 10. Consider an MCM consisting of chips and decoupling capacitors attached by means of solder bumps [9] to the top surface of the package (Fig. 10B). Since the capacitors function as power supply decouplers, an interconnection medium is required to enable the capacitor solder bumps to contact the power supply planes (Vdd and Gnd mesh planes). To compare the MCM-C and MCM-D technologies in terms of effective power supply decoupling, two interconnection mediums viz. ALO and TF have been used in Fig. 10. The ALO medium uses two power planes (Vdd and Gnd) separated by 0.15 mm (thick film) with the Vdd plane to TP (top surface of the package) separation of 0.45 mm. The 0.45 mm separation was required due to the inclusion of a redistribution layer between TP and Vdd for fanout of the signal I/Os (not shown) from a 0.225 mm to 0.45 mm grid. On the other hand the TF medium in Fig. 10 uses power plane separation of 0.045 mm (thin film) with a TP to Vdd distance of 0.009 mm (redistribution layer not required). Though Fig. 10 shows a part of the
Comparison of capacitor effectiveness for Power Supply Decoupling module, the layout can be used to calculate the effectiveness of the decoupling capacitors by computing the effective loop inductance from the capacitor to the power supply terminals of the chip. For the ALO (MCM-C) medium, the loop inductance was calculated to be 325 pH as opposed to 43 pH for the TF (MCM-D) medium providing a reduction of ~7X in the loop inductance. In other words, MCM-D technology can support more simultaneously switching drivers as compared to MCM-C, for identical capacitors, drivers and delta I noise. In general, the loop inductance in MCM-D is five fold lower than that of MCM-C.

D. Wireability

As the chip I/O and the number of chips per MCM increase, the wireability of such an application becomes a major challenge. Fig. 11 graphically shows wiring capacity of each of the different MCM technologies discussed in this paper. Note that the actual wiring utilization is roughly 40–50% of the wiring capacity due to the local congestion, blockages and coupled noise limitations. As an example, the MCM-C pitch is shown to be 450 μm, although it is available in 400, 450, and 500 μm pitches. MCM-C is shown as a function of the number of (PP) plane pairs (triplate structures) within the package and it can have as many as 63 layers. MCM-D shows 25 and 50 μm pitches (50 and 100 μm for 2-L). There are multiple ways of achieving the same wiring capacity. An application requiring 400 cm/cm² of wiring capacity could be met by an MCM-C with 10 PP or a 2-L MCM-D at 50 μm pitch or a 4-L MCM-D at 50 μm pitch or an MCM-D/C with 2, 4, or 5-L MCM-D options with different respective ceramic PP. The differences are associated with other factors such as cost and performance. The I/O escape factor is not shown in Fig. 11 but becomes increasingly important as the chip I/O and/or I/O density increases, especially in the case of large size flip chips.

V. Design Tradeoffs

An optimal package design satisfies the system application needs with economy of resources while meeting the system performance and time to market requirements. In evaluating the goodness of fit for the package to a given application, the system requirements for the package may be stipulated by parameters, namely, the off-chip pinouts (I/O per cm²), wiring capacity, average wire length, net delays, maximum allowable wiring length, reflection, crosstalk and simultaneously switching noise, cost and delivery schedule. The delivery schedule is important because of the increasing need for a system to meet time-to-market requirements. As stated by Hennessy [8], a processor design that is late is often obsolete.

The primary tradeoff variables between the thin and thick film technologies are the via density, wiring capacity and cost. The cost is a function of the overall complexity, the material set, # of layers/levels, size of substrate, # of UP’s per laminate or wafer, wiring pitch, total wiring length, # of vias, etc. These complexity factors drive the defect-limited yield. The next cost determinant is the process-limited yield which includes handling, damage, tool malfunction, etc. Lastly, the burden rate of the factory, namely, the space, tools, manpower, etc. affect the cost. Thus, there is a minimum cost for every design independent of its complexity. Since the MCM-C is a mature technology, it is less costly than that of MCM-D. Within MCM-D, the 2-L is less expensive than that of the 4-L structure due to fewer processing steps and faster turnaround time.
To determine the MCM cost, the I/O complexity factor should be accounted for as well. As the increased chip I/O counts demand higher package I/O density and wiring capacity, the package cost undergoes a non-linear growth. The increased incremental cost is driven by defect-limited yields because the increased I/O density leads to finer lines and vias, and smaller spacings.

To ascertain the performance tradeoffs, the net delays including the off-chip driver and receivers must be taken into account, rather than comparing the raw package time of flight delays. The notion of lower dielectric constant offered by thin film technology leading to lower propagation delay has to be balanced against thin film lines having larger attenuation and distortion resulting in risetime degradation and, hence, increased delays for longer nets. Thus, the thin film nets are faster for short lengths whereas the thick film nets offer better signal integrity for the long nets.

VI. SUMMARY AND CONCLUSION

A suite of MCM-C, MCM-D and MCM-D/C technologies have been described. The design tradeoffs among the various technologies have been stipulated in terms of I/O density, wiring capacity, signal propagation delays, signal fidelity, noise containment and cost. The thin and thick film interconnection media are compared with their associated pros and cons in terms of performance and cost.

The package designer should offer a suite of proven MCM options in terms of performance, wiring capacity, cost and availability to the system architect at the machine conception stage. An early package integration in the system design is needed to produce an optimal cost/performance/time-to-market machine.

The choice of a particular MCM technology should be application-specific in terms of its cost, performance and wiring density tradeoffs.

REFERENCES


Asif Iqbal received B. S. from Rutgers University in 1978, M. S. from M. I. T. in 1981 and Ph. D. from Stanford University in 1987. From 1981 to 1983, he worked at Fairchild Research Center in Palo Alto, CA on MOS device technology. He worked for NCR Corporation modeling the on-chip interconnects for CMOS circuits from 1987 through 1988. He was with IBM Corporation, Hopewell Junction, NY from 1988 to 1993, working on the electrical design and analysis of the multi-chip modules. He is currently with Amdahl Corporation working on the circuit and computer system design. He is the author of nine technical publications and has presented several papers at IEEE sponsored conferences.

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In 1990 he joined the International Business Machines Corporation, East Fishkill, NY, where he is presently working on the design, analysis, measurement and characterization of interconnects for high speed electronic packages.

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Michael Nealon, photograph and biography not available at time of publication.

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