Do Chip Size Limits Exist for DCA?

Andreas Schubert, *Member, IEEE,* Rainer Dudek, *Member, IEEE,* Rudolf Leutenbauer, Ralf Döring, Joachim Kloeser, *Member, IEEE,* H. Oppermann, *Member, IEEE,* Bernd Michel, *Member, IEEE,* Herbert Reichl, Daniel F. Baldwin, Jianmin Qu, Suresh K. Sitaraman, Madhavan Swaminathan, *Senior Member, IEEE,* C. P. Wong, *Fellow, IEEE* and Rao Tummala, *Fellow, IEEE*

***Abstract*— Solder joints, the most widely used flip chip on board (FCOB) interconnects, have a relatively low structural compliance due to the large thermal expansion mismatch between silicon die and the organic substrate. The coefficient of thermal expansion (CTE) of the printed wiring board (PWB) is almost an order of magnitude greater than that of the integrated circuit (IC). Under operating and testing conditions, this mismatch subjects the solder joints to large creep strains and leads to early failure of the solder connections [1]–[3]. The reliability of such flip chip structures can be enhanced by applying an epoxy-based underfill between the chip and the substrate, encapsulating the solder joints. This material, once cured, mechanically couples the IC and substrate together to locally constrain the CTE mismatch. However, the effects of CTE mismatch are assumed to become more severe with increasing chip size. Even with the addition of an underfill material, it has been supposed that there are limits on the chip size used in flip chip applications [4].**

***Index Terms*—Chip size, FCOB, IC design, thermo-mechanical analysis, wafer bumping.**

I. Introduction

THE Fraunhofer Institute IZM/Technical University are collaborating with the Georgia Institute of Technology to study fundamental limits of direct chip attach. The objectives of this collaborative effort are:

1) to understand the material and mechanical issues related to the thermo-mechanical reliability of direct chip attach;
2) to determine the fundamental limits of chip size by taking the processing conditions, process-induced defects, underfill material property requirements, geometry limitations and service environment into consideration;
3) to investigate the impact of various geometrical, material and operating parameters on the thermo-mechanical reliability of flip chip assemblies and to determine an optimum combination of parameters to minimize delamination, solder joint fatigue, chip cracking, and/or excessive warpage;
4) to validate results of finite element simulations with performed experiments.

Manuscript received March 17, 1999; revised October 13, 1999. This work was presented at the International Symposium on Advanced Packaging Materials, Braselton, GA, March 14–17, 1999. This work was supported by the National Science Foundation through the Packaging Research Center, Georgia Institute of Technology.

A. Schubert, R. Dudek, R. Leutenbauer, R. Döring, J. Kloeser, H. Oppermann, B. Michel, and H. Reichl are with the Fraunhofer Institute for Reliability and Microintegration IZM, Berlin D-13355, Germany.

D. F. Baldwin, J. Qu, S. Sitaraman, M. Swaminathan, C. P. Wong, and R. Tummala are with the Georgia Institute of Technology, Atlanta, GA 30332-0560 USA.

Publisher Item Identifier S 1521-334X(99)10392-6.

II. IC Trends—Packaging Roadmaps

Growing demands on performance, cost and the advancement in IC technology have drastically influenced packaging and interconnection technology. New packaging technologies and advanced materials have to be developed to handle larger dies, higher input/output (I/O) counts, lower operating voltages, high power consumption and high clock frequencies.

Along with the national roadmaps published by organizations such as the Semiconductor Industry Association (SIA) in the United States and the Electronic Industries Association of Japan (EIAJ), many IC companies have their own roadmaps describing the evolution of IC packaging.

The European NETPACK roadmap [5] describes the projected use of area-array packaging technology in the three market applications critical for the European electronics industry: telecommunications, automotive, and mobile systems.

Of the three market applications considered in this roadmap study, telecommunications is the most performance driven (Table I). This market requires larger packages with more I/O at a finer pitch operating at higher frequencies and dissipating more power than either the automotive or mobile systems markets. Power dissipation is expected to double between 1998 and 2004, from 5 to 10 W, while the chip area increases by 40% from 600 mm^2 to 850 mm^2 resulting in an increase in power density. The roadmap for maximum operating frequency of IC's for telecommunications shows an increase from 2000 MHz to 8000 MHz.

Not surprisingly, the assembly and packaging roadmap for the automotive market shows the least aggressive changes of the three market applications (Table II). Because of the somewhat conflicting needs for both high reliability and low cost, automotive electronics has been slow to adopt new technology, preferring to wait as a new approach develops a history of reliability in other applications while moving down the pricing curve. Although ongoing research in industry addresses some of the issues, there is a lack of fundamental work on the impact of large IC attach to organic boards on thermo-mechanical reliability (also projected by the SIA roadmap to be 4.0 cm for memory applications in the year 2012).

TABLE I
IC PARAMETERS FOR THE TELECOMMUNICATIONS MARKET

	1998	1999	2000	2001	2002	2003	2004
Power Dissipation (W)	5	10	10	10	10	10	10
Chip Size (mm^2)	225-600	223-650	225-700	225-700	225-700	225-800	225-850
Max Chip I/Os	350-650	400-700	400-760	400-800	600-850	600-900	800-1000
Operating Freq (MHz)	600-2000	2400	4000	4000	8000	8000	8000

TABLE II
IC PARAMETERS FOR THE AUTOMOTIVE MARKET

	1998	1999	2000	2001	2002	2003	2004
Power Dissipation (W)	1-2	1-2	1-2	2-3	2-3	2-4	2-4
Chip Size (mm^2)	100-250	100-300	150-350	150-400	200-425	225-450	250-500
Max Chip I/Os	150	150	150	150	200	200	200
Operating Freq (MHz)	8/16	8/16	8/16	8/16	32/50	32/50	32/50

TABLE III
DIE SPECIFICATION

No.	size [mm^2] incl. saw track	pitch [mm]	Pad [µm, okt.]	Pass [µm, okt.]	matrix	I/Os	/wafer
24.1	10,0x10,0	500	140	120	16x16	250	20
24.2	20,0x20,0	500	140	120	36x36	1290	13
24.3	30,0x30,0	500	140	120	56x56	3130	8
24.4	40,0x40,0	500	140	120	76x76	5770	6
24.5	10,0x10,0	500	140	120	16x16	221	18

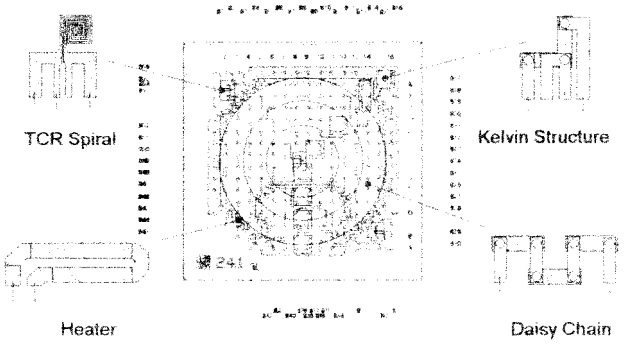


Fig. 1. Test structures.

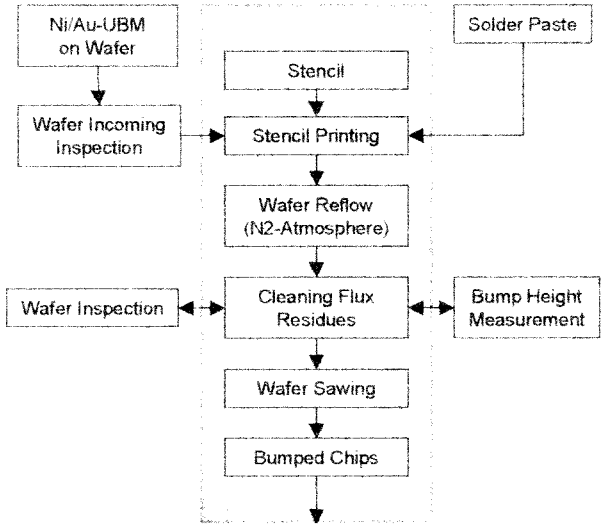


Fig. 2. Process flow for low cost bumping.

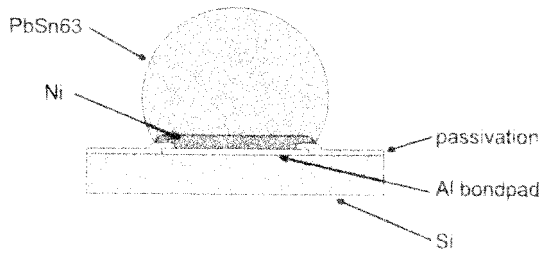


Fig. 3. Scheme of a solder bump with electroless Ni UBM.

III. IC DESIGN AND TEST STRUCTURES

For the large IC flip-chip attach five different test chips have been designed in different sizes from 10 × 10 mm^2 up to 40 × 40 mm^2 (Table III). With an area pad configuration at a pitch of 500 μm I/O numbers from 250 up to 5770 have been achieved. The four direct circuit (DC) test chips comprise daisy chains, Kelvin structures, TCR spirals and heaters distributed all over the die area (Fig. 1). The RF test chip includes inductance and capacitance measurement structures, through lines and shorts, all realized as coplanar lines.

IV. WAFER BUMPING FOR DCA

To achieve adequate economics and performance, the selection of the suitable bumping technology becomes very important. One of the economical methods for bump production on wafers is solder paste printing using a solderable electroless Ni/Au metallization over the Al bond pad. Investigations were described in several publications [6], [7]. In [8] a cost comparison of C4, electroplating and stencil printing on nickel UBM shows that the printing process can save cost up to 1/8 of the C4 and up to 1/4 of the electroplating process.

TABLE IV
EQUIPMENT USED FOR PRODUCTION OF SOLDER BUMPED CHIPS

Process step	equipment
Ni/Au UBM	8 " lab line
Solder paste printing	DEK 265 LT
Solder paste reflow	SMT 300 3.0 N2
Flux cleaning	Miele IR 6001
Bump inspection	Zeiss ZKM 500 Planaris
wafer dicing	Disco DAD 341
chip picking	Datacon PPS 2210

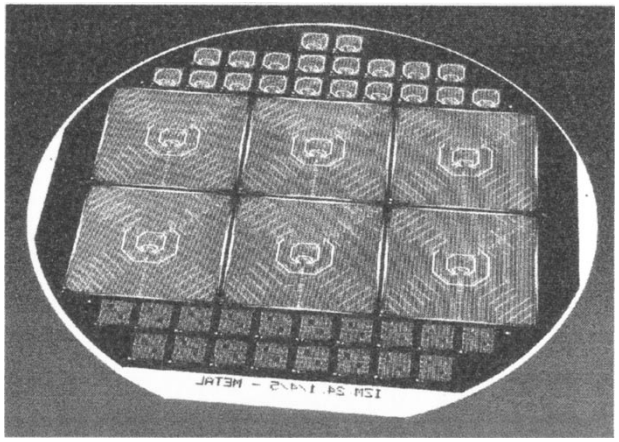


Fig. 4. Stencil printing technology of 6 in-wafer: no. of dies 44, pitch 500 μm, no. of bumps 43 598, IC size 10mm and 40 mm.

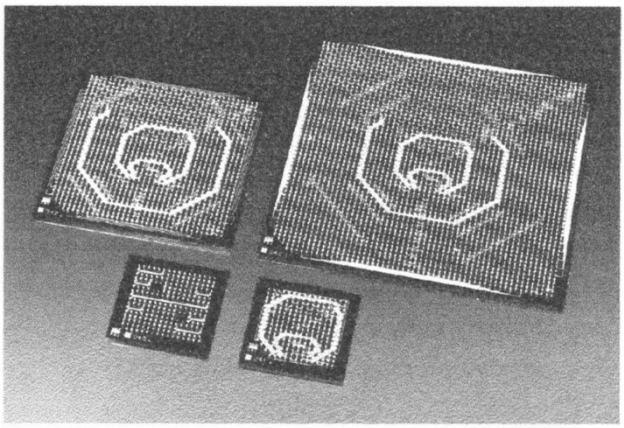


Fig. 5. Single chips, IC size 10 mm to 30 mm, I/O counts 250 to 3130.

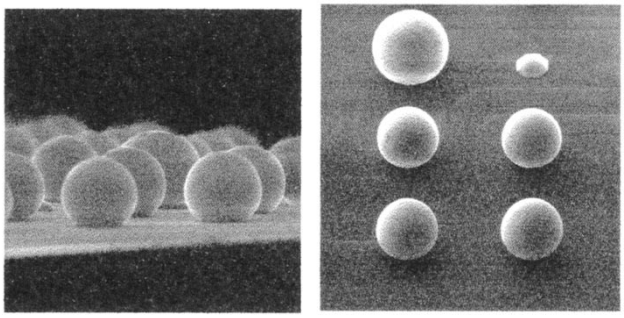


Fig. 6. Most significant failure: solder "stealing."

TABLE V
SELECTED CONSTITUTIVE MATERIALS CHARACTERISTICS

Material	Constitutive Equation	Young's Modulus [MPa]	CTE (1/K)
Underfill + 0 % SiO_2	viscoelastic	6,000 at 218 K 4,100 at 295 K 1,420 at 343 K 330 at 373 K 100 at 423 K	60.0 10^{-6}
Underfill + 63 % SiO_2	viscoelastic	9,000 at 218 K 8,500 at 295 K 7,800 at 343 K 6,000 at 393 K 1,850 at 413 K 450 at 433 K 200 at 550 K	29.0 10^{-6} at 210 K 29.0 10^{-6} at 398 K 73.0 10^{-6} at 408 K 73.0 10^{-6} at 523 K
Solder Mask	viscoelastic	6,000 at 218 K 4,100 at 295 K 1,420 at 343 K 330 at 373 K 100 at 423 K	30.0 10^{-6}
37Pb-63Sn	elastic-viscoplastic	36,000 at 210 K 21,000 at 398 K	24.0 10^{-6}

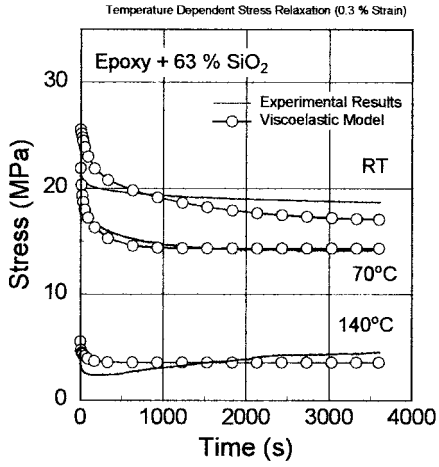


Fig. 7. Stress relaxation of the underfill encapsulant in dependence on temperature.

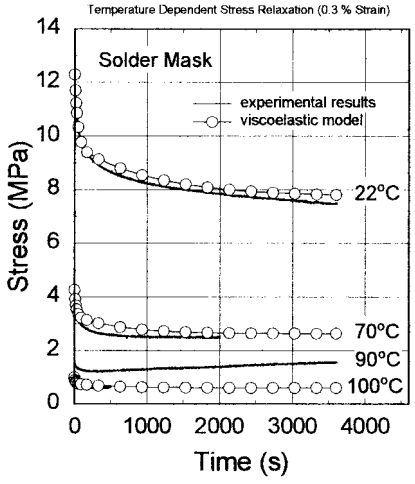


Fig. 8. Stress relaxation of the solder mask in dependence on temperature.

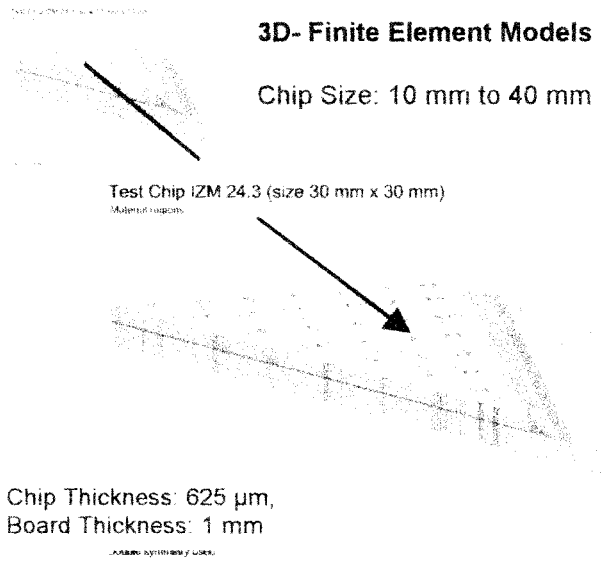


Fig. 9. Three-dimensional finite element models of FCOB assemblies with die sizes 10 mm to 40 mm.

Fig. 10. Area-array configuration, FE-model of the solder bumps.

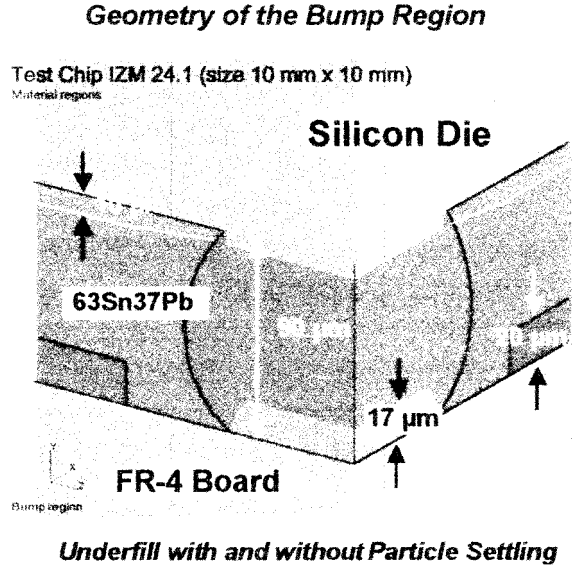


Fig. 11. Geometry of the bump region.

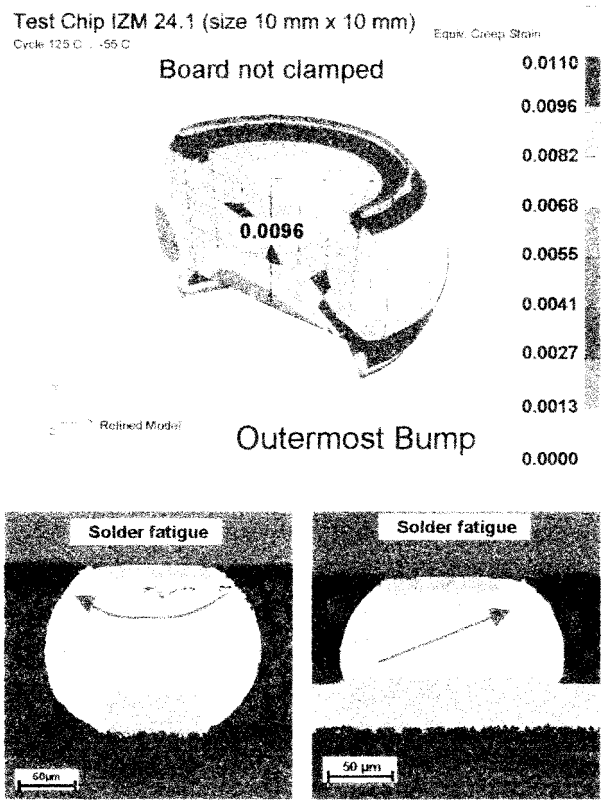


Fig. 12. Calculated and observed damage paths of solder fatigue.

In the following the low cost wafer bumping process will be described in detail. Fig. 2 shows the complete process flow of the wafer bumping technology.

The principle structure of a low cost bump is shown in Fig. 3. A layer of Ni covered by a thin Au coating is chemically deposited on the Al bond pads. The Ni UBM serves as an adhesion layer and a diffusion barrier between Al and solder. The Au is required to protect Ni from oxidation before solder application. Solder is applied by stencil printing of paste and subsequent reflow. Then the wafers are cleaned to remove flux residues.

To determine the bumping yield and to identify defect dies, wafers are inspected by an optical measurement system. With the flip chip equipment of the institute chips are handled in waffle packs. Therefore, wafers have to be diced finally and chips have to be picked (Figs. 4 and 5). The equipment used for solder bumping allows to handle wafer sizes up to 8 in. The corresponding equipment is listed in Table IV.

V. Experimental Issues

For the bumping experiments a Ni/Au-UBM with a height of 5 μm was applied on the 6 in wafers. The stencil printing of solder paste was performed using a stainless steel metal stencil. According to the printing pitch of 500 μm the aperture size was chosen to 350 μm $\times$ 350 μm square. Due to the high manufacturing cost of laser cutted stencils for very high numbers of apertures we used a chemical etched stencil for the experiments. The thickness of the designed stencil was 120 μm. For printing a eutectic Sn/Pb-63/37 solder paste from Heraeus was used (F 362). The particle size of

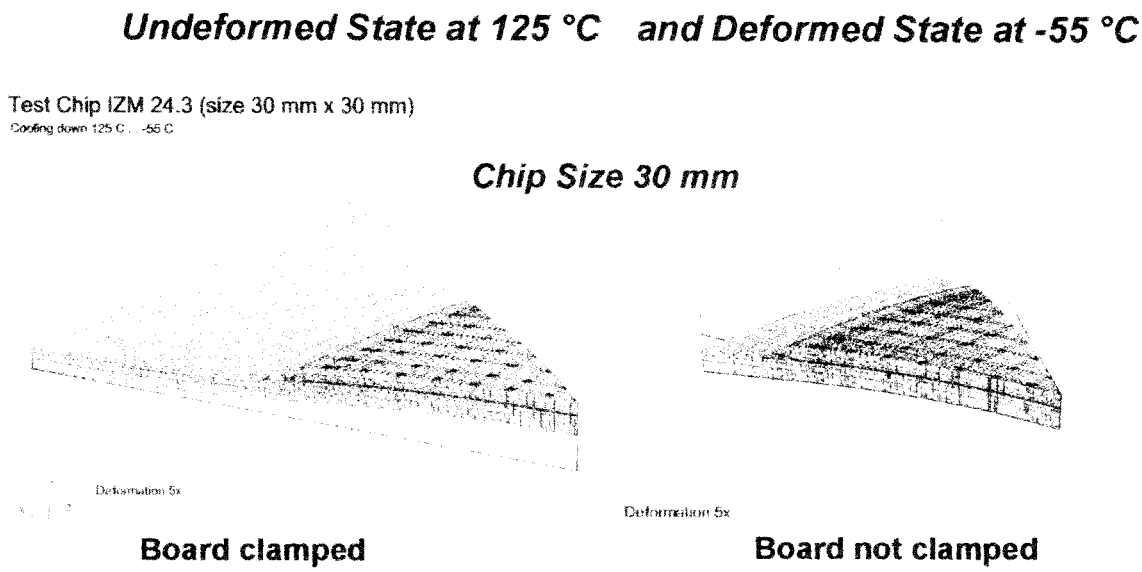


Fig. 13. The used two assembly constraints.

the paste was 25–75 μm. The reflow was performed under Nitrogen atmosphere and a standard reflow profile according to recommendations by Heraeus was used.

After cleaning the flux residues the measured average bump height was 215 μm. The measurements of the bump height distribution over a 6 in wafer show deviations in the range of $\pm$3% from the average value. The main failure mode we observed was solder stealing (see Fig. 6). Due to the high number of apertures the adhesion between the stencil and the flux of the solder paste was very high. Therefore the loosening of the stencil was critical after the printing process. A slight shift of the solder deposits from the contact pads of the wafers was the result. Whenever the shift was too large, solder was stolen by the neighbor bump during reflow.

VI. Finite Element Simulation

Materials used in the structures include FR-4 as board, nickel metallizations and copper traces, silicon die, underfill and solder mask. The copper behavior is considered as elastic-plastic. However, the solder (63Sn37Pb) has to be modeled using nonlinear constitutive laws with rate dependent plasticity (creep). The polymeric materials underfill and solder mask were treated as viscoelastic materials. Uniaxial stress relaxation tests have shown temperature dependent relaxation over a wide temperature range. Viscoelastic constitutive models have been developed for finite element analysis. Temperature dependence of the viscoelastic material response enters the calculation by both temperature dependent elastic constants and a temperature-time shift function (Table V, Figs. 7 and 8) [9], [10].

For purposes of this study, four one-eighth symmetric 3D FE models were created for 10 mm, 20 mm, 30 mm, and 40 mm square silicon dies of 0.625 mm thickness. The dies are mounted onto a 1 mm thick FR-4 board in area-array configuration with a pitch of 500 μm (Figs. 9 and 10). The interconnects are eutectic solder joints with a bump height of 90 μm. The remaining gap between silicon die and substrate is filled with solder mask up to 20 μm in height and the balance with an underfill material. Sometimes a particle settling is observed in the underfill material. To quantify this effect on the solder reliability the underfill layer was considered as "two-layered" with pure epoxy and epoxy filled with silica (Fig. 11).

VII. Thermo-Mechanical Analysis Using Non-Linear Finite Element Simulation

The chip connected to the substrate is a multimaterial structure. The mismatch in coefficients of thermal expansion between the different materials induces stresses and strains if the structure is subjected to temperature changes. The reliability of the solder connections is a critical issue. After a certain number of thermal cycles, the cyclic inelastic deformation of the solder can result in fatigue failure. To account for the time and temperature dependent nature of the solder in the calculation, the solder strain rate is additively composed of elastic and creep terms. Due to the slow loading rates in typical low cycle fatigue experiments, the temperature and time dependent secondary creep strain determines the nonlinear solder response.

In many cases it was observed that the experimentally detected damage zones coincide with the calculated bands of local maximum equivalent creep strain. The perfect plastic response reduces the load carrying capacity of highly strained solder volume elements during major parts of the thermal cycle. These solder volume elements react like weakened zones [11], [12]. Therefore, a life time model adapted from the Coffin–Manson type relation, which transforms the amplitudes of the accumulated equivalent creep strain along the damage path into an estimation of the number of thermal cycles to failure, can be used. These calculations must be taken as a tendency, not as accurate values (Fig. 12).

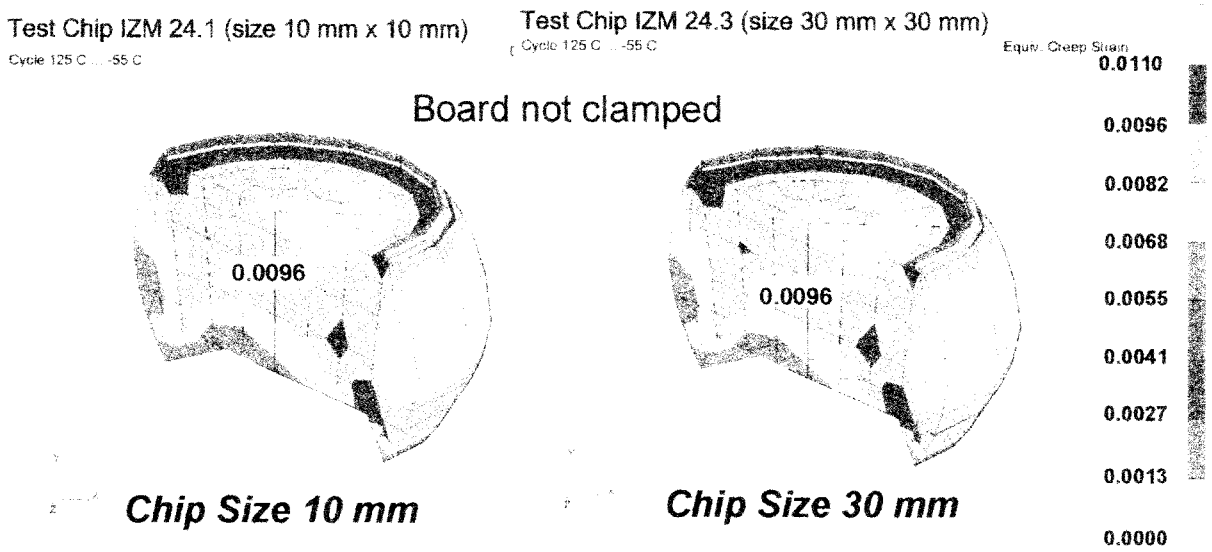


Fig. 14. Accumulated equivalent creep strain distribution in the outermost solder bumps.

The temperature cycle was chosen to range from 125 °C to −55 °C with 5 min ramp times and 10 min dwell times for a total cycle time of 30 min.

The parameters investigated in this study include die size and the effect of particle settling. Furthermore, the deformed shape of the flip chip structures depends on the size and assembly constraints of the PWB (clamped board or not clamped board, Fig. 13).

VIII. Simulation Results and Discussion

Fig. 14 is a plot of the accumulated equivalent creep strain distribution in the outermost solder bump for flip chip assemblies with a die size of 10 mm and 30 mm. It is evident that creep strain is distributed throughout the solder bump and is not constant. Calculation results for the eutectic solder joints indicate a creep strain concentration near the outer die pad edge. The solder crack path is expected to start circularly near the outer die pad edge and grow underneath the die pad or later along the diagonal direction crossing the solder bump. When comparing the influence of the two chip sizes, the accumulated equivalent creep strain distributions in the solder are very similar. Fig. 15 illustrates the effects of die size (10 mm to 40 mm) for a not clamped board on the maximum creep strain amplitude across the solder bump. These creep strains are independent of the die size.

Sometimes particle settling is present in the underfill material. From the mechanical point of view this means lowering of the overall attachment stiffness due to an additional "layer" of pure epoxy with low Young's modulus and high CTE. This leads to an increase in the creep strain range and to a reduction in life time. It should be noted that the predicted damage path is not influenced by the settling effect (Fig. 16).

Although underfilling can reduce the strains in the solder joints, it results in the risk of delamination along the chip-underfill and/or underfill-solder mask interfaces during temperature cycling [3], [13]. Special attention has to be directed to the interface properties as well as the direction

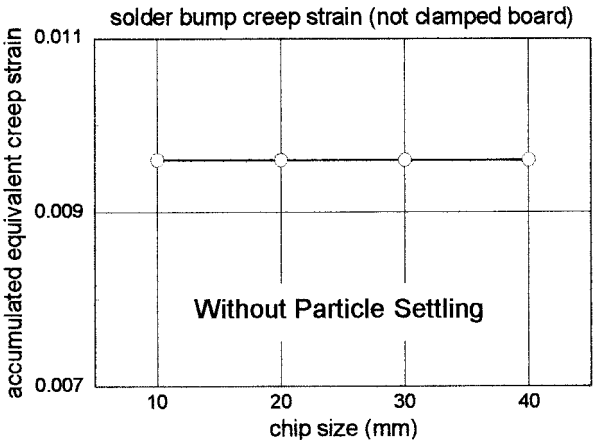


Fig. 15. Creep strain in the outermost solder bump.

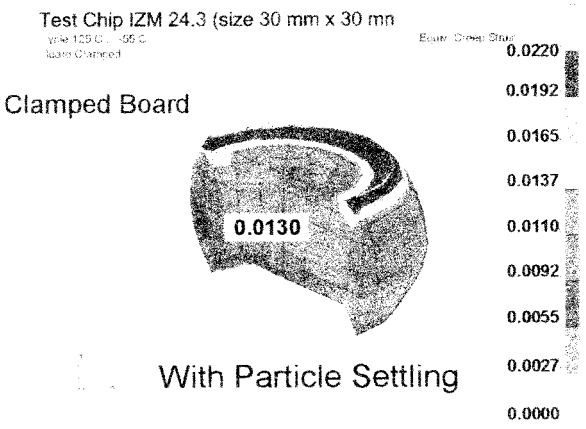


Fig. 16. Accumulated equivalent creep strain distribution in the outermost solder bump.

of the stress components acting upon these interfaces. Elastic stress singularities might occur at these bimaterial edges. Together with the viscoelastic material description, the singular

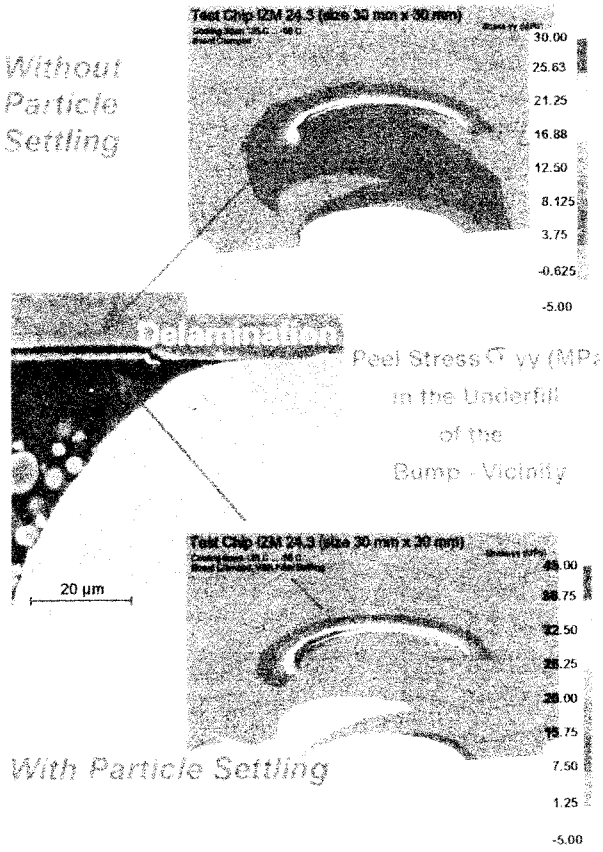


Fig. 17. Peel stress component σ_{yy} in the underfill (thermal load 125 °C $\cdots$ –55 °C), chip size 30 mm.

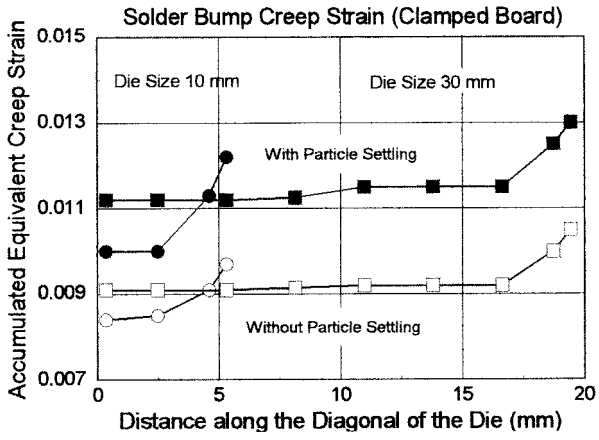


Fig. 18. Creep strains in the solder bumps in dependence of bump position.

behavior takes a temperature and time dependent form, which is rather difficult to handle. Therefore, FE-approximations using the same mesh density might be considered comparable, while absolute values cannot be given at the singular points.

Fig. 17 demonstrates the localized character of the peel stress component σ_{yy}. Note that the peel stress switches from compressive near the encapsulated corner of the chip to tensile in the vicinity of the eutectic solder bumps. The calculated maximum tensile peel stresses can be used as an indicator of delamination risk in comparative studies looking for proper material characteristics and design parameters. While the underfill material needs to be stiff enough to provide for effective coupling and reduce the solder joint creep strain, a stiff underfill material may also cause overstresses at the chip-underfill interfaces when the applied thermal load becomes large or the adhesion strength is too low.

The FE analyses have also shown that the fundamental limits on chip size for an underfilled flip chip with a clamped board are not crucially influenced by the distance to the neutral point (DNP) of the outermost solder joint. The strain fields are relatively independent of chip size and DNP (Fig. 18). These facts also suggest that larger die samples will have increased propensities for fracture, not due to increased internal strains and stresses, but due to the fact that they are statistically more likely to contain the critical size flaws under stress conditions for catastrophic crack propagation [14].

The relationship between die size and solder joint failure has a subordinate importance. Manufacturing and process-induced defects are likely to be more important limiting factors (e.g. particle settling). The assembly constraints and the influence of adjacent components may also significantly impact the determination of fundamental limits to chip size [4], [15].

Future work will be concentrated on the assembly process of large dies, the influence of manufacturing defects on thermo-mechanical reliability, and life time analysis by testing and numerical simulation.

REFERENCES

[1] K. Ramakrishna and Z. Johnson, "Effect of material and design parameters on the stresses induced in a Direct-Chip-Attach package during underfill cure," in *Proc. InterPack '97*, Mauna Lani, HI, June 15–19, 1997, pp. 1639–1646.

[2] V. Gektin, A. Bar-Cohen, and S. Witzman, "Coffin-Manson based fatigue analysis of underfilled DCA," in *Proc. InterPack '97*, Mauna Lani, HI, June 15–19, 1997, pp. 1655–1661.

[3] A. Schubert, R. Dudek, and R. Döring, "Reliability investigations of flip chip interconnects in FCOB and FCOG applications by FEA," in *Proc. 2nd Electron. Packag. Technol. Conf.*, Singapore, Dec. 8–10, 1998, pp. 49–56.

[4] C. A. Le Gall, J. Qu, and D. L. McDowell, "Thermomechanical stresses in an underfilled flip chip DCA," in *Proc. 3rd Int. Symp. Exihibition Adv. Packag. Mater.*, Braselton, GA, Mar. 9–12, 1997, pp. 128–129.

[5] E. Jan Vardaman and Frank J. Bachner, *"The NETPACK Roadmap: A European Perspective on Semiconductor Packaging and Assembly*. Austin, TX: TechSearch International, May 1998.

[6] J. Kloeser *et al.*, "Low cost bumping by stencil printing: Process qualification for 200 μm pitch," in *Proc. IMAPS Conf.*, San Diego, CA, 1998.

[7] A. Ostmann, J. Kloeser, R. Aschenbrenner, and H. Reichl, "Strategies for low cost flip chip assembly," in *Proc. ITAB Symp.*, Sunnyvale, CA, 1998.

[8] F. Stepniak, "Solder flip chips employing electroless nickel: an evaluation of reliability and cost," *Adv. Electron. Packag.*, vol. 1, 1997.

[9] R. Dudek, M. Scherzer, A. Schubert, and B. Michel, "FE-simulation for polymeric packaging materials," *IEEE Trans. Comp., Packag., Manufact. Technol. A*, vol. 21, pp. 301–309, June 1998.

[10] A. Schubert, R. Dudek, D. Vogel, B. Michel, and H. Reichl, "Materials mechanics and mechanical reliability of flip chip assemblies on organic substrates," *Adv. Microelectron.*, vol. 24, no. 4, pp. 29–32, July/Aug. 1997.

[11] R. Dudek, M. Nylen, A. Schubert, B. Michel, and H. Reichl, "An efficient approach to predict solder fatigue life and its application to SM- and area array components," in *Proc. ECTC'47*, San Jose, CA, May 1997, pp. 462–471.

[12] A. Schubert, R. Dudek, J. Auersperg, D. Vogel, B. Michel, and H. Reichl, "Thermo-mechanical reliability analysis of flip chip assemblies by combined microDAC and the finite element method," in *Proc. InterPack '97*, Mauna Lani, HI, June 15–19, 1997, pp. 1647–1654.

[13] C. A. Le Gall, J. Qu, and D. L. McDowell, "Delamination cracking in encapsulated flip chips," in *Proc. 46th Electron. Comp. Technol. Conf.*, Orlando, FL, May 1996, pp. 430–434.
[14] T. J. Goh, "Parametric finite element Analysis of solder joint reliability of flip chip on board," in *Proc. 2nd Electron. Packag. Technol. Conf.*, Singapore, Dec. 8–10, 1998, pp. 57–62.
[15] St. Michaelides and S. Sitaraman, "Role of underfilling imperfections on flip-chip reliability," in *Proc. InterPack '97*, Mauna Lani, HI, June 15–19, 1997, pp. 1487–1493.

Andreas Schubert (M'97) received the Ph.D. degree in material sciences from the Mining Academy, Freiberg, Germany, in 1985.

Since 1993, he has been with the Fraunhofer Institute for Reliability and Microintegration (IZM), Berlin, Germany, and is Head of the group "Fracture Electronics." His work is concentrated on thermo-mechanical reliability aspects of advanced packaging technologies (flip-chip and chip size package).

Dr. Schubert is a member of IMAPS and ASME. He is Managing Editor of *Microsystem Technologies* and Editor of the newsletter *European Packaging*.

Rainer Dudek (M'95) received the Ph.D. degree in mechanical engineering from the University of Technology, Chemnitz, Germany, in 1986.

From 1986 to 1993, he was a member of the staff, Department of Fracture and Micromechanics, Institute of Mechanics, Chemnitz. He joined the Fraunhofer Institute for Reliability and Microintegration (IZM), Berlin, Germany, in 1993, where he is involved with finite element modeling, experimentally based constitutive modeling, and failure prediction for electronic materials. He has authored or co-authored several technical publications.

Dr. Dudek is a member of the German Society for Materials Research and Testing (DVM) and is Chairman of the working group "Simulation Methods for Microsystems."

Rudolf Leutenbauer was born in Germany in 1961. He received the Electrical Engineering degree from the University of Munich, Munich, Germany, in 1986.

Since 1987, he has been with the Technical University of Berlin, Germany, specializing first in tape automated bonding of VLSIC's and later in the design of microsystems. In 1996, he joined the Fraunhofer Institute IZM, where he is now Group Leader in the Department of Advanced System Engineering and Local Manager in the Europractice MCM Project.

Mr. Leutenbauer is a member of IMAPS.

Ralf Döring received the diploma in mechanical engineering and information science from the Technical University of Chemnitz, Germany, in 1991.

He joined the Chemnitzer Werkstoffmechanik GmbH (CWM) in 1993, where he is involved with computer design and modeling of microcomponents, finite element modeling, and visualization of numerical and experimental results.

Joachim Kloeser (M'99) received the M.S. degree in electrical engineering from the Technical University of Berlin, Germany, in 1991.

He is a Scientist at the Fraunhofer Institute for Reliability and Microintegration (FhG/IZM) Berlin. In 1992, he joined the Microperipheric Technologies Centre, where he worked on the development of flip chip bonding technologies with thick film ceramic substrates, focusing electric testing, and reliability of flip chip interconnections. Since July 1993, he has been working in a specialized group on chip interconnection and reliability with the special regard to low cost flip chip technologies. In 1996, he became the Group Leader of flip chip processes and manufacturing in the Department for chip interconnection and reliability of FhG-IZM, IZM. He is the Head of Department for Area Array Packaging since 1999. He is the author of several publications on flip chip bonding techniques and reliability.

Mr. Kloeser is a member of the IEEE CPMT Society.

H. Oppermann (M'95) received the M.S. degree in material science and technology from the Technical University, Clausthal-Zellerfeld, Germany, in 1985 and the Ph.D. degree in material science from the Metals Research Institute, Technical University of Berlin, Germany, in 1992.

Since 1993, he has been with the Microperipheric Center, Technical University of Berlin, and was contributing to the development of the gold/tin flip chip soldering technology. Since October 1998, he has been with the Fraunhofer IZM, where he leads the group "Optoelectronic, HF and Sensor Packaging" and is the head of the department "Microsystem Integration." Between November 1998 and May 1999, he was with the Institute of Microsystem and Advanced Packaging Laboratory at the University of Tokyo, Japan, as Associated Professor.

Dr. Oppermann is a member of the IEEE CPMT Society.

Bernd Michel (M'95) received the Ph.D. degree from the Theoretical Physics University, Halle, Germany, in 1976.

He was Professor for Solid Mechanics with the Institute of Mechanics in 1982. Since 1992, he has been Head of the Department Mechanical Reliability and Micro Materials of Fraunhofer Institute (IZM), Berlin, Germany.

Dr. Michel is Chairman of the International Conferences Micro Materials, Berlin, and Chairman of the German Committee on Microsystem Technology, Society for Materials and Testing (DVM), and a member of the editorial boards of five international journals.

Herbert Reichl received the M.S. and Ph.D. degrees in electrical engineering from the Technical University of Munich, Germany, in 1971.

From 1971 to 1987, he was with the Fraunhofer Institute for Solid State Technology, Munich. Since 1987, he has been Professor at the Technical University of Berlin, Germany, and the Director of the Microperipheric Center. In 1993, he became the head of the newly established IZM.

Dr. Reichl is the General chairman of the SMT/ASIC/Hybrid Conference and Microsystem Technologies Conference, Germany.

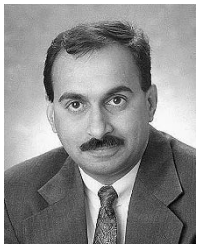
Daniel F. Baldwin received the S.M. and Ph.D. degrees in mechanical engineering from the Massachusetts Institute of Technology, Cambridge, in 1990 and 1994, respectively.

He is an Assistant Professor with the Georgia Institute of Technology, Atlanta, joining the faculty from Bell Laboratories, Princeton NJ, where he worked on electronic product miniaturization. He has seven years of experience in the electronics manufacturing and polymer processing industries, four U.S. patents, over 70 scholarly publications, and expertise in electronics packaging, advanced materials processing, and manufacturing systems design. He currently leads the Low Cost Flip Chip Processing program for the Packaging Research Center (PRC), Georgia Tech, the Advanced Interconnect Technologies research program, Georgia Tech's Manufacturing Research Center, and Georgia Tech's Center for Board Assembly Research (CBAR) Low Cost Assembly Processing Program.

Dr. Baldwin received the ASME Electrical and Electronics Packaging Division's Outstanding Young Engineer Award, in 1998 and the Milton C. Shaw Outstanding Young Manufacturing Engineer Award, Society of Manufacturing Engineers, in 1999. He also received the Outstanding Faculty of the Year Award, NSF Packaging Research Center, Georgia Tech, 1995–1996, the Outstanding Faculty Research Award, NSF Packaging Research Center 1997, 1998, and the Outstanding Faculty Technology Transfer Award, NSF Packaging Research Center, in 1997 and 1998. He served as the Technical Program Chair of the IMAPS 2nd International Advanced Technology Workshop on Flip Chip Technology and the General Chair of the IMAPS 3rd and 4th International Advanced Technology Workshops on Flip Chip Technology.

Jianmin Qu received the B.S. degree in mathematics from Jilin University, China, and the M.S. and Ph.D. degrees in theoretical and applied mechanics from Northwestern University, Evanston, IL.

He is an Associate Professor in the School of Mechanical Engineering, Georgia Institute of Technology, Atlanta. He has published over 100 papers in these areas. His research interests include micromechanics of composite materials, interface mechanics, thermomechanical reliability of microelectronic packaging, and ultrasonic nondestructive evaluation and characterization.

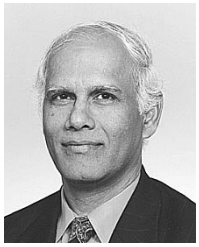


Suresh K. Sitaraman is an Assistant Professor in the School of Mechanical Engineering, the Georgia Institute of Technology (Georgia Tech), Atlanta. Prior to joining Georgia Tech in 1995, he was a Senior Scientist at the IBM Corporation. His expertise is in the area of thermo-mechanical modeling, reliability, and design of electronic packages. At Georgia Tech, he manages a number of federal and private industry research grants and contracts totaling more than $2M. He guides a group of post-doctoral, doctoral, master's, and undergraduate students, and has published more than 40 scholarly papers in journals and conferences. He co-leads the Reliability Thrust at the Packaging Research Center and directs the Computer-Aided Simulation of Packaging Reliability (CASPaR) Lab. He is also a member of the MARC/Center for Board Assembly Research and a member of Materials Research Council.

Dr. Sitaraman received the Metro-Atlanta Engineer of the Year in Education Award in 1999, Outstanding Faculty Education Award from the Packaging Research Center in 1998, and the NSF-CAREER Award in 1997. He also received the outstanding research award from the College of Engineering Graduate Council at The Ohio State University for his doctoral work. He was a Symposium Chair in the ASME International Mechanical Engineering Congress and Exposition (IMECE) 1997, was a Technical Chair of IMAPS Packaging Design Workshop 1997, has organized and chaired sessions in ASME-IMECE 1997 and 1998, ECTC 1997, 1998, and 1999 and ITHERM 1998, and is on the Program Committee for ECTC and ITHERM conferences. He also serves as the IMAPS-GT Student Chapter Advisor.

Madhavan Swaminathan (A'91–M'95–SM'98), photograph and biography not available at the time of publication.

C. P. Wong (F'92), for a photograph and biography, see this issue, p. 254.



Rao Tummala (F'94) received the B.E. degree in metallurgical engineering from the Indian Institute of Science, Bangalore, India, and the Ph.D. degree in materials science and engineering from the University of Illinois, Urbana.

He is an Endowed Chair Professor in Electrical and Computer Engineering and Materials Science and Engineering at the Georgia Institute of Technology (Georgia Tech), Atlanta. He is also the Director of the Packaging Research Center funded by NSF (as one of its Engineering Research Centers), the state of Georgia, and the electronics industry. He is also an Eminent scholar for the state of Georgia. Prior to joining Georgia Tech, he was an IBM Fellow at the IBM Corporation, where he invented a number of major technologies for IBM's products for displaying, printing, and magnetic storage. He teaches both graduate and undergraduate system level courses in microelectronic packaging, advises Ph.D., M.S., and B.S. students and is writing and editing the first undergraduate book. He has published 160 technical papers and holds 66 U.S. patents and inventions.

Dr. Tummala received the David Sarnoff Award, the Technical Achievement Award from IEEE, the John Wagnon's Award from IMAPS, the Materials Engineering Achievements Award from ASM-I, both the Arthur Friedberg Memorial and the John Jeppson Awards from American Ceramic Society, the Total Excellence in Electronics Manufacturing (TEEM) Award from the Society of Manufacturing Engineers, the European Materials Award from DVM, the Distinguished Alumni Award from the University of Illinois and Distinguished Alumni from Indian Institute of Science, Bangalore, India, the highest faculty award at Georgia Tech, was recently named by Industry Week as one of the 50 stars in the U.S. for improving U.S. competitiveness, and invented the industry's first multichip packaging for which he received 16 technical, outstanding, and corporate awards from IBM. He is a Fellow of the American Ceramic Society, a member of the National Academy of Engineering, 1996 President and current International Vice President of IMAPS, and 2000–2002 President and member of the Board of Governors for the IEEE-CPMT Society. He is co-editor of the widely used *Microelectronics Packaging Handbooks*.