Parameter Extraction and Electrical Characterization of High Density Connector Using Time Domain Measurements

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Abstract—This paper discusses the parameter extraction and electrical characterization of a high density connector system using time domain measurements. Two coupled connector pins can be represented by an equivalent circuit consisting of six parameters, namely, self capacitance/self inductance per pin, mutual capacitance between pins and mutual inductance between pins. A systematic parameter extraction algorithm has been discussed in this paper using time domain reflectometry (TDR) measurements. This method uses a combination of stand-alone, common mode, and differential mode measurements to extract the connector parasitics. The accuracy of the equivalent circuit has been studied in detail using cross talk measurements.

Index Terms—Common mode, connector, cross talk, differential mode, lumped equivalent circuit, time domain measurements.

I. INTRODUCTION

CONNECTORS play a critical role in high speed digital systems due to the large bandwidth and high density interface required between boards/cards. Due to high speed signal propagation on these connectors, electrical design issues such as signal integrity, delay, cross talk, and operating bandwidth are important. To study these effects development of accurate equivalent circuits are necessary that are compatible with existing SPICE simulators. Two methods are currently available for extracting the electrical parameters of connectors—use of electromagnetic field solvers that extract parameters from the physical structure by solving Maxwell’s equations and extraction of parameters directly from measurements. The problem with using EM solvers directly on the connector pins studied in this paper are two fold namely:

1) Complex shape of the connector pins (Fig. 1) and its nonhomogenous surrounding, requiring some form of approximation during modeling.

2) Non-inclusion of discontinuities associated with pads, contacts and fanout that arise when the pins are included as part of a package.

An alternative method is to use time or frequency domain measurements. Since the connector pins discussed in this paper are being targeted for digital applications, the choice was to use time domain measurements.

For electrically short structures, a lumped element equivalent circuit is preferred since it can be easily integrated into a SPICE model. This form of representation is largely dependent on the bandwidth of the operation. In [1], the layer-peeling algorithm has been used to extract the inductance \( L \) and capacitance \( C \) matrix using TDR measurements. Both the \( L \) and \( C \) matrices were extracted using a combination of stand alone, common mode, and differential mode measurements. Though this produces good results for \( C \), the \( L \) matrix can be inaccurate, depending on the type of calibration used. Hence the open measurement has to be combined with a short measurement to obtain the desired accuracy. This paper uses a through measurement to extract the \( L \) and \( C \) matrices of the connector, which is less prone to errors. The accuracy of the models has been correlated with both near end and far end cross talk measurements. Measurements on the bare board have been used for calibration and reference to generate the required SPICE deck. It is important to note that a through measurement to extract the \( L \) and \( C \) matrices of the connector, which is less prone to errors. The accuracy of the models has been correlated with both near end and far end cross talk measurements. Measurements on the bare board have been used for calibration and reference to generate the required SPICE deck. It is important to note that a through measurement to extract the \( L \) and \( C \) matrices of the connector, which is less prone to errors. The accuracy of the models has been correlated with both near end and far end cross talk measurements. Measurements on the bare board have been used for calibration and reference to generate the required SPICE deck. It is important to note that a through measurement to extract the \( L \) and \( C \) matrices of the connector, which is less prone to errors. The accuracy of the models has been correlated with both near end and far end cross talk measurements. Measurements on the bare board have been used for calibration and reference to generate the required SPICE deck.

SPICE models have been developed for SIPAC connectors using lumped values of resistors, capacitors, and coupled inductors in [2]. The model in [2] was extracted using an electromagnetic (EM) solver, which was optimized to fit the measurements. This can be time consuming and requires access to an EM solver, which can accurately model the required structures.
This paper discusses the parameter extraction and characterization of a high density connector as described in [3]. Extensive TDR measurements have been used to extract the equivalent circuit of the connector pins using a systematic extraction algorithm. The accuracy of the model developed has been studied using cross talk measurements. The extraction algorithm led to the development of equivalent circuits that generated cross talk (both near end and far end) results (with appropriate waveform shape) that were within 5–10% of the measured results, indicating that the method is well suited for extracting the equivalent circuits of high density connectors. The usefulness of this method is that all discontinuities associated with pin contacts, fan out on the printed circuit board (PCB) and pin pads are included in the extracted equivalent circuit, which therefore provides a true picture of the pin performance.

II. HIGH DENSITY CONNECTOR

The high-density connector system [3], [4] studied in this paper consists of 38 groups of four pins, totaling 152, in 2.5 in of linear space. Each group of pins uses a four-sided insulator post with a contact on each side. The four contacts are spaced in a north (n), south (s), east (e), and west (W) arrangement as shown in Fig. 1. The male connector is a rigid straight beam whereas the female pin is a complaint leaf style contact. The female pins are inserted over the male pins to form the mated connector contact. As shown in the figure, the shape of the male and female connector pins makes it difficult to extract the electrical parameters directly from the physical structure using EM solvers.

III. TIME DOMAIN MEASUREMENTS

Time domain measurement is a useful technique for analyzing the pulse propagation on interconnects in digital systems. A typical setup consists of a digital sampling oscilloscope with sampling heads to generate, propagate and receive waveforms. The interface between the cables connected to the sampling heads and the device under test (DUT) can be SMA connectors or probes. Time domain reflectometry (TDR) represents the time signature of the reflected waveform while time domain transmission (TDT) is the time signature of the propagated waveform.

The experimental setup used in this paper is shown in Fig. 2. It consists of SMA connectors mounted on a specially designed board with transmission lines connected to connector pins, as shown in Fig. 2(a). Printed circuit boards PCB_1 and PCB_2 housed the male and female connectors, respectively. A Tektronix 11801B digital sampling oscilloscope with 20 GHz sampling heads, each containing two channels was used. The two channels allowed for common mode and differential mode measurements which forms a critical part of the extraction process. SMA connectors were used to launch the signal with a voltage swing of 250 mV and rise time of 35 ps. A photograph of the complete setup is shown in Fig. 2(b). The time signature of the TDR waveform for a pulse propagating on the transmission line attached to a single pin is shown in Fig. 3. Based on the experimental setup, the pulse generated by the sampling head propagates through a coaxial cable, through the SMA connector, through the transmission line on the printed circuit board (PCB_1), through the mated connector and reaches the far end of PCB_2 where it gets reflected or absorbed based on the nature of the termination. Along its path, portions of the pulse get reflected based on the nature of the discontinuity. These reflections are captured at the near end and provides a signature of the interconnect system. Due to the board design, the response due to the various elements of the system are separated in time, which allows for the individual analysis of various parts of the system. Since a one-to-one correspondence exists between the measured waveform and the physical connectivity of the system, time windowing techniques have been used to study the individual parts of the system.

IV. BOARD DESIGN

As mentioned earlier, the board design represents the most important part that enables the extraction process. On boards PCB_1 and PCB_2, the embedded transmission lines were designed to have a characteristic impedance of 50 Ω to match the oscilloscope output impedance. To achieve this design goal, both PCB’s contained a layer of interconnect
above a ground plane with adequate cross-section, as shown in Fig. 4(b). The transmission lines and ground planes were connected to the connector pins using the necessary fanout on the interconnection layer, as shown in Fig. 4(a). This allowed for the inclusion of the fanout (which could be a critical parameter) and variation in the proximity of the ground pin (signal:ground ratio) in the extraction process. For adjacent interconnects, the transmission lines were adequately decoupled (20 mils spacing) to minimize coupling. This was to ensure that any cross talk measured was due to the coupling between connector pins and not due to the coupling between transmission lines. SMA connectors were mounted on the PCB to connect to the transmission lines and high speed 50 Ω cables for TDR and TDT measurements. Two kinds of pin assignments were used to extract the equivalent circuit, as shown in Fig. 5, which accounts for varying signal:ground ratios and their effect on the pin parameters.

A SPICE model for the bare board was initially constructed using the electrical parameters extracted directly from the TDR measurements on the bare board, as follows.

- Cable: \( Z_0 = 49.60 \, \Omega \); Round trip delay = 4.25 ns;
- SMA: \( Z_0 = 72.79 \, \Omega \); Round trip delay = 70 ps (positive spike);
- SMA: \( Z_0 = 20.13 \, \Omega \); Round trip delay = 56 ps (negative spike);
- PCB_1: \( Z_0 = 52.04 \, \Omega \); Round trip delay = 600 ps;
- PCB_2: \( Z_0 = 53.04 \, \Omega \); Round trip delay = 600 ps.

A cascaded transmission line model was used to represent the SMA connector. From Fig. 2, since two 50 Ω transmission lines were used on either side to connect to the connector pins, the response of the pins could be easily truncated from the waveform in Fig. 3 using time windowing as shown in Fig. 6. This represents a more robust design as compared to [1] wherein the far end of the pin was open-ended resulting in voltage doubling at the pin location.

V. THEORY

The extraction of the electrical parameters is based on the coupled mode approach wherein any complicated coupled system can be divided up into a number of isolated parts or elements. These elements can then be represented using circuit elements such as capacitors, inductors, resistors and transmission lines that are used to describe the passive behavior. The original complex coupled system is then assumed to be made up of these isolated elements weakly coupled to each other. The coupling that exists within the original complex system is reflected by the mutual inductance and mutual capacitance parameters between the individual isolated components. If this is not a valid approximation, the solutions
of the coupled system will be sufficiently different from the
uncoupled solutions and hence knowledge of the solutions for
the isolated elements will not be useful. This paper assumes
that the sub-elements are weakly coupled to each other, which
has been validated through cross-talk measurements. The
equivalent circuit for the connector can either be represented
as transmission lines (with associated impedances and delays)
or lumped elements (inductance/capacitance). A magnified
waveform in the vicinity of a connector pin is shown in Fig. 6
which indicates a capacitive discontinuity followed by an
inductive discontinuity with no distributed effects. Hence the
parameter extraction algorithm discussed in this paper assumes
lumped elements for generating the equivalent circuit.

Consider a continuous TDR waveform as shown in Fig. 6
which represents a time window of the waveform shown in
Fig. 3. Using the waveform in Fig. 6, the inductance and
capacitance of the connector pins can be computed as [5]

\[
L = \frac{1}{2} \int_{t_{1}}^{t_{2}} Z_0(t) \, dt \quad C = \frac{1}{2} \int_{t_{1}}^{t_{2}} \frac{1}{Z_0(t)} \, dt
\]

where \( Z_0(t) \) is the time variation of the characteristic
impedance, \( t_{1} \) and \( t_{2} \) are the time instants corresponding
to the time window of positive glitch, \( t_{c1} \) and \( t_{c2} \) correspond
to the negative glitch. The factor 1/2 is due to the round
trip delay. Since the digital sampling oscilloscope provides
sampled time intervals, (1) can be rewritten as

\[
L = \frac{1}{2} \sum_{i=1}^{n} Z_{0i} T_{0i} \quad C = \frac{1}{2} \sum_{i=1}^{n} \frac{Z_{0i}}{T_{0i}}
\]

where \( Z_{0i} \) is the characteristic impedance corresponding to
the \( i \)th sampling instant \( T_{0i} \) and \( n \) is the number of samples.

Equations (1) and (2) are largely dependent on the time
window and can lead to inaccurate results if they are not
coupled to a SPICE simulation. In this paper, (1) and (2) have
only been used as an initial guess with emphasis placed on the
SPICE simulation to obtain the necessary accuracy.

VI. EXTRACTION OF ELECTRICAL PARAMETERS

A. Bare Board Measurement

The first step in the extraction of the connector parameters
is the characterization of the bare board to facilitate the
representation of the bare board using an equivalent circuit.
This provides a reference waveform for the extraction process.
TDR measurements on the bare board were used to develop an
equivalent circuit. This step is fairly straightforward since the
parameters of the board are known \textit{a priori} based on the design
and hence only minor tweaking of these parameters using the
TDR measurements is necessary. The equivalent circuit for the
bare board (male and female) is shown in Fig. 7. This data was
used to represent the bare board using a SPICE model.

B. Stand-Alone Measurement

The two boards were next mated by inserting the male
pins into the female pins, as shown in Fig. 2. Consider the
assignments in Fig. 5(a), which consists of signal pins 4, 3 and
two grounds. Pulses (low to high transition) were propagated
onto pins 4 and 3 individually through the transmission
lines on the PCB which resulted in the responses shown in
Figs. 8(a) and 9(a) respectively. An initial guess using (2)
was used, where the truncated waveform corresponding to
the connector pins was numerically integrated to compute \( L \)
and \( C \), which was further tuned to obtain good correlation
between the measured and simulated waveforms, as shown in
Figs. 8(a) and 9(a). No calibration was necessary, because of
the separation of the connector through 50 \( \Omega \) lines. The slight
mismatch between the simulated and measured waveforms at
the far end can be attributed to the noninclusion of skin effect
for the PCB interconnection in the SPICE model which did
not produce any error. An alternative method is to use the
peeling algorithm in [5].

Based on the waveforms in Figs. 8(a) and 9(a), the self
capacitances and self inductances for the pins were extracted
to be 10.3 nH, 1.25 pF for pin 4 and 6.5 nH, 1.15 pF for pin 3.
The equivalent circuit for the individual pins (self inductance and self capacitance) are shown in Figs. 8(b) and 9(b). As is apparent from the figure, pin 4 has larger inductance than pin 3, indicating that the loop inductance is largely dependent on the position of the ground.

C. Even Mode Excitation

This represents the propagation of identical pulses (both low-high transitions) on pins 3 and 4. Assuming a mutual capacitance exists between the pins, the two identical pulses on the pins will cancel the effect of the mutual capacitance, as shown in Fig. 10, provided the pulses propagate on the connector pins at the same time instant. Hence control of the transmission line lengths on the PCB is critical for this measurement. To simplify the even mode excitation, delay lines can be used. A 100 ps variable delay available on the Tek 11801B was used for balancing the line lengths in this paper.

Any change in the time domain response for even mode excitation as compared to Figs. 8(a) and 9(a) is due to the mutual inductance between the pins. This is apparent by comparing Figs. 8(a), 11(a) for pin 4, where the negative dip (capacitive) does not vary while the positive peak (inductive) changes by a large amount. The mutual inductance between the pins was varied to fit the simulation with the measured waveform. It is important to note that the mutual inductance is the only parameter to be varied in this step. Based on waveform in Fig. 11(a) the mutual inductance was computed to be 3.27 nH which was incorporated into the equivalent circuit, as shown in Fig. 11(b). In [1] four channels were used to provide appropriate isolation between adjacent pins. This was considered unnecessary in this paper due to the small mutual capacitance that was expected between adjacent pins.

D. Odd Mode Excitation

This represents the propagation of identical pulses of opposite polarity (one low-high and the other high-low transition)
Fig. 11. (a) Pin 3: Response due to even mode excitation. (b) Equivalent circuit.

Fig. 12. Even mode excitation.

Fig. 13. (a) Pin 3: Response due to odd mode excitation. (b) Equivalent circuit.

TABLE I

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<tr>
<th>CONNECTOR PARAMETERS</th>
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is for the pulses to propagate on the two pins at the same time instant. The mutual capacitance between the pins was computed to be 0.125 pF, as shown in the equivalent circuit in Fig. 13(b).

The procedure developed for extracting the pin parameters for pins 3 and 4 were repeated for pins 5 and 6 shown in Fig. 3(b). The extracted pin parameters for both cases (a) and (b) have been tabulated in Table I. These values of the self-inductance, self-capacitance, mutual-inductance and mutual capacitance were incorporated into the SPICE circuit in Fig. 7 to obtain the equivalent SPICE circuit for the entire system.
VII. MODEL VALIDATION USING CROSS TALK

As indicated earlier, since the PCB transmission lines were de-coupled by design, the measured cross talk was due to the coupling between the adjacent connector pins. However, based on the measurements of the bare board, 3 mV of peak near end cross talk was observed between adjacent transmission lines for pins 3 and 4 in Fig. 5 which could account for a ~3 mV drop in the peak noise simulated. It is important to note that cross talk is a function of the rise time, with a larger cross talk for faster rise time signals. For the near end cross talk measurements between pins 3 and 4, a pulse (low to high transition) was propagated on pin 4 and the noise waveform measured at the near end of pin 3 on PCB 1 (Fig. 2). The far end of both the pins were left unterminated to allow for the reflection of the pulses. The measured near end noise waveform is shown in Fig. 14 along with the SPICE simulation of the model developed in Section VI for pins 4 and 3. As can be seen from the waveforms, the simulated waveform shape is in good agreement with the measured waveform and validates the model developed. The small discrepancy of ~6 mV at the first positive peak level can be attributed to the noise between the adjacent transmission lines, as explained earlier. However, the difference of ~6 mV between the simulated and measured waveforms (first negative peak) can be attributed to the non-inclusion of losses in spice to model the reflection level accurately. In Fig. 14, the appropriate waveform shape has been captured by accounting for all discontinuities.

Using the model developed in Section VI and the parameters in Table I, the peak noise generated by the models can be further confirmed by using analytical expressions for cross talk developed in [6] and discussed in [7]. These expressions represent simplistic models that do not have the accuracy of a SPICE simulation but are useful for comparing with measured results. The underlying assumption in the derivation is that the noise coupled on adjacent pin due to mutual inductive and capacitive components are independent of each other and can be added in phase to obtain the total noise on the quiet pin. Since the ratio of $L_{34}/L_3 \sim 0.3$ and $C_{34}/C_3 \sim 0.1$, simplified cross talk equations for loosely coupled systems and homogenous medium have been used. It is shown through calculations that the values obtained match the measurements closely, which justifies our assumption of loosely coupled system to obtain the approximate values. The ~50 Ω lines on either side of the connector pins (Fig. 7) have enough delay so as to avoid the reflections from the unterminated ends to affect the peak values of the near end and far end noise in time. Hence the approximate peak values have been calculated for the matched case.

Since high speed signals propagate through the connector pins, a figure of merit for pulse propagation is the degradation in the rise time of the pulse and the additional delay penalty due to the connector. A 35 ps rise time pulse was propagated through the bare board only, shown as PCB_1 in Fig. 2 and the rise time was measured between the 10% and 90% levels at the far end. The measured values of rise time were in the range of 240–300 ps. Any increase in rise time beyond 35 ps represents rise time degradation and can be attributed to the PCB, connector and any other discontinuities in the system. A SPICE model was generated and simulated with and without the pins to calculate the delay of the connector which is 140 ps (signal surrounded by ground), measured between 50 Ω levels. Connector delay and rise time along with the mutual inductance and capacitance can be used to calculate the near end and far end cross talk.

Near end noise on pin 4 due to the voltage on pin 3 is given by

$$V_{\text{NE}}(t) = \frac{1}{4T_d} \left( \frac{L_m}{Z_0} + C_m Z_0 \right) \left[ V_{\text{in}}(t) - V_{\text{in}}(t - 2T_d) \right].$$  \hspace{1cm} (3)

Where $T_d$ is the connector delay, $L_m$ is the mutual inductance between pins 3 and 4, $C_m$ is the corresponding mutual capacitance, $V_{\text{in}}$ is the input voltage swing (250 mV), $Z_0$ is the impedance of the transmission line. Using $T_d = 140$ ps, $L_m = 3.27$ nH, $C_m = 0.125$ pf, $Z_0 = 50$ Ω and $V_{\text{in}} = 250$ mV, the peak value of the far end noise is 31.98 mV. This value of peak near end noise is within 10% of the measured value of 30.2 mV.

The peak reflected voltage due to the inductance and capacitance on the active pin (pin 3) can be written as [8]

$$V_{\text{fl}} = \frac{L_3 V_{\text{in}}}{2Z_0 T_r}, \quad V_{\text{fr}} = \frac{C_3 V_{\text{in}} Z_0}{2T_r}$$  \hspace{1cm} (4)

where $L_3$ is the inductance, $C_3$ is the capacitance of pin 3, $T_r$ is the rise time. Equation (4) is valid for small inductive/small capacitive reactances, large rise time values and resulted in a rise time of 290 ps for $V_{\text{fl}} = 88.7$ mV and $V_{\text{fr}} = 26.9$ mV.

With this value of rise time, the far end cross talk is calculated to be 25.49 mV using (5) compared to the measured value of 24.1 mV

$$V_{\text{FE}}(t) = \frac{1}{2} \left( C_m Z_0 - \frac{L_m}{Z_0} \right) \frac{d}{dt} [V_{\text{in}}(t - T_d)].$$  \hspace{1cm} (5)

For pin combination 5 and 6, the calculated value of near end...
noise was 15.61 mV as compared to a measured value of 15.9 mV. The calculated far end noise was 10.775 mV, whereas the measured value was 16.1 mV. This discrepancy was due to the coupling between the transmission lines on the PCB for this configuration. Noise coupled into the transmission lines on the bare board corresponding to pins 5 and 6 was measured to be ~6 mV, where as the corresponding value for pins 3 and 4 was ~1.5 mV, which explains the increased error. The peak near end, peak far end cross talk measured for the configurations in Fig. 5 are tabulated in Table II along with the results from the SPICE simulation and analytical expressions. The peak cross talk measured was 12.1% of the input voltage swing for the worst case configuration shown in Fig. 5(a).

VIII. CONCLUSION

A high density connector with complex shape in a nonhomogeneous surrounding was characterized using TDR and TDT measurements. A robust method for extracting the equivalent lumped element model for the connector was discussed. The simulation of the equivalent model using SPICE shows good agreement with the measurements indicating the accuracy of the method. Extensive cross talk measurements were used to validate the technique developed.

REFERENCES