Modeling of Simultaneous Switching Noise in High Speed Systems

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Abstract—Simultaneous switching noise (SSN) has become a major bottleneck in high speed digital design. For future systems, modeling SSN can be complex due to the thousands of interconnects that need to be analyzed. This is because a system level modeling approach is necessary that combines the chip, package and board level interactions. This paper presents an efficient method to model the SSN for high speed systems by developing circuit models for the planes and interconnections that can be combined using superposition theory. This approximation is valid at frequencies where skin effect is dominant. Simulation results are compared with the measurements on a test vehicle, verifying the validity of the method. In addition a system has been simulated to compute SSN, showing the application of this method for complex systems.

Index Terms—Plane bounce, plane modeling, power distribution system, resonator model, return current, simultaneous switching noise.

I. INTRODUCTION

CURRENT complementary metal oxide semiconductor (CMOS) microprocessors and application-specific integrated circuits (ASICs) have hundreds of inputs/outputs (IOs) switching within one cycle time. When the noise produced by all the simultaneous switching circuits approaches the noise tolerance of a static CMOS circuit, the integrity of the output signal is degraded [1]. Therefore proper prediction of the level of SSN in a packaged electronics system has become one of the most important issues in high frequency digital design. As electronic packaging has progressed from traditional lead frame packages to packages that have power and ground planes, the SSN problem has shifted from a lead frame inductance problem to a power plane inductance problem. In addition, the planes could become very important in high speed systems for computing the fluctuations on the chip power supply. This approach is valid when SSN is dominated by the vertical inductance in the power distribution network. However, this modeling method can give erroneous results in future systems since it does not capture the distributed effects associated with planes. In [5], a birthday cake approach has been used to model SSN. This method models the vertical inductances and does not account for the reflection of the electromagnetic wave from the plane edges. Other approaches such as the one used in [6] model a quadrant of a chip which once again neglects the reflection from the plane edges. The rationale behind this paper is to demonstrate an efficient method for modeling SSN that captures the reflection of the electromagnetic wave from the plane edges. This effect could become very important in high speed systems for computing the fluctuations on the chip power supply.

In [3], methods have been demonstrated to extract circuit models for planes and for simulating core noise. This paper is an extension of [3] where an approach has been presented for modeling SSN produced by output drivers driving transmission lines in a multilayered board or package. This modeling approach has been validated through measurements on an active board.

This paper discusses the following.
1) Extraction of circuit models for solid plane pairs behaving as cavity resonators.
2) Demonstration of an approach that enables the stacking of planes and interconnections under the assumption of no field penetration.
3) Validity of the skin effect approximation.
4) Connection of nonlinear driver models to the circuit models in Spice for simulation of the waveforms and correlation with measurements.
5) Demonstration and explanation of the propagation of energy into the lower layers even though the plane pairs are isolated through skin effect.

The approach discussed in this paper has been used to model a system containing packages on a printed circuit board, demonstrating the application of this method.

II. EXTRACTION OF CIRCUIT MODELS FOR PLANES

Fig. 1 shows the structure of a plane pair which consists of two planes of dimensions axb, separated by a dielectric of thickness “d” and permittivity “ε.” With the assumption that a, b ≫ d where d ≪ λ (the wavelength) which is true in all electronic packages including single chip and multichip modules, the impedance matrix Z at port locations on the plane can be derived as [3]

\[ Z_{ij}(\omega) = j\omega \mu d \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{\varepsilon n \varepsilon m}{(k_{mn}^2 - k^2) \alpha \beta} f(x_i, y_i, x_j, y_j) \]  

where

\[ f(x_i, y_i, x_j, y_j) = \left( \cos \frac{m \pi x_i}{a} \sin \frac{n \pi t_{xi}}{2a} \right) \left( \cos \frac{n \pi y_i}{b} \sin \frac{m \pi t_{yi}}{2b} \right) \left( \cos \frac{m \pi x_j}{a} \sin \frac{n \pi t_{xj}}{2a} \right) \left( \cos \frac{n \pi y_j}{b} \sin \frac{m \pi t_{yj}}{2b} \right). \]

In (1), (x_i, y_i) and (x_j, y_j) are the coordinates of the port locations, (t_{xi}, t_{yi}) and (t_{xj}, t_yj) are the dimensions of the ports with k_{mn}^2 = (m \pi/a)^2 + (n \pi/b)^2 where m, n are the propagating modes on the planes. The loss is included as a perturbation with the wavenumber k given by k = k' - jk'' where k' = \omega_0 \sqrt{\varepsilon \mu} and k'' = \omega_0 \sqrt{\varepsilon \mu} (\tan \delta + \gamma/\omega) where \delta is the loss angle of the dielectric material and “γ” is the skin depth for the conductors used in the circuit.

In [3], [7], a method has been presented to linearize (1). This results in the impedance equation

\[ Z_{ij}(\omega) = \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{N_{mm} N_{mnj}}{j\omega C_{mm} + \frac{1}{j\omega L_{mn}} + G_{mn}}. \]  

Under the assumption, k' ≫ k'', the C, L and G parameters can be extracted as

\[ C_{mn} = \frac{\varepsilon ab}{d} \]

\[ L_{mn} = \frac{d}{\varepsilonabr(2\pi f_{mn})^2} \]

\[ G_{mn} = \frac{2\pi f_{mn} C_{mn}}{Q_{mn}} \]

\[ N_{mmi} = \frac{\varepsilon m e_n \cos \frac{m \pi x_i}{a} \sin \frac{n \pi t_{xi}}{2a}}{\sin \frac{n \pi t_{yi}}{b}} \]
\[ N_{mnj} = \frac{\varepsilon m e_n \cos \frac{m \pi x_i}{a} \sin \frac{n \pi t_{xj}}{2a}}{\sin \frac{n \pi t_{yj}}{b}} \]

\[ f_{mn} = \frac{\sqrt{(m/a)^2 + (n/b)^2}}{2\sqrt{\varepsilon \mu}} \]
\[ Q_{mn} = \frac{d \sqrt{\pi f_{mn} \sigma}}{1 + d \tan \delta \sqrt{\pi f_{mn} \sigma}} \]

where f_{mn} is the resonance frequency of the structure and Q_{mn} is the quality factor which contains the loss in the structure.

Equation (2) is a linear representation of the nonlinear problem described in (1). The linearity in the variable ‘s = jk’ has been obtained by assuming that the losses can be described by a tank circuit at resonance. This assumption is a very good approximation, the validity of which has been demonstrated through experiments in [3].

This model is based on waveguide theory for the planes where the circuit characteristics in the vicinity of a resonant frequency can be expressed in terms of C, L and G parameters. Since the planes act as cavity resonators, the capacitor “C” is used for storage of electric energy and the inductor “L” for storage of magnetic energy, whereby at the resonant frequency, there is an exchange of energy between the two elements. The conductance “G” is used to account for the losses in the circuit. Here, with m = n = 0, the tank circuit is reduced to C0 which corresponds to the charging and discharging of the static capacitance of the planes. This mode can be called as the zero-frequency resonant mode or electrostatic mode. Thus C0 represents the electrostatic capacitance of the structure. The information on the “port” is captured by N_{mmi} and N_{mnj} which are the ideal transformer turn ratio for the port i and j respectively.

The equivalent circuit for (2) can be implemented by using parallel resonant circuits and ideal transformers as shown in Fig. 2. The transformers are defined using the turn ratio ‘N_{mmi}’ and ‘N_{mnj}’ in (2). These transformers are used to couple energy between ports. By connecting further external ports in parallel across the resonant circuit, the equivalent circuit for the multiport structure can be represented as shown in Fig. 2. The equivalent circuit in Fig. 2 can be used to model the plane-pair as a waveguide coupled to the various natural modes of the resonators through transformers. The transformers in series at any port is used to sum the voltages produced by the resonator circuit. The frequency of oscillation is defined by each resonator and the corresponding amplitude is accounted for by the transformer turn ratio. Hence, Fig. 2 is equivalent to a circuit for summing the various fourier components of a transient signal. The accuracy of this model has been verified in [3], through TDR/TDT.
measurements. In addition, methods have been described in [3] to construct compact model representation of the planes.

The primary difference between the circuit described in [3] and Fig. 2 is the inclusion of the static mode using transformers with turn ratios \( N_{00i} = 1 \) and \( N_{00j} = 1 \). This is extremely important since it enables the voltage at every node on the plane to vary with time and allows for the stacking of plane pairs. It is also important to note that the circuit is stable and passive.

III. STACKING OF PLANES

In this section, a method is described that enables the stacking of planes for a multilayered structure. Once the plane models are constructed, the interconnections and driver models can be connected to the planes using superposition, which has been explained in the next section. This method therefore combines electromagnetic theory with network theory to capture the ground bounce phenomena that occurs when output drivers switch simultaneously.

The stacking of planes is based on a skin effect approximation, which has been described in [3]. As an example, the skin depth for copper as a function of frequency is shown in Fig. 3. As can be seen from the figure, the skin depth decreases as the frequency increases, with a depth of 2.1 \( \mu \text{m} \) at 1 GHz. As has been discussed in [8], [9], the waves that propagate between planes induce current densities on the planes that decay exponentially as they penetrate through the conductor. If the plane thickness ‘\( t \)' is larger than 3\( \gamma \), where \( \gamma \) is the skin depth, the plane layers can be completely decoupled by assuming small magnetic field penetration through the planes. In addition, magnetic field penetration is a steady state effect that becomes dominant after many cycles for thin metallization layers. For thin metal layers, the maximum field penetration through the conductor occurs when the planes resonate, as described in [9]. This effect can be safely ignored if the thickness of the conductor is large compared to the skin depth at resonance and for transient simulations where the window of interest is around the rise time of the pulse.

Since SSN is a phenomenon occurring due to the transient switching of the drivers, the rise time is the parameter that has been used to evaluate the validity of the skin effect approximation. For the test vehicle used in this paper, the rise time \( tr = 12 \) ns. Using \( f_{3dB} = 0.35/tr \) which corresponds to the 3 dB frequency, the corresponding skin depth is 12.237 \( \mu \text{m} \) at \( f = 29.167 \text{ MHz} \). Since the copper thickness used was \( t = 35 \mu \text{m} \), which is \( \approx 3\gamma \), the skin effect approximation is valid. Based on this approximation, the plane layers and interconnection layers can be decoupled and stacked using superposition. In high speed systems with very fast rise times, the skin effect approximation will be increasingly valid for thick conductors.

It is important to understand the flow of charge at a port where a via makes contact to a plane. For a good conductor, the electric field across the two surfaces of the conductor has to be zero. This is equivalent to having an instantaneous flow of charge through the plane cross-section where a via makes contact to the plane surface. Hence, based on this assumption, for the plane structure in Fig. 4(a), an equivalent circuit as shown in Fig. 4(b) can be constructed where a short-circuit has been used to connect the two plane surfaces at any port. In Fig. 4(b), the inductance of the via has been ignored, which can be included if necessary. This model can be readily extended to many layers.

In [3], (1) was used to compute the response of a multilayered plane structure under the assumption that skin effect was dominant. The results were correlated with the coupled transmission line model (CTL) described in [10]. In this paper, since (1) has been linearized to (2) for constructing an equivalent circuit, the circuit model in Fig. 4(b) has been compared with [10] to verify accuracy.

The test structure consists of 3 planes with dimensions of 4 in × 6 in as shown in Fig. 5. The separation between the power plane and the local ground plane is 62 mils with a relative dielectric constant \( \varepsilon_r = 2.5 \), and the separation between the local ground plane and the global ground plane is 200 mils with a relative dielectric constant \( \varepsilon_r = 1 \). Ports 1 and 2 are located at \( (x = 1 \text{ in}, y = 3 \text{ in}) \) and \( (x = 5 \text{ in}, y = 1 \text{ in}) \), respectively, on the power
plane. Ports 3 and 4 are located at \((x = 1\, \text{in}, y = 1\, \text{in})\) and \((x = 5\, \text{in}, y = 3\, \text{in})\), respectively, on the local ground plane. Using the equivalent circuit in Fig. 4(b), and assuming two virtual ports on the local ground plane beneath port 1 and port 2 [3], the test structure can be modeled as shown in Fig. 6. The comparison of the results between the model in Fig. 6 and the measurement is shown in Fig. 7(a) and (b), demonstrating the validity of the equivalent circuit in Fig. 4(b). In Fig. 7, the small discrepancy between the results can be attributed to the sensitivity of the measurements and the noninclusion of via effects.

IV. INCORPORATION OF TRANSMISSION LINES

Return currents on planes cause the planes to bounce. When the signal transmission lines are incorporated into the plane models, the return current which occurs on the reference planes for the signal transmission line need to be accounted for, correctly. The reference planes are not perfect and they bounce as return current accumulates and charges the parallel plate capacitance, causing waves to propagate between power and ground planes. In packages containing planes, the return current is on a reference plane that is in close proximity to the signal transmission line. This is because at high speed, the return currents follow the path of least inductance, not the path of least resistance. The lowest inductance return path lies directly under a signal conductor, minimizing the total loop area between the outgoing and returning current paths [11].

To account for the return currents and using the skin effect approximation which is still valid for signal conductors, microstrip and un-symmetric stripline transmission lines can be modeled as in Fig. 8(a) and (b), where the reference for the transmission lines is the closest plane. For a symmetric stripline, a similar approximation can be used by using two transmission lines in parallel, each with twice the impedance, referenced to the top and bottom planes. As shown in Fig. 8(b), the current on the signal trace makes reference to the nearest plane. The model used in Fig. 8(a) and (b) ensures that the magnetic field produced by the signal line is contained between the transmission line and the corresponding plane, which is valid at high frequencies.

Based on the structures in Fig. 8(a) and (b), the only information that is required to incorporate transmission lines into the plane models is a model for the transmission line and the position of the input and output reference ports on the planes.
Fig. 7. (a) Comparison of S13 between result from Fig. 6 (solid line) and result from measurement (*). (b) Comparison of S14 between result from Fig. 6 (solid line) and result from measurement (*).

This can be generated using a 2-D-solver and from the physical layout of the package or board.

V. TEST VEHICLE

A test vehicle was designed and measured to verify the validity of the modeling method. Fig. 9 shows the test vehicle consisting of planes, transmission lines and nonlinear drivers. It is a seven-layered board with interconnects consisting of four very wide microstrip transmission lines with $Z_0 = 22$ Ω. They are about 20 in (50 cm) long and driven by a Texas Instruments ABT244 buffer driver. The power and ground planes are 0.3 in (7.6 mm) wide and similar in length to the transmission lines. The stackup of the test vehicle includes 4 power planes and three signal layers in the order: sig1/Vdd1/Gnd1/sig2/sig3/Vdd2/Gnd2. The separation is 4

Fig. 8. (a) Microstrip configuration. (b) Unsymmetric stripline configuration.

Fig. 9. Test vehicle for SSN measurement.
mils of FR4 material between all copper layers except sig2 and sig3 where the separation is 24 mils. Four silicon drivers are located on the left side of the test vehicle in a 20 pin DIP package. They were powered from Vdd1 and Gnd1 planes, using vias. Two sets of 50 Ω stripline transmission lines were embedded between Gnd1 plane and Vdd2 plane. Layer sig2 is one set of striplines which is closer to the Gnd1 plane and layer sig3 is the other set (designated Strip5, Strip6, Strip7, Strip8), which is closer to the Vdd2 plane. The two power planes and two ground planes were not connected on the left side of the test vehicle, which enables independent voltage measurements between the 4 planes. Both Vdd planes and Gnd planes were connected together on the right side of the test vehicle.

A power supply of 5 v was applied at the right side of the test vehicle to power up the structure and the noise was monitored in the vicinity of the driver, when the drivers transitioned. The measurement was done for two experimental conditions, namely, 1) when the far end of the microstrip transmission lines were open and 2) when the far end of the microstrip transmission lines were terminated to both Vdd and Gnd planes using 43 ohm resistors. The power supply noise measured at the driver was captured using an oscilloscope. The noise voltages measured near the drivers were 1) voltage between Vdd1 and Gnd1 (PP1), 2) voltage between Vdd2 and Gnd1 (PP2), and 3) voltage between Vdd2 and Gnd2 (PP3). The voltage at the far end of the embedded stripline transmission lines was also simulated. These striplines were connected to each of the power planes on the left side of the board to monitor the propagated noise. Strip1 through Strip4 were right below Gnd1 plane and they were connected to each of the power planes on the left side of the board, i.e., Strip1 to Vdd1 plane, Strip2 to Gnd1 plane, Strip3 to Vdd2 plane and Strip4 to Gnd2 plane. Strip5 through Strip8 were right above Vdd2 plane and they were also connected to each of the power planes on the left side of the board, i.e., Strip5 to Vdd1 plane, Strip6 to Gnd1 plane, Strip7 to Vdd2 plane and Strip8 to Gnd2 plane. They were terminated to Gnd planes with 50 ohm resistors on the right side of the board. The purpose of these striplines was to sense the voltage of the power plane on the left side of the board and propagate that signal to the right side of the board. These striplines carry signals with respect to the nearest power plane. The amount of noise coupled to quiet striplines that are referenced to a noisy power plane can be measured using this structure.

As stated in [2], [3], the SSN problem has shifted from an inductance problem to a plane bounce cavity problem. For multilayered structures containing planes, the return current from the transmission lines on the planes contributes significantly to the plane bounce. This effect has been captured in the test vehicle and has been described in later sections.

VI. EXPLANATION OF THE NOISE WAVEFORMS

A. Test Case 1

Consider the waveform in Fig. 10 which was measured when the microstrip transmission lines were unterminated. The noise occurs during the high to low transition of the drivers and very little noise occurs during the low to high transition. This can be explained based on the return currents. When the transition is from low to high, the driver connects the Vdd1 plane to the transmission line through a small resistor $R_{eq1}$ in Fig. 11(a). Current flows into the transmission line and the return current flows on the Vdd1 plane. The current loop is completed through the Vdd1 plane, the driver resistance, the transmission line and the capacitance between the transmission line and the Vdd1 plane as shown in Fig. 11(a). Since the Gnd1 plane is not a part of the current loop, this does not excite any wave between the Vdd1-Gnd1 planes. However, when the transition is from high to low, the driver connects the transmission line to Gnd1 plane through a low impedance path $R_{eq2}$ in Fig. 11(b). Since the transmission line is initially charged to Vdd1 potential, the signal current flows out of the transmission lines through the
driver and into the Gnd1 plane, causing a deposition of positive charge. On the Vdd1 plane, the current leaves the vicinity of the driver as return current, leaving behind negative charge, as shown in Fig. 11(b). This causes the accumulation of charges with opposite polarities on the planes in the vicinity of the driver. Since the charges vary with time, they are equivalent to a displacement current source, as shown in Fig. 11(b). The current source excites a radial wave between the planes that bounces off the edges of the planes, causing the planes to bounce.

B. Test Case 2

Consider the test case when the microstrip transmission lines are terminated with two 43 ohm resistors connected to both Vdd and Gnd planes on the right side of the test vehicle. This results in a different waveform, as shown in Fig. 12. The maximum noise now occurs during the low to high transition instead of the high to low transition. This is due to the initial conditions on the transmission lines. Consider the initial condition when the driver is in the low state. Through the 43 Ω resistors, the current flows from the power supply on the right side of the test vehicle and down the 22 Ω microstrip transmission line. The pull-down device in the driver conducts the current to the local ground where it is returned back to the right side of the test vehicle through the Gnd1 plane, as shown in Fig. 13(a). The Vdd1-Gnd1 planes are charged with the ground current. With these initial conditions, the driver makes a low to high transition. When the pull-down device in the driver becomes high impedance, the initial current loop is opened. The current continues to leave the ground node of the driver, leaving negative charge. Simultaneously the pull-up device connects the Vdd1 plane to the transmission line, causing the deposition of positive charge on the Vdd1 plane near the Vdd node of the driver as shown in Fig. 13(b). The accumulation of charges near the driver acts like a displacement current source, exciting a disturbance between the Vdd1-Gnd1 plane, which causes the planes to bounce. It is important to note that the direction of the current source is opposite to Test case 1. This explains the opposite noise pattern for the two test cases. For the 22 Ω transmission line, since it is already pre-charged, no pull-up device is necessary in the driver for the first several ns. Current coming down the transmission line snaps the driver output high without any aid from the driver. When the transition is from high to low, the phenomenon occurring is similar to Test case 1. Hence, similar noise waveforms are observed.

VII. ENERGY LEAKAGE INTO LOWER LAYERS

Both the measured results in Figs. 10 and 12 show that the noise occurs in the lower plane pairs, namely, Vdd2/Gnd1 and Vdd2/Gnd2 plane pairs. The time of flight along the length of the board is 3–4 ns. The noise on the lower plane pairs occurs immediately when the drivers switch, not one or two time of flight later. This is caused by the static capacitance between the planes. The capacitors behave as a voltage divider circuit causing the instantaneous propagation of energy into the layers below. The propagation of energy into the bottom plane pairs causes the excitation of radial waves, resulting in plane bounce.

In the next section, the simultaneous switching noise was simulated by modeling the power planes and transmission lines using the equivalent circuits described in the earlier sections.

VIII. SPICE CIRCUIT

Based on the discussion in the previous sections, the test vehicle was modeled as shown in Fig. 14. In the figure, only the microstrip transmission lines are shown and the striplines have been excluded for clarity. In the circuit, two extra transmission lines have been added to provide a “dc” path to the drivers for enabling a transient simulation in Spice. These transmission lines also capture an important physical phenomena, without which the noise on the lower layers cannot be computed accurately. To describe its role, consider the microstrip line on the top layer. It
has a plane beneath it and semi-infinite space above. Hence, the microstrip line can be represented as two transmission lines in parallel. The microstrip-plane combination can be modeled as a transmission line with \( Z_0 = 22 \Omega \) and time delay \( td = 3.333 \times \sqrt{\varepsilon_{eff} \times l} \) [ns] where \( \varepsilon_{eff} \) is the effective dielectric constant and \( l \) is the length of the microstrip line in meters. This transmission line is referenced to the plane as described in Fig. 8(a). The microstrip-semi infinite space can be modeled to mimic a microstrip line with the plane at infinity, resulting in a transmission line with \( Z_0 \) large value (100 \( \Omega \)) and time delay \( td = 3.333 \times \sqrt{\varepsilon_r \times l} \) [ns] where \( \varepsilon_r = 1 \) for air and \( l \) is the length of the microstrip line in meters. This transmission line is referenced to ideal ground since potential at infinity is zero (\( V_\infty = 0 \)). In Fig. 14, the input impedance looking into the parallel combination of the two transmission lines is still \( Z_0 = 22 \Omega \), which is the impedance seen by the driver during switching. Similarly, the transmission line beneath the bottom ground plane has been used to mimic the semi-infinite space below the test vehicle. The circuit model in Fig. 14 has been simulated in Spice by attaching nonlinear drivers and compared to measured results in the next section.

**IX. CORRELATION WITH MEASUREMENT**

The equivalent circuit for the test vehicle is shown in Fig. 14, where the number of modes used for the planes was \( n = 8 \) and \( n_1 = 0 \). Since the planes in the test vehicle are very long as compared to their width, the planes behave as one-dimensional transmission lines. Hence the zeroth mode was used for \( n_1 \). Fig. 15 shows the simulation result for the microstrip transmission lines with no termination and Fig. 16 shows the case where the microstrip transmission lines are terminated to both Vdd and Gnd planes on the right side of the test vehicle with 43 \( \Omega \) resistors. The voltage fluctuations across the power supply of the driver is caused by electromagnetic waves reflecting from the edge of the planes. The amplitude of the bounce is a function of the impedance profile of the planes and the frequency spectrum of the driver signal. Simulation results show that the circuit in Fig. 14 captures the power supply bounce on the planes. It is important to note that the driver models were constructed from measurements and contains a small discrepancy in the amplitude of the noise waveforms. It is also important to note that a port specified on a plane pair should be continued through the cross section of the models to capture the effect on the lower layers.

Fig. 17(a), (b) shows the stripline simulation result for no termination. Strip1 to Strip4 make reference to Gnd1 plane while Strip5 to Strip8 make reference to Vdd2 plane. The voltage at the far end of Strip1, which is connected to the Vdd1 plane at the near end, shows the 3 or 4 ns of time delay of PP1, the voltage between Vdd1 and Gnd1 near the drivers. This time delay is due...
Fig. 17. (a) Waveforms at the far end of striplines (strip1-strip4): no termination. (b) Waveforms at the far end of striplines (strip5-strip8): no termination.

to the time of flight required for the wave to propagate on the stripline to reach the far end of Strip1. An interesting phenomenon can be observed in Strip4 in Fig. 17(a), where the near end is connected to Gnd2 plane. Since Strip4 carries the signal of the Gnd2 plane with respect to Gnd1 plane at the far end of the board, the result represents the amount of noise coupled to a quiet stripline that is referenced to a noisy power plane. In a similar manner, the noise coupled to a quiet stripline (Strip 6) that propagates the Gnd1 plane signal referenced to a noisy power plane (Vdd 2 plane) is shown in Fig. 17(b).

X. SYSTEM LEVEL SIMULATION FOR SSN

In the previous sections, a method was presented for capturing the plane bounce on a test board. It consists of separate models for the planes and interconnections which are then combined to account for the return currents. In this section, the method has been extended for modeling a system containing packages on a printed circuit board.

The system is shown in Fig. 18. The package consists of two planes (Vdd and Gnd) which measures $1.5\text{in} \times 1.5\text{in}$ with a dielectric thickness of 4 mils. The insulator used was ceramic with a dielectric constant of nine. The PCB consists of two planes (Vdd and Gnd) with size $4\text{in} \times 4\text{in}$ and a dielectric thickness of 4 mils. The insulator used was FR4 with a dielectric constant of four. The PCB contains 69 decoupling capacitors which were distributed over the board at arbitrary locations near the packages. Nine commercially available decoupling capacitors were used on the PCB. The capacitors were represented as a series RLC circuit where “R” and “L” are the series equivalent resistance and inductance of the capacitor, respectively. The PCB was powered using a 1.5 V supply at the upper left corner, as shown in Fig. 18.

The two chips were connected using 6 transmission lines as shown in Fig. 18. These transmission lines were connected to 22 active drivers with rise time of 100 ps, which were switched simultaneously. Three transmission lines were referenced to the Vdd plane and the remaining three were referenced to the Gnd plane, both on the package and PCB. Chip C4s with inductance of 0.05 nH were used to connect the chip to the package. Similarly, solder balls with inductance of 0.25 nH were used to connect the package to the PCB. The planes in the package and PCB were connected together using solder balls with inductance of 0.25 nH. A total of 16 C4s and 16 solder balls were used for the transmission lines for the driver and receiver chips and 36 solder balls were used to connect between the package and PCB planes.

A total of nine modes were used to model the package planes while 25 modes were used for modeling PCB planes. Fig. 19 shows the noise measured on the power supply planes. Fig. 19(a) is the noise measured on the package planes in the vicinity of the driver. The noise measured on the package planes in the vicinity of the receiver is shown in Fig. 19(b). Both figures show a distinct resonance in the waveforms due to the planes bouncing in the system. In addition, the noise on the receiver side is caused
XI. CONCLUSIONS

This paper describes an efficient method to model the SSN in multilayered packages and boards. The circuit models are first derived for the multiport power/ground planes. These models are then modified for the multilayered structure. Transmission lines were incorporated into the models based on superposition theory. A test vehicle was designed and measured to obtain the plane-to-plane noise waveforms. The modeling method was correlated with measurements, showing the validity of the method. The simulation of the quiet embedded stripline transmission lines showed the amount of noise coupled to a quiet stripline that is referenced to a noisy power plane. It was demonstrated that using the method discussed in this paper, a system can be modeled to simulate plane bounce and its effect on driver and receiver switching.

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