Microwave Design & Characterization of a Novel Nano-Cu Based Ultra-fine Pitch Chip-to-Package Interconnect

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Abstract

This paper presents design and characterization of Nano-Cu based ultra-fine pitch chip-to-package interconnects for microwave frequencies. Transitions are designed with this new interconnect and characterized upto 40 GHz in Packaging configurations such as Chip-on-Chip and Chip-on-Package.

1. Introduction

Reducing I/O pitch and interconnect losses are the two key technological barriers identified by the 2006 ITRS [1] for micro/nano electronic modules. Current on-chip interconnects in Si CMOS Back End of Line (BEOL) are in the nanometer range while those in package and board are in the microns to mm range. For e.g., in 65 nm node technology [2-3], the BEOL interconnect lines are arranged in 8 to 10 metal layers with line widths from 105 nm (M1) to 540 nm (M8). The state-of-the-art chip-to-package flip-chip interconnects have diameter of 30-50 µm (pitch of 60-80 µm) whereas the substrate interconnects have line widths of 50-100 µm.

The on-chip interconnects (M2) in 65 nm node have line capacitances of 93 fF/mm and sheet resistance of 178 m-ohm/sq [4]. Solder based flip-chip interconnects have parasitics (R, L, C) of 0.1-0.5 pF, 27-41 m-ohm [5] and 0.1nH (approx) respectively. The solder alternatives (ACA/ACF) suffer from high cross-talk between the particles beyond 20 GHz [6].

The above parasitics should be reduced by atleast an order of magnitude considering the clock frequency, supply voltage and Signal to noise ratio of future RF & analog mixed signal systems. In addition, the losses associated with the chip-to-package interconnect transitions should be minimized. In order to address these challenges, this paper proposes a novel Chip-to-Package interconnect technique based on Nano-grained Copper. Nano-grained electroplated copper is chosen as the interconnect material due to its excellent toughness and fracture strength in addition to good electrical conductivity and resistance to electromigration. The mechanical properties of Nano-Cu have been published by the author [7].

This paper, for the first time, presents the transition models for a Nano-copper based chip-to-package interconnect (with dimensions in the order of 15 to 0.5 µm) system. The high frequency performance is studied for Chip-on-Package and Chip-on-Chip configurations upto 40 GHz (Figures 1 and 2). Electrical parasitics of the Nano-Cu based interconnects are extracted from simulations. Physical & material parametric studies (such as interconnect material, shape, dimensions, number of ground bumps and their position) are performed on this interconnect by means of full-wave EM simulations. The paper also presents important interconnect and package design guidelines (obtained from the parametric analysis) for this Nano-copper based chip-to-package interconnect upto 40 GHz.

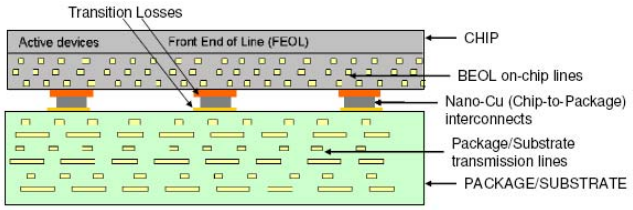

Figure 1. Cross-section view of a Chip-on-Package configuration with Nano-copper interconnections.

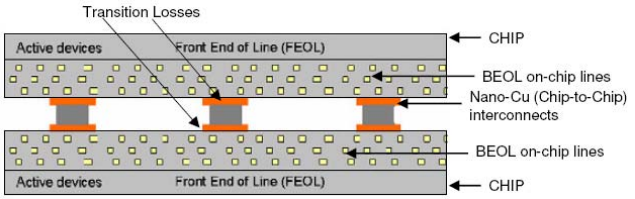

Figure 2. Cross-section view of a Chip-on-Chip configuration with Nano-copper interconnections.

2. Test Vehicle design

Two sets of test vehicles are designed, modeled, fabricated and measured. The first set has Nano-Ni chip-to-package interconnects, and the other has Nano-Cu chip-to-package interconnects.

2.1 Nano-Ni Test Vehicle

This test vehicle has a Si chip assembled on an organic package substrate using Nano-Ni chip-to-package interconnects. The substrate has Cu lines which connect the Nano-Ni chip-to-package interconnects to the probe pads at the outer edge. The Nano-Ni interconnects lead to Cu pads on the chip. Some of these pads are shorted to the adjacent pads (Figure 3) while others are kept open (Figure 4). This arrangement helps to measure the parasitic inductance and capacitance of the Nano-Ni interconnects respectively. The test vehicle is illustrated in the following HFSS models.

2.2 Nano-Cu Test Vehicle

Two sets of test vehicles are designed, modeled and fabricated to have a complete electrical and physical parametric study of chip-on-chip (TV1) and chip-on-package

(TV2) systems with Nano-Cu interconnect transitions. The Chip-on-Chip structures models the Nano-Cu interconnect performance in a 3D chip stack as well as in Si Chip Carrier applications. In TV1, two chips with 65 nm node BEOL interconnects are connected face-to-face by Nano-Cu interconnects. Nano-Cu interconnects of different dimensions from 15 to 0.5 micron (diameter and height) are studied along with a 30 microns diameter solder bump. In TV2, a chip with 65 nm node BEOL interconnects is connected to a 50 micron wide substrate interconnect using different chip-to-package interconnects (solder bump, Au stud and Nano-Cu interconnects). The diameter and height of the Nano-Cu interconnects are varied from 15 to 0.5 microns. Spherical, cylindrical and conical Nano-Cu interconnects are also studied.

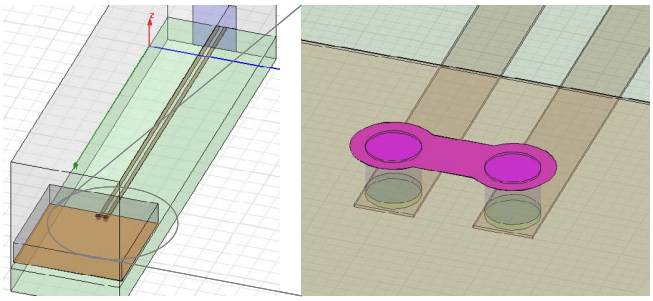

Figure 3. A HFSS model of TV with Nano-Ni interconnects. The adjacent chip pad pairs are connected together.

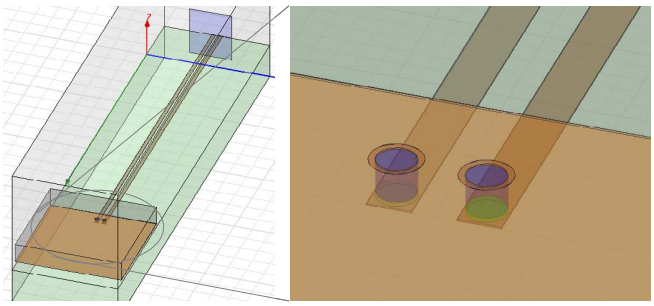

Figure 4. A HFSS model of TV with Nano-Ni interconnects. The chip pads are not connected to any on-chip line.

3. Modeling and Simulations

3.1 Modeling

The interconnect wiring on the Chip and Package is modeled as Microstrip lines. For the on-chip BEOL lines, the simulations are performed with the 65 nm node [2] BEOL line dimensions. Microstrip lines are modeled as lines in the last layer of metallization (M8 layer in Intel's 65 nm node). BCB ($\varepsilon r = 2.65$) is used as a low-k package substrate material. Carbon-doped Oxide ($\varepsilon r = 2.6$) is used as on-chip inter-metal layer dielectric material in the 65 nm node BEOL line models (Figure 5). Ansoft HFSS is used as a 3D full-wave EM simulator to study the system response from 1 to 40 GHz.

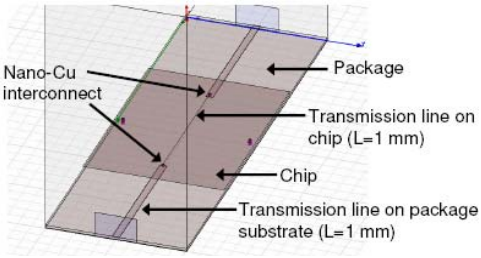

Figure 5. HFSS model for a Chip-on-Package configuration with Nano-copper interconnect.

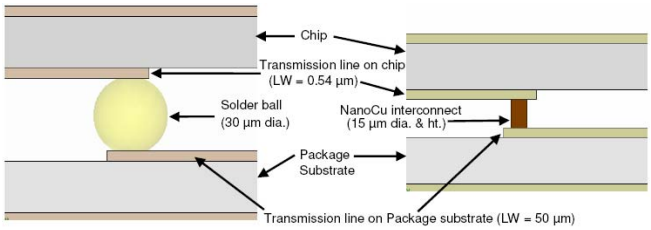

Figure 6. A comparison between traditional solder ball flip-chip and Nano-copper interconnect.

3.2 Comparison with Flip-chip bumps

The Nano-Cu based interconnect (15 µm diameter and height) is compared with traditional solder ball flip-chip bump as well as with gold-stud bumps for interfacing a 65 nm node chip to an organic Package. Figure 4 show the cross-sectional view and Figure 7 shows the S-parameter system response of the structures. It is seen that the Nano-Cu based interconnect offers approximately 5 dB lower return loss as compared to the other interconnects till 40 GHz.

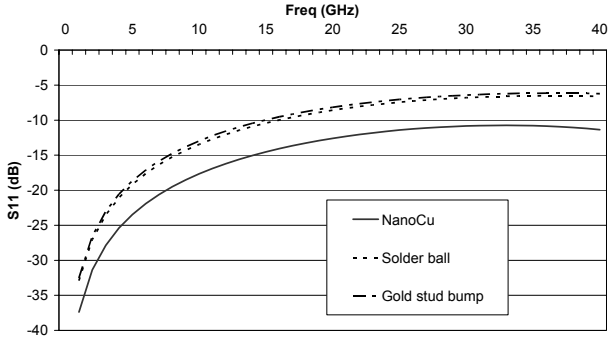

Figure 7. The effect of interconnect material on signal transmission.

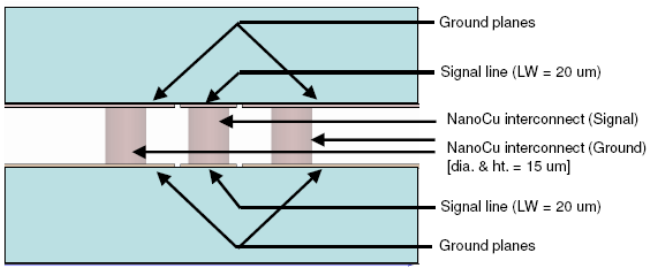

Figure 8. A Package-on-Package structure (cross-section view) with CPW lines connected by Nano-copper interconnects.

3.3 Equivalent circuit model & Parasitic extraction

To investigate and compare the interconnect parasitics, a Package-on-Package structure with Coplanar Waveguide (CPW) lines (LW = 20 um) on BCB package substrate (connected by 15 µm diameter Nano-copper interconnects) is simulated in HFSS (Figure 8).

The CPW lines are de-embedded from the system response to obtain the response of the transition region. An equivalent circuit model (Figure 9) [8] is used to represent this transition region.

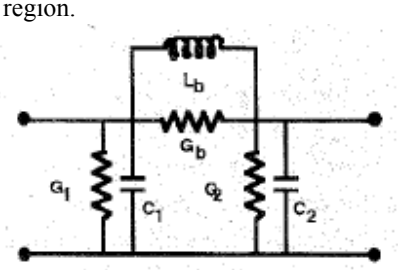

Figure 9. An equivalent circuit model of a chip-to-package interconnect. [8]

The circuit elements' values are extracted from the transition response. A similar PoP structure connected by solder bumps (30 µm diameter) is also simulated, and the transition region parasitics are extracted. Figures 10, 11, 12 and 13 compares the radiation conductance (Gb), bump inductance (Lb), substrate loss conductance of the package (G1 and G2), and the discontinuity capacitance at the package (C1 and C2) respectively of the two interconnects.

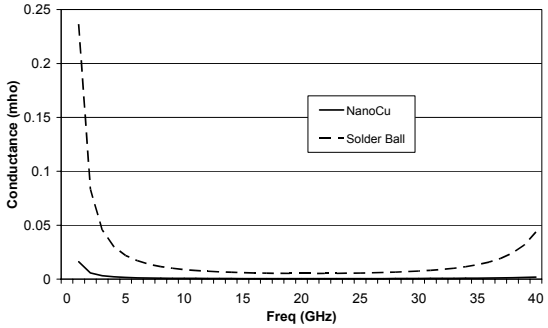

Figure 10. Comparison of the radiation conductance (G_b) of Nano-copper interconnects and solder bumps.

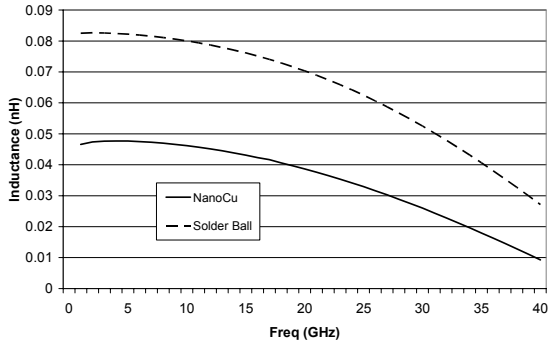

Figure 11. Comparison of inductance (L_b) of Nano-copper interconnects and solder bumps.

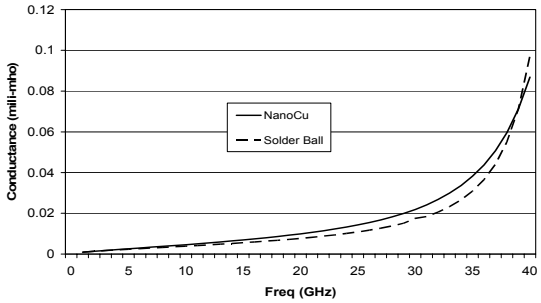

Figure 12. Comparison of the substrate loss conductance of the package (G_1 and G_2) for Nano-copper interconnects and solder bumps.

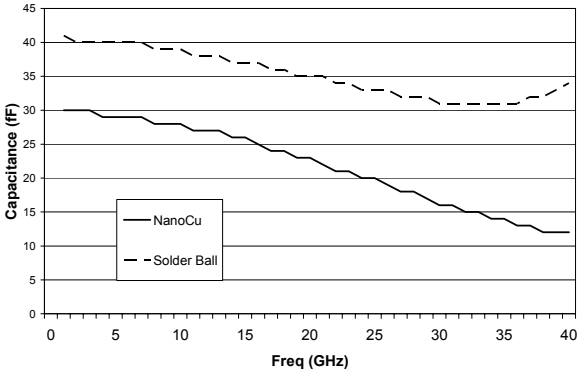

Figure 13. Comparison of the discontinuity capacitance at the package (C_1 and C_2) for Nano-copper interconnects and solder bumps. [Note: The NanoCu interconnect pitch in this case is 60 µm in order to compare with solder bumps of similar pitch.]

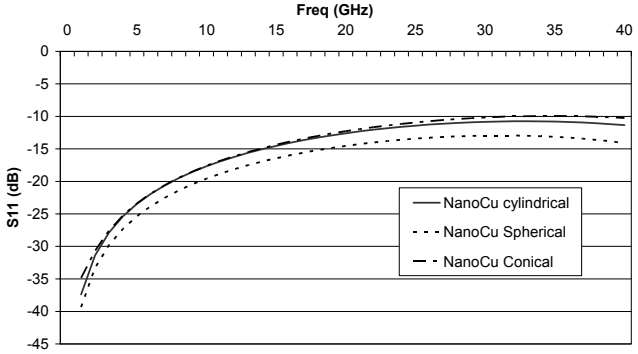

Figure 14. The effect of shape of Nano-copper interconnects on system response in a Chip-on-Package configuration.

For the capacitance study, the NanoCu interconnect pitch is 60 µm in order to compare with solder bumps of similar pitch. The NanoCu interconnect has smaller capacitance than the solder bump. It also has much lower inductance than the solder bump. The radiation conductance of the Nano-copper interconnect is also lower than that of the solder bump indicating that the Nano-Cu interconnect has much smaller radiation loss from 1 to 40 GHz.

4. Design optimizations

Different parametric studies are performed with Nano-Cu interconnect such as: 1) Interconnect shape (Cylindrical, Conical, Spherical), 2) Interconnect dimension (Diameter &

height – from 30 μm to 0.5 μm), 3) Number of ground bumps, and 4) Position of the ground bumps.

4.1 Interconnect shape

Figure 14 shows the Chip-on-Package system response with on-chip and package Microstrip lines connected by Nano-Cu interconnect of different shapes. The spherical Nano-Cu interconnects are seen to have approximately 3 dB lower return loss than the cylindrical and conical Nano-Cu interconnects.

4.2 Interconnect dimension

The parametric study on the Interconnect dimension is carried out for both - Chip-on-Chip and Chip-on-Package configurations. The Chip-on-Chip structures (Figure 2) models the Nano-Cu interconnect performance in a 3D Face-to-Face chip stack as well as in Silicon Chip Carrier applications. In this configuration, two 65 nm chips are connected face-to-face by the Nano-Cu interconnects. Nano-Cu interconnects of different dimensions from 0.5 μm to 15 μm (diameter and height) are studied along with a 30 μm diameter solder bump for these packaging configurations.

The best response for Chip-on-Package configuration is observed in the model with NanoCu bump of 5 μm diameter and height (Figure 15). There are two transitions to the bump in this structure. One is from the transmission line on chip (LW = 0.54 um) to the bump, and the other one is from bump to the transmission line on package substrate (LW = 50 μm). As the dimension (diameter and height) of the bump is reduced from 30 μm to 0.5 μm, the dimensional mismatch between the transmission line on chip and the bump decreases, but the mismatch between the transmission line on package substrate and the bump increases. So the signal scattering at the chip-to-bump interface decreases whereas the scattering at the package-to-bump interface increases.

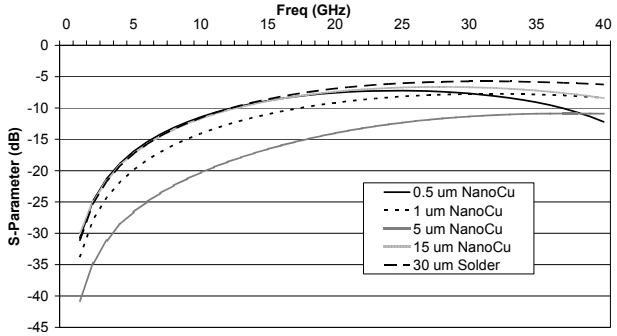

Figure 15. A parametric study on the dimensions (diameter and height) of the Nano-copper interconnects in a Chip-on-Package configuration.

The transitions in a Chip-on-Chip system are from the transmission line on chip to the bump. As the dimension (diameter and height) of the bump is reduced from 30 μm to 0.5 μm, the dimensional mismatch between the line and the bump decreases. This leads to less signal scattering at the interface region. Therefore lower losses are observed in the simulations with smaller bumps, the best system response being the one with Nano-Cu interconnects of diameter and height 0.5 μm (Figure 16).

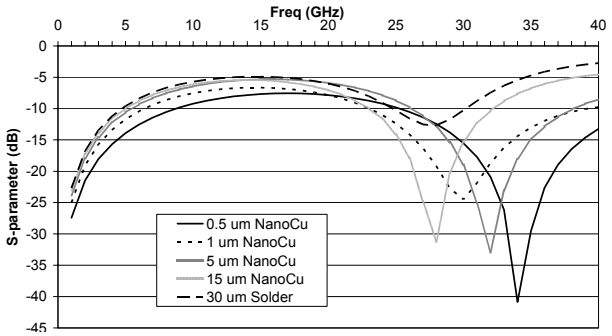

Figure 16. A parametric study on the dimensions (diameter and height) of the Nano-copper interconnects in a Chip-on-Chip configuration.

4.3 Number of Ground connections

The number of ground vias/bumps connecting the chip and package ground planes (with transmission lines on package and chip modeled as Microstrip lines) in a Chip-on-Package configuration is varied to observe its effect on the system response. The chip-to-package interconnects used in this parametric study are Nano-Cu interconnects (15 μm diameter and height). It is observed from Figure 17 that the system response greatly improves by increasing the number of ground via/bump connections.

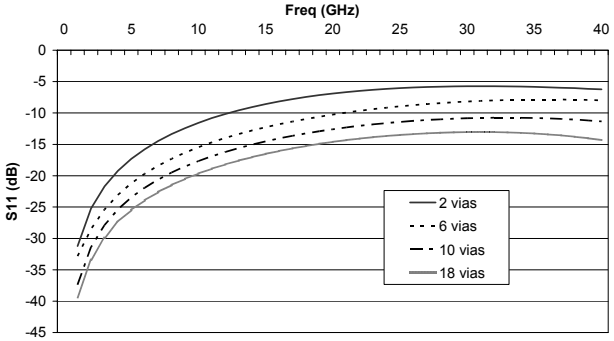

Figure 17. System response variations due difference in the number of ground bumps/vias connections in a Chip-on-Package configuration.

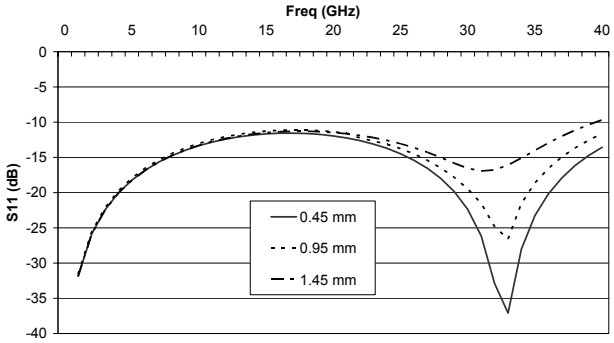

Figure 18. System response variations due difference in the distance between the ground bumps/vias connections and the signal line in a Chip-on-Package configuration.

4.4 Position of Ground connections

The effect of the position of the ground connections relative to the signal line (and the signal transition points) is also studied with Nano-Cu interconnects. It is seen from

Figure 18 that bringing the ground connection points closer to the signal line reduces the signal loss above 20 GHz.

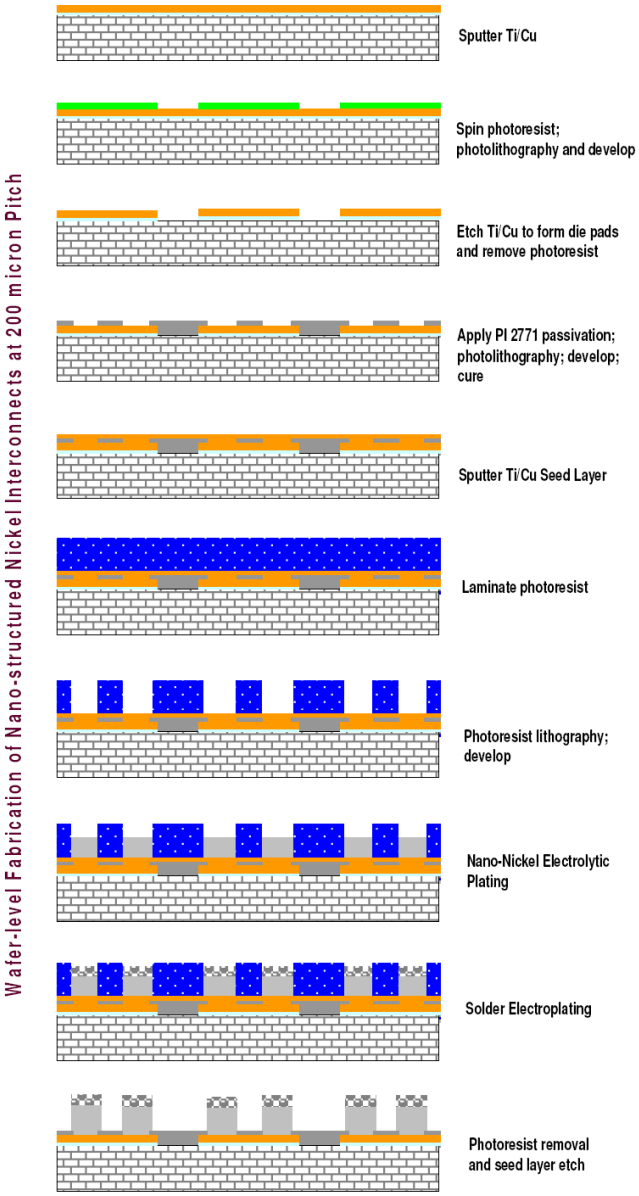

Figure 19. Baseline process for fabrication of nanostructured Ni interconnections with solder caps. [9]

Figure 20. Plating Steps and reflow process for formation of AuSn solder cap. [9]

5. Test Vehicle Fabrication

5.1 Nano-Ni Test Vehicle

The process for fabrication of nanostructured Ni-interconnects is shown in Figure 19. The pitch of the NanoNi interconnects is 200 µm. A negative photoresist, WBRT50 is used as the electroplating mold. Nickel HT-2, a nickel sulfamate electroplating chemistry (Technic Inc.), is used for plating the nano-nickel interconnects. This produces ultra-fine grained low-stress deposits of nickel. The nanostructure (60 nm grain size) was confirmed with XRD and SEM studies. A high reliable and fluxless contact is achieved using eutectic AuSn solder. The surface of the AuSn bumps consists of a eutectic composition 80Au20Sn, which is used for creating a solder joint to the NiAu landing pads on the substrate. The formation of eutectic AuSn solder is done by electroplating of Au and Sn in successive process steps (Figure 20) followed by a reflow step at 300°C to allow interdiffusion of Au and Sn stacks during which eutectic solder cap is formed. The reflow leads to an even bump surface and prevents the bumps surface from oxidizing.

Si dies are assembled on an organic substrate. A subtractive process is used to form the metal traces on the organic substrate. 100 µm wide lines are used to connect to the substrate pads. More details about the fabrication and assembly of the NanoNi interconnects can be found in [9].

5.2 Nano-Cu Test Vehicle

5.2.1 Die Fabrication

3mm x 3mm dies with a daisy chain of electroplated Cu bumps at 30 micron pitch are fabricated at wafer level. The interconnects are fabricated on 4" silicon wafers where each die pad footprint matches the substrate, which in this study is a Silicon carrier, to which each singulated die will subsequently be assembled onto. The baseline process for fabrication of electroplated Cu-interconnects is shown in Figure 21. Figure 22 displays the cross-sectional view of wafer used to fabricate the interconnect structures.

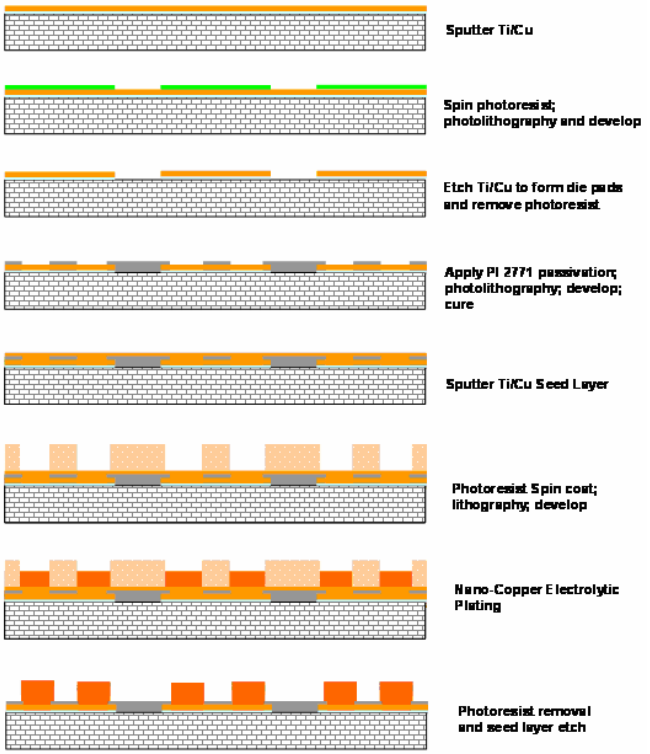

Figure 21. Baseline process for fabrication of electroplated Copper interconnections

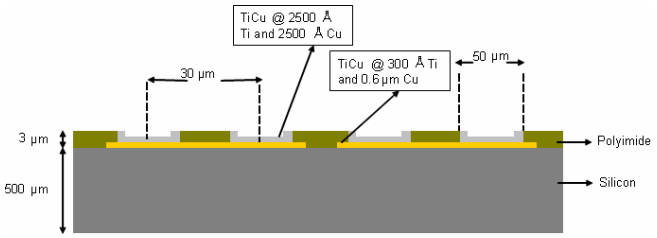

Figure 22. Cross-sectional View of Silicon Wafer used to fabricate the Copper interconnects at 30 µm pitch.

1.5 micron thick SiO_2 layer is put on pre-cleaned 4" Silicon wafers using PECVD to passivate the wafers. This is followed by sputtering of Ti (300Å)/Cu (6000Å) as die-side metallization. Here, Ti serves as an adhesion layer between silicon oxide and the copper layer that forms the conducting traces on the die side. Copper as such does not have a very good adhesion with silicon/silicon oxide and hence such an adhesion layer is very critical. This metallization is then patterned with an etch back process to make die-side pads and CPW lines using a thin layer of SC 1813 photoresist (Shipley Chemicals). This positive tone photoresist selectively protects the die-side pads and CPW lines and the rest of the metallization is etched using Copper and Titanium etchants sequentially. 3 microns thick Polyimide (PI 2771) passivation is used to protect the die-side pads and CPW lines. PI2771 (HD Microsystems) is a commercially available photo-definable polyimide. This polyimide layer works as a stress buffer and also provides protection from moisture, corrosion, ion transport, and mechanical damage during packaging steps. Followed by passivation, the wafer is sputtered with a layer of Ti/Cu that serves as a seed layer for the electroplating step. The sputtered seed layer comprises of 2500Å each of titanium and copper.

NR5-8000 negative photoresist from Futurrex is used as mold for electroplating 10 micron tall and 15 microns diameter electroplated Cu bumps. Negative Resist NR5-8000 is a negative tone photoresist designed for thick film applications and is compatible with UV exposure tools emitting at the 365nm wavelength. It has superior resolution capability and high photospeed which translates into high exposure throughput.

Copper Gleam 125-EX chemistry from Rohm and Haas is used for plating the interconnections. It is a high-acid Copper electroplating chemistry that produces ultra-fine grained equiaxed deposits of Copper. Followed by electroplating of Copper interconnections, photoresist is stripped-off and seed layer is etched away with Copper and Titanium etchants.

5.2.2 Silicon Carrier Fabrication

The Silicon carrier, that the dies are assembled onto, has 20 microns diameter bump pads and pad to pad spacing of 10 microns. Every fourth bump is routed to a probe pad of dimensions 1.5mm x 1.5 mm through 15-50 micron wide traces This is done to monitor the daisy chain connectivity. The three sets of CPW lines are routed to GSG probe pads which are used to measure the electrical parasitics of the interconnects and the performance of the interconnect when a high frequency signal is propagated through the system.

The Silicon carrier is made using a lift-off process. The Silicon carrier metallization is Cr (300Å)/Cu (4000Å)/Au (1000Å). NR5-8000 negative photoresist is used here also to evaporate and lift-off the bump pads and traces.

5.2.3 Assembly

Singulated dies are assembled onto Silicon carriers using NCF and nano-ACF. NCF is a non conducting film of epoxy and nano-ACF is anisotropically conductive due to nano-Ag fillers embedded in the epoxy film The film thickness used is 25 microns.

Assembly with nano-ACF/NCF is carried out using Fineplacer assembly tool. The n-ACF/NCF film is applied onto the substrate. The chip and substrate are then aligned and pre-heated at 80°C to decrease the viscosity of the epoxy. Followed by this, the chip and substrate are pressed together and heated upto 180 °C for 5 minutes to ensure complete curing of the epoxy. During the curing process, the epoxy shrinks and holds the chip and substrate together enabling a mechanical contact in case of NCF and a metallurgical contact in case of nano-ACF due to the sintering of nano-Silver particles to the substrate metallization and bump surface.

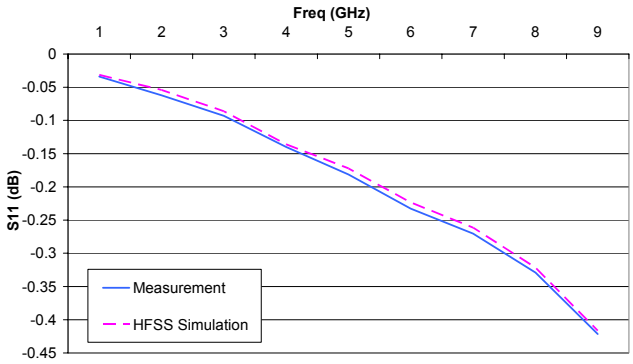

Figure 23. Correlation between HFSS simulation and measurement results for TVs with chip pads not connected to one another (Figure 4).

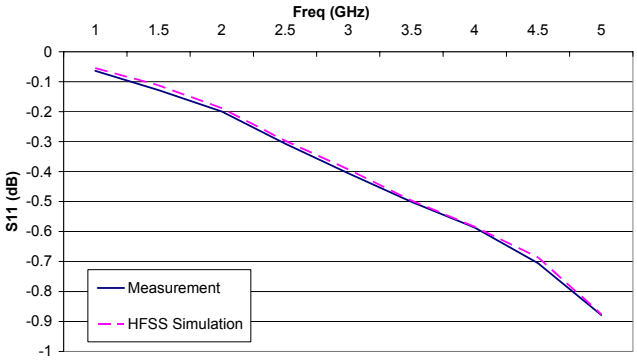

Figure 24. Correlation between HFSS simulation and measurement results for TVs with chip pads connected to the adjacent pad (Figure 3).

6. Measurement methodology and results

The TVs with Nano-Ni interconnects are fabricated and the models are validated by frequency domain measurements from 1 to 5 GHz. The test vehicle measurements are done using a 1 port Vector Network Analyzer from Agilent Technologies. SOLT calibration is performed prior to

measurements. The return losses (S11) are measured and the following figures show the correlation between simulation and measurement results.

The test vehicles with Nano-Cu interconnects have been fabricated. The measurement and model validation of these test vehicles are being performed. The initial results of chip-to-chip interconnect with Nano-Ni and Nano-Cu in 3D is shown in Figure 25. A TV has also been prepared with a Si die assembled on a glass substrate with Nano-Cu interconnects. The simulation result for this is also shown in Figure 25.

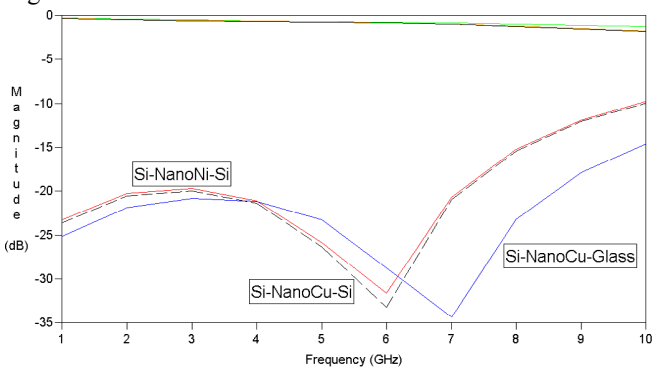

Figure 25. HFSS simulation results showing the Insertion and Return losses for 3D Nano-Cu and Nano-Ni interconnects in Si die on Si substrate and, Si die on glass substrate configurations.

Modeling & measurements with Nano-Ni, and simulations and parametric design optimizations with Nano-Cu interconnects are discussed in this paper.

7. Conclusions

The novel Nano-structured copper based chip-to-package interconnect exhibits a much better high frequency response as compared to conventional flip-chip bumps in Chip-on-Chip and Chip-on-Package configurations. Nano-Cu interconnects offers approximately 5 dB lower return losses till 40 GHz, as compared to solder bumps and Au stud interconnects. They have ~40% lower capacitance, ~50% lower inductance, and lower radiation conductance than solder bumps in the frequency range of 1-40 GHz. Further, Nano-Cu interconnects exhibit 8 dB lower return losses in Chip-on-Package applications, and 5 dB lower return losses in Chip-on-Chip applications. The spherical interconnects show better high frequency response than cylindrical interconnects.

Acknowledgments

The authors would like to acknowledge Abdemanaf Tambawala and Ankur Aggarwal for the measurements and fabrication of the Nano-Ni test vehicles, respectively. The authors also thank the companies involved in the EMAP consortium for their funding support.

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