Correlation of PDN Impedance with Jitter and Voltage Margin for High Speed Channels

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Abstract: Timing margin (jitter) and voltage margin (noise) are the main bottlenecks in the performance of high speed digital channels. The simultaneous switching noise (SSN) induced by the return path discontinuities such as signal via transitions and plane cutouts is a major source of jitter and noise introduced by the package and the printed circuit boards on the signal interconnects of these channels. In this paper, we present a new methodology to correlate SSN induced signal jitter and noise with the power distribution network (PDN) impedance by studying the exact mechanism of how the PDN impedance affects signal jitter and voltage margin. Further, we validate the analysis by both simulations and measurements and suggest design practices to reduce jitter and noise on the signal.

I. INTRODUCTION

Advances in packaging technology have resulted in large scale integration and miniaturization making it possible to support increasing data rates on the package and the printed circuit board (PCB) interconnects [1]. The signal traces on the package and the PCB are referenced to either the power plane or the ground plane or both to provide return current path for transverse electromagnetic wave propagation. Any change in the reference from the power plane to the ground plane or vice versa, due to signal via transitions or plane cutouts can result in a discontinuity in return current path called return path discontinuity (RPD). The return current induces simultaneous switching noise (SSN) between the power and ground planes at the RPD [2-4].

The SSN induced by the RPDs is a significant source of noise and jitter introduced on the high speed signal interconnects on the package and the PCB. As a result, the package and the PCB still remain the main bottlenecks in performance of high speed channels such as Front Side Bus (FSB) and dual data rate (DDR) memory. Hence, it is important to quantify the jitter and noise induced on signal interconnects due to SSN.

Prior work in this area has mainly focused on studying, modeling and reducing SSN [3-6]. Some work has also been done to demonstrate the effect of SSN on signal propagation delays and voltage levels [6-8]. In this paper, we present a new methodology of quantifying the impact of SSN on timing and voltage margin by looking at jitter and noise on the signal in terms of PDN impedance. We provide a detailed analysis of the impact of PDN impedance on the SSN induced jitter and noise on pseudo random bit stream (PRBS) and clock signals and validate it with hardware measurements. Finally, we suggest design guidelines that can be used to reduce jitter and noise induced due to the presence of RPDs.

The paper is organized as follows: Section II describes the mechanism of how PDN impedance affects timing and voltage margin. Section III describes the test structures and measurement results to validate the analysis. And, Section IV describes design practices to reduce jitter and noise.

II. IMPACT OF PDN IMPEDANCE ON JITTER AND VOLTAGE MARGIN

The impact of PDN Impedance on jitter and voltage margin is analyzed first by analyzing its impact on the insertion loss of signal having RPD, and then analyzing the impact of the signal insertion loss on jitter and noise.

A. Impact of PDN Impedance on Insertion Loss

The PDN impedance is a function of frequency and has alternate minima and maxima at resonances and anti-resonances (parallel resonance) based on the resonance modes. Since, the return current of the signal sees the PDN impedance at its RPD, the insertion loss of the signal peaks at the maxima of PDN impedance. This can be shown by comparing the insertion loss and the PDN impedance (at RPD) for Structure-A and Structure-B in Fig. 1 and Fig. 2. Though both the structures have the same PDN, the PDN impedance at the RPD in Structure-1 has fewer anti-resonances compared to the PDN impedance of Structure-2 at its RPD. As a result, the insertion loss for Structure-A has fewer peaks compared to that of Structure-B.

In the presence of multiple RPDs, the frequency at which the insertion loss of the signal peaks depends on the magnitude and phase of SSN voltage (V_{SSN}) induced at each RPD. V_{SSN} at a particular RPD, in turn depends on the magnitude and phase of the PDN impedance and the return current at that RPD. When the induced SSN voltages are out of phase, they tend to cancel each other out, reducing the impact on signal insertion loss. For example, in case of Structure-C, shown in Fig. 1(c), the signal insertion loss (Fig. 2(c)) doesn't peak at 600 MHz in spite of anti-resonance in PDN, as V_{SSN1} and V_{SSN2} completely cancel each other out at that frequency. Similarly, at other frequencies, the insertion loss is higher or lower or equal to that of Structure A or Structure B based on the magnitude and phase of V_{SSN1} and V_{SSN2}.

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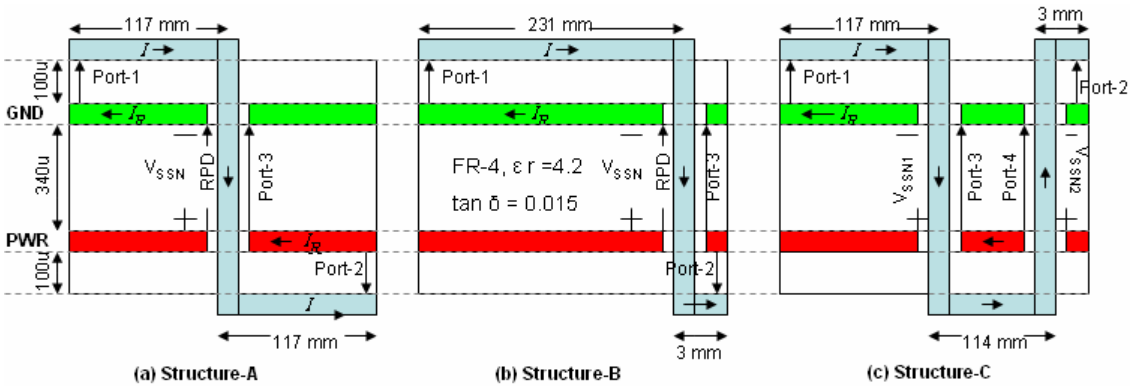

Fig. 1. Cross-section of three 234x20mm structures having different RPD locations on signal interconnect.

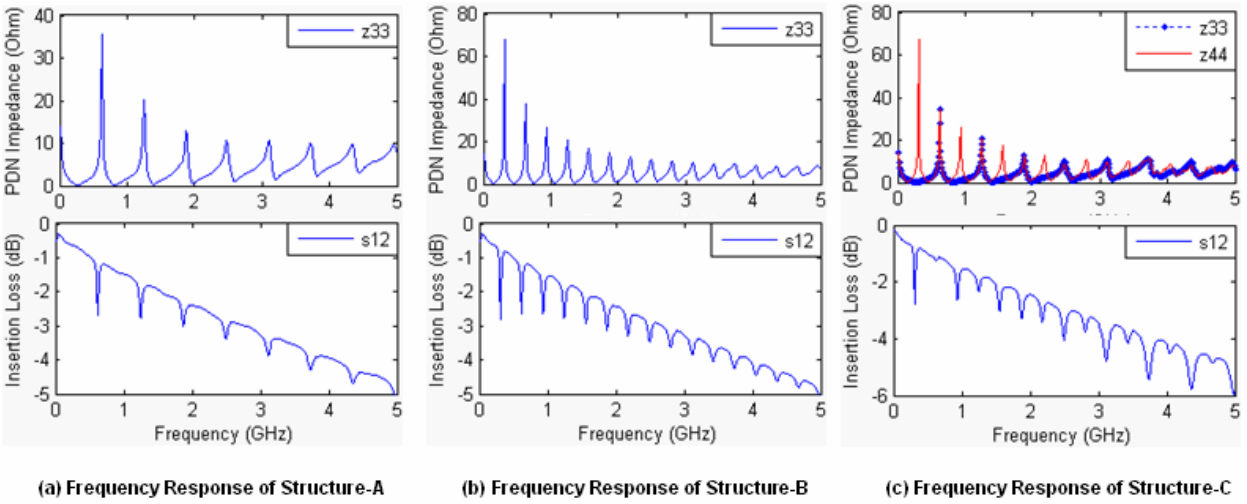

Fig. 2. Simulated values of PDN impedance and insertion loss of structures A, B and C.

From the above analysis, it can be inferred that PDN impedance at RPD has a significant impact on the signal insertion loss.

B. Impact of Signal Insertion Loss on Timing and Voltage Margin

The insertion loss of the signal along with its harmonic content governs the jitter and noise and hence the timing and voltage margin of the signal.

The harmonic content of pseudo random bit stream (PRBS) is spread across multiple frequencies, the envelop of which is a sinc^2 function with nulls at the multiples of the bit rate. For example, the power spectrum of a 600 Mbps PRBS (2^{31}-1), shown in Fig. 3, has nulls at multiples of 600 MHz and has significant harmonic content at 900 MHz, 1500 MHz and so on. If the significant harmonics of a signal coincide with the peak in its insertion loss, they undergo a large attenuation causing degradation in the signal voltage and its rise/fall times. If the spectrum is spread out as in case of a PRBS, different degrees of attenuation and degradation in the rise/fall times result in the noise and jitter on the signal decreasing the voltage and timing margins.

For a clock signal the harmonics are concentrated at the odd multiples of clock frequency as shown in Fig. 4. If significant clock harmonics undergo attenuation due to high insertion loss, they cause a large reduction in clock signal amplitude and an increase in rise/fall times. However, since these harmonics are concentrated at discrete frequencies, there is very little variation in the rise/fall times and hence only a small amount of jitter is induced.

The analysis done in both the above subsections is validated by measurements on the test structures described below.

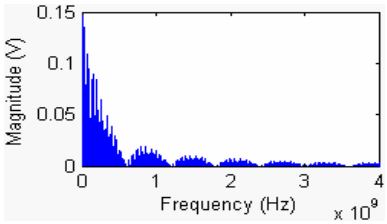

Fig. 3. Power spectrum of 600 Mbps 2^{31}-1 PRBS.

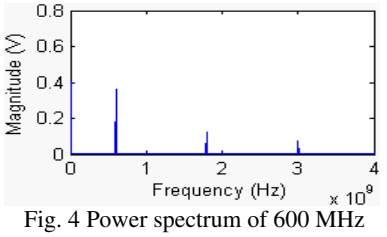

Fig. 4 Power spectrum of 600 MHz clock.

III. TEST STRUCTURES

Two test structures TS1 and TS2 are manufactured as shown in Fig. 5. TS1 has two and TS2 has four via transitions. Capacitor pads are provided at each via transition so as to reduce PDN impedance at the RPD by soldering surface mount decoupling capacitors (decaps) with capacitance value of 4700pF, ESL of 0.3nH and ESR of 0.25 Ohms.

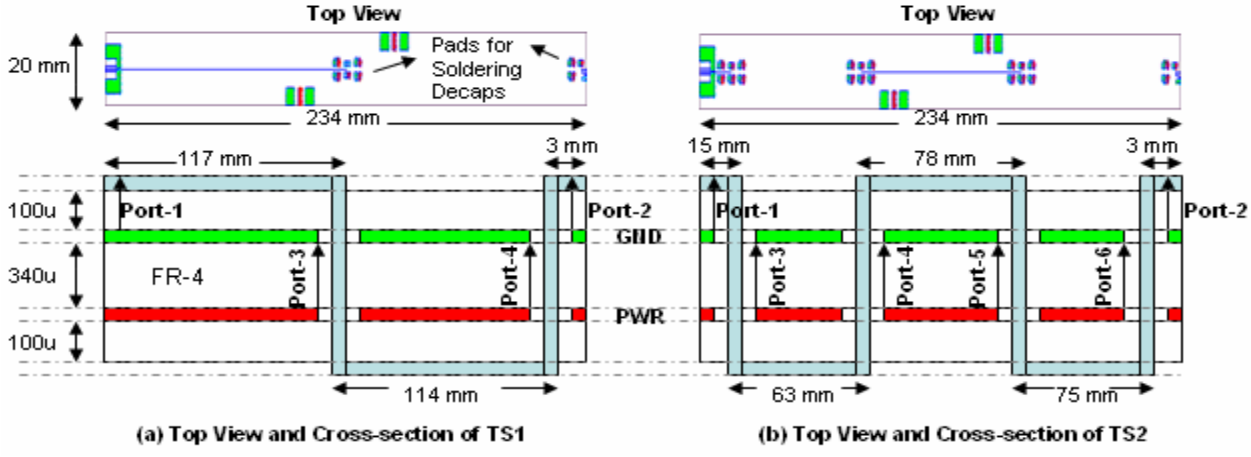

Fig. 5. Top-view and cross-section of manufactured test-structures, TS1 and TS2.

A comparison of measured value of PDN impedance and insertion loss for TS1, with and without decoupling capacitors, is shown in Fig. 6.

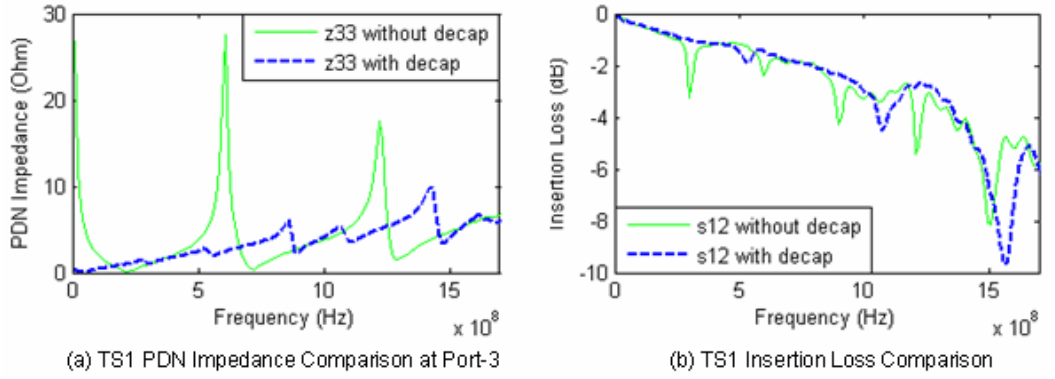

Fig. 6. Comparison of measured PDN impedance and insertion loss of TS1 with and without decoupling capacitors.

The resulting eye diagrams measured at port-2 (terminated with 50 ohm resistance) with 600-Mbps PRBS (2^{23}-1) as input at port-1 are shown in Fig. 7.

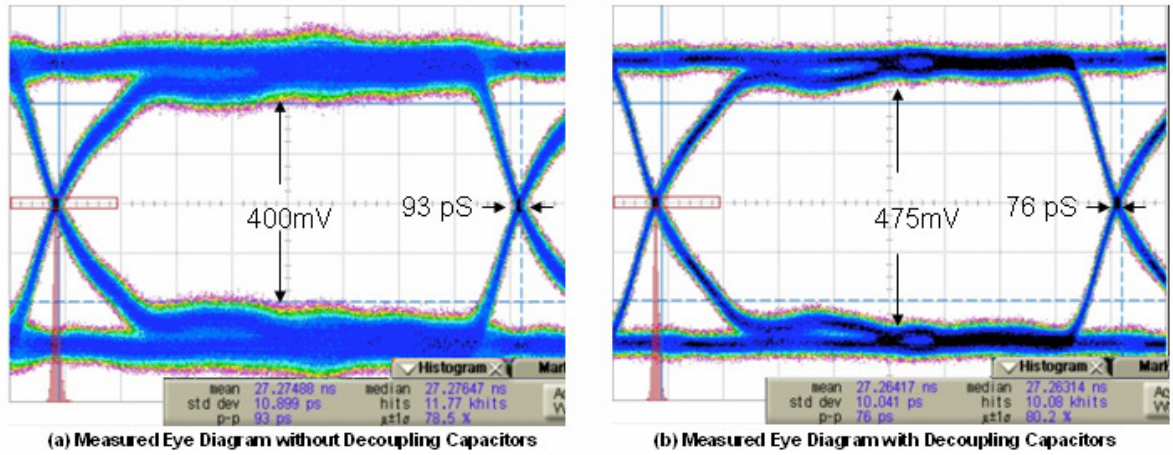

Fig. 7. Measured eye at port-2 of TS1 for 0.8V, 600-Mbps, 2^{23}-1 PRBS.

A summary of similar measurements with clock and PRBS on TS1 and TS2 is presented in Table 1.

Signal Type	**0.8V, 600 MHz CLOCK**		**0.8V, 600-Mbps, 2^{23}-1 PRBS**	
Test Structure	**Jitter**	**Amplitude**	**Jitter**	**Eye Height**
TS1 without Decap	15 pS	590 mV	93 pS	400 mV
TS1 with Decap	12 pS	680 mV	76 pS	475 mV
TS2 without Decap	18 pS	200 mV	84 pS	550 mV
TS2 with Decap	13 pS	575 mV	71 pS	590 mV

Table 1. Measured Eye Height and Jitter Values for TS1 and TS2 for Clock and PRBS Signals.

From the above results following observations can be made:

1. Smaller value of the PDN impedance at RPD (obtained by adding decoupling capacitors) results in smaller jitter and noise.
2. In spite of having more RPDs than TS1, test structure TS2 induces smaller jitter and noise on a 600-Mbps PRBS. This is because the significant harmonics of 600-Mbps PRBS coincide with the peak in the insertion loss of TS1. On the other hand, there are no harmonics present at the peak in the insertion loss of TS2. Comparison of measured values of insertion loss of TS1 and TS2 overlapped with power spectrum of 600-Mbps PRBS is shown in Fig. 8.
3. In the absence of decaps, a 600 MHz clock signal sees huge attenuation in TS2 (refer Table 1) as the peak in insertion loss in TS2 coincides with the fundamental harmonic of the clock.
4. The jitter on clock signal is very small in comparison with the jitter on a PRBS.

The above observations validate the analysis in Section-II.

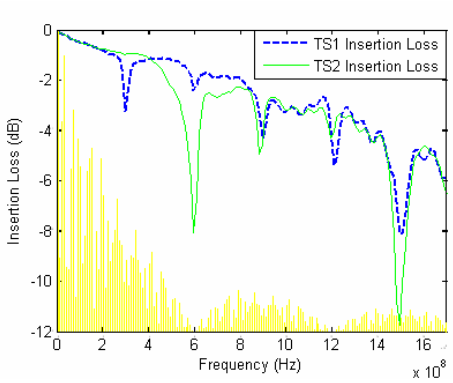

Fig. 8. Comparison of TS1 and TS2 insertion loss.

III. DESIGN GUIDELINES TO REDUCE SIGNAL JITTER AND NOISE

Based on the analysis and results in the previous sections, following design guidelines are proposed to increase the timing and voltage margin of PRBS and clock signal:

1. The PDN impedance at RPDs should be minimized. Suitable decoupling capacitors may be added for the same.
2. For a given power delivery network, the RPDs should be chosen at the point of minimum PDN impedance. Multiple RPDs at optimal locations can be used to reduce the impact of PDN impedance at frequencies of interest.
3. The PDN impedance should be designed such that the anti-resonances do not coincide with significant harmonic content of signals supported on the system.

IV. CONCLUSION

A detailed analysis of the effect of PDN impedance on timing and voltage margin has been done. It is shown that anti-resonances in PDN impedance cause significant increase in the insertion loss of interconnect whose return current is disrupted at return path discontinuities. The increase in insertion loss may attenuate significant harmonics of a signal degrading its rise/fall times and voltage level leading to decreased timing and voltage margins. The analysis is validated by hardware measurements, based on which, design guidelines to reduce jitter and noise have been proposed.

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