Polarization Mode Basis Functions for Modeling Insulator-Coated Through-Silicon Via (TSV) Interconnections

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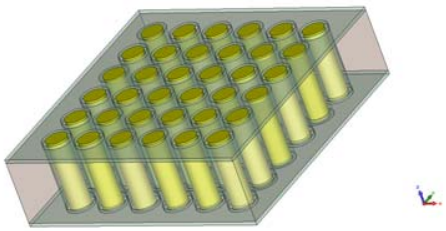
Abstract

For the design of high-density 3-D integration, this paper presents a method to model through-silicon via (TSV) interconnections. Focusing on the modeling of annular insulator coating around the TSV, this paper proposes a new type of modal basis functions that describe polarization current density distribution in insulator. The equivalent network including modal excess capacitance from the basis functions provides accurate electrical characteristics, compared with analytic and EM simulation results.

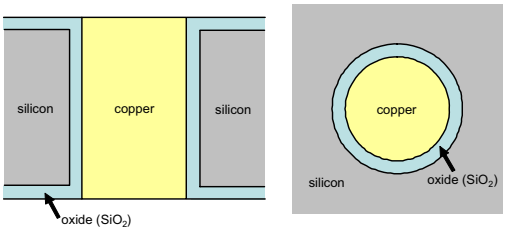
Introduction

To meet the demands for higher density integration, the trend of three-dimensional (3-D) packaging is moving to silicon-based technology [1]. In the silicon-based packaging, the vertical interconnections are realized as through-silicon via (TSV) interconnections, the electrical behavior of which is important for successful signal transmission between stacked dies and boards. Thus, the accurate and efficient modeling approach is necessary for the proper design of TSV interconnections.

For modeling cylindrical via structures, equivalent circuit with cylindrical modal basis functions can be a suitable method [2]. However, TSV interconnection is not simply a cylindrical conductor, but is surrounded by an insulator (SiO_2) layer in the silicon media, as shown in Figure 1. Since the insulators and lossy silicon media modify the characteristics of via conductors, the analysis of the effects of these parameters is critical for accurate TSV interconnection modeling.



(a) Typical TSV array configuration.



(b) Side (left) and top (right) views of a single TSV.
Figure 1. Structural description of TSV interconnection.

In this paper, we mainly focus on the modeling of thin insulator coating on the TSV interconnections. To describe the polarization currents in insulator, new cylindrical modal basis functions are proposed, and resultant modal excessive capacitances are combined with other modal elements. Examples of simple TSV structures are simulated and the results are compared with an existing analytic full-wave EM simulation results.

Polarization Mode Basis Functions

Figure 1 shows that the insulator coating on a TSV conductor forms an annular dielectric region between the cylindrical conductor and the surrounding media. In DC or low frequencies, the dielectric region blocks the leakage of conduction current from via interconnection to the silicon media. However, as frequency increases, the capacitance of the annular dielectric provides the path of leakage polarization currents, which increases insertion loss in high frequencies.

To capture the polarization currents in the annular dielectric region is the basic idea of constructing polarization mode basis functions (PMBS). PMBSs come from the general solutions of Laplace's equation [3] in the dielectric region, so satisfy both Dirichlet boundary condition on the conductor-insulator interface and Neumann boundary condition on the insulator-background interface [4]. After normalization, the PMBSs are defined as follows.

$$\vec{u}_{imd}(\rho,\varphi) = \begin{cases} \dfrac{1}{A_{i0}}\dfrac{\rho_c}{\rho}\hat{\rho} & m=0 \\ \dfrac{1}{A_{imd}\rho}\left\{P_m\left(\dfrac{\rho}{\rho_c}\right)\cos(m\varphi)\hat{\rho} - Q_m\left(\dfrac{\rho}{\rho_c}\right)\sin(m\varphi)\hat{\varphi}\right\} & m>0,\ \mathrm{d-mode} \\ \dfrac{1}{A_{imq}\rho}\left\{P_m\left(\dfrac{\rho}{\rho_c}\right)\sin(m\varphi)\hat{\rho} + Q_m\left(\dfrac{\rho}{\rho_c}\right)\cos(m\varphi)\hat{\varphi}\right\} & m>0,\ \mathrm{q-mode} \end{cases}, \quad (1)$$

where

$$P_m(\rho/\rho_c) = m\left\{(\rho/\rho_c)^m + (\rho/\rho_c)^{-m}\right\},$$
$$Q_m(\rho/\rho_c) = m\left\{(\rho/\rho_c)^m - (\rho/\rho_c)^{-m}\right\},$$

and A_{imd} 's are normalization constants in m^2.

As in the case of the other cylindrical modal basis functions, the phases of two higher order functions are orthogonal to each other. PMBSs are vector functions that are composed of radial and angular components, but are independent of frequency like cylindrical accumulation mode basis function (AMBF) [2]. The two higher order functions are also orthogonal to each other in their physical directions.

Exemplary vector plots of the fundamental and higher-order mode basis functions are shown in Figure 2. All the basis functions are the solutions of Laplace's equation, and

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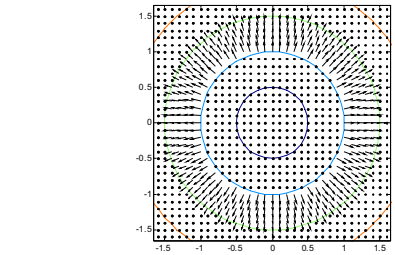
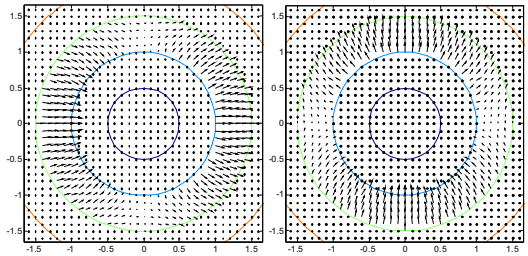
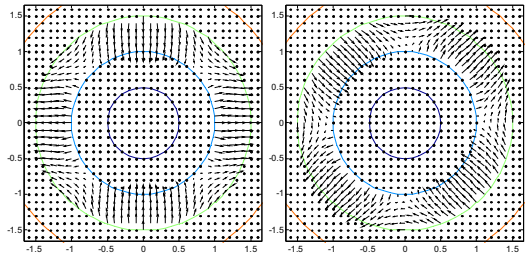


(a) Fundamental mode



(b) 1st order modes



(b) 2nd order modes

Figure 2. Vector plots of PMBFs in an annular dielectric region between the radius of 1 and 1.5.

satisfy the boundary condition at the inner conductor interface.

EFIE Formulation

For the complete modeling of TSV interconnections, we need to find the following interconnection parasitic elements.

1) Loss and inductive coupling in copper conductors.
2) Capacitive coupling on copper conductor surfaces.
3) Capacitive coupling on oxide surfaces.
4) Excess capacitance in annular oxide structure.

For extracting 1), EFIE formulation with cylindrical CMBFs can be used [5]. After replacing the free-space permittivity with the silicon permittivity, capacitive couplings in 2) and 3) can be found from scalar potential integral equation with cylindrical AMBFs [2]. Therefore, this paper does not discuss in detail about 1), 2) and 3), and focuses on the excess capacitance extraction in oxide structure.

The cylindrical PMBFs are involved with electric field integral equation (EFIE), which expresses the voltage difference produced by polarization currents in the annular dielectric region. Since there is no conduction current in an insulator, conduction current is not included in EFIE. Instead, the following polarization current $\vec{J}^P$ is defined as in the conventional partial element equivalent circuit (PEEC) method including dielectric [6].

$$\vec{J}^P(\vec{r}) = j\omega\varepsilon_0(\varepsilon_r - \varepsilon_B)\vec{E}(\vec{r}), \qquad (2)$$

where ε_r and ε_B are the permittivities of insulator (oxide) and background media (free space or silicon), respectively. The polarization current contributes the potential gradient as shown in the following EFIE.

$$\frac{\vec{J}^P(\vec{r})}{j\omega\varepsilon_0(\varepsilon_r - \varepsilon_B)} + j\omega\frac{\mu}{4\pi}\int_{v'} G(\vec{r},\vec{r}')\vec{J}^P(\vec{r}')dv' = -\nabla\Phi\,. \qquad (3)$$

After approximating the polarization current with the cylindrical CMBFs and applying inner product based on Galerkin's method, we can obtain the following equation.

$$\frac{I^P_{imd}}{j\omega C^+_{imd}} + \sum_{j,n,q} j\omega L_{imd,jnq} I^P_{jnq} = \Delta V_{imd}, \qquad (4)$$

where C^+_{imd} is a modal excess capacitance that is defined as follows.

$$C^+_{imd} = \frac{\varepsilon_0(\varepsilon_r - \varepsilon_B)}{\int_{v_i}|\vec{u}_{imd}|^2 dv_i} = \begin{cases} \frac{2\pi l_i\varepsilon_0(\varepsilon_r-\varepsilon_B)}{\ln(\rho_d/\rho_c)} & m=0 \\ \frac{16ml_i\varepsilon_0(\varepsilon_r-\varepsilon_B)}{\pi\tanh(\rho_d^m/\rho_c^m)} & m>0 \end{cases}. \qquad (5)$$

$L_{imd,jnq}$ is modal partial self or mutual inductance representing inductive coupling caused by the polarization current, and ΔV_{imd} represents a modal voltage difference.

$$\Delta V_{imd} = \int_{v_i} \vec{u}_{imd}\cdot(-\nabla\Phi)dv_i\,. \qquad (6)$$

Equivalent Circuit

The modal voltage difference (6) contains important information about connecting excess capacitances in insulators with other parasitic elements, such as series impedances along conductors and parallel capacitances (admittances) across conductors. Using a vector identity, (6) can be reduced to the following surface integrals on inner (S_C) and outer (S_D) surfaces on the annular dielectric region.

$$\Delta V_{imd} = -\int_{S_C}\Phi^C_i\vec{u}_{imd}\cdot\hat{n}_c dS_C - \int_{S_D}\Phi^D_i(\varphi)\vec{u}_{imd}\cdot\hat{n}_d dS_D\,, \qquad (7)$$

where all the vectors, surfaces, and potentials are defined in Figure 3. Φ^C_i is the electric potential on the conductor surface, so should be a constant value. However, the potential $\Phi^D_i(\varphi)$ on the oxide boundary is not a constant, but can be expressed by a linear combination of harmonic functions.

$$\Phi^D_i(\varphi) = \Phi^D_{i0} + \frac{4}{\pi}\sum_{m=1}[\Phi^D_{imd}\cos m\varphi + \Phi^D_{imq}\sin m\varphi]. \qquad (8)$$

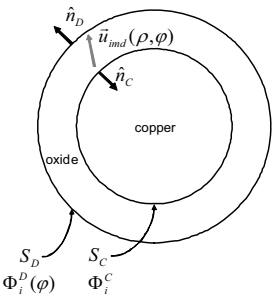


Figure 3. Surfaces, normal vectors, and potentials definitions on conductor (copper) and insulator (oxide) surfaces.

With the above definitions, the modal voltage difference is simplified as follows.

$$\Delta V_{imd} = \begin{cases} +\Phi_i^C - \Phi_{i0}^D & m = 0 \\ -\Phi_{imd}^D & m > 0 \end{cases}. \quad (9)$$

In other words, the modal voltage difference regarding the fundamental mode (m = 0) is the difference between the conductor node voltage and the fundamental voltage on the dielectric boundary. Thus, the excess capacitance C_{imd}^{+} is inserted between the conductor node and the dielectric node that is connected to the fundamental mode coefficient of potential. On the other hand, the modal voltage difference regarding the higher-order modes (m > 0) is just the higher-order modal voltage, so the excess capacitance is connected between ground and the higher-order mode coefficient of potential.

Therefore, the entire equivalent circuit is constructed as shown in Figure 4. The potential on the conductor node (Φ^C) and the fundamental mode potential on the dielectric modes (Φ_0^D) are connected by the circuit elements obtained from the fundamental mode PMBFs. The grounded loops are composed of higher-order capacitances, which represent the charge crowding in the conductor and the insulator regions. Although not shown in Figure 4 for simplicity, other floating loops of higher-order *R-L* networks capture the current crowding (proximity effect) in the conductor.

Figure 4 illustrates the case when the background media is lossless dielectric. Since the lossless dielectric permittivity ($\varepsilon_B > 1$) is generally different from the permittivity of conductor, an additional excess capacitance is included at the conductor impedance network. However, the effect of the excess capacitance is very small in usual frequency range, so we can neglect the capacitance.

When the background dielectric is lossy like silicon, all the capacitive couplings include resistive elements. In the TSV model, the behavior of the combined *R-C* network depends on the complex permittivity model.

Generally, the inductive coupling in the insulator network influences on the voltage drops in the other conductors and dielectrics. However, in case of TSV interconnections, inductive coupling to conductors can be neglected since the directions of polarization currents (in insulator) and conduction currents (in conductor) are orthogonal to each other. Furthermore, the insulator inductance is very small since the insulator geometry has a short current path length and a large area. Therefore, insulator network can be simplified to excess capacitances only.

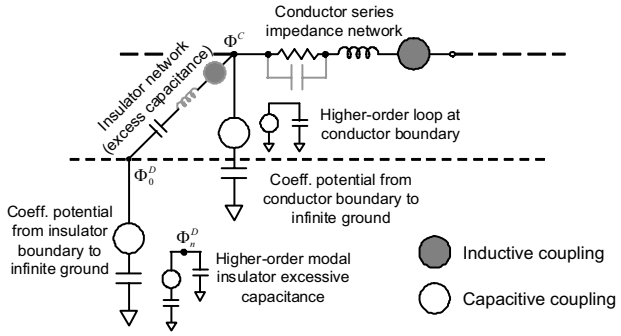


Figure 4. Equivalent circuit model of an inductive cell and a capacitive cell of a TSV interconnection.

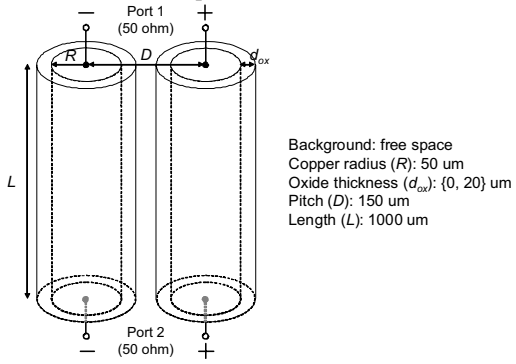
Simulation Results

This section validates the proposed TSV modeling approach with analytic results and simulation results that are correlated with measurements.

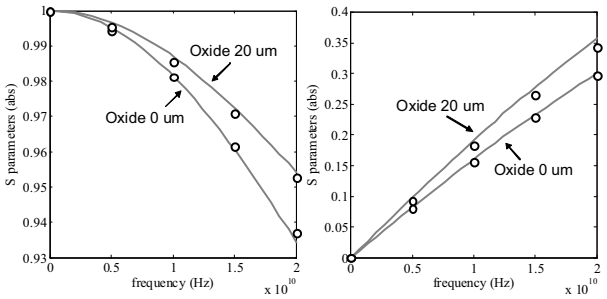
A. Two oxide-coated via interconnections in free space: Figure 5(a) shows the geometry of two oxide-coated cylindrical interconnections. In free space, we can observe the effect of oxide coating on the characteristics of via interconnections by testing the cases with or without the oxide coating. The thickness of oxide is 20 um, which is rather thick compared to the diameter of conductor (100 um).

2-D analytic methods to calculate the capacitance between two parallel conductors can be used to obtain analytic results. When the oxide layer is removed, the problem is reduced to a simple two cylindrical conductor problem, the analytic solution of which is well known [7]. Two parallel cylindrical conductors with annular dielectrics can be calculated by using a conformal mapping technique [8]. For both cases, the p. u. l. inductances are identical because the inductive coupling is not influenced by the oxide coating.

Comparing S-parameter data of the proposed method to the analytic formula in Figure 5(b) shows a good correlation. The addition of the oxide coating modifies the capacitance between two interconnections, so the characteristic impedance is changed. Although the effect of oxide coating on the variation of S-parameters seems small in this example, the effect can be more significant in lossy dielectric surroundings as shown in the next example.



(a) Geometry and electrical configuration



(b) S-parameter results (left: insertion loss, right: return loss, solid lines: analytic transmission line, dots: proposed method)

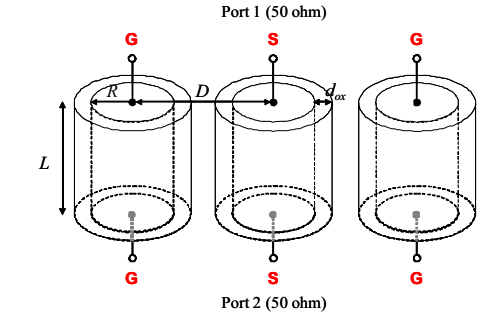
Figure 5. Two via interconnections with oxide coating in free space.

B. Three TSV interconnections: In addition to the oxide coating effect, silicon substrate is a significant factor that determines the electrical behavior of TSV interconnections. In general, the permittivity of doped silicon is expressed as follows [9].

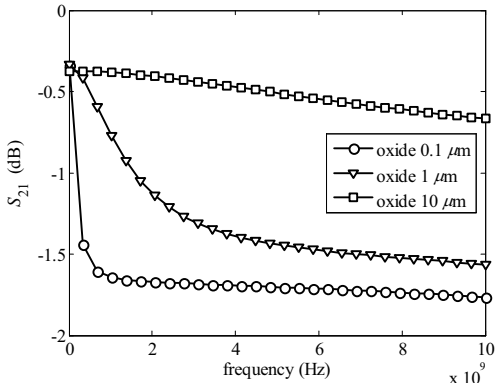
$$\varepsilon_{\mathrm{Si}} = \varepsilon_0 \varepsilon_{\mathrm{Si},i} \left(1 - j \tan\delta - j \frac{\sigma_{\mathrm{Si}}}{\omega \varepsilon_0 \varepsilon_{\mathrm{Si},i}} \right), \qquad (10)$$

where $\varepsilon_{\mathrm{Si},i}$ is dielectric constant (the real part of complex permittivity), $\tan\delta$ is intrinsic loss tangent, and σ_{Si} is the conductivity of silicon. In the following simulations, σ_{Si} is defined as 10 S/m, which is a value of low resistivity silicon made by high-level doping.

The proposed method with the silicon permittivity model is applied for a three-TSV structure shown in Figure 6(a). The original setup of the geometry and electrical configuration can be found in [10], where conductor radius (R) is 50 um, pitch (D) is 150 um, and via length (L) is 100 um. To observe the effect of the oxide thickness (d_{ox}), the values of 0.1, 1, and 10 um are tested. Figure 6(b) shows the insertion losses obtained from the proposed modeling method for three different oxide thicknesses. The frequency-dependent behaviors show the effects of various oxide thicknesses clearly, and they are fairly matched with the 3-D EM simulation results [10]. However, Figure 6(b) shows non-zero losses at DC, which are not shown in measurements. Actually, the offset losses are originated from the use of homogeneous Green's function, which generates leakage currents leading to non-zero DC conductances.



(a) Geometry and electrical configuration



(b) Insertion losses for different oxide thicknesses

Figure 6. Electrical characteristics of three TSV interconnections.

Conclusions

For accurate and efficient modeling of TSV interconnections, this paper proposed a new equivalent circuit model based on integral equations combined with modal basis functions. The main focus was on modeling the effect of oxide coating on vias, the polarization current density distribution in which was captured by using cylindrical PMBFs. The modal excess capacitance of the oxide coating and other inductive and capacitive couplings provide an accurate equivalent model that enables characterizing general multi-TSV structures. The proposed method can be used effectively for the electrical design of the emerging TSV interconnection technology, although the offset losses due to the homogeneous media assumption should be corrected in future work.

Acknowledgments

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