Constant Current Power Transmission Line-Based Power Delivery Network for Single-Ended Signaling

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***Abstract*—The performance of a system depends heavily on the communication speed between integrated circuits. One of the most important bottlenecks that limit the communication speed is simultaneous switching noise (SSN). A major contribution to SSN is return path discontinuities, which are caused by the change or disruption in return currents due to via transitions, aperture effects, etc. In this paper, a new concept based on power transmission line (PTL) is proposed to supply power, improve signal and power integrity, and enhance chip-to-chip communication speed. The first demonstration of constant current PTL (CCPTL)-based single-ended signaling scheme is implemented and measured. The results show that the CCPTL scheme improves the quality of the received signal in terms of voltage and timing margin.**

***Index Terms*—Low noise, power delivery network (PDN), power transmission line (PTL), simultaneous switching noise (SSN).**

I. Introduction

CURRENT transients on the power delivery network (PDN) cause power supply noise. The increasing operating frequency of ICs and the growing power density induce an increase in the amount of transient current drawn from the PDN, contributing to the rising importance of power supply noise [1]–[3]. The power supply noise is a major component of simultaneous switching noise (SSN) in high-speed systems, which can cause functional failures or incorrect bits to be transmitted and received [3].

Most PDNs in high-speed systems consist of power and ground planes to provide a low-impedance path between the voltage regulator module (VRM) and the IC on the printed circuit board (PCB). For off-chip signaling, charging and discharging signal transmission lines induce return currents on the power and ground planes. The return current always follows the path of least impedance on the reference plane closest to the signal transmission line [3]. The return current path plays a critical role in maintaining the signal integrity of the bits propagating on the signal transmission lines.

As described in [4] and [5], interruption in the return current path leads to return path discontinuities (RPDs). This occurs due to via transitions, apertures on the power/ground planes, or split planes, to name a few [4]–[10]. Even when signal lines are referenced to a continuous plane, RPDs can be induced during either the low-to-high or high-to-low transitions of the driver [6]. In all of these RPDs, excessive voltage fluctuation can occur between the power and ground planes due to the cavity modes in the structure. These cavity modes can degrade the signal integrity of the waveform, as described in [4]. The current solution to this problem is the use of decoupling capacitors or shorting vias at the RPD locations [11]–[16], or the use of new technologies with thin dielectrics between the power and ground planes [17]–[20]. These are often times expensive solutions.

In this paper, we propose a new solution that can reduce the layer count, remove the effect of cavity modes, and help eliminate the decoupling capacitors for mitigating RPDs. This solution is based on the power transmission line (PTL) concept [21]. In this approach, transmission lines replace the power plane to convey power from the VRM to each IC on the PCB, and, hence, are called as PTLs. The PTL-based PDN enables both power and signal transmission lines to be referenced to the same ground plane so that a continuous current path can be achieved as shown in Fig. 1(c), unlike with the power-plane-based PDN as shown in Fig. 1(a) and (b). When a power plane is used as a reference conductor as shown in Fig. 1(a), the I/O driver and termination circuitry induce an RPD even with a solid reference conductor underneath the signal transmission line. The displacement current at the RPD location induces supply voltage fluctuation. The RPD effect becomes even more severe when the switching frequency of the I/O driver coincides with the cavity resonant frequency of the power/ground plane pair, resulting in the degraded waveform at the receiver. Since the RPDs are induced by a disruption between the power and ground planes, using a ground plane as a reference conductor does not resolve the problem, as shown in Fig. 1(b). However, using PTLs and eliminating the power plane allow for closed current loops by sharing the reference conductor with signal lines, and therefore remove the RPD effects, as shown in Fig. 1(c).

Though using PTLs solves the RPD issue, it generates other problems such as 1) output-data-dependent dc drop on the PDN due to the terminating resistance; 2) mismatch effect between the PTL and the termination; 3) line congestion; and 4) increased power consumption. First, the state of the output data dictates whether the output driver draws current from the PDN or not, resulting in the fluctuation of the dc level on the PTL. Second, using transmission lines can cause impedance mismatch in PTLs due to manufacturing variation. Third, if one PTL is used per I/O driver, the number of lines on the PCB doubles and causes congestion. Finally, as the signaling scheme and the I/O driver

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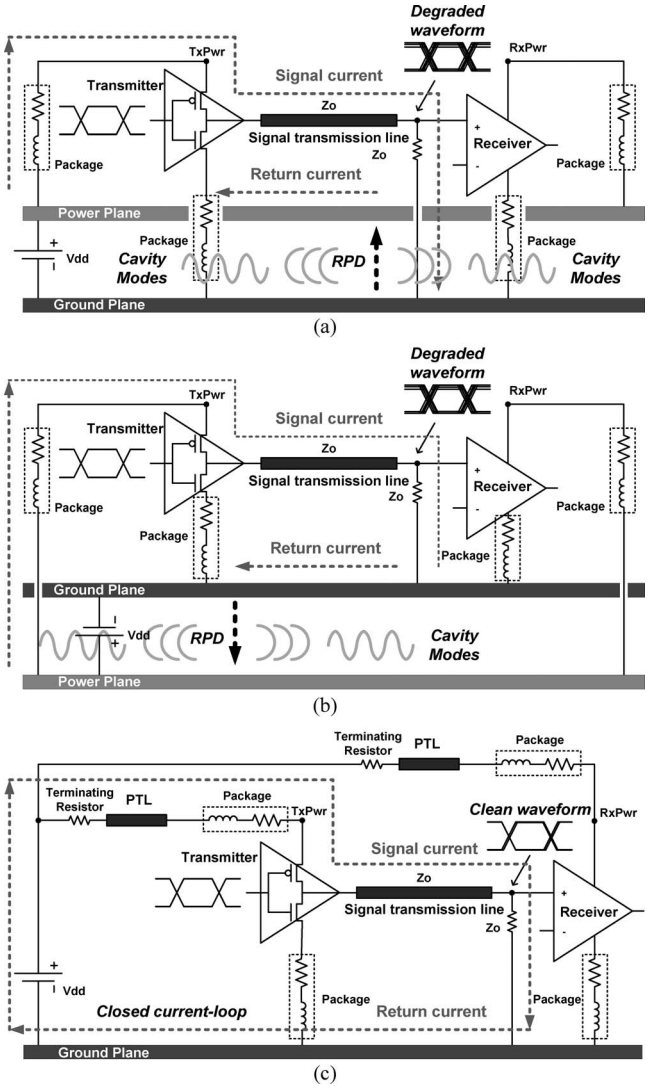


Fig. 1. Chip-to-chip communication. (a) Plane-based with a power plane as a reference conductor. (b) Plane-based with a ground plane as a reference conductor. (c) PTL-based with a ground plane as a reference conductor.

are adjusted to accommodate the new PDN, the required power to transmit 1 bit of data changes, requiring careful analysis of the power consumption. To make the PTL feasible in a realistic environment, these issues need to be addressed first, which is the focus of this paper. In this paper, early results on the constant current PTL (CCPTL) scheme [22] have been discussed along with the measurements. The CCPTL scheme severs the link between the current flowing through the PTL and the output data of the I/O driver connected to it. Also, it eliminates the charging and discharging process of the PTL, thereby completely eliminating power supply noise in idealistic situations.

In this paper, proof of concept for the CCPTL signaling scheme is presented using test vehicles. Two types of test boards were fabricated: one with a power plane and the other with a PTL. An off-the-shelf device was mounted on each board to function as an I/O driver. Time domain measurements have been made of the eye diagram at the receiver side after the signal travels a distance of 2.6 in along the transmission line. The measurement results show that the CCPTL scheme improves the quality of the received signal significantly in terms of voltage and timing margin.

The rest of this paper is organized as follows. In Section 2, the PTL and CCPTL signaling schemes are discussed. In Section 3, the test vehicle details are provided along with modeling and simulation results. In Section 4, the measurement results are discussed along with correlation with simulation, followed by the conclusion in Section 5.

II. Power Transmission Line

Planes are generally used to supply power from the VRM to the IC due to their high-frequency characteristics and low dc drop related issues. To accommodate return current paths for multiple signal traces in the board or package, either ground or voltage plane is used as the reference conductor. However, voltage and ground plane pairs can contribute to RPDs, which can cause detrimental effects on signal integrity [4]. Therefore, decoupling capacitors are required to mitigate the RPD effects.

In the proposed PDN scheme in this paper, transmission lines are used to replace the voltage plane and convey power from the VRM to the die, which are called as PTLs. The characteristic impedance of the PTL is decided based on the characteristic impedance of the signal transmission line, the desired eye height at the receiver side, the turn-on impedance of the I/O driver, to name a few. As the characteristic impedance of the signal transmission line is typically between 25 and 70 Ω, that of the PTL also falls within this range. Hence, the PTL concept enables the use of a high impedance network for power delivery, which is in direct contrast to the method being currently pursued. In this paper, the impedance of the PTL used is around 25 Ω.

The PTL-based signaling scheme is shown in Fig. 2. In Fig. 2(a), the PTL is source terminated with a resistor of 25 Ω matched impedance. The reason for the source termination of the PTL is to prevent multiple reflections when there is an impedance mismatch between the signal transmission line and load-terminating resistor. The other end of the PTL is connected to a signal network, which consists of an I/O driver, a signal transmission line, and a terminating resistor. The impedance of the signal network is carefully designed, considering the PTL impedance and the desired eye height. The PTL and signal transmission lines are referenced to a common ground plane, thereby eliminating RPDs during both transitions of the driver.

An issue that arises with the PTL-based signaling scheme is dynamic dc drop due to the terminating resistance between the voltage supply and the PTL. The state of the output data dictates whether the I/O driver draws current from the PDN or not. In the case of a voltage-mode driver and ground-tied termination, the high state of the output data induces current to flow from the PDN toward the signal transmission line, while the low state of the output data stops the current flow. Thus, only during the high state, dc drop occurs on the PDN, and a fraction of the original supply voltage appears on the power supply node (TxPwr) of the I/O driver. This is illustrated in Fig. 2(b). As the characteristic impedance of the signal transmission line is 50 Ω, the turn-on impedance of the I/O driver is designed to be 25 Ω so as to have

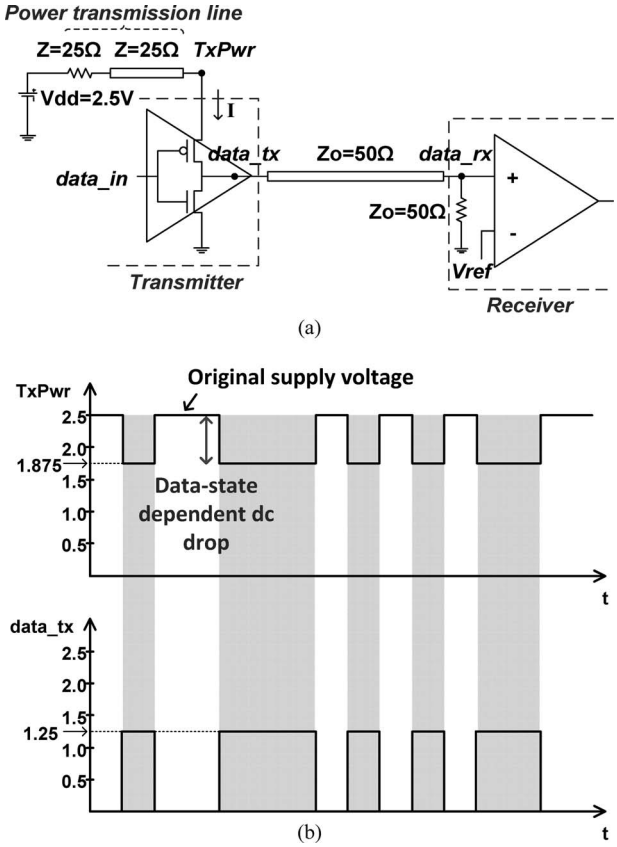


Fig. 2. Single-ended signaling using PTL. (a) Schematic. (b) Waveform.

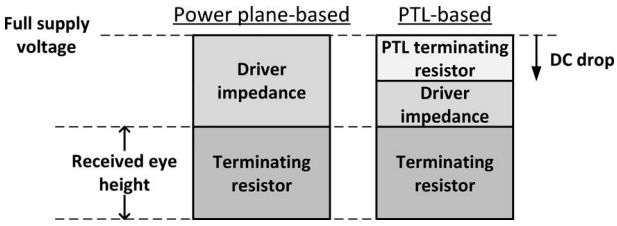


Fig. 3. Comparison of supply voltage division.

the amplitude of the output data equal to one-half of the supply voltage. The dc voltage level at the power supply node (TxPwr) of the I/O driver alternates between the original supply voltage and a fraction of the original supply voltage, depending on the data state at the output node (data_tx), as shown in Fig. 2(b).

The dc drop on the PDN during the high state of the output data is different from SSN. It is data state dependent, while SSN is data transition dependent. In other words, the dc drop is due to the resistive element, while SSN is mainly due to the inductive element. It is interesting to note that the dc drop does not affect the amplitude of the received data as illustrated in Fig. 3. When a power plane is used as the I/O PDN, the turn-on impedance of the I/O driver is typically matched to the signal transmission line, which is terminated with the impedance-matching resistor at the far end. Hence, the output voltage swing is one-half of the supply voltage. This impedance matching scheme cannot be applied to the PTL-based I/O PDN because using a PTL requires a source termination. The intervention of the PTL-terminating resistance can be compensated by reducing the turn-on impedance of the I/O driver. When the sum of the PTL-terminating resistance and the turn-on impedance of the I/O driver is matched to the signal transmission line, the received eye height can be maintained to be one-half of the supply voltage.

However, the dynamic dc drop shown in Fig. 2 can create problems if combined with the impedance mismatch in the PTL-based circuit, which comes from manufacturing variations. This can create signal-integrity-related issues, as shown in Fig. 4. When the PTL and terminating resistor are mismatched by 20% as shown in Fig. 4(a), the PTL is underdriven. Moreover, the balance of impedance between the PTL and the signal network is upset. Depending on the reflection coefficient, the reflection back and forth within the PTL continues until the steady-state voltage is reached. These multiple reflections induce a staircase-step waveform at the power supply node (TxPwr) of the driver and signal overshoot at the output node (data_tx), as shown in Fig. 4(a) [22], [23].

The issue due to the dynamic dc drop gets even more complicated when one PTL is used to serve multiple I/O drivers. If one PTL is used to support multiple I/O drivers, the power supply nodes of the drivers need to be tied together, which results in varying current through the PTL based on the data pattern. This affects the dc voltage level at the common power supply node and the amplitude of the transmitted and received signal waveforms. In Fig. 4(b), a PTL is used to feed power to two I/O drivers. The power supply node of each driver is connected to the same PTL. Since the output data of the two drivers are independent of each other, there are three possible data patterns in terms of the number of 1s, namely 00, 01/10, and 11. The three possible combinations result in three different amounts of current through the PTL, which leads to three different dc voltage levels on the PDN (TxPwr), and three different amplitudes of the output data pattern (data1_tx, data2_tx, data1_rx, and data2_rx). Therefore, the PTL-based power distribution scheme needs to be modified to eliminate the data-state-dependent dc drop.

The CCPTL scheme resolves the two issues related to the PTL, namely dynamic dc drop on the PDN caused by the source termination and the mismatch effect between the PTL and the terminating resistor. The varying dc drop shown in Figs. 3 and 4 are due to the current flowing through the PTL only during the high state of the output data. To maintain the dc voltage level constant, a current path is required during the low state of the data. In the CCPTL scheme, an additional current path from power to ground is supplemented using a data pattern detector and dummy path, as shown in Fig. 5(a). The data pattern detector detects the state of the input data. It then determines whether to connect or disconnect the dummy path to the PTL. The dummy path is a resistive path whose impedance is matched with that of the signal path so as to induce the same amount of current during the low state as during the high state of the data. It can be implemented with transistors whose width and length are optimized to yield the desired resistance. As a result, the dc voltage level at the power supply node (TxPwr) of the driver remains constant regardless of the output data state, as shown in

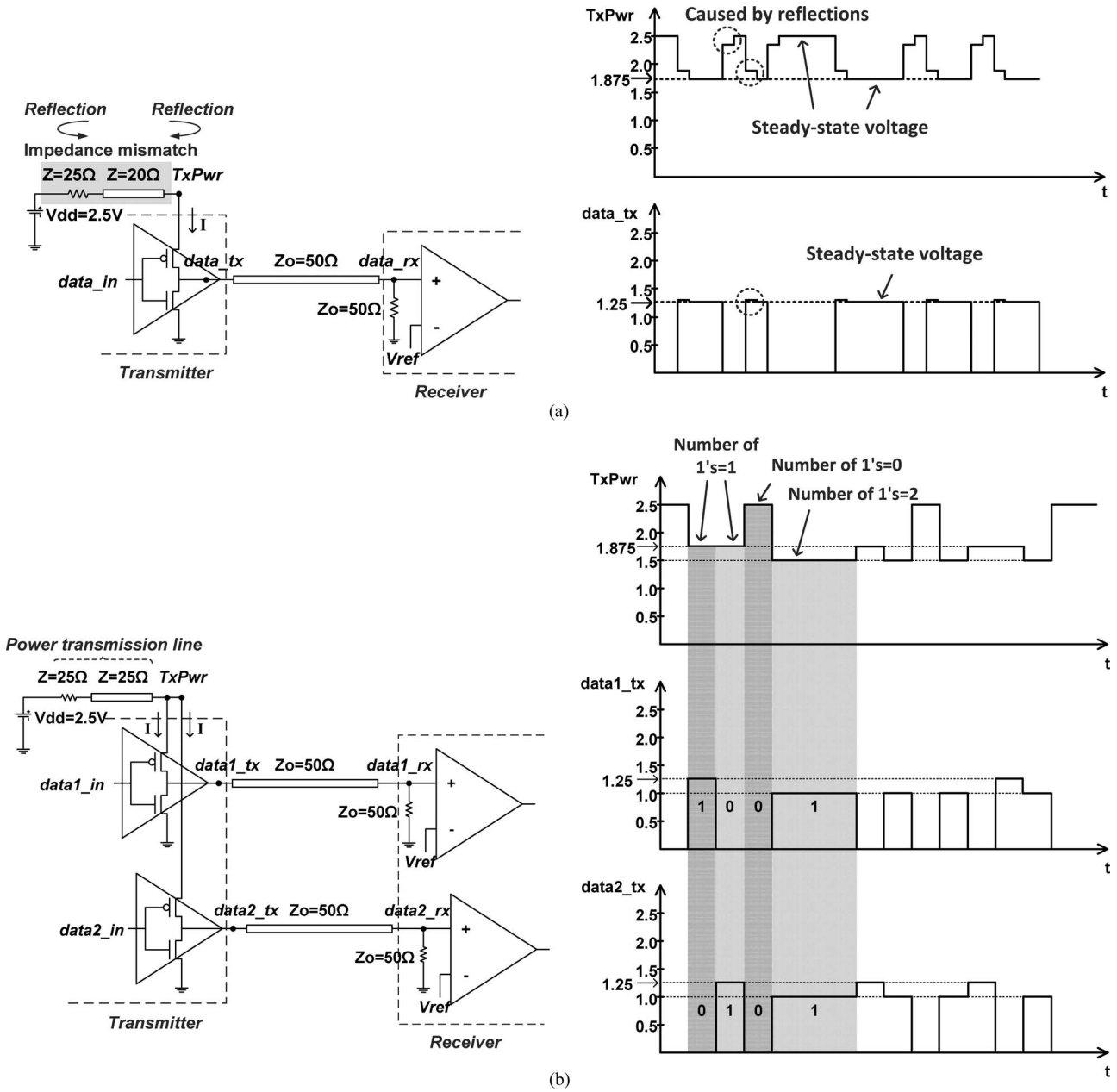


Fig. 4. Issues with PTL-based signaling scheme. (a) Impedance mismatch in PTL. (b) Two I/O drivers per PTL.

Fig. 5(b). The dc drop due to the PTL-terminating resistor can be compensated either by reducing the turn-on impedance of the output driver or by increasing the supply voltage. Then, the dc drop at the power supply node (TxPwr) does not reduce the eye height of the transmitted/received signal. Between the two compensation methods, the latter is used during measurements, which will be discussed in a later section.

The constant current through the PTL eliminates the repeated charging and discharging of the PTL. It, therefore, keeps the PTL always fully charged so that the voltage on the line at a given time can be assumed to be the same at all points, which excludes the possibility of any impedance mismatch. Consequently, the mismatch effect will not appear on the signal line even when there is an impedance mismatch in the PTL. Even with a 20% impedance mismatch between the PTL and the termination, the dc voltage level at the power supply node (TxPwr) and the amplitude of the signal waveform at the output node (data_tx) maintain the steady-state voltages, resulting in the same waveform as Fig. 5(b).

The application of the CCPTL scheme can be extended to support multiple I/O drivers. To feed power to multiple I/O drivers with one CCPTL, a data pattern detector and multiple dummy paths can be used. When the power supply nodes of multiple I/O drivers are tied together, the amount of current through the PTL varies based on the data pattern. Therefore, the number of dummy paths needs to be equal to the number of possible data patterns. For example, if two I/O drivers are being driven by one PTL as shown in Fig. 6, there are three

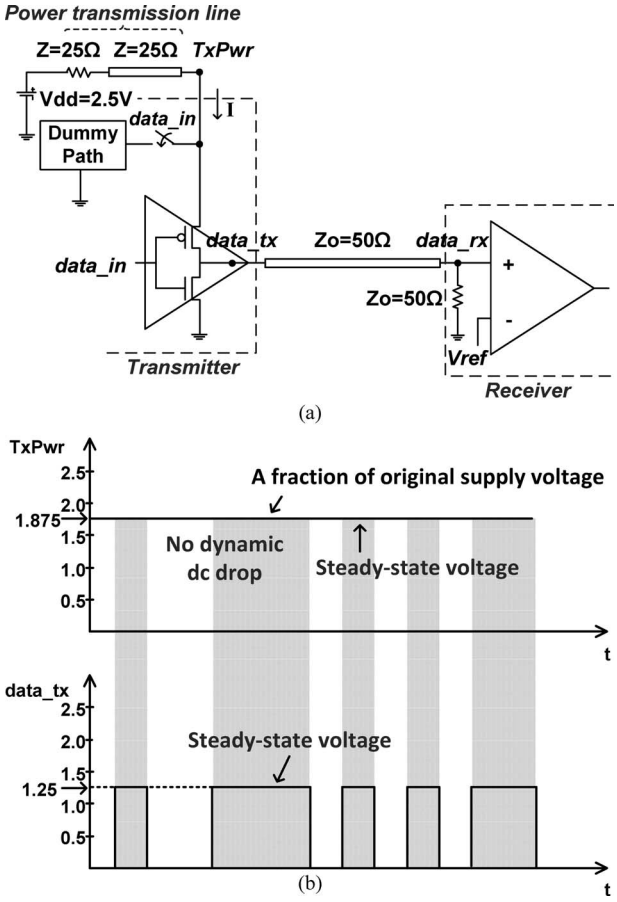


Fig. 5. Single-ended signaling using CCPTL. (a) Schematic. (b) Waveform.

possible data patterns: the number of turned-on drivers can be from 0 to 2. The maximum PDN current will be drawn by the drivers when all the drivers are turned ON with all the output data being high, while no current will flow when all the drivers are turned OFFF with all the output data being low. The data pattern detector detects the number of turned-off drivers and enables the corresponding dummy paths to carry currents from the PDN, as shown in Fig. 6. As a result, the total amount of current drawn from the PDN by either the drivers or the dummy paths will be kept constant regardless of the data pattern.

The advantages of the CCPTL signaling scheme include reduction of layer counts and elimination of decoupling capacitors for mitigating RPDs, which lead to lower cost. Also, this scheme provides increased voltage and timing margins that enable the enhancement of the channel data rate. However, potential disadvantages using the presented scheme are increased power consumption and circuit area, which are associated with inducing constant current in the power distribution network. If the PTL is being source terminated, the dc drop due to the terminating resistance should then be compensated either by reducing the turn-on impedance of the output driver or by increasing the power supply level.

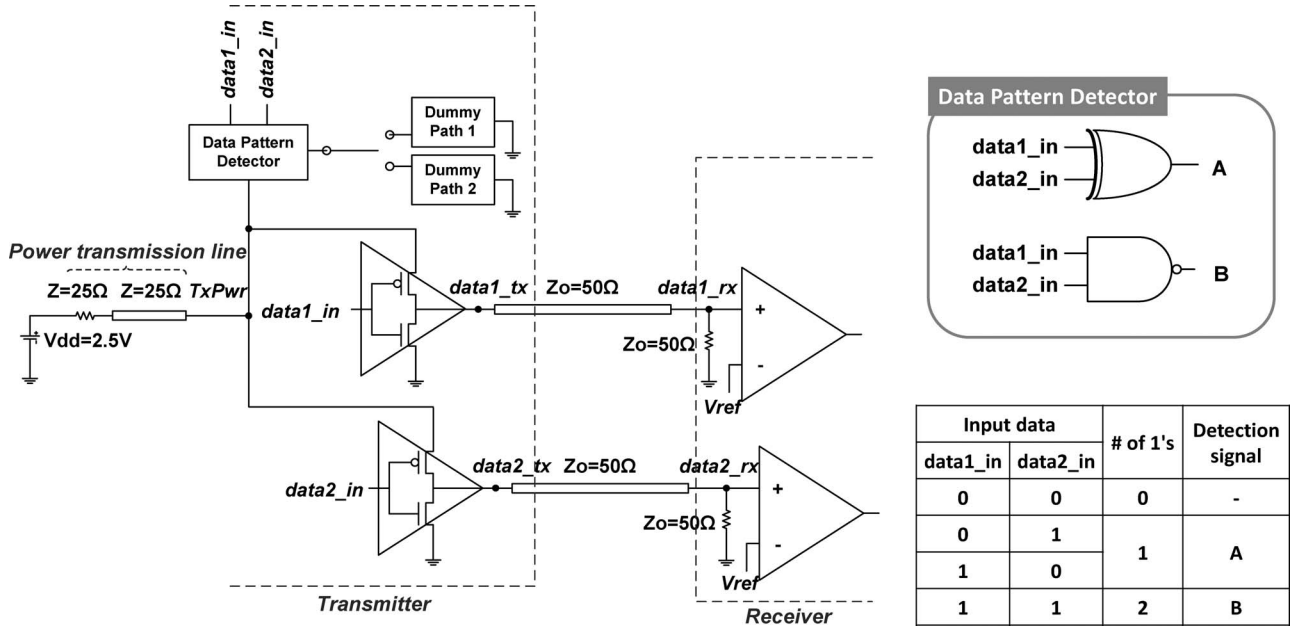
It is important to note that if the same concept is extended to differential signaling, most of these limitations can be resolved because the two complementary signals in differential signaling draw constant current from the PDN by construction. In differential signaling, a natural dummy path is created in the process of transmitting a pair of complementary data bits. However, it doubles the off-chip PCB trace count and the I/O pin count. The focus of this paper is on improving signal integrity for single-ended signaling and, therefore, includes only the simulation and measurement results of the CCPTL-based single-ended signaling scheme.

III. Test Vehicle Design and Modeling

Two test vehicles were designed and fabricated to explore the impact of RPDs on signal integrity in the power-plane-based PDN and to demonstrate the efficacy of the PTL-based PDN. Two test boards were custom designed to incorporate two different PDNs, and an off-the-shelf chip was mounted on each board. A 16-pin QFN-packaged SiGe differential driver was used. For a differential output pin pair, one output pin was connected to a 2.6-in-long signal transmission line. The signal transmission line was terminated inside the oscilloscope with 50 Ω. The other output pin was directly connected to a 50 Ω resistor to function as a dummy path outside the chip. During the high state of the output data, current flows along the signal transmission line, while during the low state of the output data, the dummy path draws the same amount of current. Therefore, constant current flows through the PDN in both the power-plane-based and PTL-based test vehicles at all times. Although the power-plane-based PDN does not require a dummy path, the dummy path is still implemented to have all the setup the same between the two test vehicles except for the PDN. SubMiniature version A (SMA) connectors were used to support wide bandwidth for input and output signals.

The top views of the power-plane-based board and the PTL-based board are shown in Fig. 7. The width and length of the power and ground planes are 3.8 and 2.5 in, respectively. For the PTL-based test vehicle, a 25 Ω transmission line was used as a PTL, and a 25 Ω resistor was used as a source-terminating resistor. The source termination of the PTL is used to reduce the possibility of multiple reflections if the first reflection is initiated by the impedance mismatch between the signal transmission line and the load-terminating resistor. The ground plane serves as a reference conductor for the PTL as well as for the signal transmission line. The only difference between the two test vehicles is the method used to provide power to the driver.

The stack-up details of the test boards are shown in Fig. 8. Copper and FR4 are used for the metal and dielectric layers. The conductivity of copper was assumed to be 5.8×10^7 S/m. The dielectric constant and loss tangent of FR4 were 4.6 and 0.025, respectively. The power-plane-based board consists of four layers, which are signal-power-ground-signal layers. On the other hand, the PTL-based board consists of three layers, which are signal/power-ground-signal layers, having both signal and power transmission lines on the top layer. It is important to note that in both boards, the signal transmission line and other connections were placed on the top signal layer, while the bottom signal layer was nearly empty with only a couple of lines



Input data		# of 1's	Detection signal
data1_in	data2_in		
0	0	0	-
0	1	1	A
1	0		
1	1	2	B

Fig. 6. Schematic of two I/O drivers per CCPTL.

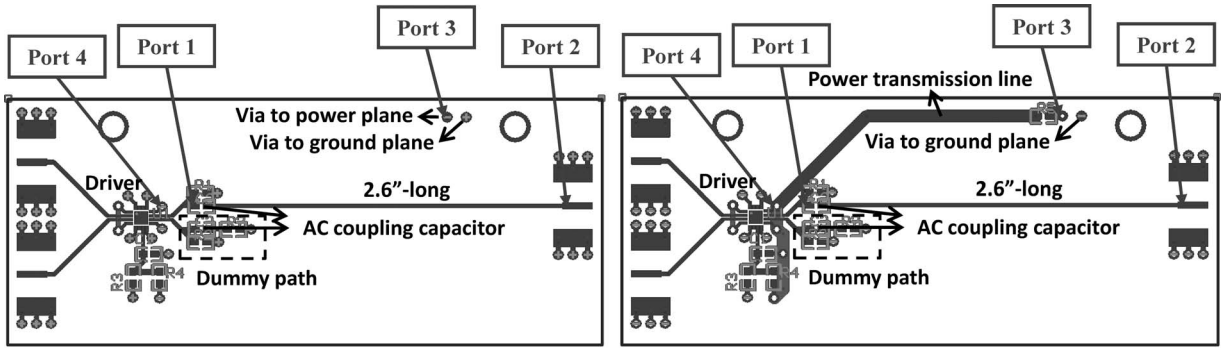


Fig. 7. Top view of test vehicles. (a) Plane-based test vehicle. (b) PTL-based test vehicle.

connecting to control and power pins. The lines placed on the bottom layer are also shown in Fig. 7.

In the power-plane-based test vehicle, a cavity is formed between the power and ground planes. The resonant frequency of the structure can be calculated, based on the rectangular waveguide formula defined by

$$f_{\text{resonant}} = \frac{c}{2\sqrt{\varepsilon_r \mu_r}} \sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2} \qquad (1)$$

where "c" is the speed of light, "a" and "b" are the width and length of the rectangular structure, respectively, "m" and "n" are the integers to represent the dominant mode number, and ε_r and μ_r are the relative permittivity and the relative permeability of the substrate [3]. The first half wavelength ($\lambda/2$) resonance of the plane pair occurs at 724.6 MHz. The first four resonant frequencies are summarized in Table I.

Sphinx [24], a multilayer finite difference method [3] based electromagnetic solver, was used to model the two test vehicles in frequency domain and compare the insertion losses of the signal transmission lines of the two test vehicles. Here, the insertion loss (IL) is defined as $\text{IL} = -20\log_{10}|S_{21}|\text{dB}$, when Port 1 and Port 2 are at the input and output of the signal transmission line, respectively, using the same reference impedance of 50 Ω. Four ports were defined for each structure, two for the signal line (Port 1 and Port2 at input and output, respectively), and the other two for the PDN, as shown in Figs. 7 and 8. The reference used for all the ports was the ground plane.

TABLE I
CALCULATED RESONANT FREQUENCY

w (inch)	l (inch)	m	n	$f_{\lambda/2}$ (Hz)
3.8	2.5	1	0	7.2459E+08
		0	1	1.1014E+09
		2	0	1.4492E+09
		2	1	1.8202E+09

The ILs of the signal transmission lines in the two test vehicles are compared in Fig. 9. The IL of the PTL-based test vehicle has

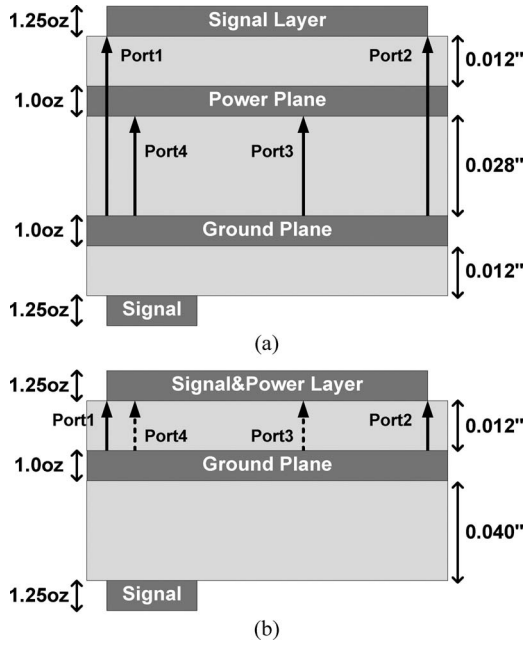


Fig. 8. Side view of test vehicles. (a) Plane-based test vehicle. (b) PTL-based test vehicle.

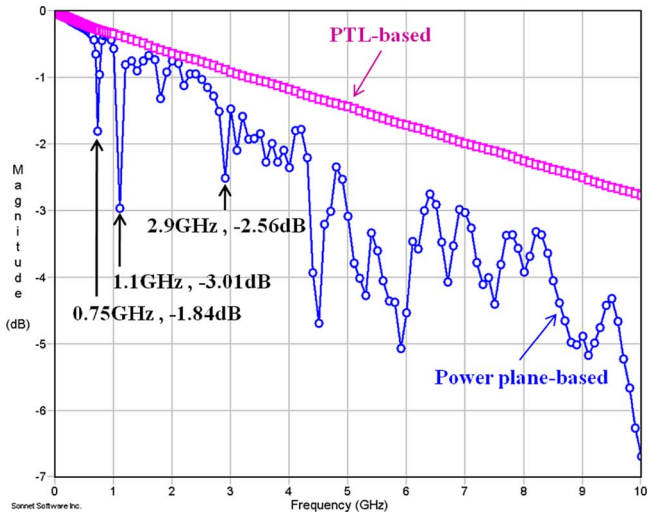


Fig. 9. Insertion loss of a signal transmission line with plane-based PDN and PTL-based PDN.

a smooth negative slope with -2.77 dB IL at 10 GHz. This behavior is expected of a microstrip line with the main contributor to IL being conductor and dielectric loss. On the other hand, the IL of the signal line in the power-plane-based test vehicle has multiple resonances. The first dip in the IL appears at 750 MHz. This frequency corresponds to the $\lambda/2$ resonant frequency of the plane pair. The rest of the dips shown in Fig. 9 are consistent with the resonant frequencies shown in Table I. The reason that the resonant frequencies of the signal line correspond to the cutoff frequencies of the cavity modes is because those resonances are induced by the coupling between the signal line and the PDN [25]. Therefore, the transmission characteristic of the signal line suffers from nonmonotonic variation over frequency, which can create problems for signal integrity. The resonances also cause rapid increase in the IL reaching -6.69 dB at 10 GHz.

For time-domain analysis, the frequency samples in the 4×4 scattering matrix of the test vehicle need to be converted into a simulation program with integrated circuit emphasis (SPICE)-compatible equivalent circuit. This is important when modeling the coupling between the signal-power network to include the nonlinear effects of the driver/receiver circuitry and their effects on signal and power integrity [4]. A macromodeling tool, IdEM Plus [26], was used to create a macromodel and SPICE netlist from Sphinx's frequency domain response. By using the macromodel, passivity and causality were guaranteed using data certification procedures provided in IdEM Plus, as described in [4]. The frequency response of the macromodel is compared with the original IL data from Sphinx in terms of magnitude in Fig. 10, which shows good agreement for both test vehicles. As shown in Fig. 11, good agreement is also observed between the phase data from Sphinx and the macromodel for both test vehicles. Only the comparison between the Sphinx data and the macromodel for the IL is shown in Figs. 10 and 11, though a macromodel for the 4×4 matrix was constructed using IdEM Plus, which includes return loss effects as well.

The SPICE simulation setup with the macromodel is shown in Fig. 12. Ports 1 and 2 represent the input and output of the signal line, while Ports 3 and 4 represent ports on the PDN, respectively. A complementary pair of 2^7-1 pseudorandom bit stream (PRBS) data was applied to the differential driver as inputs. One output pin of the driver was connected to Port 1 of the macromodel, and the load termination was connected to Port 2. The other output pin was connected to a 50 Ω resistor, which functions as the dummy path as described earlier. The dc voltage was supplied to Port 3, and the power pin $V_{\rm DD}$ of the driver was connected to Port 4. CMOS transistors were used to operate as the voltage-mode driver. The I/O buffer information specification (IBIS) model of the device was not used due to its incapability of handling power supply noise [27], and therefore, a 0.28 μm CMOS process was used to replicate the behavior of the device. The widths of the transistors were tuned so as to match the output waveform of the CMOS driver with that of the IBIS model as the ideal power and ground were supplied. The simulation setup in Fig. 12 incorporates the electromagnetic behavior of the test board, the nonlinear characteristic of the I/O driver, and the passive components. The data rate of 1500 Mb/s was used to excite the cavity resonance in the plane-based test vehicle.

The resulting eye diagrams at the receiver end (Port 2) for the two test vehicles are compared in Fig. 13. The eye diagram shown in Fig. 13(a) is when the ideal power and ground supply was applied, which serves as a baseline. The eye diagram in Fig. 13(b) shows the result when the power/ground plane pair is used as the I/O PDN. The voltage and timing margin has been reduced due to power supply noise. The eye height and eye width are 353 mV and 626 ps, respectively, which are reduced by 29.5% and 2% as compared to the baseline. Fig. 13(c) shows the eye diagram of the received data when the PTL is used as the power supply path. The eye height and width are 488 mV and 640 ps, respectively, which are similar to Fig. 13(a). The

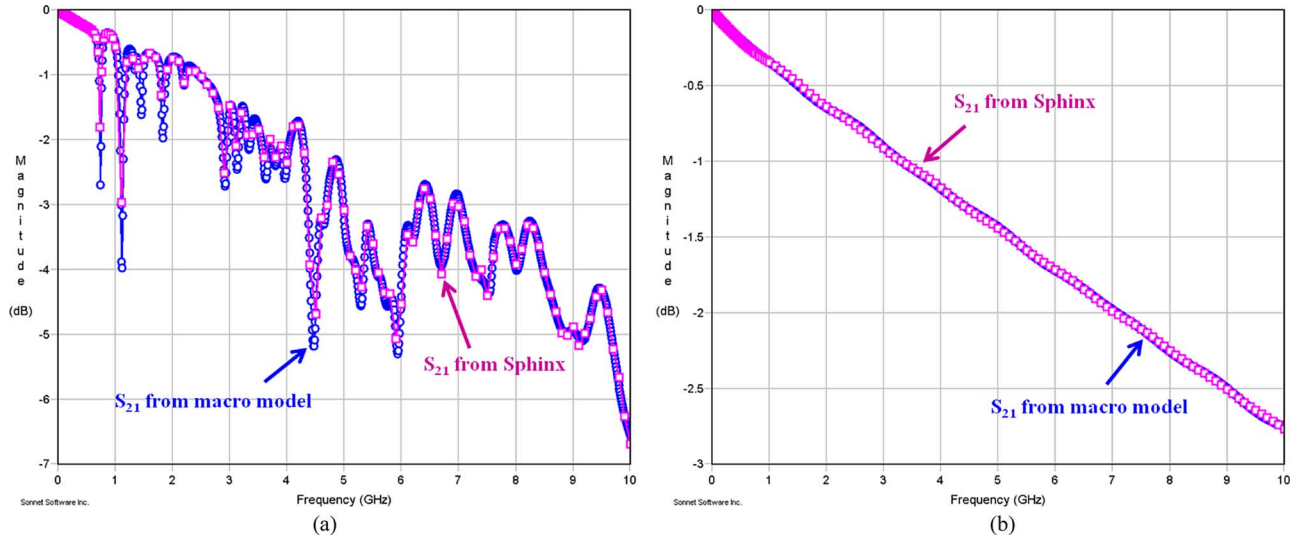


Fig. 10. Comparison of magnitude of IL from Sphinx and macromodel. (a) Power-plane-based test vehicle. (b) PTL-based test vehicle.

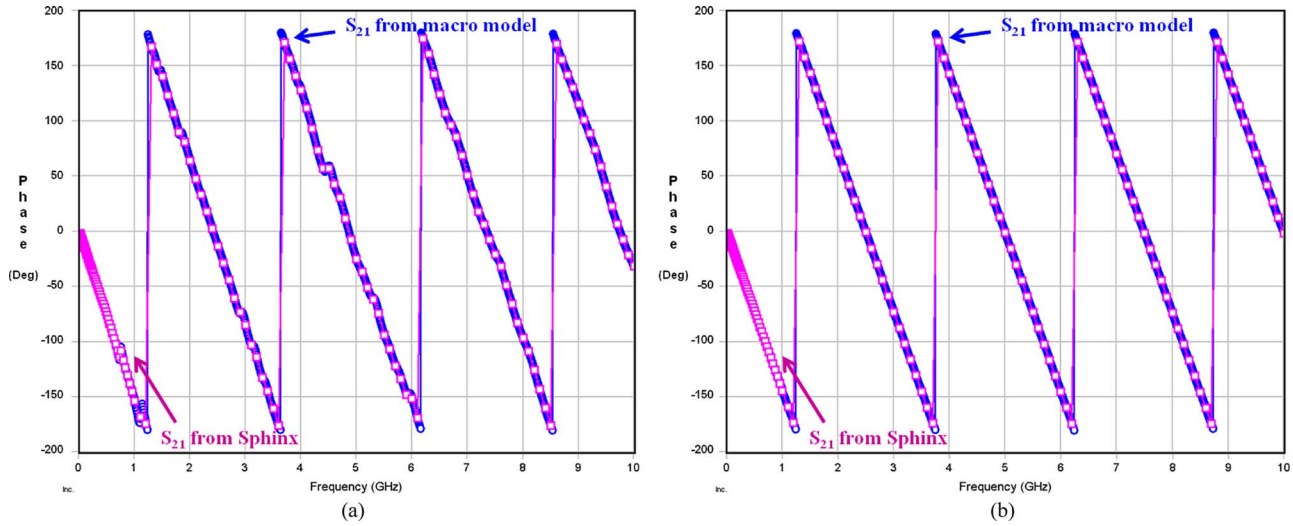


Fig. 11. Comparison of phase of IL from Sphinx and macromodel. (a) Power-plane-based. (b) PTL-based test vehicle.

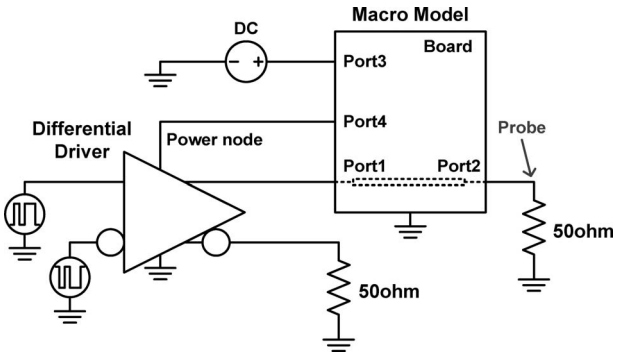


Fig. 12. SPICE simulation setup with a macromodel.

eye height is reduced by only 2.6% as compared to the baseline, and the eye width is 1 ps larger. The simulation setup did not include the package model of the chip and the discontinuities due to SMA connectors, cables, and oscilloscope. Therefore, the measurement results can be worse than the simulation results in terms of voltage and timing margin. However, the simulation does show a trend and indicates the advantage of using a PTL for power distribution.

The test vehicle with an ac coupling capacitor added between the output of the driver and the signal transmission line was simulated as well. The ac coupling capacitor is generally used to suppress the dc current flow and to provide a bias for the oscilloscope. The SPICE simulation setup with the ac coupling capacitor is shown in Fig. 14. One output pin of the driver was connected to Port 1 of the macromodel through a 0.1 μF capacitor. The other output pin was connected to a 0.1 μF capacitor and 50 Ω resistor in series to function as a dummy path outside the chip. The rest of the setup was kept identical to Fig. 12.

The resulting eye diagrams at the receiver end (Port 2) are compared in Fig. 15. The eye diagram shown in Fig. 15(a) is the result when the ideal power and ground supply was applied,

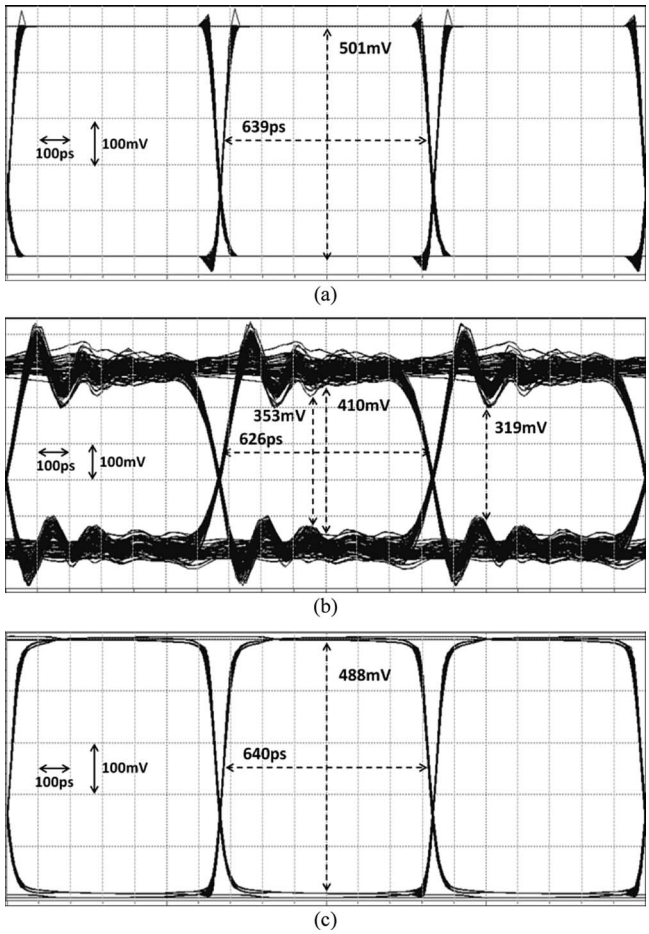


Fig. 13. Simulated eye diagrams of the received 1500 Mb/s PRBS. (a) Ideal power supply. (b) Plane-based PDN. and (c) PTL-based PDN.

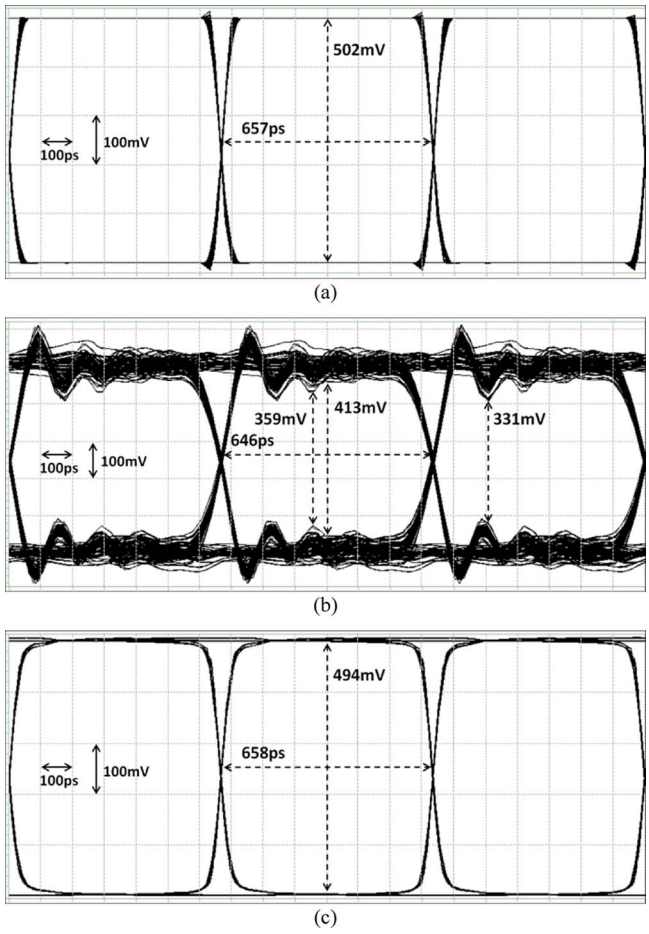


Fig. 15. Simulated eye diagrams of the received 1500 Mb/s PRBS when ac coupling capacitors are added. (a) Ideal power supply. (b) Plane-based PDN. (c) PTL-based PDN.

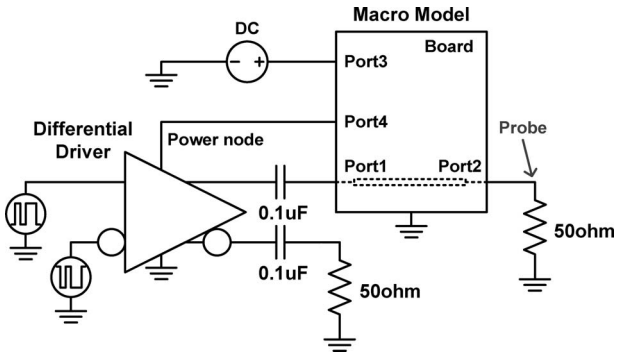


Fig. 14. SPICE simulation setup with ac coupling capacitors.

which serves as a baseline. Fig. 15(b) and (c) shows the eye diagrams of the received output data in the power-plane-based and PTL-based test vehicles, respectively. With the inclusion of the ac coupling capacitor, the transition crossing point has become closer to 50% of the eye height, which improves the eye width. The eye height and eye width in Fig. 15(b) are 359 mV and 646 ps, respectively, which are reduced by 28.5% and 1.7% as compared to the baseline. The eye height and eye width in Fig. 15(c) are 494 mV and 658 ps, respectively. The eye height is reduced by only 1.6% as compared to the baseline, and the eye width is 1 ps larger.

The PTL-based PDN outperforms the power-plane-based PDN in terms of voltage and timing margins with and without the ac coupling capacitor between the output of the driver and the signal transmission line. The performance improvement is mainly coming from the removal of RPDs by using the PTL. Since the dummy path is replicating the signal network during the low state of the output data, the sum of ac and dc currents is maintained the same regardless of the inclusion of ac coupling capacitors in both the test vehicles. As a result, the ac coupling capacitor does not disturb the function of the CCPTL signaling scheme.

IV. Measurements and Correlation

Fig. 16 shows the test environment and measurement setup along with the port locations from Fig. 7. Agilent 81133 A was used to generate a 2^7-1 PRBS pattern at the desired frequency. A supply voltage of 2.5 V was used for the power-plane-based test vehicle, while 3.98 V was used for the PTL-based test vehicle. Due to the source termination of the PTL, a dc drop occurs across the resistor. Since it causes the device to be supplied with

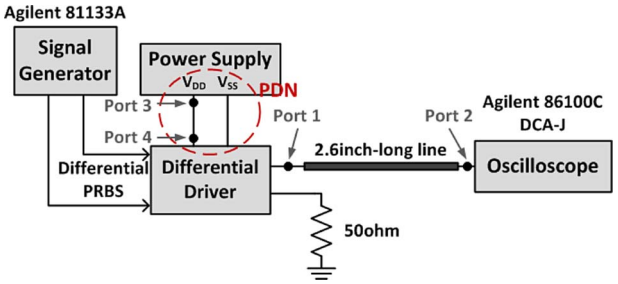


Fig. 16. Test environment.

less voltage than the original supply voltage, the dc drop should be compensated either by reducing the turn-on impedance of the output driver or by increasing the supply voltage to maintain the same voltage level at the device and the receiver side as in the power-plane-based test vehicle. The limitation of the off-the-shelf chip precluded the former method so the latter method was used.

The drivers of both test vehicles were excited with a 1500 Mb/s differential PRBS pattern. The fundamental frequency of the 1500 Mb/s PRBS pattern coincided with the resonant frequency of the signal line in the plane-based test vehicle. Eye diagrams were measured at the output of the transmission line (Port 2) after the signal traveled a distance of 2.6 in along the transmission line, using Agilent 86100 C DCA-J oscilloscope. To maintain consistency, 10 000 samples were used to construct the eye diagram. Two types of jitters were measured using the oscilloscope, namely the RMS jitter and the peak-to-peak (p-p) jitter. The RMS jitter utilizes all the 10 000 samples for calculation. Assuming that the mean is 0, the RMS jitter quantifies the standard deviation of the jitter distribution. This number is more meaningful compared to the p-p jitter which is the distance between the two farthest data points. However, since the jitter is mainly caused by power supply noise, its distribution can be non-Gaussian. In such a case, the p-p jitter is more useful. Hence, both jitters are presented in this paper.

Fig. 17 shows the eye diagram of a 1500 Mb/s PRBS at the receiver side in each test vehicle. Fig. 17(a) is the eye diagram of the signal generator output, and Fig. 17(b) and (c) is the eye diagrams at the receiver side in the power-plane-based and PTL-based test vehicles, respectively. The output of the signal generator has an initial p-p jitter of 19.1 ps. The p-p jitter increases to 36 ps in the power-plane-based test vehicle, while it increases to 27 ps in the PTL-based test vehicle. The difference between the p-p jitters in the two test vehicles is 9 ps, which is a reduction of 25% for the PTL-based test vehicle. The eye height is ~463 mV in the power-plane-based test vehicle, and ~523 mV in the PTL-based test vehicle, which shows an improvement of 13.0%.

In Table II, the measured eye diagrams at 1500 Mb/s are compared to the simulation results in terms of voltage and timing window. Good agreement is observed for the eye height between the measurement and simulation results. The measured eye heights are 11.4% and 6.7% larger than the simulated eye heights in the power-plane-based and PTL-based test vehicles,

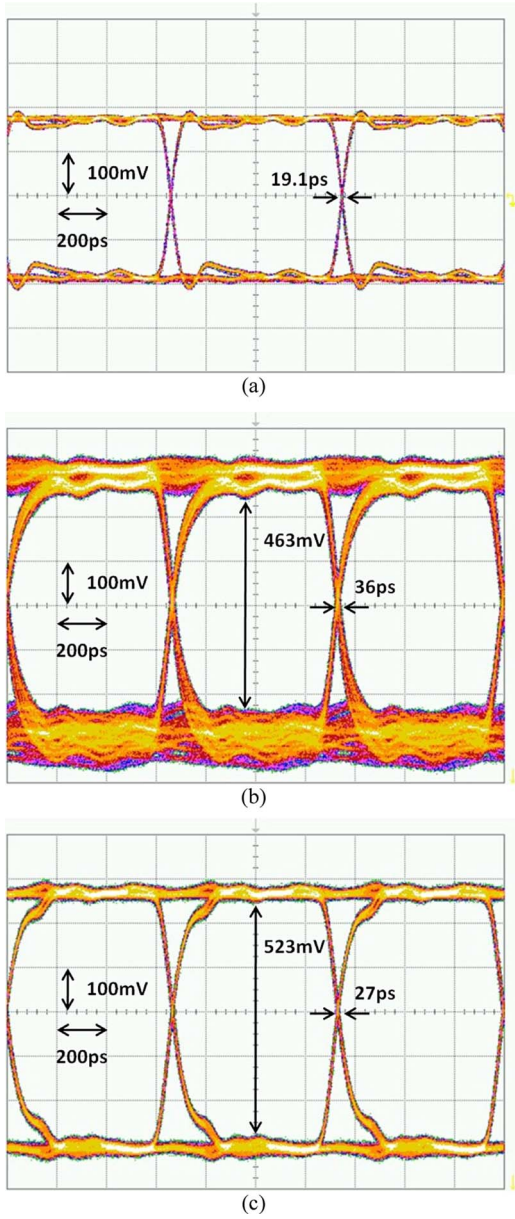


Fig. 17. Measured eye diagrams of the received 1500 Mb/s PRBS. (a) Signal generator. (b) Power-plane-based PDN. (c) PTL-based PDN.

TABLE II
COMPARISON OF EYE OPENING FROM SIMULATION AND MEASUREMENT

1500Mbps PRBS	Eye height (mV)		P-P Jitter (ps)	
	Simulation	Measurement	Simulation	Measurement
Power Plane	410	463	40.67	36
PTL	488	523	26.67	27

respectively. This discrepancy can be attributed to manufacturing variation of the stack-up dimensions and the material properties. As the thickness and dielectric constant between the power and ground planes have an influence on the power supply noise, the variation can generate unexpected positive or negative deviation. The p-p jitter from simulation is greater than the p-p jitter

from measurement by 4.67 ps in the plane-based test vehicle. In the PTL-based test vehicle, the simulated p-p jitter and the measured jitter are different by less than 1ps. The simulation results have provided almost the same or larger p-p jitter as compared to the measurement results. The reason for this is due to the discrepancy between the actual device used in the measurement and the driver model used in the simulation. The IBIS model of the device could not be used due to its inability to incorporate power supply noise [27], and therefore, the impact of the power supply noise on the signal quality could not be simulated using the IBIS model. Therefore, the device was substituted with a CMOS inverter, which was tuned to generate the same output waveform as the device's IBIS model when ideal power and ground were used. As a result, discrepancies occur between the model and measurements as the supply voltage fluctuates at the power and ground terminals of the driver. In the simulation, the duty cycle of the resulting waveform was less than 50%, which led to the increased p-p jitter. However, the simulation results capture the improvement in eye opening and signal integrity by using the PTL scheme, similar to the measurement results.

When 3.98 V was used as the supply voltage for the PTL-based test vehicle, the dc voltage level at the power pin of the chip equaled 2.498 V, which matches the supply voltage provided to the device in the power-plane-based test vehicle. The increased voltage level for the PTL-based test vehicle raises the power consumption as compared to the plane-based test vehicle. As 3.98 V is 59.2% larger than 2.5 V, the power consumption is 59.2% higher. Here, the amount of current drawn from the PDN is the same in both test vehicles so as to result in the same eye height at the load end in idealistic situations. Thus, the additional power consumption comes from the increase in the power supply voltage level.

The power consumption issue can be resolved by reducing the turn-on impedance of the I/O driver by custom-designing the CCPTL scheme, or by eliminating the source termination of the PTL. Unless the turn-on impedance of the I/O driver is reduced, the source termination of the PTL requires the increase in the supply voltage level to get the same current level through the signal network as that in the plane-based test vehicle, which leads to the increased power consumption. Since the source termination of the PTL is used to prevent multiple reflections as mentioned in the previous section, it can be removed if the load-terminating resistor is matched well to the characteristic impedance of the signal transmission line.

In Fig. 18, the received eye diagram of the PTL-based test vehicle without the source termination is compared to that of the power-plane-based test vehicle. Without the source-terminating resistor, no compensation for the dc drop across the PTL is required so that 2.5 V is used as the supply voltage in the PTL-based test vehicle as well as in the plane-based test vehicle. Thus, the same amount of power is consumed in both test vehicles. The difference between the p-p jitters in the two test vehicles is 9 ps, which is a reduction of 25% for the PTL-based test vehicle. The eye height is ∼463 mV in the power-plane-based test vehicle, and ∼546 mV in the PTL-based test vehicle, which shows an improvement of 17.9%.

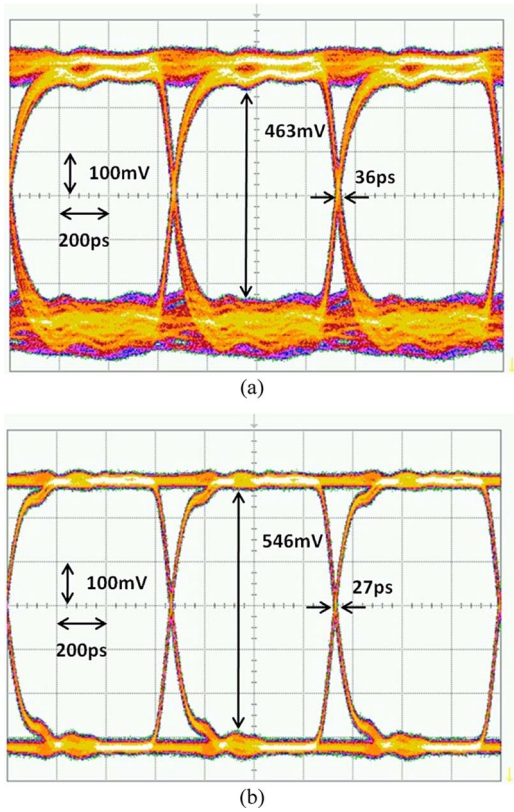
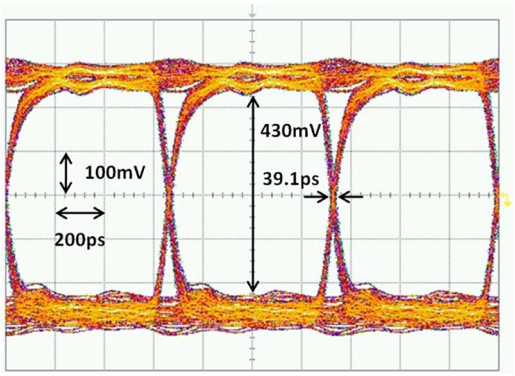


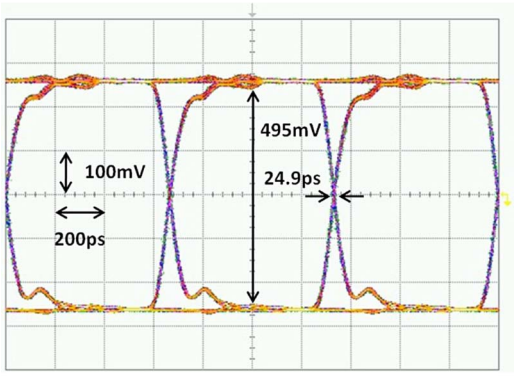
Fig. 18. Measured eye diagrams of the received 1500 Mb/s PRBS. (a) Power-plane-based PDN. (b) PTL-based PDN without source termination.

As compared to Fig. 17, the eye height of the PTL-based test vehicle is increased after removing the source termination from 523 to 546 mV. This is because the impedance mismatch between the signal transmission line and load-terminating resistor was negligible, thereby minimizing reflections. Also, even though constant current is being drawn from the PDN, current fluctuations are inevitable during data transition. The dc drop over the source-terminating resistor then fluctuates, thereby inducing noise on the power rail. As a result, the PTL without the source termination has better power integrity, increasing the eye height by 4.4%. However, even with the source termination, the fluctuation of the power rail is still far less than the SSN-induced supply noise in the plane-based test vehicle. It is important to note that the source termination is instrumental in preventing multiple reflections and ensuring signal integrity due to manufacturing variations, which can cause impedance mismatch at the load.

To reduce the increment in the power supply voltage level when using the source termination, an ac coupling capacitor of 0.1 μF was added between the output of the driver and the signal transmission line. Using an ac coupling capacitor also provides a bias for the oscilloscope without giving a separate dc offset. A 0.1 μF capacitor was also added to the dummy path to replicate the signal network. As a result, the dc current flow was suppressed and the signals became dc-balanced. The required supply voltage level for the PTL-based test vehicle was reduced from 3.98 V to 3.47 V after the inclusion of the ac coupling



(a)



(b)

Fig. 19. Measured eye diagrams of the received 1500 Mb/s PRBS with ac coupling capacitors. (a) Power-plane-based PDN. (b) PTL-based PDN.

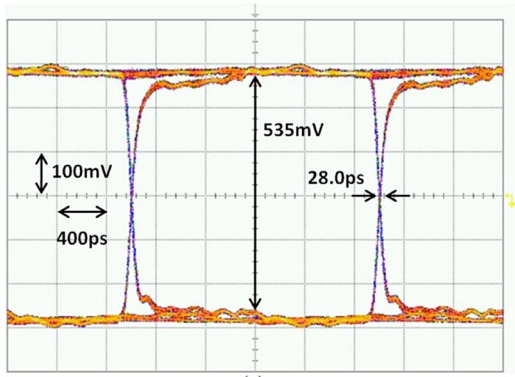
TABLE III
COMPARISON OF EYE OPENING FROM SIMULATION AND MEASUREMENT WITH AC COUPLING CAPACITORS

1500Mbps PRBS	Eye height (mV)		P-P Jitter (ps)	
	Simulation	Measurement	Simulation	Measurement
Power Plane	413	430	20.67	39.1
PTL	494	495	8.67	24.9

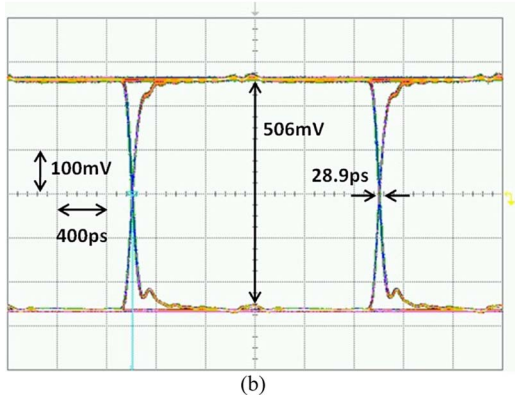
capacitor. As 3.47 V is 38.8% larger than 2.5 V, the power consumption is also 38.8% higher.

Fig. 19 shows the eye diagrams at the receiver side when ac coupling capacitors were added to the signal path and the dummy path in both test vehicles. Fig. 19(a) and (b) is the eye diagrams of the received 1500 Mb/s PRBS in the power-plane-based and PTL-based test vehicles, respectively. The output of the signal generator has an initial p-p jitter of 19.1 ps, as shown in Fig. 17(a). The p-p jitter increases to 39.1 ps in the power-plane-based test vehicle, while it increases to 24.9 ps in the PTL-based test vehicle. The difference between the p-p jitters in the two test vehicles is 14.2 ps, which is a reduction of ∼36.3% for the PTL-based test vehicle. The eye height is ∼430 mV in the power-plane-based test vehicle, and ∼495 mV in the PTL-based test vehicle, which shows an improvement of 15.1%.

In Table III, the measured eye openings at 1500 Mb/s are compared to the simulation results. Good agreement is observed for

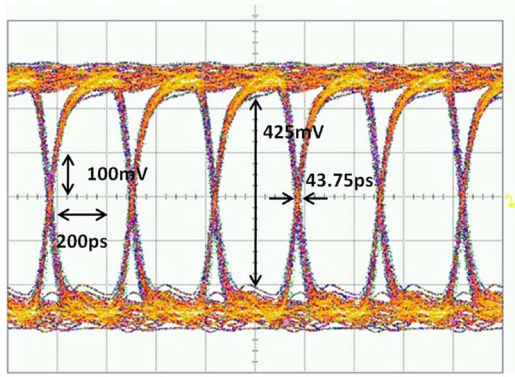


(a)

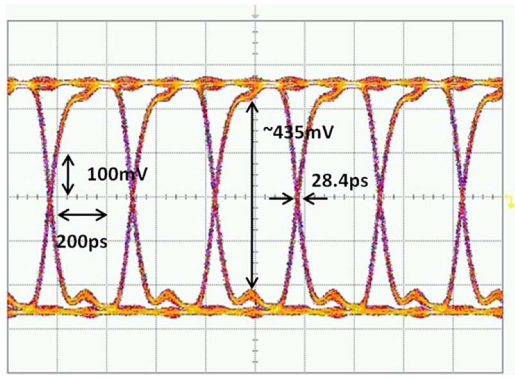


(b)

Fig. 20. Measured eye diagrams of the received 500 Mb/s PRBS with ac coupling capacitors. (a) Power-plane-based PDN. (b) PTL-based PDN.



(a)



(b)

Fig. 21. Measured eye diagrams of the received 3000 Mb/s PRBS with ac coupling capacitors. (a) Power-plane-based PDN. (b) PTL-based PDN.

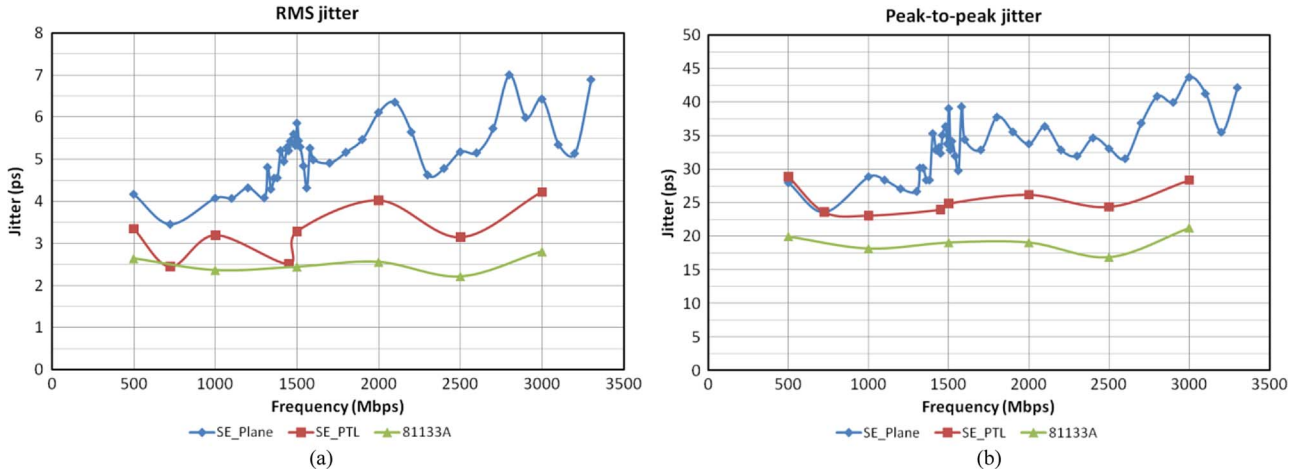


Fig. 22. Jitter variation over frequency. (a) RMS jitter. (b) Peak-to-peak jitter.

the eye height between the measurement and simulation results. The small discrepancy between the measured and simulated eye heights can be attributed to the manufacturing variations in material properties and physical dimensions, and the difference in the number of samples used to construct the eye diagrams. In terms of p-p jitter, since the PRBS patterns used in the simulations do not include source jitter, the simulated jitters cannot be directly compared to the measured jitters. Here, a rough estimation can be made by adding the signal generator jitter of 19.1 ps to the simulated jitters. For the power-plane-based test vehicle, the estimated jitter is the sum of 19.1 ps and 20.67 ps, which is 39.77 ps. This jitter value closely matches the measured jitter with an error of 1.7%. For the CCPTL-based test vehicle, the estimated jitter is 27.77 ps, which approximates the measured jitter of 24.9 ps with an error of 11.5%. Although it is not completely accurate to add the two p-p jitters, which are composed of deterministic jitter and random jitter, arithmetically, it gives a rough estimation. To sum up, the simulation results reasonably capture the improvement in performance by using the CCPTL scheme, which is verified by the measured eye diagrams.

To explore the impact of power supply noise on signal integrity under different data rates, the input data rate was swept from 500 to 3200 Mb/s in steps of 500 Mb/s for the PTL-based test vehicle, and in steps of 100 Mb/s for the plane-based test vehicle. From 1300 to 1600 Mb/s, a data rate step of 20 Mb/s was used to examine the jitter variation around the first resonant frequency of the plane-based test vehicle closely. Starting from 500 Mb/s at which the plane-based PDN does not resonate, the eye openings at the receiver sides in both test vehicles are almost the same, as shown in Fig. 20. The eye height of the plane-based test vehicle is larger by 5.4% as compared to that of the PTL-based test vehicle. The p-p jitters of the two test vehicles are different by only 0.9 ps.

The highest p-p jitter appeared at 3000 Mb/s, as shown in Fig. 21. The eye height is ∼425 mV in the power-plane-based test vehicle, and ∼435 mV in the PTL-based test vehicle, which is an improvement of ∼2.4%. The p-p jitter is 43.75 and 28.4 ps in the power plane- and PTL-based test vehicles, respectively, which is a reduction of ∼35%.

TABLE IV
SUMMARY OF MEASURED JITTERS WITH AC COUPLING CAPACITORS

Data rate (Mbps)	RMS jitter (ps)			Peak-to-peak jitter (ps)		
	Plane	PTL	Reduction	Plane	PTL	Reduction
500	4.17	3.35	-	28	28.9	-
1449	5.20	2.52	51.5%	32.4	24.0	25.9%
1500	5.85	3.28	43.9%	39.1	24.9	36.3%
3000	6.43	4.22	34.4%	43.75	28.4	35.1%

The RMS and p-p jitters at various data rates are shown in Fig. 22(a) and (b), respectively. The jitter is plotted along the y-axis, while the data rate is plotted along the x-axis, which bands from 500 to 3000 Mb/s. The line with triangular marker connects the varying jitters of the direct output of the signal generator (Agilent 81133 A). The line with rectangular marker (SE_PTL) and the line with circular marker (SE_Plane) indicate the jitters of the PTL-based and plane-based test vehicles, respectively. Both RMS and p-p jitters of the PTL-based test vehicle have relatively monotonic behavior, whereas those of the plane-based test vehicle have nonmonotonic behavior, similar to the IL of the signal line in the plane-based test vehicle.

The fundamental frequencies (one-half of the data rate) at which the jitter peaks coincide with the calculated resonant frequencies are shown in Table I. The first local maximum jitter appears at 1500 Mb/s, which concurs with the first resonant frequency predicted from the frequency-domain modeling. The RMS and p-p jitter at 500, 1449, 1500, and 3000 Mb/s are summarized in Table IV. The measurement results show that the PTL is effective in reducing the jitter and increasing the timing margin.

V. Conclusion

The first demonstration of the CCPTL-based signaling scheme has been implemented and measured in this paper. Using a PTL resolves the RPD issue, which is the main source of SSN in packages and PCBs. The CCPTL scheme addresses the dynamic dc drop on the power supply network. By adding a dummy path in parallel with the driver, constant current is induced, and it removes the dynamic dc drop along with the charging and discharging process of the PTL during signal transitions. Therefore, the CCPTL scheme is able to deliver noise-free power supply to the IC in idealistic situations, and reduces the layer count. To explore the efficacy of the CCPTL scheme, two test vehicles were fabricated. Off-the-shelf chips were mounted on the custom-designed test boards, one with a power plane and the other with a PTL. Over data rates ranging from 500 Mb/s to 3 Gb/s, eye diagrams were measured at the far end of the 2.6-in-long transmission line. The results show that the PTL improves the quality of the received signal in terms of voltage and timing margin. In terms of correlation, the local maximum jitter appeared at the frequencies where the plane pair was expected to resonate based on the simulation and calculations. The time-domain simulation showed the trend of signal integrity improvement by using the PTL, which was verified using measurements.

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References

[1] N. H. Khan, S. M. Alam, and S. Hassoun, "System-level comparison of power delivery design for 2D and 3D ICs," in *Proc. 3D Sys. Integr. Conf.*, Sep. 2009, pp. 1–7.

[2] M. Wang and J. Hu, "Power delivery network optimization for laptop and desktop computer platforms," presented at the DesignCon, Santa Clara, CA, 2010.

[3] M. Swaminathan and A. E. Engin, *Power Integrity Modeling and Design for Semiconductor and Systems*. Englewood Cliffs, NJ: Prentice-Hall, 2007.

[4] M. Swaminathan, D. Chung, S. Grivet-Talocia, K. Bharath, V. Laddha, and J. Xie, "Designing and modeling for power integrity," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 2, pp. 288–310, May 2010.

[5] I. Ndip, F. Ohnimus, K. Lobbicke, M. Bierwirth, C. Tschoban, S. Guttowski, H. Reichl, K.-D. Lang, and H. Henke, "Modeling, quantification, and reduction of the impact of uncontrolled return currents of vias transiting multilayered packages and boards," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 2, pp. 421–435, May 2010.

[6] S. Chun, M. Swaminathan, L. D. Smith, J. Srinivasan, and Z. Jin, "Modeling of simultaneous switching noise in high speed systems," *IEEE Trans. Adv. Packag.*, vol. 24, no. 2, pp. 132–142, May 2001.

[7] Q. Chen and J. Zhao, "Via and return path discontinuity impact on high speed digital signal quality," in *Proc. Electr. Perform. Electron. Packag.*, Oct. 2000, pp. 215–218.

[8] A. E. Engin, M. Coenen, H. Koehne, G. Sommer, and W. John, "Modeling and analysis of the return path discontinuity caused by vias using the 3-conductor model," in *Proc. Int. Symp. Electromagnetic Compatibility*, May 2003, pp. 1110–1113.

[9] J. Kim, J. Pak, J. Park, and H. Kim, "Noise generation, coupling, isolation, and EM radiation in high-speed package and PCB," in *Proc. Int. Symp. Circuits Syst.*, May 2005, pp. 5766–5769.

[10] C.-T. Wu, G.-H. Shiue, S.-M. Lin, and R.-B. Wu, "Composite effects of reflections and ground bounce for signal line through a split power plane," *IEEE Trans. Adv. Packag.*, vol. 25, no. 2, pp. 297–301, May 2002.

[11] W. Cui, X. Ye, B. Archambeault, D. White, M. Li, and L. J. Drewniak, "EMI resulting from a signal via transition through DC power bus—Effectiveness of local SMT decoupling," in *Proc. Asia-Pacific Conf. Environ. Electromagn.*, May 2000, pp. 91–95.

[12] W. Cui, X. Ye, B. Archambeault, D. White, M. Li, and J. L. Drewniak, "EMI resulting from signal via transitions through the DC power bus," in *Proc. Int. Symp. Electromagnetic Compatibility*, vol. 2, Aug. 2000, pp. 821–826.

[13] M. Pajovic, J. Yu, Z. Potocnik, and A. Bhobe, "GHz-range analysis of impedance profile and cavity resonances in multilayered PCBs," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 1, pp. 179–188, Feb. 2010.

[14] X.-X. Wang and D.-L. Su, "The Influence of power/ground resonance to via's SSN noise coupling in multilayer package and three mitigating ways," in *Proc. Int. Conf. Electron. Mater. Packag.*, Dec. 2006, pp. 1–5.

[15] I. Ndip, H. Reichl, and S. Guttowski, "A novel methodology for defining the boundaries of geometrical discontinuities in electronic packages," in *Proc. Ph.D. Research. Microelectron. Electron. Conf.*, Jun. 2006, pp. 193–196.

[16] C.-Y. Jin, C.-H. Chou, D.-R. Li, and T.-Y. Chuang, "Improving signal integrity by optimal design of power/ground plane stack-up structure," in *Proc. Elecron. Packag. Tech. Conf.*, Dec. 2006, pp. 853–859.

[17] P. Muthana, M. Swaminathan, E. Engin, P. Markondeya Raj, and R. Tummala, "Mid frequency decoupling using embedded decoupling capacitors," in *Proc. Electr. Perform. Electron. Packag.*, Oct. 2005, pp. 271–274.

[18] C. Scogna, "Suppression of simultaneous switching noise in power and ground plane pairs," *Conformity*, vol. 12, no. 6, pp. 36–43, Jun. 2007.

[19] I. Novak, "Lossy power distribution networks with thin dielectric layers and/or thin conductive layers," *IEEE Trans. Adv. Packag.*, vol. 23, no. 3, pp. 353–360, Aug. 2000.

[20] J. M. Hobbs, H. Windlass, V. Sundaram, S. Chun, G. E. White, M. Swaminathan, and R. R. Tummala, "Simultaneous switching noise suppression for high speed systems using embedded decoupling," in *Proc. Electron. Compon. Technol. Conf.*, May 2001, pp. 339–343.

[21] A. E. Engin and M. Swaminathan, "Power transmission lines: A new interconnect design to eliminate simultaneous switching noise," in *Proc. Electron. Compon. Technol. Conf.*, May 2008, pp. 1139–1143.

[22] S. Huh, D. Chung, and M. Swaminathan, "Achieving near zero SSN power delivery networks by eliminating power planes and using constant current power transmission lines," in *Proc. Electr. Perform. Electron. Packag.*, Oct. 2009, pp. 17–20.

[23] S. H. Hall, G. W. Hall, and J. A. McCall, *High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices*, 1st ed., New York: Wiley-IEEE Press, 2000.

[24] Sphinx V2.5. (2010). E-System Design. [Online]. Available: http://www.e-systemdesign.com/

[25] V. Laddha and M. Swaminathan, "Correlation of PDN impedance with jitter and voltage margin for high speed channels," in *Proc. Electr. Perform. Electron. Packag.*, Oct. 2008, pp. 73–76.

[26] IdEM R2009a. (2009). [Online]. Available: www.idemworks.com

[27] A. Varma, M. Steer, and P. Franzon, "Improving behavioral IO buffer modeling based on IBIS," *IEEE Trans. Adv. Packag.*, vol. 31, no. 4, pp. 711–721, Nov. 2008.

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