Abstract—Signal and power integrity are crucial for ensuring high performance in high-speed digital systems. As the operating frequency of digital systems increases, the power and ground bounce created by simultaneous switching noise (SSN) has become a limiting factor for the performance of these devices. SSN is caused by parasitic inductance that exists in the power delivery network (PDN), and voltage fluctuations on the power and ground rails can lead to reduced noise margins and can limit the maximum frequency of a digital device. A new PDN design has been suggested that achieves significantly reduced SSN [1] by replacing the power plane structure with a power transmission line (PTL). In this paper, a new power delivery scheme is shown to significantly reduce switching noise at lower power. This concept has been demonstrated through theory, simulation, and measurements.

Keywords—power delivery network; simultaneous switching noise; power transmission line

I. INTRODUCTION

The rapid increase in data rates and transistor density in digital integrated circuits (ICs) introduces significant challenges for signal and power integrity. A critical problem in these areas is switching noise due to the high current transients of digital devices. Most power delivery networks (PDNs) in digital systems utilize power and ground planes, as this provides a low-impedance path between the system power supply and the power pin of an IC on the PCB. As signal currents flow from the transmitters to the receivers, corresponding return currents are created traveling in the opposite direction on the reference plane. The return current always follows the path of least impedance on the reference plane closest to the signal transmission line in order to form a closed current loop. However, the return current can be disrupted by via transitions, apertures on power/ground layers, or split planes [3]. Disruptions in the current return loop induce parasitic inductance on the PDN, and coupled with large current transients, this can lead to simultaneous switching noise that adversely affects the signal quality [4]. A common solution to this problem is to add large decoupling capacitors between the power and ground planes to suppress voltage fluctuations across parasitic inductance, as well as to ensure current continuity.

To combat the SSN problem, a new I/O signaling scheme is proposed and tested. This solution is based on the power transmission line (PTL) concept [1], in which a transmission line is used in place of a power plane to transfer power from the VRM to an IC on the PCB. The PTL-based PDN allows both power and signal transmission lines to be referenced to the same ground plane so that a continuous current loop is established, and therefore removes return path discontinuity (RPD) effects [2].

While using PTLs helps solve the RPD issue, it presents additional difficulties. One such issue that arises with the PTL-based signaling scheme is dynamic dc drop due to the terminating resistance between the voltage supply and the PTL [2]. The state of the output data dictates how much current the I/O drivers draw from the PDN. In the case of a voltage-mode driver, the high state of the output data induces current to flow from the PDN toward the signal transmission line, while the low state of the output data draws much less current. Thus, the DC drop that occurs on the PDN is data-dependent and can degrade the driver performance [2]. The following discusses a new signaling method that is an extension of the PTL concept which reduces the amount of power supply noise. The concept proposed in this paper enables the design of a high impedance power distribution network as opposed to a low impedance power distribution that is currently used. This is because the PTL has a relatively high characteristic impedance associated with it as compared to a power and ground plane.

Figure 1. Constant Voltage Power Transmission Line topology

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II. PROPOSED (PTL) SCHEME

A variant of the PTL signaling topology is presented here that can address the data-dependent DC drop in the PDN. The new PTL-based signaling scheme is shown in Fig. 1. Depending on the input data, a data pattern detector is used to select a resistor path in the PDN to keep the impedance looking into the input of the PTL ($Z_{PTL,in}$) constant.

The resistor values (shown as $R_s$, $R_{on}$, and $R_2$ in Fig. 1) are carefully chosen to keep the power supply voltage seen by the drivers, $V_{DD}$, at a constant level regardless of driver states. For $N$ drivers, there are a total of $2^N$ possible data combinations. However, the current that is drawn by the PDN is dictated not by the number of output combinations, but by the number of drivers that are in a “high” state at any given time. Consequently, for $N$ drivers, $N+1$ different values of source current can be drawn, so $N+1$ different resistor values are required in the PDN. The following equations are used to calculate each resistance path value in the PDN.

$$R_{driver,k} = \frac{R_s + R_{on}}{k}$$  \hspace{1cm} (1)

$$R_i = \frac{R_s V_{DD} R_{driver,k}}{R_{driver,k} V_i - R_{driver,k} V_{DD} - R_i V_{DD}}$$  \hspace{1cm} (2)

$$R_o = \frac{R_s V_{DD}}{V_o - V_{DD}}$$  \hspace{1cm} (3)

In equations (1)-(3), $k$ denotes the number of “on” drivers at any given time (and thus, $k = 1, 2, \ldots, N$). Consequently, the data pattern detector would select the same resistor value when the data pattern is “0101” and “1010” since it is the number of active drivers that dictate the amount of current flow and not the actual bit pattern itself. The quantity $R_i$ denotes the PTL terminating resistor, $R_{on}$ is the on-resistance of each driver (these equations assume all drivers are the same), $Z_{sig}$ is the characteristic impedance of the output signal transmission line, $V_i$ is the voltage provided by the power supply, $R_m$ is the resistance of the switch used for resistance path selection, $R_{driver}$ is the resistance looking into the power supply node of the drivers, $V_{DD}$ is the desired voltage at the driver’s power supply pin, and $R_{on}$ is the load resistance as seen by the driver.

III. DESIGN OF TEST VEHICLE

In order to demonstrate the benefits of using the proposed PTL signaling scheme, two test boards were designed and fabricated to transmit a 4-bit data sequence. For both test boards, an off-the-shelf 20-pin octal buffer/line driver was used as the device-under test. One test board has the driver powered by a conventional power and ground plane measuring 240mm by 52mm designated TV1, while the other is implemented with a 25Ω power-transmission line (TV2). In order to prevent reflections from occurring on the PTL, a 25Ω resistor termination is placed at the end of the power transmission line. At the output pin of each driver, a 450Ω series resistor is placed to limit the amount of current that the driver has to supply as well as the amount of current that can flow into the oscilloscope. In addition, each output connects to the SMA connectors by a 205mm long 50Ω trace, which is either terminated with a 50Ω load or by the 50Ω internal termination provided by the oscilloscope. In addition, a 0.1μF decoupling capacitor is placed between the power and ground pins of the driver to supply the high frequency charge. The layer stack-up of each board is shown in Figure 3. One can see that by using the PTL configuration, the power plane is not needed, thus requiring less layers and therefore reducing the effect of RPDs.

By using equations (1)-(3), the resistor path values can be determined to implement the new PTL signaling circuit. However, in order to implement the circuit as-is, one would require 5 unique resistor values that would have to be switched according to the output data sequence. Consequently, it was chosen to encode the input data by using a bus-inversion encoding scheme. This scheme, as described in [5] and [6], requires an extra bit to be transmitted in addition to the 4-bit data sequence. In this implementation, the extra bit, or the “inversion” bit is set to ‘0’ by default. However, when the number of ones in the 4-bit data is or exceeds 3, the inversion bit is set to ‘1’ and the data sequence is inverted. For example, when the data sequence to be transmitted is “1011”, the actual transmitted sequence is “10100”, where the first bit is the inversion bit and the remaining four bits are the compliment of

![Figure 2. Test vehicle (a) TV1 utilizing a power transmission line, (b) TV2 utilizing conventional power and ground planes](image)

![Figure 3. Layer stack-up for test vehicle](image)
the original data sequence. With this encoding scheme, instead of requiring 5 resistors in the PDN, we only require 3 because the encoding scheme will only transmit 0, 1, or 2 high states at any given time.

Due to the difficulty in implementing a high speed switching resistor network with a solid-state switch, it is necessary to implement this switching network using an alternate means. By activating extra drivers in addition to the data drivers, one can dynamically affect the impedance that is seen by the PDN, since enabling extra drivers effectively serves to add an extra parallel impedance onto the power supply path. The on-resistance of a single active driver was measured to be approximately \( R_{on} = 11.7 \, \Omega \) and the driver IC requires a 4.5V supply. Consequently, the impedance seen looking into the power supply pin when a single driver is activated is approximately \( 512 \, \Omega \) (the driver’s on resistance plus the 450Ω series resistor and the 50Ω load termination). By using equations (1)-(3), the resistances required on the PDN to maintain 4.5V at the driver’s power supply pin with a 4.94V source are summarized in the Table I.

### TABLE I. IMPLEMENTING RESISTOR PATHS

<table>
<thead>
<tr>
<th># of “on” drivers w/ bus inversion encoding</th>
<th>Additional parallel resistance needed ((R_k))</th>
<th>Accomplished by</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>( R_0 = 256 , \Omega )</td>
<td>Turn on two extra drivers</td>
</tr>
<tr>
<td>1</td>
<td>( R_1 = 512 , \Omega )</td>
<td>Turn on one extra driver</td>
</tr>
<tr>
<td>2</td>
<td>( R_2 = \infty , \Omega ) (or high Z)</td>
<td>Turn off all extra drivers</td>
</tr>
</tbody>
</table>

Consequently, 2 extra drivers are required to implement the switching resistor path. Combined with the inversion bit discussed previously, in order to transmit 4-data bits utilizing this scheme, 7 drivers are required. For custom chip designs, this requirement can be relaxed by using a more elaborate encoding scheme.

### IV. MEASUREMENT RESULTS

The input signals are provided by a HP 83000 Automatic Test Equipment (ATE) and the waveforms at the end of the signal transmission line are measured using an Agilent 96100C oscilloscope. The input data signal is a \( 2^7-1 \) PRBS that has been encoded using the method described in the previous section and the data rate is 100Mbps, 200Mbps, and 300Mbps. The measured eye diagrams are shown in Figure 4 along with measured peak-to-peak jitter in Table II. In addition, the power supply voltage variation was measured for each test vehicle, as shown in Figure 5.

One can see that the use of the power transmission line with the switching resistance network significantly improves the shape of the waveform, as it reduces return path discontinuities and results in less power and ground bounce, as seen in the waveforms in Figure 5. In addition, tests were performed with the PTL board with and without the PTL source termination to reduce the ohmic drop across the resistor, thereby reducing power consumption. Note that the “%Δ” values given in Table II compare the corresponding PTL results with those of the plane-based case.

At the maximum operating data rate of the device, 300Mbps, the peak-to-peak jitter is reduced by 18.2% when using the proposed power transmission line scheme as opposed to using conventional power and ground planes. This is due to the fact that the PTL reduces return path discontinuities by providing a smaller current loop on which the return current can travel. In addition, by removing the series termination in the power transmission line, the p-p jitter is also reduced, though slightly.

![Figure 4. Output eye diagrams of PTL circuit (left column) and power/ground plane test circuits (right column)](image)

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>Plane-based</th>
<th>PTL-based w/o termination</th>
<th>PTL-based w/ termination</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>p-p Jitter (ps)</td>
<td>ΔVdd (mV)</td>
<td>Jitter % Δ</td>
</tr>
<tr>
<td>100Mbps</td>
<td>322</td>
<td>364</td>
<td>-9.9%</td>
</tr>
<tr>
<td>200Mbps</td>
<td>533</td>
<td>382</td>
<td>-13.3%</td>
</tr>
<tr>
<td>300Mbps</td>
<td>418</td>
<td>344</td>
<td>-26.3%</td>
</tr>
</tbody>
</table>

Table II. Peak-to-peak jitter and power supply voltage measurements
Table III shows the truth table that is implemented using this scheme. The variables A, B, C, D represent the data bits, and the inversion column shows the state of the inversion bit that is used in the bus inversion encoding scheme. The “Ex1” and “Ex2” bits are, as discussed in Section III, used to implement the resistance path. The last column shows the total number of “high” states that are transmitted during each cycle. In this 4-bit configuration, there are 2 “high” states at any given time. Consequently, for a PRBS input, on average, only 2 drivers will be active at any time. Using a standard 4-bit signaling scheme with power and ground planes without encoding will result in an average of 2 active drivers at any given time as well. Consequently, one can see that this constant voltage scheme not only benefits from improved signal integrity, but consumes approximately the same amount of power as the plane-based circuit without encoding.

VI. CONCLUSION

This paper presents a new power delivery network utilizing a switching resistor network and power transmission line. This signaling scheme provides power through a transmission line in place of a power plane while dynamically changing the resistance of the power delivery network to keep a constant voltage at the power pin of the IC. Consequently, this reduces the effects of return path discontinuities and can improve the quality of output signal by reducing power and ground bounce. Two test boards were built, one with conventional power and ground planes, and the other with the PTL-based power delivery network. The test boards measured with a PRBS input signal that is encoded using a bus inversion encoding scheme. The signal quality of the output waveform was measured and analyzed in the form of transition jitter. Measurements of transition jitter show that by using the power transmission line as the power delivery network, the transition jitter can be reduced by up to 26.3% as compared to using a power plane.

REFERENCES