DESIGN OF POWER DELIVERY NETWORKS USING POWER TRANSMISSION LINES FOR HIGH SPEED I/O SIGNALING IN COMPLEX ELECTRONIC SYSTEMS

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DESIGN OF POWER DELIVERY NETWORKS USING POWER TRANSMISSION LINES FOR HIGH SPEED I/O SIGNALING IN COMPLEX ELECTRONIC SYSTEMS

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Dedicated to my loving family and trusting friends who have sustained me through this journey. It was not easy but we did it.

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LIST OF SYMBOLS AND ABBREVIATIONS

IC	Integrated Circuit
PI	Power Integrity
SI	Signal Integrity
SSN	Simultaneous Switching Noise
PDN	Power Delivery Network
PSR	Power Supply Rejection
PSN	Power Supply Noise
I/O	Input/Output
I/P	Input
O/P	Output
PTL	Power Transmission Line
CC-PTL	Constant-Current Power Transmission Line
CP	Complementary Path
PB-PTL	Pseudo-Balanced Power Transmission Line
CV-PTL	Constant Voltage Power Transmission Line
RPD	Return Path Discontinuity
PCB	Printed Circuit Board
PG	Power-Ground
GP	Ground-Power
B-B	Board to Board
LDO	Low Drop-out Voltage regulator
PRBS	Pseudo-Random Binary Sequence
VRM	Voltage Regulator Module
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
TSV	Through Silicon Via
SMA	SubMiniature version A

CHAPTER 1. INTRODUCTION

The advancement in semiconductor industry and technologies continues to fuel the upward trend of number of transistors per integrated function predicted by Moore's Law [1]. The transistor feature size has been pushed into single digit number in the nanometer range. IBM ® recently announced their first functional transistors with 7 nm technology [2], as shown in Figure 1 [3]. As the transistor size continues to reduce enabling the integration of many systems, the computing systems have reduced from giant mainframe computers that could take up an entire floor in the 1950's to handheld mobile devices in the 21st century, and down to even more embedded solutions as shown in Figure 2 with a size reduction of 10^{12} times smaller in a 60 years period [4].

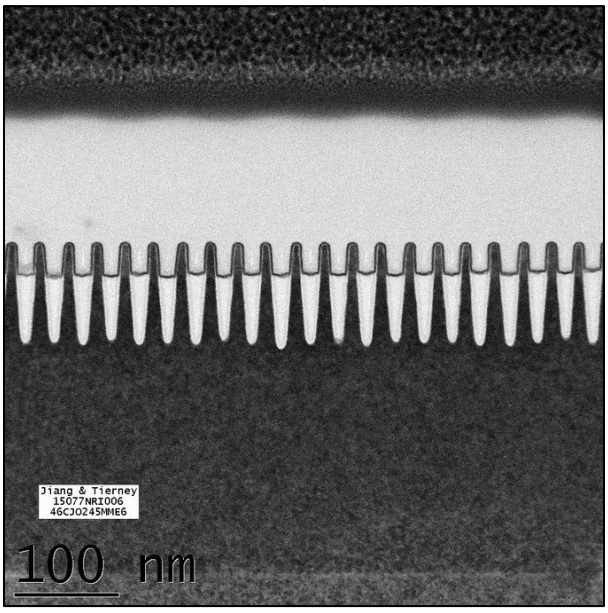


Figure 1 IBM's seven-nanometer node transistors [3].

Within the impressively eye-appealing, multifunctional, multi-interface consumer electronics, hides the miniaturized systems joined together by various interconnects [5], [6]. The system is powered by a complex power delivery network (PDN) that incorporates many voltage rails with different frequency response and transient power requirement [7]. The limited bandwidth along with other signal integrity (SI) and power integrity (PI) issues such as simultaneous switching noise (SSN) and return path discontinuities (RPD) in the interconnect and PDN poses new bottle necks to the overall system performance. Therefore, electrical engineers are spending an increasing amount of engineering hours on power integrity related issues.

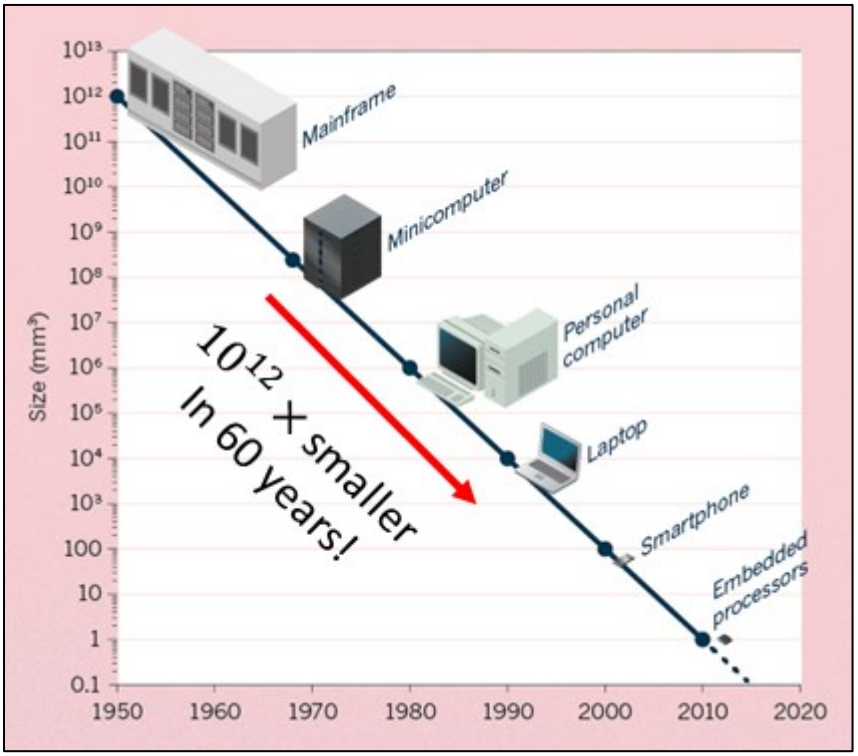


Figure 2 Revolution of computing machines from 1950 to 2020, adopted from [4].

The leading network technology company, CISCO ®, recently conducted a study on the types of technical problems and number of hours spent on each by their 28-member high speed digital design team. The work was categorized into four main areas: SerDes, Power Integrity, Mixed Signal and Time Domain. The reported data is shown in Figure 3. The data suggests that from 2004 to 2013, the time that this team spent on power integrity related issues has sextupled in 9 years. The amount of time spent on PI was approximately 30% of total effort of the entire global team in 2013. Furthermore, PI is the only category that grew in such a fast pace among all of the four categories. The result of this case study is another clear indication that power integrity is a major and very important issue and worth the attention of the research community to tackle and provide effective solutions for. This dissertation is dedicated to address some of the major power and signal integrity issues presented in high speed digital designs to include return path discontinuities and simultaneous switching noise issues.

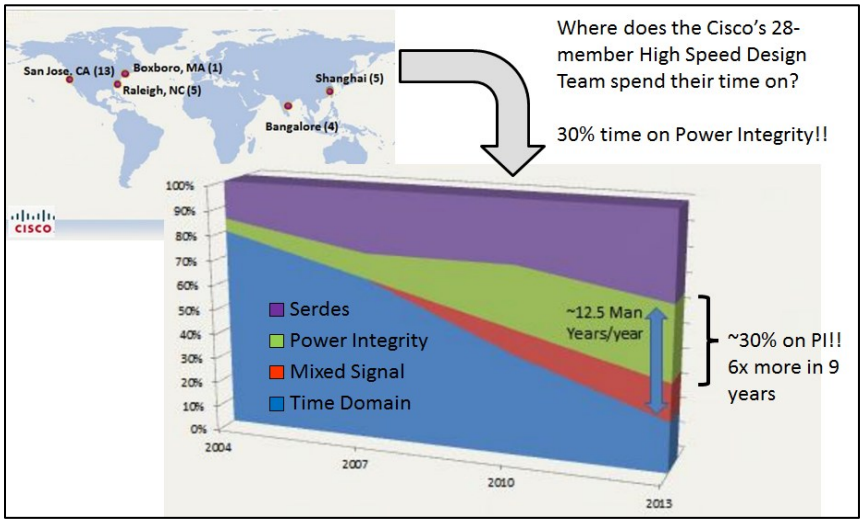


Figure 3 CISCO ® high speed design team work load from 2004-2013 [8].

One problem that leads to power integrity issues and affect signal quality is the integration of various components in a computer system with multiple dimension ranges from nanometers to meters. The computer system includes semiconductor dies, package and printed circuit boards (PCB) all joined together by metal traces, solder bump, balls, bond wires, etc. The data transfer speed, such as PCIE (Peripheral Component Interconnect Express) Generation 3, SATA (Serial AT Attachment), and USB (Universal Serial Bus) 3.0, taking place between different parts of a system can be in the range of megabits to gigabits per second. As the frequency content in the interconnect increases, the electrical feature size seen by the signals is magnified. The impedance discontinuities within the interconnect are also pervasive and difficult to manage due to dimension and material property mismatches. Therefore, physical design and layout of signal traces that carry high speed data becomes increasingly critical. Return path discontinuities (RPD), which are common in scenarios such as a signal line making via transition through the stack-up, or going over a small aperture in the reference plane, can lead to significant SI and PI issues [6], [9]. The trend to reduce the number of voltage and ground layers that could otherwise be used as signal reference layers in package and PCB designs in order to reduce manufacturing cost further exacerbates the RPD induced issues. Therefore, one main goal in this research is to address the RPD issue head-on and propose our corresponding solutions in complex integrated systems.

Bandwidth limitation of the interconnect is another critical factor that can affect signal propagation with fast rising/falling edges, as shown in [6], [9] and [10]. In order to reduce the impact on interconnect bandwidth, 2.5D and 3D integrated systems on a chip solution have been sought after [11]. On the power management front, the recent trend is

to move towards fully integrated voltage regulators (FIVR) to supply both the core and I/O circuits for System on Chip (SOC) applications to improve both power efficiency and voltage regulation [12], [13] and [14]. One implementation of FIVR is to integrate the buck converter and Low dropout (LDO) regulators as a two chip solution on a package with passives such as inductors and capacitors either surface mounted or embedded in the package [15]. To ensure fine grained power management, LDO circuits are integrated in the SOC in close proximity to the load. Several LDOs integrated in the SOC are used to provide voltage regulation for both the core and the I/O circuits. An embodiment of a switching voltage regular module (VRM) connected to an LDO circuit is shown in Figure 4.

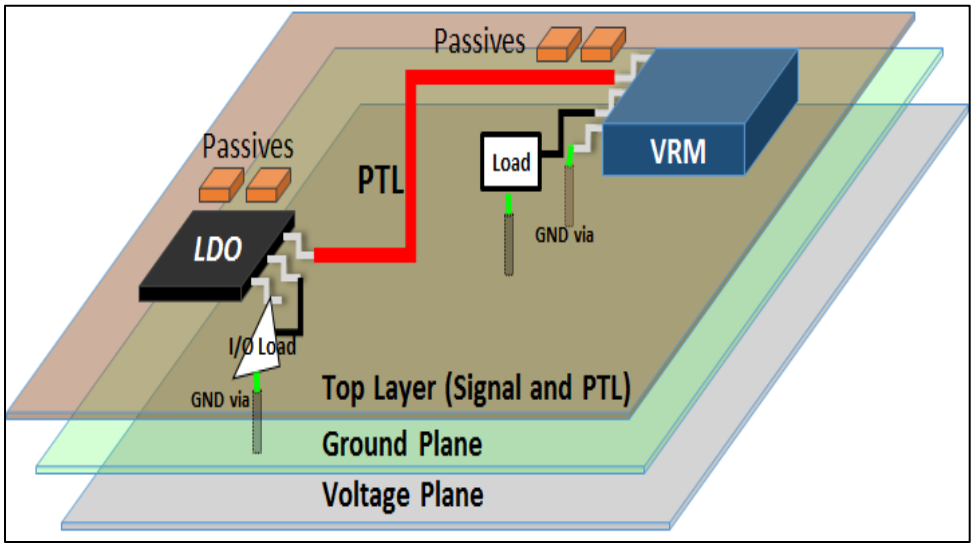


Figure 4 Integrated voltage regulator solution with a VRM and LDO on package

The LDO circuit is mainly used to provide clean power to noise sensitive and/or fast switching digital (I/O) circuits. It regulates its output through a negative feedback loop

[16]. Due to the limited bandwidth of the internal circuitry, the LDO circuit begins to lose its regulation as the loop gain of the feedback starts to drop. This drop starts to peak when the loop gain reaches 0 dB at certain frequency, usually in the range of megahertz (MHz) to gigahertz (GHz) for integrated LDOs [15], [16]. As a result, more input power supply noise can couple to the output. This phenomenon is called power supply rejection (PSR) peaking. The second topic studied under this dissertation is to enhance the PSR bandwidth and at the same time improve the overall energy conversion efficiency of the LDO circuit. Figure 4 shows the VRM connected to an LDO circuit via a PTL to power I/O drivers.

1.1 Current Power Distribution Network Design Approaches and Their Challenges

The main goal of power distribution network (PDN) design is to provide clean power to various types of loads [19]. The PDN is a comprehensive system that includes VRMs, LDOs, interconnect conduits, filters and etc. The type of interconnect used in PDN designs is typically power-ground plane pairs to distribute power. From this point on, we refer the conduit that connects a power source such as a VRM to its loads as the PDN unless otherwise noted.

In order to design a satisfactory PDN, a frequency domain target impedance profile $Z_{target}(f)$ is usually established based on maximum current transient, $I_{max}(f)$, and allowable noise ripple ($V_{ripple}(f)$), as shown in (1), where f represents the frequency spectrum under evaluation.

$$\mathbf{Z_{target}(f) = \frac{V_{ripple}(f)}{I_{max}(f)}} \quad (1)$$

As the transistor size continues to decrease, the gate oxide breakdown voltage also decreases. Along with this decrease is the tolerable noise requirement on the supply rails.

The target impedance, which is directly related to the noise tolerance, is usually around only several milliohms over a wide range of frequencies in modern digital designs [20]-[21]. The current PDN design approach is to utilize power and ground plane pairs for power delivery due to the low DC resistance. However, in the frequency domain the impedance of a power-plane pair exhibits anti-resonance peaks and resonance nulls behavior, as shown in Figure 5. Figure 5 is the simulated impedance profile at port location 1-inch by 1-inch on a plane pair of size 6-inch by 5-inch. The separation of the planes is 40 mil using FR-4 material with a dielectric constant of 4.5. The addition of other mounting structures and perforations to the PDN further complicates its impedance profile [6]. If a noise current source occurs at these high impedance points, substantial amount of noise can be generated [9].

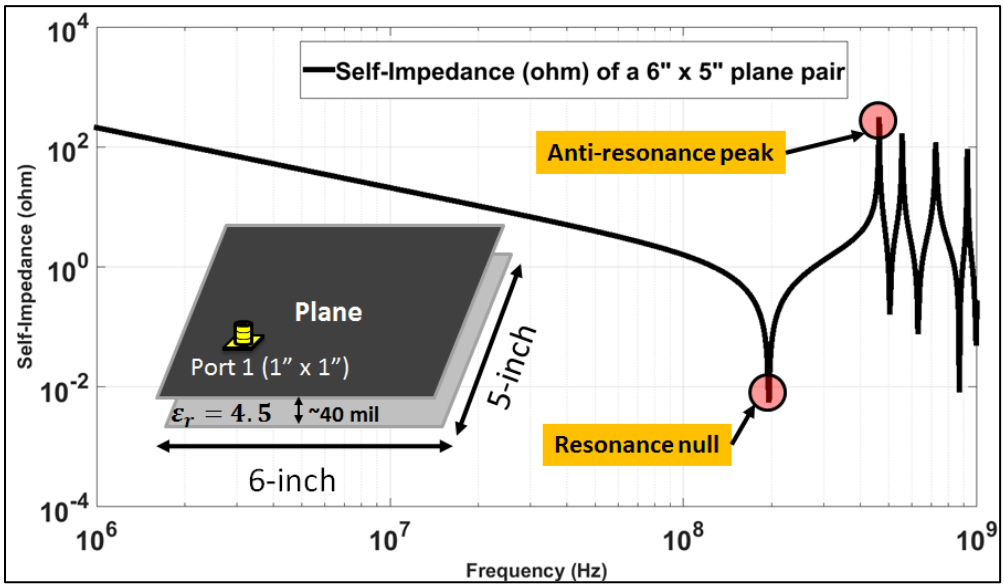


Figure 5 Simulated plane pair self-impedance taken at port location 1" x 1" on a 6" x 5" board.

In order to lower the peaks caused by anti-resonance in the impedance profile of a voltage-ground plane pair, decoupling capacitors with various sizes and values have been used. However, due to the physical dimension and limited quality factors of the capacitors, the effectiveness of the capacitors are restricted [20][21][22][23]. For example, the capacitors have series parasitic resistance and inductance that can interact with the plane impedance and create other unwanted impedance peaks [6].

In the construction of a PCB, voltage planes are often sandwiched between either signal and/or ground layers. Although it is ideal to have solid planes for power distribution and signal referencing [9], unfortunately planes, especially voltage planes, are often divided into small islands to accommodate many different voltage rails given a limited number of plane layers [24]. A signal referenced to a discontinuous plane or being routed over other physical apertures such as an anti-pad of a via, resulting in the return current path for the signal being interrupted and can lead to severe signal degradation as shown in [9] and [25].

In order to counter the drawbacks in PDN designs, certain signaling techniques such as differential signaling is used. For example, when a differential pair is used, a complete current loop is formed within the pair. Even there could be RPDs in the nearby plane layer, the impact on the differential signal in terms of cross talk and coupling is limited. Additionally, a differential receiver can easily cancel out common mode noise existing on the differential pair by subtracting the negative signal from the positive signal and obtaining twice the magnitude of the signal as illustrated in [25]. The successful cancellation of common mode noise however relies on good matching of the two signal

traces within the pair without phase delay. Unfortunately, differential pairs often suffer from mismatched length within the pair during routing and fiber weave effect [26].

It was previously mentioned that interconnects in high speed designs suffers from impedance mismatch and limited bandwidth issue than can slow down a rising or falling edge of a signal. However, the bandwidth limitation issue does not only exist in interconnects. Power supply sources such as VRMs and LDOs also suffers from limited bandwidth. As a result, power droop and power supply rejection peaking can hinder the overall performance of clean power delivery [16].

The uniqueness to the PDN design challenges is that there is no fail-safe solution to a stand-alone issue. In reality the potential solution to one problem has its own limitation and sometimes can create other problems such as the aforementioned use of decoupling capacitors, which will be further discussed in the following section. Table 1 summaries the challenges in PDN design.

Table 1 Power Distribution Network Design Challenges

Ideal Scenario for PDN Designs	Challenges in Realistic Designs
Full solid power and ground planes	Voltage and ground plane splits [24]
Decoupling Capacitors	Limited bandwidth [20]-[23]
Uninterrupted signal return path	Return Path Discontinuities (RPD) [6][9]
High bandwidth power supplies	Limited bandwidth and power supply rejection peaking [16]
Differential Signaling without phase mismatch	Routing congestion, skew, fiber weave effect [26]

1.1.1 Use of Decoupling Capacitors in PDN Design

Decoupling capacitors are often used in PDN designs to lower the impedance peaks in order to provide a wide spectrum of low impedance profile that meet the target impedance requirement. There have been numerous research work and study done on such techniques to include selection of decoupling capacitors, their placement, design and inclusion of secondary effects due to parasitic such as [20]-[23] and [27]-[34]. A very common methodology is to use banks of decoupling capacitors of different types, sizes and values. The capacitors are used to target and suppress resonance peaks at different frequency spectrum region based on current transient requirement to provide a smooth impedance profile. This method is illustrated in Figure 6 [35].

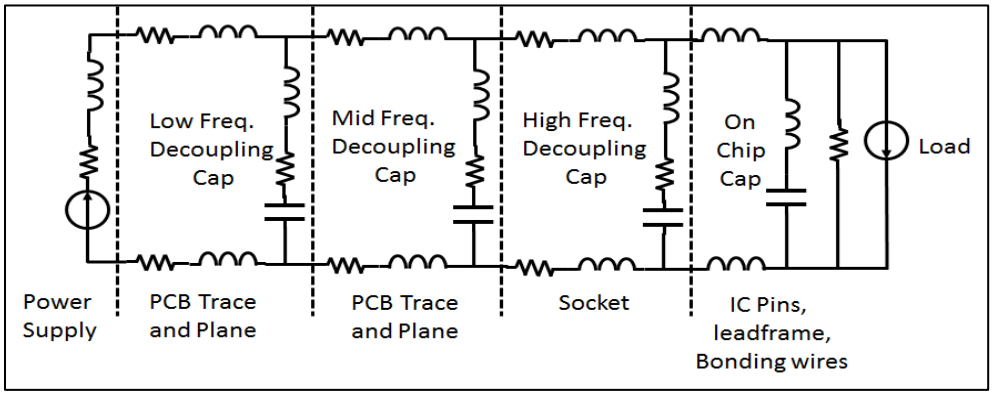


Figure 6 Power Distribution Network and decoupling capacitor network bank [35]

There are several drawbacks to this approach. First, the capacitors have both equivalent series inductance and resistance, ESL and ESR, respectively [34]. Furthermore,

there are other additional series inductance from the mounting structure of the capacitors and the spread inductance associated with power/GND planes further contribute to the total parasitic inductance as a result of adding decoupling capacitors [20], [34]-[38]. In its more complete form, a physical capacitor can be modeled as a capacitor in series with ESL and ESR, as shown in Figure 6. A comparison of the ideal and non-ideal models of a capacitor is shown in Figure 7. The frequency where the null is located is called the resonance frequency beyond which point the capacitor no longer acts as a capacitor but rather as an inductor. The impedance at the resonant frequency is equal to ESR.

The second drawback is that the power and ground pair of a PDN forms a capacitor and also has its own loop inductance. A decoupling capacitor can interact with the plane inductance to form other impedance peaks as shown in [6], [9] and [39]. Depending on the location of these peaks, they can excite other unwanted noise. Furthermore, due to the parasitic, the addition of decoupling capacitance cannot always lower the impedance to the desired value especially in on-die or on-package designs due to very limited space [40]-[41].

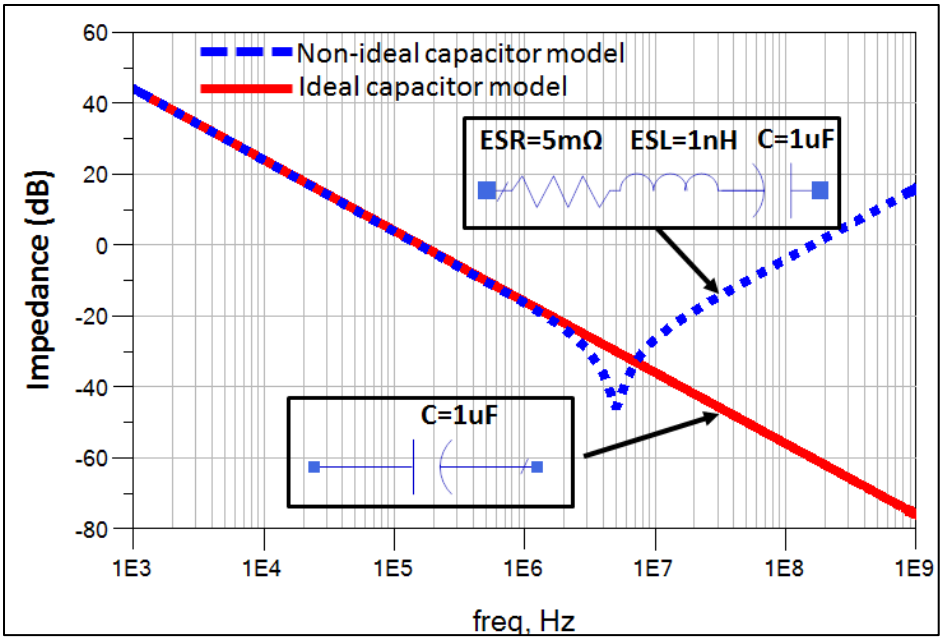


Figure 7 Ideal vs. non-ideal capacitor impedance plot (C=1uF, ESL=1nF, ESR=5 mΩ)

Lastly, a printed circuit board design can sometimes takes several hundreds or even thousands of decoupling capacitors for mid and lower frequency bypassing and decoupling [36]. This increases manufacturing and design cost. The question of "how many decoupling capacitors are enough" is getting harder to answer given the complexity of modern PCB and package designs. Where to place the capacitor is another important question to answer. Wrong placement or unnecessary use of capacitors not only can be ineffective but may actually hurt circuit performance [42]. Often times, simulation and modeling are necessary to answer such questions or "rules of thumb" are often used. Finally, the capacitors are also subjected to aging degradation and temperature variation. With a large number of capacitors being used, the reliability of the products and performance decreases [43].

1.1.2 Voltage-Ground Plane Pair based PDN Design Approaches and Their Challenges

Traditionally, voltage-ground plane pairs have been used in PDN design due to its low DC resistance and ease of dropping vias to make connections between components and internal plane layers. However, a plane based PDN has its own limitations. As previously mentioned, the central goal of the PDN design is to design a low impedance profile to meet the target impedance. However, the current transient spectrum is usually unknown to most PDN designers [20]. The PDN designers therefore have to estimate the current signature which may lead to inaccurate calculation of the target impedance. The eventual PDN could be either under- or overdesigned as a result. Second of all, the inductive region of a plane can interact with decoupling capacitors, which results in unwanted impedance peaking. Figure 8 shows the impedance profile of a 6" x 5" plane pair with separation of 40mil before and after adding a 2.2nF capacitor at the measurement port, located at 1" x 1". The solid curve indicates the impedance profile without the decoupling capacitor. There is a peaking at ~110 MHz. After adding the capacitor with 400 pH ESL and 8 mΩ ESR, the peaking at ~110 MHz is suppressed. However, another peaking at around 50 MHz is inadvertently created as shown by the dashed curve. The dash-dot curve represents the capacitor. More on the potential danger of this peak shifting will be discussed in a later chapter.

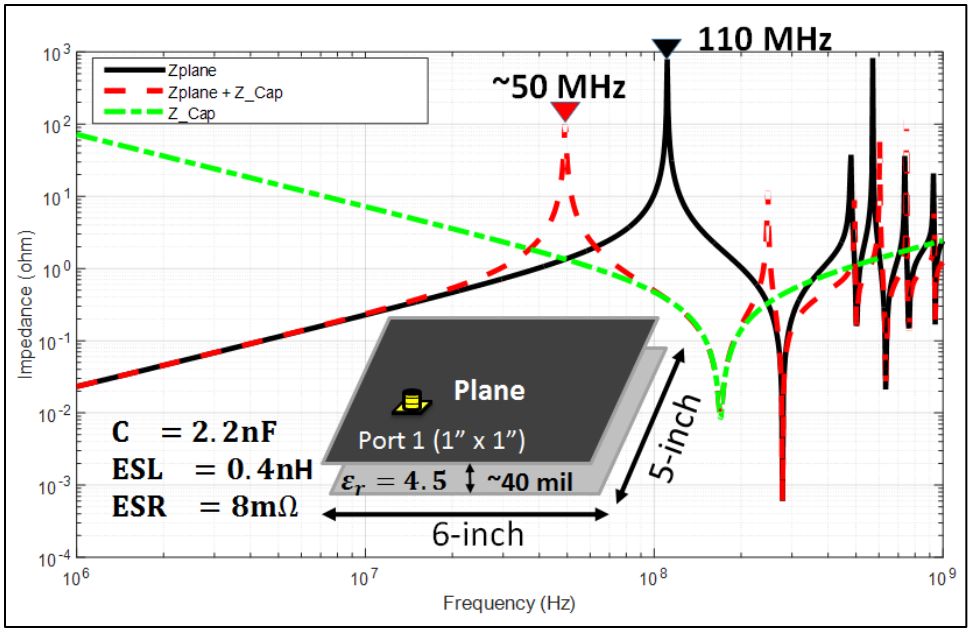


Figure 8 Impedance profile of a plane before and after adding a decoupling capacitor

The notion and practicality of using full solid planes for voltage supply and ground reference are also being challenged in modern competitive electronics market especially in the consumer electronics sector. It is often the manufacturing and design cost that drives many of the design decisions and trade-offs. One area that is often being scrutinized is the reduction in number of layers for PCB or package stack-up design. Decision makers frequently request the number of layers to be reduced in order to save cost. The power and ground plane layers are often the first ones to be reduced or removed. For example, package designs for mobile electronics and applications mostly have a 4-layer design while many low-end designs have been pushed down to two layers. While a 4-layer design provides more electrical design flexibility and mechanical robustness, 2-layer packages greatly cut down the cost which is an attractive factor in the now fiercely competitive market. As a result, many voltage domains have to share a single voltage plane, which is divided into

small islands. An example of two separate voltages sharing the same plane layer is shown in Figure 9. In such a design environment, a full solid ground plane is difficult to maintain. The irregular shapes of the power and/or ground planes that form a 2D structure makes estimating the anti-resonance frequencies very difficult and can lead to cavity resonance effect as the waves propagate [6]. As a result, it is often an iterative process; and requires in-depth modeling to eventually arrive at an effective filter network solution to handle the anti-resonance impedance peaks.

Last but not least disadvantage in using plane based PDN designs is the return path discontinuities (RPD) created in such structures as demonstrated in [11], [44]-[48] and explained in the next section.

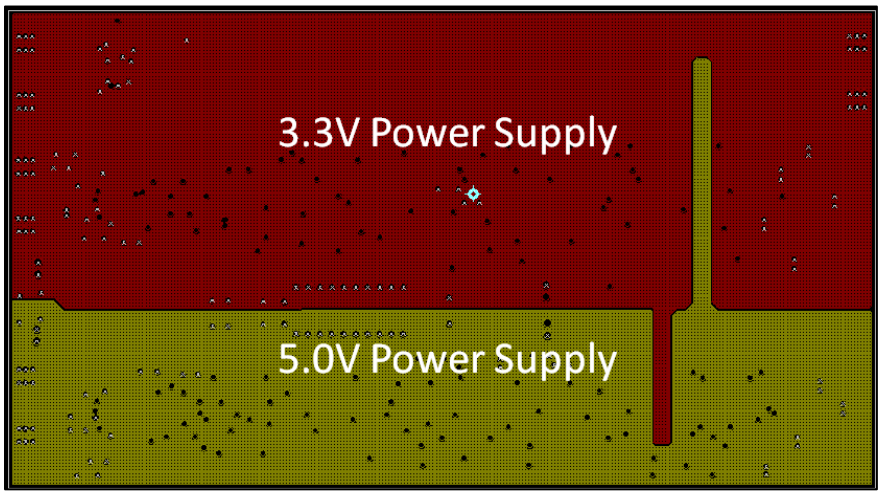
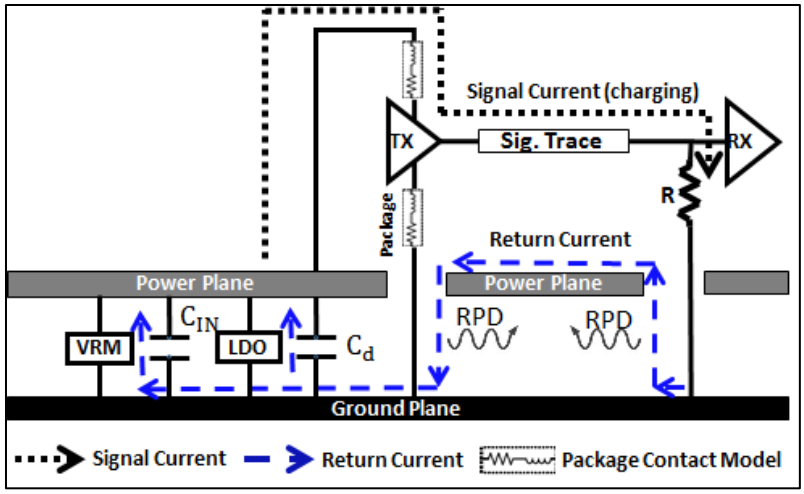


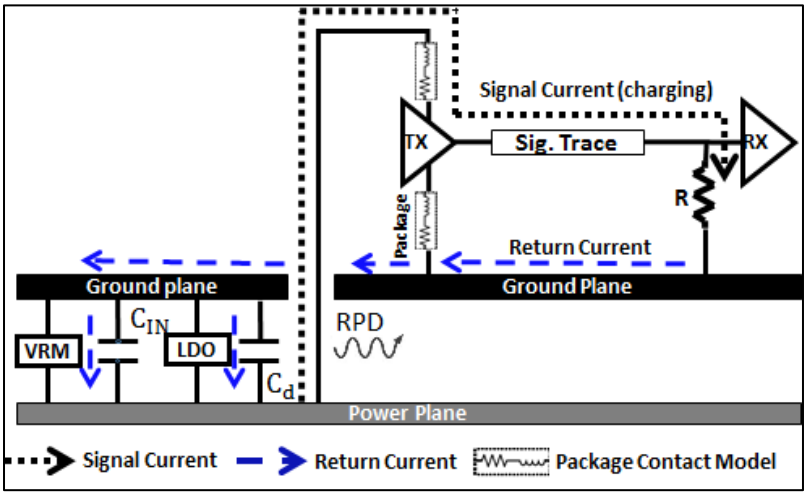
Figure 9 An example of a split power plane for two power supplies.

1.1.3 Return Path Discontinuity (RPD).

Simultaneous switching noise (SSN) is detrimental to signal and power integrity in modern high speed digital designs [9], [30] and [49]. A major and common contributor to SSN is the return path discontinuity (RPD) [9]. RPD is broadly defined as the interruption in the current return path of a high speed signal. The RPD effects occur due to the interruption in the return current path as a result of perforations in the voltage planes, split planes, via to via transitions, to name a few [50]. In addition, cavity resonances between the voltage and reference planes can further degrade signal integrity due to excessive power supply noise. The mode of coupling between the power distribution and signal distribution are through Return Path Discontinuities (RPD) [50]. When planes are used, irrespective of the signal referencing (signal referenced to voltage or signal referenced to ground), the interruption in the current path causes RPDs that can affect signal and power integrity. The source of these discontinuities are shown in Figure 10, where the receiver (RX) is terminated by a resistor in parallel. The current path for the charging of the signal line is shown in Figure 10 (discharging scenario not shown), where RPDs occur due to the return current transitions between inner planes [9]. Since the continuity of the reference layer for the return signal is lost, the return current needs to find its way back to the transmitter through other AC paths such as through a nearby decoupling capacitor, C_d, as shown in Figure 10 [9]. As a result, RPDs are induced, the current loop size increases leading to increased parasitic inductance and caused the signal energy to interact unfavorably with surrounding circuit elements through means of electromagnetic interference. The degrading effect of RPD on signal and power integrity will be further demonstrated in later chapters through simulation and measurement.



(a)



(b)

Figure 10 Current return path during a low-to-high transition for signal line referenced to planes (a) voltage above ground plane, and (b) ground plane above voltage plane.

1.2 **Power Transmission Line (PTL).**

As shown in Figure 10, [9] and [50], RPD is inevitable and its effect more difficult to handle and suppress in a PDN design with multiple reference layers at different voltage potentials. Therefore an alternate power distribution scheme using power transmission

lines was proposed recently to target RPD related issues [44]-[47]. The essential idea of PTL based PDN is to replace the voltage planes with transmission lines to deliver power from the source to the loads. Since a transmission line is tasked for power delivery, we call this as Power Transmission Line or PTL. In the case of PTL based PDN as shown in Figure 11, a power transmission line replaces the role of the voltage plane to carry power from the VRM to the load. Both the signal traces and PTL are referenced to the same ground layer. As a result, a complete closed current loop with minimal loop inductance is formed between the signal trace and the ground reference layer [44]. The RPDs in Figure 10 are therefore eliminated. This significantly improves signal and power integrity in systems as demonstrated in [44]-[45] and [48]. For example, in the past it was shown that using PTLs to power I/O drivers improves eye height and jitter by over 15% and 36% in [44], respectively, since any coupling between the signal and PDN is minimized as demonstrated in [63], [65] and [66].

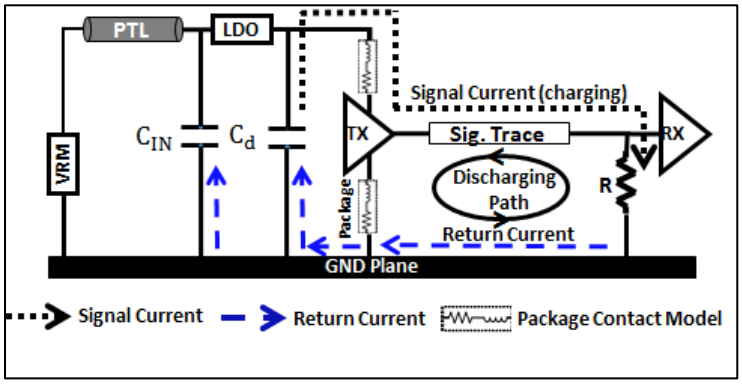


Figure 11 Current return path during a low-to-high and high-to-low transition using PTL

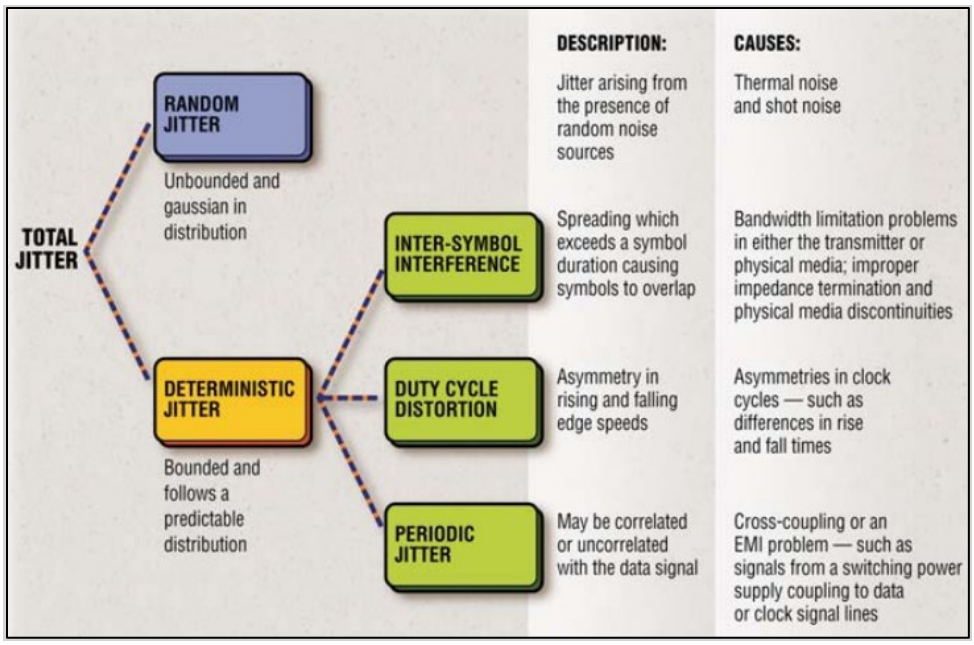


Figure 12 Classification of Jitter [51]

Another advantage of utilizing PTL is its ability to suppress jitter variation as compared to plane based design. Timing Jitter is the deviation of the significant timing instances such as a rising or falling edge of a signal from their ideal locations according to the International Telegraph and Telephone Consultative Committee (CCITT). Jitter can be classified as random and deterministic jitter, as shown in Figure 12 [51]. The magnitude of random jitter is unbounded. This type of jitter is usually caused by thermal and shot noises in the system [51]. However, a major cause of deterministic or data dependent jitter is due to the bandwidth limitation of the interconnect and impedance anomalies within the physical media such as a PDN [51].

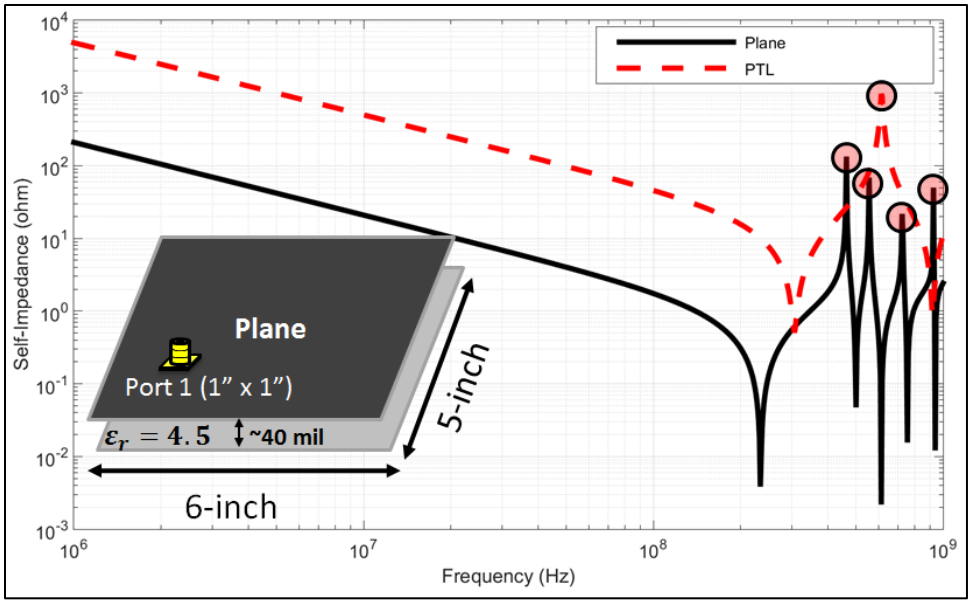


Figure 13 Impedance comparison between a 6" x 5" plane and a 5" long and 50-mil wide PTL

Figure 13 compares the self-impedance profile of a voltage-ground plane pair and that of a PTL. The plane pair size is 6" long by 5" wide with 40 mil separation measured as 1" by 1" location. The PTL is a 5" long and 50 mil wide microstrip structure. As can be seen in Figure 13, the plane based impedance profile displays much higher variation in impedance than the PTL design which would lead to more deterministic jitter and worse signal quality [51]. As can be seen in Figure 13, there are four distinct anti-resonance peaks in the plane based design as compared to only one peaking in the PTL design. This conclusion of more jitter variation in plane based designs is also corroborated by the simulation and measured data in [44],[45] and [48], and those shown in the later chapters of this dissertation. The higher impedance of a PTL also helps to dampen energy reflection within the PTL due to impedance mismatch [9][10][25].

Since PTLs may have higher DC resistance than traditional power planes, it is more suitable in low power and high signal fidelity applications such as powering high speed I/O drivers and sensitive circuitries such as a phase lock loop (PLL). A study in [47] was done to demonstrate the power consumption tradeoff and design guidelines on the design of physical parameters of PTLs.

1.3 Past work on PTL

Three signaling schemes centered on PTL have been explored in the past and can be summarized using Figure 14. Each has its unique design goals and implementation. They are discussed in the following sections.

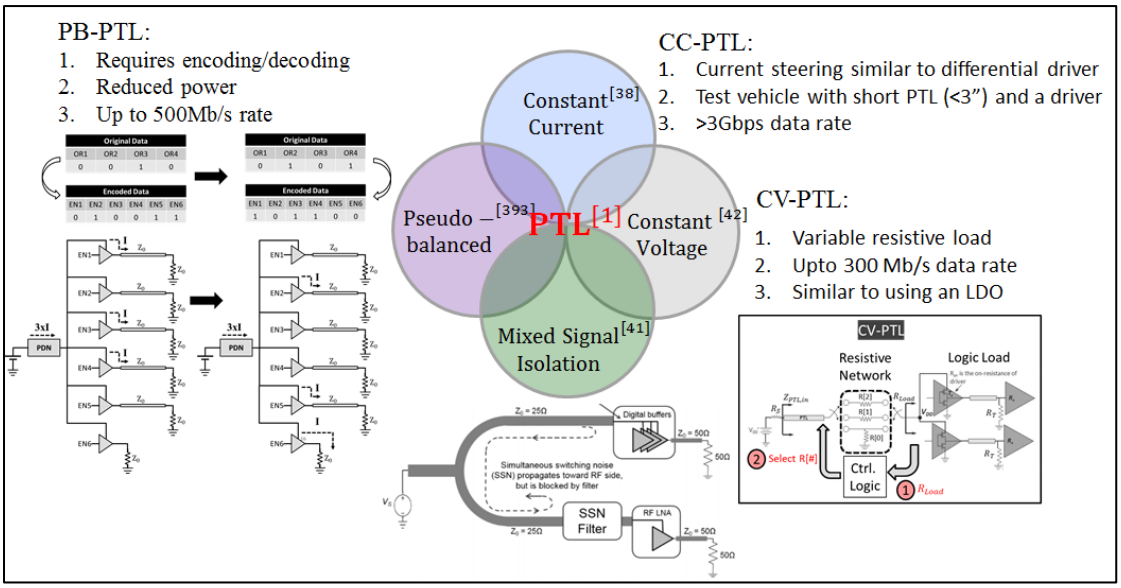


Figure 14 PTL and its signaling schemes

1.3.1 Constant Current Power Transmission Line (CC-PTL)

Since PTL is fundamentally a transmission line, it needs to be terminated at the power supply source to minimize reflection from the load due to impedance mismatch and/or manufacturing variations. As shown in Figure 16a, a series terminating resistor R_S is added between the DC supply and the PTL to dampen any reflection from far end. However, the issue of dynamic DC drop arises at the load end of the PTL since the terminating resistor and the on-resistance of the driver form a resistor divider network. This DC drop at node V_PTL, where the PTL connects to the driver, is highly dependent on the output states of the driver supplied by the PTL [44]. To mitigate this issue, a novel signaling scheme was introduced to add to the PTL design. The idea is to minimize current transient ($\partial \mathrm{i}/\partial \mathrm{t}$) on the PTL regardless of input data pattern by keeping the PTL constantly charged, as shown in Figure 16b. Therefore, the overall simultaneous switching noise (SSN), which is defined as $\mathrm{V_{SSN}} = \mathrm{L} * \partial \mathrm{i}/\partial \mathrm{t}$, is significantly reduced. This is achieved by adding a complimentary path (CP) that is impedance-matched ($\mathrm{Z_C}$=$\mathrm{Z_M}$) to the signal path, as shown in Figure 16a. The added circuity from the CP is circled by the dashed box in the figure. When the main signal path is drawing current from the V_PTL node, the complimentary path is off and vice versa. Regardless of the input data pattern, the same amount of current always flows through the PTL so V_PTL reaches a quasi-steady state. Therefore, the current transient on the PTL is very low. This comprehensive design topology combining PTL and the compensation scheme is called Constant Current Power Transmission Line or CC-PTL, and is explained in detail in [46].

The signaling method used in CC-PTL relies on current steering and compensation which is similar to differential signaling. One major difference is that in CC-PTL, the complementary path is locally terminated, as shown in Figure 16a, making it a modified

version of differential signaling, or constant current (CC) signaling. In term of output trace routing, since the complementary path is locally terminated only one output trace is routed out for each signal bit, which is similar to single ended signaling. However, single ended signaling operates at much lower speed than differential signaling as it is more prone to adverse effects from crosstalk, ground bounce and other issues. Some of the common industry standards that utilize single ended signaling includes RS-232, PCI (Peripheral Component Interconnect) and SCSI (Small Computer System Interface), which all have a speed in the range between kbps to several hundred megabits per second. As a matter of fact, many single ended signaling schemes have been upgraded due to low speed and been converted to differential signaling. One such example is the upgrade of PCI to PCI Express that utilizes differential signaling method. Some examples of the communication protocols that utilize differential signaling that can reach up to Gbps range are DDR SDRAM at 3.2 Gbps, USB 3.0 at 5 Gbps and 10 Gigabit Ethernet at 10 Gbps. A main bottle neck to the wide use of differential signaling is routing congestion. As the driver and receiver density increases, the amount of traces to be routed for differential signaling is massive given a limited number of routing layer in a stack-up and the complexity of component placement in a PCB design. Another physical phenomena called fiber-weave effect can also affect the performance of high speed differential signaling [26]. To maintain good differential mode signaling, a good symmetry needs to be maintained for the differential pair. The two traces not only need to be routed with little or no phase delay, the property of their surrounding substrate can also make an impact as the propagation delay of an electromagnetic wave is determined by the dielectric constant of the dielectric material surrounding the conductor [9]. The most common substrate material is made of FR-4 (fire retardant 4) dielectric

which is made of woven fiberglass fabric that is filed with an epoxy resin. There are many different type of FR-4 that yields different woven density and thickness, which lead to various dielectric constant and loss tangent. Each type may have different warp count, fill count, warp yarn and fill yarn as shown in Figure 15 [52]. If the traces within a differential pair are being routed across parts of the dielectric material with different construction, the dielectric constant will be different leading to different signal propagation delay. It is not uncommon to route two traces with the same physical length for several inches and yields a phase delay of tens of picoseconds [26].

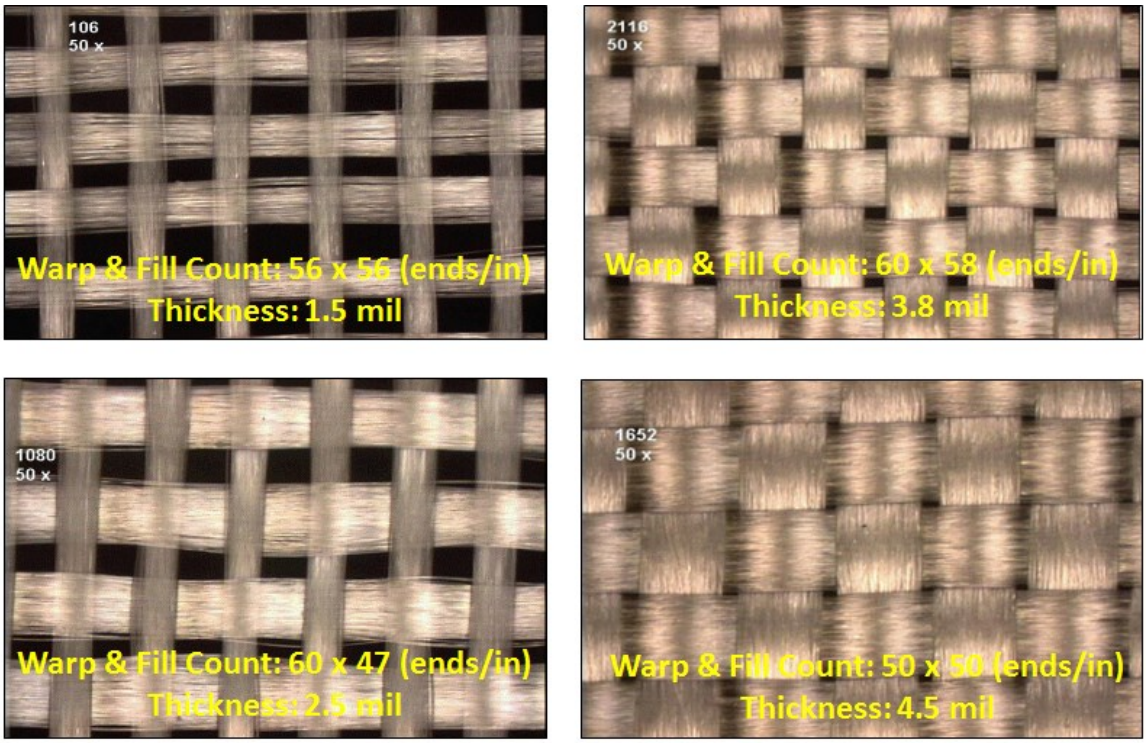


Figure 15 Four FR-4 samples with different woven density and thickness [52]

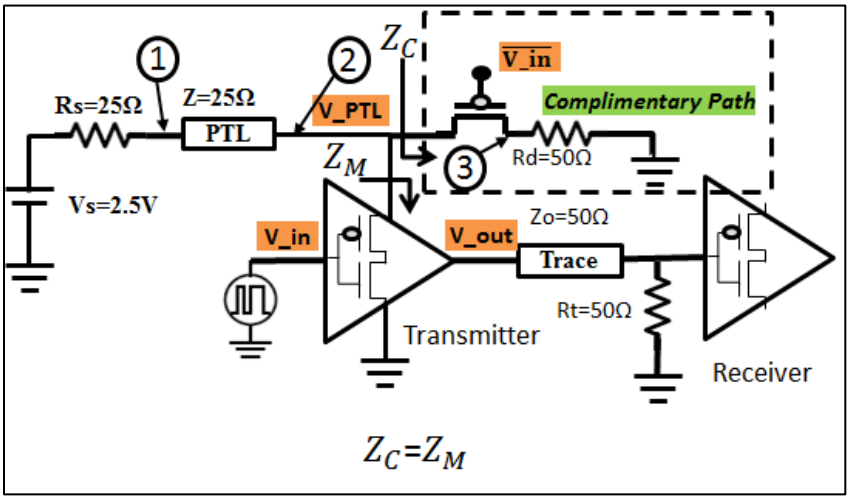
The utilization of constant current signaling, as shown in Figure 16a, takes the advantage of both single ended signaling and differential signaling. Since CC utilizes current steering and compensation method which is the same as in a differential signaling scheme, it can reach a data speed comparable to that of differential signaling. In fact, the implementation of CC in all test vehicle designs utilized high speed differential drivers in this research work. The difference is that one of the differential output or the CP, as shown in Figure 16a, is locally terminated to ground resulting in only one high speed interconnect that needs to be routed. Therefore, high speed single-ended signaling or constant current signaling is still possible while reducing the burden on routing congestion [44].

Table 2 Comparison between Different Signaling Schemes

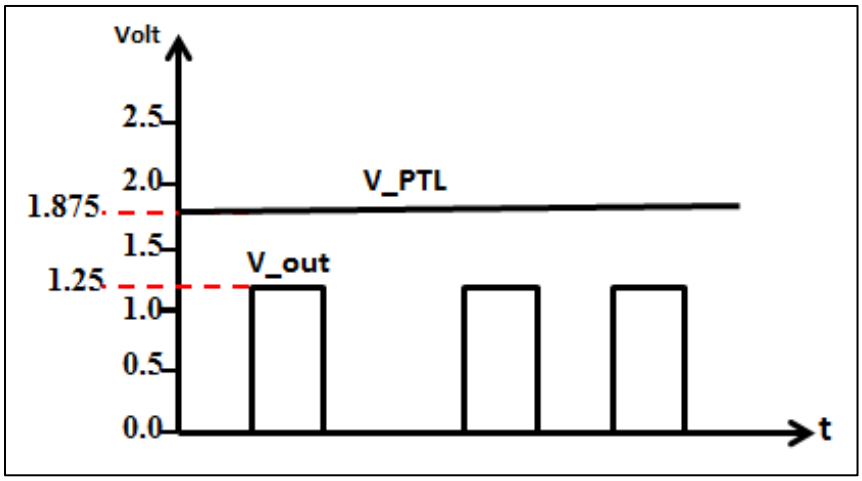
	High Speed Data Transfer	Energy Consumption	Routing Congestion Issue	Immunity from Fiber Weave Effect
Single Ended Signaling	Bad	Good	Good	Good
Differential Signaling	Good	Acceptable	Bad	Bad
Constant Current Signaling in CC-PTL	Good	Acceptable	Good	Good

Later in Chapter 3 the signal quality from differential signaling and CC signaling will be compared through measurement data. Both methods reached the same speed with comparable signal quality. In summary, the purpose of implementing constant current signaling is to 1) minimize current transient on the PTL, 2) alleviate impedance mismatch effect between the PTL and its connecting components such as the terminating resistor and

the driver, and 3) improve data speed much higher than single ended signaling and comparable to differential signaling while reducing routing congestion. Table 2 summarizes the advantage and disadvantages between single ended, differential and constant current signaling schemes. The latter was used in the implementation of CC-PTL in test vehicle designs [44]



(a)



(b)

Figure 16 CC-PTL transistor level circuit illustration

To show proof of concept of CC-PTL, a simple 4-layer PCB board with both CC-PTL and power plane based test vehicles were designed [44]. One high speed differential driver (PN: NBSG16VS) was mounted on each test vehicle. The size of the boards was 3.8-inch x 2.5-inch. The length of the PTL was approximately 1.77-inch long. Eye diagrams and timing jitter were shown and compared between the test vehicles for various data speeds ranging from 500 Mbps to 3000 Mbps; different circuit configuration such as AC coupled signal line versus DC coupled; and terminated and unterminated PTL. As a result of constant current signaling, the measured eye height and jitter were comparable between terminated and unterminated PTL at a data rate of 1500Mb/s PRBS. When the output signal was DC coupled, the eye height and p-p jitter for the PTL based PDN performed better than the power-plane based PDN by 17.9% and 25% respectively. When the output signal was AC coupled, the eye height and p-p jitter for the PTL based PDN improved by 15.1% and ~36.3% respectively as compared to the plane based design [44]. However, the in-depth analysis as to why the SI and PI of the CC-PTL was better than the plane design, which also used the same differential drivers, was lacking in [44].

1.3.1.1 Potential Sources of Noise and Energy Reflection in CC-PTL

In the experimental implementation of the constant current signaling concept; there are realistic issues that can contribute to noise sources on the V_PTL node due to manufacturing imperfection, variable and loose component tolerances, imperfect matching within the differential driver that can all lead to mismatches and energy reflection within the system. To name a few, the possible locations for mismatch are marked as 1, 2 and 3 in Figure 16a, which represent mismatch between 1) the source terminating resistor Rs and

the PTL, 2) PTL and the driver, and 3) the transistor on impedance and the 50Ω terminating resistor Rd, respectively. Although there are sources of mismatch causing noise, the implementation of the current compensation leading to minimized current transient on the PTL can help minimize the impact and reduce the noise on the PTL node, as shown in [44] which will also be demonstrated through measured data in Chapter 3.

1.3.1.2 Trade-off between Energy Consumption and Signal Quality in CC-PTL

Although CC-PTL can provide superior signal performance at gigabit data rate, it poses the issue of extra power consumption by the CP, similar to differential signaling, in order to keep the PTL constantly charged. The energy efficiency of CC-PTL is almost the same as using differential signal scheme since both requires current compensation. In other words, power has been traded off for good SI and PI. Two alternative PTL based designs were proposed to resolve this issue namely, Pseudo-Balanced Signaling with PTL (PB-PTL) [45] and Constant Voltage Signaling with PTL (CV-PTL) [48]. As shown in [47], the energy per transmitted data bit consumed by CC-PTL is 53.7 pJ. The PB-PTL has reduced this energy by 25% and CV-PTL reduced the energy consumption per bit by 40% to 32.2 pJ; trade-off is in speed performance and is summarized in Table 3. Although PB-PTL and CV-PTL have energy per bit advantage, their demonstrated speed performance in [45] and [48] and shown in Table 3 is 83.3% and 90% slower than that of CC-PTL [44]. In the case of CV-PTL, the slow-down is due to it utilized single-ended signaling.

Table 3 Energy and Speed Performance Comparison in PTL Based Signaling Designs

Scheme	Energy/bit [47]	% of Improvement over CC-PTL	Demonstrated Speed	% Slow Down as Compared to CC-PTL
CC-PTL [44]	53.7 pJ	N/A	3000 Mbps	N/A
PB-PTL [45]	40.4 pJ	24.8%	500 Mbps	83.3%
CV-PTL [48]	32.2 pJ	40.0%	300 Mbps	90.0%

1.3.2 Pseudo-Balanced Signaling with PTL (PB-PTL)

The previously proposed CC-PTL relies on complimenting each individual bit using a complementary path in order to maintain minimal voltage fluctuation on the PTL that supplies the I/Os. Pseudo-Balanced Signaling (PBS), on the other hand, focuses on bundling and transmitting multiple digital bits together through encoding in order to control the power supply noise and lower power consumption as compared to CC-PTL.

Given M number of data bit, PBS utilizes a coding scheme [45] to encode it into N bits (N>M). Furthermore, the number of encoded bits is less than that from conventional encoding schemes [53]. For example, if M=4, (2) shows N=5 is enough to include all permutations as opposed to 6 bits according to [53].

$$\frac{5!}{2!\cdot 3!}\cdot\frac{5!}{3!\cdot 2!} = 20 > 2^4 = 16 \quad (2)$$

A balancing bit is then added, if necessary, to N so that the encoded bit stream has an equal number of 1s and 0s, as explained in [45]. This approach ensures minimal current transient on the PTL that can ensure reduced voltage ripple. Furthermore, since N bits are enough for the receiver to decode, the additional balancing bit is locally terminated and not

transmitted to further reduce routing congestion and pin count, as shown in Figure 17. Therefore, as a result, PBS with PTL incurs less power penalty than utilizing CC-PTL.

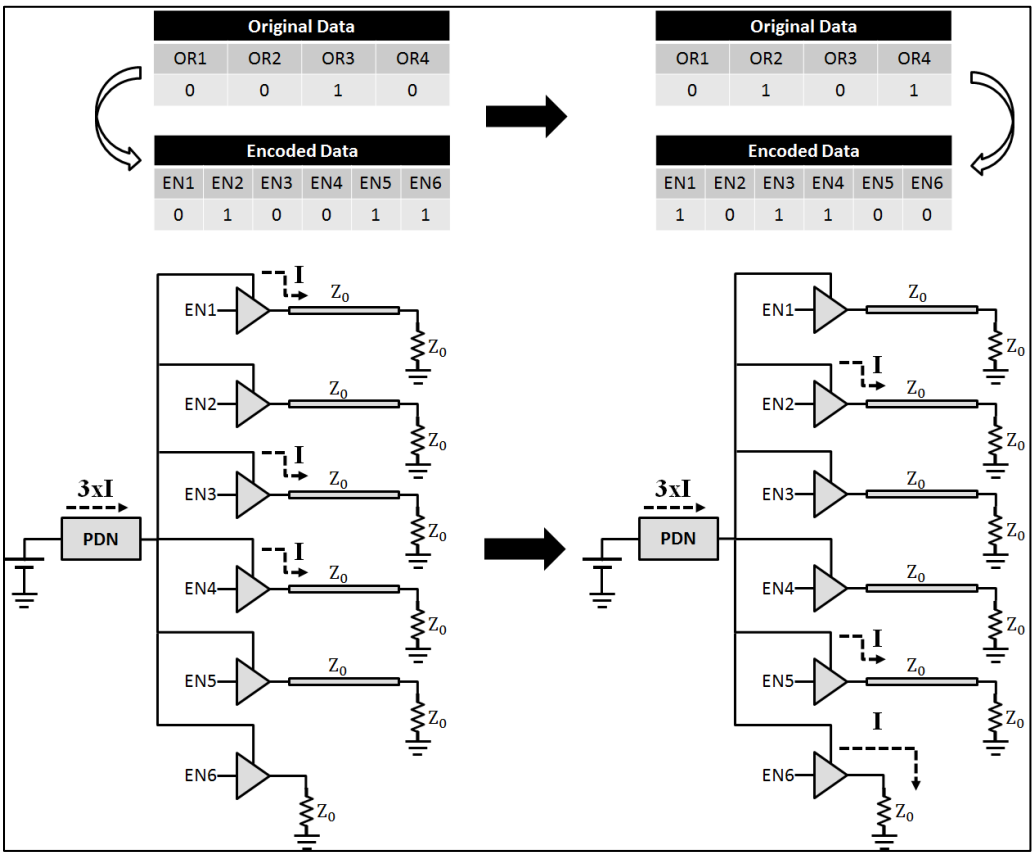


Figure 17 PB-PTL encoding scheme [45]

Test vehicles (TV) and a custom IC based on PTL and plane based PDN were made and results reported in [45]. Based on the TV measurement results, using the PB-PTL scheme reduces the p–p jitter by 10.5% and improves the eye height by 34.8% on average, as compared to using the power-plane PBS scheme in the test vehicle. In the IC measurement, the PB-PTL also produced better than 29% eye height improvement at data rate from 100 Mbps to 500 Mbps.

PB-PTL; however, requires additional hardware to implement the encoding circuitry. The hardware complexity scales up with the increased number of encoded data bits. These encoding hardware can consume additional energy and therefore has limited potential to improve the overall energy efficiency.

1.3.3 Constant Voltage Signaling with PTL (CV-PTL)

The voltage ripple on a PDN is due to varying impedance seen by the PDN as a result of the fast switching action of logic circuits. CV-PTL inserts an adjustable resistive network as shown in the dotted box in Figure 18 between the PTL and the driver circuit. Based on the load condition looking into the driver network, the resistive network selects the corresponding resistor, R[#], so that the sum of R[#] and R_{driver} remains constant regardless of the driver logic state. Therefore, the total impedance looking into the resistive network seen by PTL remains constant. As a result, minimal disturbance on the PTL voltage can be achieved.

Test vehicles fabricated based on constant voltage signaling are discussed in [47]-[48] and CV-PTL has been shown to consume approximately 55% less power than CC-PTL. The total peak to peak jitter could be reduced by up to 46% and supply noise was reduced by 44.7% as compared to using a power plane. However, compared to CC-PTL, CV-PTL was only shown to support up to 300 Mbps with acceptable signal eye as compared to gigabits per second data rate demonstrated in CC-PTL. This is limited by the low speed of the commercially off-the-shelf (COTS) switching and selecting logic to control the resistive network. Another factor that affect the performance of CV-PTL is that the resistor values in the resistor network was implemented in discrete values. However, the resistor values did not account for transitioning impedance during the period when the

load switch from one state to another. Although CV-PTL consumes reduced power, it requires a series resistor network to be always connected between the PTL and the load. This extra network consumes additional power that is not attractive in modern power conscious electronic systems. Furthermore, in extreme cases such as when the logic load is not sourcing any current, the resistor R[0] as shown in Figure 18 will take its place and sinks current that could otherwise be eliminated.

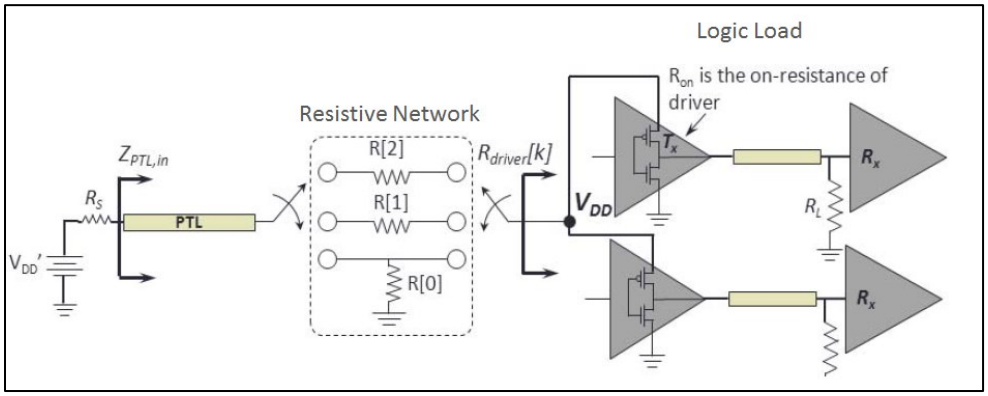


Figure 18 CV-PTL Illustration [48]

1.3.4 PTL in Mixed Signal Design

Mixed signal designs are very common especially in the all-encompassing consumer electronics that interface with the outside world through analog and RF electronics and process the converted digital signals at the backend. Since the analog and RF signals are much more sensitive and require very low noise environment, they require separate PDN away from noisy digital sources. The conventional separation method has been first identifying digital and analog domains and then physically separating the voltage rails and ground references or using filters for isolation [55]. Nonetheless, the “clean” or

analog ground and the "dirty" or digital ground will eventually join together somewhere in the system. The close proximity among the analog and digital domains further increases the risk of electromagnetic coupling leading to EMC and EMI issues [56] due to decreasing form factors in PCBs or packages. Electromagnetic bandgap (EBG) structures is another popular method for preventing EM coupling as shown in [58]-[59], however, EBG structure prove to be difficult when used in designs with high speed signal and high routing density [60]-[61].

PTL is fundamentally a transmission line which can be designed into band-pass or band-stop filters [57]. This property was explored and the PTL concept was recently applied to mixed signal electronics for minimizing the noise coupling between digital and RF circuitry, as shown in Figure 19. The PTL based design with isolation filter provided ~13 dB better than of isolation as compared to an EBG bandgap structure at 1.82 GHz, as shown in [54].

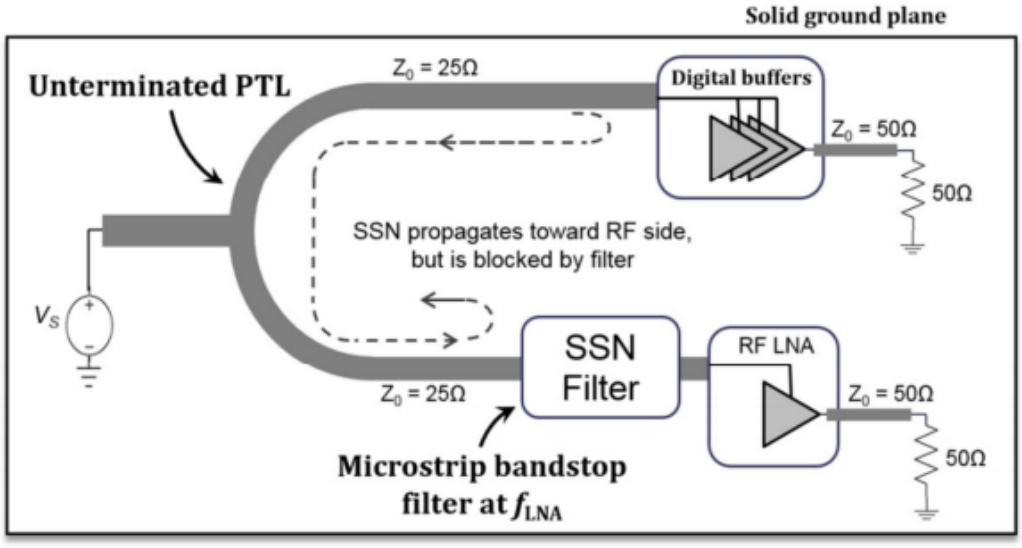


Figure 19 PTL used for power domain separation in a mixed signal design [54]

1.4 **Dissertation**

This dissertation presents the research work and outcome which represents the extension of work in [46]-[47]. First of all, the PTL concept, particularly the CC-PTL design, was applied to an advanced system. In the previous work, CC-PTL and CC-plane were implemented on a standard poker-card sized PCB board with a single high speed driver and one PTL with length less than 3" [44]. In this work, we first apply PB-PTL and CC-PTL to a stacked 3D IC level system that involves a PCB for main power delivery from a VRM to the die stack, a silicon-type interposer and three IC dies with logic and power network [62], as shown in Figure 20. Up to 4 drivers from each IC die were switched simultaneously. Plane based designs without utilizing PBS and CC signaling schemes were also modeled for comparison [62].

To show proof of concept, the 3D model was implemented using PCB technology by fabricating two separate systems each of which consisted of four stacked PCB boards consisting of three daughter cards and one motherboard [63], as shown in Figure 21. The first system was based on PTL PDN and the second was based on voltage-ground plane pair PDN. For comparison, constant current signaling schemes were implemented in both systems namely CC-plane and CC-PTL. Since the structure has a vertically growing dimension, the effect on SI and PI due to increased parasitic inductance from the interconnect between the boards was examined at each level of the stacked daughter card along with measurement of power supply noise and eye diagrams. Performance was also gauged and compared while running the system in several real world configurations such as in board-to-board communication. Since there were multiple drivers within the system,

effect of simultaneously switching multiple drivers on PSN was measured and analyzed. This is radically different as compared to the previous work in [44].

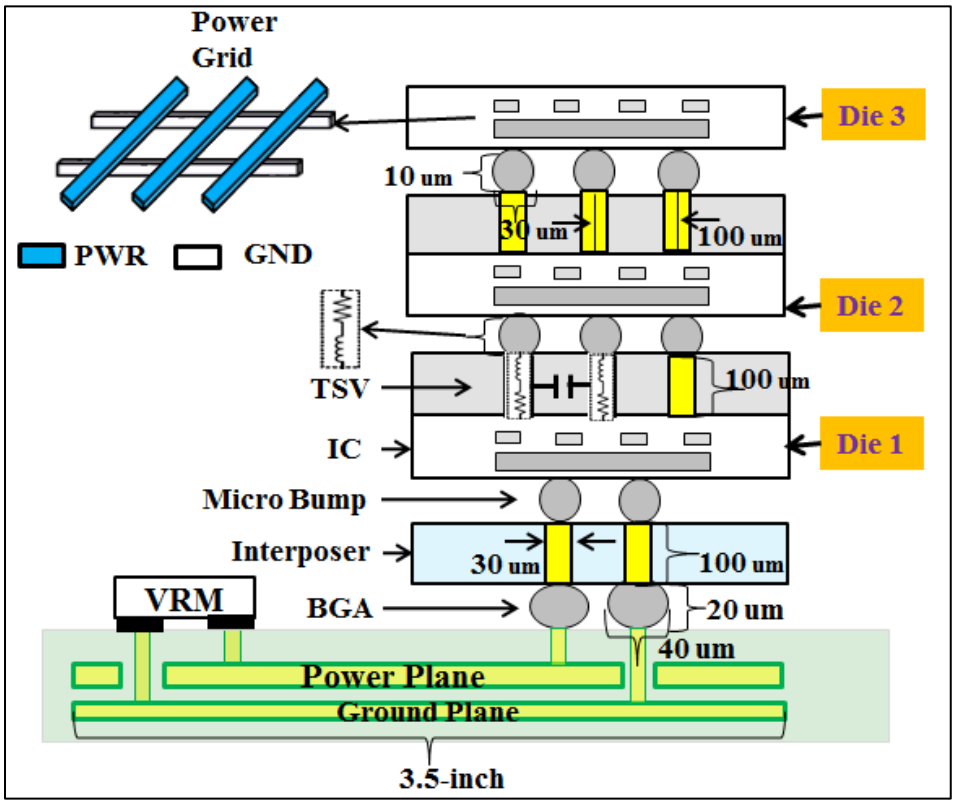


Figure 20 A cross-sectional view of a conventional power-plane based 3D-Stacked system [62]

In the second phase of the study, we closely examined and compared the electromagnetic (EM) coupling and crosstalk between power supply noise (PSN) and signal network for both PTL and plane based designs. Two signal routing topologies were studied, namely microstrip lines and via-transitioned lines. We correlated and quantified the measured EM coupling factor and coupled noise. The measurement results showed that

PTL based designs consistently produced lower than -40dB of EM isolation for a wide bandwidth of 6GHz as compared to its counterparts [65]-[66].

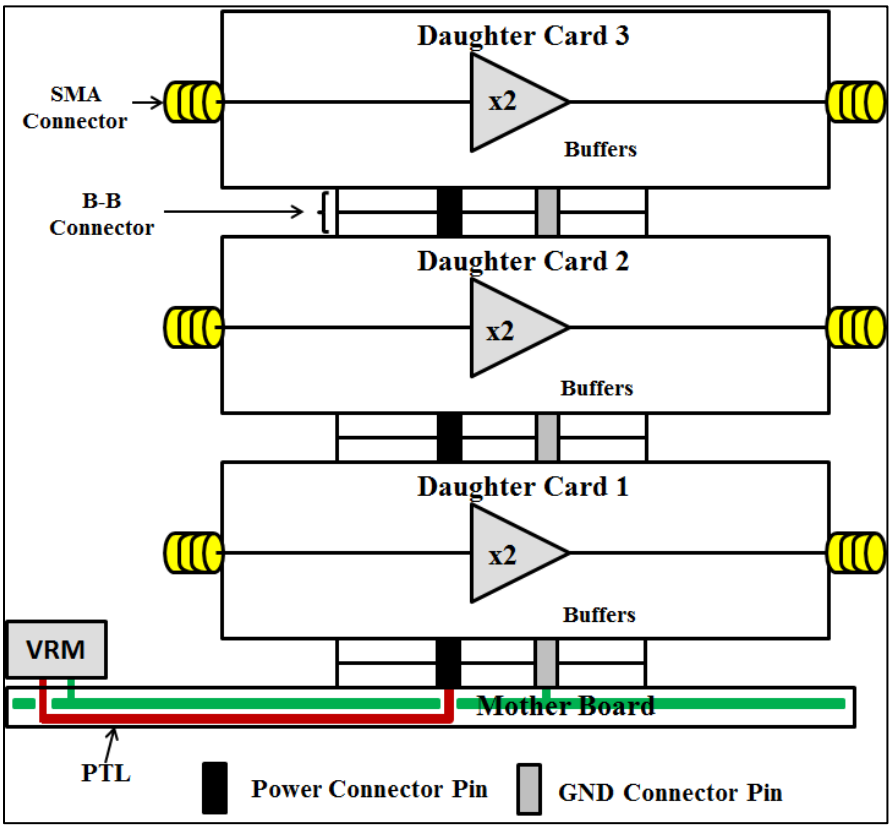


Figure 21 3D stacked CC-PTL test vehicle diagram

The core concept of CV-PTL relies on a tunable resistive network, which when closely examined, is similar to the core function of an LDO regulator circuit. However, there are two main differences. The first difference is the CV-PTL utilizes external hardware logic that is required to monitor the load condition and select the correct resistor value to complement the load impedance. This feedback action requires very fast switching

mechanism to minimize the time delay between load change and new resistor value selection. Due to the use of external component to implement such switching logic, the reaction time is slow which led to only 300 Mbps signaling speed being demonstrated. The second difference in CV-PTL is the tenability of the resistive network is digital in nature as there are only a certain number of resistor values within the resistive network, as shown in Figure 18. As shown in Figure 22, the LDO circuit uses a negative feedback network to monitor the output. When there is a change on the output voltage, the on-resistance of the PMOS is modulated by the error amplifier to compensate for the current sourcing or sinking action. The modulation is analog which means the on-resistance can be tuned in much finer scale as compared to CV-PTL. The LDO also has the capability to reject power supply noise from its input to output.

However, due to the gain-bandwidth limitation of the internal error regulating amplifier, the power supply noise rejection (PSR) capability of the LDO circuit begins to decrease when the loop gain of the regulating feedback loop decreases. The PSR reaches its worst value when the gain is at its 0 dB point, as shown in Figure 23. The effectiveness of PSR can be defined by (3),

$$\mathrm{PSR} = \frac{\partial V_{OUT}}{\partial V_{IN}} \qquad (\mathbf{3})$$

where ∂V_{IN} is the change in LDO voltage input, and ∂V_{OUT} is the corresponding change in V_{OUT} of the LDO.

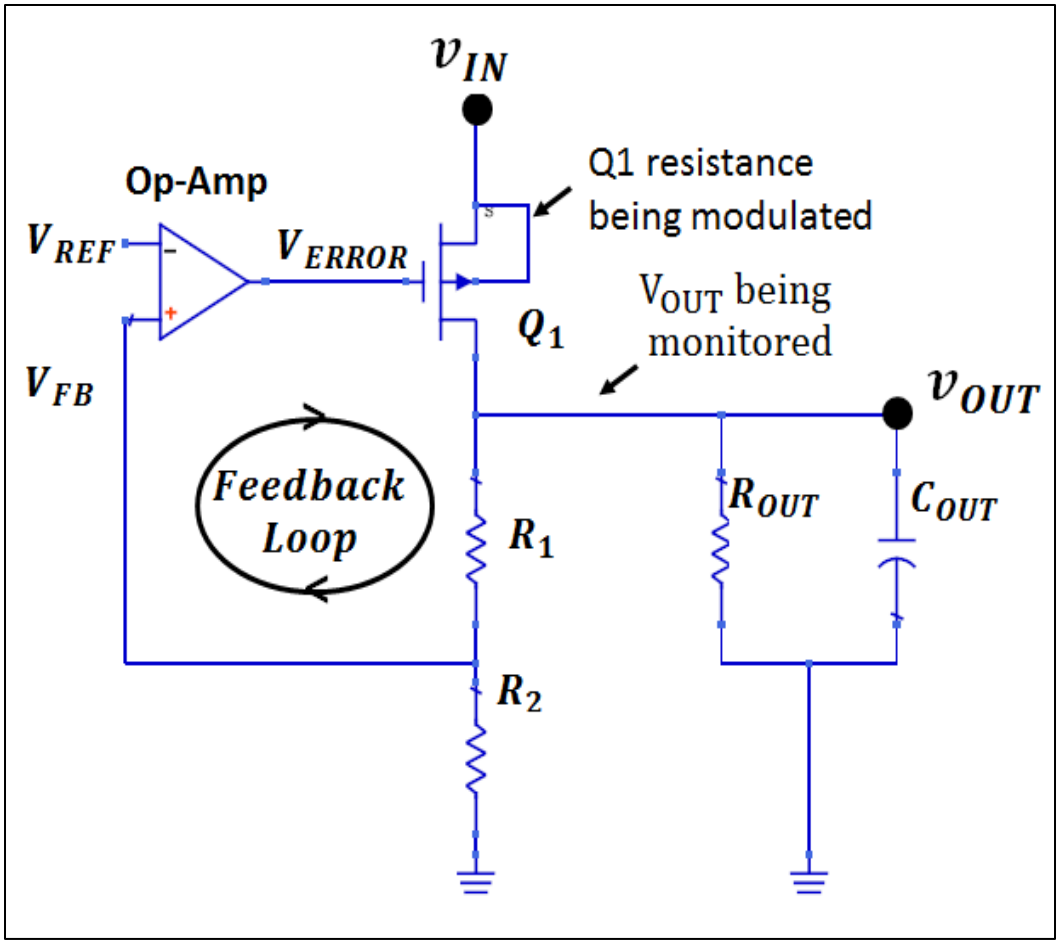


Figure 22 Internal circuit of an LDO

By comparing the loop gain plot with the plot of the PSR, one may see that at the f_{0dB} frequency, where the loop gain reaches 0 dB, the PSR starts to peak. This phenomenon is commonly referred to as PSR peaking. In the last phase of the dissertation, we take a unique approach by co-designing the PTL and LDO circuit to enhance the power supply noise rejection bandwidth of an LDO and improve overall energy conversion efficiency [67] as compared to using traditional power-ground planes to connect to an LDO circuit. To enhance the bandwidth, we utilize the inductive nature of the PTL and capacitors to create a low impedance resonance at the PSR peaking region where the PTL connects to

the LDO input. As a result, minimal amount of noise power, represented by the shaded spike in frequency band B3 where the PSR peaking occurs, will be seen by the LDO input, as shown in Figure 24. Hence less noise is coupled to the LDO output. Since less noise is coupled to the output due to the PTL, the dropout voltage of the LDO circuit can be lowered to reduce power consumed by the on-resistance of the PMOS transistor. We will show that the power saved by reducing the dropout voltage of the LDO greatly exceeds the power consumed by using the PTL due to its higher DC resistance as compared to using a voltage plane to carry the supply current.

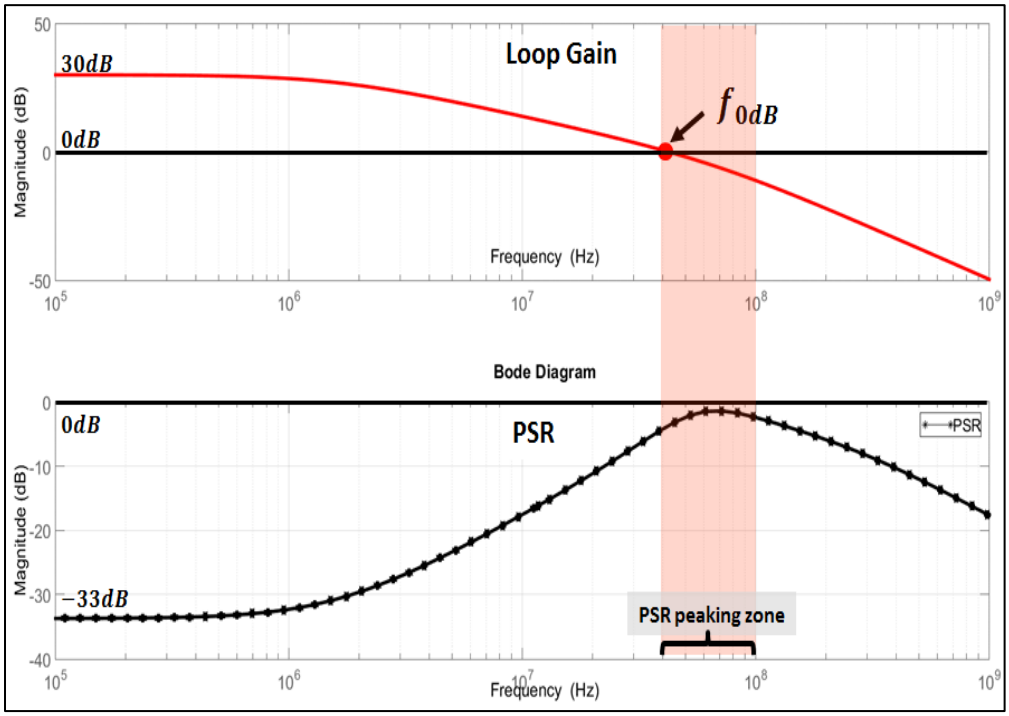


Figure 23 Relationship between loop gain of the error amplifier in an LDO circuit and its PSR

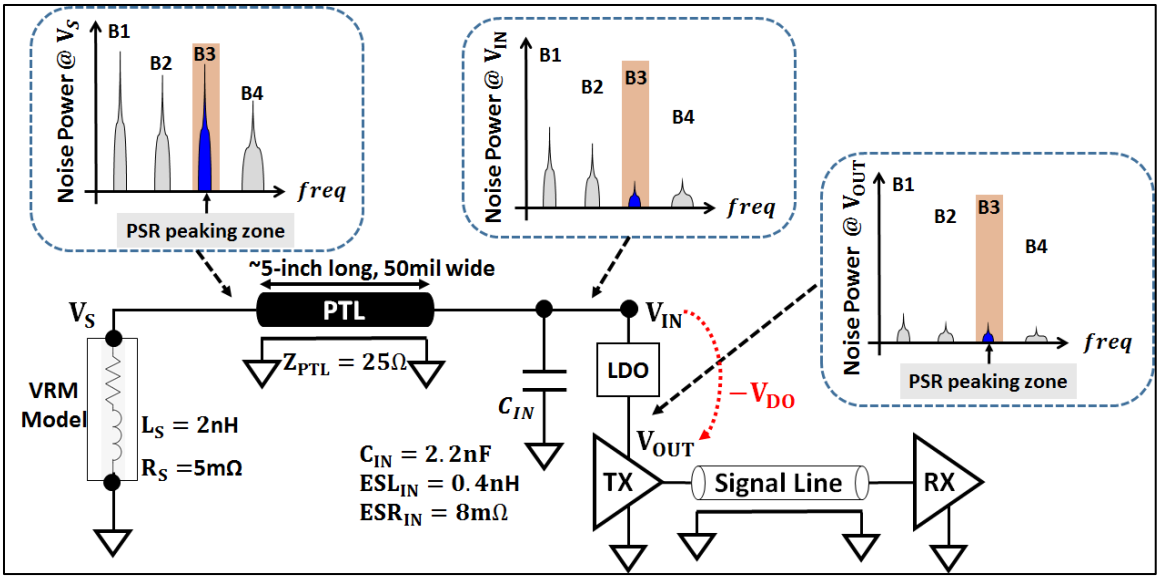


Figure 24 PTL and LDO design goal illustration

1.5 Contribution

The major contributions of the dissertation are as follows:

- A complete 3D model that incorporated a PCB with different PDN designs, a silicon interposer and 3 IC dies with power network and logic was developed. The model designed with PTL based PDN was used to study the signal and power integrity and compared with the conventional plane based model. In the CC-PTL test vehicle, the simulated eye height and jitter showed improvement of 15.1% and 36.3% respectively, and in the PB-PTL case, they improved by 68.7% and 24.2% respectively as compared to the conventional plane design [62]. The 3D model created was also instrumental in serving as a simulation and modeling platform for [48].
- Two complex test vehicle systems made of four stacked PCBs (three daughter cards and one mother board) with multiple drivers were designed to emulate conventional

and PTL based 3D systems. Each system involved two PCB designs, namely the daughter card and the mother board. The PDN of the first system was designed based on conventional power-ground plane pair approach while that of the second system was based on PTL concept. Each daughter card implemented CC-PTL, PB-PTL and CV-PTL signaling schemes. Each daughter card had four high speed differential buffers rated for 12 Gbps to simulate simultaneous switching scenario. SI and PI were demonstrated through real-world scenarios such as simultaneously switching multiple drivers, 3D stacking and board to board communication. A state-of-the-art, low skew (pair-pair skew < 10 mil) 1:16 fan-out board was designed to interface between a signal generator and the test vehicles to facilitate multi-driver testing. We successfully demonstrated the card to card communication from the first to the top most daughter card up to 3Gpbs with an eye height of 432 mV and a jitter of 143 ps. At this data rate, the eye closed for the plane based design. Six drivers, two on each daughter card, were also simultaneous driven and produced over 400 mV of eye height and less than 100 ps of jitter [63].

- The benefit of broadband electromagnetic isolation (less than -40 dB of isolation in a bandwidth of 6 GHz) between PDN and high speed signal networks offered by using PTL in PCB designs was demonstrated. Effect of EM coupling due to RPDs from high speed signal lines was quantified through measurement of power supply noise, as shown in [63], [65], [66]. These findings also provided the fundamental backing to the performance advantage of PTL based designs in power and signal integrity documented in [44].

- A unique solution to reduce the impact on power supply noise due to power supply rejection peaking of an LDO by co-designing PTL with an LDO circuit was developed. As shown through simulation, it was shown that PTL based architecture to connect a buck converter to an LDO circuit can offer both system-level high power supply noise rejection and improved energy conversion efficiency. Three proof of concept test vehicle PCBs were designed and fabricated based on PTL and voltage-ground plane PDNs. The PTL design was shown to provide more than 80% of reduction in power supply noise when compared with the other two plane based test vehicles [67].
- SSN in PTL and plane based designs were compared in [63]. RPD effect on crosstalk, SI and PI in both PTL based and voltage-ground plane based designs were quantified, measured and compared for the first time [65]-[66].

1.6 **Organization of the Thesis**

The thesis consists of 6 chapters. Chapter 2 provides a detailed overview of the CC-PTL design concept with an emphasis on test vehicle implementation. Additionally, CC-PTL, PB-PTL and conventional voltage plane based 3D IC-level models are demonstrated along with a discussion on their performance. Proof of concept 3D system based on PTL and its SI and PI performance were compared with conventional PDN design and demonstrated through several real-world data communication scenarios in Chapter 3. Chapter 4 presents the electromagnetic coupling comparison between PDN and high speed signaling networks between PTL and conventional plane based designs. Chapter 5 provides solutions to use PTL based PDN to improve power supply rejection bandwidth and energy

conversion efficiency for LDO circuits. Finally, a summary and future work are discussed in Chapter 6.

CHAPTER 2. MODELING AND COMPARISON FOR 3D INTEGRATION

2.1 Introductions

As the demand for smaller, faster and more power efficient Integrated Chips (ICs) based products grows from the industrial and consumer sectors, the size of the fundamental building block in ICs namely the transistors, is being pushed down to the sub-nanometer region. One of the major limiting factors to the performance of high speed systems today is simultaneous switching noise (SSN) which is contributed by parasitic inductance from interconnects and high current transients flowing through these interconnects.

In a 3D IC system multiple chips are stacked together by means of Through Silicon Vias (TSV) and micro bumps. The stack is then soldered onto a Printed Circuit Board (PCB) through an interposer or package. The addition of structures such as TSV and solder bumps further contribute to the existing parasitic inductance of the overall structure. As demonstrated in [69], the inductance increases from a lower die to the next higher die along the stack. This in turn causes increased power supply noise (PSN) and jitter, and decreased eye height as the position of the die in the stack increases, as shown in Figure 25.

A common method to lower impedance and reduce power supply noise is to add decoupling capacitors between power and ground rails. However, there are several disadvantages to this approach. First, the capacitors themselves can add self and loop inductance to the overall system due to its physical dimension and loop area formed between the capacitors and the circuit. Second, adding decoupling capacitors do not always help the design to meet the impedance target in ICs with high inductances, as shown in

[69]. Third, decoupling capacitors take up valuable real estate on ICs which can be otherwise used for other purposes such as placing TSVs.

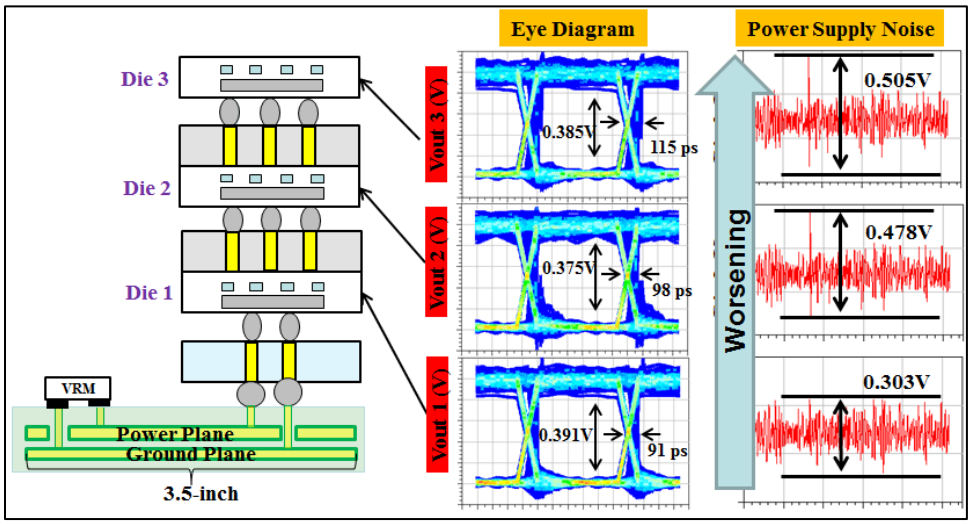


Figure 25 A cross-sectional view of a conventional power-plane based 3D-Stacked system and its simulated eye diagram at the receiver end on each of the three dies with 3 Gbps PRBS data.

In conventional PCB designs, power and ground planes are used for power delivery. However, the power planes cause return path discontinuity (RPD), which induces power supply noise and coupling between the signal distribution network and the power delivery network (PDN) [44]. In this work we apply the PTL in the PCB to connect the VRM to the PDN. This enables the elimination of return path discontinuities, thereby creating a high impedance conduit for supplying the charge to the 3D stack. To manage the inductive effect in the die stack we rely on current steering (CC-PTL) and pseudo-balanced coding (PB-PTL) to keep the PTL always charged which neutralizes the effect of inductance, leading

to near zero noise in the PDN. Through simulation we show that high speed signaling between the dies in the stack is possible with minimum jitter and maximum eye height with the PDN we proposed.

2.2 CC-PTL Signaling

The CC-PTL concept contains two main features. The first one is the replacement of the voltage plane with a power transmission line to carry power from the source to the load. PTL can achieve high SI and PI by reducing return path discontinuities (RPD) [44]. Figure 10 shows an example of the stack-up based on a conventional PDN design that use a power-ground plane pair. A signal trace referenced to the power plane in this case leads to the return current flowing on the top surface of the power plane, which follows the path of the forward signal. The signal trace terminated at the far-end at the receiver side (RX) causes the forward current to flow into ground plane. The undesired and interrupted transition of return current from ground to power plane as shown in the figure forces RPDs and can lead to issues such as ground bounce and simultaneous switching noise [6],[9]. In the proposed design, as shown in Figure 11, power plane is replaced by PTL which is an impedance controlled transmission line that is used to transport power from a power source to its load. The PTL can be laid out on the same layer as the signal traces so that a complete and smaller current loop is formed between the forward and return path. As a result, there is no interruption in the current flow loop that would otherwise lead to RPDs. A source termination resistor can be added between the VRM and the PTL to dampen any reflection from the load. However, this resistor will consume additional power which is undesirable as previously mentioned for the CV-PTL scheme [48]. Additionally, in the case of CC-

PTL, current transient is kept low on the PTL therefore reflection due to impedance mismatch is minimized.

The second feature of CC-PTL concept is the implementation of a constant current mechanism through current steering. It is achieved by adding an impedance-matched complementary path to the signal path, which is similar to the workings of a differential driver, as shown in Figure 26. However, since the complementary path is locally terminated to ground, high speed single-ended signaling is possible. The purpose of implementing constant current signaling are to 1) minimize current transient on the PTL, and 2) alleviate mismatch effect between the PTL characteristic impedance and connecting components [44]. Since differential drivers were used in the test vehicle design discussed later, we use a simple differential driver model made up of two identical npn bipolar junction transistors (BJT) to explain the CC-PTL signaling concept.

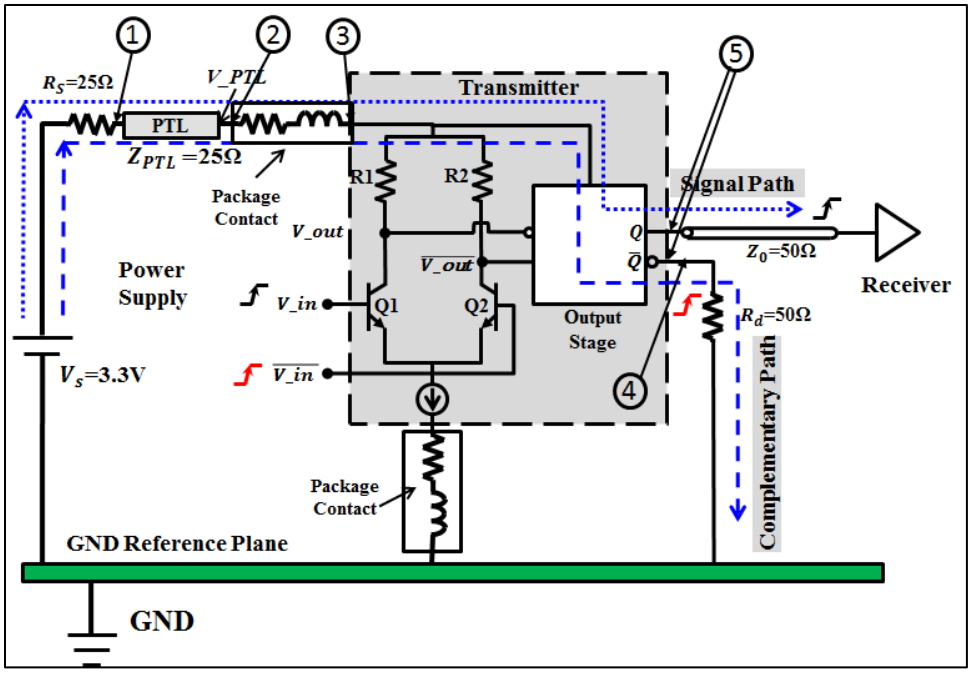


Figure 26 Constant Current Power Transmission Line scheme

To achieve minimal current transient and energy reflection, transistors Q1 and Q2 needs to be matched and resistors R1 and R2 should be equal in Figure 26. However, in a real implementation, there will be mismatch between impedances at locations such as those indicated by circled 1, 2, 3 and 4, as shown in Figure 26. Additionally, the capacitive and resistive loads seen by the output stage of the transmitter between the two complementary outputs are also different as indicated by circled number 5. All of these imperfection and mismatch will cause additional noise fluctuation on the PTL.

As shown in Figure 26, the bases of Q1 and Q2 are connected to the input signal, V_in, and the complementary signal, $\overline{V\_in}$, of the transmitter, respectively. The collector terminals of the differential stage are connected to transmitter inverting output stage. The positive terminal of the output stage drives a transmission line with a 50 Ω characteristic

impedance to the receiver. The inverting output, $\bar{Q}$, is locally terminated to ground through R_d, a 50 Ω resistor. Therefore, either output of the last transmitter stage drives the same impedance load.

When *V_in* transitions from logic low to high, Q1 in the transmitting buffer turns on and *V_out* goes low. Current follows the signal path as shown by the dotted line in Figure 26 flows from the PTL through the output stage into the signal transmission line thereby charging it. During the following clock cycle when *V_in* switches from high to low, the signal line is discharged. During this time, transistor Q2 turns on causing $\overline{V\_out}$ to go low and the inverting output $\bar{Q}$ transitions from low to high. As a result, the current is steered from the PTL into the termination resistor R_d following the complementary path as shown by the dashed line in Figure 26. The advantages of the signaling scheme illustrated in Figure 26 are the following: a) the cavity resonances between the voltage and reference planes are eliminated; b) the flow of current between the signal line and reference plane is always continuous, thereby eliminating RPDs; c) due to current steering, the PTL is constantly charged thereby minimizing the current transient impact on the PTL and d) the effect of process variations on signal integrity is minimized [44]. As a result of utilizing the complementary path that includes R_d, additional power is consumed. There is DC drop associated with using PTL and power dissipation through the source terminating resistor, R_s. The DC drop is a function of the current being drawn and can be controlled by optimizing the line width. In all the test vehicle designs found in this thesis, which will be described in a later chapter, the characteristic impedance of the PTL was set to 25 Ω unless noted otherwise and left unterminated (R_s = 0 Ω) to reduce power consumption thereby causing some reflections. However, the reflection is minimal due to the use of high end

differential driver and carefully matched signal lines during routing. There are a few factors that affect the choosing of the characteristic impedance of the PTL. Firstly, the impedance value needs to be chosen close to the on-resistance of the differential driver. However, this is not usually listed in the datasheet of a high speed driver. The second factor is the allowed DC voltage drop due to the resistance of the PTL which in turn depends on the geometry of the PTL. A detailed analysis on the tradeoff between PTL geometry and DC drop was discussed in [47]. In this case, 25 Ω was chosen for ease of routing and low DC drop, which was 9.7 mΩ per inch according to simulation result.

Figure 26 is similar to differential signaling except that only a single transmission line is routed at the output of the buffer. This reduces routing congestion for complicated designs, and eliminates the fiber-weave effect [26], [70] that causes skew for differential lines. To compare the signal quality between unmodified differential and constant current signaling in measurement, the performance of both cases by comparing their eye diagrams will be demonstrated in Chapter 3.

2.3 **PB-PTL Signaling**

The PB-PTL signaling scheme was detailed in [45] and described in Chapter 1. A four to six bit encoding scheme was utilized. However, in order to simplify the circuit in the simulation model, the encoding hardware was not implemented. Instead, six driver circuits were implemented on each stack of the 3D model to transmit the encoded bits. The bit streams feeding to the drivers were managed to ensure that the number of logic 1's and 0's are the same at any given transmitting interval. The transmitted bits from each lower stack were then sent to the inputs of the drivers on the next higher stack.

2.4 Simulation Model Description

The 3D system considered here consists of a PCB, an interposer and three IC dies, as shown in Figure 25. Each die size is 1mm x 1mm. Each IC contains a TSV layer, PDN and digital logic. The TSV layer is modeled based on [71]. It consists of three TSVs; power, signal and ground TSVs. The Interposer model was constructed using a 3D EM solver [72]. It contains a power and ground TSV pair. All TSVs are surrounded by 0.1 um thick oxide layer. The micro bumps and BGA balls between layers are modeled as a resistor in series with an inductor. Resistance and inductance of BGA balls are 2.4 mΩ and 6.44 pH respectively while those of micro bumps are 2.8 mΩ and 0.8 pH respectively. Dimensions of TSV, BGA and micro bumps are shown in Figure 25. The PDN contains power and ground grid corresponding to the top metal layers in the IC. In each grid, the rails are laid out orthogonally in two separate layers separated by 40 um with rail width of 40 um. Each grid is divided into unit cells with individual cell size 200 um x 200 um, as shown in Figure 27. Each cell is modeled as two separate resistor networks with resistance in each branch (R_b) calculated to be ~51 mΩ. The coupling capacitance between power and ground rails within a cell is approximated to be 4.2 fF. The PCB for the conventional power plane-based design is a two layer board with the power plane on the top and ground plane on the bottom layer. The PCB model was created using Sphinx [73]. The PCB for CC-PTL and PB-PTL cases was modeled as a two layer board and laid out as a microstrip structure. The PTL is a microstrip line of length 2.76-inch referenced to the ground plane that connects the VRM to the stacked IC in the PCB, as shown in Figure 28.

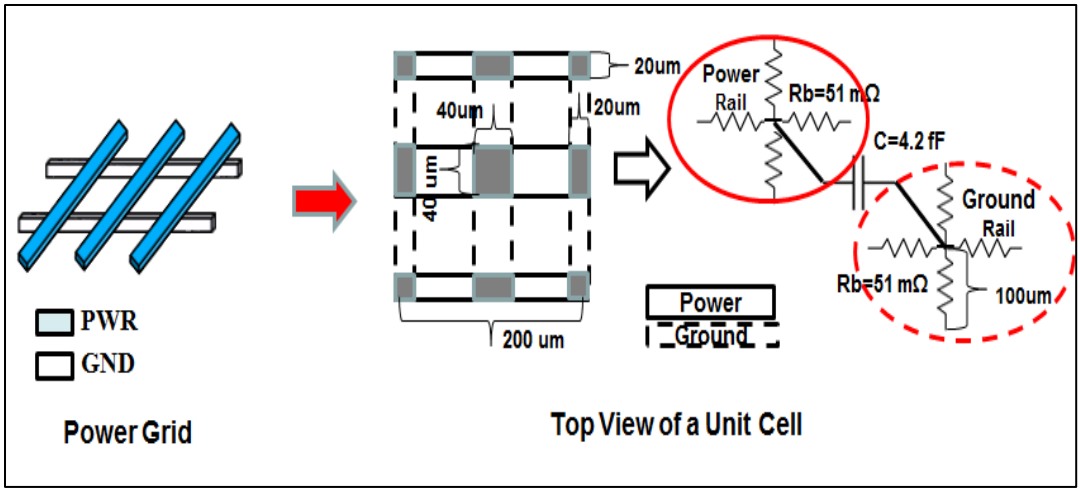


Figure 27 Power grid unit cell structure and lumped circuit model

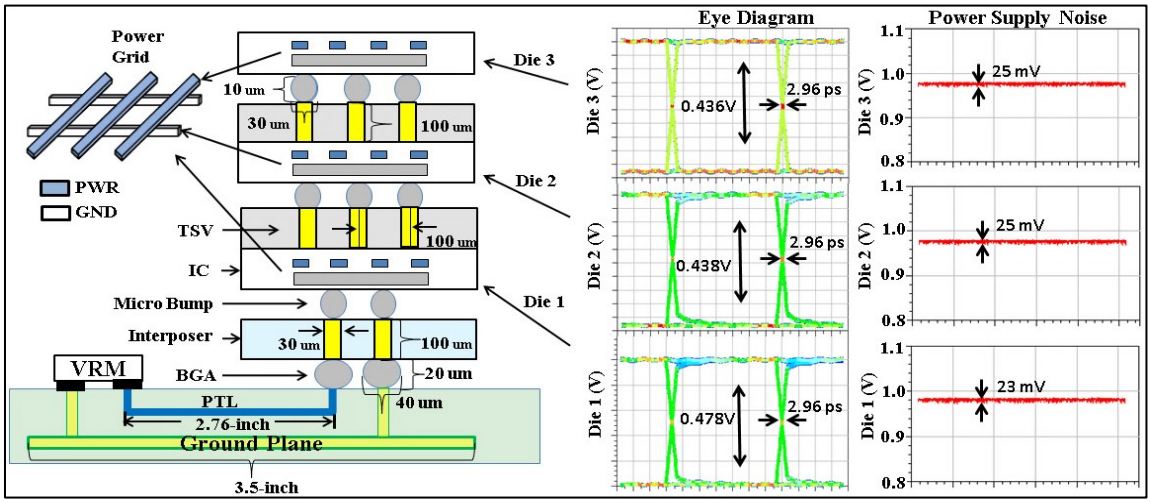


Figure 28 A cross-sectional view of a conventional power-plane based 3D-Stacked system and its simulated eye diagram at the receiver end on each of the three dies with 3 Gbps PRBS data.

The impedance profile of the power rail for each of the three IC dies in the conventional power plane based design model from 0.1 to 10 GHz is shown in Figure 29.

As can be seen, the impedance in the inductive region increases as the position of die in the stack increases. This trend is also corroborated by [69]. As a result of this increased inductance, the power noise will increase as the position of the die in the stack increases. This phenomenon is reinforced by the study detailed in [74]. From Figure 25, with a 3Gbps, 12-bit pseudo-random bit stream (PRBS), the eye diagram deteriorates as one goes up the stack due to an increase in the power supply noise.

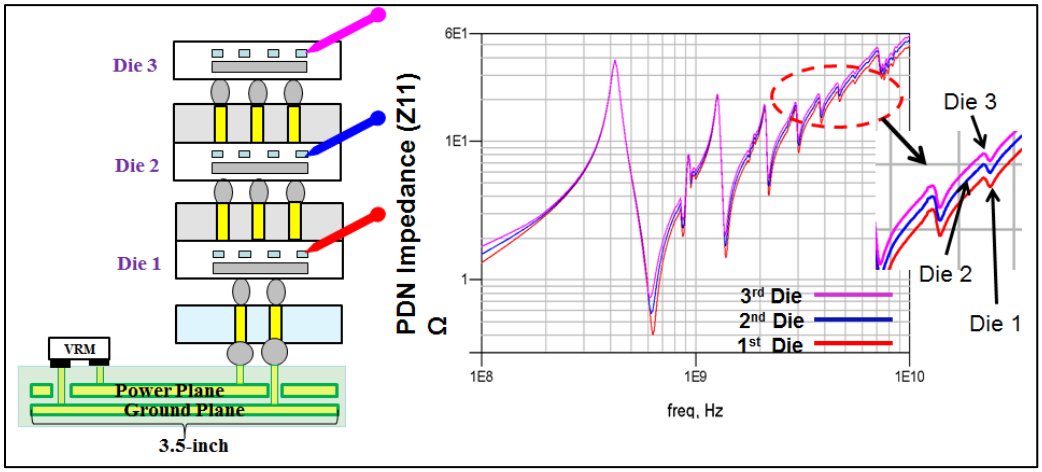


Figure 29 The impedance profile of the conventional power-plane based design.

2.5 Performance of CC-PTL and PB-PTL in 3D Systems

Three test cases were generated to compare the performances between a conventional design, CC-PTL and PB-PTL using the models described previously. In all three cases, driving signals are fed into digital logic on the bottom most die which then transmits them up to the logic in the upper dies. Supply voltage to PTL is set to one volt. Each eye measurement was taken at the far end of a signal (Vout) which was terminated

using a 50 Ω resistor to ground, as shown in Figure 30. Table 4 compares the eye height, jitter and power supply noise of all three stacked dies for all the three cases.

2.5.1 Case 1: 4 Gbps clock signal

In this case, the performance of the conventional and CC-PTL designs were compared by feeding them with a 4 Gbps clock signal. Figure 31 shows the eye diagram measured on the 3rd die. The measured eye height in CC-PTL was 0.486V and the p-p jitter was 2.28 ps. The eye height was improved by 12% and p-p jitter improved by over 90% as compared to the plane-based PDN design. The power supply noise for the CC-PTL case was lowered by over 90%, as shown in Table 4.

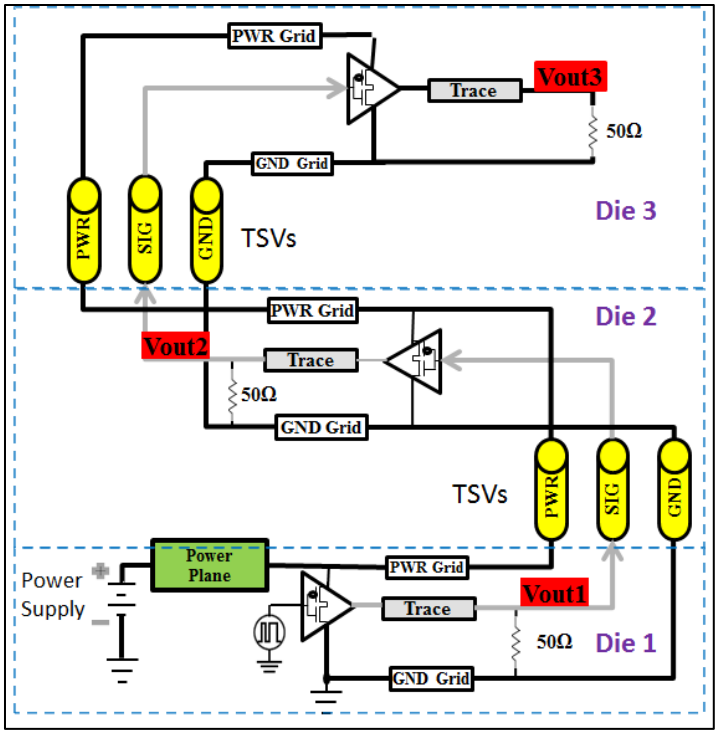


Figure 30 CC-PTL Circuit Schematic for 1-Bit Signal.

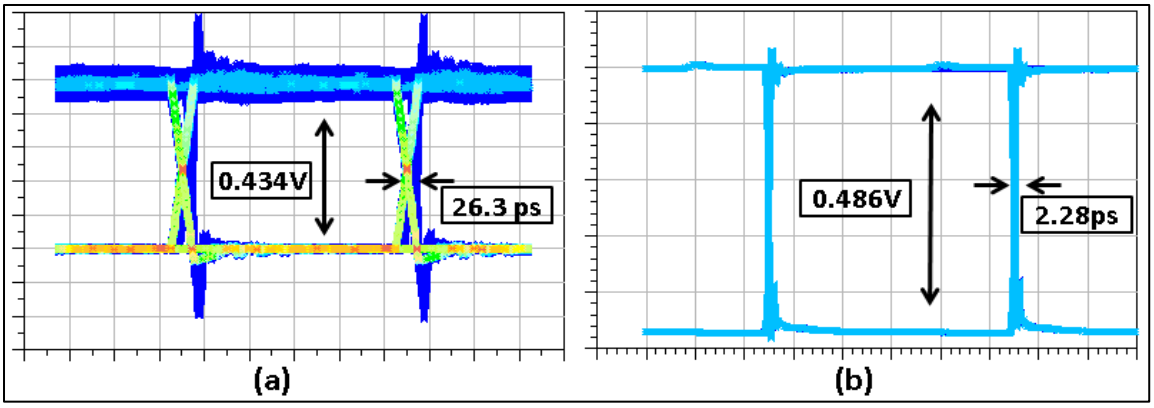


Figure 31 Simulated eye diagram of 4 Gbps clock signal on die 3. (a) conventional and (b) CC-PTL based designs.

2.5.2 Case 2: 12-Bit, 3Gpbs Random data.

A 12-bit bus carrying PRBS at 3Gpbs was fed into the CC-PTL and conventional power-plane based designs separately. Figure 28 shows the eye diagram for signaling and power supply noise levels in all three dies. Compared with Figure 25, the eye height was increased by 13.3%, p-p jitter and worst case power supply noise were reduced by 97.4% and 95.1% respectively at the 3rd die, as shown in .

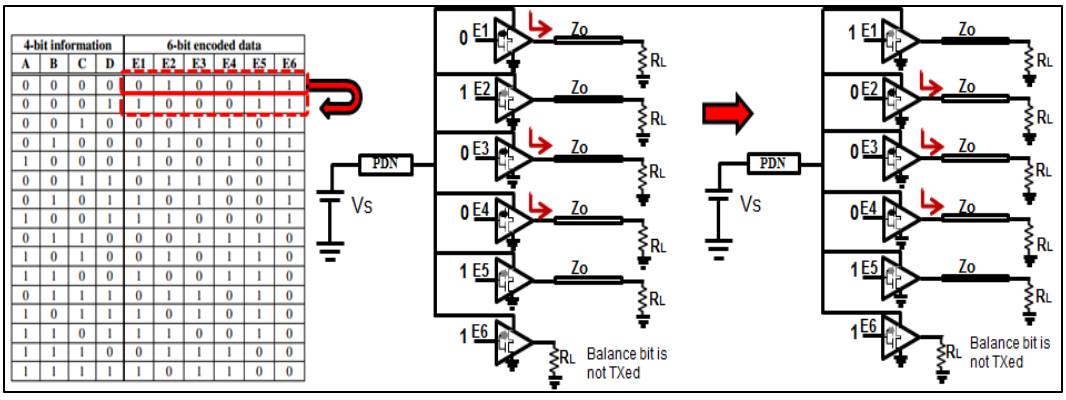


Figure 32 An example of PB-PTL based encoding and data transition. n=4, m=6.

2.5.3 Case 3: PB-PTL Using 4/6Bit Encoding.

Performance of PB-PTL versus conventional design was examined in this case. Here every 4-bit original data is encoded into 6-bit, as shown in Figure 32. Encoded bit rate was set to 3Gbps. The simulated schematic is shown in Figure 33. Figure 34 shows the eye diagrams measured on die 3. The measured eye height in PB-PTL improves by ~16.7%, p-p jitter and power supply noise reduce by 95.9% and 93.4% respectively as compared to the conventional design. The simulated results across all three stacks is summarized in Table 4.

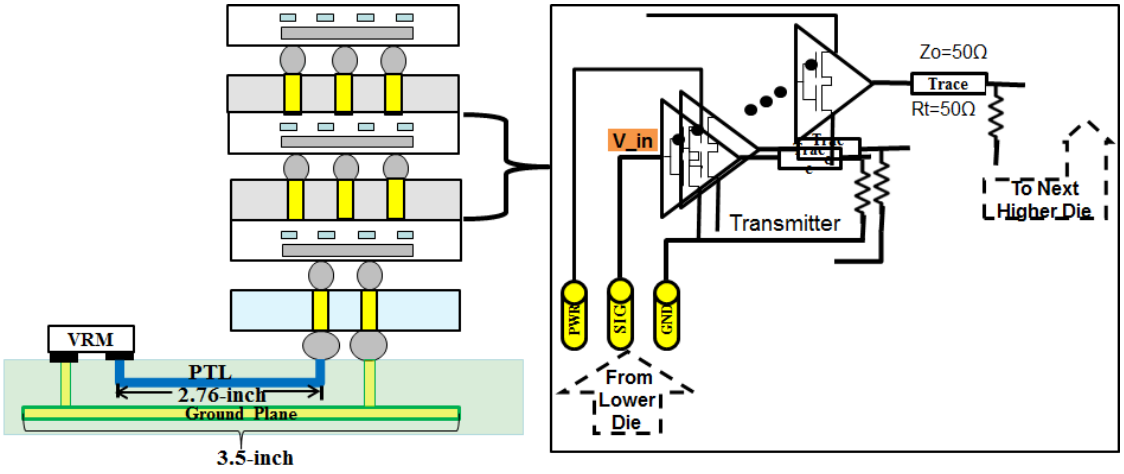
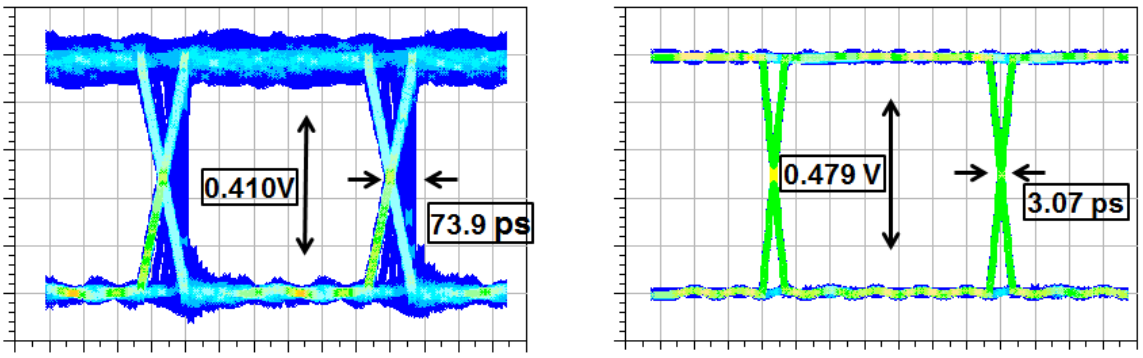


Figure 33 Simulated PB-PTL in the 3D Model



(a) Eye on 3rd Die in Conventional PDN Based Design

(b) Eye on 3rd Die in PBPTL based Design

Figure 34 Simulated eye diagrams of a) power plane based and b) PB-PTL designs in case 3

Table 4 Performance comparison between PTL and conventional designs in the 3D IC Model

		Eye Height (V)			P-P Jitter (ps)			PSN (V)		
		CNV*	CC-PTL	% Δ	CNV*	CC-PTL	% Δ	CNV*	CC-PTL	% Δ
Case 1	Die 3	*0.434*	*0.486*	*12.0*	*26.3*	*2.28*	*-91.4*	*0.395*	*0.024*	*-93.9*
	Die 2	*0.444*	*0.482*	*8.56*	*20.6*	*2.28*	*-88.9*	*0.386*	*0.021*	*-94.6*
	Die 1	*0.440*	*0.486*	*10.5*	*23.0*	*2.22*	*-90.4*	*0.362*	*0.020*	*-94.5*
		CNV*	CC-PTL	% Δ	CNV*	CC-PTL	% Δ	CNV*	CC-PTL	% Δ
Case 2	Die 3	*0.385*	*0.436*	*13.3*	*115*	*2.96*	*-97.4*	*0.505*	*0.025*	*-95.1*
	Die 2	*0.375*	*0.438*	*16.8*	*98.0*	*2.96*	*-97.0*	*0.478*	*0.025*	*-94.8*
	Die 1	*0.391*	*0.478*	*22.3*	*91.0*	*2.96*	*-96.8*	*0.303*	*0.023*	*-92.4*
		CNV*	PB-PTL	% Δ	CNV*	PB-PTL	% Δ	CNV*	PB-PTL	% Δ
Case 3	Die 3	*0.410*	*0.479*	*16.8*	*73.9*	*3.07*	*-95.9*	*0.394*	*0.026*	*-93.4*
	Die 2	*0.412*	*0.473*	*14.8*	*74.4*	*3.07*	*-95.9*	*0.358*	*0.030*	*-91.6*
	Die 1	*0.415*	*0.474*	*14.2*	*63.6*	*3.07*	*-95.2*	*0.262*	*0.022*	*-91.6*

*CNV=Conventional Power Plane Based Design

2.6 Summary and Conclusion

Proof of concept test vehicles for CC-PTL and PB-PTL were previously presented and compared to the conventional design in [44] and [45]. In the CC-PTL test vehicle, the

eye height and jitter measurement showed improvement of 15.1% and 36.3% respectively, and in the PB-PTL case, they improved by 68.7% and 24.2% respectively as compared to conventional design.

In this work we applied PTL concept to a 3D IC system that included PCB-based power distribution network, a silicon based interposer and 3 stacked IC dies. A conventional plane based PDN was also simulated for comparison with PTL based model. We demonstrated through simulation that power supply noise worsens as we go higher up in the stack of dies. Nonetheless, both the CC-PTL and the PB-PTL showed considerable improvement in power supply noise (PSN), eye height and p-p jitter as compared to the conventional design, as shown in Table 4. These measurements confirm the validity and possibility of CC-PTL and PB-PTL design concepts for 3D systems.

CHAPTER 3. APPLICATION OF CC-PTL TO COMPLEX PRINTED CIRCUIT BOARDS MIMICKING 3D SYSTEMS

3.1 Introduction

In the previous chapter, CC-PTL and PB-PTL concepts were applied to a 3D stacked IC system to demonstrate the viability of PTL based PDN in a 3D environment through simulation. Since CC-PTL was successfully demonstrated to run at gigabit speed in a simple PCB based test vehicle with good SI and PI performance [44], CC-PTL was selected to be applied to two complex PCB-based systems that mimic 3D systems, with PTL and conventional plane based PDNs.

The work published on CC-PTL [44] so far has been limited to simple test vehicles consisting of 1) a single integrated circuit (IC) chip containing either a single gigabit data high speed buffer or four sub-megahertz buffers, ii) short interconnect lengths of no more than a few inches, and iii) a single Printed Circuit Board (PCB) with a stack-up of either three or four layers and with the signal lines routed on a single layer. In this chapter we apply the PTL scheme to a complex test vehicle consisting of i) six individual high speed buffer ICs capable of switching simultaneously, ii) approximately 12” long interconnections, and iii) three daughter cards stacked on a motherboard via highly inductive sockets. By implementing the Constant Current PTL (CC-PTL) [44], [63] which was explained in detail in Chapter 2, we demonstrate that up to 3 Gbps of signal speeds is possible with minimum jitter, large eye opening and minimum power supply noise..

In this chapter, we provide extensive results that include: i) demonstration of the signal quality on stacked daughter cards as the parasitic inductance increases, ii) the effect on power supply noise when the buffers are driven synchronously and asynchronously, iii)

comparison of signal integrity between the top and bottom daughter cards in a stacked structure, and iv) signal quality in the scenario of card to card communication at various gigabit data rates. This PTL implementation scheme is then compared to a power distribution scheme that uses voltage-ground planes.

3.2 Test Vehicle and Fanout Board Design

3.2.1 Printed Circuit Board Description and Characterization

The test vehicle includes two separate PCB designs; one is the motherboard and the other is the daughter card, as shown in Table 5. The test vehicle consists of three daughter cards and one motherboard stacked vertically using board-board (B-B) connectors, as shown in Figure 35. (Figure 35 is similar to Figure 21 with additional PCB dimension information) All PCB designs are 4-layer boards. The stack-up information is shown in Figure 36. The top and bottom layers were used for component placement, signal and PTL routing. The middle two plane layers were used as ground (GND) reference planes.

Table 5 Test Vehicle Information

Test Vehicle	PCB Design (Qty.)	PCB Stack-up (common to all designs)
CC-PTL	Motherboard: 1	--SIG-- --GND-- --GND-- --SIG--
	Daughter Card: 3	

The overall thickness of each PCB was approximately 62-mil. The dimension of the motherboard was 7.3-inch x 4.0-inch and that of the daughter card was 4.8-inch x 14.1-inch. The dielectric material of the PCBs was FR4 Tg130 material with a dielectric constant

of 4.5 [75]. A loss tangent of 0.025 was used during simulation of a 50 Ω microstrip transmission line. Based on Isola Tg130 series data sheet [76], the permittivity is 4.37 and loss tangent is 0.022 at 1 GHz.

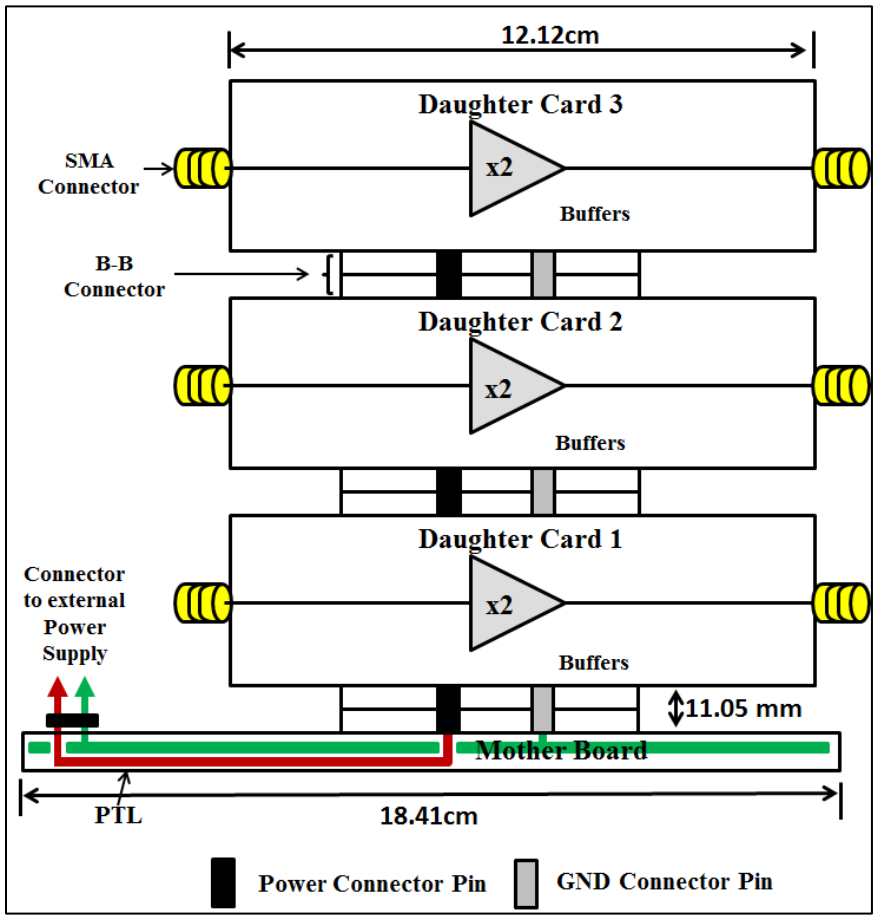


Figure 35 Illustration of stacked test vehicle

To compare the impedance of fabricated microstrip lines with simulated impedance results, Time-domain Reflectometer (TDR) measurement was done. A TDR measurement of a 50 Ω microstrip transmission line on the daughter card is shown in Figure 37. The TDR system is connected to one of the female SubMiniature Version A (SMA) connectors

which connects to an approximately 3.75 inches long microstrip transmission line which ends at the output of a buffer on the daughter card. However, the buffer was removed during TDR measurement and hence the transmission line was open circuited at the other end. The TDR launches a step with a rise time of 35 ps into the SMA connector. Figure 37 is an illustration showing the impedance profile from the TDR measurement which consists of the SMA connector and the transmission line. We observed that the variation of the transmission line impedance is within +/-15%.

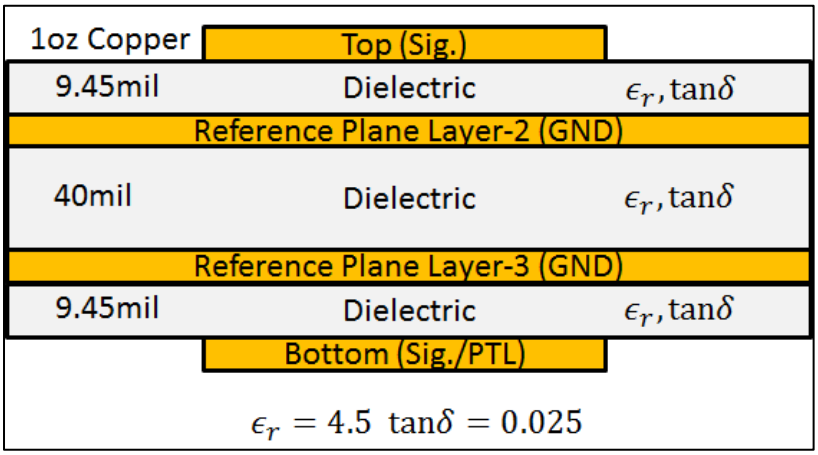


Figure 36 Test vehicle PCB stack-up

The PTLs were routed as 50-mil wide microstrip lines which had an impedance of 25 Ω. The length of PTLs from the point of power entry to the different I/O buffers varied with the longest being approximately 11.68 inches and shortest being approximately 7.89 inches.

The B-B connectors were surface mount connectors that were designed to carry power and ground return signals. The mating height of the B-B connector was 11.05 mm.

Each connector had 20 pins arranged in two rows, as shown in Figure 38. The cross section of each pin was 0.64 mm x 0.64 mm with a pin-pin pitch of 2.54 mm.

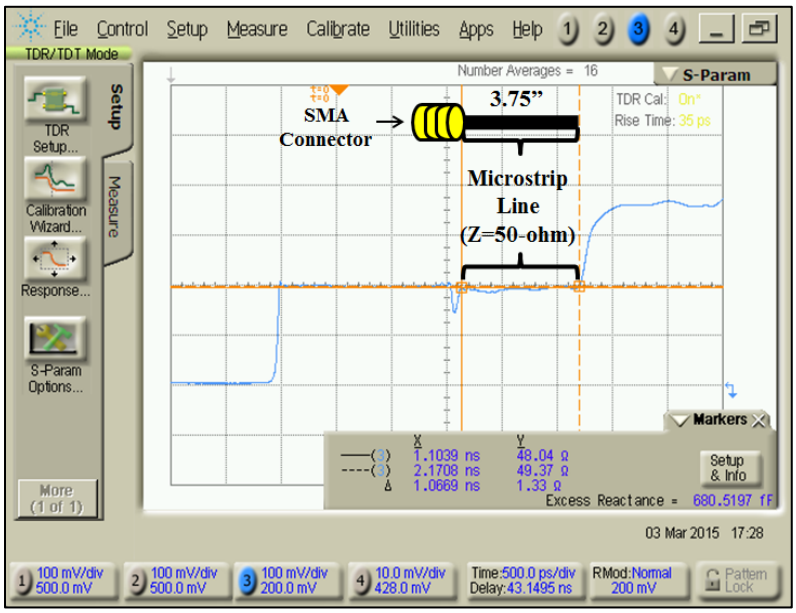


Figure 37 TDR measurement of impedance of a microstrip signal line in a daughter card on the top layer.

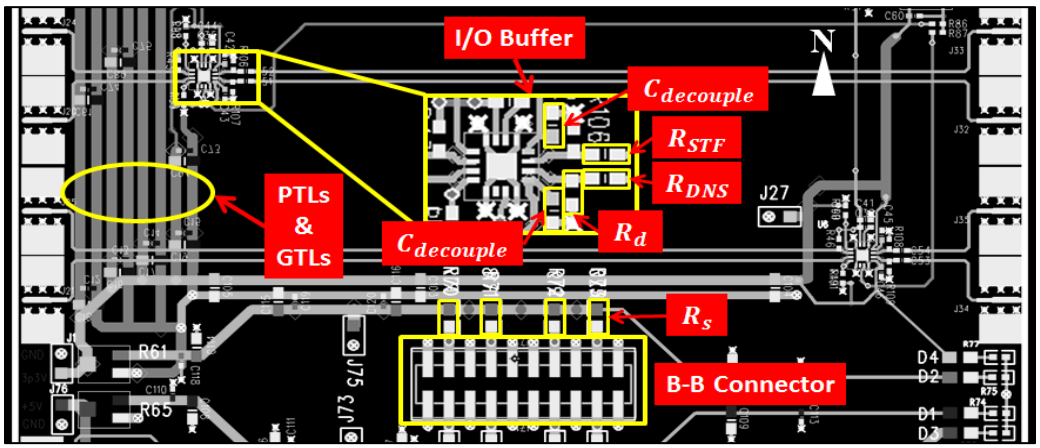


Figure 38 Portion of a PTL-based daughter card showing main components

3.2.2 Schematic Design and PCB Layout

All PCBs in the test vehicle share the same power and ground supply rails through the B-B connectors. For this chapter, only the top row pins of the B-B connectors were used for supporting the on-board operations. The pins were alternatively assigned to GND and 3.3V to ensure each power pin has two ground pins on either side of it to provide close ground reference and shielding. Consequently, there are a total of 4 power pins and 6 GND pins with the two outer pins assigned to GND. To magnify the parasitic inductance effect, only one power pin was used on the B-B connector to connect to the on-board PTL network. The measured loop inductance between one power pin and the other ground pins utilized was calculated as approximately 7.32 nH at 1GHz.

On the motherboard, there are two IC buffers for testing and verification. They were deactivated during measurement. The motherboard was solely used to provide power from the voltage source to the stacked daughter cards via PTLs and B-B connector. The voltage source was provided by an external bench power supply.

Each daughter card has several components that include two high speed I/O buffers, SMA connectors, a female B-B connector on the bottom layer and a male connector on the top layer. Figure 39 shows a schematic of the major components on the daughter card for one channel. Commercially available high speed differential buffers (P/N: NBSG16VS) were used. The differential buffers were chosen for their high speed (up to 12 Gbps) switching capability and Quad Flat No-leads (QFN) package with small parasitic inductance. The negative leg of the differential pair was treated as the path controlled by the Q2 transistor in Figure 26. For the ease of discussion, the North direction is marked on

the top right corner of Figure 38 and Figure 39. Although both the positive and negative outputs of the buffer are routed in the East direction from the IC to the board edge and terminated with SMA connectors, the outputs can be configured as either differential-output or single ended output. In the case of single-ended signaling, R_{STF} (Figure 38) was put in series between the positive output of the buffer and the corresponding output signal trace so the positive output of the buffer would reach the output SMA connector. For the negative output, R_{DNS} (Figure 38) was left unpopulated and R_d was a 50 Ω resistor to ground; therefore, the negative output is locally terminated, as shown in Figure 38. During all the measurements presented in this work the negative leg of the differential output for all buffers was terminated to ground through 50 Ω resistors. The positive output of the differential driver was routed in the East direction and terminated with the SMA connector. Hence, single ended signaling has been used in this chapter. For simplicity, R_{STF} and R_{DNS} are not shown in Figure 39. The buffer IC was powered using a 3.3 volt supply. There are two power pins on each of the ICs. One 0402 sized 0.1 uF decoupling capacitor was placed close to each of the power pins as recommended by the IC vendor. The placement of the decoupling capacitors ($C_{decouple}$) is shown in Figure 38. No other decoupling capacitors were used on the daughter card.

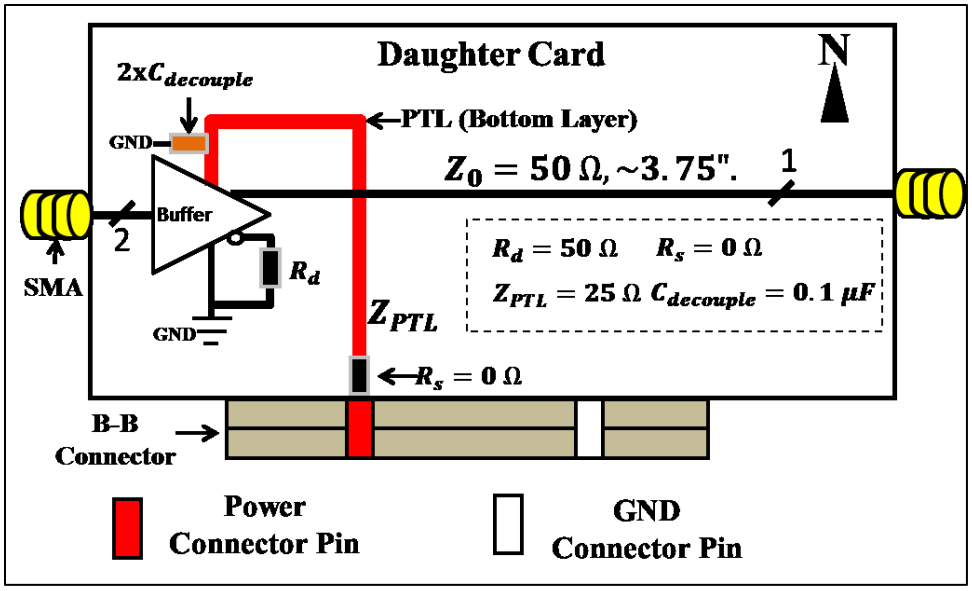


Figure 39 Single channel connection on a daughter card

Since all drivers were placed north of the B-B connector, the majority of PTLs was routed on the bottom layer from the connector up in the north-bound direction to feed each of the drivers, as shown in Figure 38. To avoid crosstalk between adjacent PTLs; transmission lines connected to GND were designed between adjacent PTLs. These GND transmission lines or GTLs have the same width as the PTLs. The spacing between the PTL and GTL ranges between twenty to thirty mils. Soldering pads for 0402 and 0603 size decoupling capacitors were placed on adjacent PTLs and GTLs in intervals for evaluating the effect of the capacitors on power supply noise. These soldering pads were left unpopulated during the measurement shown in this chapter.

Terminating resistor (R_s) was placed between one of the B-B connector power pins and the PTL as illustrated in Figure 38. To reduce power dissipation a 0 Ω resistor of 0805 size was used which is equivalent to setting the source terminating resistor, R_s, to 0 Ω in Figure 39.

3.2.3 Scalable Fanout Board Design

The signal generator used in the measurement was capable of generating one pair of differential signals. To drive multiple drivers simultaneously, we designed a two-stage scalable fanout board. The board used one pair of differential signals as input and generated multiple pairs of identical differential signals. We implemented the design with commercially available differential 1:4 fanout Low-voltage positive emitter-coupled logic (LVPECL) buffers (P/N: NB7L14). The fanout buffers were arranged in two buffering stages, as shown in Figure 40.

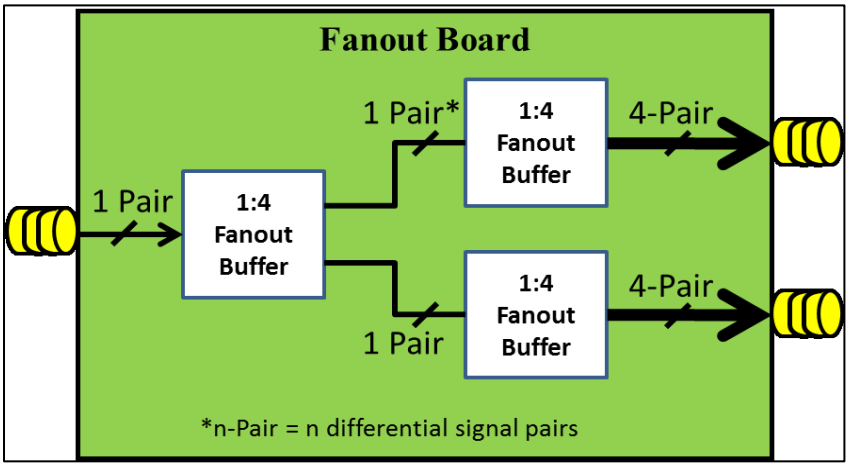


Figure 40 Fanout buffer ICs placement on the fanout board

The trace lengths of all output signals of the buffers were carefully matched. The routed trace lengths within a differential pair were matched within 1-mil. The tolerance among all pairs was within ±10-mil which corresponds to approximately ±2.44 ps of maximum difference in timing skew. To evaluate the performance of the fanout board, the jitter and eye diagrams were compared between outputs of the fanout board and the signal

generator. Figure 41 shows the measured peak-peak (P-P) jitter from six channels of the fanout board that produced the most consistent signal integrity with the P-P jitter measured from the signal generator. Each diamond-shaped data point represents a differential pair of the fanout board. The P-P jitter of the signal generator at 2 Gbps was 14.95 ps while the jitter measured from the fanout board ranges from 20.34 ps to 24.06 ps. The P-P jitters from all channels had a very small standard deviation of 1.70 ps with an average of 22.26 ps which is 7.31 ps higher than the P-P jitter measured directly from the signal generator. At a data rate of 3 Gbps, the fanout board had a standard deviation of 3.07 ps and an average P-P jitter of 29.67 ps which is about 7.39 ps higher than the P-P jitter (22.28 ps) measured directly out of the signal generator. The statistics suggest that the fanout board can replicate the signals from the signal generator with good precision and stable performance. Therefore, the output signals from the fanout board were used to excite the buffers on the test vehicle simultaneously. Figure 42 shows the measured eye diagrams from the signal generator and the fanout board at 2 Gbps. The amplitude of the eye height in Figure 42 was set to be compliant with the input voltage range of the buffers on the daughter cards.

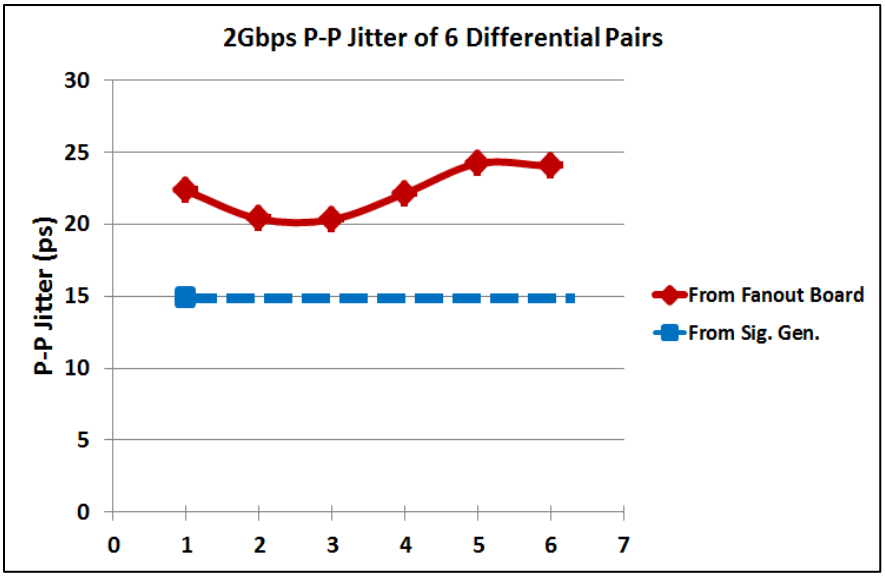


Figure 41 Comparison of measured P-P jitter at 2 Gbps data rate between signal generator output and outputs of six differential-pair channels from the fanout board.

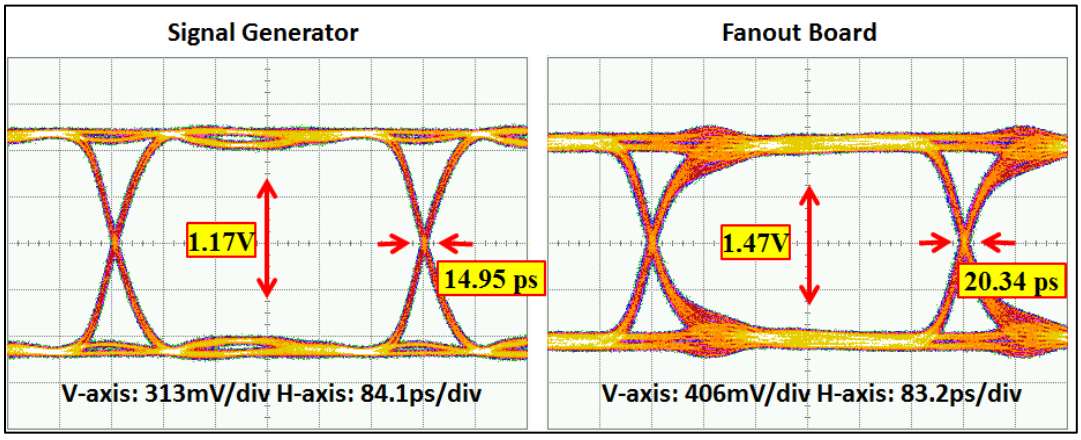


Figure 42 Comparison of measured eye diagrams at 2 Gbps: data from signal generator (left) and fanout board (right).

3.3 Test Setup

Since the data rates used were in the gigabit range, we used state of the art high performance and high speed equipment that had sufficient bandwidth to ensure that the

signal quality was not limited by the measuring equipment. The setup with the lab equipment and test vehicle is shown in Figure 43. An Agilent® 81133A wideband signal generator was used to provide a differential signal pair to drive the test vehicle. When multiple buffers on the test vehicle needed to be excited simultaneously, the fanout board was used to replicate the differential signal from the signal generator and transmitted to the test vehicle. The single ended output of the buffer under test was then connected to an Agilent® DCA-X 86100D oscilloscope through a 20 dB attenuator. The front-end receiving module of the oscilloscope was HP® 54752A which has a bandwidth of 50GHz.

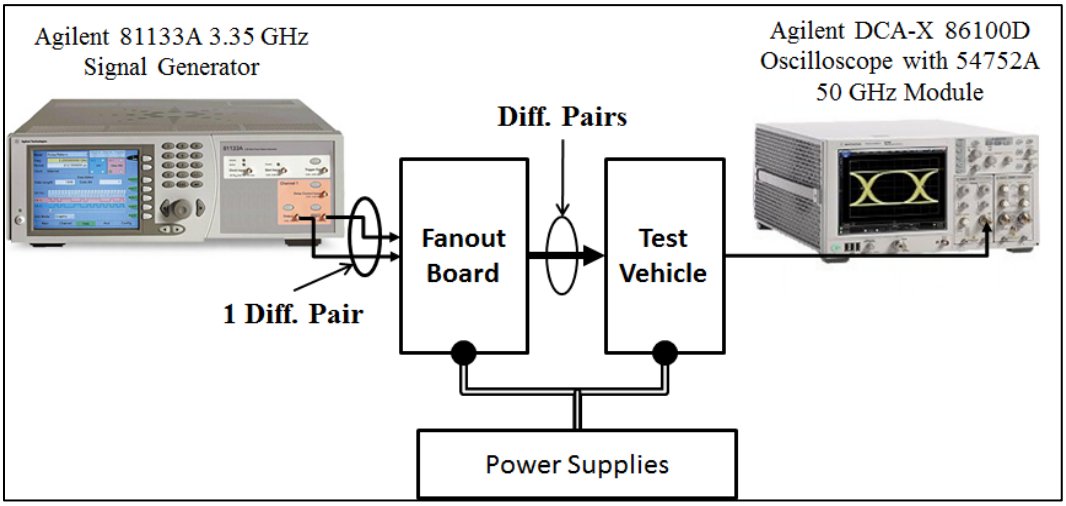


Figure 43 Block diagram showing test setup and lab equipment.

3.4 **Measurement Result**

In this section various metrics are used to demonstrate signal and power integrity for the CC-PTL signaling method.

3.4.1 Comparison between constant current signaling and unmodified differential signaling.

As is previously described, the differential drivers in the test vehicles can be configured as either single ended (or constant current) signaling or differential signaling by populating different sets of discrete components. The signal integrity performance between the unmodified differential and constant current signaling is compared in this section. The high speed differential driver used was NBSG16VS from On Semiconductor ® to implement the two schemes. In the single ended (or constant current signaling case), the negative output of the differential driver was terminated to ground through a 50Ω resistor. The driver was running at 0.5 Gbps, 1 Gbps, 2 Gbps and 3 Gbps. The output eye diagrams are shown in Figure 44 between CC and differential signaling.

Figure 47 a and b show the eye height and p-p jitter values for both signaling schemes are comparable. In fact, the eye height of the constant current signaling scheme generated more than 90% of that from differential signaling at all four data rates. Therefore, constant current signaling is a good alternative to differential signaling method to avoid routing congestion and fiber weave effect [26], [70].

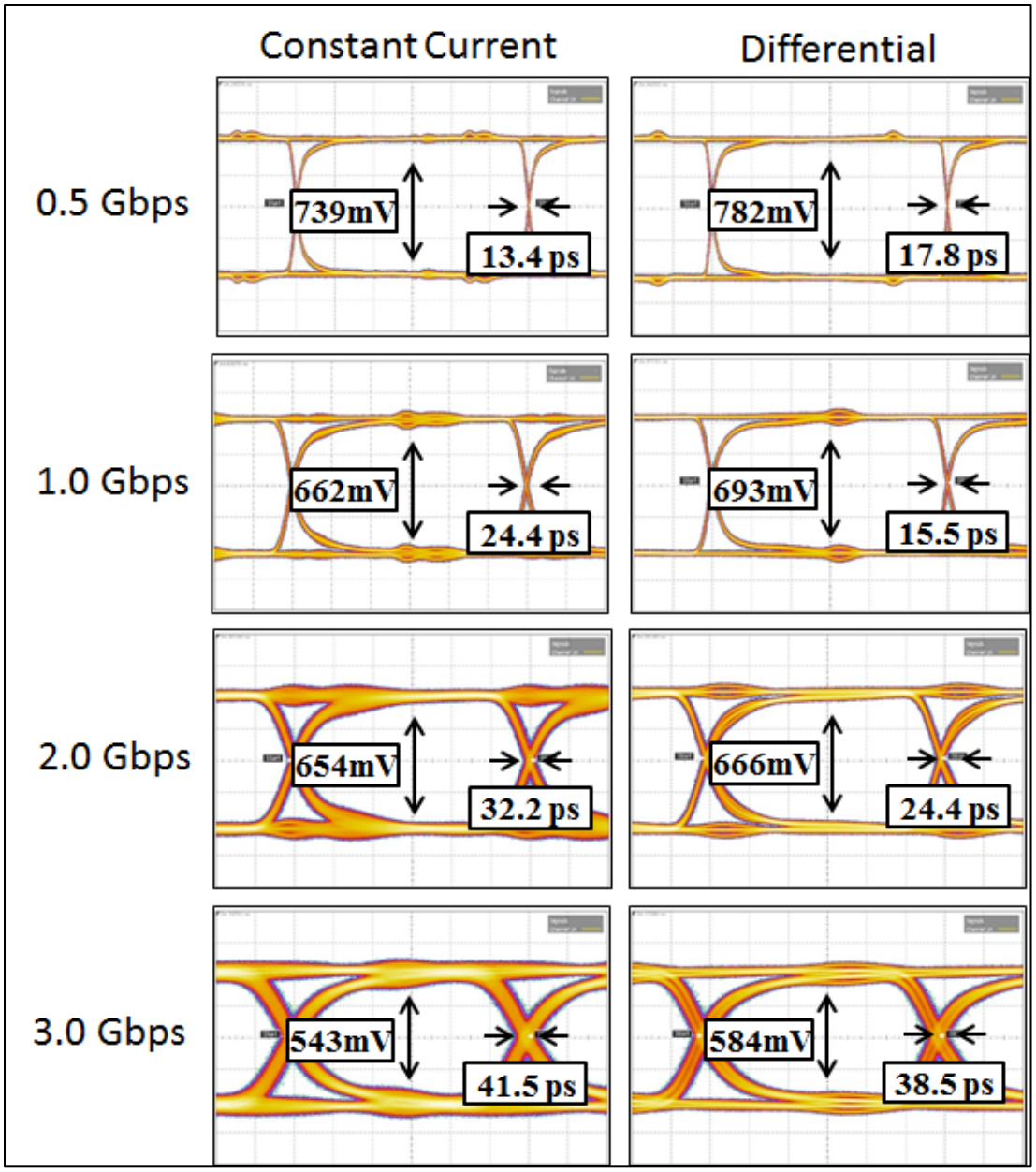
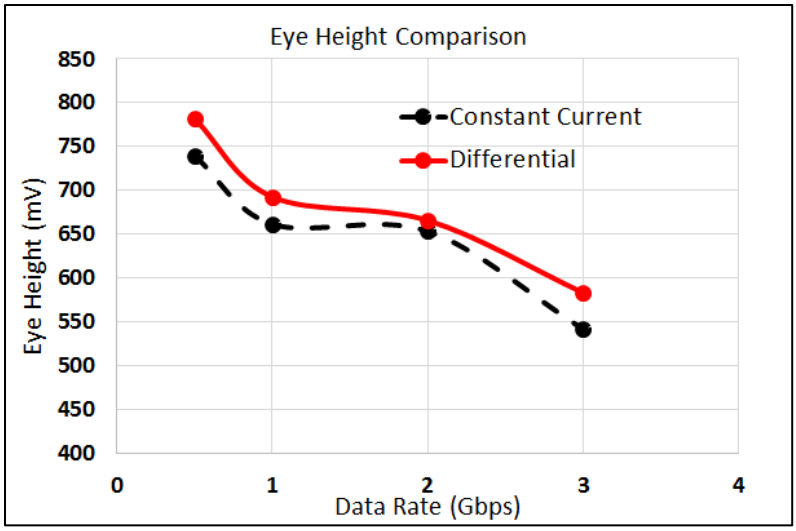
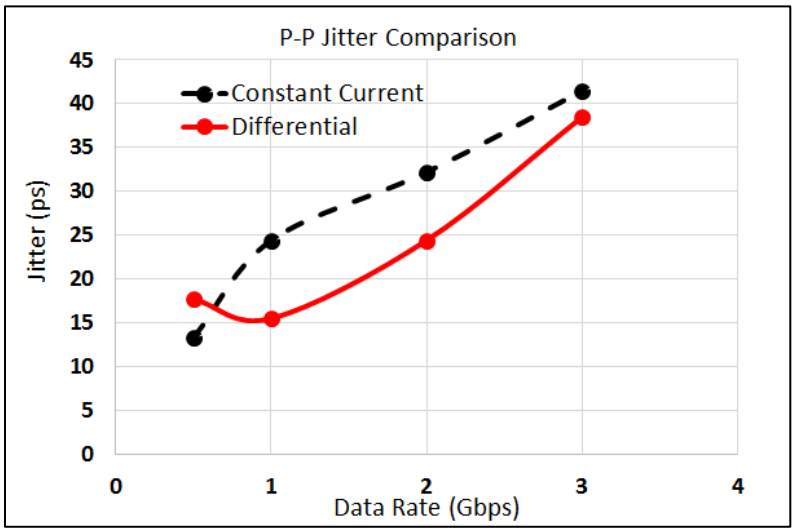


Figure 44 Eye diagram comparison between constant current signaling and differential signaling



(a)



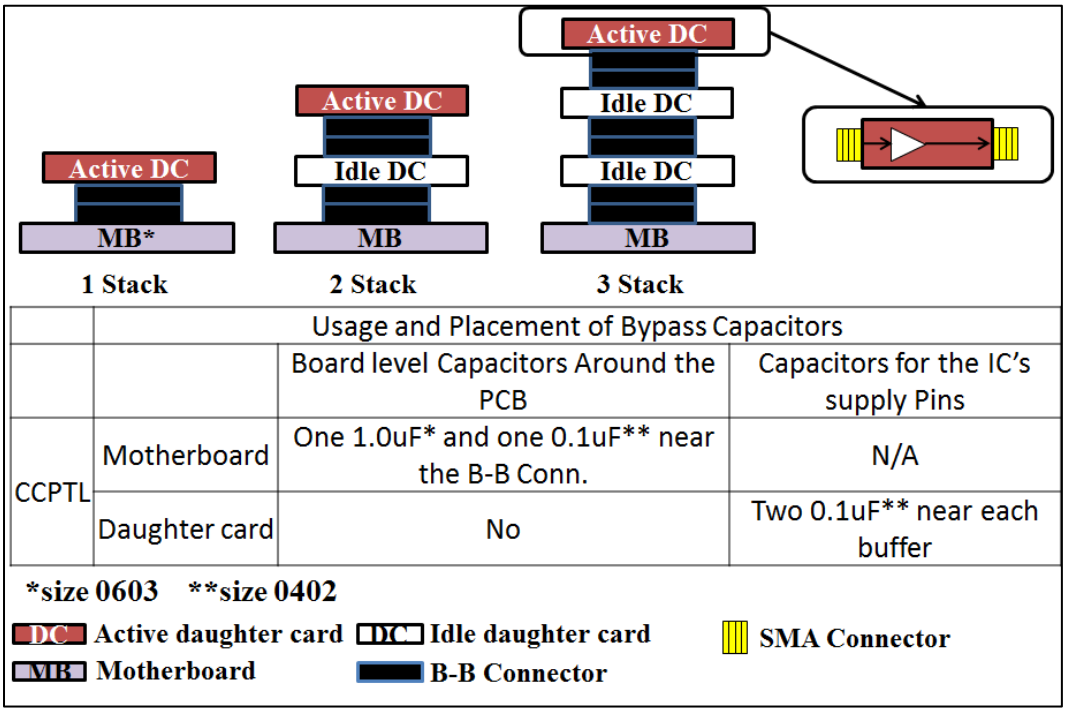
(b)

Figure 45 Statistical comparison in a) eye height and b) p-p jitter between constant current signaling and differential signaling schemes at 4 different bit rates.

3.4.2 Signal Integrity

The focus here is to increase the inductance along the power supply path and capture its effect on signal integrity. As is well known, as the inductance increases the

signal integrity can degrade [6]. The B-B connector has been used to increase the inductance by stacking the daughter cards on each other. We begin by connecting a single daughter card to the motherboard. Then an I/O buffer on the daughter card was driven directly by the signal generator with PRBS at 1, 2 and 3 Gbps. The eye diagram of the signal output was measured on the daughter card. We then elevated the position of this daughter card by inserting another daughter card above the motherboard. This added additional parasitic inductance on the interconnect between the active daughter card and the motherboard. We repeated the process with one and two inserted daughter cards and took measurements on the top active daughter card, as shown in Figure 46.



	Usage and Placement of Bypass Capacitors		
		Board level Capacitors Around the PCB	Capacitors for the IC's supply Pins
CCPTL	Motherboard	One 1.0uF* and one 0.1uF** near the B-B Conn.	N/A
	Daughter card	No	Two 0.1uF** near each buffer

***size 0603 **size 0402**

DC Active daughter card **IDC Idle daughter card** **SMA Connector**

MB Motherboard **B-B Connector**

Figure 46 Test vehicle setup: Signal Integrity (SI) vs Parasitic Inductance Evaluation.

If only the inductance of the B-B connector was included in the power supply path, a measured value of about 7.32 nH of inductance was added with the insertion of each daughter card given the dimensions and physical spacing of the power and ground pins of the B-B connector and the pin-assignment. This inductance was increased by the PTL inductance and the inductance of the traces from the power supply source on the motherboard. As indicated in Figure 46, there were only two bypass capacitors (one 0402 sized 0.1 uF and one 0603 sized 1.0 uF) that were placed on the motherboard near the B-B connector to provide the charge to the switching circuits. In addition, there were two 0402 sized 0.1 uF decoupling capacitors ($C_{decouple}$) placed near the two power supply pins of each buffer on the daughter card, as shown in Figure 38 and Figure 39.

Figure 47 shows the eye diagrams measured on the active daughter card for the cases when there were one, two and three daughter cards stacked on the motherboard (MB) for data rates of 1, 2 and 3 Gbps. Table 6 summarizes the measured eye height and P-P jitter at the output of the active buffer. At the lowest data rate of 1 Gbps PRBS, the average eye height was about 602 mV with a standard deviation of 7.2 mV. The average P-P jitter was 17.37 ps with a 2.14 ps deviation. At the highest date rate of 3 Gbps rate, the average eye height was 447 mV with a standard deviation of approximately 4.2 mV. The average P-P jitter was 46.67 ps with a 1.84 ps standard deviation. From the measured parameters, we observe that the signal quality remains relatively stable as measured by the eye height and jitter even when the inductance was increased three fold for each data speed.

3.4.3 Simultaneous Switching Noise (SSN) and Signal Integrity

In this section we switched multiple drivers and captured the effect on power supply noise and signal integrity. Since there were two high speed buffers on each daughter card

and the test vehicle consisted of three stacked daughter cards, there were a total of six buffers that could be switched simultaneously.

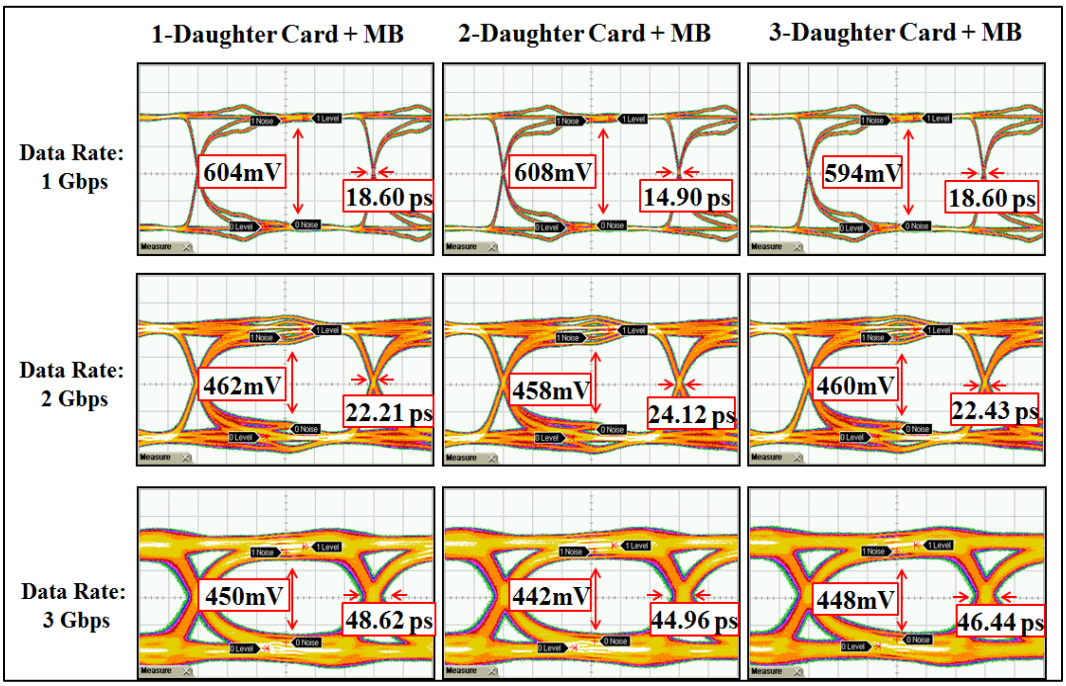


Figure 47 Eye diagrams comparison between 1, 2 and 3 Gbps data rate across the stack for CC-PTL based test vehicle.

As a first step we simulated the power supply noise in the frequency domain for the two cases in which three daughter cards were stacked together with two active I/O buffers on each daughter card and all of the buffers were either simultaneously or non-simultaneously switched. The IBIS model of the buffers was obtained from the vendor. The S-parameters of the transmission lines in the daughter card were modeled using Sphinx®, an electromagnetic simulation software package [73]. The IBIS model and S-parameters were then imported into Advanced Design System® [77] from which the power supply noise was simulated. For the non-simultaneous simulation case, we introduced

additional random delays to each of the PRBS data pattern generators that were used to drive the buffers as follows: 1.71, 2.46, 3.45, 3.64, 4.57 and 4.85 ns of delay. The simulated SSN and non-simultaneous switching noise (NSSN) when an input clock signal of 3 GHz was used are shown in Figure 48a and Figure 48b respectively. The noise level measured for the first three harmonics are labelled in both plots. It can be seen that when the six drivers were driven simultaneously, the power supply noise is approximately 10 dBm and 12 dBm higher than the non-simultaneous switching case at the first two odd harmonics. The peak to peak noise level in time domain for the simultaneous switching case was 214 mV which is 41 mV higher than the NSSN when 45000 clock cycles were run. The peak to peak noise was calculated by taking the difference between the maximum noise and the minimum noise points in the time domain. Figure 49a and Figure 49b show a segment of the measured AC-coupled noise from 300 to 305 nsec for SSN and NSSN respectively in the time domain.

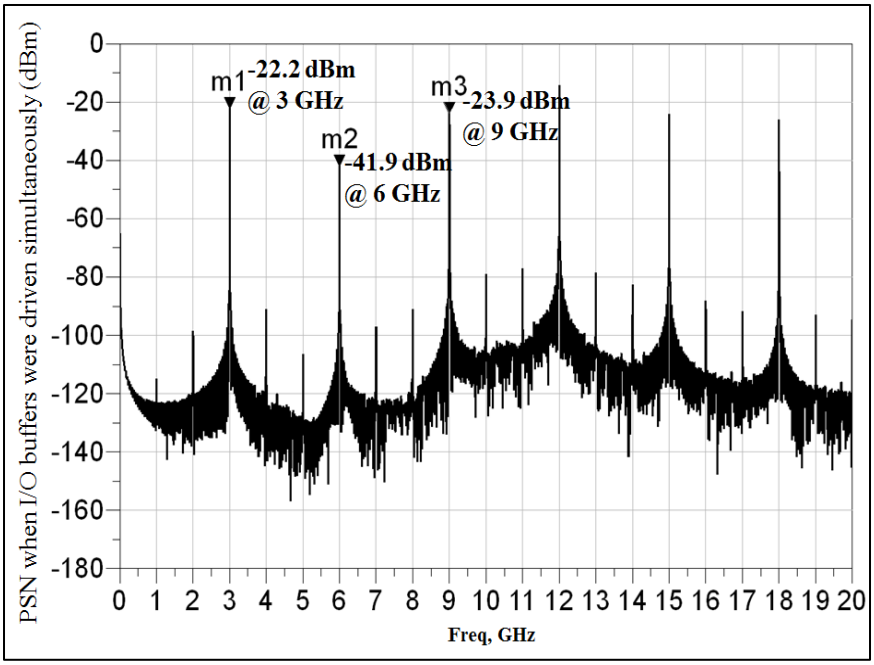
To measure the power supply noise, a clock signal was fed to the fanout board which was then used to drive a total of six I/O buffers simultaneously, two on each daughter card. To maximize SSN, we used the same length of SMA coaxial cables between the fanout board and daughter cards. To construct the scenario where all I/O buffers are driven at the same time but by different data bit streams, we introduced various delays between the fanout board and the daughter cards by using coaxial cables of different lengths. We define this scenario as asynchronous or non-simultaneous driving case. In this chapter, the words asynchronous and non-simultaneous are used interchangeably. The words synchronous and simultaneous are also used interchangeably. The length of the cable in the synchronous case was 7 inches. The cable lengths for the asynchronous case were 7,

12, 13, 15, 18.5 and 20 inches which corresponded to propagation delays of 1.71, 2.46, 3.45, 3.64, 4.57 and 4.85 ns respectively as measured using TDR. These propagation delays introduced additional skews for the asynchronous switching case.

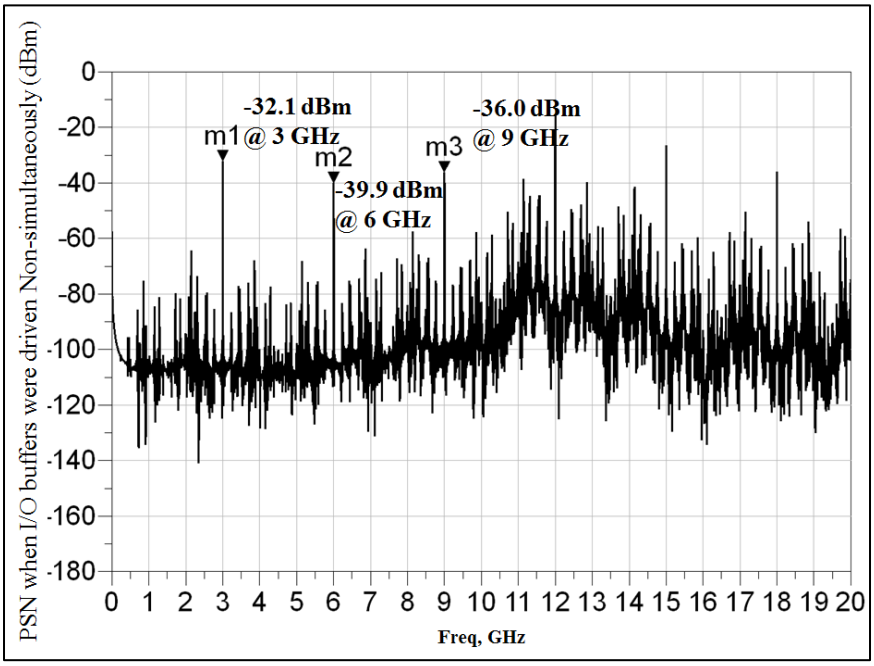
Table 6 Measured Eye Height and P-P Jitter When Inductance was Increased

	Eye Height (mV)			Avg. (mV)	STDEV. (mV)
Data Rate	1*	2*	3*		
1 Gbps	604	608	594	602	7.2
2 Gbps	462	458	460	460	2.0
3 Gbps	450	442	448	447	4.2
	P-P Jitter (ps)			Avg. (ps)	STDEV. (ps)
Data Rate	1*	2*	3*		
1 Gbps	18.60	14.90	18.60	17.37	2.14
2 Gbps	22.21	24.12	22.43	22.92	1.05
3 Gbps	48.62	44.96	46.44	46.67	1.84

*Number of stacked daughter cards (DC) on the MB as shown in Figure 46.

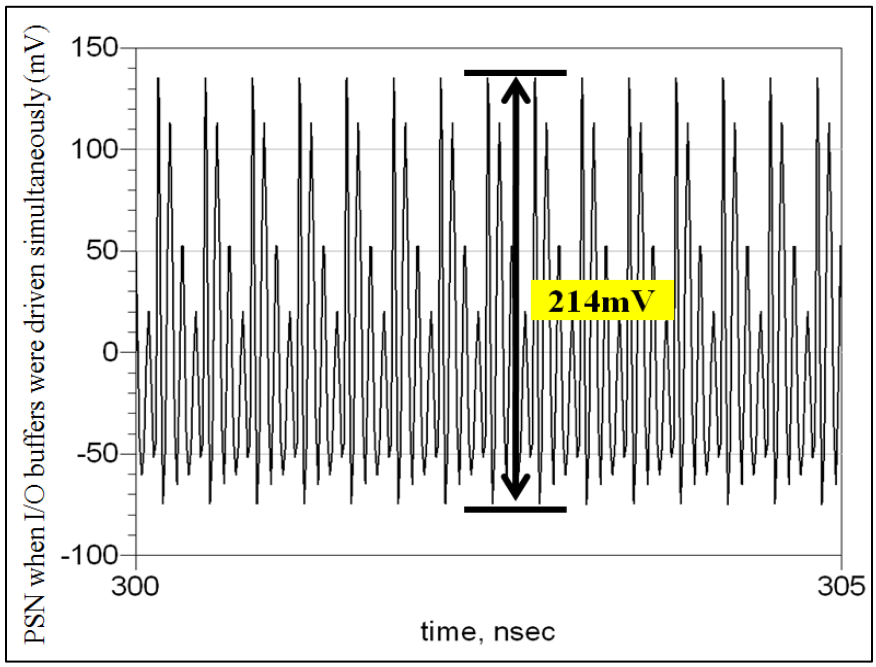


(a)

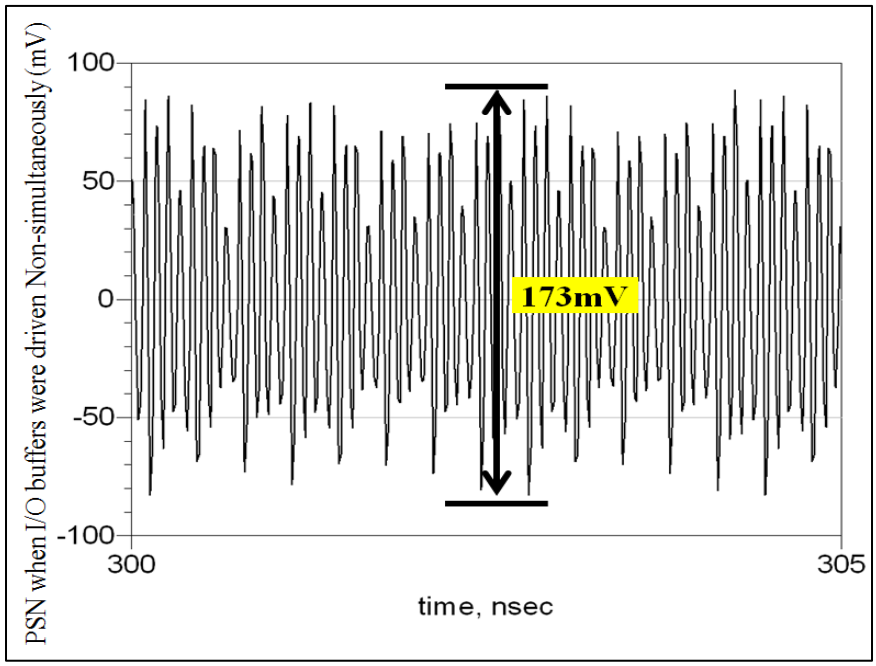


(b)

Figure 48 Simulated power supply noise frequency spectrum when six buffers are driven (a) simultaneously and (b) non-simultaneously at 3GHz.



(a)



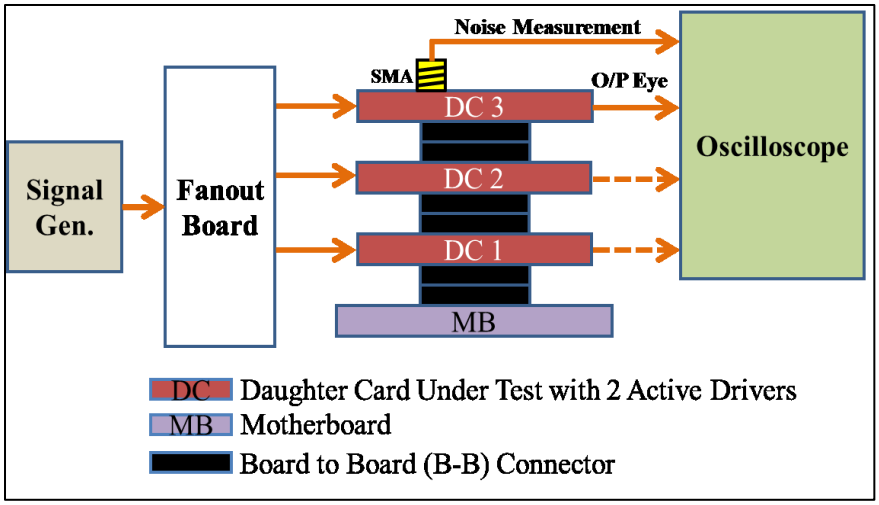
(b)

Figure 49 Simulated power supply noise in time domain when six buffers are driven (a) simultaneously and (b) non-simultaneously at 3GHz.

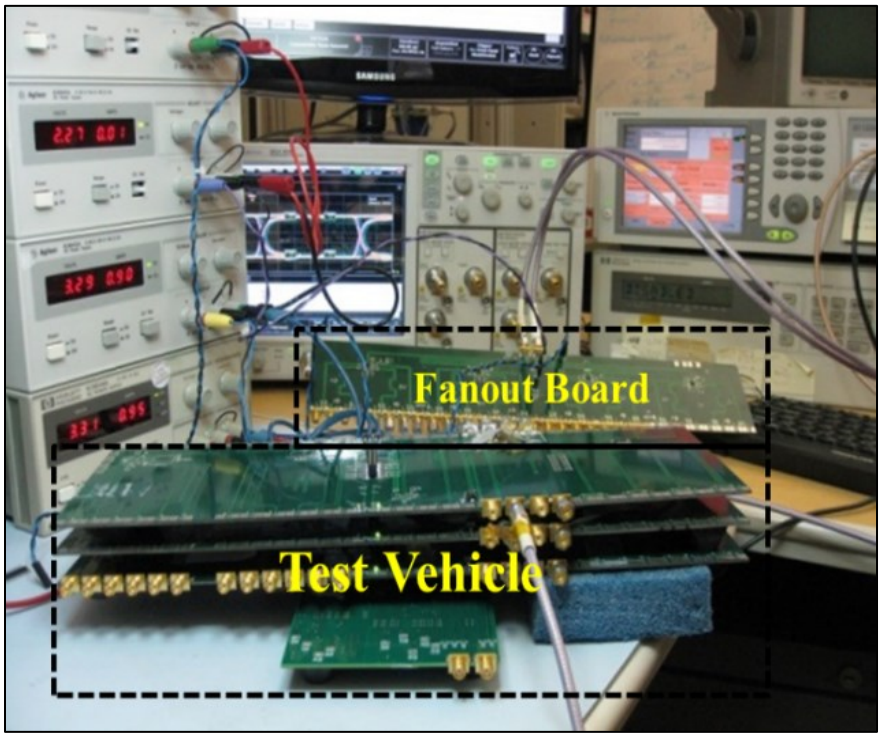
The noise measurement fixture on the test vehicle was done by soldering a vertical SMA connector to a power-ground via pattern closest to the load which was less than 9 mm away on the top most daughter card of the test vehicle, as shown in Figure 50a. A high quality SMA coaxial cable was used to connect the SMA connector to the oscilloscope through a DC blocking capacitor with a wide bandwidth of 0.045 Hz - 26.5 GHz. Figure 50b shows the lab setup with the test vehicle at the lower center of the figure. The test vehicle was connected to a power supply, oscilloscope and output ports of the fanout board. The differential input ports of the fanout board were then connected to the signal generator.

The measured power supply noise when the drivers were driven synchronously and asynchronously using a 3 GHz clock signal were -22.52 dBm and -28.33 dBm respectively at the fundamental frequency, a 5.81 dB difference, as shown in Figure 51. The measured results correlate well with the simulation.

Table **7** shows the noise comparison for the fundamental and next two harmonics when the buffers were driven synchronously and asynchronously at 3GHz. The first and second harmonics were higher by 5.81 dB and 15.65 dB respectively in the synchronous case. Although the third harmonic is slightly higher by 2.19 dB for the asynchronous case, it would not change the overall noise dominance of SSN over NSSN. The measured peak-peak SSN and NSSN in time domain were 70.7 mV and 45.9 mV, respectively, as shown in Figure 52. The 54% increase in noise level for the synchronous case is expected since the current transients are the highest when buffers are switched simultaneously.



(a)



(b)

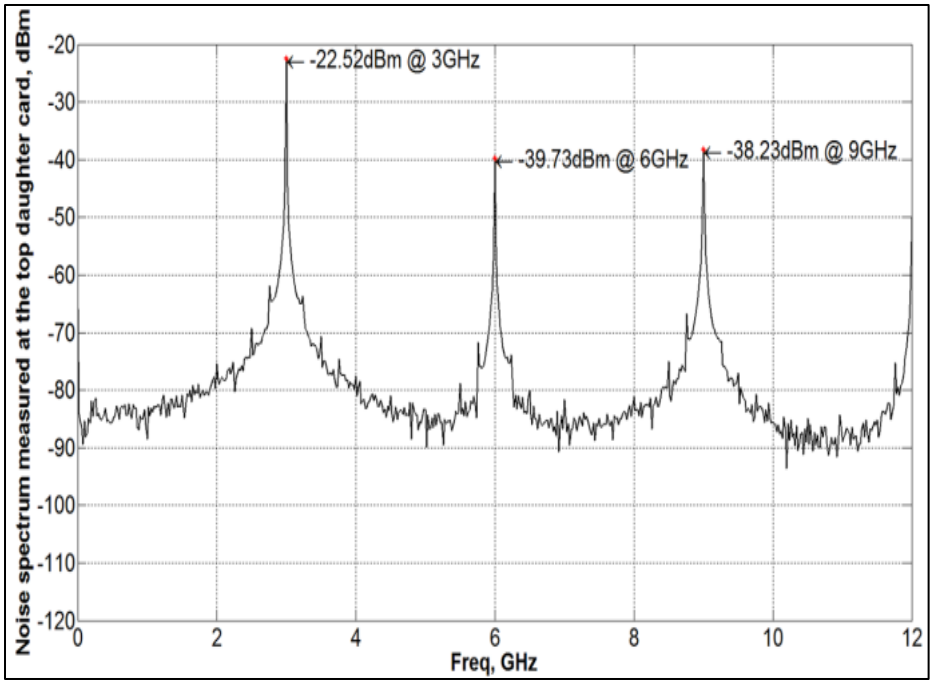
Figure 50 (a) Measurement setup for synchronous and asynchronous switching (b) photograph of the test bench setup for the synchronous switching case.

Table 7 Noise Level Comparison For The First Three Harmonics When Six Buffers were Driven Synchronously and Asynchronously with 3 GHz Clock Signal

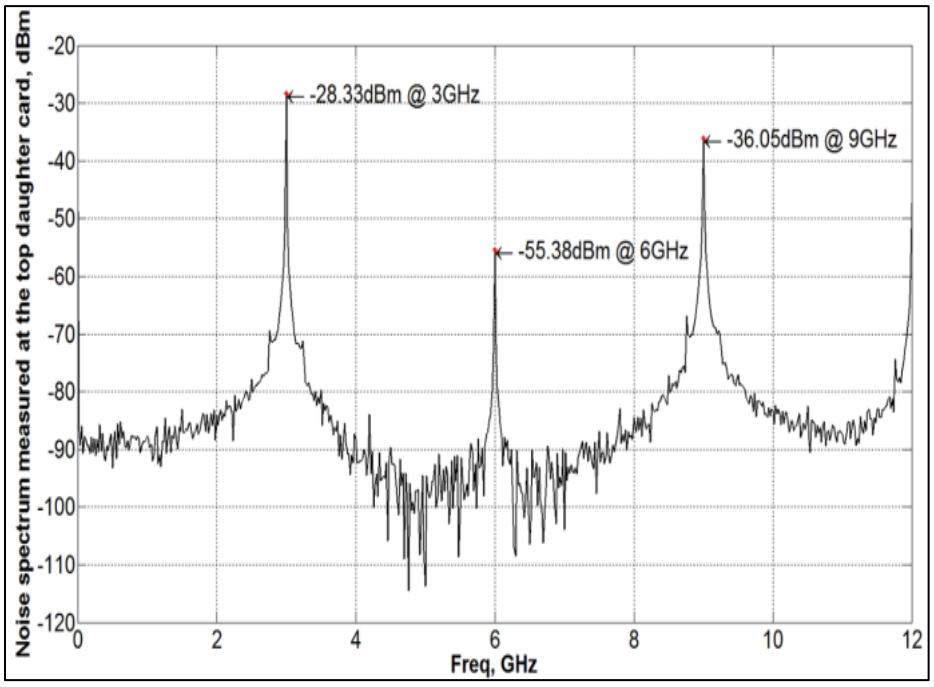
Measured Noise Level:	3 GHz	6 GHz	9 GHz
Synchronous (dBm)	-22.52	-39.73	-38.23
Asynchronous (dBm)	-28.33	-55.38	-36.05
Difference (dB)	-5.81	-15.65	2.18

Six buffers were driven simultaneously next using a 3 Gbps PRBS. The measurement setup is shown in Figure 50a. While measuring one output with the oscilloscope, the outputs of the other active drivers were terminated with 50 Ω resistive load.

Figure 53 shows the measured eye diagrams on each daughter card along with eye height and P-P jitter information. The P-P jitter increased from 83.16 ps to 91.67 ps from daughter card 1 to 3 in the PTL design. The eye height decreased from 463 mV to 414 mV as the position of the daughter card was elevated in the stack. Both P-P jitter and eye height exhibited small standard deviation of 4.4 ps and 25 mV, respectively from the lowest to the highest daughter card despite the large parasitic inductance within the power and ground connections. As for the plane based design, the eye height was in the range of 200 mV while the p-p jitter was in the range of 200 ps across the stack. The improvement in eye height and p-p jitter are both evident, as shown in Table 8.

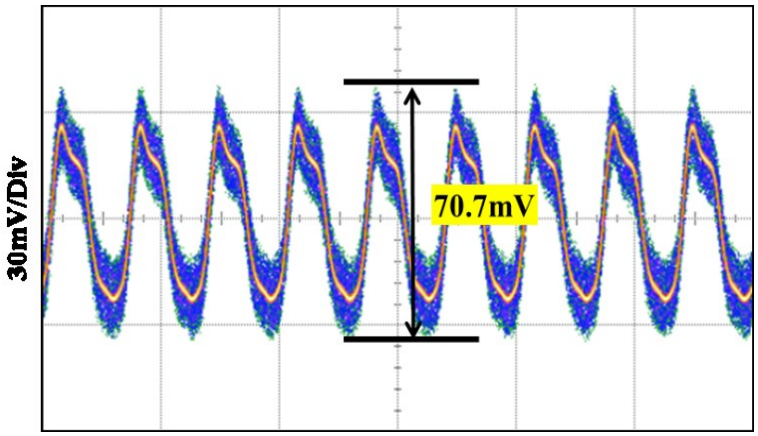


(a)

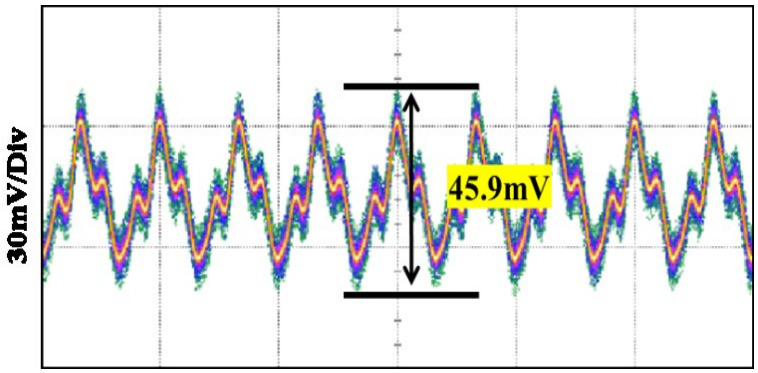


(b)

Figure 51 Measured power supply noise spectrum for (a) synchronous and (b) asynchronous switching.



(a)



(b)

Figure 52 Measured power supply noise in time domain when six buffers were driven a) synchronously and b) asynchronously by a 3 GHz clock signal.

Table 8 Measured Eye Height And P-P Jitter On Each Daughter Card At 3 Gbps Prbs When 6 Buffers Were Switched Simultaneously.

D.C. #	Eye Height (mV)			P-P Jitter (ps)		
	Plane	CC-PTL	Improvement*	Plane	CC-PTL	Improvement*
3	203	414	103.9%	196	91.7	53.3%
2	258	429	66.3%	184	85.4	53.7%
1	251	463	84.5%	210	83.2	60.5%

*The improvement is CC-PTL over plane design.

3.4.4 Card to Card Communication

In this test setup, we mimic board to board high speed communication by connecting daughter cards in a daisy chain using 20-inch long coaxial cables, as shown in Figure 54. The length of the cables may introduce minor amplitude reduction but enable smooth connection between the cards without any bending or problems with structural integrity. All daughter cards and the motherboard share a common power distribution network.

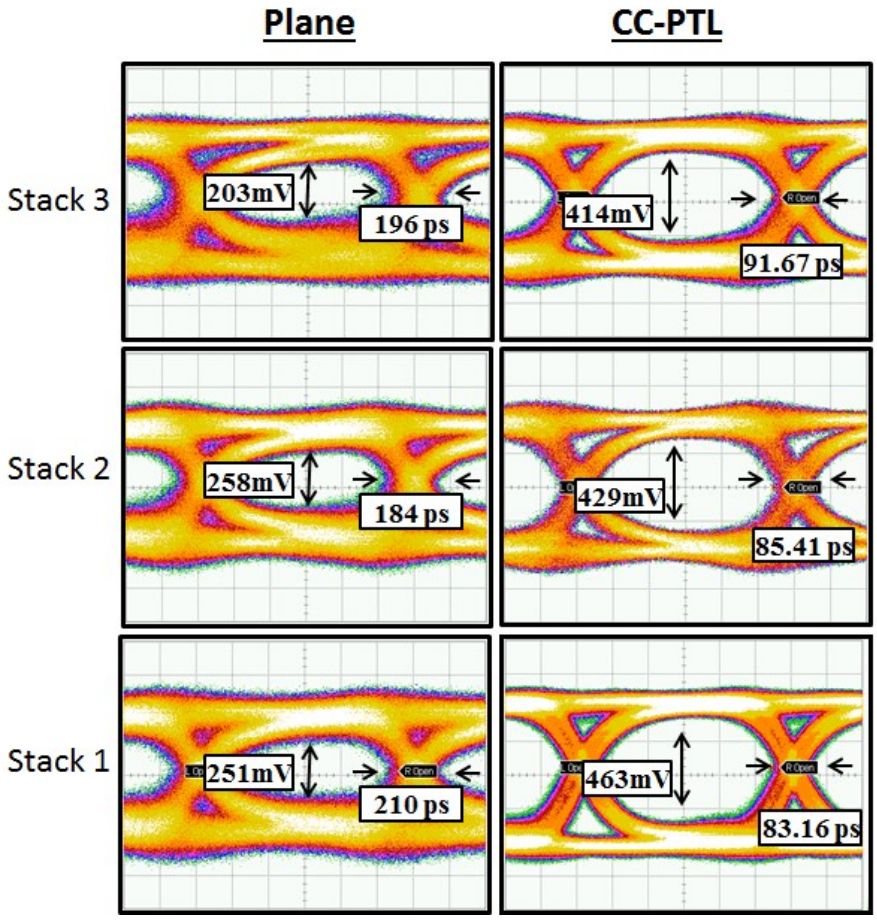


Figure 53 Signal integrity on each daughter card at 3 Gbps PRBS for six simultaneously switching buffers.

Figure 55 shows the measured eye diagrams on the top most daughter card when running the data at 1, 2 and 3 Gbps PRBS for both CC-PTL and CC-plane systems. At 1 Gbps, the signal integrity was very good with a measured eye height of 607 mV and P-P jitter of 48.2 ps for the CC-PTL case. Although the signal integrity degrades at 3 Gbps, the eye still remains open with an eye height of 432 mV and 143 ps of P-P jitter whereas in the plane based design, the eye is closing. Table 9 shows the measured data comparing the measured eye height and p-p jitter when the buffers were driven with 1, 2 and 3 Gbps PRBS data. It shows again that PTL-based design showed significant improvement of over 50% in signal integrity as compared with plane based design.

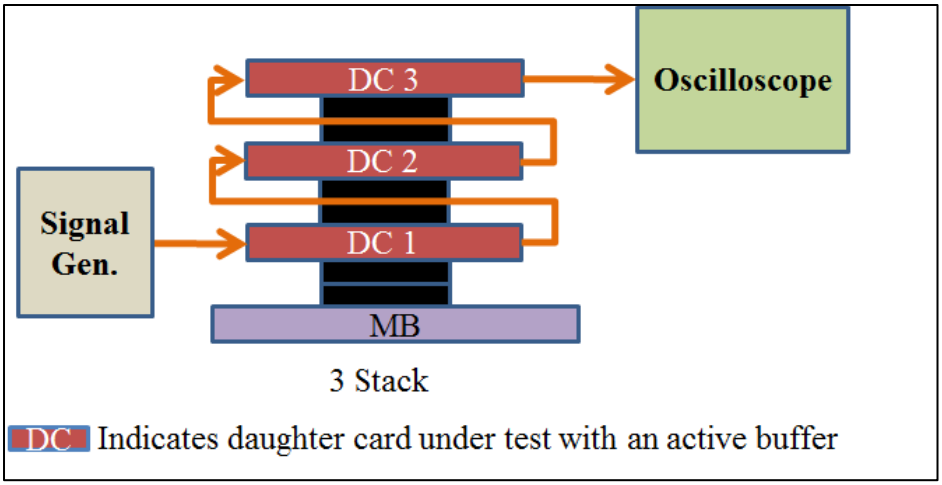


Figure 54 Daughter card to daughter card communication measurement setup.

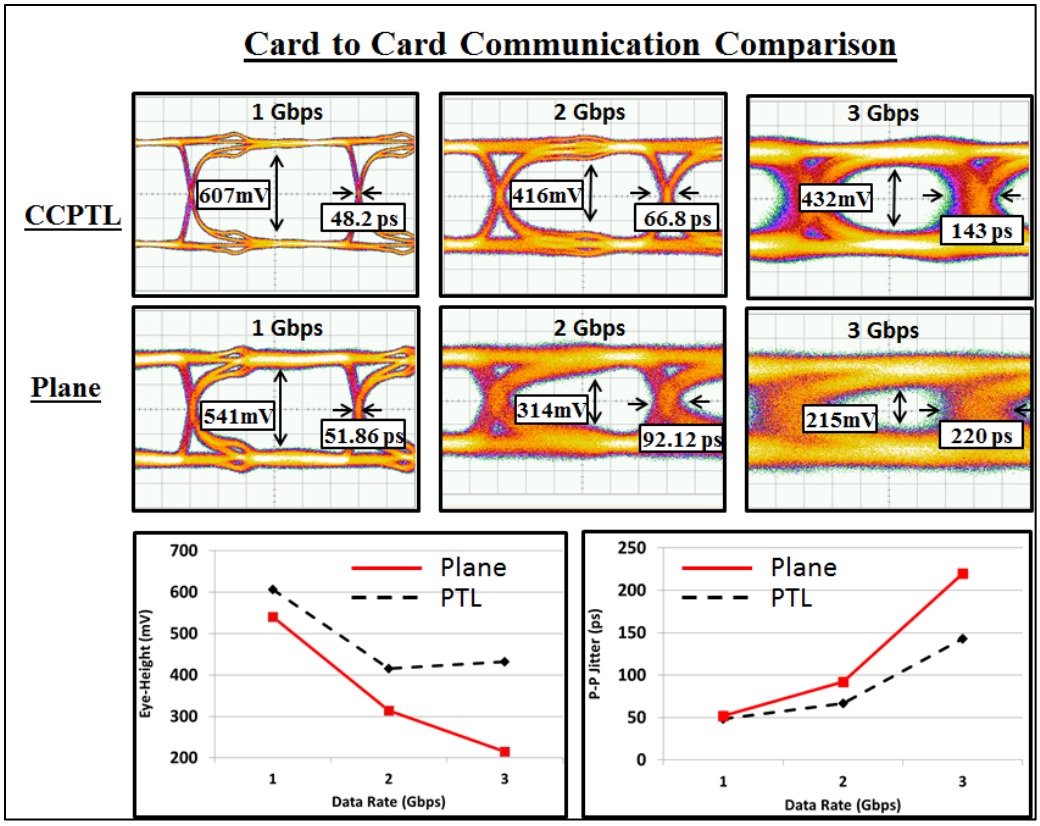


Figure 55 Signal Integrity comparison for card to card communication for data rate of 1, 2 and 3 Gbps PRBS when measured at the output of the 3rd stacked daughter card.

Table 9 Measured Eye Height and P-P Jitter At the Third Daughter Card At 1, 2 And 3 Gbps PRBS When Daughter Buffers Were Daisy Chained Together

Gbps	Eye Height (mV)			P-P Jitter (ps)		
	Plane	CC-PTL	Improvement*	Plane	CC-PTL	Improvement*
1	541	607	12.2%	51.9	48.2	7.1%
2	314	416	32.5%	92.1	66.8	27.5%
3	215	432	100.9%	220	143	35.0%

3.5 Routing of PTLs for a Large Number of Drivers

A ~12 inch long PTL was demonstrated to support 6 drivers each drawing about 25 mA of current in section 3.4.2. In modern high computing systems, hundreds of I/O drivers can exist. The number of drivers a PTL can sustain depends on the current carrying ability of the PTL and the sum of the maximum current transient of the buffers. The current capacity of a conductor such as a PTL can be calculated according to empirical formula (3) and (4) given by [64].

$$\text{Area}[\text{mils}^2] = \text{Width}[\text{mils}] * \left(\text{Thickness}[\text{oz}] * 1.378 \left[\frac{\text{mils}}{\text{oz}}\right]\right) \qquad (4)$$

$$\text{Current [Amps]} = \text{Area [mils}^2] * \left(\text{k} * (\text{Temp\_Rise}[\text{deg. C}])^{\text{b}}\right)^{\frac{1}{\text{c}}} \qquad (5)$$

where, b=0.44, c=0.725, k=0.024 for internal layers, and k=0.048 for external layers such as a microstrip line structure. Temp_Rise is the rise of temperature within the conductor relative to ambient temperature, which is assumed to be 25 degree Celsius. For a PTL trace of 50 mils wide, which was used in the test vehicles used in this chapter, with a temperature rise equal to 10 degree Celsius the current capacity of the microstrip line based PTL is approximately 4.23 A. Assuming the maximum current transient on the PTL contributed by each driver is ~25 mA, the total number of drivers can be supported by the 50-mil PTL is about 160 according to equation (6). If the trace width is only 10-mil wide, which is comparable with the width of most signal traces in modern high density PCB designs, the current capacity is ~0.85 A and can support up to 34 drivers.

$$\text{Num. of drivers to be supported} = \frac{\text{Current [Amps]}}{\text{Max. Current Per Driver [Amps]}} \qquad (6)$$

In [46], the author suggested routing PTL as grids to connect to the loads. However, such route planning would render the routing of high speed signal on adjacent layers

impossible as the grids would introduce significant return path discontinuities. The argument is similar to the reason as to why band-gap structures are highly discouraged to be used in high speed digital designs [78] and [79]. In addition, the routing and placement of components and vias are highly irregular making routing PTLs in regular grids practically difficult and time consuming. In this work, we recommend the method of "fly-by" routing topology that is commonly used in Double Data Rate (DDR) 3 and DDR 4 Synchronous Dynamic Random-access memory (SDRAM) routing as a more practical and proven routing alternative [80]. This topology is illustrated in Figure 56. The main PTLs can reside in either internal or external dedicated PTL-routing layers or on signal layers. They fan out from the power entry point and reach the vicinity of the loads. The PTLs then transition to the component layers through vias to make the connection to the power pins of loads. To reduce reflection the part of the PTL that is on the mounting side of the PCB should be kept at a minimum length, length "B", as shown in Figure 56. In the case there is a mismatch between the width of the PTL on the component side and that of the component power pins, the PTL should be tapered gradually to minimize abrupt impedance discontinuity. In addition, as the PTL transitions from the main PTL layer to the external layers, ground vias can be planted around the PTL via to maintain impedance continuity. The ground via spacing and distance from a center via can be determined through 3D electromagnetic solver. The "fly-by" routing strategy was used for the PTLs in all of the PTL based test vehicles throughout this research work. As shown in Figure 53, good signal quality was achievable by using this routing topology. Another advantage of using the "fly-by" topology is that it is highly scalable and can accommodate many loads, as shown in Figure 56.

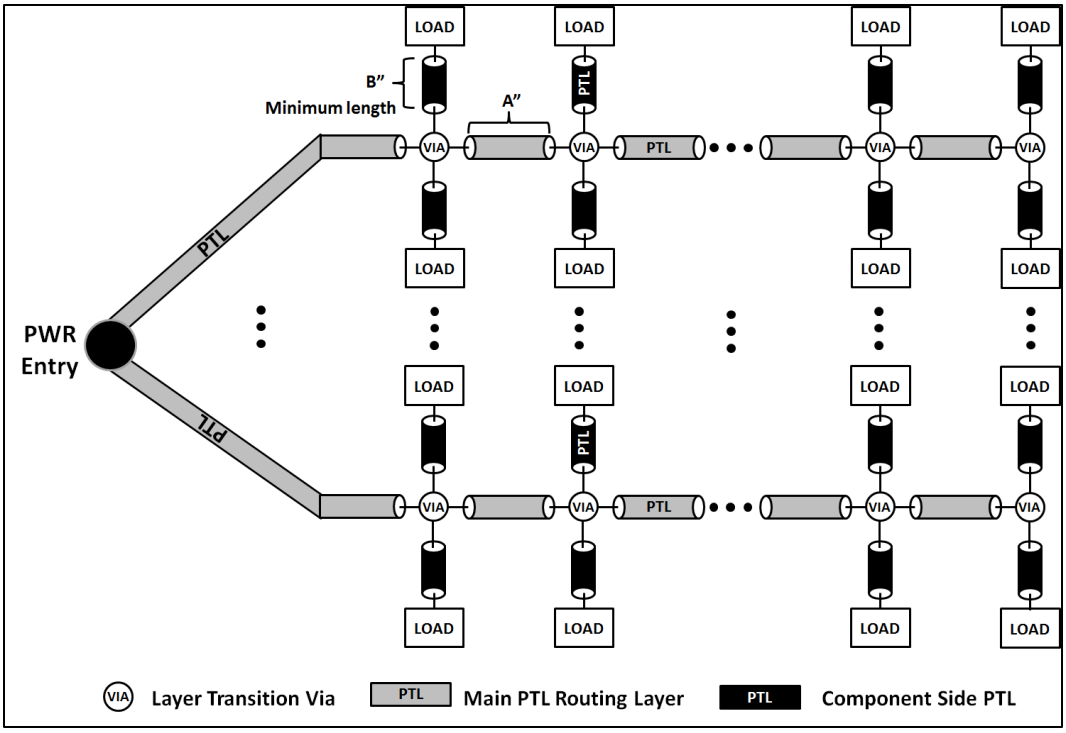


Figure 56 System level PTL routing for a large number of loads

Other than the current carrying capacity of the PTL, the DC drop, characteristic impedance, anti-resonance peaks of the PTLs can also affect the determination of the physical dimension of the PTLs. These factors, which will be discussed further in Chapter 5, take a rather more predominant role in designing the physical length, width and thickness of the PTL since the current capacity of a copper trace is rather generous as compared to the current consumption of many state of the art buffers. For example, a 50 mil wide copper trace can support 160 drivers assuming each consumes 25 mA. If the PTL is found to be too narrow to support the planned number of loads, the number should be reduced so that it will not affect the aforementioned factors; characteristic impedance and anti-resonance peaks location.

As a PTL is loaded with more drivers, its width will increase leading to a reasonable DC drop. The potential impact on energy reflection due to impedance match between the PTL and the connected power pins from the components can be minimized through the use of constant current signaling as described in Chapter 2.

3.6 Summary and Conclusion

In this chapter, we applied Power Transmission Line (PTL) based power distribution method combined with constant current signaling scheme to a complex test vehicle that consisted of four stacked PCBs (one motherboard and three daughter cards) using board-board connector. The use of power transmission lines minimized effects of cavity resonance as a result of the elimination of large cavities formed between voltage and ground reference planes that arise in a conventional voltage plane based power distribution network. By eliminating voltage planes, power transmission lines also reduced return path discontinuities which can cause unwanted electromagnetic coupling between circuits, signal integrity degradation, and higher power supply noise [50]. Furthermore, isolation between signal lines and power distribution network can be achieved in PTL-based design as a result of the routing flexibility of PTLs. The PTLs can be either routed away from the signal lines on the same layer with ground traces/vias in between to avoid coupling between them, or perpendicularly on another layer with the reference plane between the signal layer and the PTL layer. In the next chapter, we will demonstrate the measured isolation in the PTL-based PCB design and compare it with the voltage plane based designs quantifiably.

The constant current signaling scheme was achieved by adding a complementary resistive path to the signal path from PTL to ground reference. The complementary operation by the signal and the resistive path resembles that of a differential driver.

Therefore, the current transient on the power transmission line was maintained at a minimal level. Since only one output was transmitted, single-ended high speed signaling was achieved.

The signal integrity was measured through three test setups namely by i) varying parasitic inductance of the power and ground connections, ii) switching six buffers synchronously and asynchronously at gigabits per second rate, and iii) daisy chaining three daughter cards for board to board communication. In the first test case, the PTL based design showed less than 10 mV of standard deviation from stack to stack in eye height and less than 2 ps deviation in p-p jitter. In the second test case where 6 drivers were switched simultaneous, the CC-PTL design showed over 66% improvement in eye height and ~50% less p-p jitter when compared with the plane case across all three stacked daughter cards. Finally, when the buffers on the three daughter cards were daisy chained together, card to card communication was realized in test case 3. Once again, the PTL showed significant improvement in eye measurement when the buffers were driven at 1, 2 and 3 Gbps. The improvement was most significant at 3 Gpbs when the measured eye height and p-p jitter were 432 mV and 143 ps, which are 100.9% and 35% better than the eye height and jitter, respectively, in the plane based design.

The measured data in all three scenarios showed that the PTL-based design offers good and consistent signal quality in spite of the large parasitic inductance in the PDN. This finding suggests the possibility of reduced number of layers in the stack-up with fewer decoupling capacitors.

The test vehicle implemented in this work also resembles a 3D system, which consists of IC dies and an interposer stacked on a PCB, in terms of increased parasitic

inductance along the stack and a complex power distribution network. The CC-PTL scheme can therefore be applied to IC level 3D systems. Initial simulation has shown signal and power integrity advantages for 3D integration by utilizing CC-PTL based design in [62] and Chapter 2.

Finally, an analysis on system level scalability and limitation of PTL was presented. The calculation of number of drivers a PTL can support based on current carrying capacity as a function of PTL width was provided. A PTL centric routing strategy for a system with a large number of drivers was also proposed. The strategy is similar to the "fly-by" topology commonly used in DDR3 and DDR4 SDRAM layout designs.

CHAPTER 4. REDUCTION OF ELECTROMAGNETIC COUPLING BETWEEN SIGNAL AND POWER DISTRIBUTION NETWORK

4.1 Introduction

Return path discontinuity (RPD) for signal lines carrying high speed signals has been attributed to many factors that affect signal and power integrity. These factors include ground bounce, simultaneous switching noise and crosstalk coupling [9]. The use of PTL was aimed to reduce RPD, and it's effectiveness to improve SI and PI had been largely measured based on eye height, jitter and reduced power supply noise in the previous chapter and [44], [45], [48]. However, the more underlying contributors such as electromagnetic coupling between signal and power distribution network has neither been quantified nor compared with conventional plane based designs. Furthermore, the PTL based design was always compared with conventional voltage plane designs that had the signal trace referenced to the power plane as in [44]. Although such arrangement is not uncommon in high speed designs, signals referenced to ground plane is another popular topology that has not been addressed. The work presented in this chapter fills this void to 1) quantify RPD effect on power supply noise and EM coupling in PTL based design and 2) compare the effect with plane based designs for both voltage plane and ground plane referenced stack-ups in both time and frequency domains.

4.2 Reduction of PDN Induced Coupling Using PTL Power Distribution

Transmission lines carrying high speed I/O signals can couple significant amount of electromagnetic energy to power distribution network (PDN), which can then adversely affect signal and power integrity of the entire electrical system. Similarly, the reverse is

also true. We present the signal to PDN coupling measurement on three very complex printed circuit boards (PCBs) based on different PDN designs. These boards include via transitions on signal lines that tend to amplify the coupling. The stack-up information of the PCBs is summarized in Table 10. The foot-prints for vertical SubMiniature Version A (SMA) connectors was incorporated into the design at the location near the drivers. These behave as loads to the PTL so that the SMA connectors used to measure coupled energy to the PDN can be directly soldered onto the PCB. This provides stronger mechanical support and better reference connection for measurements. Through measured results, we demonstrate that PTL-based design provides better isolation than plane based designs for I/O circuits.

Table 10 Test Vehicle Information

	PTL Based (PTL)	Plane Based #1 (GP)	Plane Based #2 (PG)
Stack-up	--SIG-- --GND-- --GND-- --SIG/PTL--	--SIG-- --GND-- --PWR-- --SIG--	--SIG-- --PWR-- --GND-- --SIG--

4.2.1 PCB Information and Test Vehicle Design

Three 4-layer PCBs of the same size were designed. The stack-up information is summarized in Table 10. The overall thickness of each PCB was approximately 62-mil. The dimension of the PCBs was 6-inch x 5-inch. The dielectric material of the PCBs was FR4 Tg130 material with a dielectric constant of ~4.5 and loss tangent is ~0.025 at 1GHz. The prepreg thickness between the top/bottom layer and the adjacent plane layer was ~9.45 mil.

The inner core thickness was ~40 mil. The signal lines were routed as 50-ohm traces. For the PTL-based PCB, the PTL was routed as a 50-mil wide microstrip line which had an impedance of 25 Ω. The length of PTL from the point of power entry to the load is ~1.5 inches.

All component placement, types and signal trace routing were identical for all three test vehicles to ensure a fair comparison. The only differences were the stack-up arrangement and PTL-related layout. A screenshot of part of the fully routed design with critical components and routing is shown in Figure 57. We selected 12Gbps capable NBSG16VS drivers from On-Semiconductor® as the switching buffers. During the measurement, we used one buffer as the active load and the adjacent one as the idle or victim buffer. The buffers are differential drivers. To demonstrate coupling, we used the drivers in a single ended signaling fashion. Only one of the differential buffer output pins was routed to the output connector through a ~4.5-inch trace. The other differential output pin of the driver was locally terminated to ground through a 50-ohm resistor through "stuffing" options, as shown in Figure 57. Each driver has two power supply pins. Each pin is decoupled by a closely placed 0.1uF 0402 size decoupling capacitor to supply charge during high frequency transient. The placement of the decoupling capacitors, labelled as 1, and the 50-ohm terminating resistor, labelled as 2, is shown in the enlarged and dashed square box in Figure 57.

The output trace, the aggressor, that carries active signals is on the top of Figure 57 and goes through four vias to reach the output port, port 1, as shown in Figure 57 and Figure 58, which shows the side view of the routing. Port 1 is terminated to an edge-mount 50-ohm SMA connector. The length of segments of the trace ranges from ~790 mils to ~1250

mils. The overall output trace is ~4.5 inch. The victim trace, as shown in Figure 57 is 930 mils from the aggressor. The victim trace was routed as a microstrip line and terminated at Port 2, as shown in Figure 57. Port 3 connector is a vertical SMA connector placed between the two drivers. It has one center pin connected to the power rail. The surrounding 4 pins are ground posts. Such mounting provides sturdy mechanical support and good electrical connection. The final assembled PCB board is shown in Figure 59.

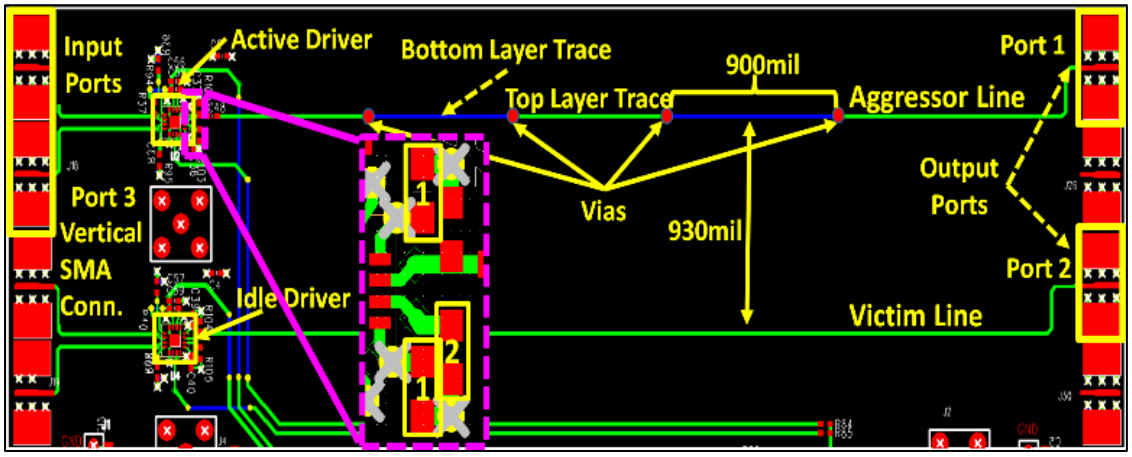


Figure 57 Sample printed circuit board layout showing critical components and dimensions

4.2.2 Measured EM Coupling from Signal Traces to PDN

To study the coupling effect between the signal traces and the PDN, we excited from port 1 and port 2 and measured the output on port 3 that is connected to the PDN. All measurements were done by using an Agilent Technologies E8363B PNA Series Network Analyzer that was calibrated using Short, Load, Open, and Through (SLOT) method. The test setup is shown in Figure 59b.

First we measured the coupling on the three bare PCBs with no other components other than the SMA connectors. Figure 60a is the measured s-parameter (S32) showing the coupling from port 2 to port 3. The PTL, GP and PG are shown as dashed line, solid line and dotted line, respectively. The same plotting convention is used for Figure 60b-

Figure 61 as well. As can be seen, the PTL-based PCB exhibits good and consistent isolation performance below -50 dB from ~200 MHz to 5 GHz while the PG PCB ranges above -10 dB in the low frequency region (below 1 GHz). The GP version of the plane design shows better isolation than the PG and similar performance as the PTL-based PCB but it shows generally more coupling above 1.4 GHz than the PTL-base PCB. At around 2.5 GHz, the PTL case is about 8 dB and 26 dB lower than the GP and PG cases, respectively, as shown in Figure 60a.

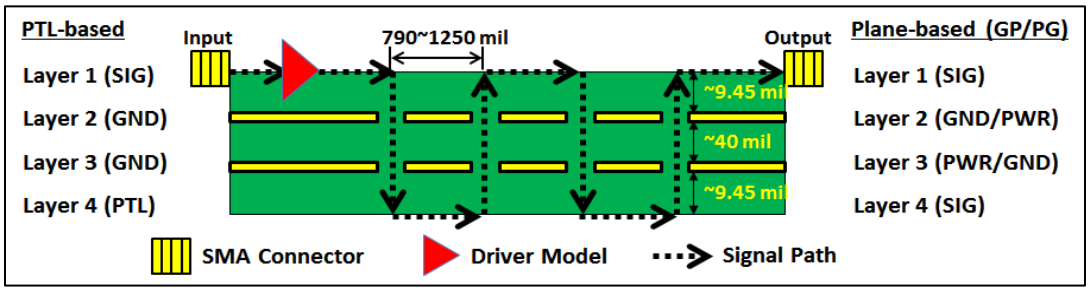
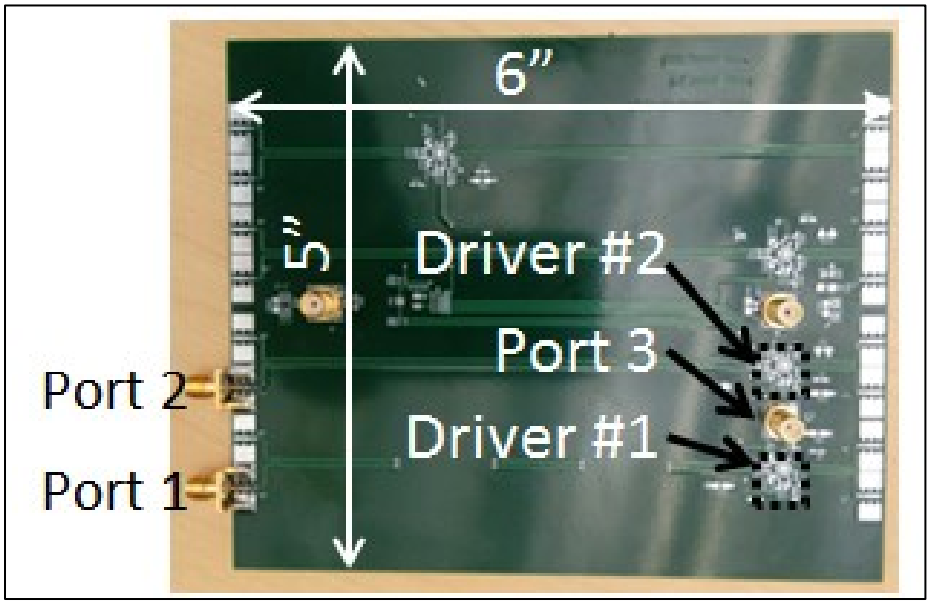


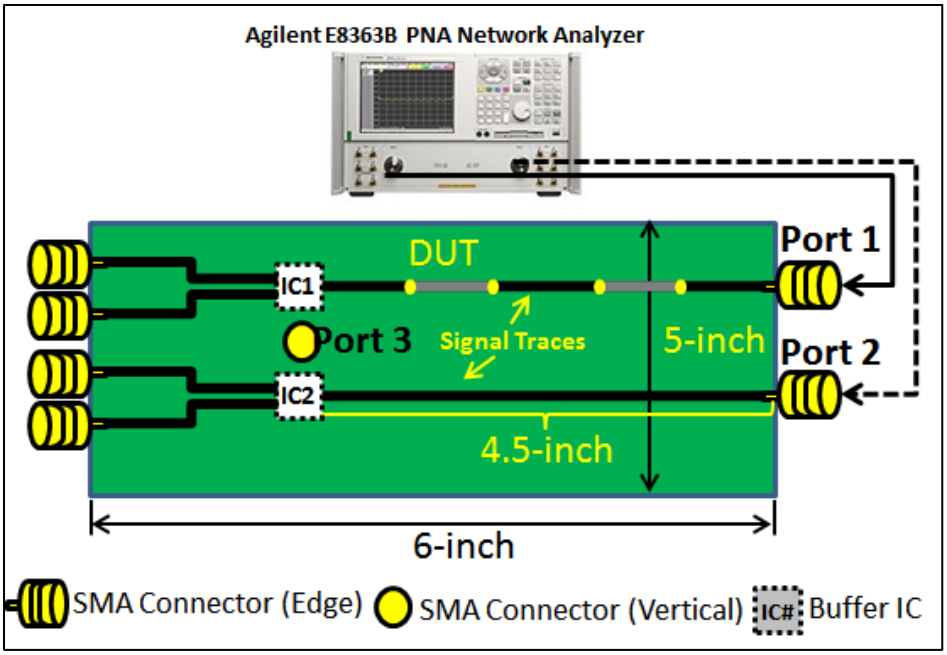
Figure 58 The signal path that makes several transitions through the PCB (not drawn to scale)

Figure 60b shows the measured coupling between port 1 and port 3 to examine how the coupling is affected when a signal makes via transitions through the board. This is a

practical scenario as some of the high speed signals would be forced to make transitions in high density board or package layouts. As can be seen the overall isolation is worse than if the signal was to be routed as a continuous microstrip line without any discontinuities as as in the shown in Figure 60a. Nonetheless, the advantage of PTL-based design in terms of isolation is evident in Figure 60b. As can be seen the coupling for the PTL design remains at or below -40dB. For example, at around 2.5 GHz, the PTL case is about 20 dB lower than both the GP and PG cases as indicated in Figure 60b. The advantage with GP over PG version can be clearly seen diminishes when the signal line traverses through the PCB with approximately equal amount of coupling to the power plane and ground plane. Therefore, PTL-based design is a better choice in a design that has limited layout area and many high speed signals going through via-transitions.



(a)

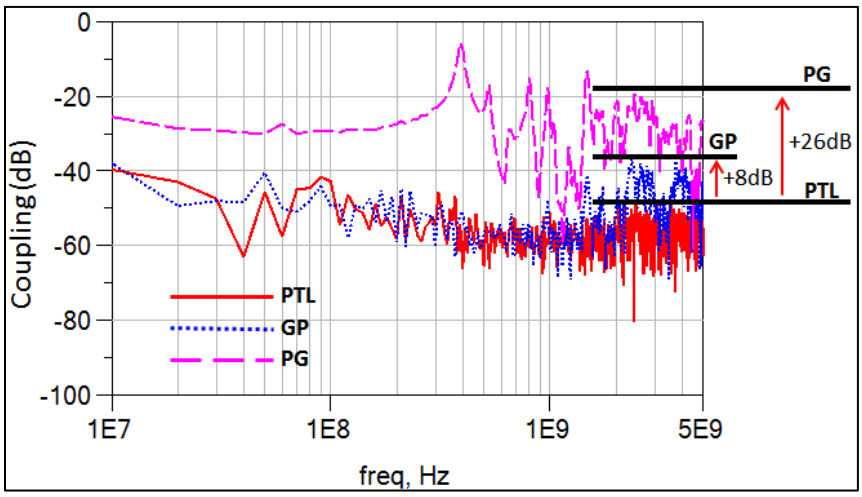


(b)

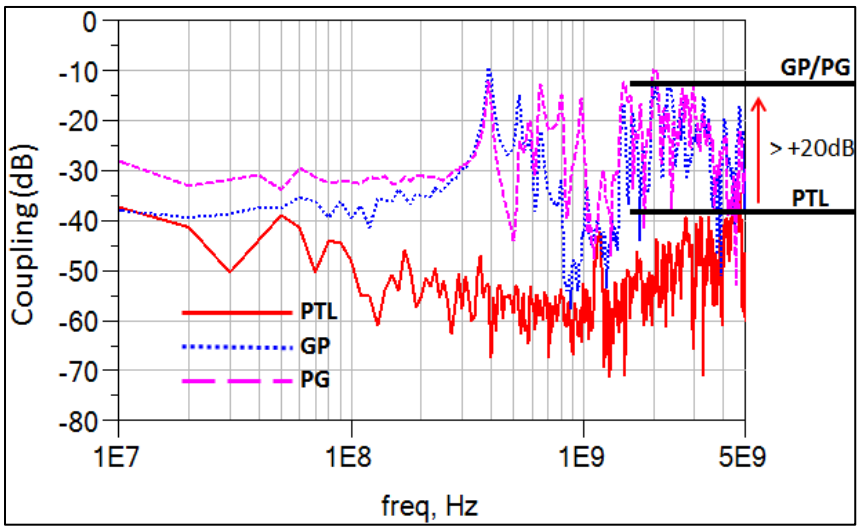
Figure 59 a) picture of the PCB and b) Test setup

Next, 0.1uF 0402 sized decoupling capacitors were soldered onto each of the bare boards, two capacitors near the power pins of each driver. Should the drivers be populated, these capacitors supply charge to the drivers under high switching I/O operation. As shown in Figure 61, the overall isolation at higher frequency range has become worse for all 3 cases as the decoupling capacitors serve as additional means to couple noise from the power plane and PTL to the ground reference plane. In the microstrip line coupling case as shown in Figure 61a, the PTL case is approximately 17 dB and 23 dB lower than the Ground-Power (GP) and Power-Ground (PG) cases, respectively at 2.5 GHz. In the via transition case as shown in Figure 61b, PTL-based design shows consistently lower than -30dB coupling in the entire measured frequency range, from 10 MHz to 5 GHz. At around

2.5 GHz, the PTL case is approximately 19 dB and 31dB lower than the GP and PG designs, respectively.



(a)

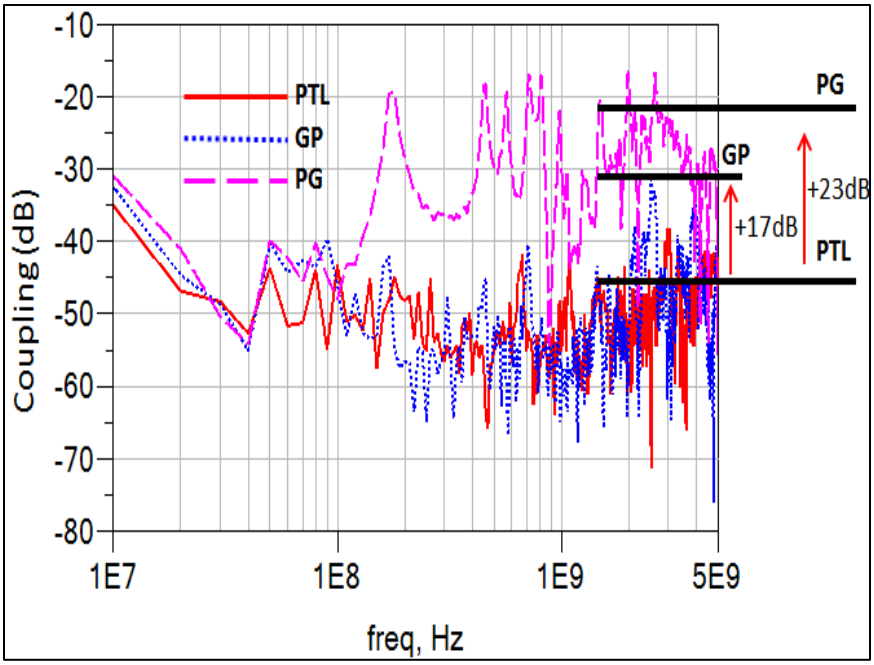


(b)

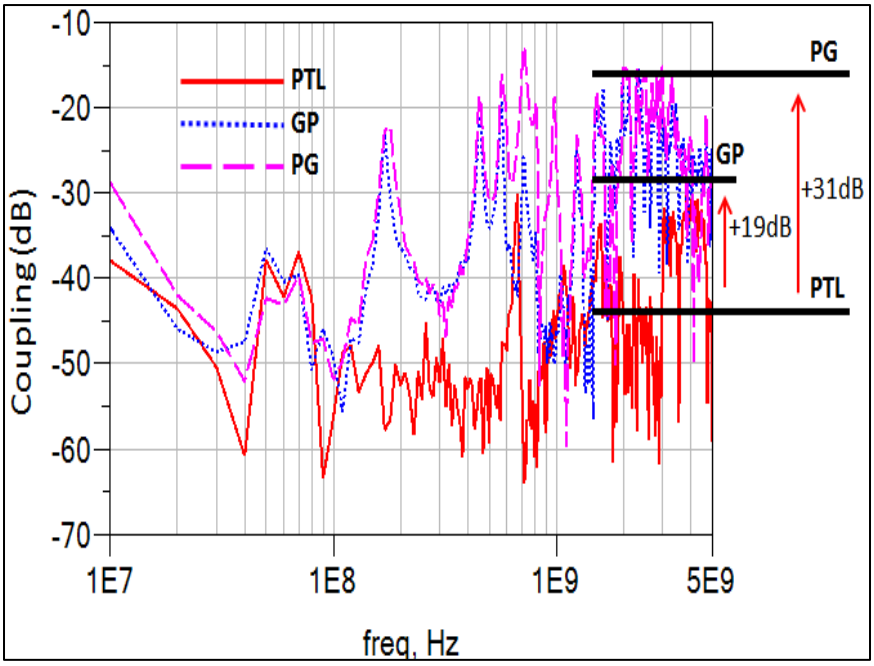
Figure 60 Coupling measurements for a) microstrip line and b) via-transitioned line on the bare PCBs

The signal and power integrity were evaluated for the three test vehicles as well when the active driver were populated on each of them and was driven differentially by an Agilent 81133A signal generator capable of producing up to 3.35 Gbps PBRS sequence with a randomness of $2^{31} - 1$. The eye diagrams and power supply noise were measured with an Agilent® DCA-X 86100D oscilloscope with a 50GHz bandwidth front receiver module. The eye diagrams were taken at port 1 and power supply noise was measured at port 3 near the active driver. The stimulus differential signals were set to 2^{31} PRBS, which had a very flat spectrum in the frequency domain. Five frequency sampling points from 1Gbps to 3Gbps were taken with an equal interval of 500Mbps. The statistical data for eye height, peak-to-peak (p-p) jitter is shown in Figure 62. The eye diagrams of port 1 when running at 2Gbps PRBS for the three test vehicles are also shown in Figure 62. The power supply noise measurement is shown in Figure 63.

The eye height and jitter data of both PTL and GP are better than the PG case. This is due to the additional RPDs in the PG case since the edge-mount SMA connectors were referenced to the ground plane while their connected traces were referenced to the power layer. There is no significant difference between the PTL and GP cases. However, Figure 63 shows PTL based design has a significant reduction in power supply noise than the other two plane based design. This is because of the elimination of the voltage plane and the reduction of electromagnetic coupling between signal lines and PDN network over a wide frequency range. Table 11 summarizes the comparison of power supply noise at the sampled frequency points. The PTL design reduced the noise by more than 68% over a wide range of frequency.



(a)



(b)

Figure 61 Coupling measurements for a) microstrip line and b) via-transitioned line on the PCBs with 0.1uF decoupling capacitors

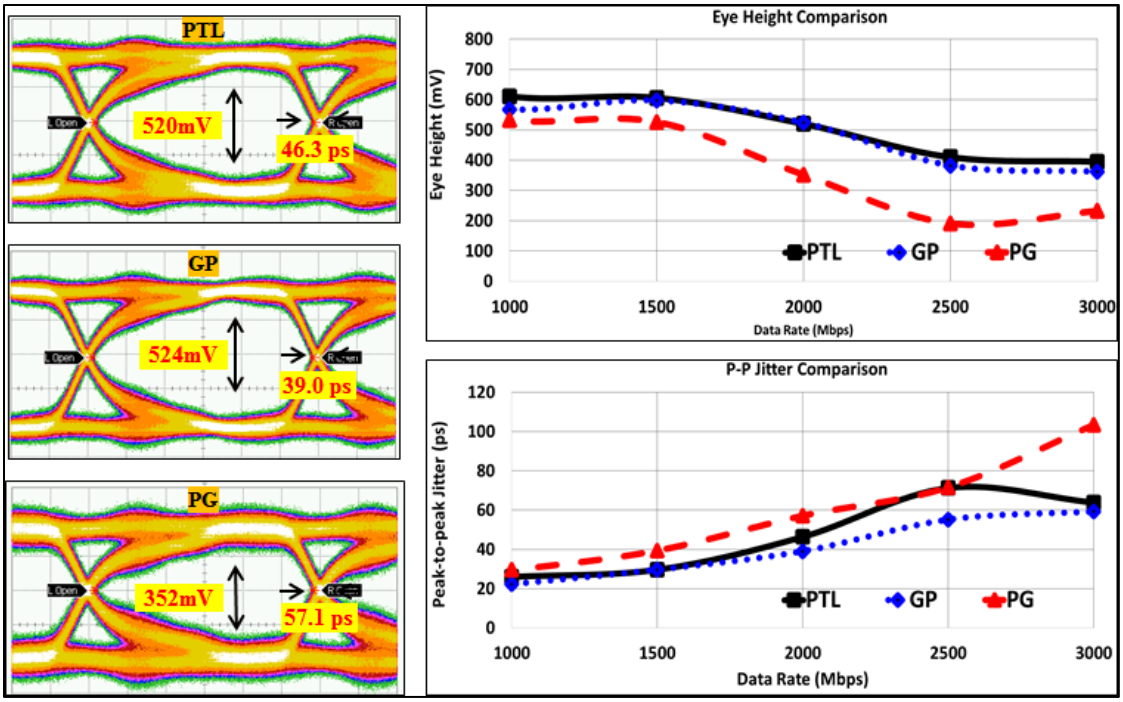


Figure 62 The comparison of the eye height and p-p jitter of three test vehicles and eye diagrams when running at 2Gbps PRBS signals.

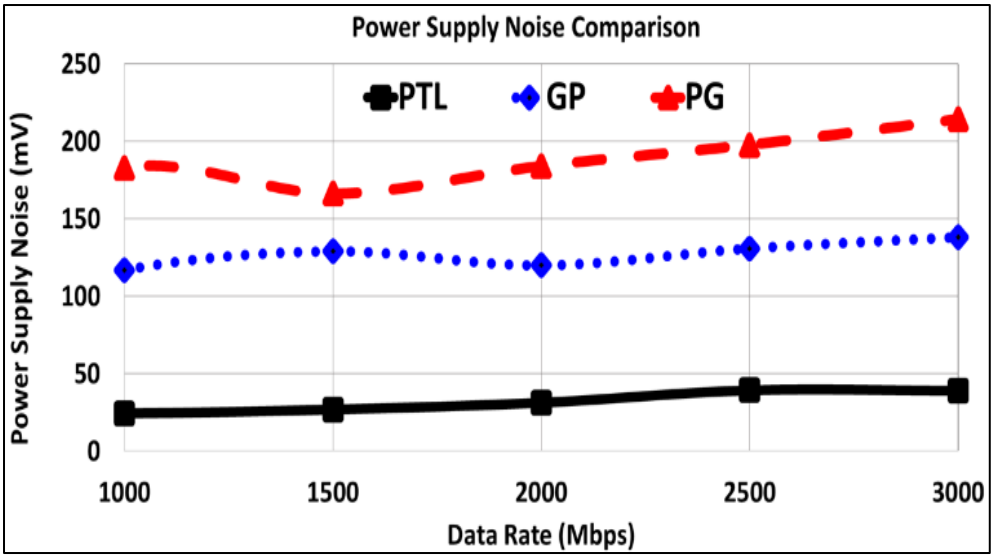


Figure 63 PSN of the three test vehicles when running gigabit rate PRBS signals.

4.2.3 Measured EM Coupling from Active Signal Trace to quiet Victim Trace

In this section we examine the coupling between the active signal trace making via transitions and the idle signal line on the three test vehicles by measuring coupling from port 1 to port 2, as shown in Figure 59a. Figure 64 is the measured s-parameter (S21) from 1GHz to 6 GHz. showing the coupling from port 1 that was connected to the via-transition trace to port 2, which was connected to the victim microstrip line. The PTL, GP and PG are shown as solid line, dotted line, and dashed line, respectively. The same plotting convention was used for Figure 65 as well. As can be seen, the PTL-based PCB exhibited good and consistent isolation performance below -40 dB from 1 GHz to 6 GHz while the PG test vehicle peaks above -10 dB between 1 GHz and 2GHz. The GP version of the plane design showed better isolation than the PG test vehicle but had worse performance than the PTL-based PCB except in narrow bands due to resonances.

Table 11 Power Supply Noise Comparison

Data Rate (Mbps)	PTL (mV)	GP (mV)	PG (mV)	noise reduction over GP*	noise reduction over PG*
1000	24.437	80.627	121.92	68.86%	79.41%
1500	26.957	117.09	182.87	79.13%	86.64%
2000	31.335	129.09	166.3	79.12%	83.79%
2500	39.349	120.03	184.09	73.89%	82.98%
3000	39.07	130.97	197.76	69.96%	80.10%

* The percentage of power supply noise reduction in PTL as compared to the plane based test vehicle at the corresponding data rate.

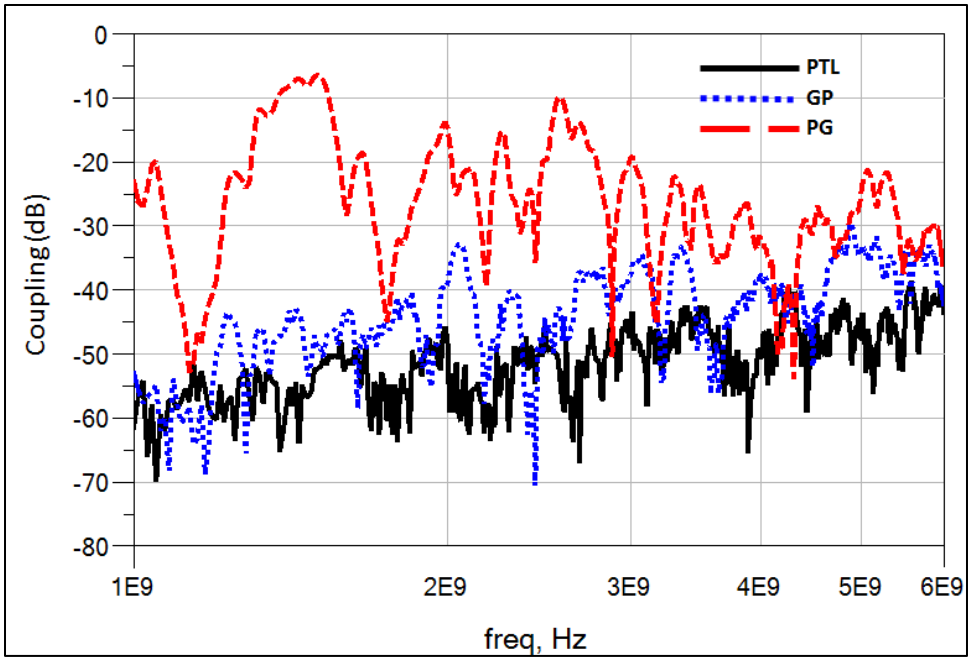


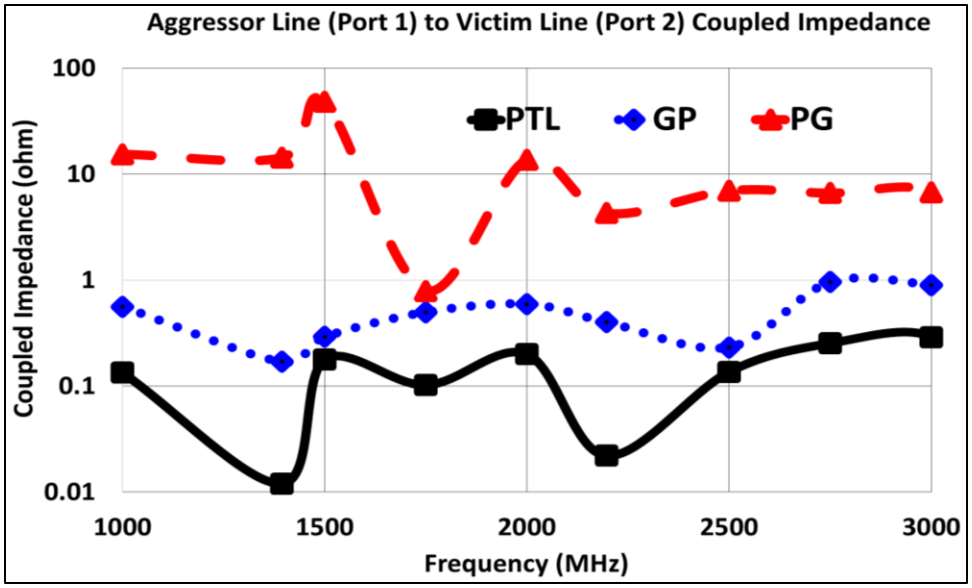
Figure 64 Measured coupling between port 1 and port 2 for all three test vehicles

Since the measured noise could be well correlated with coupled impedance, we convert several representative frequency points (1000, 1394, 1500, 1750, 2000, 2197, 2500, 2750, and 3000MHz) in Figure 64 from s-parameters to impedance magnitudes, as shown in Figure 65a. We then injected clock signals into input port running at the frequencies corresponding to those frequency points. The noise power at port 2 at the fundamental frequency of each clock signal was then measured and plotted in Figure 65b. Figure 65a and Figure 65b shows a reasonably well first order correlation indicating the higher the mutual coupled impedance between the two traces, the more noise will be coupled from one to the other. For example, at 1750MHz, there is a big drop in impedance on the PG curve in Figure 65b, which then corresponds to a lowered coupled noise in Figure 65b. In Figure 65b, we see that PTL has an overall lower and flatter coupled noise than the plane based PDN designs.

4.3 Coupling Between Signal Lines and Power Delivery Network in the 3D Test Vehicle

The advantage of reduced and wideband EM coupling by using PTL was shown in the previous sections. We now revisit the test vehicles built for the complex 3D systems and provide the fundamental backing for obtaining better SI and PI performance provided by the PTL-based system. Another advantage of studying another set of the PCBs is so that we can generalize and solidify our previous observation and conclusion. We focus our study on the daughter cards since they were used for signaling. Although we only had one voltage plane based daughter card with the power-ground inner layer assignment in the stack-up, we modified another PG board so that the second layer (reference layer for the signal) was reassigned to ground layer. Since the buffers used could operate under negative supplies, we had ensured normal circuit operation without issues.

For ease of referencing, we denote the PTL based daughter card (DC) as PTL_DC (Figure 66a). The original plane based DC with power-ground inner layer assignment as VP_DC (Figure 66b). The modified DC with ground-power layer assignment is named SVP_DC (Figure 66c). The stack-up for the third PCB (SVP_DC), therefore, had signal-ground-power-signal assignments. The size of the overlapped area between voltage and ground planes for both VP_DC and SVP_DC was 4.75-inch x 7.64-inch. The total length of the power transmission line was approximately 43.46-inch long with a width of 50-mil for PTL_DC. Other than the stack-ups and the PDN arrangements, all three daughter cards had the same component placement and signal routing topology.



(a)

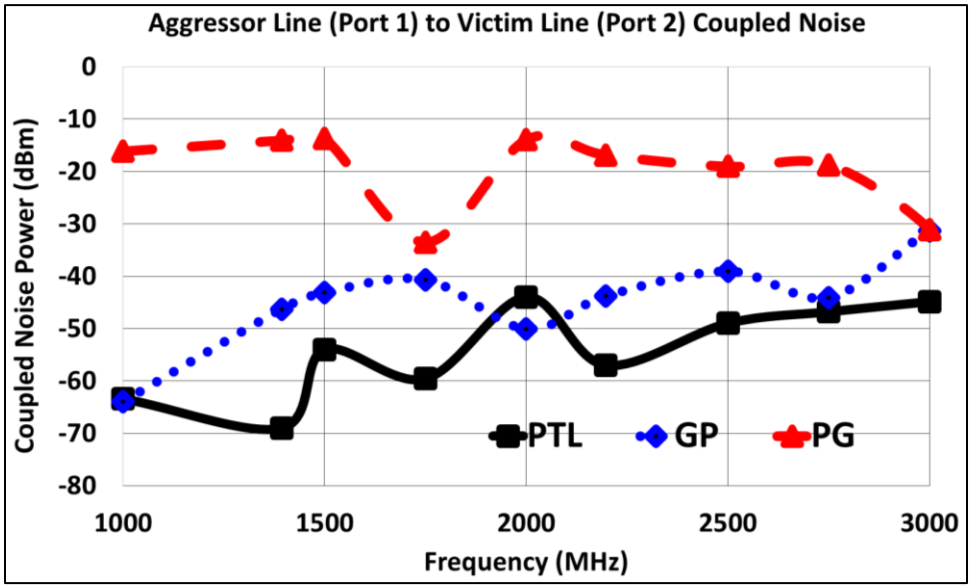


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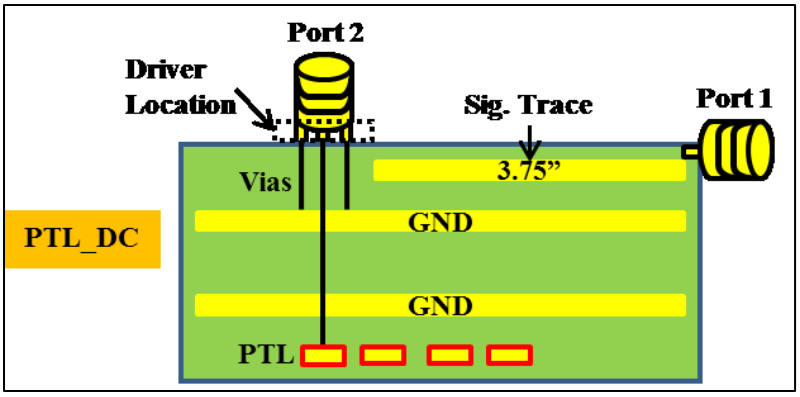
Figure 65 (a) Measured impedance from port 1 to port 2 and (b) measured coupled noise power at port 2 for all 3 test vehicles at the select frequencies. X-axis shows the clock frequencies of the aggressor.



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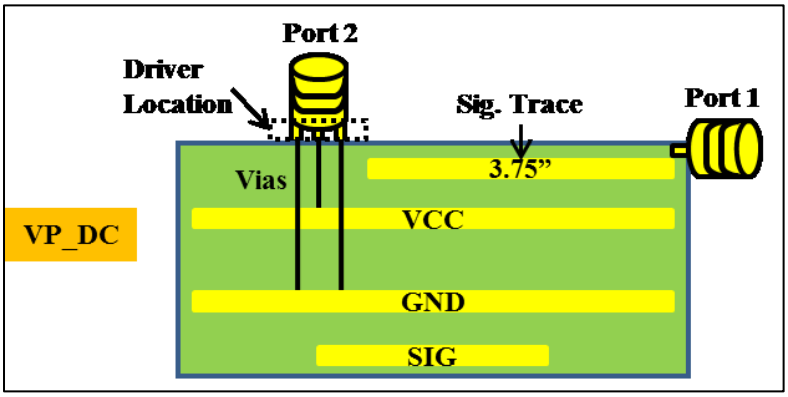

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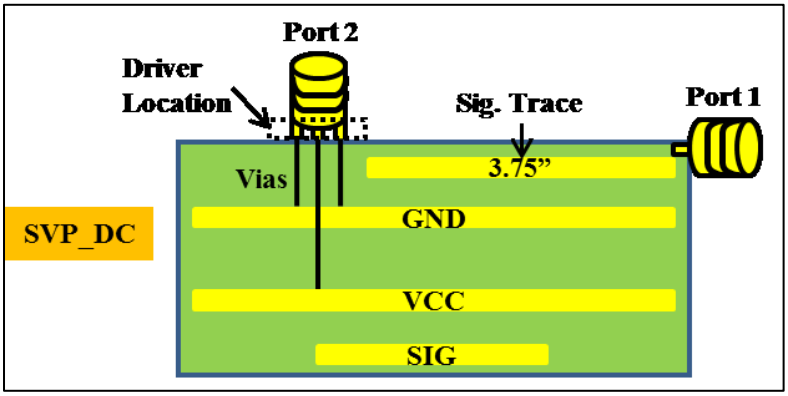


(c)

Figure 66 Daughter card stack-up for a) PTL_DC, b) VP_DC and c) SVP_DC.

None of the three PCBs had any populated I/O buffers. It is important to note that the mounted components for all three cards were the same and were at the same locations. The B-B connector pin assignments were identical for all boards and the same decoupling capacitors were used on the daughter cards as described earlier in Figure 39. The signal generator was connected to port 1 of each daughter card (Figure 66) through an SMA coaxial cable. The oscilloscope was then connected to port 2 of each card to measure coupled noise. Port 1 connector was connected to the single-ended output pin of the I/O buffer footprint on the daughter card through an approximately 3.75-inch long microstrip signal line, which was then connected to GND through a 50 Ω resistor, not shown. Port 2 was soldered to a power-ground via pattern near the I/O buffer location, as shown in Figure 66. The location of Port 2 was the same as where the power supply noise was measured when three daughter cards were stacked together, as shown in Figure 50a. Figure 67 is the measured s-parameter (S21) showing the coupling from port 1 to port 2 by using an Agilent Technologies E8363B PNA Series Network Analyzer. The PTL_DC, VP_DC and SVP_DC are shown as dashed line, solid line and dotted line, respectively. The same plotting convention is used for Figure 68- Figure 70 as well. As can be seen, the PTL daughter card exhibits good and consistent isolation performance below -35 dB from 10 MHz to 4 GHz while the voltage plane PCBs are above -20 dB in the low frequency region below 1 GHz. The peaks relate to the anti-resonance points due to the size of the voltage-ground plane cavity. The calculated anti-resonance frequencies based on rectangular waveguide formula as described in [44] for different modes are shown in Table **12**. Although, voltage plane based PCBs shows better isolation in narrow bands at higher frequencies, the isolation for the PTL design is consistently below -35 dB, which

constitutes less than 2% coupling. To better understand the coupling effect on noise, the following frequency points were converted from the S21 plot in Figure 67 to Z21: 0.25, 0.50, 0.75, 1.0, 1.5, 2.0, 2.5, 2.72 and 3 GHz, and the results are plotted in Figure 68 for all three PCBs. Port 1 was driven by the signal generator with a clock signal, which was used as an aggressor, at the aforementioned frequencies. The coupled time-domain P-P noise at port 2 corresponding to the selected frequencies was then measured and is shown in Figure 69. The x-axis is the clock frequency of the aggressor signal. When comparing Figure 68 and Figure 69, both figures show a direct correlation between the impedance between the two ports and the amount of coupled noise. For example, the measured impedance for SVP_DC peaks at 750 MHz, which implies maximum coupling, and dips at 2.72 GHz, which indicates the least coupling, as can be seen in both Figure 67 and Figure 68. The measured P-P noises at these two extreme frequencies were 108 mV and 7.62 mV, respectively. For the PTL_DC, the measured P-P noise showed stability across the measured frequency range. The noise levels were also measured in the frequency domain when the signal generator was driving port 1 at the same nine frequencies as listed above. The noise level in dBm measured at the fundamental frequency of each of the nine clock frequencies is shown in Figure 70. The x-axis is the clock frequency of the aggressor signal. A similar trend shown in Figure 68 is evident in Figure 70 as well.

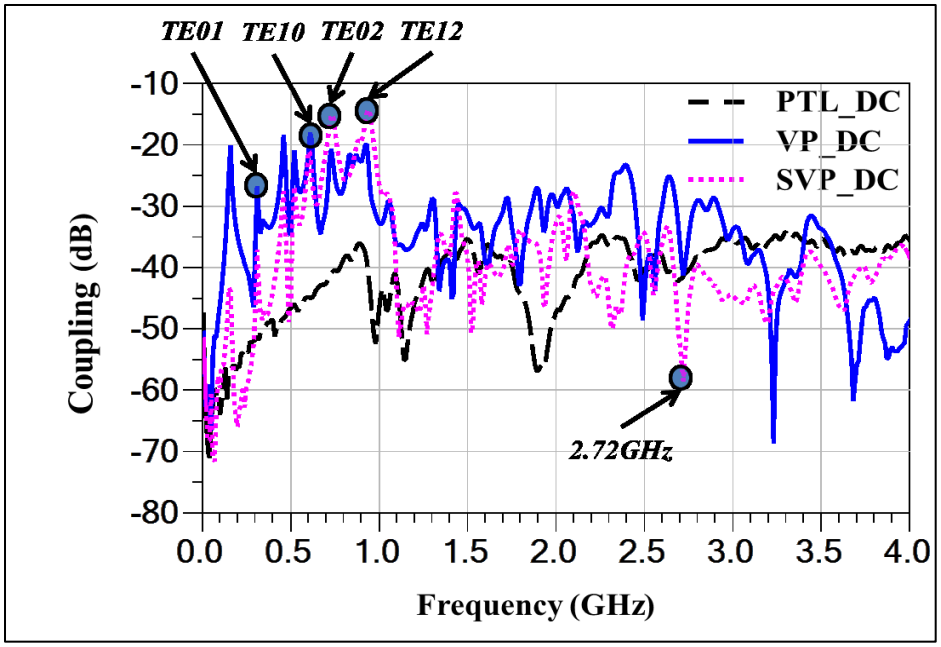


Figure 67 S-Parameter of isolation for the three daughter cards.

Table 12 Calculated & Measured Resonant Frequency

Width (inch)	Length (inch)	m	n	Calculated (GHz)	Measured (GHz)
4.75	7.64	0	1	0.36	0.31
		1	0	0.59	0.61
		0	2	0.73	0.73
		1	2	0.94	0.94

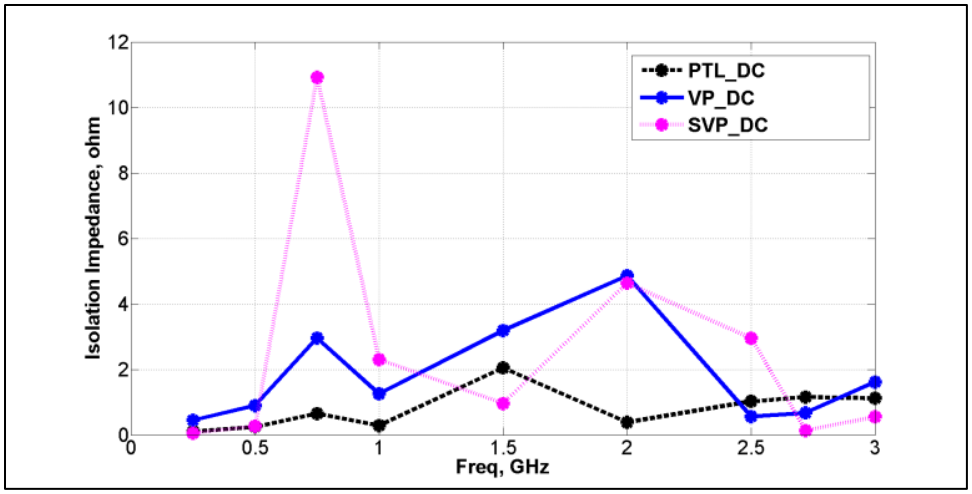


Figure 68 Measured impedance from port 1 to port 2 for all 3 bare boards at the select frequencies.

Overall we observe that PTL based daughter card showed consistently low coupling below -35 dB, as shown in Figure 67. The measured P-P coupled noise on the PDN was below 40 mV with small deviation from 250 MHz to 3 GHz. The reason that voltage plane based daughter cards showed higher and more variant noise coupling is due to the coupling between the signal trace and the PDN. On the other hand, the performance advantage of the PTL based design can be attributed to the PDN and signal lines sharing a common reference plane.

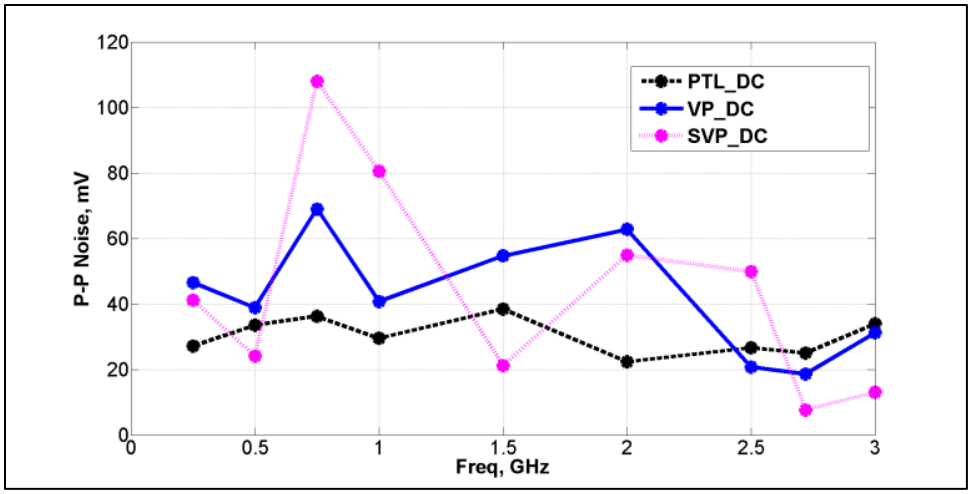


Figure 69. Measured coupled P-P noise at port 2 for all 3 bare boards at the select frequencies. X-axis shows the clock frequencies of the aggressor.

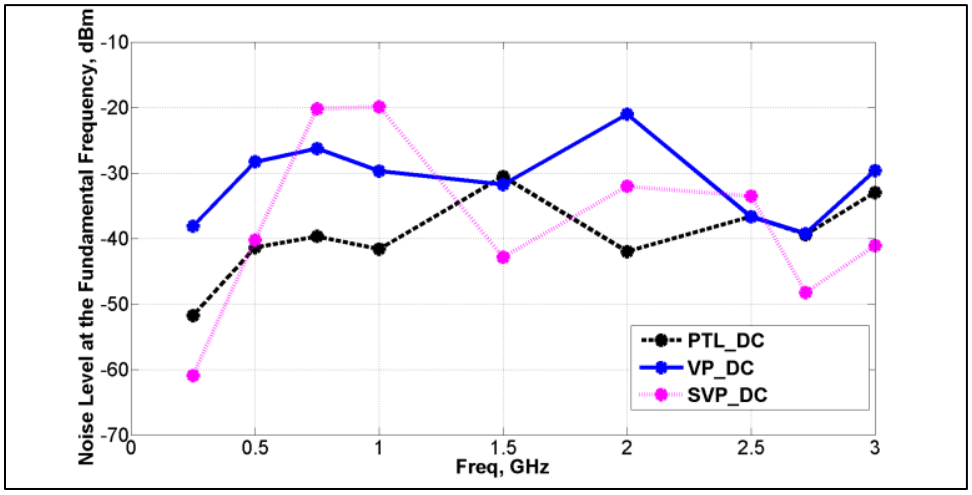


Figure 70. Measured coupled noise at port 2 at the fundamental clock frequencies of the aggressor for all 3 bare boards at the select frequencies.

4.4 Summary and Conclusion

In this chapter, we first presented three PCB designs each with a different power delivery network design. One is based on power transmission line concept and the other

two based on conventional power-ground plane based approach. We first examined the noise coupling from high speed signal traces to the PDN and made comparisons between the three designs. Through measured results we showed the following:

1) Without any active or passive components, the PTL-based PCB showed consistent isolation below -50dB between the microstrip signal line and the PDN from 200 MHz to 5 GHz. The GP test board showed similar performance up to around 1.4 GHz. The PG plane based board; however, showed the worse coupling performance with some peaks reaching above -20 dB, as shown in Figure 60a.

2) When a signal made via transitions, the overall isolation became worse and the difference between the two plane-based cases was statistically insignificant across the entire 5GHz bandwidth. However, the advantage in PTL was still evident with a better than -40dB isolation in most of the bandwidth, as shown in Figure 60b.

3) When decoupling capacitors were added to a PCB, the signal to PDN isolation was adversely affected as the capacitors served as AC short between the power and ground planes. The PTL still offered better and consistent isolation than the plane based designs in most of the bandwidth; better than -40dB in the microstrip case (Figure 61a) and better than -30 dB in the via-transition case (Figure 61b). The lower power supply noise provided by PTL can serve as a significant advantage in managing power distribution network in noise sensitive system applications.

We next turned our attention to study the effect of electromagnetic coupling from a high-speed signal line that traverses through a multi-layered PCB by means of through-hole vias to adjacent signal lines and the power distribution network. Through measured results, we showed that there is a clear and direct first-order correlation between the

coupled impedance between the aggressor and victim trace, and the measured noise at the fundamental frequencies of the excitation clock signals. The PTL-based design showed an overall lower measured coupling below -40 dB from 1 GHz to 6 GHz. As a result, less coupled noise was observed due to the reduced RPD effects. We also compared the signal integrity and power supply noise between the three test vehicles. PRBS signals of different bit rates were utilized to drive the buffer that was connected to the signal trace with vias on each PCB. Since the PTL-based design had better electromagnetic isolation between signal traces and PDN in most of the frequency spectrum, as shown in Figure 64, the measured power supply noise in this design was more than 68% lower than the other two test vehicles at five sampled bit rates from 1 Gbps to 3 Gbps.

We also revisited the daughter cards used in the 3D test vehicles as described in Chapter 3. One of the plane based daughter card was modified so the second layer that the signal trace referenced was assigned to ground plane. Similar EM coupling measurement between an active microstrip-type signal trace and the PDN was done for both PTL based and the two plane based daughter cards with opposite inner ground and power layer assignment. The PTL based designed showed better than -35 dB coupling from 10 MHz to 4.0 GHz while the plane based PCBs showed frequency peaking well above -30 dB.

In summary, the PTL based PDN offers broadband and better EM isolation between signal and power distribution network than conventional PDN designs that use voltage-ground pairs. Such advantage makes PTL especially attractive to highly sensitive circuits with very stringent noise and coupling requirement.

CHAPTER 5. ENHANCING THE BANDWIDTH OF LOW-DROPOUT (LDO) REGULATORS USING POWER TRANSMISSION LINES FOR HIGH SPEED I/Os

5.1 Introduction

The constant voltage PTL or (CV-PTL) as outlined in Chapter 1 and detailed in [48], places a resistive network between the PTL and the logic load, as shown in Figure 71. The controlling logic of the resistive network will ensure the sum of the selected resistor value in the network and the total resistance looking into the logic load will remain the same regardless of the logic level of the digital load. However, such implementation is digital in nature as there are only a certain number of discrete resistor values that can be chosen. It is; therefore, unable to allow for change in impedance when the digital loads transition from one logic state to another. Furthermore, the resistor in series with the PTL further consume additional power as a result of this implementation. When examined closely; nonetheless, the function and purpose of the resistive network in the CV-PTL implementation is primarily similar to that of a Low-Dropout voltage regulator (LDO) that regulates the current flow to the external load by adjusting the on-resistance of the pass power transistor, as shown in Figure 22. Therefore, instead of using the resistive network to minimize current transient on the PTL, we turn our attention to using LDO in its place.

Before going into the detail of the co-design of PTL with LDO, we examine the current state of the art power delivery topology. In modern computer systems, there are many voltage supplies. These are generated using DC/DC converters where buck converters are used to step-down the voltage from a main DC supply. Depending on the voltage conversion ratio, buck converters have a power efficiency in the range of 70%-

90% [81], [82], [83] and [84]. The buck converters are also referred to as Voltage Regulator Modules (VRM). To improve both power efficiency and voltage regulation, the recent trend is to move towards fully integrated voltage regulators (FIVR) to supply both the core and I/O circuits for System on Chip (SOC) applications [85], [86] and [87]. One implementation of FIVR is to integrate the buck converter with SOC as a two chip solution on a package with passives such as inductors and capacitors either surface mounted or embedded in the package [88].

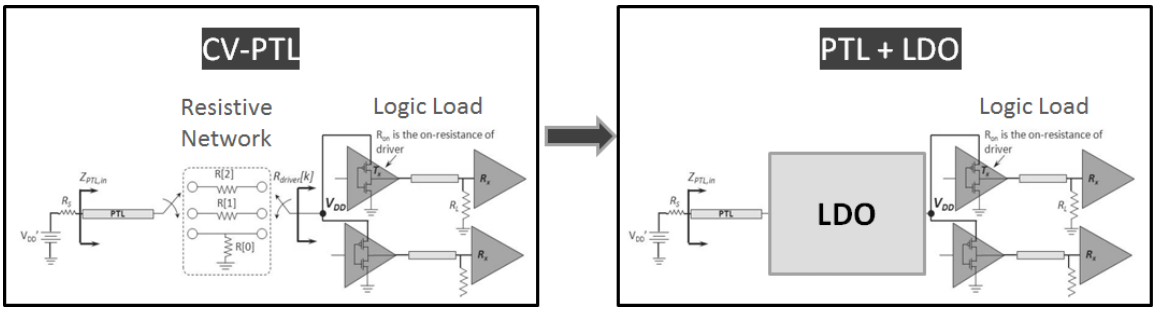


Figure 71 CV-PTL design transitioning to PTL and LDO circuit implementation

To ensure fine grained power management, LDO regulators are integrated in the SOC in close proximity to the load. Several LDOs integrated in the SOC are used to provide voltage regulation for both the core and the I/O circuits. An embodiment of a VRM connected to an LDO circuit was shown in Figure 4 and is again shown in Figure 72 for ease of referencing. However, the PDN dimension information is shown in Figure 72 pertaining to the design parameters in this chapter. The voltage from the buck converter is supplied to the LDOs using voltage and ground planes in the package and/or printed circuit board (PCB), as shown in Figure 72. Often times, voltage islands are used to separate the

core and I/O power distribution to minimize noise coupling between the two. One of the challenges in the implementation of LDO circuits is the power supply rejection (PSR) peaking that occurs when its regulating feedback loop gain reaches 0 dB. Around this frequency, the PSR of the LDO degrades resulting in large power supply noise. Hence, it is important to keep the impedance of the power delivery network (PDN) low in this frequency range. For typical LDOs, the PSR peaking occurs in the 50 MHz – 100 MHz range [89], [90], a frequency range where the chip-package or board anti-resonances occur [6]. A combination of PSR peaking and large package/board impedances can reduce the bandwidth of the LDO regulator leading to excessive power supply noise. This can also decrease the LDO efficiency. In this chapter, our focus is on the LDO regulators used for I/O drivers. As shown in Figure 72, our objective is to replace the power planes with power transmission lines (PTL) between the VRM and the LDO regulator so as to enhance the bandwidth of the LDO, thereby reducing noise at the power supply terminals of the I/O drivers.

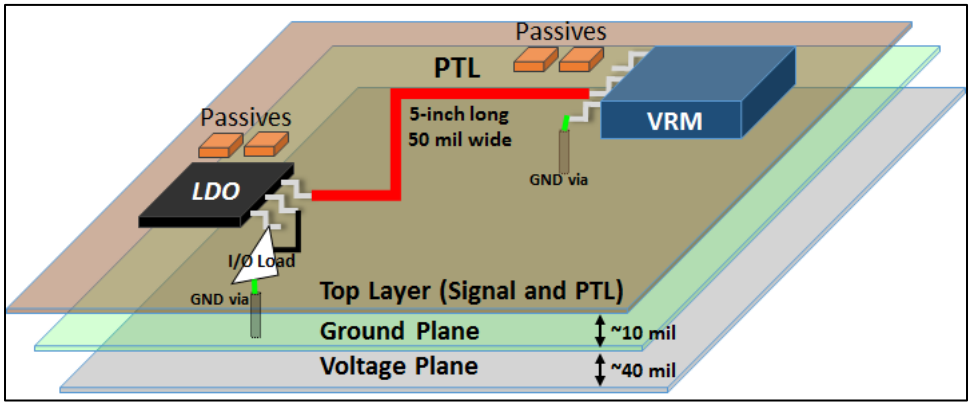


Figure 72 Two-chip voltage regulator (not drawn to scale)

Power transmission lines, unlike power/ground planes, are high impedance structures that can be used for power delivery in computer systems. These structures have been shown to reduce power supply noise for I/O drivers by eliminating return path discontinuities [44], minimizing coupling in mixed signal circuits [54] and significantly reducing the coupling between signal and power delivery networks in printed circuit boards [63], [65] and [66]. In this chapter, we extend this concept for LDO regulators with a goal of improving its bandwidth, reducing power supply noise and enhancing system performance. We demonstrate these improvements through measurements on a PCB containing commercial off-the-shelf (COTS) components by comparing the PTL implementation with a more conventional plane based implementation.

5.2 Working of an LDO

This section describes the workings of an LDO using design equations with emphasis on its loop gain, PSR and efficiency. Consider Figure 73(a) where the buck converter supplies voltage to the LDO through a power delivery network (PDN). The LDO regulator regulates the voltage at its output, v_{OUT}. The output of the LDO is shown as a simple RC load. In the figure, v_{IN} and v_{OUT} contain both DC and small signal AC components corresponding to the DC voltage and voltage ripple, respectively. The PSR for the LDO regulator can be defined as:

$$\text{PSR} = \frac{\partial v_{OUT}}{\partial v_{IN}} \equiv \frac{v_{out}}{v_{in}} \quad (3)$$

where v_{in} and v_{out} represent the small signal ac components only. For an LDO regulator, the goal is to minimize PSR to ensure that the LDO can effectively reject a large ripple at its input to minimize ripple at its output.

An example of an LDO regulator circuit is shown in Figure 73 (b) where a shunt-feedback loop is used for voltage regulation. To derive the PSR of the LDO regulator, a small-signal voltage divider model can be used, as shown in Figure 73 (c) [16]. In the figure, the error amplifier is used to sense and regulate the LDO regulator output by modulating the power transistor resistance of Q_1. To simplify the analysis, we assume that the negative feedback loop in the circuit can be represented as a two pole system, where the dominant internal pole (P_1) is at the gate of the PMOS transistor Q_1, and a second pole (P_2) is at the output of the LDO. In the circuit, the low frequency loop gain is A_{LG0}. The frequency dependent loop gain A_{LG} in Figure 73(b) can be written as:

$$A_{LG} = \frac{A_{LG0}}{\left(1 + \frac{s}{j2\pi P_1}\right) * \left(1 + \frac{s}{j2\pi P_2}\right)} \quad (7)$$

where s=jω and ω is the angular frequency.

In Figure 73(c), Z_{UP} is the impedance between the input and output of the LDO given by:

$$Z_{UP} = \frac{v_{IN} - v_{OUT}}{I_{PMOS}} \quad (8)$$

where I_{PMOS} is the current through the PMOS transistor. The shunt feedback impedance, Z_{SH} in Figure 73(c), which is the open-loop output impedance reduced by the loop gain assuming v_{in} is an AC ground can now be calculated as [16]:

$$Z_{SH} = \frac{Z_{UP} \parallel Z_{LOAD} \parallel (R_1 + R_2)}{A_{LG}} \quad (9)$$

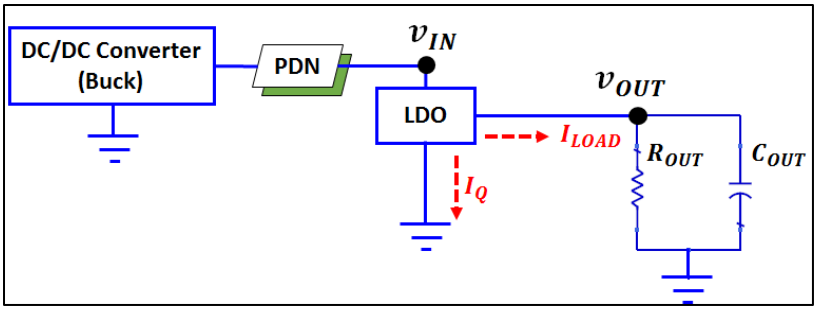
where Z_{LOAD} is the parallel impedance of the output resistance and capacitance, R_{LOAD} and C_{LOAD}, respectively. The pull down impedance Z_{DN} can now be calculated as the total impedance from v_{OUT} to AC ground, which is the impedance of Z_{LOAD} and Z_{SH} in

parallel, as shown in Figure 73(c) [16]. The PSR can now be derived as:

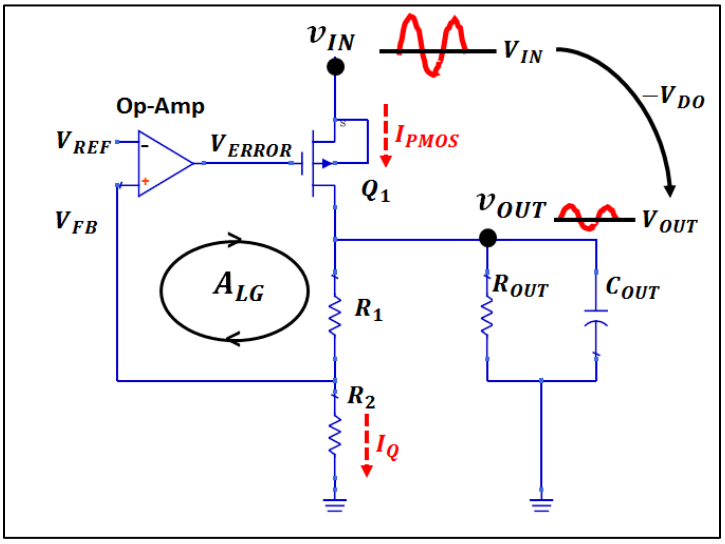
$$\mathrm{PSR} = \frac{\partial v_{OUT}}{\partial v_{IN}} = \frac{Z_{DN}}{Z_{DN} + Z_{UP}} \quad (10)$$

From (7), to maintain good PSR, a high Z_{UP} to reject noise, and a low Z_{DN} to bypass current ripple away from the LDO output is desired.

Using equations (7)-(10), the frequency response of the loop gain and PSR are shown in Figure 74. Typical LDO design parameters used in obtaining the plot are shown in Table 13. At lower frequency before pole P_1 (Region 1), the loop gain is at its maximum value, and the corresponding PSR is at its minimum. This corresponds to good power supply rejection where the PSR can be approximated as Z_{DN}/Z_{UP} since $Z_{DN} \ll Z_{UP}$. In Figure 74, pole P_1 occurs at ~1.5 MHz. Beyond pole P_1 the loop gain begins to decrease, thereby increasing impedance Z_{SH}. The PSR now begins to rise, as shown in Figure 74 until it peaks near the 0dB frequency (f_{0dB}) at approximately 50 MHz. At this frequency, the LDO has its worst regulation, and the PSR can be approximated as $Z_{DN}/Z_{DN} \cong 1$ or 0 dB. From Figure 74, the PSR has a large value in the 40 MHz to 100 MHz frequency range (Region 2). Between Region 1 and 2, the PSR is moderate. After the second pole P_2, which occurs at ~66 MHz, the impedance Z_{SH} begins to decrease again causing the PSR to decrease [16]. It is important to note that the PSR of the LDO circuit can be affected by other parasitics in the package and board. The important takeaway from the analysis is the frequency range of 40MHZ-100MHz where the PSR peaking occurs, which coincides with the package and board PDN anti-resonances in most systems [6]. Therefore, the PDN in Figure 73(a) needs to be co-designed with the LDO circuit to compensate the PSR peaking effect.



(a)



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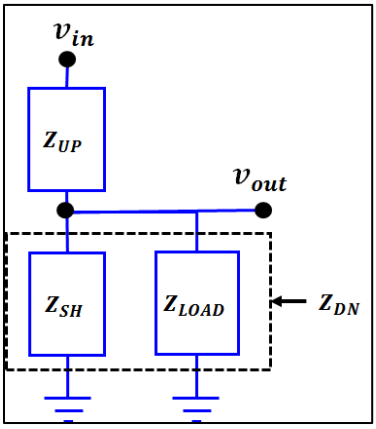


(c)

Figure 73 (a) Voltage distribution and regulation schematic, (b) LDO regulator circuit and (c) voltage-divider model [16]

Table 13 Parameters Used to Generate PSR and Loop Gain of an LDO

Parameter	Value	Unit
V_{IN}	1.2	V
V_{OUT}	0.8	V
I_{PMOS}	100	mA
R_{LOAD}	8	Ω
C_{LOAD}	300	pF
A_{LG0}	-30	dB
P_1	10e6	rad/sec
P_2	416e6	rad/sec

Along with the PSR, another important parameter for the LDO circuit is its energy conversion efficiency (η_{LDO}). The efficiency can be defined as:

$$\eta_{LDO} = \frac{P_O}{P_O + P_{loss}} = \frac{I_{LOAD} * V_{OUT}}{(I_{LOAD} + I_Q) * V_{IN}} = \eta_I * \frac{V_{OUT}}{V_{IN}} \quad (11)$$

where P_o and P_{loss} is the output power and the power loss. I_{LOAD} and I_Q are the DC load and quiescent current as in Figure 73(a), respectively, and η_I is the current efficiency. The DC input and output voltages are related to each other by:

$$V_{IN} = V_{OUT} + V_{DO} \quad (12)$$

where V_{DO} is the dropout voltage across the PMOS transistor, as shown in Figure 73(b); this results in:

$$\eta_{LDO} = \eta_I * \frac{V_{OUT}}{V_{IN}} \approx \frac{V_{OUT}}{V_{IN}} = \frac{V_{OUT}}{V_{OUT} + V_{DO}} \quad (13)$$

where $\eta_I \sim 1$ assuming quiescent current is negligible compared to I_{LOAD}.

From (13), the dropout voltage (V_{DO}) is an important parameter that determines the efficiency where a lower dropout voltage (or low Z_{UP} impedance) always results in higher conversion efficiency. However, good PSR rejection for the circuit requires a large Z_{UP}

impedance. Hence, a design solution to handle the tradeoff between PSR and energy conversion efficiency is required. This is possible by co-designing the PDN and LDO circuit such that both good PSR and high efficiency are achievable. We provide details of these design tradeoffs in the next section.

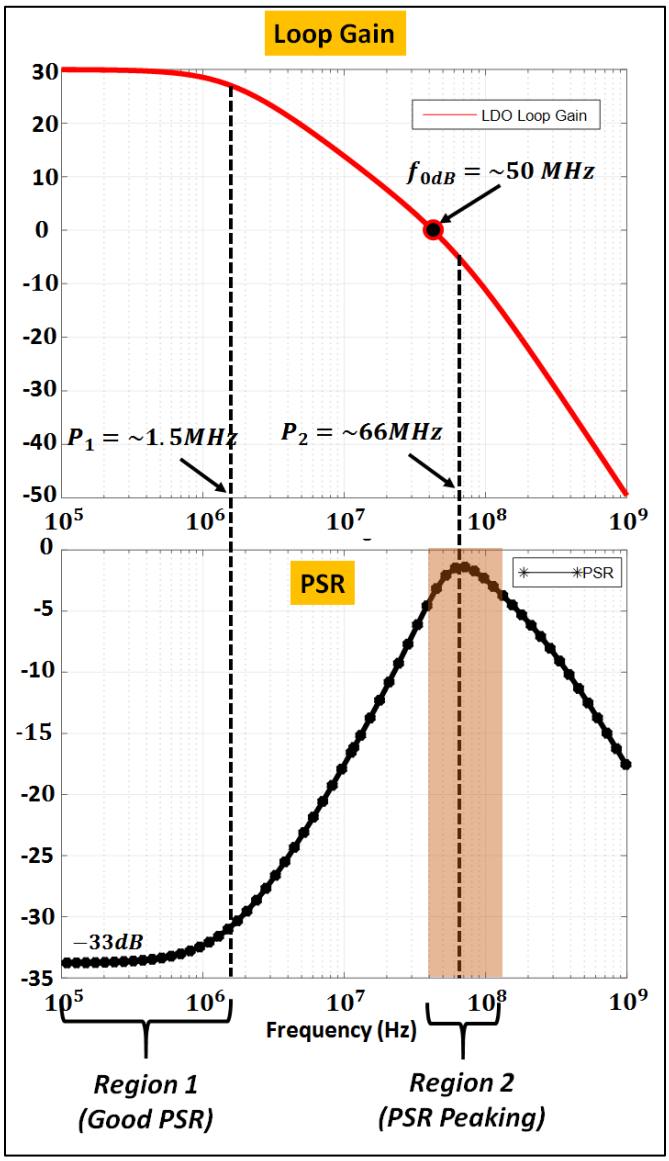


Figure 74 Simulated Loop Gain and PSR of the LDO circuit

5.3 Modeling and Simulation

Traditionally, DC/DC converter and LDO are connected through a power delivery network (PDN). The PDN consists of voltage/ground planes and bulk/decoupling capacitors. The goal of designing the PDN is to keep its impedance low in a wide frequency range [20], [23]. However, a combination of the plane and capacitor parasitics causes its impedance to increase. In addition, the interaction between the chip and package causes an increase in its impedance as well. Most of these high impedances occur in the frequency range of 40MHz – 100MHz [91], [92] and [93], a frequency range where the PSR peaking occurs for typical LDO regulators (Region 2 in Figure 74). Our focus in this section is to quantify the impact of such high PDN impedances on the workings of the LDO regulator, and suggest remedies. In this section we use structures used later in measurements (Section VIII) to illustrate these effects.

Based on Figure 73(a), the PDN delivers power from the buck converter to the LDO circuit which in turn regulates the voltage for the I/O drivers. Based on prior work [6], [91], [92] and [93], the PDN impedance in general peaks in the 50MHz frequency range. Since the impedance peak occurs due to the parallel resonance between the chip capacitance and package/PCB inductance, moving these impedances to lower or higher frequencies can be difficult. For example, any reduction in the inductance of the PDN to shift the impedance peak to higher frequencies can be challenging due to the limitations posed by the geometrical structures used in the package and PCB. Similarly, pushing the impedance peak to lower frequency by increasing the capacitance on chip can be difficult as well.

To capture the effect of the PDN impedance on the workings of an LDO, we construct a circuit as shown in Figure 75, where voltage and ground planes measuring 6”

x 5” separated by 40 mil of FR-4 (dielectric constant is 4.5) are used in the PCB to connect the buck converter to the LDO circuit. The capacitor C_{IN} in Figure 75 is used to create a parallel resonance between the planes and the capacitor. In Figure 75, the self-impedance at V_{IN} looking towards the buck converter is constructed by adding the capacitor C_{IN}, which results in an impedance peak around 50MHz so as to mimic the behavior of the PDN in realistic systems [91], [92] and [93]. The self-impedance at port V_{IN} looking towards the buck converter is shown in Figure 76 before and after placing the capacitor. From the figure, the high impedance can be seen around 50 MHz where C_{IN} = 2.2 nF with ESR = 8 mΩ and ESL= 400 pH has been used. In Figure 75, the switching converter is represented using a simple series R-L circuit to capture its close-loop impedance, where L_S=2 nH and R_S=5 mΩ.

Based on Figure 75 and Figure 76, we perform two sets of studies to understand the effect of PDN impedance and DC resistance on overall energy conversion efficiency, PSR and power supply noise (PSN). We assume $V_{IN} = 1.2V$ and that the quiescent current is negligible ($I_{LOAD} \cong I_{PMOS}$= 100 mA). The noise current is assumed to be 5% of the load current at 5 mA. In Figure 75, the noise power spectrum density in the PSR peaking region is represented by the shaded spike in frequency band B3 where noise in other bands (B1, B2 and B4) are outside of the PSR peaking region. From the figure, the noise spectrum at the output of the LDO circuit can be high (B3), since the impedance of the PDN is high in this frequency range.

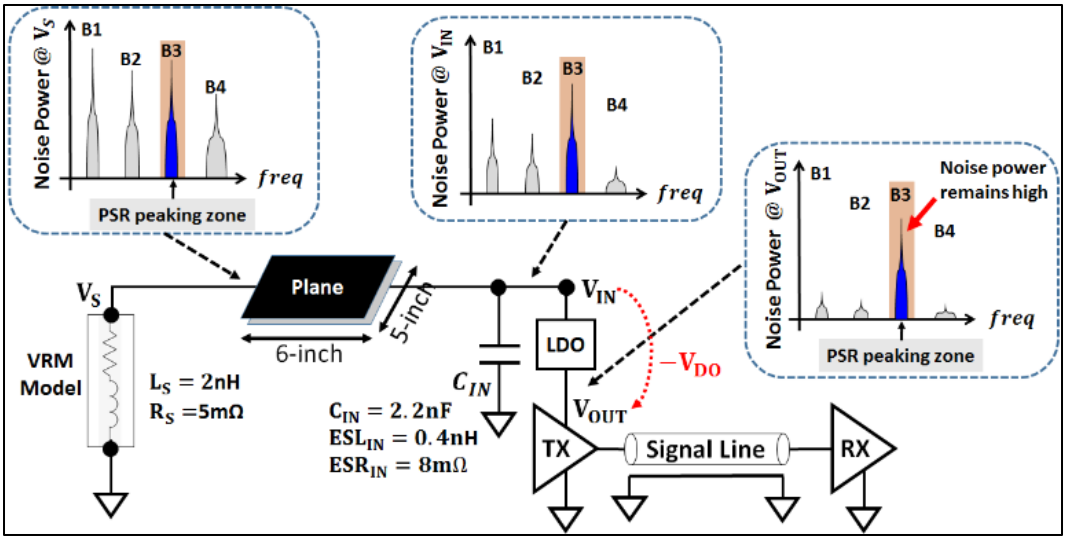


Figure 75 Plane PDN architecture connection between VRM and LDO.

Using a plane resistance ($R_{DC-plane}$) of 5 mΩ, the LDO model described in section II has been used to calculate the performance of the LDO circuit. Table 14 lists the PSR and efficiency. The V_S shown in Figure 75 is the sum of V_{IN} and the voltage drop across the PDN due to the DC resistance. Two cases have been studied, as described below.

Case 1. LDO dropout voltage, V_{DO}=0.4V

In the first study we set the dropout voltage across the LDO PMOS transistor as 0.4V. For I_{LOAD}=0.1 A, the power absorbed by the PDN is $P_{PDN} = I_{LOAD}^2 * R_{DC-plane} = 50$ uW; the power loss due to the PMOS transistor is $P_{DO} = I_{LOAD} * V_{DO} = 40$ mW and output power is $P_{OUT} = I_{LOAD} * V_{OUT} = 80$ mW. Therefore, the input power is 120.05 mW according to:

$$P_{IN} = (P_{PDN} + P_{DO}) + P_{OUT} = P_{LOSS} + P_{OUT} \quad (14)$$

The energy conversion efficiency of the system is therefore:

$$\eta_{SYS} = \frac{P_{OUT}}{P_{IN}} = 66.6\% \quad (15)$$

The LDO power supply noise at node V_{IN} in Figure 75 can be calculated as:

$$V_{IN\_noise} = Z_{IN} * I_{noise} \quad (16)$$

where I_{noise} is the noise current, which is assumed to be 5mA, and Z_{IN} is 99.45 Ω from the simulation results. Based on the LDO circuit model in section II, the PSR was calculated as -2.07 dB with a resulting power supply noise at the output of the LDO circuit to be ~0.39 V. The results of this case are shown in Table 14.

Case 2. V_{DO}=0.5V

In this study we improve the PSR of the LDO circuit by increasing the dropout voltage to 0.5V. As can be seen in Table 14, the PSR improves by 16.6% to -3.65 dB, which was obtained by setting $V_{OUT} = 0.7V$ in the simulated LDO model. The resulting power supply noise at the output of the LDO circuit is ~0.33 V, which improved by 16.6% as compared to Case 1. However, due to the increased dropout across the PMOS transistor, the power efficiency reduces by 12.5% to 58.3% as compared to Case 1. Hence, it is difficult to achieve high efficiency and low power supply noise at the output of the LDO circuit simultaneously, especially at frequencies where the PDN impedance peaks occur, as illustrated by the results in Table 14. We provide a remedy for this problem by using power transmission lines, as described in the next section.

5.4 Power Transmission Lines (PTL)

In Figure 72, we first separate the PDN for the core and I/O circuits where unlike the voltage and ground planes used to distribute power to the core, we use a narrow interconnection to connect the buck converter to the LDO regulator for the I/O circuits.

This is shown in Figure 77, where the power transmission line (PTL) represents the narrow interconnection. (Figure 77 is a repeat of Figure 24 for ease of referencing.) The PTL is referenced to the ground plane used in the package and PCB to form a continuous loop and represented as a microstrip line in Figure 77. The architecture in Figure 77 was simulated in this section and compared to Cases 1 and 2 described in the previous section.

Table 14 PSR and Energy Conversion Efficiency Comparison

Row #	**Energy Conversion Efficiency Result**			
		Case 1 Plane (V_{DO}=.4V)	Case 2 Plane (V_{DO}=.5V)	Case 3 PTL (V_{DO}=.3V)
1	η_{SYS} (%)	66.6%	58.3%	74.7%
2	η_{SYS} Improvement		-12.5%	12.1%
	PSR Result			
3	PSR rejection (dB)	-2.07	-3.65	-0.405
4	Impedance at LDO input Z_{IN} @ 50 MHz, (Ω)	99.45	99.45	1.68
5	Noise at LDO output, V_{OUT_noise} (V)	0.39	0.33	0.008
6	Noise improvement		16.6%	97.9%

As an example, consider a PTL geometry that is 50 mil wide, 5 inch long and with a dielectric thickness of 10 mil above a ground plane. The self-impedance of the PTL at V_{IN} of the LDO circuit is shown in Figure 78. As expected, the frequency response is very inductive as compared to a typical PDN structure. Placing a capacitor at the V_{IN} port of the LDO circuit results in an impedance peak due to the parallel resonance between the PTL

inductance and capacitor capacitance. By controlling the dimensions of the PTL and value of the capacitor, the position of the impedance peak can be tuned, thereby leading to low impedance in the PSR peaking region of the LDO circuit. This is illustrated in Figure 78, where the same capacitor C_{IN} (Figure 75) is used in the circuit in Figure 77, leading to an impedance peak at ~24 MHz. The resulting impedance around 50MHz is small at ~1.68 Ω. The effect of the small PDN impedance is shown in Figure 77, where the noise spectrum density in the PSR peaking region shown as B3 is significantly attenuated at the output of the LDO circuit, leading to smaller power supply noise as we will show in the Case 3 study.

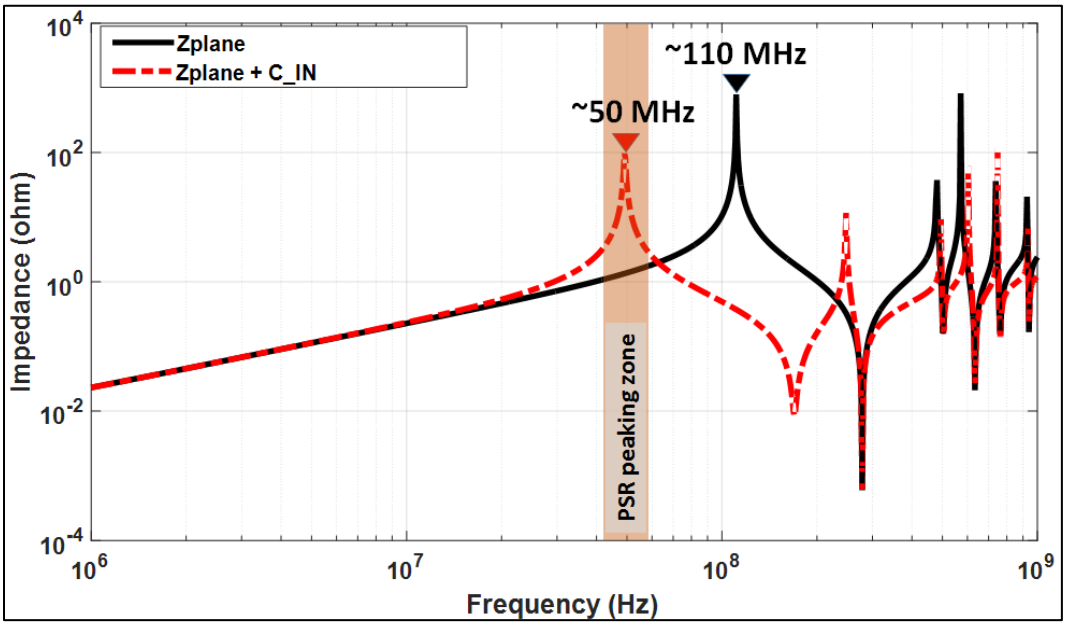


Figure 76 Plane self-impedance with and without decoupling capacitor

Unlike, a typical PDN, PTLs are easy to design and tune. We compare the response of the LDO circuit described in Figure 77 with the two cases described earlier but with a

lower drop out voltage to illustrate that both the efficiency and PSN can be improved using this architecture.

Case 3. V_{DO}=0.3V

In Figure 77, we set the dropout voltage across the PMOS transistor to 0.3V resulting in a worsening of the PSR to -0.405 dB according to the simulated LDO model by setting $V_{OUT} = 0.9V$. However, since the self-impedance of the PDN which is 1.68 Ω is much lower compared to the previous cases at around 50 MHz, the resulting power supply noise at the output of the LDO circuit is 8.04 mV, as represented by the significantly reduced noise power spike in B3 of Figure 77 at the LDO output. As compared to Case 1, the power supply noise reduces by 97.9% using PTL. Though the PTL has a higher simulated DC resistance (48.5 mΩ in this example), the overall energy conversion efficiency is 74.7%, an improvement of 12.1% as compared to Case 1 due to the lower dropout voltage. As can be seen from Table **14**, the results for Case 3 are much better as compared to both Cases 1 and 2 in terms of efficiency and power supply noise.

We conclude therefore that by co-designing the PTL with the LDO circuit, significant improvements in overall energy conversion efficiency and power supply noise are possible.

5.5 Design of Power Transmission Lines

Unlike power planes, PTLs are easier to design. Since voltage and ground planes are 2D structures, they behave as a cavity resonator resulting in standing wave resonances along two dimensions [6]. In contrast PTLs are 1D structures and hence the standing wave resonances occur only along a single dimension. Since the PTL connects the Buck Converter to the input of the LDO circuit, the DC resistance of the PTL needs to be

controlled to maximize system efficiency. In addition, the inductance of the PTL needs to be controlled to ensure that the parallel resonance between the PTL and capacitor leads to low impedance in the PSR peaking range. These can be managed by designing the PTL with suitable width (W), length (L), and dielectric thickness (D), as shown in Figure 72.

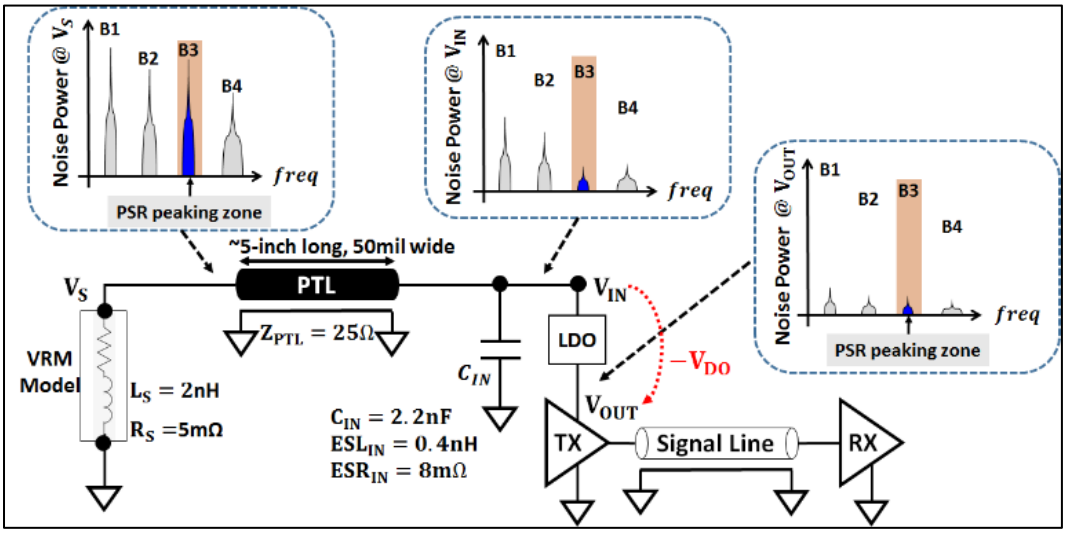


Figure 77 Proposed architecture to combine PTL with LDO

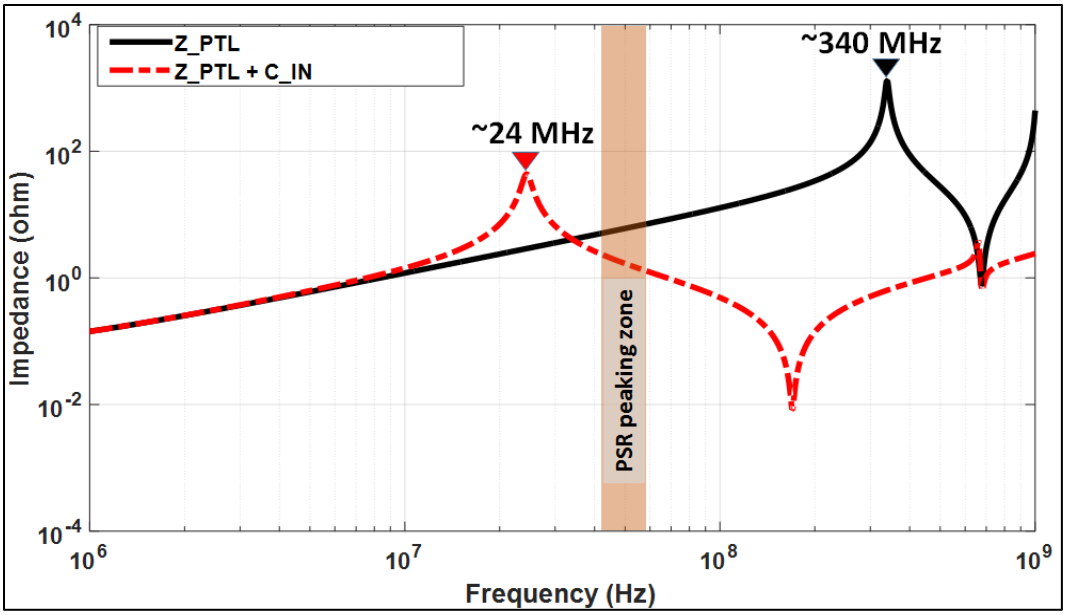


Figure 78 PTL self-impedance with and without decoupling capacitor

As an example for an LDO circuit with a dropout voltage of 0.2V, the DC drop across the PTL can be budgeted to be 2% of the dropout voltage, which translates to a system efficiency of ~80% for a 1V input. For a load current of 0.1A, the DC resistance of the PTL therefore needs to be 40 mΩ. This parameter can be used to determine the W and L of the PTL based on:

$$R = \rho \frac{L}{W \times T} \quad (17)$$

where ρ is the resistivity and T is the thickness of the line. Similarly, since the inductance of a microstrip line can be approximated as [94]:

$$L = 0.00508 * L * \left(\ln\left(\frac{2*L}{W*D}\right) + 0.5 + 0.2235 * \left(\frac{W+D}{L}\right)\right) \quad (18)$$

Depending on the inductance required, the width W, length L and dielectric thickness D can be suitably adjusted. Therefore, the design equations in (17) and (18) can be co-

optimized to determine the optimum values for W, L, and D that provides the lowest DC resistance and the desired inductance. After determining the physical dimensions of PTL, equations (4)-(6) can be used to determine the maximum number of loads a PTL can support.

Signal distribution networks in the package and PCB often incur return path discontinuities (RPD) due to the interruption in current return path of signal lines. RPDs can lead to significant signal integrity issues such as ground bounce, simultaneous switching noise and crosstalk to name a few [9], [50]. When planes are used, irrespective of the signal referencing (signal referenced to voltage or signal referenced to ground), the interruption in the current path causes RPDs that can affect signal and power integrity. The source of these discontinuities are shown in Figure 10 where the receiver (RX) is terminated by a resistor in parallel. The current path for the charging of the signal line is shown in Figure 10 (discharging scenario not shown), where RPDs occur due to the return current transitions between inner planes [9], [50].

In contrast, the signal trace in the construction of the PTL references the ground plane. This eliminates the voltage plane for I/O circuits and hence inherently ensures an uninterrupted current return path regardless of data transition direction, as shown in Figure 11. This significantly improves signal and power integrity in systems as demonstrated in [44]. Since PTLs are primarily inductive, they are high impedance structures, as opposed to power planes that have low impedance. In the past we have shown that using PTLs to power I/O drivers improves eye height and jitter by over 15% and 36% [44], respectively, since any coupling between the signal and PDN is minimized [63], [65] and [66]. Furthermore we have shown that a single PTL can be used to power multiple drivers [44],

[63]. Hence, along with improving LDO efficiency and power supply noise, PTLs provide significant SI benefits as well.

5.6 Test Vehicle Design

In this section we validate the results from the previous sections using PCB test vehicles with COTS components.

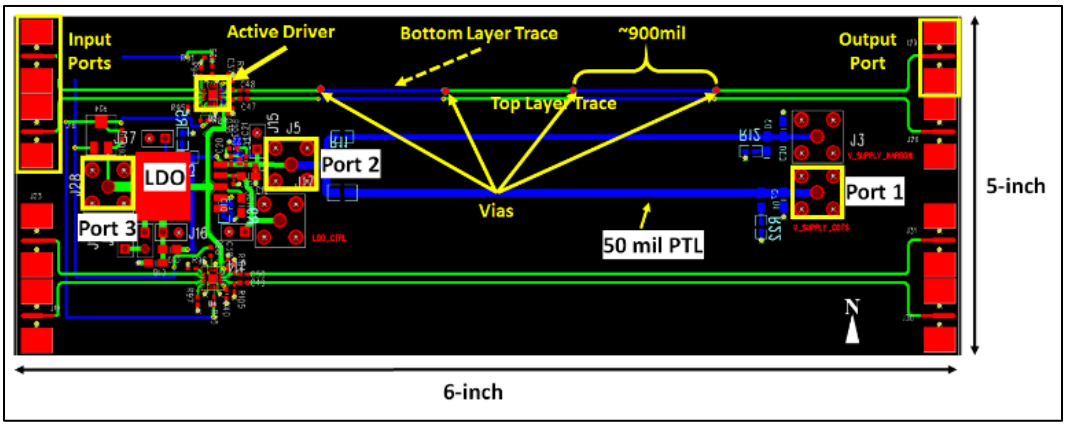
5.6.1 Design of Printed Circuit Board Test Vehicles

Three 4-layer PCBs were designed and fabricated. The first PCB design used PTL while the other two used power and ground planes to connect to the input of the LDO circuit. The layer assignments for all three boards are shown in Table 15.

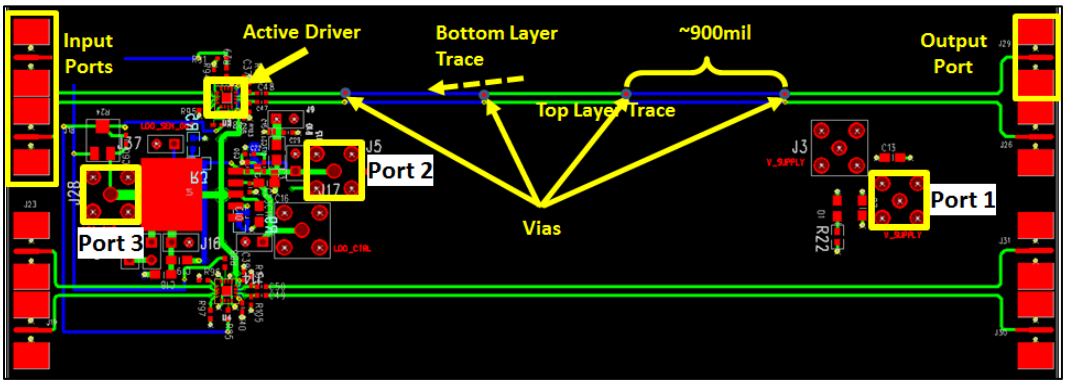
The PCBs using planes were categorized as GP (Ground-Power) and PG (Power-Ground). This was done to look at two scenarios where the signal line is either referenced to the ground or voltage plane. The PTL PCB had no inner power layers since the power was delivered using PTL, which was routed on the bottom layer. A 50-mil wide PTL was used to supply the LDO chip, where the PTL length was ~4.98 inches. This translates to a characteristic impedance of 25 Ω. The measured DC resistance was ~30 mΩ by using a digital voltage meter. The measured inductance was approximately 3.97 nH at 100 MHz. The PTL PCB design layout is shown in Figure 79, which shows the critical components and dimensions. The fabricated PCB material information and dimensions are the same as in Chapter 4 and 5.3. The PCBs using planes had the same construction as in the PTL based design (except for the PTL routing) and is shown in Figure 79b

Table 15 Test Vehicle PCB Stack-Up Information

Test Vehicle	PTL	Plane: GP	Plane: PG
Stack-up	--SIG-- --GND-- --GND-- --SIG/PTL--	--SIG-- --GND-- --PWR-- --SIG--	--SIG-- --PWR-- --GND-- --SIG --



(a)



(b)

Figure 79 Test vehicle layout for a) PTL design and b) plane design

5.6.2 Schematic Design and PCB Layout

Each test vehicle included an LDO supplying two high speed I/O buffers and a 27 Ω load resistor, R_L, as shown in Figure 80. The buffers and LDO regulator were from On-Semiconductor (P/N: NBSG16VS) and Linear Technology (model number: LT3083 [95]), respectively.

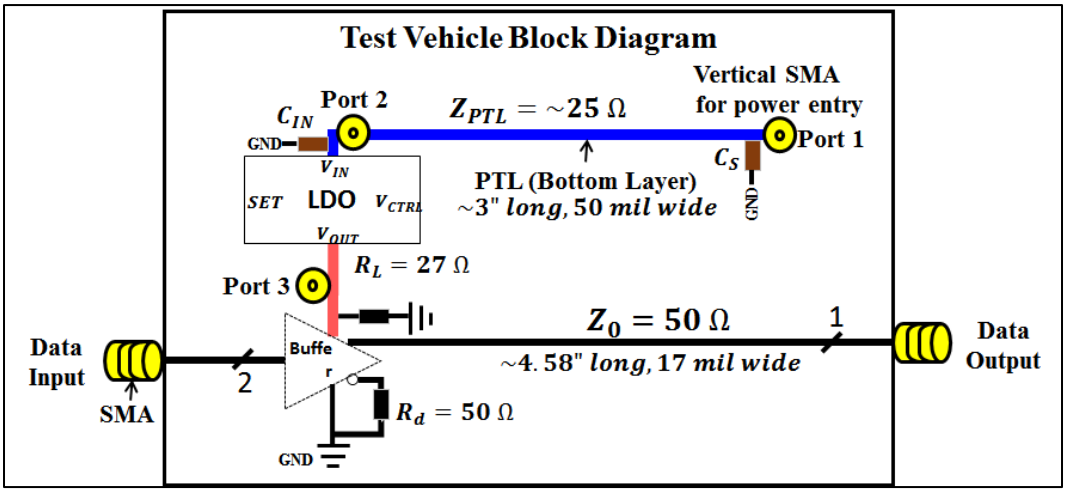


Figure 80 Schematic of PTL PCB showing the main components and ports

The V_{IN} pin in Figure 80 represents the LDO power input which was connected to the power delivery network. The V_{OUT} pin in Figure 80 represents the power output and was connected to power various loads including high speed buffers and a 27 Ω resistor, R_L, as shown in Figure 80. The V_{CTRL} pin in Figure 80 was decoupled using a 4.7 µF capacitor (not shown). The SET pin was connected to a resistor and bypassed by a capacitor (not shown) and used to ensure the output was set to ~2.5 V. Port 1, was bypassed using a 0603 1uF capacitor, which was used for connecting to the external power supply source.

Differential buffers were used as pseudo single ended transmitters, as detailed in Chapter 3.

5.7 Power Supply Rejection (PSR) Measurement

Figure 81 shows the test setup used for measuring the PSR of the LDO chip. A signal generator was used as a noise source to generate a sinusoid. Its output was connected to the input of a 1:2 splitter. One output of the splitter was monitored using an oscilloscope. The other output was connected to the RF port of a 3-port Bias-Tee module, as shown in Figure 81. The DC port of the Bias-Tee was connected to an external power supply to bias the V_{IN} pin of the LDO. The output of the Bias-Tee, which was the sum of the RF and DC inputs was then fed into the LDO input.

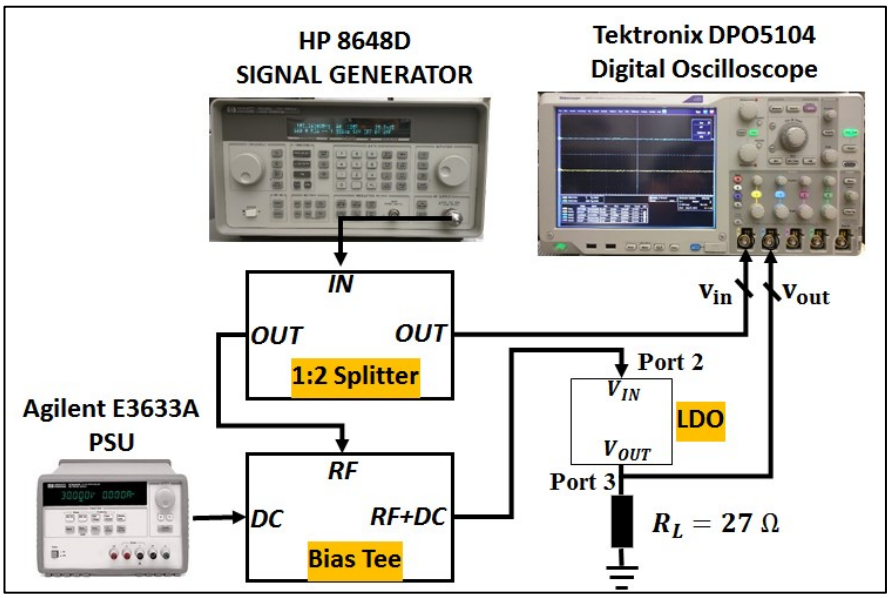


Figure 81 Measurement Setup for PSR measurement

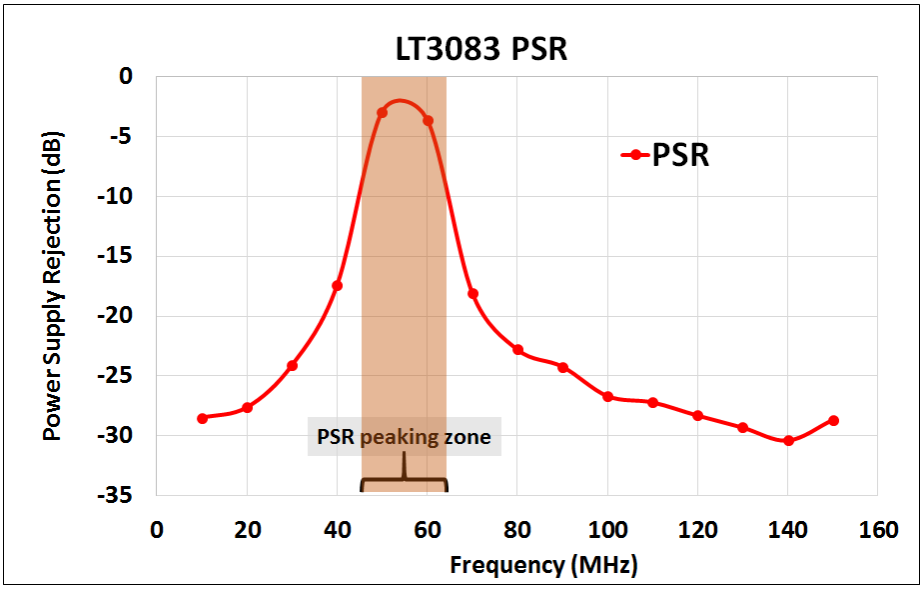
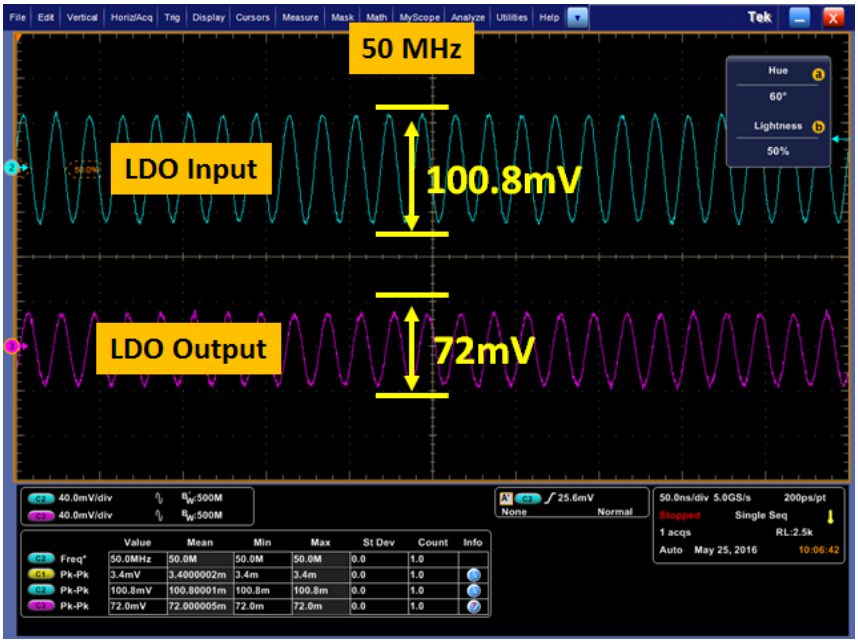


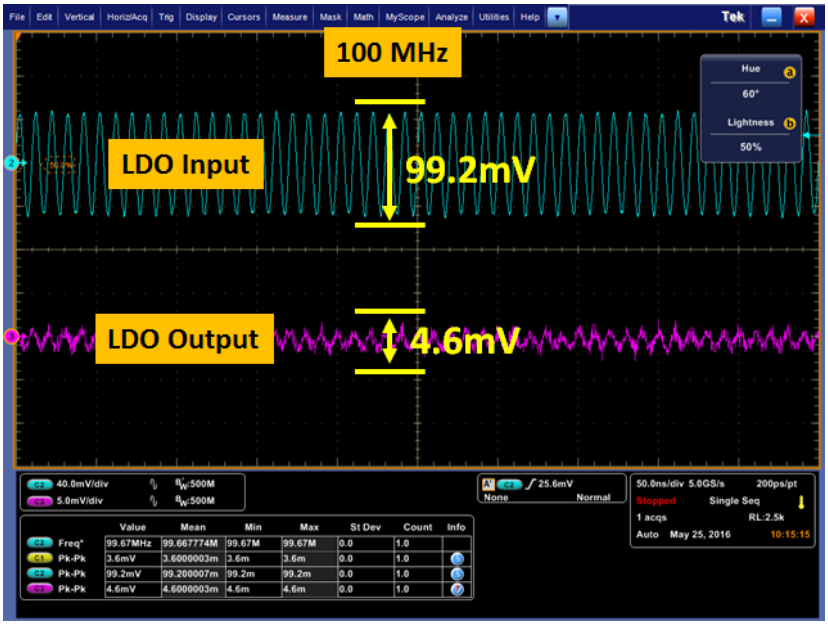
Figure 82 Measured power supply rejection of LT3083 LDO Chip.

The LDO output voltage was set to 2.5 V while driving a 27 Ω resistor. Therefore, the load current was ~100 mA. As the frequency of the input sinusoid was varied from 10 MHz to 150 MHz with 10 MHz increment, the amplitude of the AC noise at the LDO output (v_{OUT}) was measured. The ratio of noise to ac input voltage ($v_{in} = 100$ mV) was used to obtain the PSR as a function of frequency, similar to (3). The PSR plot is shown in Figure 82. As can be seen, the PSR of the LDO peaks in the region centered around 50 MHz, similar to Figure 74.

A comparison of the input and output waveforms at 50 MHz, and the waveforms at 100MHz is shown in Figure 83a and Figure 83b, respectively. At 50 MHz, where PSR peaked, there are about 70% of input noise coupled into the output. The PSR rejection was only about -3dB which correlated well with data shown in figure 77. At 100 MHz, where the LDO has strong noise rejection, a mere ~5% of noise was let through from the LDO input.



(a)



(b)

Figure 83 Power Supply Rejection Demonstration for a) 50MHz and b) 100MHz

5.8 Power Supply Noise (PSN) Measurement Results

In this section we compare the power integrity for the three boards under different load conditions.

5.8.1 PSN under static load

The impedance profile of the PDN for the three test vehicles were measured at port 1 and 2 using an Agilent® E8363B network analyzer. The test setup and measurement results are shown in Figure 84. An impedance peak at ~100 MHz for both PG and GP PCBs at port 2 near the LDO chip can be seen, while this occurs at ~150 MHz for the PTL PCB.

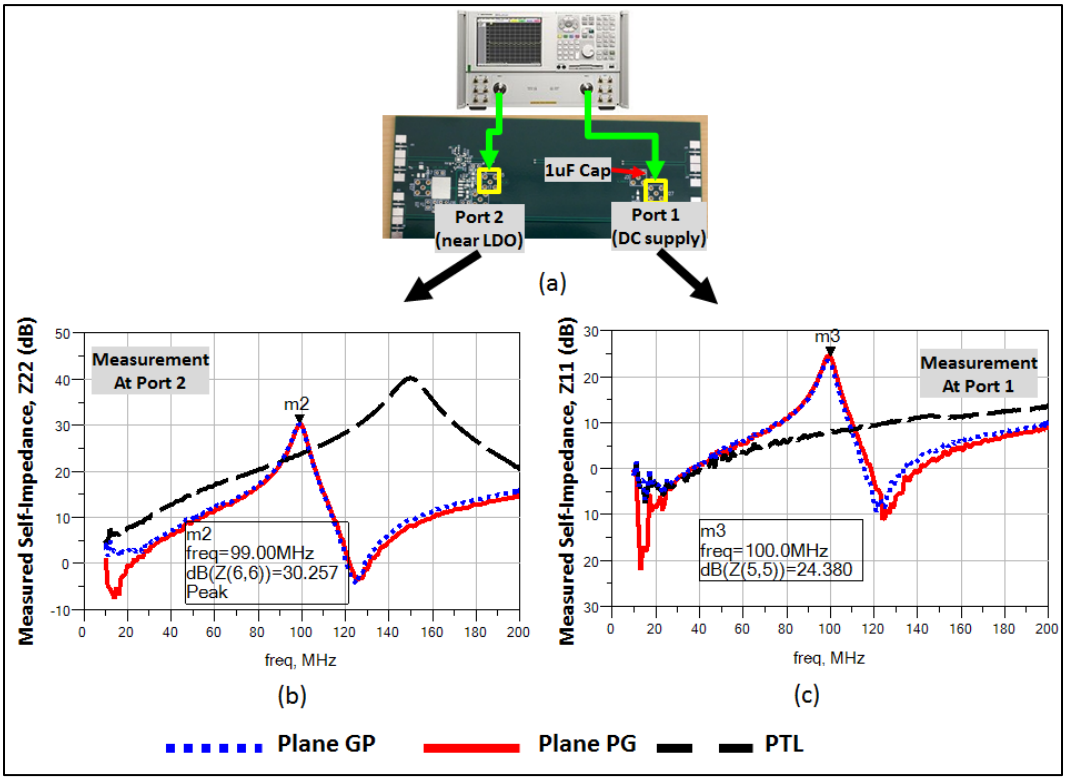


Figure 84 The S-parameter setup (a), impedance measurement at LDO location, port 2 (b), and at the DC supply port 1 (c).

For each test vehicle, an AC noise source was injected into port 1 with a ~100mV sinusoid in the same aforementioned frequency range. The measured power supply noise at the LDO chip output for the plane and PTL PCBs are shown in Figure 85. We observe two noticeable noise surges at around 50MHz and 100MHz region for GP and PG PCBs. The peaking at 100MHz is due to the high self-impedance (Figure 84), while though the impedance peaked at 150MHz at port 2 for the PTL PCB, the impedance at port 1 is relatively low. Therefore, less noise appears at port 2 after propagating through the PTL. Since the LDO chip has good PSR at 150 MHz, the impedance peak at 150MHz is not an issue. However, the second peaking at ~50 MHz for the plane PCBs is a concern due to the ineffectiveness of PSR of the LDO at ~50 MHz to reject it (Figure 82). This leads to larger noise at the LDO chip output.

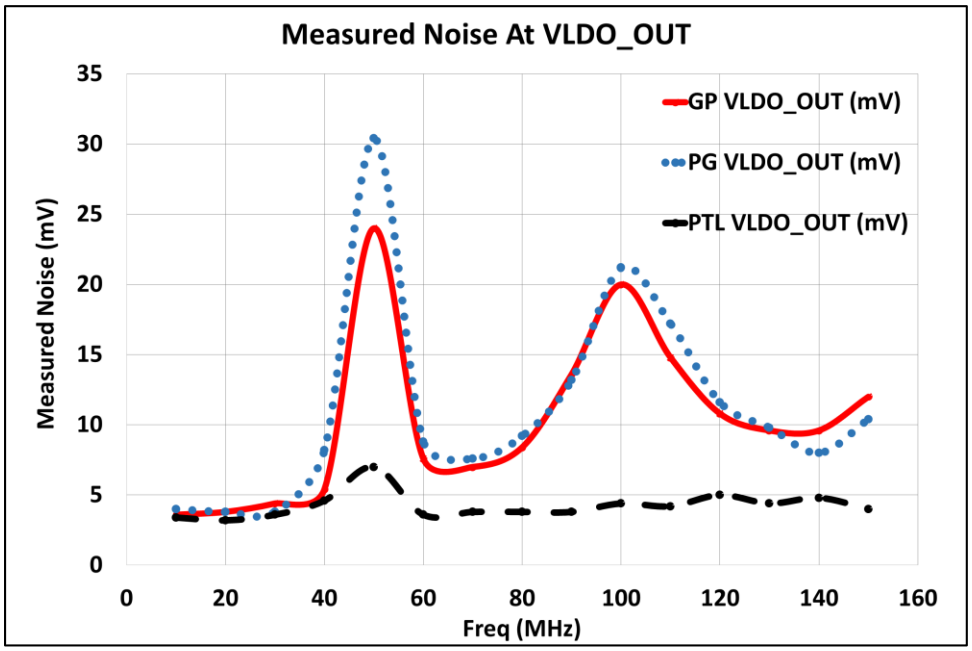


Figure 85 Measured noise at LDO output with ~100mV P-P noise source and frequency from 10MHz to 150MHz.

To bypass the 100MHz noise, a 1 nF capacitor was added near the LDO input pin. The self-impedance at port 2 near the LDO V_{IN} pin was re-measured and is shown in

Figure 86. The solid curve represents the self-impedance at port 2 for the plane PCBs before adding the 1nF decoupling capacitor. The dotted line represents the impedance after adding the capacitor. As can be seen, the peaking at 100MHz was effectively suppressed. However, an impedance peak at ~50 MHz was generated due to the parallel combination of the capacitor and the plane. To further exacerbate the issue, this high impedance lies within the PSR peaking region of the LDO (Figure 82).

Figure 87 shows the re-measured power supply noise at the LDO output after the addition of the 1 nF capacitor. The noise level at 100 MHz was successfully suppressed to below 5 mV peak-peak for the PG and GP PCBs as shown by the dotted line and solid line in Figure 87, respectively. Table 16 compares the measured PSN at the LDO output at 100 MHz showing that it has been reduced by over 76% for both plane PCBs after adding the capacitor (C_{IN}).

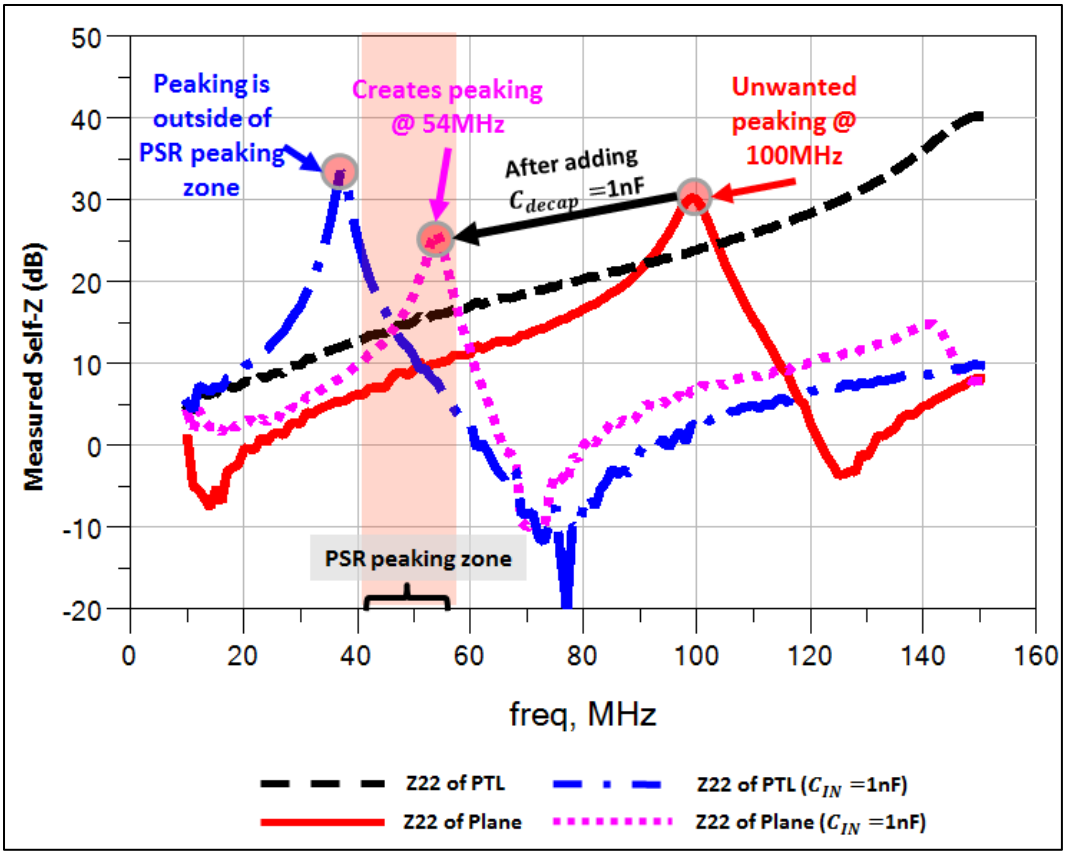


Figure 86 Measured self-impedance at port 2 near the LDO input after adding a 1nF decoupling capacitor at LDO V_IN pin

However, the measured noise due to a 50 MHz stimulus as shown in Table 17 showed little improvement in the LDO output noise for the plane designs. However, the measured noise was very low at around 5 mV for the PTL PCB as indicated by the dashed line in Figure 87. Table 17 shows that the PTL PCB offered significant reduction in PSN (over 80%) after adding C_{IN} as compared to the plane PCBs due to the lower impedance of the PDN at the LDO input. The peak at around 38MHz for the PTL PCB as indicated by the dash-dot line in

Figure 86 was out of the LDO PSR peaking region; and therefore, poses no issue to power integrity.

Table 16 Measured Power Supply Noise at LDO Output with 100 MHz Input Noise Source Before and After Adding C_IN

	PTL (mV)	GP (mV)	PG (mV)	Noise reduction over GP*	Noise reduction over PG*
No C_{IN}	4.4	20	21.2	78.0%	79.2%
$C_{IN} = 1\ nF$	3.4	4.8	3.8	29.2%	10.5%
Noise reduction†	22.7%	76.0%	82.1%	N/A	N/A

* The noise reduction in PTL as compared to the corresponding test vehicle.
† Comparing the noise before and after adding C_{IN}.

Table 17 Measured Power Supply Noise at LDO Output with 50 MHz Input Noise Source at LDO Input Before and After Adding C_IN

	PTL (mV)	GP (mV)	PG (mV)	Noise reduction over GP*	Noise reduction over PG*
No C_{IN}	7.0	24.0	30.4	70.8%	77.0%
$C_{IN} = 1\ nF$	4.6	27.2	29.6	83.1%	84.5%
Noise reduction†	34.3%	-13.3%	2.6%	N/A	N/A

* The noise reduction in PTL as compared to the corresponding test vehicle.
† Comparing the noise before and after adding C_{IN}.

5.8.2 Measurement under active load

In this section, the 27 Ω load resistor (R_L) was deactivated. Instead, the high speed buffer was utilized and was driven by a clock signal to create a dynamic load for the LDO, as shown in Figure 80. The input and output signal ports of the buffer are marked in Figure

80 and Figure 79. The signaling method used at the output was pseudo single ended signaling, as described in Chapter 3. The output trace had four via transitions through the entire PCB. A 50 MHz clock signal was sent from a signal generator (Agilent 81133A) to the buffer. The spectrum of the power supply noise at the LDO chip output for the PTL PCB is shown in Figure 88. The measured noise power was -57.42 dBm at 50MHz. The noise power spectrum of the GP PCB was ~6 dB higher than the PTL PCB (-43.79 dBm), as shown in Figure 89a. The PG PCB had a much higher noise power at -14.98 dBm, as shown in Figure 89b, which was in part due to the additional return path discontinuities at the SMA edge connectors on the input and output, as demonstrated in Chapter 4.

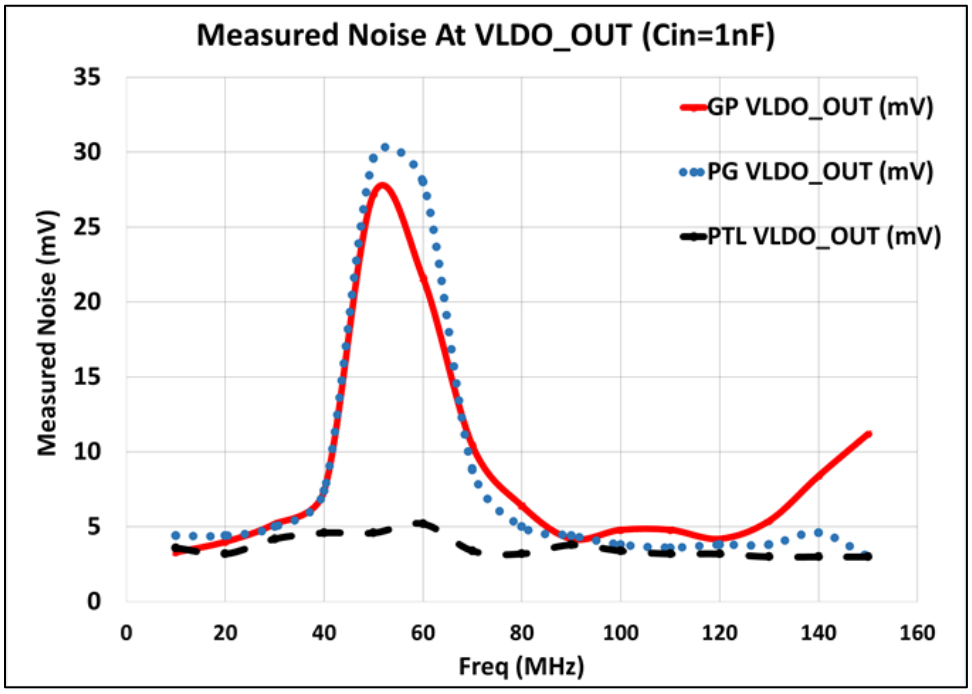


Figure 87 Measured noise at LDO output when noise source is ~100mV P-P with frequency from 10MHz to 150MHz and Cin is 1nF.

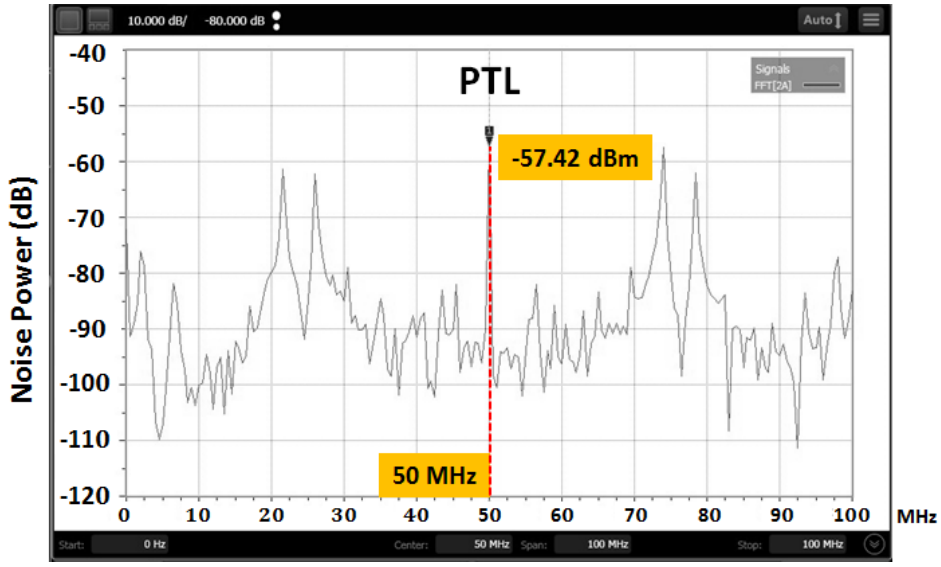
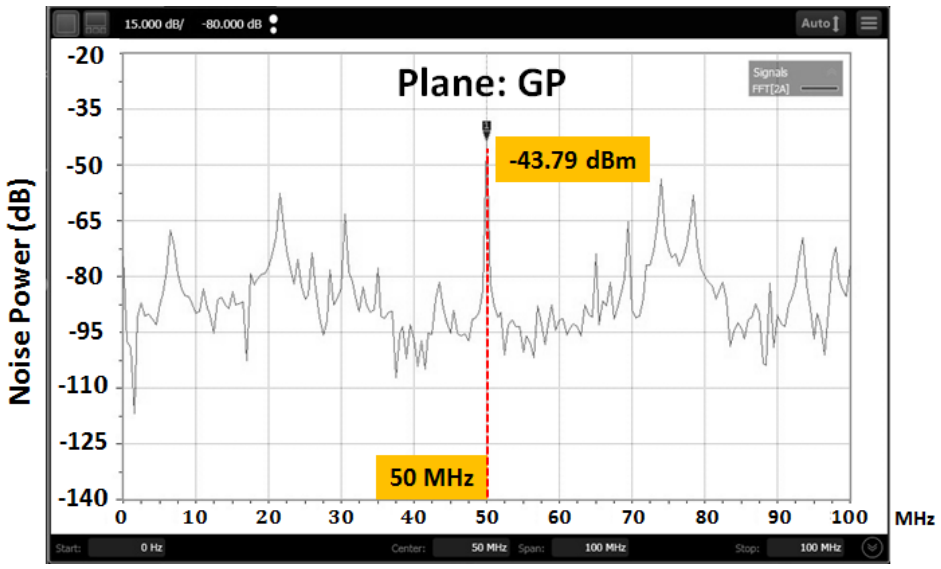


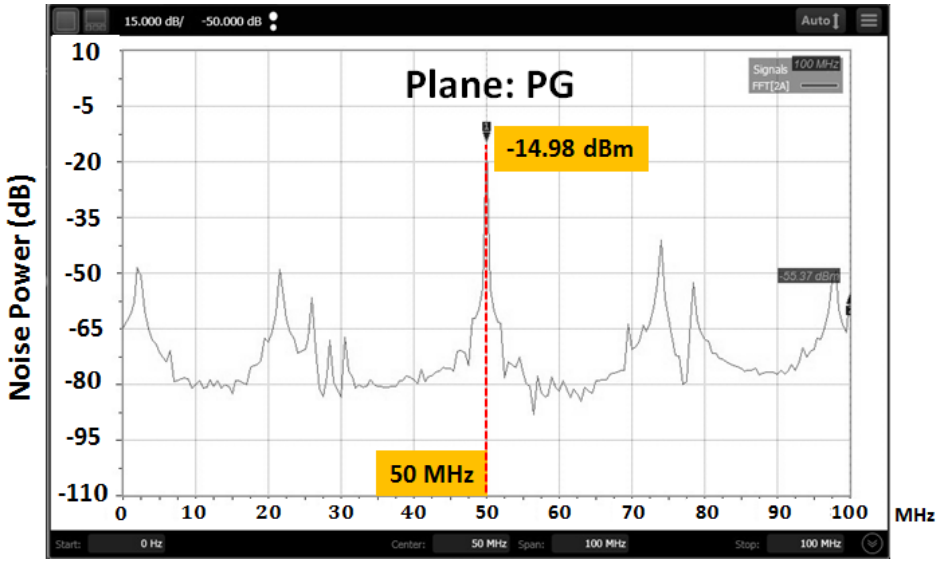
Figure 88 Measured power supply noise spectrum due to 50 MHz clock excitation at the LDO output (PTL PCB).

5.9 **Summary**

Typical LDO circuits exhibit PSR peaking effect that falls in the 40-100MHz range, a frequency range where most of the chip-package and PCB anti-resonances occur. This limits the bandwidth of the LDO circuit to control power supply noise. Improving the PSR can often result in decrease in energy efficiency. In this chapter, we demonstrated a method where the power supply noise and efficiency of the LDO circuits can be improved by co-design of the PDN and LDO circuit. We showed through simulations that by using power transmission lines in the PDN, both the power supply noise and efficiency can be improved by ~98% and 12.1% respectively, as compared to more conventional designs using voltage-ground planes. These results were validated through measurements on test vehicles using COTS components, where improvement of ~80% in power supply noise were observed as compared to more traditional plane based design approaches.



(a)



(b)

Figure 89 Measured power supply noise spectrum due to 50 MHz clock excitation at the LDO output for a) PCB-GP and b) PCB-PG design.

CHAPTER 6. FUTURE WORK

6.1 Demonstration of Electromagnetic Compatibility (EMC) and Electromagnetic Immunity (EMI) advantage of PTL based designs

Electromagnetic (EM) radiation has been a long standing issue facing electronics manufacturers especially in high speed digital I/O circuits. The vendors need to ensure their products meet both EMI and EMC requirement set forth by Federal Communication Commission (FCC). It was also shown that cyber attackers have also taken advantage of such EM emission from electronics such as personal computers or other mobile devices eavesdrop on their victims [96][97]. Method for finding frequency modulated and amplitude modulated EM radiation was also shown in [98]. Power transmission line based designs were demonstrated to show better EM isolation between signal and power distribution network even in the case where a signal line makes several via-transitions through a PCB board. The EM coupling advantage was demonstrated within PCBs. Next, near and far field EMI and EMC measurement and analysis should be conducted to exam how PTL based designs perform as compared to plane based.

6.2 Implementation of PTL with LDO in a System on Chip (SoC)

To improve both power efficiency and fine grained voltage regulation, the recent trend is to move towards fully integrated voltage regulators (FIVR) to supply both the core and I/O circuits for System on Chip (SOC) applications. PTL and LDO were demonstrated to enhance the power supply noise rejection bandwidth of an LDO while improving overall energy conversion efficiency by using a COTS LDO on a PCB. A fully integrated package level design to include a VRM and a LDO joined by PTL should be explored next, as shown in Figure 90. In Figure 90, the LDO and VRM are both solder-bumped to the substrate.

Although Figure 90 is similar to Figure 4, the power plane was removed. Instead, the PTL is used as an interconnect between the VRM and the LDO. Embedded passives such as capacitors and/or inductors can also be implemented to improve integration density, as shown in Figure 90.

Due to the smaller size of a package as compared to a PCB, the frequency range of interest would in the gigahertz range. The width of the PTL can also be forced to be narrower in a package design as compared to a PCB design. Therefore, the length of the PTL needs to be carefully designed to maintain acceptable DC resistance to avoid excessive DC voltage drop across the length of the PTL.

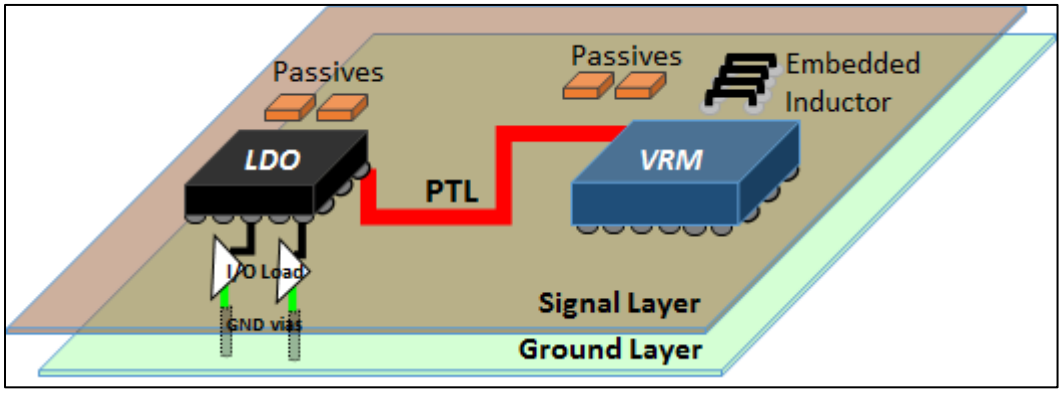


Figure 90 Fully integrated voltage regulator to include a VRM and an LDO joined by a PTL for an SoC system

6.3 System Level CC-PTL Implementation

CC-PTL design scheme provides the advantage of superior signal and power integrity performance margin at gigabit rate speed [44], [45] and [63]. The remaining area to improve is the overall power consumption of CC-PTL. One major power consumer can

be attributed to the use of the complementary path to keep the PTL constantly charged to minimize its current transient. The idea of system level CC-PTL or CC-PTL-S is to investigate ways by which a complementary path (CP) can be controlled; either enabled or disabled, by control logic based on power supply noise (PSN) level. If the PSN is low, multiple CPs can be turned off to reduce power consumption. When the PSN rises above a certain preset threshold, the control logic can turn on CPs discretely until the PSN drops below a low-level threshold. The control logic can be implemented with a FPGA or Analog to Digital converter (ADC). Figure 91 illustrates the CC-PTL-S design concept.

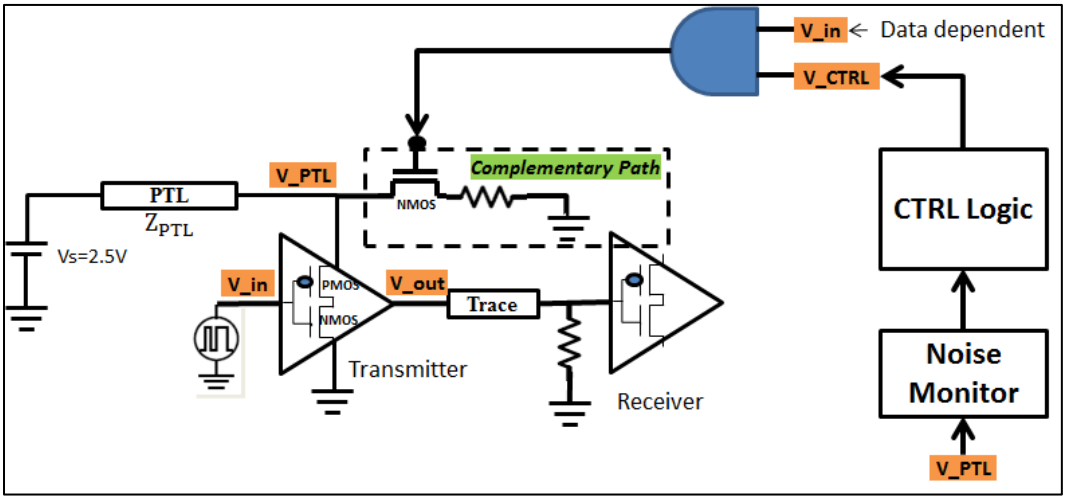


Figure 91 System level CC-PTL concept

A passive noise detection circuit (NDC) was created by using an NMOS switch which serves two purposes by utilizing a feedback loop. The first purpose is to detect power supply noise on the PTL. When the noise level exceeds its threshold voltage, the NDC will be triggered and serves its second function which is to either inject or sink current from the

PTL to compensate for the current transient. Figure 92 shows the block diagram of the conceptual design. As can be seen, multiple drivers are being supplied by a single PTL without a complementary path, as shown in Figure 16a.

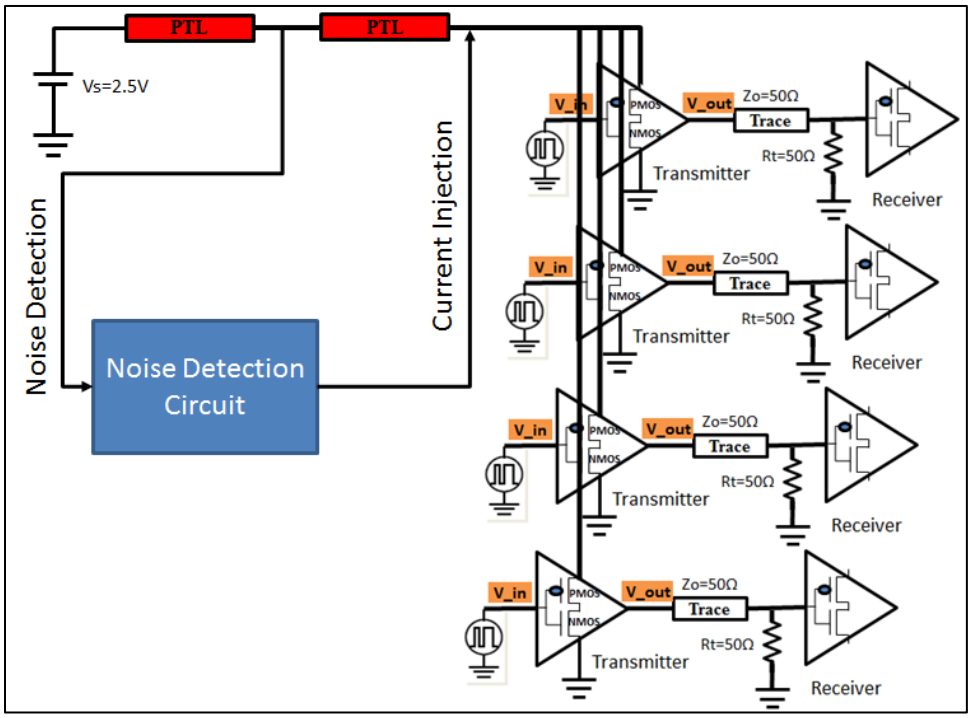


Figure 92 Block diagram of a CC-PTL-S implementation

Figure 93 shows the simulated result of the noise detection part of NDC. The top shaded portion of the plot shows the noise levels at discrete time for every 1 msec. As can be seen, when the noise level exceeds the threshold above 1.2 Volt, the compensation mechanism is triggered, as shown in the bottom portion of the plot.

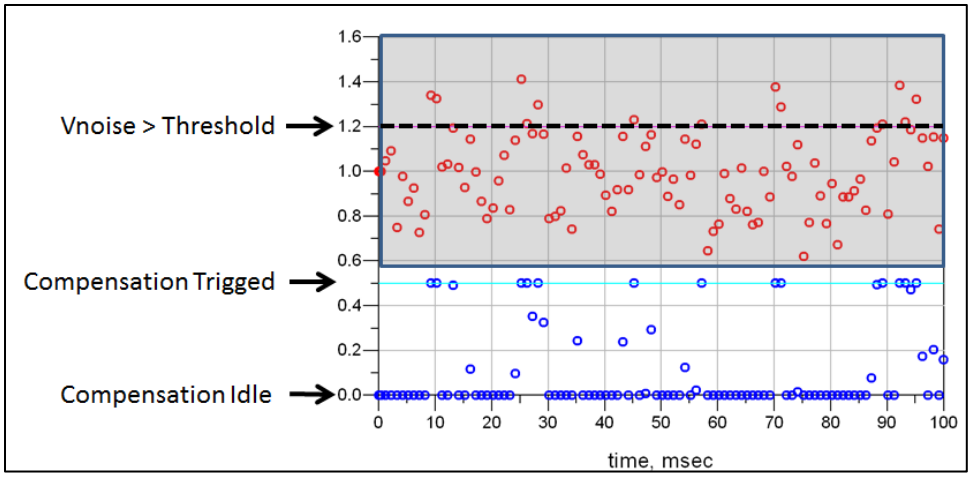


Figure 93 Noise detection circuit simulation results

Figure 94 shows a schematic of an inverter acting as a transmitter without any current compensated circuit powered by PTL. It is combined with the passive NDC. The NDC detect noise on the PTL close to the transmitter (TX) at location "a", as shown in Figure 94. The compensation current is injected into location "b", as shown in Figure 94, where the PTL connects to the inverter supply node.

Figure 95 shows the simulated noise when PRBS data was being transmitted from the TX at 1 Gbps at the input of the TX.

Figure 95a shows the p-p noise of 2 V without any compensation method.

Figure 95b shows the p-p noise of 0.83 V with the CC-PTL-S approach. The noise reduction is 58.5 %. The absolute noise levels can be reduced by reducing voltage swing of the transmitter. In term of energy, the CC-PTL-S consumed 158.2 pJ as compared to 900 pJ for the regular CC-PTL case, which was an energy saving of over 82.4%.

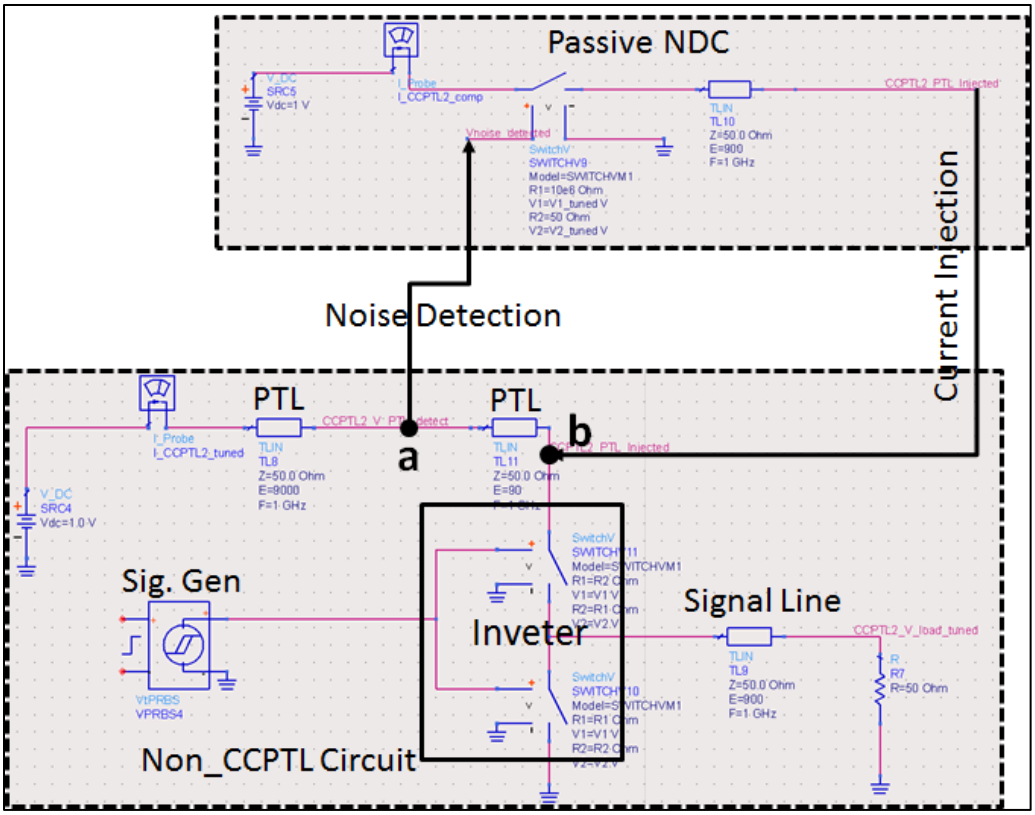


Figure 94 Schematic of noise detection circuit with non-CC circuit

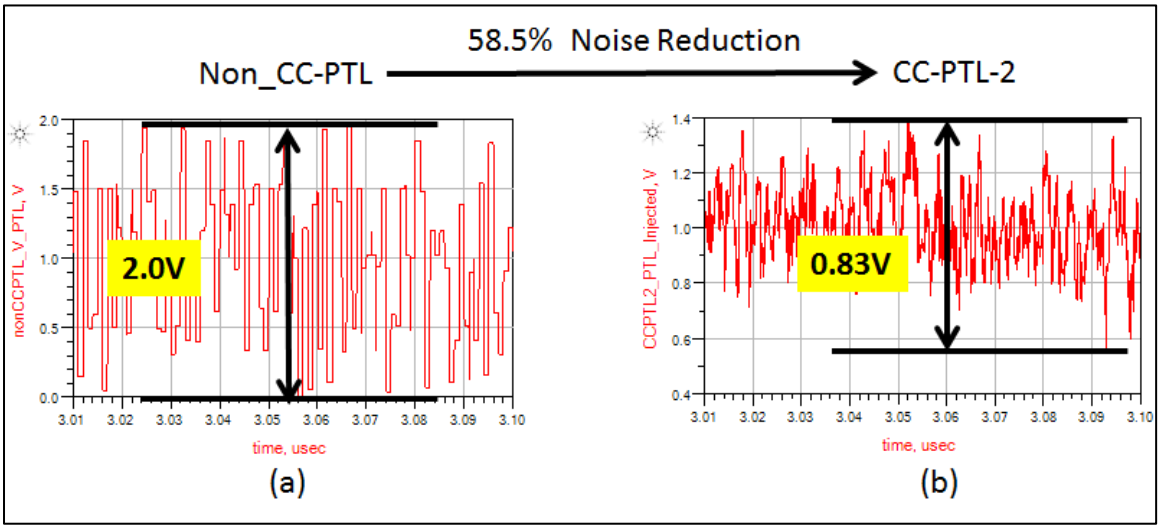


Figure 95 Power supply noise comparison between non_CC-PTL (a) and CC-PTL-2 (b).

CHAPTER 7. CONCLUSION and PUBLISHED WORK

7.1 Conclusion

The past work on PTL focused on proof of theory through simulation and proof of concept by designing simple test vehicles. The effect of return path discontinuities (RPD) on signal and power integrity was only indirectly shown by measuring eye diagrams. Furthermore, when compared to PTL based designs, the plane based designs often were designed with signals referenced to a voltage plane instead of to ground planes.

In this research, the application of PTL in advanced and complex systems was demonstrated and shown through proof of concept PCB test vehicles. By incorporating multiple high speed drivers in the system, the simultaneous switching noise (SSN) could be measured and compared with non-SSN scenarios. Furthermore, several other scenarios that are common in data transmission were also demonstrated using the test systems by stacking four PCBs on top of each other. These scenarios include high speed board to board communication through daisy-chain and multiple driver switching.

The co-design of the PTL and LDO was also presented to address the limited bandwidth of LDO due to power supply rejection peaking, without sacrificing energy conversion efficiency. The methodology to design a PTL to create a low impedance null at where the PSR peaks while minimizing DC power loss due to the DC resistance of the PTL was outlined in chapter 5.

To dive deeper into the advantage of reduction of RPD by using PTLs, electromagnetic coupling between signal and power distribution networks were closely examined in cases such as microstrip line signals and via-transitioning signal lines. The PTL design was also compared with voltage-ground plane cases that had both voltage plane

and ground plane referenced stack-ups for the signal lines. The coupling coefficient was also correlated with the magnitude of coupled noise through measurement on various test vehicles in both time and frequency domains.

The contribution of this research was summarized in Chapter 1. The following section lists all the publications and technical presentation as the outcome of this research effort.

7.2 Publication and Presentation

7.2.1 Journals

- D. Zhang; M. Swaminathan; A. Raychowdhury and D. Keezer, "Enhancing the Bandwidth of Low-Dropout (LD) Regulators Using Power Transmission Lines for High Speed I/Os," submitted to IEEE Trans. Compon., Packag., Manuf. Technol., Sep. 2016.
- D.C. Zhang, M. Swaminathan, and D. Keezer, "Application of a New Power Distribution Scheme for Complex Printed Circuit Boards for High Speed Signaling," IEEE Trans. Compon., Packag., Manuf. Technol., vol. 5, iss. 6, pp. 806-817, 2015.
- S. Telikepalli, D. C. Zhang; M. Swaminathan; D. Keezer, "Constant Voltage-Based Power Delivery Scheme for 3-D ICs and Interposers," Components, Packaging and Manufacturing Technology, IEEE Transactions on, vol.3, no.11, pp.1907-1916, Nov 2013

7.2.2 Conferences

- D. C. Zhang; M. Swaminathan; D. Keezer, “Effect of via-transitions on signal integrity using power transmission lines,” 2016 IEEE 20th Workshop on Signal and Power Integrity (SPI), pp. 1-4, May 8-11, 2016.
- D. C. Zhang; M. Swaminathan; D. Keezer, “Reduction of PDN induced coupling into signal lines using PTL power distribution,” Electrical Performance of Electronic Packaging and Systems (EPEPS), 2015 IEEE 24th, pp. 117-120, Oct. 25-28, 2015. **Best Poster Paper Award**
- D. C. Zhang; M. Swaminathan; D. Keezer; S. Telikepalli, "Characterization of alternate power distribution methods for 3D integration," Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th, vol., no., pp.2260,2265, 27-30 May 2014
- D. C. Zhang; M. Swaminathan; S. Huh, "New power delivery scheme for 3D ICs to minimize simultaneous switching noise for high speed I/Os," Electrical Performance of Electronic Packaging and Systems (EPEPS), 2012 IEEE 21st Conference on, pg. 87-90, 2012.
- S. Müller, D. C. Zhang, M. Swaminathan, “Verringerung der Abstrahlung von Leiterplatten durch optimierte leitungsbasierte Spannungsversorgung,” International Exhibition and Conference on Electromagnetic Compatibility EMV Düsseldorf conference, Germany, 2015.

7.2.3 Technical paper and presentation

- D. Zhang; S. Telikepalli; S. Huh; M. Swaminathan, “New Power Delivery Scheme for 3D ICs to Minimize Simultaneous Switching Noise in High Speed Digital

I/Os,"3rd Annual Global Interposer Technology (GIT) Workshop, Atlanta, GA, 2013.

- D. Zhang; M. Swaminathan; D. Keezer, "A Novel Power Delivery Network Based Design to Improve Signal and Power Integrities in 3D IC Systems from Concept to Prototype," 4th Annual Global Interposer Technology (GIT) Workshop, Atlanta, GA, 2014.
- D. Zhang; M. Swaminathan; D. Keezer, "Wideband Reduction of Cross Coupling between High Speed Signal Lines and Power Distribution Network Through the Use of Power Transmission Line Based Design," Center for Co-design of Chip, Package, Systems (C3PS) Workshop, Atlanta, GA, May 26, 2015.
- D. Zhang; M. Swaminathan; D. Keezer, "Power Transmission Lines to Reduce Coupling between High Speed Signal Lines and PDN," Power Delivery for Electronic Systems (PDES) Consortium, Center for Co-design of Chip, Package, Systems (C3PS), Atlanta, GA, May 27, 2015.

7.2.4 Invention Disclosure

- David Zhang; Madhavan Swaminathan and Arijit Raychowdhury, "Enhancing The Bandwidth of Low-Dropout (LDO) Regulators and Improving System Level Energy Conversion Efficiency By Co-Designing Power Transmission Lines With LDO," Invention Disclosure ID: 7395, Sep. 2016, Provisional Patent Application filed by Georgia Tech.

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