ELECTROMAGNETIC MODELING OF INTERCONNECTIONS IN THREE-DIMENSIONAL INTEGRATION

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ELECTROMAGNETIC MODELING OF INTERCONNECTIONS IN THREE-DIMENSIONAL INTEGRATION

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To my family

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SUMMARY

As the convergence of multiple functions in a single electronic device drives current electronic trends, the need for increasing integration density is becoming more emphasized than in the past. To keep up with the industrial need and realize the new system integration law, three-dimensional (3-D) integration called System-on-Package (SoP) is becoming necessary. However, the commercialization of 3-D integration should overcome several technical barriers, one of which is the difficulty for the electrical design of interconnections. The 3-D interconnection design is difficult because of the modeling challenge of electrical coupling from the complicated structures of a large number of interconnections. In addition, mixed-signal design requires broadband modeling, which covers a large frequency spectrum for integrated microsystems. By using currently available methods, the electrical modeling of 3-D interconnections can be a very challenging task.

This dissertation proposes a new method for constructing a broadband model of a large number of 3-D interconnections. The basic idea to address the many interconnections is using modal basis functions that capture electrical effects in interconnections. Since the use of global modal basis functions alleviates the need for discretization process of the interconnection structure, the computational cost is reduced considerably. The resultant interconnection model is a $RLGC$ model that describes the broadband electrical behavior including losses and couplings. The smaller number of basis functions makes the interconnection model simpler, and therefore allows the generation of network parameters at reduced computational cost. Focusing on the modeling of bonding wires in stacked ICs and through-silicon via (TSV) interconnections, this research validates the interconnection modeling approach using several examples from 3-D full-wave EM simulation results.

CHAPTER 1

INTRODUCTION

During the current and the next decade, a leading trend of electronics is to increase the integration density by using package-based three-dimensional (3-D) integration. Currently, 3-D integration is realized by stacking integrated circuit (IC) dies, which communicate with other submodules through vertical 3-D interconnections. Thus, 3-D interconnection is a key factor that enables 3-D integration for achieving the desired performance.

However, 3-D interconnection design requires engineering solutions to issues that were not observed earlier in planar interconnection design. Compared to 2-D design, 3-D interconnections have more degrees of freedom for wiring, so the resultant geometric complexity makes the estimation of electrical performance more difficult. Furthermore, the increased wiring density of 3-D integration needs the characterization of a large number of interconnections. For such 3-D designs, current commercial modeling tools have limitations in their application to real designs.

To minimize the design cycle time of 3-D integration, significant progress in computer-aided design (CAD) tools is mandatory. The desired 3-D CAD tools should be supported by accurate electrical modeling of 3-D vertical interconnections to facilitate complicated schematic design, routing, and physical layout along with maintaining improved electrical characteristics. In order to respond to the industry need for new 3-D CAD tools, this research focuses on the development of efficient and accurate electrical modeling methods for 3-D interconnections.

As an introductory discussion, this chapter presents the basic background of the research in this dissertation. Section 1.1 overviews the current technology trend and emphasizes the need for 3-D integration technology. Section 1.2 focuses on the interconnections used in 3-D integration, followed by Section 1.3 that discusses modeling

issues in the design of 3-D interconnections. To check the availability of the existing methods for 3-D modeling, Section 1.4 surveys and discusses previous approaches for interconnection modeling and simulation. After clarifying the limitations of the current methods, the last two sections introduce the proposed research in this dissertation.

1.1 Need for 3-D Technology in System Integration

Improving computational speed and data bandwidth is the main purpose of modern electronics, which realizes the progress by increasing the level of transistor integration density in semiconductor technology [10, 11]. The growth of the integration technology has been driven by silicon-based technology, covering from the development of integrated circuits (IC) to system-on-chip (SoC). Currently, a typical SoC is targeting the capability for miniaturization of a computing unit, including a microprocessor, memory blocks, timing circuits, and various interfaces [12].

Although silicon technology supports subsystem integration, the extension of the functionality with SoC is limited, especially when the application is in multimedia mobile devices. In addition to digital computing units, integrated systems should contain various subsystems including analog, radio frequency (RF), optic, and sensor submodules. Furthermore, SoC has difficulty in system design flexibility that satisfies the rapidly increasing variety of multimedia mobile applications.

The challenges of multi-functional integration in today's mobile applications can be overcome by using package-based system integration. Since advanced packaging technology enables combining submodules with various substrate materials in a single package platform, the realization of the multi-functional system can be much easier than silicon-based technology. With the progress in processing technology, package-based system component density will increase, as estimated in Figure 1 [1].

For the realization of the new system integration law, a key issue is the design

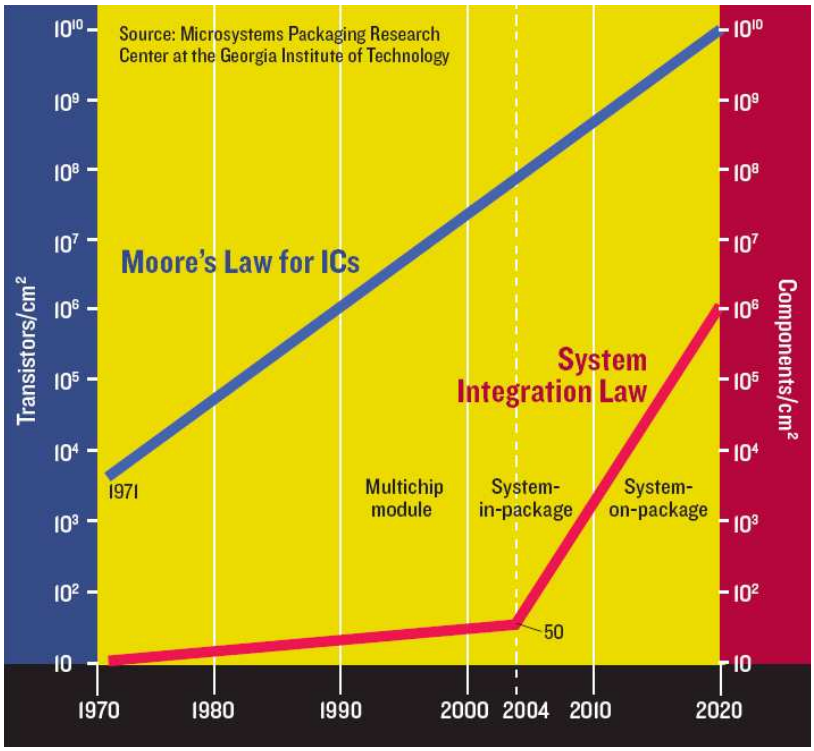


Figure 1. An estimate of system integration density driven by package-based technology [1].

of an efficient packaging architecture that minimizes packaging space and maintains required functions. A common idea underlying many of the new packaging solutions is utilizing 3-D space, instead of mounting chips on the planar substrate layout as in the traditional multi-chip modules (MCM). Currently, the 3-D packaging concept is realized through System-in-Package (SiP), which stacks bare or packaged ICs vertically. A more extensive architecture of 3-D integration is System-on-Package (SoP), which covers SiP as well as embedded passive and active components in a package. For microminiaturization, 3-D technology is the fundamental method being pursed for today's package-based system integration [2].

1.2 Interconnection Elements in 3-D Integration

In 3-D integration or SiP, the communication among the stacked ICs and embedded components requires vertical interconnections. Since processing the vertical interconnections is challenging compared to the planar ones, the electrical and mechanical characteristics of the vertical interconnections can be a bottleneck for achieving the required system performance. Thus, various types of vertical interconnections are still being proposed.

Several interconnection elements are already popular in industry. Figure 2 shows typical SiP structures with three types of interconnections, including bonding wires, via interconnections, and metal bumps. Among them, bonding wire interconnections have been used most widely because their processing is mature and cost effective. To improve electrical performance, via interconnections are becoming a major choice to replace the bonding wires. In 3-D integration, the trend of using via interconnections is realized as through-silicon via (TSV) interconnections by employing silicon as a new packaging substrate, which increase the integration density considerably. This section briefly discusses the main features of vertical interconnections, focusing on bonding wires and TSV interconnections.

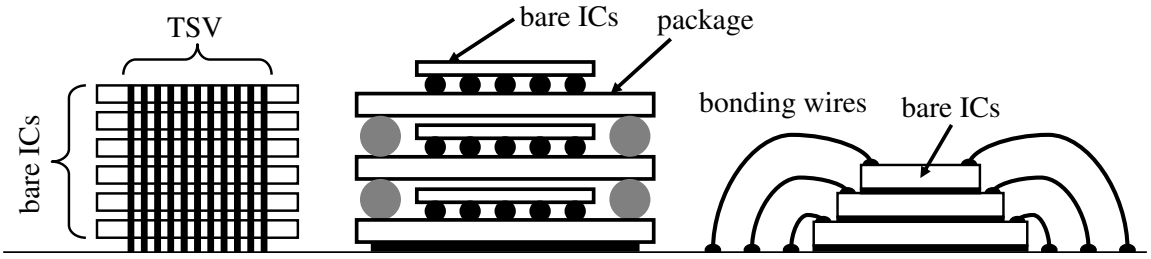


Figure 2. Examples of SiP structures with interconnection elements [2].

1.2.1 Bonding Wire Interconnections

Since the original beam lead technology of AT&T, bonding wires have been the preferable technology for chip-to-package interconnections because of their high flexibility, high reliability, and low defect rates [13]. The application of bonding wires to 3-D

integration was proposed in late 1990's [14], and the bonding wire technology is still evolving with increasing levels of integration, as shown in Figure 3. A method for increasing density is to reduce the wire pitch, which is currently about 60 μm [15].

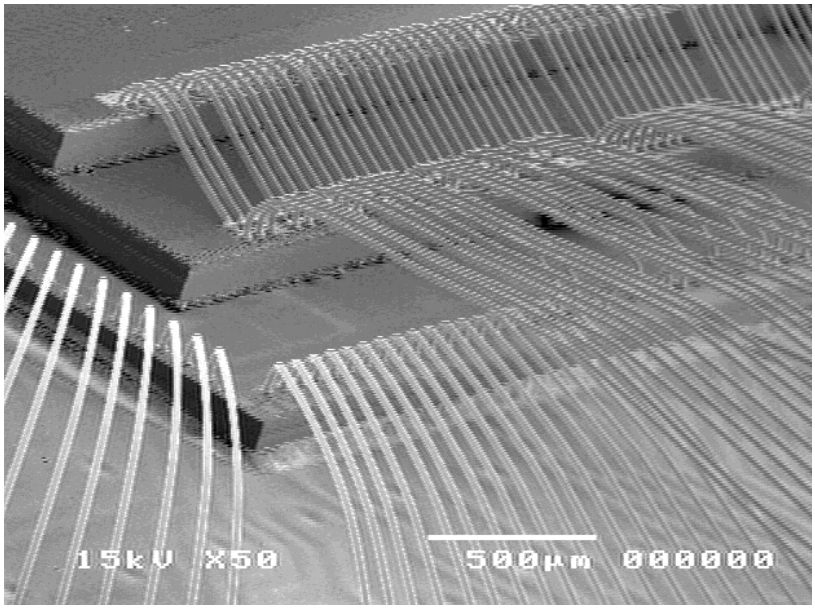


Figure 3. An example of 3-D bonding wire bond integration. (Photo courtesy of Amkor Technology, Inc.)

In spite of the popularity in industry, its long interconnection length limits the use of bonding wires in high-speed applications. Using bonding wires for chip-to-chip interconnections is difficult when chips are stacked, and improving the integration density is also limited because bonding wires are located only on the periphery of chips. In addition, the electrical coupling among wires is difficult to predict because their geometric configurations are very complicated, especially when using bonding wires in 3-D stacked ICs. The uncertainty of the horizontal and vertical coupling levels obstructs reliable design since it impacts signal and power integrity. To make matters worse, the complicated crossing of bonding wires can result in unexpected electrical short circuits with nearby interconnections [16].

1.2.2 Through-Silicon Via (TSV) Interconnections

Originally, via-type interconnections have been fabricated to connect planar interconnections in a multilayered printed circuit board (PCB). The vertical interconnections for the PCB design are called though-hole via (THV) interconnections. Since via interconnections can reduce the interconnection length for inter-chip communication, they can be an alternative to the bonding wire technology. Therefore, new applications of via interconnections to stacked IC packaging designs have been proposed [17] since the 1990s.

In addition to the reduced interconnection length, integration density can be enhanced by fabricating via interconnections in silicon substrate [18]. Thus, via interconnections in SiP and SoP are usually fabricated in silicon substrate, and they are called though-silicon via (TSV) interconnections. Currently, the main issue regarding TSV interconnections is the fabrication process [19, 20, 21], but TSVs are beginning to be used in stacked memory chip applications [22]. An example of TSV array is shown in Figure 4.

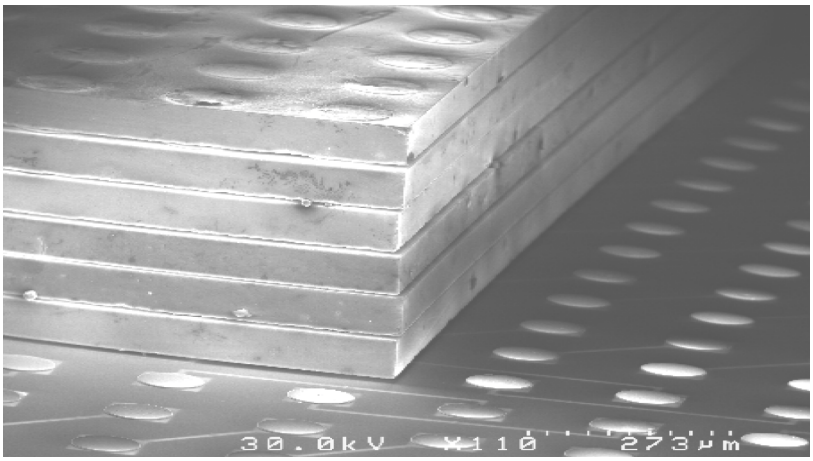


Figure 4. An example of fabricated TSV array [3].

Along with fabrication challenges, the electrical design of TSV interconnections is another major challenge due to their complicated electrical behavior. The main electrical bottleneck is coupling from lossy silicon substrates, especially when using

highly-doped silicon. Substrate coupling and leakage current may generate considerable insertion loss that degrades signal integrity. To avoid high insertion loss and coupling, electrical designers should control several parameters such as silicon resistivity, oxide thickness, and the pitch between interconnections [5]. In addition, an external bias voltage can modify the depletion region in the silicon substrate, resulting in the variance of effective capacitance between TSVs [23].

1.3 Electrical Modeling Issues in 3-D Interconnection Design

As discussed in the previous section, bonding wire and TSV interconnections are popular choices for 3-D integration design, but their undesirable electrical properties motivates more careful design considerations. The estimation of the electrical behaviors of 3-D interconnections is challenging since the electrical model of 3-D interconnections is very difficult to extract. Consequently, the increased design uncertainty retards the design and production cycles.

A major difficulty in modeling 3-D interconnections comes from the need to obtain the entire coupling model of a large number of 3-D interconnections. In a typical SiP composed of several stacked ICs, the number of bonding wires or TSV interconnections are close to a thousand [24], causing coupling between interconnections due to criss-crossing of the wires. Since achieving higher integration density reduces the pitch size among interconnections, the number of interconnections will increase further, along with stronger electrical coupling that can lead to noise interference.

Furthermore, for accurate electrical design of SiP including radio frequency (RF), analog, and digital submodules, the 3-D interconnection model should cover a sufficiently wide frequency range. The broadband model needs to capture frequency-dependent losses, coupling, and mismatch, which are contributed by the parasitic elements such as series inductances, resistances, shunt capacitances, and conductances. Extracting the frequency-dependent conductor loss and inductive coupling is

especially difficult because they are calculated from the current density distribution that is affected by skin and proximity effects.

In case of modeling TSV interconnections, the silicon substrate should be considered as another source of loss. Significant silicon substrate loss not only influences the signal attenuation, but also complicates interconnection characteristics. Interconnections around silicon substrate show diverse behaviors (operation modes) depending on conductor/oxide dimensions, frequency, and silicon resistivity [25]. Thus, an accurate TSV model should provide the right operation mode by addressing all the effects of the design parameters. Clearly, this modeling requirement is extremely challenging when a large number of TSV interconnections are involved.

In summary, a desired 3-D interconnection modeling tool should be able to describe the broadband electrical behavior of interconnections accurately by extracting parasitic elements from a large number of 3-D interconnections, as illustrated in Figure 5. In addition, the modeling tool needs to be computationally efficient and should have the capability to interface with existing 3-D CAD tools, as part of a design flow. To discuss the required features in more detail, the following section surveys existing modeling methods and their limitations in modeling 3-D integration.

1.4 Previous Research on Modeling 3-D Interconnections

This section outlines the background and the previous research related to the modeling of interconnections in 3-D integration. After a brief definition of interconnection modeling, the following subsection discusses analytical and measurement-based approaches for modeling the bonding wire and TSV interconnections. Commenting on the limitations of the analytical methods, the last subsection presents several numerical electromagnetic (EM) approaches for obtaining the generalized model.

The purpose of modeling interconnections is to extract equivalent circuits that describe the electrical characteristics of given interconnection structures. A typical

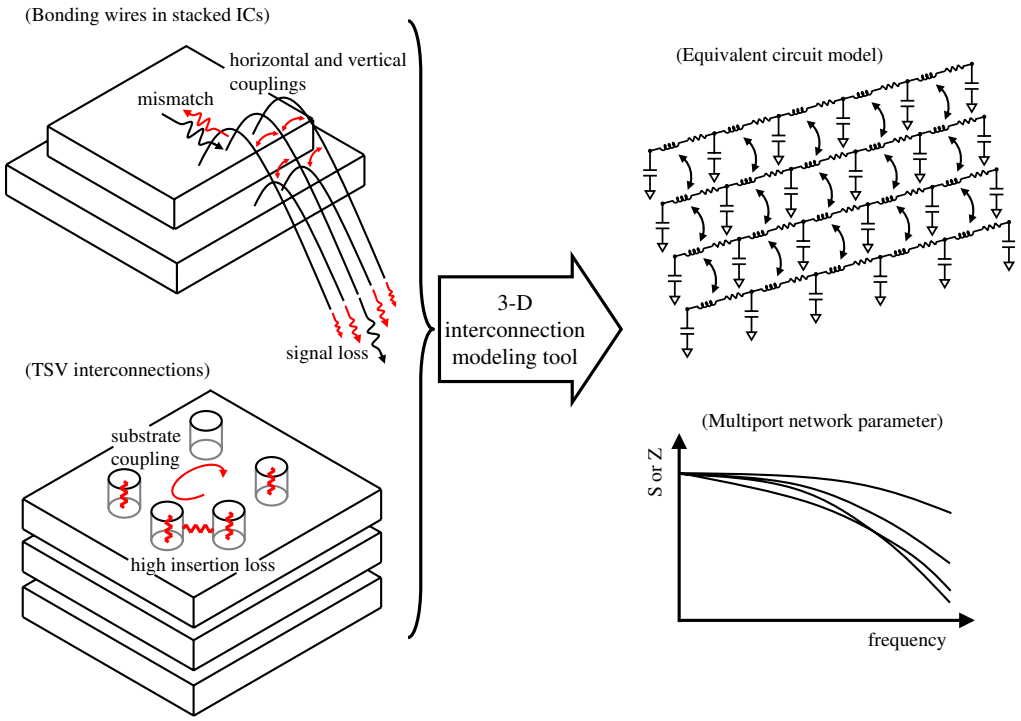


Figure 5. 3-D interconnection modeling tool that captures the electrical behavior of bonding wires and TSV interconnections.

lumped model of a single interconnection is shown in Figure 6, which is composed of a series inductor, a series resistor, and a parallel capacitor. The values of circuit elements are determined by the shape of the interconnection itself as well as the coupling from nearby interconnections and other passive structures such as power/ground planes.

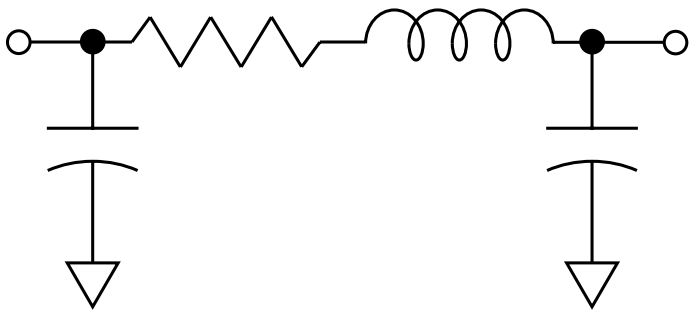


Figure 6. A typical lumped model of a single interconnection (π model).

As a signal-guiding structure, interconnections represent a more general structure

than transmission lines. In other words, interconnections like bonding wires and via interconnections are basically 3-D structures that may not have a uniform cross section throughout the direction of signal propagation. Thus, applying transmission line theory for 3-D interconnection modeling is not appropriate [26]. Because of this fundamental difficulty with 3-D interconnection modeling, most previous research relied on indirect ways for characterization based on measurements, analytical methods, and numerical methods.

1.4.1 Measurement-based and Analytic Modeling Methods

Measurement data can be used for extracting models of 3-D interconnections. The characterization based on measurements of various interconnections including bonding wires has been discussed extensively in [27], using the following approximate formula to extract the interconnection inductance:

$$L \simeq (2\pi f)^{-1}\mathrm{Im}\frac{1+\Gamma}{1-\Gamma}, \tag{1}$$

where Γ is the reflection coefficient. The above simple formula is valid up to the lumped model limit f_B, which satisfies $\angle\Gamma(f_B) = 0.6\pi$. Measurement can also be used to validate various modeling and simulation methods [4, 28]. However, design procedures that are purely based on measurements requires an increased number of design iterations. In particular, the measurement of high-density 3-D interconnections requires a large number of probings along with a complicated setup, resulting in additional cost for design.

By providing an initial guess, analytical approaches reduce the design cost of the purely measurement-based modeling methods. One type of analytical method uses partial inductances [29, 30]. Since the concept of partial inductance was proposed in the early 1900's [31], many analytical expressions of partial inductances for various geometries have been reported. For example, per-unit-length self and mutual partial inductances of two parallel cylindrical conductor segments can be derived as follows

[32]:

$$\begin{aligned} L_{dc} &= \frac{\mu}{2\pi}\Big[\ln\frac{2l}{\rho}-\frac{3}{4}\Big], \\ L_{ac} &= \frac{\mu}{2\pi}\Big[\ln\frac{2l}{\rho}-1\Big], \\ M &= \frac{\mu}{2\pi}\Big[\ln\frac{l}{d}+\sqrt{1+\frac{l^2}{d^2}}-\sqrt{1+\frac{d^2}{l^2}}+\frac{d}{l}\Big], \end{aligned} \tag{2}$$

where ρ, l, and d are the radius, length, and pitch of straight conductors. Since the closed-form models are efficient and do not require numerical computations, they can be used for the modeling of large 3-D interconnections. However, analytic mutual inductance formulas may be inaccurate, especially when two conductors are close to each other [33]. In addition, the simple expression does not include high-frequency effects such as skin and proximity effects.

Another analytic approach models interconnections as the combinations of transmission lines [34, 35], with the characteristics obtained from quasi-static methods as shown in Figure 7. For a single wire and a double-wire pair models, the quasi-static method has been validated with full-wave numerical results [4]. However, the extension of the two-dimension based method to general 3-D problems is not as simple as the single or double-wire case. Similar to the analytical partial component methods, the quasi-static method does not consider conductor losses.

For the TSV interconnection modeling, an equivalent model can be constructed from physical intuition [5, 6]. As shown in Figure 8, the model contains series impedances of copper conductors, shunt oxide capacitances, and shunt silicon admittances. The value of each component is found by tuning the circuit elements to fit its frequency response with measurement data. Although the generated model exhibits good correlation with the measurement data, the measurement-based equivalent model is difficult to extend to general multi-TSV structures due to the increased number of model parameters that need to be tuned to fit multi-port measurement data.

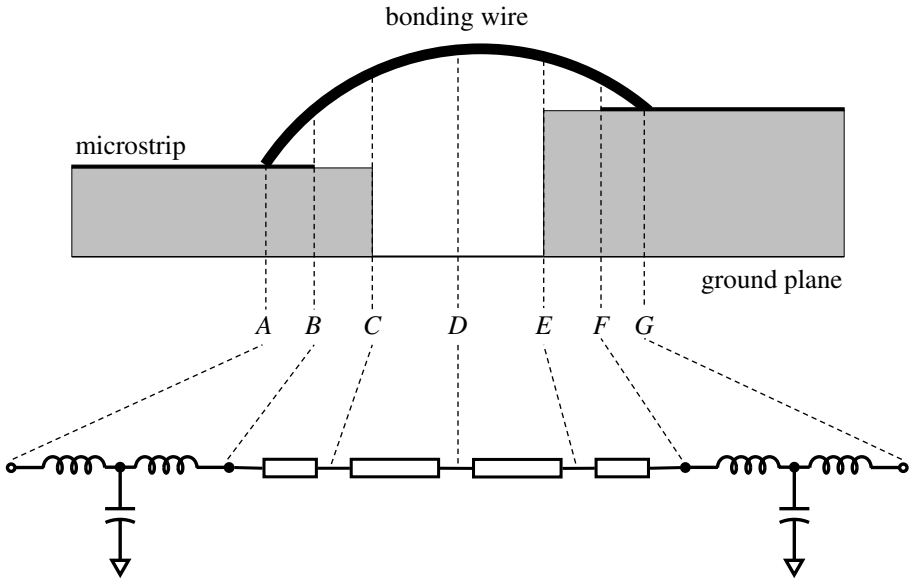


Figure 7. Transmission line segment model of a single interconnection [4].

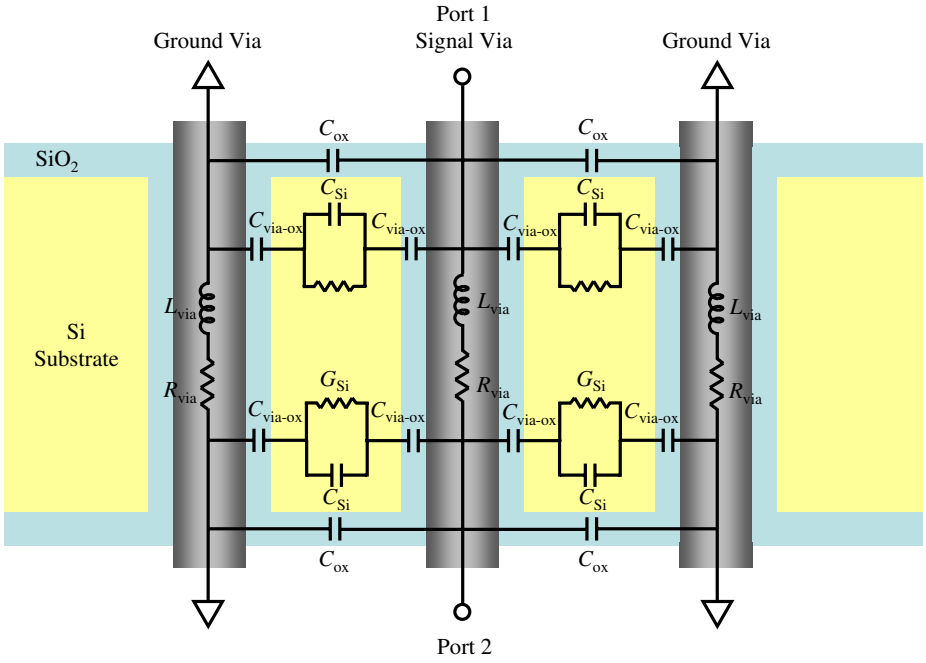


Figure 8. Equivalent circuit model of three TSV interconnections [5, 6].

In summary, measurement-based and analytical modeling methods provide simplified equivalent circuit models for the design of single-chip package and RF circuits.

However, the broadband modeling of complicated 3-D interconnections requires accurate models that contain full electrical coupling among interconnections with high-frequency loss effect. The generality in interconnection modeling can be obtained by using various computational electromagnetic (CEM) techniques. The details of several EM simulation methods are discussed in the following subsection in the context of 3-D modeling.

1.4.2 EM Simulation Methods for 3-D Electrical Interconnections

As discussed in the previous section, numerical simulation is becoming an essential element in the design of 3-D interconnections. As the density of integration and operating frequency increase, the accuracy and efficiency of electromagnetic simulation become important. In addition, the application of EM simulation to 3-D interconnection problems generates new issues that were not important in conventional EM modeling methods. Focusing on the simulation of 3-D interconnections, this subsection reviews the existing nemerical methods.

1.4.2.1 Generic Approaches: Finite Element Method (FEM), Method of Moments (MoM), and Finite Difference Time Domain Method (FDTD)

According to the solution domain and the type of governing equation, CEM methods are categorized into time-/frequency-domain methods and differential/integral equation based methods, as shown in Table 1.[1] This subsection presents three popular methods from each of the three categories: the finite element method (FEM), the method of moments (MoM), and the finite difference time domain (FDTD) method. Their applicabilities to the 3-D interconnection problems are also discussed.

In FEM, the entire problem space is divided into localized cells that represent unknown electric or magnetic fields. The system matrix equation is formulated from the variational principle, where the unknown approximate fields minimize an energy functional related to the differential form of the Maxwell's equation. Since each field

[1] Based on the lecture note of "Topics in Computational Electromagnetics," Georgia Tech.

Table 1. Category of CEM methods.

	Time domain	Frequency domain
Differential equation based	FDTD TLM	FEM
Integral equation based	PEEC	MoM PEEC BEM

quantity interacts only with neighboring elements, the system matrix is sparse. However, generating meshes for the entire problem space may result in a large matrix, especially in the case where finite conductivity in interconnections should be considered. Some of the popular general-purpose EM solvers are developed with FEM, which is applied to the simulation of various microwave problems including transmission line, waveguide, scattering, and antenna. In the area of interconnection characterization, many authors are utilizing commercial FEM solvers [36, 37] to obtain scattering parameters that fit with an equivalent circuit model.

MoM is based on various forms of integral equations that relate excitation fields to the responding current distributions [38]. The current distribution is defined only on the conductor surface, but each cell on the surface is coupled with the Green's function. Therefore, the system matrix from MoM has small but dense property. MoM is efficient especially for the scattering problem of electric conductors. In addition, some of the 2.5-D MoM simulators are popular for the design of planar RF and microwave circuits. A proposed application of MoM to the bonding wire simulation [39, 40] follows MoM formulation of thin perfect conducting wires, and inserts distributed internal impedance in the system matrix.

FDTD solves the differential form of the Maxwell's equation explicitly in time domain [41]. In the leapfrog algorithm, which couples electric and magnetic fields, the

costly process of matrix inversion is not required. On one hand, with its simplicity and memory-saving property, FDTD algorithm is preferred for solving large EM problems. On the other hand, practical implementation of FDTD has several issues such as absorbing boundary condition, excitation, conditional stability, and proper geometric modeling. The time-domain nature of FDTD is also applied popularly to the lumped element simulation of circuits. FDTD simulation of bonding wires and their modeling has been proposed [4, 42], but the incorporation of frequency-dependent losses in the FDTD application is not addressed.

All the generic full-wave methods discussed above provide accurate solutions for bonding wire and via interconnections. However, discretization of the entire structure results in large computational time and memory, especially when modeling 3-D interconnections. Furthermore, the solution type of the generic EM methods is usually a set of numerical data in time or frequency domain, which requires additional steps for extracting the equivalent network. For the simple modeling of a few interconnections, an initial model can be constructed by intuition or through a simple optimization process to find component values that fit the simulated scattering parameters. However, for generalized modeling, macromodeling such as vector fitting [43] with broadband passivity enforcement [44, 45] may be necessary. This extraction procedure can be a computational burden when we try to address large 3-D interconnections arising in SiP.

1.4.2.2 Partial Element Equivalent Circuit (PEEC) Methods

A prominent feature of the PEEC method from the common CEM approaches described in the previous subsection is that it automatically generates equivalent circuits directly from Maxwell's equation. Thus, the PEEC method is especially popular in the research of electromagnetic compatibility (EMC) and interconnection modeling, where equivalent circuit models should represent electromagnetic behavior accurately. This subsection introduces a brief history and formulation of the PEEC method.

The theory and formulation of PEEC, proposed first by Ruehli [46], was originally aimed for the calculation of 3-D equivalent inductances and capacitances under the quasi-static assumption. Over thirty years after the seminal work, the PEEC method was generalized to a full-wave method by including retardation [47], and extended to problems involving inhomogeneous dielectrics [48].

The PEEC method is constructed from the following volume integral equation in a point of a conductor, which is obtained by substituting integral expressions of scalar and vector potential in Maxwell's equation. In this formulation, homogeneous dielectric is assumed, and excitation of electric field in a conductor is neglected.

$$\frac{\vec{J}(\vec{r},t)}{\sigma} + \frac{\mu}{4\pi}\int_{V'} G(\vec{r},\vec{r'})\frac{\partial \vec{J}(\vec{r'},t')}{\partial t}dV' = -\nabla\Phi(\vec{r},t), \tag{3}$$

$$\frac{1}{4\pi\epsilon_0}\int_{V'} G(\vec{r},\vec{r'})q(\vec{r'},t')dV' = \Phi(\vec{r},t), \tag{4}$$

where $t' = t - |\vec{r} - \vec{r'}|/v_p$ is the retarded time and $G(\vec{r},\vec{r'}) = 1/|\vec{r} - \vec{r'}|$ is the Green's function.

The basic scheme of discretization in the classical PEEC method is to divide a conductor into a number of filaments and panels as shown in Figure 9. The current density and the electric charge density are approximated to be constant over the conductor elements. The staircase approximation of the current and charge is equivalent to using the following piecewise constant basis functions.

$$\vec{J}(\vec{r},t') \simeq \sum_{n=1} \vec{w_n}(\vec{r})I_n(t_n), \tag{5}$$

$$q(\vec{r},t') \simeq \sum_{j=1} v_j(\vec{r})Q_j(t_j), \tag{6}$$

where

$$\vec{w_n}(\vec{r}) = \begin{cases} \frac{\vec{l_n}}{|V_n|} & \vec{r} \in V_n \\ 0 & \text{elsewhere} \end{cases},$$

$$v_j(\vec{r}) = \begin{cases} 1 & \vec{r} \in S_j \\ 0 & \text{elsewhere} \end{cases},$$

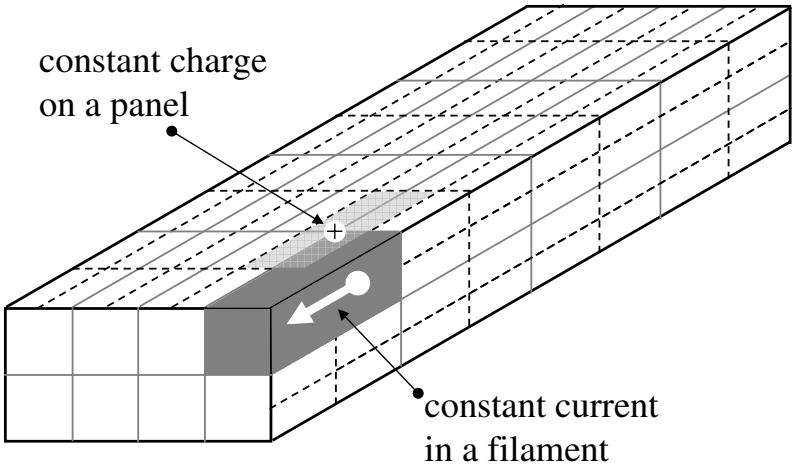


Figure 9. Discretization model for PEEC method.

n is the element index, and $t_n \equiv t - |\vec{r} - \vec{r}_n|/v_p$ is the approximation of t'.

Inserting the approximate current and charge functions and applying the inner product based on the Galerkin's method results in the following equivalent circuit equation.

$$R_{Pmm} I_m(t_m) + \sum_{m=1}^{M} \sum_{n=1}^{N} L_{Pmn} \frac{\partial I_m(t_n)}{\partial t} = - \int_{V_m} \nabla \Phi(\vec{r}, t) dV_m, \tag{7}$$

$$\sum_{i=1}^{I} \sum_{j=1}^{J} P_{Pij} Q_j(t_j) = \int_{S_i} \Phi(\vec{r}, t) dS_i, \tag{8}$$

where

$$\begin{aligned} R_{Pmm} &= \frac{1}{\sigma} \frac{l_m^2}{V_m^2} \int_{V_m} dV_m, \\ L_{Pmn} &= \frac{\mu}{4\pi} \frac{\vec{l_m} \cdot \vec{l_n}}{|V_m||V_n|} \int_{V_m} \int_{V_n} G(\vec{r}, \vec{r}') dV_n dV_m, \\ P_{Pij} &= \frac{1}{4\pi\epsilon_0} \int_{S_i} \int_{S_j} G(\vec{r}, \vec{r}') dS_j dS_i. \end{aligned}$$

The approximate circuit equation is composed of resistance, partial inductance, and the coefficient of potential (inverse of the capacitance). Each partial element can be obtained by computing an analytical or numerical integral. Clearly, the circuit equation can be expressed by the PEEC model [7] as shown in Figure 10. For generating

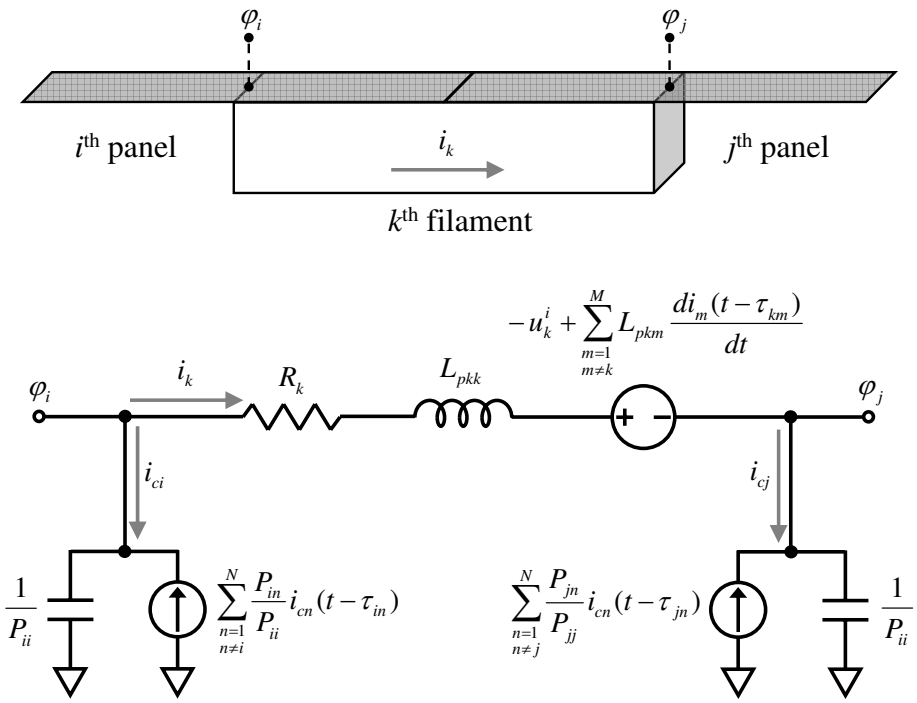


Figure 10. Equivalent circuit model of a conductor filament and two panels for the PEEC method [7].

the equivalent network, the PEEC method is flexible and can be combined with the time-domain SPICE approach for simulating with non-linear components [7].

In spite of its benefits in 3-D interconnection simulation and modeling, the conventional PEEC method has difficulties in modeling large 3-D interconnection structures. Bonding wire simulation examples using the PEEC method [42, 28] show a computational cost issue due to the large full matrix generated from the interaction among conductors. Although acceleration methods using the fast multi-pole method (FMM) [49] or asymptotic waveform evaluation (AWE) enabled the PEEC method to solve larger conductor problems, further improvements are required for solving 3-D interconnections with hundreds and thousands of bonding wires.

Another issue of using the PEEC method for 3-D interconnection modeling is addressing the cross-sectional geometry which has a cylindrical shape. Usually, many of 3-D interconnection such as bonding wires and via interconnections have circular cross section, so the rectangular staircase discretization shown in Figure 9 is not

efficient to capture the geometry.

1.4.2.3 EFIE with Conduction Mode Basis Functions (CMBF)

A solution to reduce the large matrix from the classical PEEC method is to introduce global basis functions. The method for using the global bases originates from modal network theory [50], and its application to the modification of the PEEC method was first proposed by Daniel et al. [51]. The global basis function is the solution of the diffusion equation of the current density in the conductor cross section, which leads to the following series representation [52]:

$$J_z(x,y) = \sum_{\nu} C_\nu e^{-p_\nu x} e^{-q_\nu y}, \tag{9}$$

where $p_\nu^2 + q_\nu^2 = \left(\frac{1+j}{\delta}\right)^2$, $\delta = 1/\sqrt{\pi f \mu \sigma}$ is the skin depth, f is frequency, $\mu = 4\pi \times 10^{-7}$ is the free-space permeability, and σ is the conductivity. The combination of a small number of basis functions can describe current crowding without filament discretization, as shown in Figure 11. Since a few global conduction mode basis functions (CMBF) capture skin and proximity effects, the CMBF-based method reduces the size of the partial impedance matrix considerably compared to the classical PEEC method.

By using the Galerkin's method similar to the PEEC method, the CMBF-based approach generates modal equivalent circuits. For example, the equivalent network formed in Figure 12 is constructed with three basis functions [53]. The voltage sources represent resistive and inductive couplings. Since the number of modal basis functions is much less than the number of staircase basis functions in the PEEC method, the complexity of the entire network is considerably reduced.

Although the CMBF-based method has the benefits of memory reduction and simplified equivalent circuit model, some issues should be addressed for the simulation and modeling of 3-D bonding wires or via interconnections. Like the rectangular piecewise constant basis functions in the conventional PEEC method, the proposed

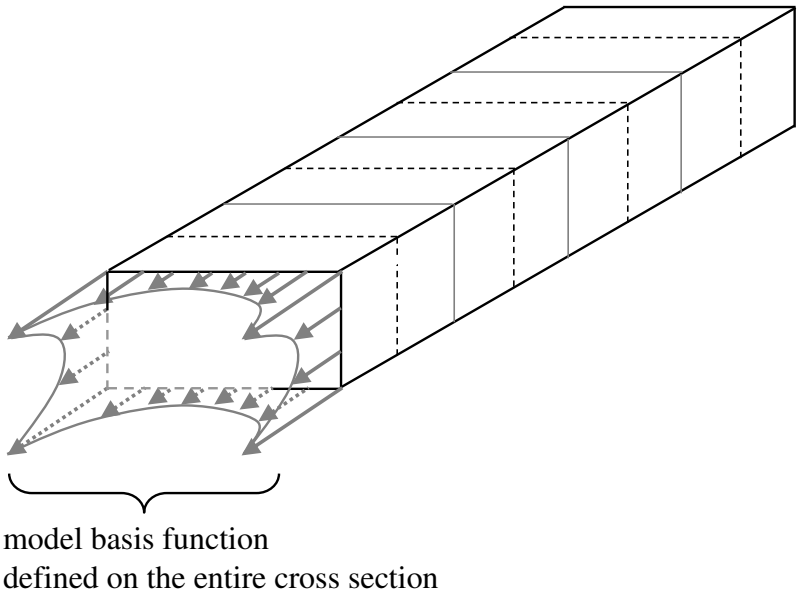


Figure 11. Skin effect described by CMBFs on a rectangular conductor cross section.

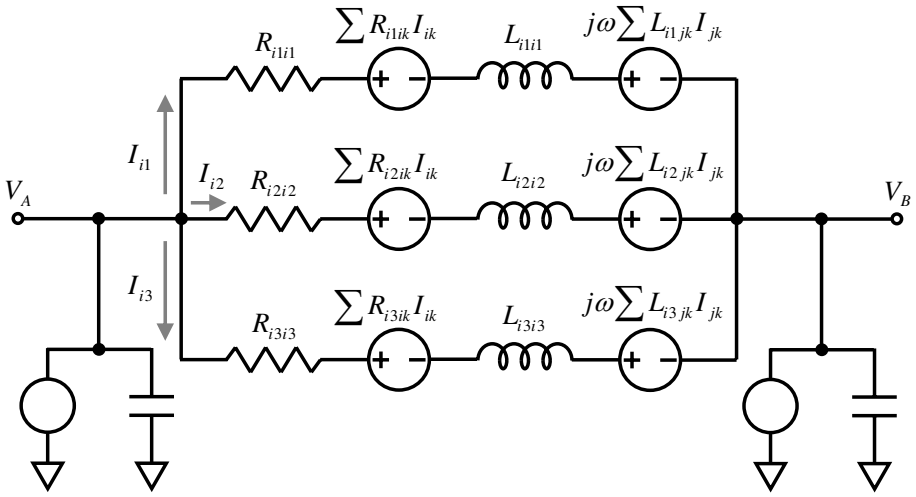


Figure 12. An example of the equivalent circuit of a conductor segment from the CMBF-based method.

CMBF can be used for modeling rectangular geometries, which are applicable for planar interconnections on a printed circuit board (PCB). Thus, the CMBF-based method is not suitable for modeling circular wire bond and via interconnections.

Another issue to be considered when using the rectangular CMBF is about constructing a suitable set of basis functions for each conductor. Identifying the required

modes and allocating them are important for the accurate capturing of current crowding caused by the proximity effect. In the case of brick-type conductors on a planar substrate, "corner mode" and "edge mode" basis functions can be manually allocated according to the physical configuration of conductors. In addition, proximity templates can be used to describe current crowding in arbitrary cross sectional shapes [54]. Nevertheless, capturing current crowding in the 3-D interconnection structure requires a more deliberate allocation of basis functions. The complicated 3-D geometry makes the intuitive definition of required modes very difficult, and the process becomes almost impossible when the number of interconnections becomes large. Therefore, for the practical use of the CMBF for generalized modeling, more efficient ways of allocating basis functions are necessary.

1.5 Completed Research

The discussion in the previous section shows that the existing methods are not optimized in their accuracy and applicability for modeling interconnection structures in 3-D integration. Therefore, for 3-D integration to be a dominant technology that leads the system integration law, this dissertation research sets the objective as the construction of an efficient method to model large number of 3-D interconnections accurately. The basic methodology used in this research is to construct an integral-equation-based model, which is associated with new types of global basis functions. The proposed basis functions will be shown to be efficient both in the practical use for 3-D modeling and in its computational performance. The proposed method has been applied for modeling bonding wires in stacked ICs and TSV interconnections, but can be generally used for other cylindrical interconnections as well.

The following work has been completed in this dissertation.

- **Inductance and resistance extractions of cylindrical conductors**: Since

series inductance and resistance are the most significant interconnection parasitic elements, the accurate extraction of them is the fundamental goal of this dissertation. To calculate frequency-dependent resistances and inductances, a new cylindrical conduction mode basis function (CMBF) is developed. The cylindrical CMBFs automatically capture arbitrary current density distribution in the cross section of conductors, so skin and proximity effects can be easily included. The modal partial resistance and inductances are calculated, and two efficiency enhancement schemes are used for accelerating the inductance matrix generation. Several validation examples show that the calculated inductances and resistances are well matched with the existing simulation tools, and the computational time of the proposed method is considerably reduced.

- **Capacitance extraction of cylindrical conductors**: Accurate modeling of the capacitive coupling is important for high-frequency characterization of 3-D interconnections. Thus, a new cylindrical accumulation mode basis function (AMBF) is developed to capture the charge density distribution on a cylindrical conductor, and modal partial coefficients of potential are calculated from the scalar potential integral equation. For modeling molded interconnections, the formulation is generalized to the case that interconnections are in lossless dielectric background media. The broadband parasitic model is generated by combining the series R-L model and the capacitive coupling model. Two capacitance calculation examples are shown to validate the proposed method with the existing analytic and simulation data.

- **Bonding wire modeling with the inclusion of planar coupling**: The constructed RLC modeling method can be applied to extract parasitic elements of coupled bonding wires, but more accurate bonding wire modeling requires the consideration of the coupling from other planar structures such as bonding pads,

finite ground planes/rings, and planar interconnections. To capture the effect of planar structures, the integral equations are re-formulated to couple the cylindrical CMBF/AMBF with piecewise constant basis functions. In addition, the image method is used for approximating large and solid ground plane. Modeling examples of bonding wires in packaged IC stacks validates the proposed method with the full-wave EM simulation results.

- **TSV interconnection modeling with modal excess capacitance extraction**: TSV interconnections can be modeled by using the proposed modal *RLGC* model, but the effect of oxide coating around the via conductor should be considered additionally. Thus, a new cylindrical polarization mode basis function (PMBF) is developed to capture polarization currents in the oxide region. The resultant modeling with the cylindrical PMBF produces excess capacitances in a similar way of the conventional PEEC method [48]. Although some low-frequency errors are observed, the proposed preliminary method can characterize a large number of TSV interconnections efficiently.

1.6 Dissertation Outline

The rest of this dissertation consists of the following chapters. Chapter 2 proposes inductance and resistance calculation method based on the electric field integral equation combined with cylindrical CMBFs. Details of EFIE formulation, partial element calculations, and modal voltage differences are presented. Chapter 3 discusses the capacitance and conductance calculation method based on the scalar potential integral equation with cylindrical AMBF. A modal voltage equation is constructed in a similar way as in Chapter 2.

After presenting the theoretical framework in Chapter 2 and 3, the following chapters presents the application to model 3-D interconnections. Chapter 4 models typical bonding wire structures that are combined with ground plane and other planar

structures. Chapter 5 discusses TSV modeling. To consider the current leakage to the substrate, thin insulators are modeled with the cylindrical PMBF. The lossy dielectric effect is also included. Chapter 6 concludes this dissertation and proposes future work.

CHAPTER 2

INDUCTANCE AND RESISTANCE EXTRACTIONS OF CYLINDRICAL INTERCONNECTIONS

As discussed in the introduction, 3-D integration enables the miniaturization of systems. However, a major difficulty in the realization of such systems is the parasitics of the 3-D interconnections. Hence, the modeling of such interconnection parasitic elements is significant. Among the 3-D interconnection modeling tasks, the extractions of the conductor resistance and the inductance are especially important since they are dominant elements that determine the electrical characteristics of the interconnections from DC to high frequencies.

The main difficulty of inductance and resistance extractions arises when capturing their frequency-dependent behaviors. These behaviors originate from the inductive reactance in the internal region of the interconnection. As frequency increases, current flows on the surface of the interconnection, so the effective cross sectional area for the current is reduced. The resultant increase in the high-frequency interconnection resistance is called the skin effect [55]. The current density distribution is more complicated when several interconnections are inductively coupled to each other. Depending on the conductor orientation and the relative current directions, the high-frequency currents can crowd in a localized region. This behavior is called the proximity effect, which can further increase the high-frequency resistance. With the existing methods, modeling the skin and the proximity effects in 3-D interconnections can be challenging.

To address the high-frequency issues in modeling a large number of 3-D interconnections, this chapter proposes an efficient modeling method that extracts an equivalent network from the approximation of the volume electric field integral equation (EFIE). The proposed method is based on the same framework as the partial element

equivalent circuit (PEEC) method [46], but it is different in that it uses the global conduction mode basis functions (CMBF). The original work [56] used the CMBF to improve efficiency for modeling planar interconnections. However, this approach was not suitable for cylindrical geometries, which is necessary for modeling conductors with a cylindrical cross section arising in 3-D integration. Therefore, this chapter utilizes another type of basis function called the cylindrical CMBF.

This chapter is organized as follows. Section 2.1 introduces the CMBF with its classification and discusses the formulation of the EFIE combined with the basis functions. The formulation procedure also includes the computation of partial resistances and inductances and the construction of equivalent circuits. Section 2.2 discusses the implementation of the proposed method with two schemes to achieve the capability required for modeling a large number of 3-D interconnections. Section 2.3 shows several application examples that validate the accuracy and efficiency of the proposed method, followed by the summary in Section 2.4.

2.1 Formulation of EFIE with Cylindrical CMBFs

This section introduces the cylindrical CMBF with its classification and applies the basis functions to the construction of equivalent circuit equations. Several techniques for computing partial resistances and inductances are discussed as well.

2.1.1 Cylindrical CMBF

The main feature of the CMBF is that it globally describes the current density distribution in the cross section of a conductor. Using this global nature of the CMBF reduces the required number of basis functions, which can be large when using localized constant basis functions [46]. Clearly, the smaller number of bases has merit for reducing the size of the partial impedance matrix, as discussed in the use of the CMBF for rectangular geometries [56].

The cylindrical CMBFs are constructed from the following current density diffusion equation [50].

$$\nabla \times \nabla \times \vec{J} + \alpha^2 \vec{J} = 0, \tag{10}$$

where $\vec{J}$ is the current density (A/m^2), $\alpha^2 = -j\omega\mu\sigma = -\left(\frac{1+j}{\delta}\right)^2$, $\omega = 2\pi f$ is angular frequency (rad/sec), $\mu = 4\pi \times 10^{-7}$ is the free-space permeability (H/m), σ is the conductivity (S/m), and $\delta = 1/\sqrt{\pi f \mu \sigma}$ is the skin depth (m). One assumption for deriving (10) from Maxwell's equations is that the medium is a good conductor ($\sigma \gg \omega\epsilon$). The other assumption about the current density is that it flows in the axial direction without any longitudinal variation. These assumptions are valid for thin conductors used in practice. By inserting $\vec{J} = J_z(\rho, \varphi)\hat{z}$, (10) is simplified to the following equation in cylindrical coordinates:

$$\frac{1}{\rho}\frac{\partial}{\partial \rho}[\rho \frac{\partial J_z}{\partial \rho}] + \frac{1}{\rho^2}\frac{\partial^2 J_z}{\partial \varphi^2} + \alpha^2 J_z = 0. \tag{11}$$

By using the separation of variables, i.e., $J_z(\rho, \varphi) = R(\rho)\Phi(\varphi)$, (11) is separated into the following two ordinary differential equations.

$$\rho^2 R''(\rho) + \rho R'(\rho) + (\alpha^2 \rho^2 - \nu^2) R(\rho) = 0. \tag{12}$$

$$\Phi''(\varphi) + \nu^2 \Phi(\varphi) = 0. \tag{13}$$

Since the current density distribution should be continuous over the conductor cross section, the solutions of (13) are periodic (harmonic) functions, and ν should be an integer n. Substituting ν^2 with n^2 converts (12) to the Bessel differential equation of order n. Therefore, the basis functions, which are the solutions of the diffusion equation, have the following form [57].

$$\cos(n(\varphi - \varphi_0)) J_n(\alpha\rho) \quad n = 0, 1, 2, \cdots, \tag{14}$$

where $J_n(\alpha\rho)$ is the n^{th} order Bessel function or Kelvin function [58], the asymptotic behavior of which is the exponential function of ρ. For the use of (14) as basis functions, a proper classification of the order n and the orientation φ_0 is necessary.

The physical behavior of the bases with different orders classifies the cylindrical CMBFs into skin-effect (SE) and proximity-effect (PE) modes. The SE-mode basis is the fundamental-order ($n = 0$) function, which shows the same behavior as that of the skin-effect current distribution in a circular cross section. The PE modes are the remaining higher-order ($n > 0$) basis functions, which have sinusoidal behaviors in their angular variations. The collection of the harmonic angular functions in PE modes enables the description of current crowding caused by proximity effects. Considering that Fourier series expansion can express any periodic function of φ, we classify two orthogonal basis functions for each order of the PE modes. In summary, the cylindrical CMBFs are classified into the following groups for the i^{th} conductor in global coordinates:

Skin-effect (SE) mode ($n = 0$):

$$\vec{w}_{i0} = \begin{cases} \frac{\hat{z}_i}{A_{i0}} J_0(\alpha(\vec{r} - \vec{r}_i) \cdot \hat{\rho}_i) & \vec{r} \in V_i \\ 0 & \text{elsewhere} \end{cases}, \tag{15}$$

Proximity-effect, direct (PE-d) mode ($n > 0$):

$$\vec{w}_{ind} = \begin{cases} \frac{\hat{z}_i}{A_{in}} J_n(\alpha(\vec{r} - \vec{r}_i) \cdot \hat{\rho}_i) \cos(n\varphi_i) & \vec{r} \in V_i \\ 0 & \text{elsewhere} \end{cases}, \tag{16}$$

Proximity-effect, quadrature (PE-q) mode ($n > 0$):

$$\vec{w}_{inq} = \begin{cases} \frac{\hat{z}_i}{A_{in}} J_n(\alpha(\vec{r} - \vec{r}_i) \cdot \hat{\rho}_i) \sin(n\varphi_i) & \vec{r} \in V_i \\ 0 & \text{elsewhere} \end{cases}, \tag{17}$$

where $\vec{r} = x\hat{x} + y\hat{y} + z\hat{z}$ is a point in the i^{th} conductor, $\vec{r}_i = x_{i0}\hat{x} + y_{i0}\hat{y} + z_{i0}\hat{z}$ is the center point of the i^{th} conductor, and A_{in} is the effective area. A_{in} is the constant that normalizes the basis function so that the integration of the function over the cross section equals unity. If $n = 0$, the effective area can be found as follows.

$$A_{i0} = \frac{2\pi\rho_i}{\alpha} J_1(\alpha\rho_i). \tag{18}$$

However, the integration of the higher-order basis functions ($n \geq 1$) should be zero because of the harmonic component in the φ direction. Thus, the normalization is redefined as follows.

$$\int_{S_{in}} \vec{w}_{in} \cdot d\vec{S} = \frac{1}{2n}, \tag{19}$$

where S_{in} is a part of the cross section occupied by a half period of the harmonic function, which is $\frac{1}{2n}$ of the entire cross sectional area. By inserting (16) or (17) into (19):

$$A_{in} = \frac{2^{2-n}\alpha^n \rho_i^{2+n}}{(2+n)n!} {}_1F_2\Big(1 + \frac{n}{2}; \{2 + \frac{n}{2}, 1 + n\}; -\frac{1}{4}\alpha^2\rho_i^2\Big), \tag{20}$$

where ${}_1F_2$ is one of the forms of the generalized hypergeometric function.

A main advantage of using the cylindrical CMBF is that the orthogonal PE-mode bases automatically capture current crowding in any orientation. This feature makes the proposed method free from pre-constructing the shapes of the basis functions based on conductor geometry or the generation of proximity templates [54]. Thus, we can apply the cylindrical CMBF for more general 3-D interconnection problems, where many conductor segments are located in a complicated fashion. For example, Figure 13 demonstrates how the linear combination of SE- and PE-mode basis functions describes a specified current density distribution induced by the proximity of nearby conductors.

2.1.2 EFIE Formulation

The previously defined cylindrical CMBFs are inserted into the volume EFIE to form equivalent voltage equations, which are composed of the modal partial impedances of each conductor. This subsection outlines the formulation procedure, including the calculation of the impedances and the construction of the equivalent network.

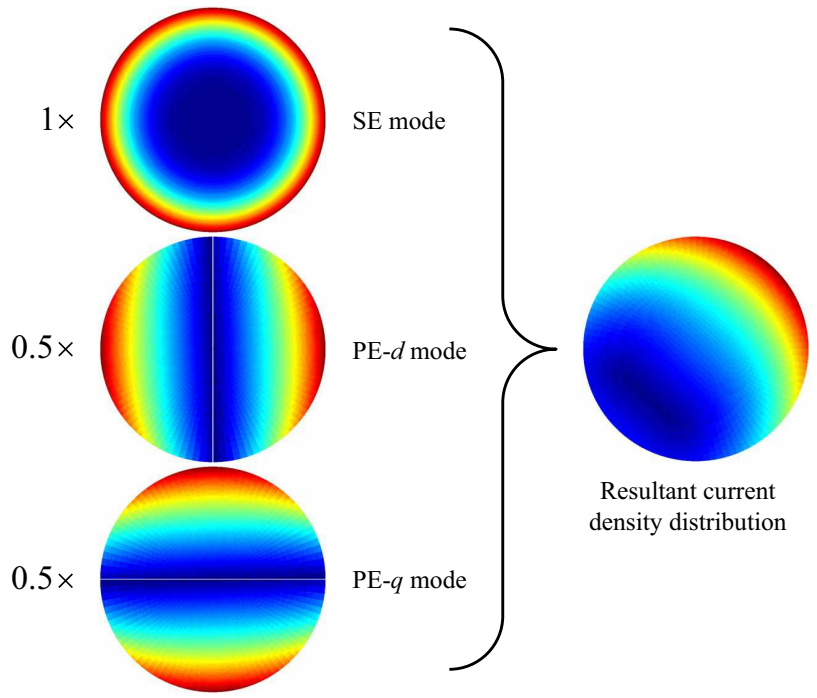


Figure 13. Examples of cylindrical CMBFs at 10^8 Hz and their combination to generate a current density distribution.

2.1.2.1 Voltage Equation

As in the classical PEEC method [46] and the original CMBF-based method [56], the proposed method approximates the following volume EFIE.

$$\frac{\vec{J}(\vec{r},\omega)}{\sigma} + j\frac{\omega\mu}{4\pi}\int_{V'} G(\vec{r},\vec{r'})\vec{J}(\vec{r'},\omega)\mathrm{d}V' = -\nabla\Phi(\vec{r},\omega), \tag{21}$$

where $\Phi(\vec{r},\omega)$ is electric potential (V) and $G(\vec{r},\vec{r'}) = e^{-jk_0|\vec{r}-\vec{r_j}|}/|\vec{r}-\vec{r_j}|$ is the Green's function. An assumption used in this chapter is that the maximum size of the problem space is much smaller than the wavelength of the maximum modeling frequency, so the retardation term ($e^{-jk_0|\vec{r}-\vec{r_j}|}$) is negligible as in the (L_p, R) PEEC method [26].

Figure 14 defines a general N-conductor system to be discussed in this section. As discussed in the previous subsection, a major difference of the CMBF-based method from the classical PEEC method is that the integral equation is not discretized to volume filaments but to globally-defined conduction modes. However, each cylindrical CMBF is localized to each conductor, as shown in (15) to (17). Therefore, for the

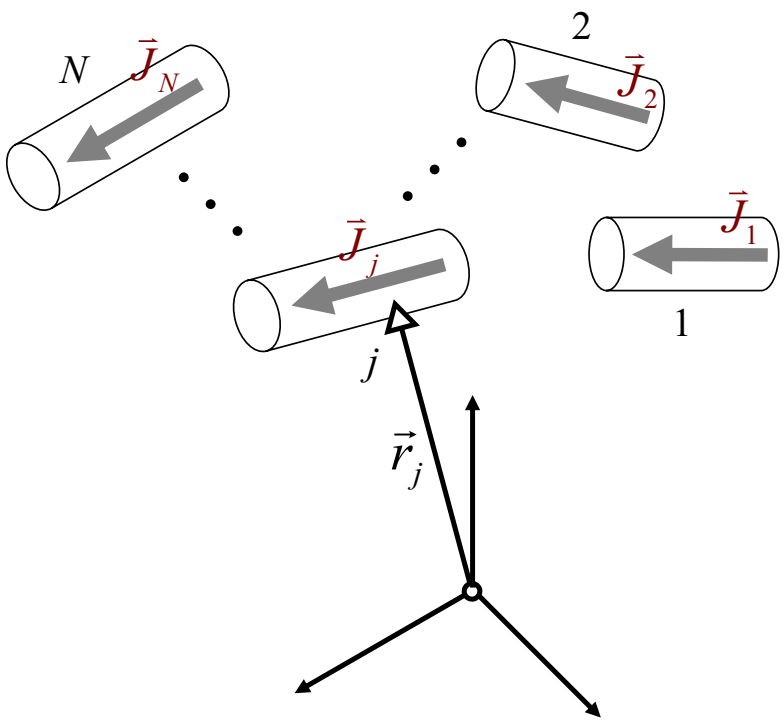


Figure 14. General configuration of N-cylindrical conductor system.

approximation of current density on a conductor segment j, basis functions that belong to the conductor are combined as follows:

$$\vec{J}_j(\vec{r},\omega) \cong \sum_{n,q} I_{jnq}\vec{w}_{jnq}(\vec{r},\omega). \tag{22}$$

By inserting the approximation (22) into the current density term in (21) and applying the following inner product based on Galerkin's method,

$$\langle \vec{w}_{imd}(\vec{r},\omega), \vec{x}\rangle = \int_V \vec{w}^*_{imd}(\vec{r},\omega)\cdot\vec{x}\mathrm{d}V, \tag{23}$$

we obtain the voltage equation containing the following partial resistance, partial inductance, and modal voltage difference.

$$\sum_{n,q} I_{jnq}R_{imd,jnq} + j\omega\sum_{n,q} I_{jnq}L_{imd,jnq} = \Delta V^j_{imd}, \tag{24}$$

where

$$R_{imd,jnq} = \frac{1}{\sigma}\int_{V_i} \vec{w}^*_{imd}(\vec{r_i},\omega)\cdot\vec{w}_{jnq}(\vec{r_j},\omega)\mathrm{d}V_i,$$
$$L_{imd,jnq} = \frac{\mu}{4\pi}\int_{V_i}\int_{V_j} \vec{w}^*_{imd}(\vec{r_i},\omega)\cdot\vec{w}_{jnq}(\vec{r_j},\omega)\frac{1}{|\vec{r_i}-\vec{r_j}|}\mathrm{d}V_j\mathrm{d}V_i,$$

and

$$\Delta V_{imd}^{j} = -\int_{S_i} \Phi_j(\vec{r_i})\vec{w}_{imd}^{*}(\vec{r_i},\omega)\cdot \mathrm{d}\vec{S_i}.$$

After applying the same inner products with other basis functions in the i^{th} conductor, we can combine all voltage equations into the following submatrix equation, which represents the interactions between all modes in two conductors i and j.

$$(\mathbf{R_{ij}} + j\omega\mathbf{L_{ij}})\mathbf{I_j} = \mathbf{V_i^j}, \tag{25}$$

where

$$\mathbf{R_{ij}} = \begin{pmatrix} R_{i0,j0} & R_{i0,j1d} & \dots & R_{i0,jNq} \\ R_{i1d,j0} & R_{i1d,j1d} & \dots & R_{i1d,jNq} \\ & & \ddots & \\ R_{iMq,j0} & R_{iMq,j1d} & \dots & R_{iMq,jNq} \end{pmatrix},$$

$$\mathbf{L_{ij}} = \begin{pmatrix} L_{i0,j0} & L_{i0,j1d} & \dots & L_{i0,jNq} \\ L_{i1d,j0} & L_{i1d,j1d} & \dots & L_{i1d,jNq} \\ & & \ddots & \\ L_{iMq,j0} & L_{iMq,j1d} & \dots & L_{iMq,jNq} \end{pmatrix},$$

$$\mathbf{I_j} = \begin{pmatrix} I_{j0} & I_{j1d} & \cdots & I_{jNq} \end{pmatrix}^T,$$

and

$$\mathbf{V_i^j} = \begin{pmatrix} \Delta V_{i0}^{j} & \Delta V_{i1d}^{j} & \cdots & \Delta V_{iMq}^{j} \end{pmatrix}^T.$$

Finally, all the submatrix equations between conductor segments congregate to form the global impedance matrix equation, whicn contains loss and inductive coupling in the entire conductor system. The size of the global impedance matrix is approximately $(N_c N_m) \times (N_c N_m)$, where N_c and N_m are the number of conductor segments and the required number of modes for a conductor, respectively. N_m is one when only the SE mode is used and is more than one when additional PE modes are used. From a practical standpoint, the number of PE-mode basis pairs is two or three

for accurately describing current crowding, so the required memory of the proposed method is considerably reduced compared to that of the classical PEEC method. An exemplary convergence study is shown in Section 2.3.1. Controlling the number of PE bases, to be discussed in Section 2.2, further reduces the computational cost.

2.1.2.2 Partial Impedances

The calculation of partial resistances and inductances in (24), which involve the computation of sixfold integrals with frequency-dependent integrands, can be computationally expensive. This section discusses analytical and numerical integration techniques that can reduce computation time.

For partial resistances, indefinite integrals can be easily found, and the mutual resistances vanish because of the local and orthogonal properties of the cylindrical CMBFs. Therefore, the global matrix of partial resistances becomes diagonal in the form:

$$R_{imd,jnq} = \begin{cases} \frac{\pi\delta^2\rho_i l_i}{\sigma|A_{i0}|^2}\Im(\alpha J_0^*(\alpha\rho_i)J_1(\alpha\rho_i)) & i=j, m=n=0 \\ \frac{\pi\delta^2\rho_i l_i}{2\sigma|A_{im}|^2}\Im(\alpha^* J_{m-1}^*(\alpha\rho_i)J_m(\alpha\rho_i)) & i=j, m=n\neq 0, d=q \\ 0 & \text{otherwise} \end{cases} . \tag{26}$$

The partial resistance from the SE mode is actually identical to the analytic internal resistance formula of a cylinder [59]. The derivation of (26) is shown in Appendix A.

In contrast to the partial resistances, closed-form expressions of the partial inductances cannot be found; therefore numerical methods need to be used. However, analytical integrations over three variables can reduce the original sixfold integral to the following triple integral:

$$L_{imd,inq} = \frac{\mu}{8\pi}\int_0^{\rho_i}\int_0^{\rho_i}\int_0^{2\pi} \rho\rho' \frac{J_m^*(\alpha\rho)J_n(\alpha\rho')}{A_{im}^* A_{in}} I_{\varphi_\Sigma} I_z \mathrm{d}\varphi_\Delta \mathrm{d}\rho' \mathrm{d}\rho, \tag{27}$$

where

$$I_{\varphi_\Sigma}(\varphi_\Delta) = \begin{cases} 8\pi - 4\varphi_\Delta & m = n = 0 \\ 2(2\pi - \varphi_\Delta)\cos(n\varphi_\Delta) - \frac{2}{n}\sin(n\varphi_\Delta)\cos(2\varphi_d) & m = n \neq 0, d = q \\ \frac{4(-1)^{m+n+1}}{m^2-n^2}[m\sin(m\varphi_\Delta) - n\sin(n\varphi_\Delta)] & m \neq n, d = q(\text{PE-}d) \\ \frac{4(-1)^{m+n+1}}{m^2-n^2}[n\sin(m\varphi_\Delta) - m\sin(n\varphi_\Delta)] & m \neq n, d = q(\text{PE-}q) \\ 0 & \text{otherwise} \end{cases},$$

$$I_z(D, l_i) = 2(\sqrt{D^2} - \sqrt{l_i^2 + D^2}) + l_i \log\left[\frac{l_i^2 + \sqrt{l_i^2 + D^2}}{-l_i^2 + \sqrt{l_i^2 + D^2}}\right],$$

and

$$D^2(\rho, \rho', \varphi_\Delta) = \rho^2 + \rho'^2 - 2\rho\rho'\cos\varphi_\Delta.$$

$D^2(\rho, \rho', \varphi_\Delta)$ is the distance between two points on the cross sectional plane. φ_Δ is a new angular variable that is obtained from the following coordinate transformation of φ and φ', which is useful for both reducing computational cost and avoiding the Green's function singularity during numerical integrations [60].

$$\begin{pmatrix} \varphi_\Delta \\ \varphi_\Sigma \end{pmatrix} = \begin{pmatrix} 1 & -1 \\ 1 & 1 \end{pmatrix} \begin{pmatrix} \varphi \\ \varphi' \end{pmatrix}. \tag{28}$$

Since the Green's function is not a function of φ_Σ, the indefinite integral over φ_Σ reduces one of the six numerical integrals. The detailed derivation of $I_{\varphi_\Sigma}(\varphi_\Delta)$ is shown in Appendix B. In the remaining numerical integrals, singular points of the integrands are concentrated on a line where both $\varphi_\Delta = 0$ and $\rho = \rho'$ hold. In numerical integration based on adaptive Lobatto quadrature [61], the singular points are simply avoided by adjusting the starting points as a small value such that $\varphi_\Delta = 0.01\pi$.

For the calculation of the partial mutual inductances, we rewrite the inductance formula in (24) with the following frequency-dependent and frequency-independent parts:

$$L_{imd,jnq} = \frac{\mu}{4\pi}\int_{\rho_j,\rho_i} \rho_i\rho_j \frac{{J_m}^*(\alpha\rho_i)J_n(\alpha\rho_j)}{A^*_{imd}A_{jnq}} I_{z,\varphi}(\rho_i, \rho_j)\mathrm{d}\rho_i\mathrm{d}\rho_j, \tag{29}$$

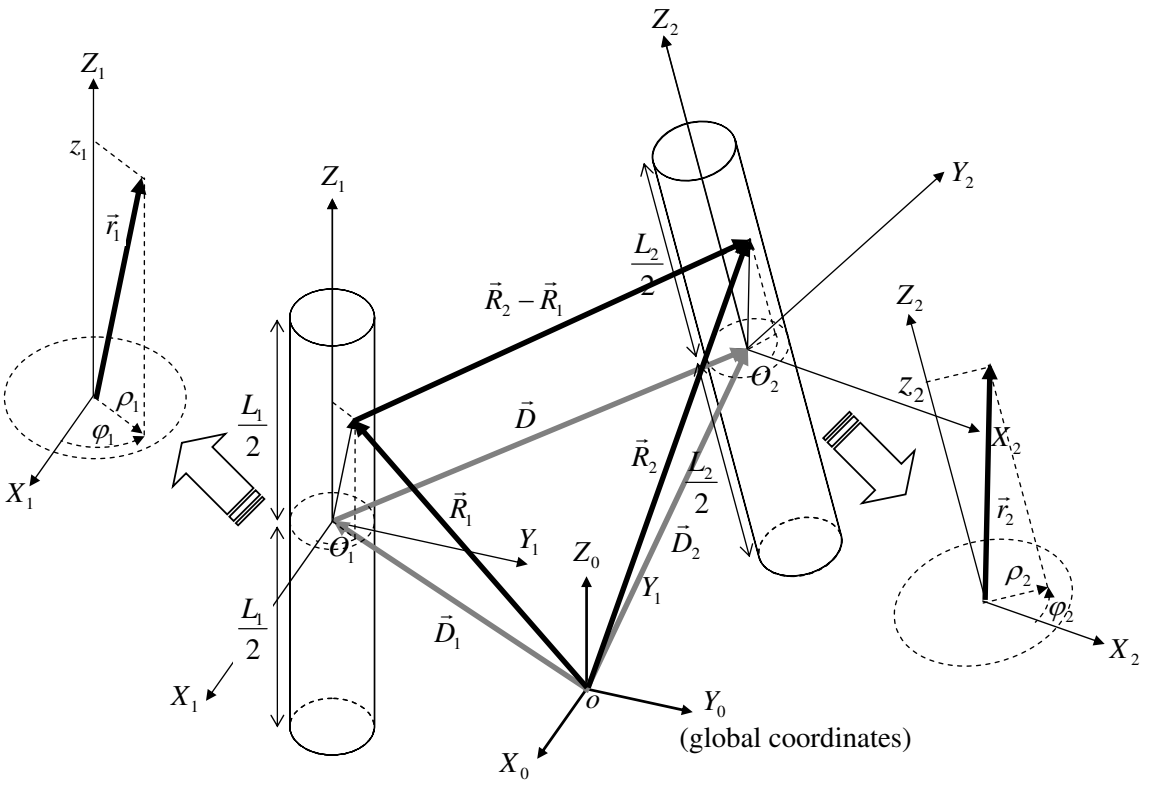


Figure 15. Definition of the orientation parameters between the two separate cylinder segments.

where

$$I_{z,\varphi}(\rho_i,\rho_j)=\int_{\varphi_j,\varphi_i}\cos\left(\varphi_i-\varphi_{i,d}\right)\cos\left(\varphi_j-\varphi_{j,q}\right)\times\int_{z_j,z_i}\frac{(\hat{z}_i\cdot\hat{z}_j)}{|\vec{r_i}-\vec{r_j}|}\mathrm{d}z_i\mathrm{d}z_j\mathrm{d}\varphi_i\mathrm{d}\varphi_j.$$

The frequency-independent $I_{z,\varphi}(\rho_i,\rho_j)$ is composed of analytical integration over (z_i,z_j) and numerical integration over (φ_i,φ_j).

For the calculation of the analytical integral over (z_i,z_j), the distance between two points in two different conductor segments should be formulated with predefined orientations. In Figure 15, translation and rotation (based on Euler angles) can be determined from the defined global coordinates. Then, each point in a conductor is specified with the local cylindrical coordinates, which are related to the cylindrical CMBFs. With the calculated distance, we can obtain indefinite integrals for axial variables (z_i,z_j), as discussed in Appendix C. This analytical expression is more generalized than that of the two thin conductor filaments [30] since it contains local

coordinate variables that represent the inside of the two conductor segments.

To reduce total frequency sweep time, the frequency-independent integrals ($I_{z,\varphi}$s) over (φ_i, φ_j) can be computed before the sweep simulation. The precomputed frequency-independent $I_{z,\varphi}$ is multiplied by the frequency-dependent integrands during the numerical integration over (ρ_i, ρ_j). One issue of this approach is that storing the values of $I_{z,\varphi}$s for every point of (ρ_i, ρ_j) requires a large amount of memory. Fortunately, we can reduce the memory requirement by using the property that $I_{z,\varphi}(\rho_i, \rho_j)$ is a "smooth" bivariate function. That is, the variations in the frequency-independent part of the integrand are smaller than those in the frequency-dependent Kelvin functions. Therefore, after computing integration values for only a small number of data points, the following simple interpolation formula can be used:

$$I_{z,\varphi}(\rho_i, \rho_j) \simeq (1-s)(1-t)I_{p,q} + s(1-t)I_{p,q+1} + (1-s)tI_{p+1,q} + stI_{p+1,q+1}, \quad (30)$$

where $0 \leq s, t \leq 1$ are interpolation parameters, and $I_{p,q}$s are sampled points near (ρ_i, ρ_j). Each $I_{p,q}$ is obtained by double numerical integration over (φ_i, φ_j) based on adaptive Simpson quadrature rule. The total number of the sampled points is determined adaptively according to the relative variation of the Green's function.

For integrals over the remaining two variables (ρ_i, ρ_j), the double integral using adaptive Lobatto quadrature [61] was used since the algorithm provides improved accuracy and reliability compared to adaptive Simpson quadrature and other higher-order quadratures [62].

2.1.2.3 Equivalent Circuit

In addition to the calculated partial resistances and inductances, the modal voltage difference should be considered to generate the global impedance matrix equation and the corresponding equivalent circuit. Since $\Delta V_{imd}^j = 0$ when $i \neq j$, the combined modal voltage difference is reduced as follows:

$$\Delta V_{imd} = \sum_j \Delta V_{imd}^j = \Delta V_{imd}^i, \quad (31)$$

where V_{imd}^{j}'s are modal voltages induced by the j^{th} current density in (24). Since the integral over the lateral surface of a cylinder is zero, we can simplify ΔV_{imd} to the integral over the inlet and the outlet planes (S_i^- and S_i^+, respectively) as follows:

$$\Delta V_{imd} = -\int_{S_i^+} \Phi(\vec{r_+})\vec{w}_{imd}^{*}(\vec{r_i},\omega)\cdot d\vec{S_i^+} - \int_{S_i^-} \Phi(\vec{r_-})\vec{w}_{imd}^{*}(\vec{r_i},\omega)\cdot d\vec{S_i^-}, \qquad (32)$$

where the potentials $\Phi(\vec{r_+})$ and $\Phi(\vec{r_-})$ are assumed to be constant over the cross section.

When the SE-mode basis is involved, the integrals of $\vec{w}_{imd}^{*}$ in (32) are unity since the basis functions are normalized, as discussed in Section 2.1. Thus, the modal potential difference becomes the actual voltage difference between the two nodes. In the case where the PE-mode bases are involved, the modal potential difference becomes zero since the integral of the harmonic functions in the higher-order bases vanish. In summary, the global impedance matrix equation can be expressed as follows:

$$\begin{pmatrix} \mathbf{Z_{ss}} & \mathbf{Z_{sp}} \\ \mathbf{Z_{ps}} & \mathbf{Z_{pp}} \end{pmatrix} \begin{pmatrix} \mathbf{I_s} \\ \mathbf{I_p} \end{pmatrix} = \begin{pmatrix} \mathbf{\Delta V_i} \\ \mathbf{0} \end{pmatrix}, \qquad (33)$$

where $\mathbf{Z_{ss}}$, $\mathbf{Z_{sp}}$, $\mathbf{Z_{ps}}$, and $\mathbf{Z_{pp}}$ are partial impedances grouped by SE and PE modes, $\mathbf{I_s}$ and $\mathbf{I_p}$ are skin- and proximity-effect currents, and $\mathbf{\Delta V_i}$ is the voltage difference across a conductor segment.

From the viewpoint of circuit topology, the equivalent circuit generated from the PE-mode basis function forms a closed loop like a shielded conductor, which is inductively coupled with the other circuits. In an example of the equivalent circuit of two conductor segments (Figure 16), two branches are generated from the SE-mode partial components, and eight loops come from four orthogonal pairs of two PE modes. The number of PE-mode loops varies according to the strength of the proximity effect.

Extending the two-conductor model, Figure 17 illustrates a general equivalent network of coupled 3-D bonding wires. The wires are approximated using connections of several straight conductors, and the physically connected nodes are identical to the

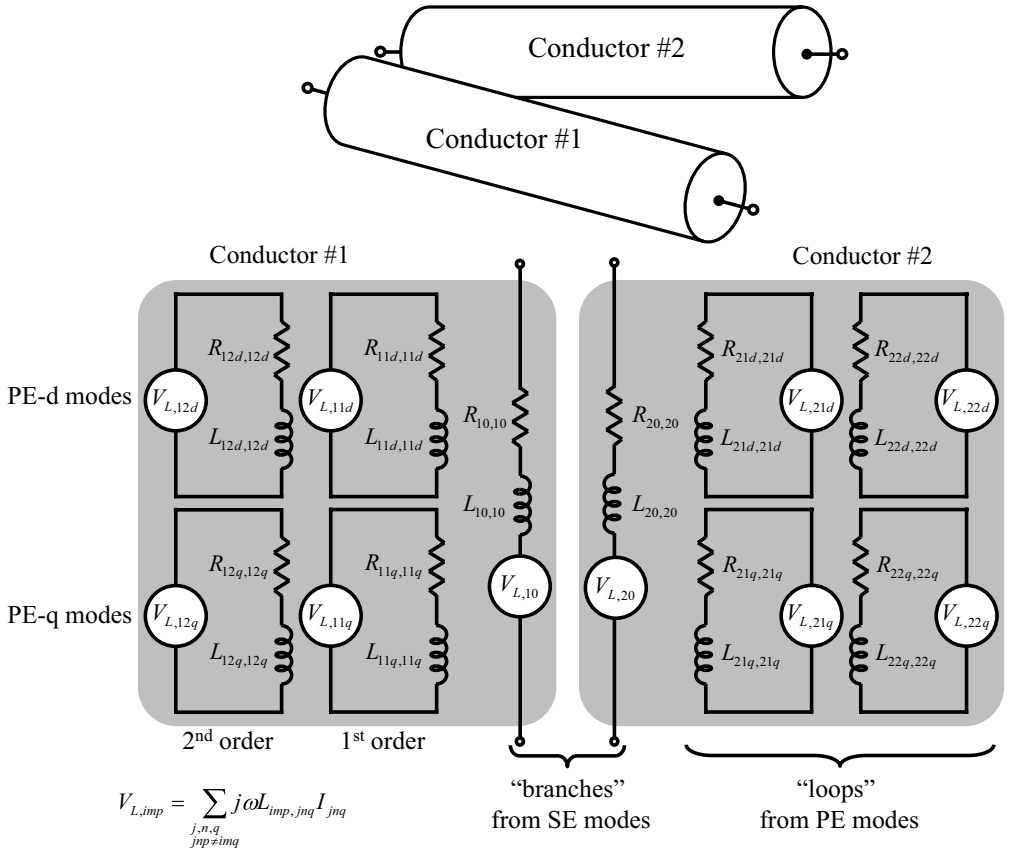


Figure 16. Equivalent circuit example of two coupled cylinders. Two PE-mode basis functions are included for each conductor.

circuit nodes of the SE branches. During the approximation of the bonding wires with the conductor segment model, the number of segments is controlled so that the approximate model captures the original curvature of bonding wires accurately. Since the proposed method assumes that current flows in the axial direction only, the current distribution may be inaccurate, especially at any sharp edge connecting adjoining conductor segments.

2.2 Efficiency Enhancements and Implementation

The proposed method discussed throughout the previous section has the benefit of using the equivalent network's system matrix (33), which is much smaller than the matrix using the classical PEEC method. However, the calculation of the partial impedances (24) for each frequency step is more complicated than the classical PEEC

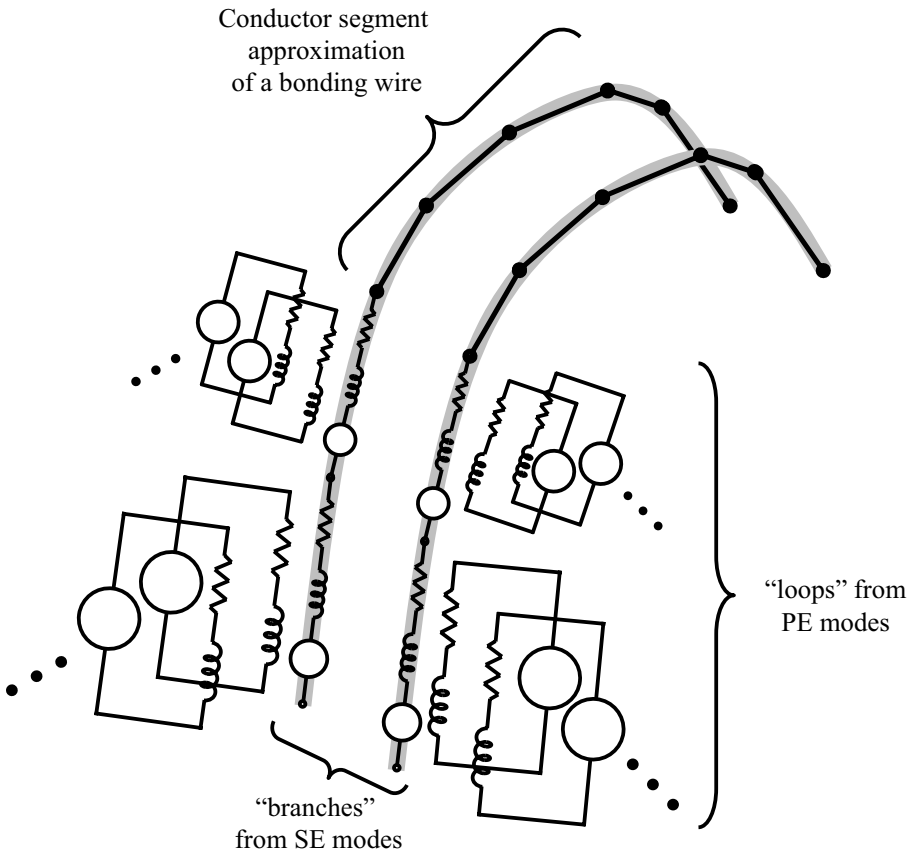


Figure 17. Equivalent circuit of two bonding wires.

method. Therefore, for the modeling of 3-D interconnections in SiP, further reduction of computational cost is necessary.

2.2.1 Controlling the Number of PE-Mode Basis Functions

One of the ideas for reducing computational cost is to use the number of higher-order (PE-mode) bases differently for each neighboring conductor [63]. We can assign a reduced number of higher-order bases to each conductor because calculations related to the higher-order basis functions are not necessary when the distance between two conductors is sufficiently large or when the coupling coefficient is small enough. This can be explained more clearly with an example (see Figure 18). Here we select an arbitrary conductor (e.g., conductor i) and group its neighboring conductors according to their different coupling levels to the conductor i. For the group of conductors

that is within the close proximity to the conductor i, such as conductor j in Figure 18, the computation of PE-mode interactions is required up to the second order. However, for those that are more distant from conductor i, such as conductor k, only the computation of the first order PE-mode interaction is required. Then, when generating the matrices involving PE-mode bases, only partial mutual inductances between the required PE modes are computed and filled, and other elements are set to zero, as shown in Figure 19. Therefore, besides reducing the time to compute modal

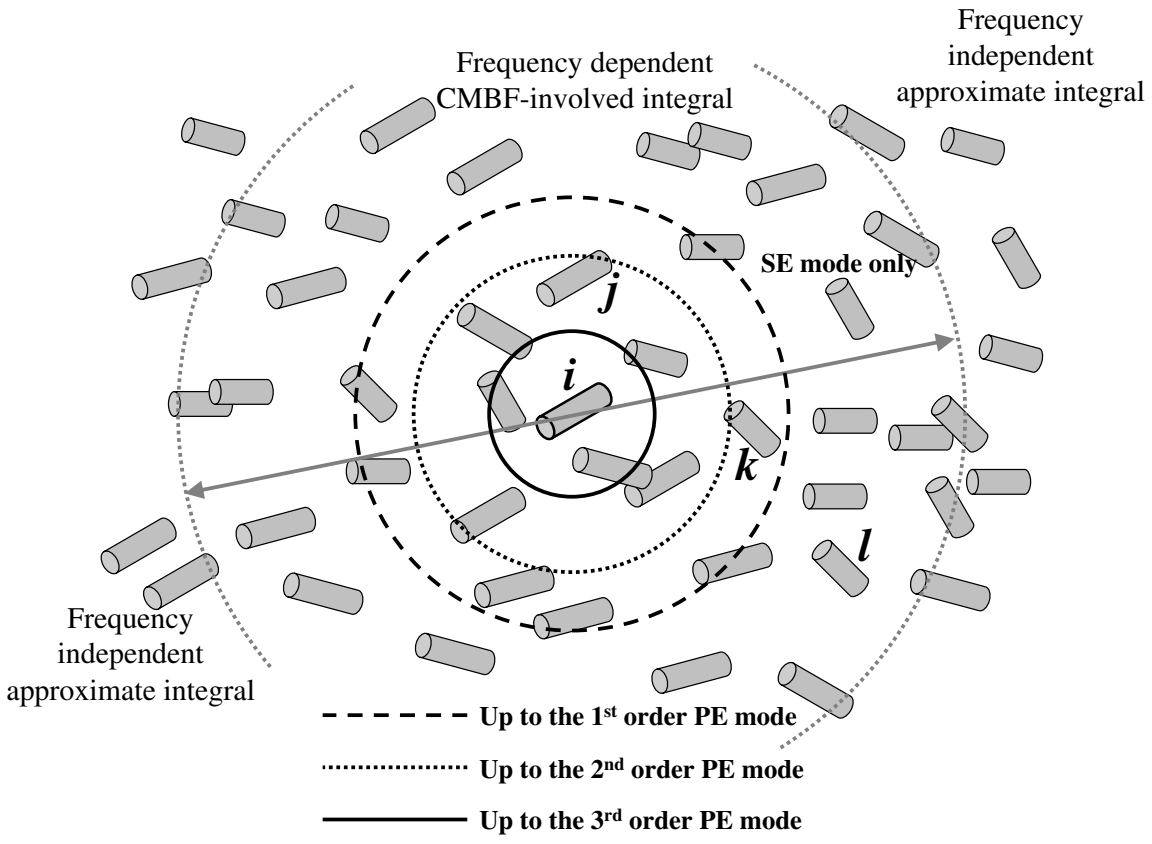


Figure 18. Conceptual diagram of two efficiency enhancement schemes.

mutual inductances, we can save memory for storing non-zero elements because such grouping enables the higher-order submatrices ($\mathbf{Z_{sp}}$, $\mathbf{Z_{ps}}$, and $\mathbf{Z_{pp}}$) of the partial impedance matrix to become sparse.

In the actual calculation of the required number of PE-mode basis functions in each group, we need to consider two key parameters. One is the initial coupling

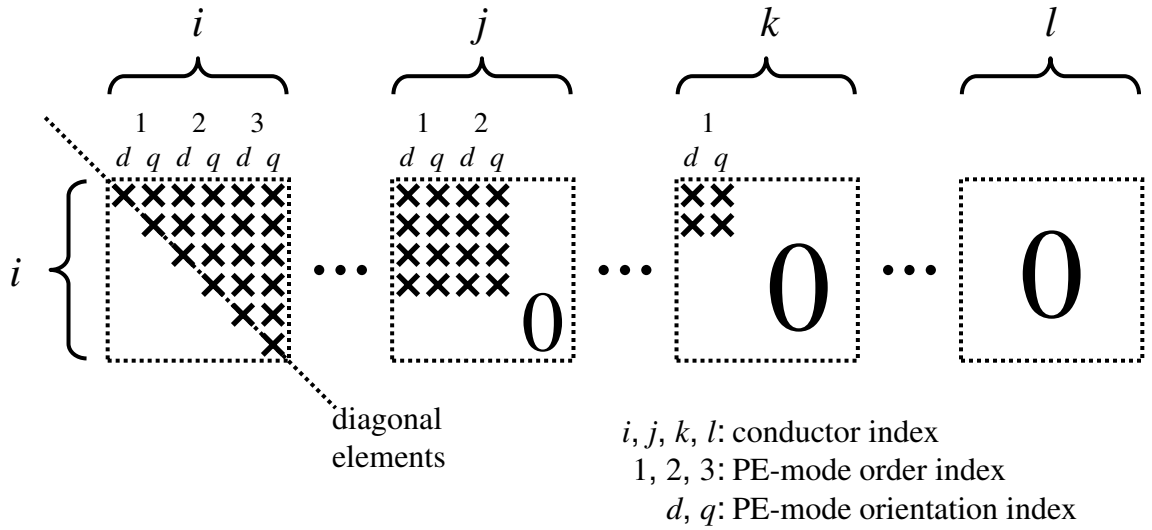


Figure 19. Matrix ($\mathbf{Z_{pp}}$) filling example involving the conductor i in (a). 'X's and '0's represent computed non-zero elements and zeros, respectively.

coefficient obtained with SE-mode bases only, and the other is the aspect ratio of the diameter to length of a cylinder. These parameters have the following important characteristics. The higher the initial coupling coefficient and the larger the aspect ratio, the more higher-order PE-mode basis functions are required. We can show these characteristics by drawing the boundaries of the required number of basis functions under a defined error bound (10^{-3} for example) in Figure 20, which are obtained by computing relative errors in the resultant coupling coefficients for various aspect ratios and initial coupling coefficients.

However, the numerical experiments of Figure 20 are based on a simplified case where the two conductors are parallel and have identical shape (thus aspect ratio). Therefore, one might expect that more rigorous evaluation covering other possible cases where the two conductors have different orientation and shapes from each other is necessary. However, the proximity effect arising from parallel conductors is the maximum compared to other cases of arbitrarily oriented conductors; hence the required PE modes are maximized as well. As for the issue of different shapes of cylinders, we can select the largest aspect ratio among cylinders when determining

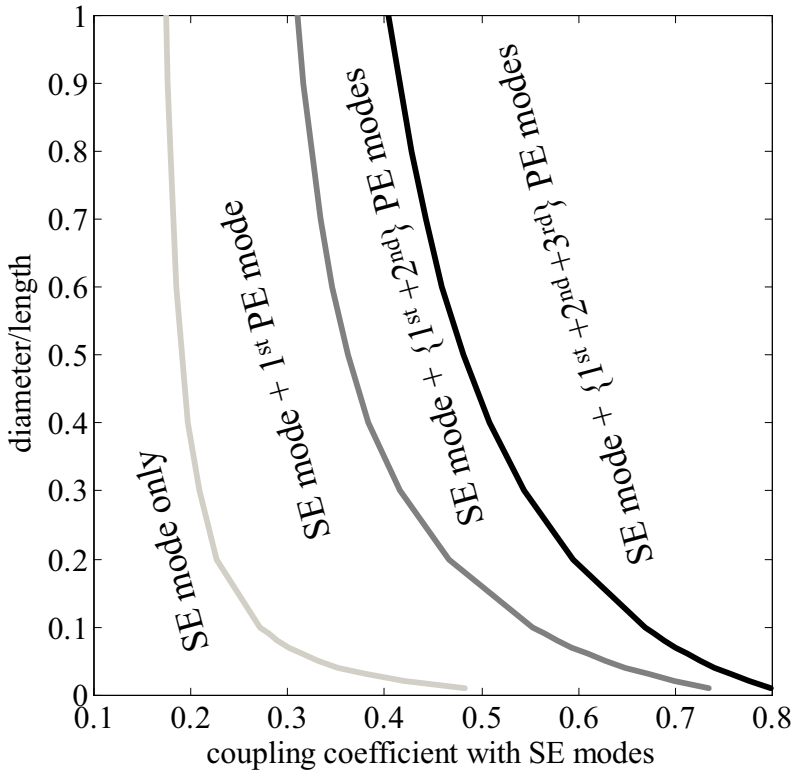


Figure 20. Relative error boundaries that define the required cylindrical CMBFs at 10 GHz (from copper two-parallel-conductor experiments.

the required number of PE modes.

2.2.2 Multi-Function Method (MFM)

In addition to the PE-mode order reduction, we can use simplified approximate integrals to reduce the computational cost of generating $\mathbf{Z_{ss}}$. Since the approximations are frequency-independent, the number of $\mathbf{Z_{ss}}$ elements to be calculated is reduced during a frequency sweep. Therefore, the computational effort of generating the dense matrix becomes that of generating a banded matrix.

When the two conductors are sufficiently separated (Figure 18), the variation of current density in conductors is negligible. Thus, the following thin-filament approximation can be used instead:

$$L_{i,j} = \frac{\mu}{4\pi} \int_{z_i} \int_{z_j} G(\vec{r_i}, \vec{r_j}) dz_j dz_i. \tag{34}$$

The integrand in the above double integral does not contain frequency-dependent

CMBFs and can be calculated analytically for any orientation of two straight conductor segments [30]. The accuracy of the thin-filament approximation is ensured when the distance between conductors is sufficiently large. The numerical experiments of two parallel cylinders with various dimensions show that the relative error of the thin-filament approximation from the exact integral depends on the aspect ratio of diameter to length of a cylinder, as in the case of the PE-mode order reduction. Figure 21 shows the boundary where the thin-filament approximation maintains the relative error less than 10^{-3}. The threshold pitch of using the frequency-independent approximations is usually higher than that of the controlling higher-order bases.

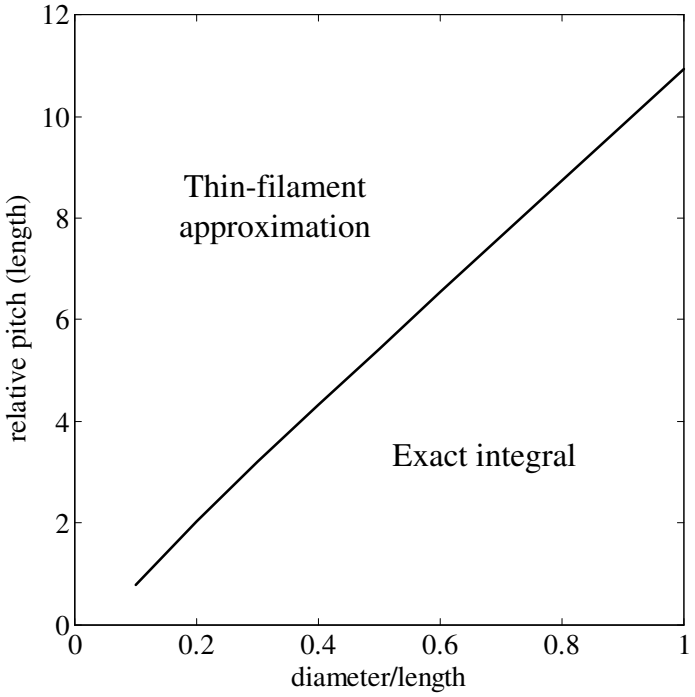


Figure 21. Error thresholds of using the thin-filament approximation as a function of diameter per length at 10 GHz.

For a conductor system occupying a very large dimension, the following center-to-center approximation [64] is also available:

$$L_{i,j} = \frac{\mu}{4\pi}\frac{l_i l_j}{R_{ij}}, \tag{35}$$

where l_i, l_j, and R_{ij} are the length of the i^{th} and the j^{th} conductor, and the distance

between the centers of the two conductors, respectively. From a similar numerical experiment, the relative pitch (w.r.t. length) where the center-to-center approximation is available is about 9.12, regardless of the cylinder lengths.

2.2.3 Implementation of Modeling Tool

Based on the discussed impedance calculation and efficiency enhancement schemes, we developed an inductance extraction tool called IPEX3D (Interconnection Parasitic Extractor for 3-D integration). The flowchart in Figure 22 shows how the procedures of controlling PE-mode bases and MFM are combined with the basic impedance computation routine.

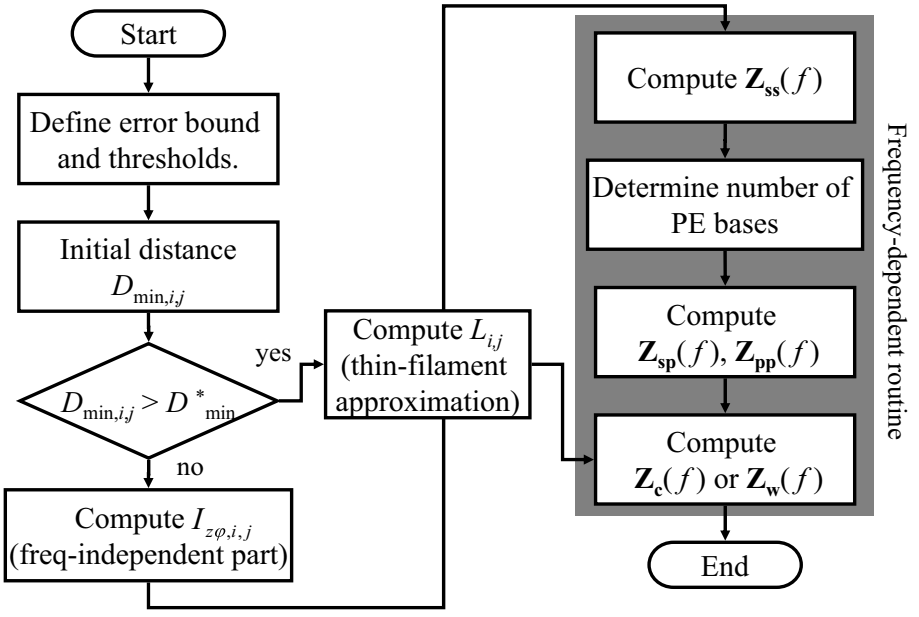


Figure 22. Flowchart of the 3-D inductance extraction tool.

In the beginning of the flowchart, the availability of using MFM is tested for every pair of conductors. If the distance between the conductors is larger than a defined threshold distance, the thin-filament approximate integral can be computed for frequency-independent mutual inductance. If the distance is not large enough for the approximation, sampled values of the frequency-independent integral $I_{z,\varphi}$ are computed before the frequency sweep simulation.

During the frequency sweep, impedances from SE modes ($\mathbf{Z_{ss}}$) are computed first. Initial coupling coefficients found from $\mathbf{Z_{ss}}$ determine the required number of PE-mode basis functions by using the diagram in Figure 20. The total number of PE-mode bases determines the size of $\mathbf{Z_{pp}}$ and $\mathbf{Z_{sp}}$, whose values are computed at the latter part of the frequency sweep. Finally, conductor and wire impedances $\mathbf{Z_c}$ and $\mathbf{Z_w}$ are found from the matrix equation (33).

In the later chapters, the IPEX3D will be extended to extract capacitive couplings from cylindrical interconnections and coupling from planar structures.

2.3 Validation

In this section, the accuracy of the proposed method is validated by a comparison with existing simulation tools. Additionally, the efficiency of the proposed method is demonstrated with its application to large interconnection structures. All simulations were performed using an Intel(R) Xeon 3 GHz CPU with 3.25 GB RAM.

2.3.1 Convergence Study with Two Parallel Cylindrical Conductors

As discussed in Section 2.1.2.1, the required number of basis function orders can be about two or three in usual interconnection problems. In this subsection, a simple example of two parallel cylinders shows a convergence characteristic with a small number of basis functions. Figure 23 illustrates the two parallel cylindrical conductors, where $D = 40\mu$m, $d = 30\mu$m, and $L = 100\mu$m. The ends of a conductor are grounded, and the impedances between the terminals of the other conductor were observed.

Figure 24 shows the resistance and inductance values of the structure in Figure 23 with an increasing number of basis function orders. As we increase the number of higher-order basis functions, the resistance and inductance values converge to the results that were computed in FastHenry. By using the method proposed in this chapter, the first and the second order PE-mode basis functions are sufficient to

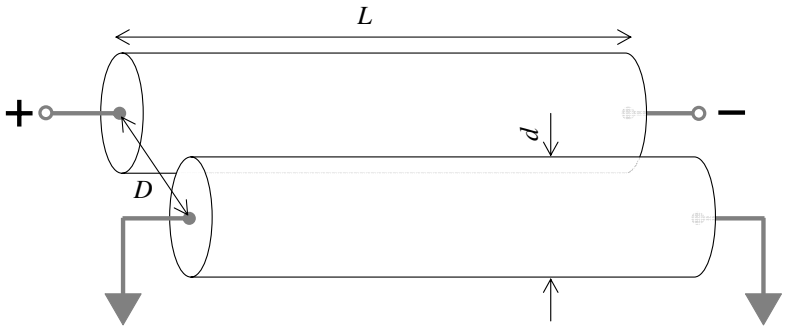
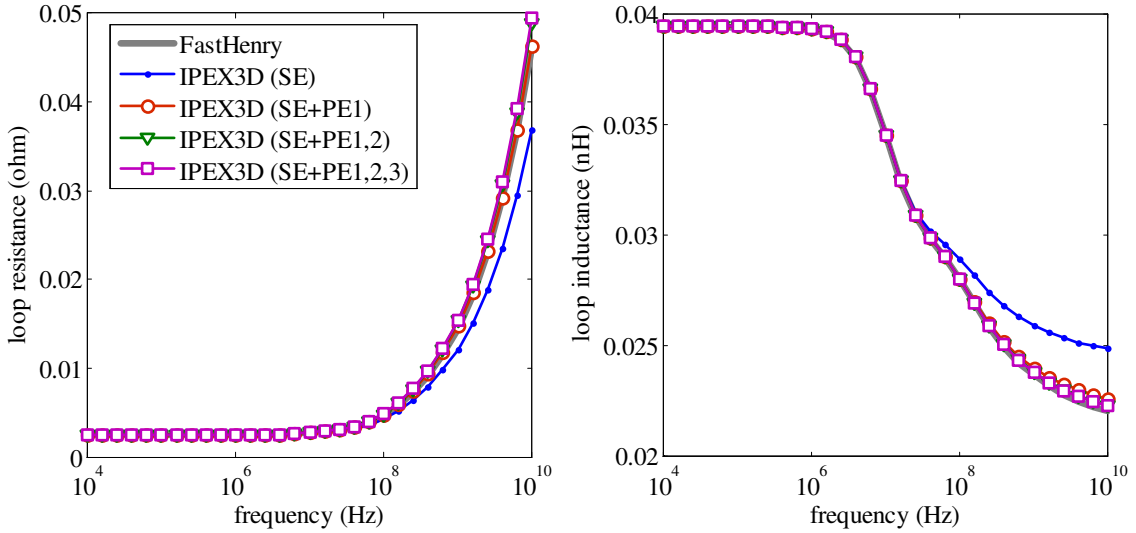


Figure 23. Geometry of two parallel cylindrical copper conductors with grounding and loop definitions.



(a) Resistances. (b) Inductances.

Figure 24. Loop resistances and inductances of cylindrical conductor with different uses of basis functions.

capture the accurate electrical parameters.

2.3.2 Accuracy Validation with Three Cylindrical Conductors

This subsection demonstrates simple three-conductor problems for evaluating the accuracy of the proposed approach. The test structure is shown in Figure 25, where two conductors (1 and 2) are connected at the far end with the other conductor grounded. Since the accuracy of the proposed method should be examined for arbitrary orientations of conductor segments, we applied variations in rolling angle (θ_R), yawing angle (θ_Y), and parallel shift (L_s) of the conductor 1.

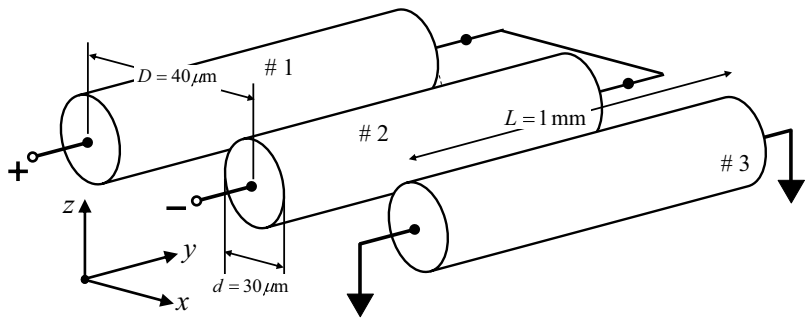


Figure 25. Geometry of three parallel cylindrical copper conductors. (Three parallel aligned cylinders.)

Loop resistances and inductances from these situations were compared with the results from FastHenry [49], which is an inductance extracting tool based on the PEEC method combined with the Fast Multipole Method (FMM). Since FastHenry uses brick-type filaments for modeling interconnection geometry, we constructed approximate cylinder model with the brick elements, as shown in Figure 26. For all the simulation cases, a logarithmic frequency sweep from 10^4 to 10^{10} Hz was used, and the total number of frequency points was 31. Figure 27 shows that the loop resistances and inductances obtained from the proposed method and FastHenry are well matched for all geometric variations. In Table 2 showing the relative accuracy of IPEX3D data (compared to FastHenry), the high-frequency error for loop resistances in the case of the shifted conductor is significant. It is because the conductor model used in IPEX3D does not capture accurately the proximity effect, which is concentrated in the overlapping regions of adjacent conductors. This error can be removed by increasing the number of segments along the axial direction (local Z directions in Figure 15).

As shown in Table 2, IPEX3D requires much less simulation time than FastHenry mainly because the number of basis functions is considerably small. The huge simulation times of FastHenry is due to the approximate discretization of the circular cross section, which may not be suitable for the optimal matrix computation, especially at high frequencies. The number of the required bases in IPEX3D varies with coupling

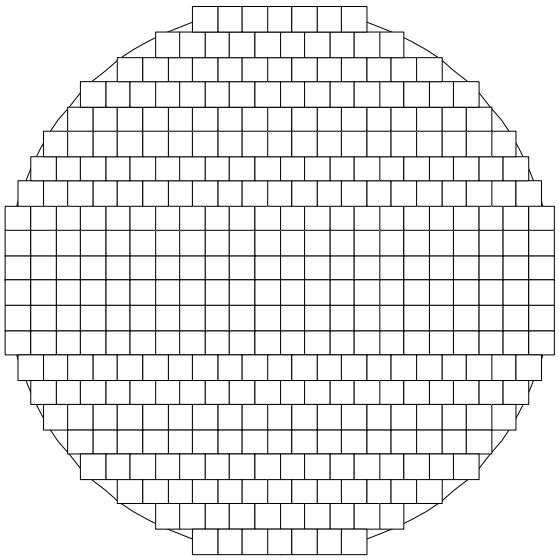
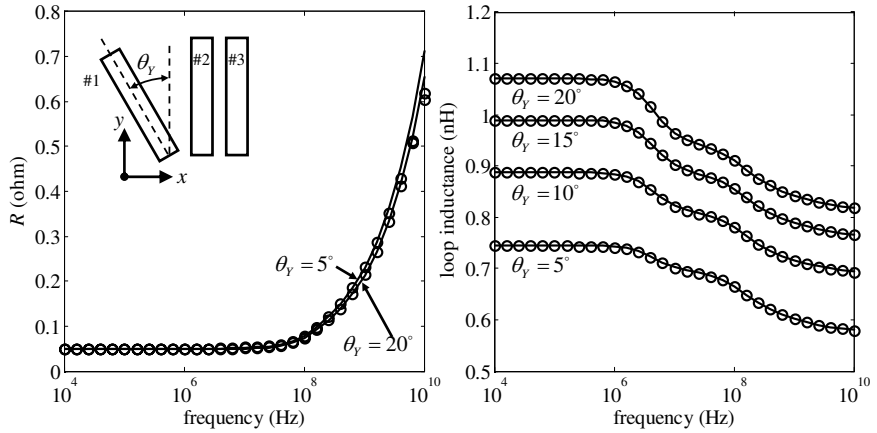


Figure 26. Discretized approximate model of cylindrical conductors in FastHenry. The number of bricks per cross section is 378.

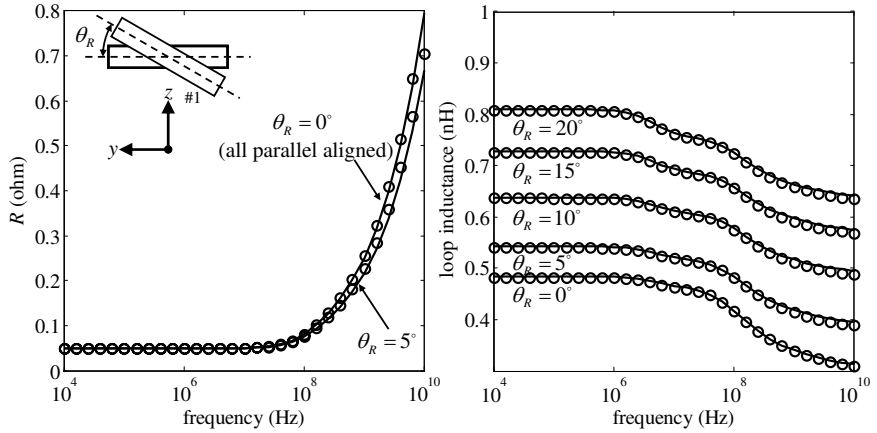
Table 2. Comparison of IPEX3D and FastHenry for three cylinder problem

		Total simulation time (sec.)[1]		Maximum relative error (%)[2]	
		FastHenry	IPEX3D	loop R	loop L
θ_R (deg.)	0	29065.0	860.9	3.01	0.92
	5	30213.5	1009.14	6.38	1.7
	10	22023.1	944.79	5.64	1.46
	15	17633.1	710.57	4.81	1.17
	20	15571.6	601.47	4.14	0.94
θ_Y (deg.)	5	9240.05	725.88	5.68	0.28
	10	5225.37	608.65	4.83	0.15
	15	10444.6	604.6	5.0	0.15
	20	9488.7	609.0	5.15	0.22
L_S (mm)	0.1	35840.1	878.22	5.23	2.19
	0.3	27670.5	510.22	7.59	2.87
	0.5	25928.3	616.84	11.37	2.88
	0.7	9134.4	509.40	1.76	0.19

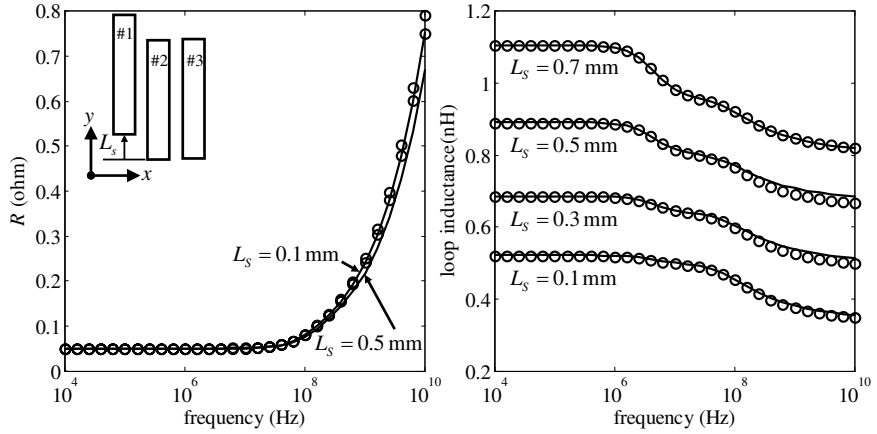
levels for different conductor orientations. In this example, up to seven basis functions (one SE mode and six PE modes) were required. The simulation time also depends on the geometric configuration, but the effect is small because the integrations involving conductor orientations are not related to frequency.



(a) Loop inductances with increasing θ_Y.



(b) Loop inductances with increasing θ_R



(c) Loop inductances with increasing L_s.

Figure 27. Loop resistances and inductances of cylindrical conductors with geometric variations of conductor 1. (circles: FastHenry, lines: IPEX3D)

2.3.3 Scalability Analysis with THV Array

This subsection shows required speed and memory for the modeling of the THV array in Figure 28 with increasing number of interconnections for two different pitches (30 and 50 μm). The THV array is a good configuration to perform the scalability analysis of the proposed method since it suffers from strong inductive couplings caused by the small pitch sizes. In addition, the electrical parameters of the THV array are useful for predicting the characteristics of emerging interconnection structures such as through silicon via (TSV) and ball grid array (BGA) interconnections.

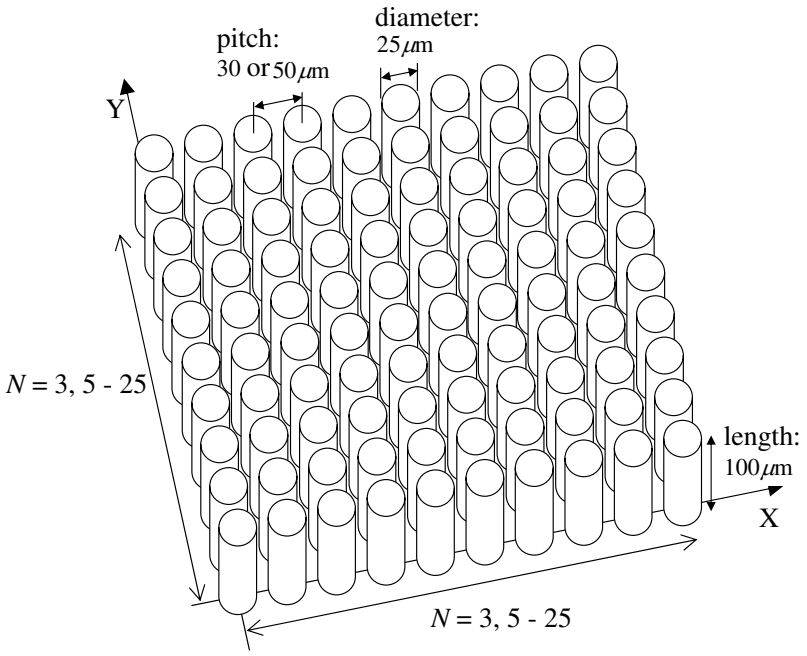
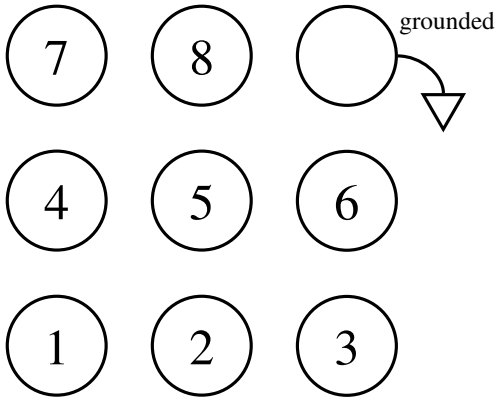
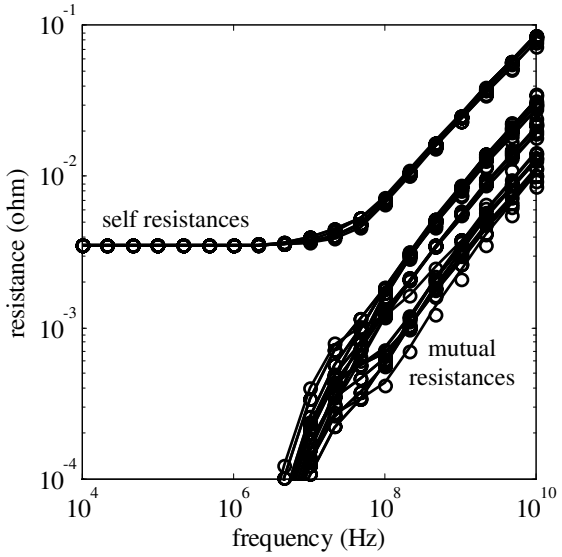


Figure 28. Copper THV array configuration.

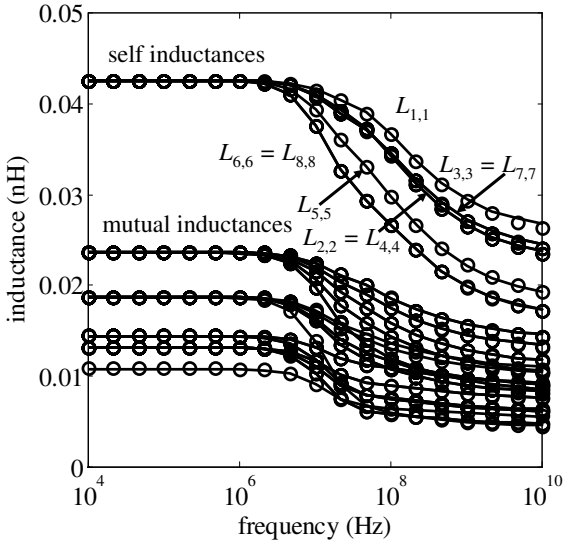
Before performing the scalability analysis, resistances and inductances of a simple 3-by-3 THV array with pitch of 30 μm was validated with FastHenry. Figure 29 shows all the inductance and resistance values, and Table 3 compares the performance of the two simulators. As in the case of the previous subsection, the number of basis functions in IPEX3D is much smaller than that in FastHenry, so the simulation time of IPEX3D is considerably smaller. The possible sources of error (based on matrix norm) of the IPEX3D results relative to FastHenry, which are less than 6.5% as shown



(a) Conductor index and ground definition.



(b) Resistances.



(c) Inductances.

Figure 29. Resistances and inductances of conductors in 3-by-3 THV array. (circles: FastHenry, lines: IPEX3D)

in Table 4, comes from the discretization of circular cross section in FastHenry. Table 5 shows required time for numerical integrations. The integration of self inductances needs more effort than that of mutual inductances, but the total time for computing all the mutual elements takes more time. For both self and mutual inductances, integration time increases with frequency.

Since the dominant factor that determines the simulation speed of the proposed method is the time for generating the system matrix, the scalability analysis is focused on the measured values of the number of non-zero elements, as shown in Figure 30

Table 3. Comparison of IPEX3D and FastHenry for 3-by-3 THV array problem

	FastHenry	IPEX3D
Number of frequency points	19	19
Number of basis functions[3]	378	5
Total simulation time (sec.)	7624.15	1199.27

Table 4. Relative matrix errors of IPEX3D to FastHenry (in %) for 3-by-3 THV array problem

	R	**L**
Average	1.52829	0.38416
Maximum	6.5434 (10 GHz)	1.3448 (10 GHz)

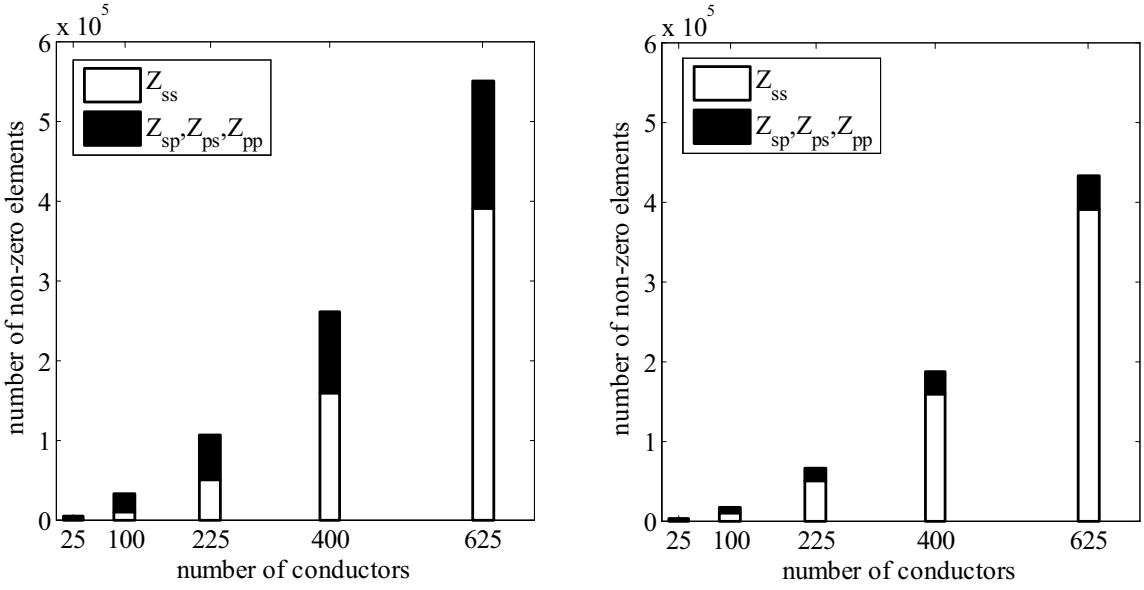
(a) for two different pitches. Although the submatrix $\mathbf{Z_{ss}}$ should be dense, controlling the number of PE-mode basis functions reduces the number of non-zeros in $\mathbf{Z_{pp}}$ and $\mathbf{Z_{sp}}$. The number of non-zero elements directly influences the time for generating the system matrix in Figure 30 (b), which indicates that the computation time of the proposed method is between $O(N^{1.6})$ and $O(N^{1.8})$, where N is the number of conductors.

The overall computational cost is actually a function of the strength of inductive coupling. Compared to the case of 30 μm pitch, the increased pitch (50 μm) requires much less simulation time. Although today's design trend is to reduce the pitch size among interconnections, the pitch of 50 μm between conductors with the interconnect diameter of 25 μm is sufficiently small in current technology.

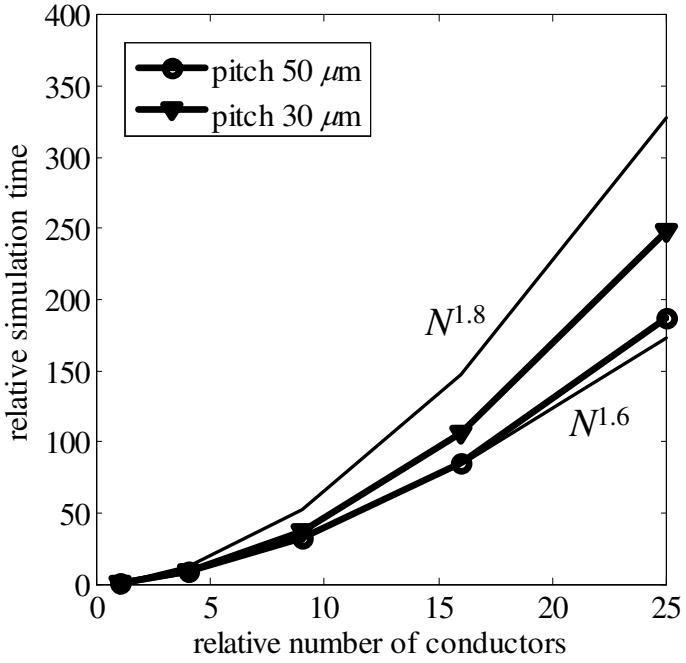
Figure 31 shows current density distribution of 20-by-20 THV array with an 'E'-shaped differential excitation. As frequency increases from 10^7 to 10^9 Hz, skin and proximity effects become dominant, resulting in current crowding along the boundary

Table 5. Numerical integration time of IPEX3D (in seconds/element) for 3-by-3 THV array problem

	Self inductance	Mutual inductance
Pre-computation	N/A	0.296
Frequency sweep (avg.)	0.806	0.131
Frequency sweep (max.)	1.422 (10 GHz)	0.406 (4.6 GHz)



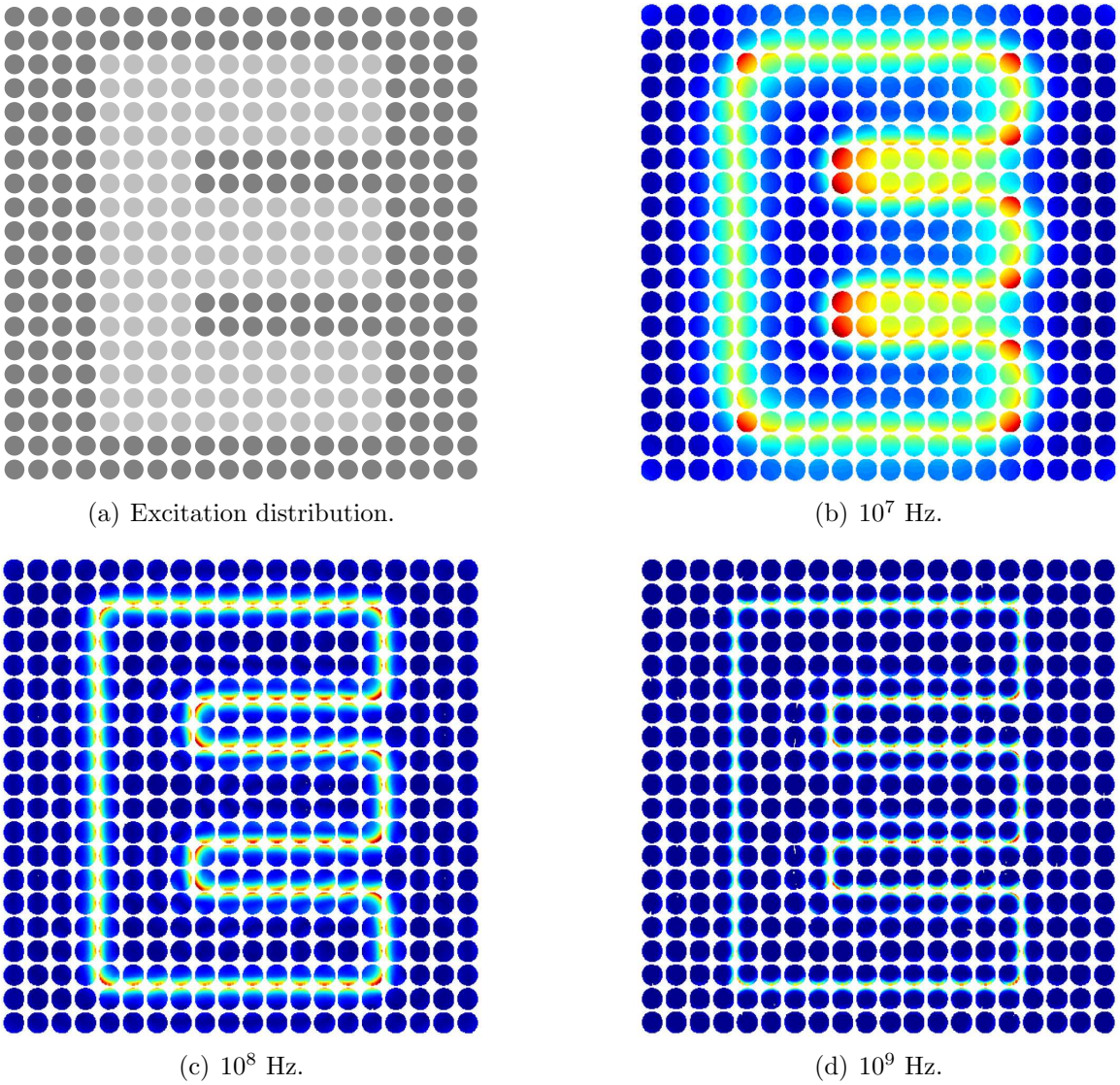
(a) Number of non-zero elements. (left: pitch 30 μm, right: pitch 50 μm)



(b) Total relative simulation time.

Figure 30. Scalability analysis of the proposed method with THV array model. The number of frequency points is 30.

of the differentially excited conductors. Figure 32 shows resistances and inductances of 19 diagonal conductors with an edge conductor grounded. Different proximity effects and ground effects make the large variety of high-frequency resistances and



(a) Excitation distribution.

(b) 10^7 Hz.

(c) 10^8 Hz.

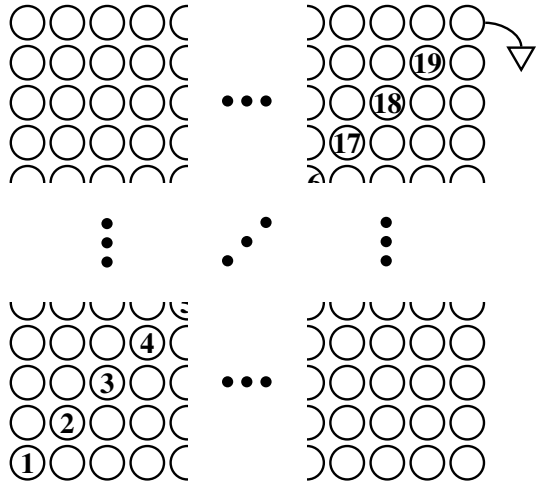
(d) 10^9 Hz.

Figure 31. A current density distribution at different frequencies in 20-by-20 THV array. Excitation voltages to the dark and the light parts of (a) are -1 and +1 volts, respectively.

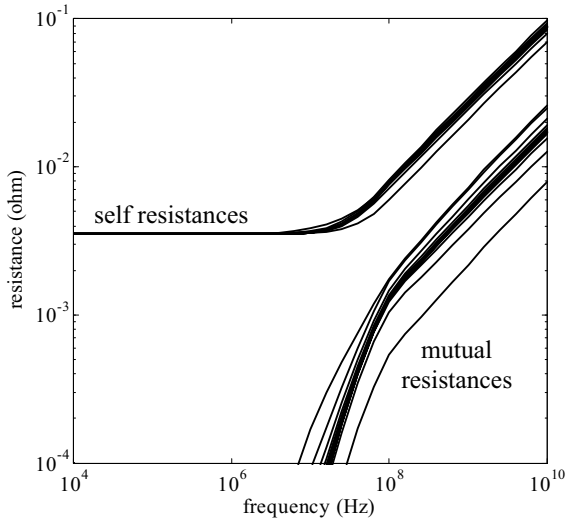
inductances.

2.4 Summary

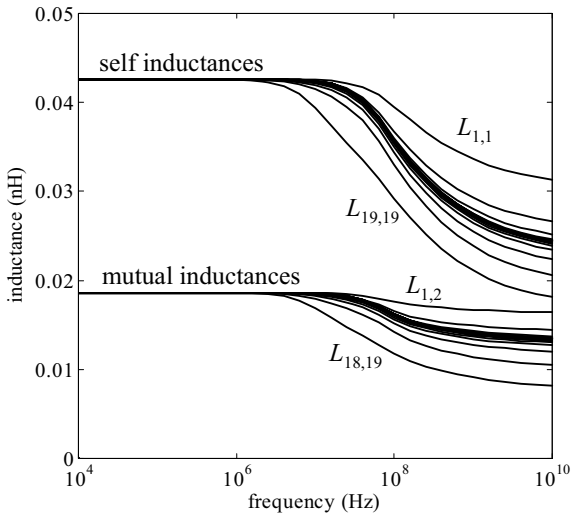
This chapter presented an efficient method for extracting the frequency-dependent resistance and inductance from a large number of interconnections that are used in today's 3-D packaging. Unlike currently available methods, the proposed method improves the efficiency by using cylindrical CMBFs, whose global property reduces



(a) Conductor index and ground definition.



(b) Resistances.



(c) Inductances.

Figure 32. Resistances and inductances of diagonal conductors in 20-by-20 THV array.

the size of the system matrix. In addition, the orthogonal property of the cylindrical CMBFs enables automatic capturing of current crowding caused by skin and proximity effects. This chapter discussed the application of such cylindrical CMBFs to the EFIE and provided details for computing partial resistances and inductances. Furthermore, we introduced two enhancement schemes for accelerating the computation of mutual inductances, so that the speed to fill the system matrices is improved to $O(N^{1.8})$, where N is the number of conductors. Finally, our developed modeling tool

based on the proposed method demonstrated good accuracy and capability for solving large 3-D interconnection structures. Therefore, the proposed method can be a possible solution to the industrial need for broadband electrical modeling of practical high-density interconnections arising in SiP or 3-D integration.

CHAPTER 3

CAPACITANCE AND CONDUCTANCE EXTRACTION OF CYLINDRICAL INTERCONNECTIONS FOR BROADBAND MODELING

Inductance and resistance of 3-D interconnections, which were discussed in the previous chapter, are major parasitic elements affecting the electrical behavior of interconnections. As frequency increases, however, the effect of capacitive coupling between interconnections becomes significant, so the interconnections behave like electrically long transmission lines. Moreover, when interconnections are surrounded by lossy dielectric materials, the loss tangent of the material causes signal attenuation as well. Thus, interconnection models should be constructed with accurate capacitive coupling between interconnections for ensuring broadband model accuracy.

This chapter proposes a method to extract the capacitance of cylindrical structures. The surface charge density distribution on a cylinder is approximated by the linear combination of global harmonic basis functions. In a manner similar to the R-L calculations in Chapter 2, a scalar potential integral equation (SPIE) is converted to an equivalent circuit equation, which relates charge and potential at each node of the interconnection. Since the capacitances can be modified by surrounding media such as a molding compound, the integral equations are re-considered to include the influence of homogeneous dielectric media.

The calculated shunt capacitances in this chapter and the series R-L model in the previous chapter together constitute a broadband interconnection model. The interconnection model is similar to an approximate transmission model that consists of a cascaded ladder network of series impedances and shunt capacitances. The complexity, or the number of parasitic elements of the interconnection model, depends on the maximum modeling frequency. The constructed model provides broadband network parameters, the examples of which will be shown in Chapter 4 and 5.

The following section introduces a group of global basis functions called the cylindrical accumulation mode basis functions (AMBFs) to capture the charge density distribution on a cylindrical conductor, and Section 3.2 discusses the formulation of SPIE with the cylindrical AMBFs in free space. Section 3.3 presents additional discussions regarding homogeneous dielectric media. Section 3.4 proposes the resultant equivalent RLC network and the procedure to obtain frequency-domain network parameters. For validation, Section 3.5 shows two examples to calculate capacitances and compares the capacitance values with analytic or numerical results.

3.1 Cylindrical AMBF

In a similar manner to the definition of cylindrical CMBFs for computing inductances and losses, we can define another set of global basis functions that capture the charge density distribution on the surface of a cylindrical conductor. The basic idea is that any the charge density distribution can be found from the electric scalar potential solution of Laplace's equation [65]:

$$\nabla^2 \phi = 0. \tag{36}$$

In cylindrical coordinates, the general solution of Laplace's equation is a function of all the coordinate variables (ρ,φ, and z). For example, a single cylinder has higher charge density distribution at the two edges of the cylinder [66, 67]. However, the charges crowding at the edges cancel each other when cylinders are concatenated, as in the case of bonding wires. In addition, since the variation over the axial coordinate (z) can be described by axial discretization, we can assume the axial variation constant and simplify Laplace's equation to the following two-dimensional form:

$$\frac{1}{\rho}\frac{\partial}{\partial \rho}\Big(\rho \frac{\partial \phi}{\partial \rho}\Big) + \frac{1}{\rho^2}\frac{\partial^2 \phi}{\partial \varphi^2} = 0. \tag{37}$$

The linear combination of all the solutions of (37) results in the following general expression for potential:

$$\begin{aligned}\phi(\rho,\varphi) &= C_1 \ln\rho + C_2 \\ &\quad + \sum_{n=1}^{\infty}\{\rho^n(A_n \sin n\varphi + B_n \cos n\varphi) + \rho^{-n}(A'_n \sin n\varphi + B'_n \cos n\varphi)\},\end{aligned} \tag{38}$$

where C_1, C_2, A_n, B_n, A'_n, and B'_n are all arbitrary constants. By applying (38) to the boundary condition of normal electric fields, the following expression for charge density distribution can be obtained:

$$\sigma = \hat{n}\cdot\epsilon_0\vec{E}\big|_{\text{conductorsurface}} = \hat{\rho}\cdot\epsilon_0\big(-\nabla\phi(\rho,\varphi)\big) = \sigma_0 + \sum_{n=1}^{\infty}\{\sigma_q \sin n\varphi + \sigma_d \cos n\varphi\}, \tag{39}$$

where σ_0, σ_d, and σ_q are undefined constants of surface charge density in $\mathrm{C/m^2}$. Equation (39) indicates that the surface charge density distribution on a cylinder is the linear combination of harmonic functions, which is identical to a Fourier series expansion. Thus, the capacitance extraction approach in this chapter becomes equivalent to MoM-based methods with harmonic basis functions [68, 69].

After finding normalization factors following a similar process as used with the cylindrical CMBFs, we can summarize the following surface modal basis functions:
Skin-effect (SE) mode ($n = 0$):

$$v_{l0} = \begin{cases} \frac{1}{a_{l0}} & \vec{r} \in S_l \\ 0 & \text{elsewhere} \end{cases}, \tag{40}$$

Proximity-effect, direct (PE-d) mode ($n > 0$):

$$v_{lnd} = \begin{cases} \frac{1}{a_{ln}}\cos(n\varphi_l) & \vec{r} \in S_l \\ 0 & \text{elsewhere} \end{cases}, \tag{41}$$

Proximity-effect, quadrature (PE-q) mode ($n > 0$):

$$v_{lnq} = \begin{cases} \frac{1}{a_{ln}}\sin(n\varphi_l) & \vec{r} \in S_l \\ 0 & \text{elsewhere} \end{cases}, \tag{42}$$

where n is the order of the basis function and S_l is the lateral surface of the conductor l. The parameter a_{ln} is the effective area used to normalize the surface integral of the basis functions over the surface S_l:

$$a_{ln} = \begin{cases} 2\pi\rho_l l_l & n = 0 \\ 4\rho_l l_l & n > 0 \end{cases}, \tag{43}$$

where ρ_l and l_l are the radius and the length of the conductor l, respectively. As in the classification of cylindrical CMBFs, direct and quadrature modes in the higher order bases are orthogonal to each other, and the linear combination of them describes arbitrary charge crowding caused by nearby conductors.

3.2 SPIE Formulation in Free Space

The AMBFs introduced in the previous section approximate the surface charge density distribution in SPIE, which means the contribution of charge density distribution to the potential at a testing point $\vec{r}$. SPIE can be written as follows:

$$\frac{1}{4\pi\epsilon_0}\int_{V'} G(\vec{r},\vec{r}')q(\vec{r}',\omega)dV' = \Phi(\vec{r},\omega), \tag{44}$$

where $q(\vec{r}',\omega)$ is volume charge density, $\Phi(\vec{r},\omega)$ is electric potential, and $G(\vec{r},\vec{r}')$ is Green's function. The retardation term in Green's function is assumed to be negligible. By inserting the approximation of charge density distribution $q = \sum_{n=0}\{Q_{knq}v_{knq}\}$ to (44) and applying the following inner product:

$$\langle v_{lmd}(\vec{r},\omega), x\rangle = \int_S v_{lmd}(\vec{r},\omega)x\mathrm{d}S, \tag{45}$$

we can obtain the following equation that relates surface charges and conductor potentials:

$$\sum_{n,q} Q_{knq}P_{lmd,knq} = V^k_{lmd}, \tag{46}$$

where k and l are conductor indices,

$$P_{lmd,knq} = \frac{1}{4\pi\epsilon_0}\int_{S_l}\int_{S_k} v_{lmd}(\vec{r_l})v_{knq}(\vec{r_k})\frac{1}{|\vec{r_l}-\vec{r_k}|}dS_k dS_l$$

is the partial coefficient of potential (F^{-1}), and

$$V_{lmd}^{k} = \int_{S_l} \Phi_k(\vec{r_l}) v_{lmd}(\vec{r_l}) d\vec{S_l}$$

is the modal voltage on the conductor surface due to the coupling of the k^{th} conductor. The modal voltage, which is the potential value relative to the ground at infinity, must be distinguished from the modal voltage difference (32) between two nodes on conductors.

The computation of the partial coefficient of potential $P_{lmd,knq}$ involves integrals over four variables (φ_l, φ_k, z_l, and z_k). Since the integrals have the same form as those of the partial inductances (24), we can use the techniques in Section 2.1.2.2, where analytic integrals over the axial variables (z_l and z_k), the coordinate transform of angular variables, and numerical quadratures are discussed.

Since cylindrical AMBFs are scalar surface functions, the partial coefficient of potential does not include the integrals over radial variables. The independency to the radial variable reduces the computational cost for applying the numerical quadrature rule. In addition, cylindrical AMBFs do not depend on frequency, so frequency sweep is not necessary. Therefore, the required cost for computing integrals involving cylindrical AMBFs is much lower than the cost for computing CMBF-based integrals.

The modal voltage V_{lmd}^{k} in (46) also shows similar properties to the modal voltage difference for fundamental and higher-order mode basis functions in (32). When an AMBF is in the fundamental mode ($m = 0$), the integral over the lateral surface becomes unity, so V_{lmd} equals to the actual nodal voltage Φ_l. When the AMBF is one of higher-order mode harmonic functions ($m > 0$), the integral becomes zero. Thus, the equivalent network of modal coefficients of potential is composed of the fundamental-order capacitive coupling among conductor nodes and higher-order capacitive coupling from the closed loops. The details of the construction of combined equivalent circuit will be discussed in Section 3.4.

3.3 Consideration of Homogeneous Media

In the previous section, the surrounding medium of interconnections was assumed to be free space ($\epsilon = \epsilon_0$). The free space assumption is valid when interconnections are exposed for measurement, but the real environment for 3-D interconnections is usually filled with various packaging or substrate materials. For example, bonding wire interconnections are usually submerged in molding compounds, and vertical interconnections are fabricated in multilayered substrates using organic, ceramic, and silicon materials.

Most of the packaged interconnection applications are based on inhomogeneous media, which includes the combination of various materials and free space. To consider inhomogeneous media in integral equations, we need to use a special type of Green's functions such as the multilayered Green's function. In this thesis, only the homogeneous media is considered. For example, the molding compound surrounding bonding wires can be assumed to be a homogeneous media since the size of the molding region is large relative to the size of the entire wire structure.

3.3.1 Vector and Scalar Potentials

When the retardation term is neglected, the permittivity is shown in SPIE (44) but is not apparently involved EFIE (21). Thus, replacing the free space permittivity (ϵ_0) by a dielectric background permittivity ($\epsilon_0\epsilon_B$) seems to be sufficient for modeling interconnections in a homogeneous dielectric media [70]. However, the permittivity difference also influences the EFIE (21) if the background is not free space. To clarify the effect of the permittivity term in EFIE, we need to reconsider Maxwell's equation for modifying the formulation.

At first, the displacement current term in Ampere's law can be rewritten as follows:

$$\begin{aligned} \nabla \times \vec{H} &= \vec{J}^C + \epsilon_r \epsilon_0 j\omega \vec{E} \\ &= \vec{J}^C + [\epsilon_0(\epsilon_r - \epsilon_B)] j\omega \vec{E} + \epsilon_0 \epsilon_B j\omega \vec{E}, \end{aligned} \tag{47}$$

where ϵ_r is the relative permittivity of an interconnection, and ϵ_B is the relative permittivity of the background media. Similar to the free-space media case [48], we can define the following total current, which is composed of conduction current due to free charge and equivalent polarization current due to dielectrics:

$$\vec{J} = \vec{J}^C + [\epsilon_0(\epsilon_r - \epsilon_B)]j\omega\vec{E}. \tag{48}$$

It is important to note that the polarization current is nonzero even in conductors having free-space permittivity (ϵ_0) since the background media is not free space. In the equivalent circuit model, an excessive capacitance represents this effect. Inserting the total current density, the following vector Helmholtz equation is obtained:

$$\nabla^2\vec{A} - \mu\epsilon_0\epsilon_B(j\omega)^2\vec{A} = -\mu\vec{J}. \tag{49}$$

In the homogeneous dielectric media, Gauss' law can be written as follows:

$$\nabla \cdot \vec{E} = \frac{q^T}{\epsilon_0\epsilon_B}, \tag{50}$$

where $q^T = q^F + q^B$ is total charge density, q^F is free charge density, and q^B is bound charge density. By using this total charge density as an excitation term, the following scalar Helmholtz equation is derived:

$$\nabla^2\Phi - \mu\epsilon_0\epsilon_B(j\omega)^2\Phi = -\frac{q^T}{\epsilon_0\epsilon_B}. \tag{51}$$

The solutions to the vector and scalar Helmholtz equations (49, 51) are the following vector and scalar potentials:

$$\vec{A} = \frac{\mu}{4\pi}\int_{v'} G(\vec{r},\vec{r'})\vec{J}(\vec{r'})dv'. \tag{52}$$

$$\Phi = \frac{1}{4\pi\epsilon_0\epsilon_B}\int_{v'} G(\vec{r},\vec{r'})q^T(r')dv'. \tag{53}$$

If the exact form of Green's function $G(\vec{r},\vec{r'})$ is used, the non-free-space medium permittivity ϵ_B is also included in the retardation term ($e^{-jk|\vec{r}-\vec{r'}|}$) of (52) and (53).

If the media is lossy, the attenuation in the retardation term may not be negligible even under the assumption that the interconnection structure is electrically small. However, when the media is lossless, we can neglect the retardation term and the effect of the media permittivity on the Green's function.

Since the difference of scalar potential equation (53) and (44) is the addition of the non-free-space media permittivity, the capacitive coupling between interconnections in the background dielectric media can be calculated in the same way as discussed in Section 3.2. However, we have to modify the construction of the voltage equation from the vector potential integral equation (52), since the total current contains the polarization current.

3.3.2 Equivalent Circuit Model of Conductor

In a conductor, the total electric field is contributed by the conduction current $\vec{J^C}$ (Ohm's law) and inductive coupling. When the background media is not free space, total current $\vec{J}$ is not reduced to the conduction current only, but also has the polarization current term. Therefore, the integral equation is expressed as follows:

$$\frac{\vec{J^C}}{\sigma} + j\omega\frac{\mu}{4\pi}\int_{v'} G(\vec{r},\vec{r'})\vec{J^C}(\vec{r'})dv' + j\omega\frac{\mu}{4\pi}\int_{v'} G(\vec{r},\vec{r'})\epsilon_0(\epsilon_r-\epsilon_B)j\omega\vec{E}dv' = -\nabla\Phi. \quad (54)$$

In the above equation, the two current terms in the two integrals are coupling terms from conduction current and polarization current from all of the interconnections.

Approximating the conduction current with the cylindrical CMBFs and applying inner product based on Galerkin's method, we obtain the following voltage equation:

$$R_{imd}I_{imd} + j\omega\sum_{j,n,q} L_{imd,jnq}I_{jnq} + j\omega\sum_{j,n,q} L_{imd,jnq}[j\omega R_{jnq}C^{ex}_{jnq}I_{jnq}] = V_{imd}, \quad (55)$$

where

$$\begin{aligned} R_{imd} =& \frac{1}{\sigma}\int_{V_i}\vec{w}^*_{imd}\cdot\vec{w}_{imd}dV_i, \\ L_{imd,jnq} =& \frac{\mu}{4\pi}\int_{V_i}\int_{V_j} G(\vec{r_i},\vec{r_j})\vec{w}^*_{imd}\cdot\vec{w}_{jnq}dV_jdV_i, \\ C^{ex}_{jnq} =& \frac{\epsilon_0(\epsilon_r-\epsilon_B)}{\int_{V_j}\vec{w}^*_{jnq}\cdot\vec{w}_{jnq}dV_j}, \end{aligned}$$

and

$$V_{imd} = -\int_{S_i} \Phi(\vec{r_i})\vec{w}^*_{imd}(\vec{r_i},\omega)\cdot d\vec{S_i}.$$

In (55), all the modal partial resistances and inductances and the voltage differences remain the same as derived in Chapter 2, and the added excess capacitance term C^{ex}_{jnq} represents the polarization current in the interconnection. The voltage equation (55) can be expressed by the equivalent circuit model shown in Figure 33, where the modal current I_{imd} flows across the partial resistance.

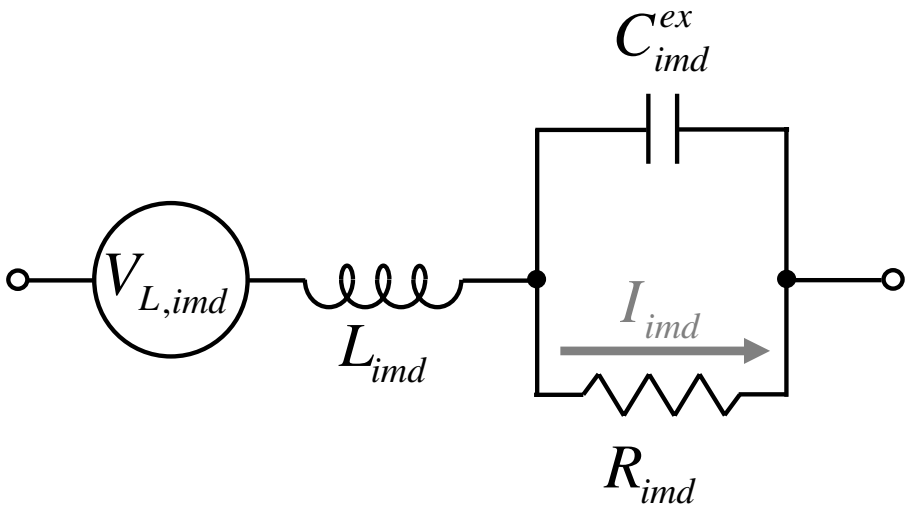


Figure 33. Equivalent circuit model including excess capacitance. $V_{L,imd}$ **represents the voltage drop through inductive coupling.**

To check the significance of the excess capacitance, the equivalent impedance of the parallel R-C network is considered as follows:

$$\begin{aligned} Z_{RC} =& \frac{R}{1+j\omega RC^{ex}} \\ =& \frac{R}{1+j\omega\frac{1}{\sigma}\int_{V_i}\vec{w}^*_{imd}\cdot\vec{w}_{imd}dV_i \times \frac{\epsilon_0(\epsilon_r-\epsilon_B)}{\int_{V_j}\vec{w}^*_{imd}\cdot\vec{w}_{imd}dV_i}} \\ =& \frac{R}{1+j\omega\frac{\epsilon_0(\epsilon_r-\epsilon_B)}{\sigma}}. \end{aligned} \tag{56}$$

In case of good conductors such as copper and gold, the term $j\omega\epsilon_0(\epsilon_r-\epsilon_B)/\sigma$ is very small in the typical frequency range of interest. For example, if gold bonding wires are used in a typical molding compound ($\epsilon_B = 4.3$), the frequency where the magnitude

of $j\omega\epsilon_0(\epsilon_r - \epsilon_B)/\sigma$ becomes 0.1 is

$$\begin{aligned} f =& 0.1 \times \frac{1}{2\pi}\Big|\frac{\sigma}{\epsilon_0(\epsilon_r - \epsilon_B)}\Big| = 0.1 \times \frac{1}{2\pi} \times \Big|\frac{4.1 \times 10^7}{8.854 \times 10^{-12} \times (1 - 4.3)}\Big| \\ =& 2.23 \times 10^{16}\text{Hz}. \end{aligned} \tag{57}$$

The effect of the excess capacitance appears at considerably high frequencies, which means the charge relaxation time is negligible in the typical frequency ranges, where package structures are currently used. Therefore, we can omit the the excess capacitance of the interconnection branch and use the original equivalent circuit constructed in Chapter 2.

3.3.3 Consideration of Dispersive Media

As discussed in the previous subsections, we can observe the effect of dielectric media surrounding interconnections by using dielectric permittivity in the SPIE (53). Using (53) is still valid when the background media is a dispersive media, which is expressed by a complex-valued function of frequency. In this case, the resultant equivalent potential coefficients become frequency-dependent complex numbers, so the equivalent network is composed of capacitances and conductances.

3.4 Broadband Equivalent Circuit (RLC Network)

The combination of calculated potential coefficients (Section 3.2) and series R-L in the previous chapter can be used to construct the equivalent network of the interconnection structure, and the resulting equivalent model can cover a wide frequency band by subdividing interconnections along the axial direction. This section discusses the procedure to establish an equivalent RLC network and to compute multi-port network parameters.

The initial step to extract an equivalent model of a given interconnection is to set the maximum modeling frequency, which determines the required number of inductive and capacitive cells along the axial direction. The initial number of cells is determined

by the geometrical model input, but the length of the generated cell from the geometry can be electrically long at the maximum frequency. In this case, the initial cell is divided into additional subcells, the length of which is less than

$$lc_{max} = \frac{\lambda_r c}{\sqrt{\epsilon_B} f_{max}}, \tag{58}$$

where lc_{max} is the maximum cell length, λ_r is the wavelength ratio, $c = 3 \times 10^8$(m/s) is the velocity of light in free space, ϵ_B is the relative permittivity of the background media, and f_{max} is the maximum modeling frequency. The parameter λ_r is defined to ensure the cell length is sufficiently small at the modeling frequency. If $\lambda_r = 0.05$, the maximum cell length should be less than 1/20th of the wavelength at the maximum frequency. Since the maximum cell size lc_{max} is proportional to the inverse of the maximum frequency, the complexity of a interconnection problem increases with frequency. For example, the size of global impedance matrix becomes four-times larger if the maximum modeling frequency is doubled, as discussed in Section 2.1.2.1.

Figure 34 shows how inductive and capacitive cells are generated. Each inductive cell defines the volume current flowing through the cross section of the interconnection, and each capacitive cell defines the surface charge on the lateral surface of the interconnection. Figure 34 illustrates that the volume inductive cells and the surface capacitive cells overlap each other, so they establish an RLC network like the lumped-element approximation of transmission lines. Placing small capacitive cells at the ends of interconnections enables capturing charge density crowding at the ends of interconnections.

From the defined discretization, partial resistance, partial inductance, and partial coefficients of potential between modal basis functions are calculated by using (24) and (46), and voltage equations can be obtained as shown in the following matrix form:

$$\begin{pmatrix} \mathbf{Z_{ss}} & \mathbf{Z_{sp}} \\ \mathbf{Z_{ps}} & \mathbf{Z_{pp}} \end{pmatrix} \begin{pmatrix} \mathbf{I_s} \\ \mathbf{I_p} \end{pmatrix} = \begin{pmatrix} \mathbf{\Delta V_i} \\ \mathbf{0} \end{pmatrix}. \tag{59}$$

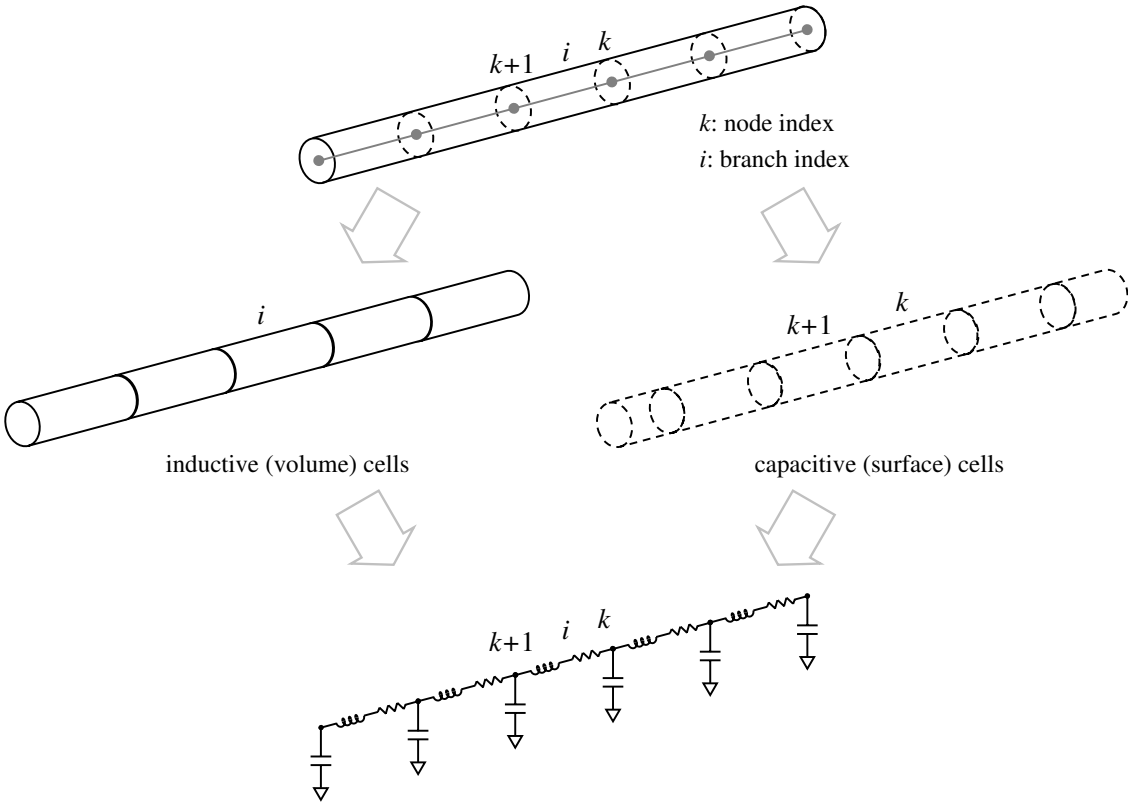


Figure 34. Axial cell discretization and the generation of RLC equivalent circuit model. (Mutual coupling terms are omitted for simplicity.)

$$\begin{pmatrix} \mathbf{P_{ss}} & \mathbf{P_{sp}} \\ \mathbf{P_{ps}} & \mathbf{P_{pp}} \end{pmatrix} \begin{pmatrix} \mathbf{Q_s} \\ \mathbf{Q_p} \end{pmatrix} = \begin{pmatrix} \mathbf{V_i} \\ \mathbf{0} \end{pmatrix}. \tag{60}$$

Equation (59) is the identical to (33) in Chapter 2. Equation (60) represents the relation of charge and modal scalar potential, which was discussed in Section 3.2. The above voltage equations are expressed in Figure 35 for a two-bonding wire example, where the R-L and the C circuitry are drawn separately for clarity. In a capacitance network, the self potential coefficient from the SE mode is attached at the physical node of the original interconnection, and the higher-order mode potential coefficients form grounded loops. Since the potential coefficients are independent of frequency, this capacitance equivalent model can be reduced to the capacitance matrix that does not show the higher-order mode loops explicitly.

The connection of the series R-L's and the shunt C's in Figure 35 is based on the

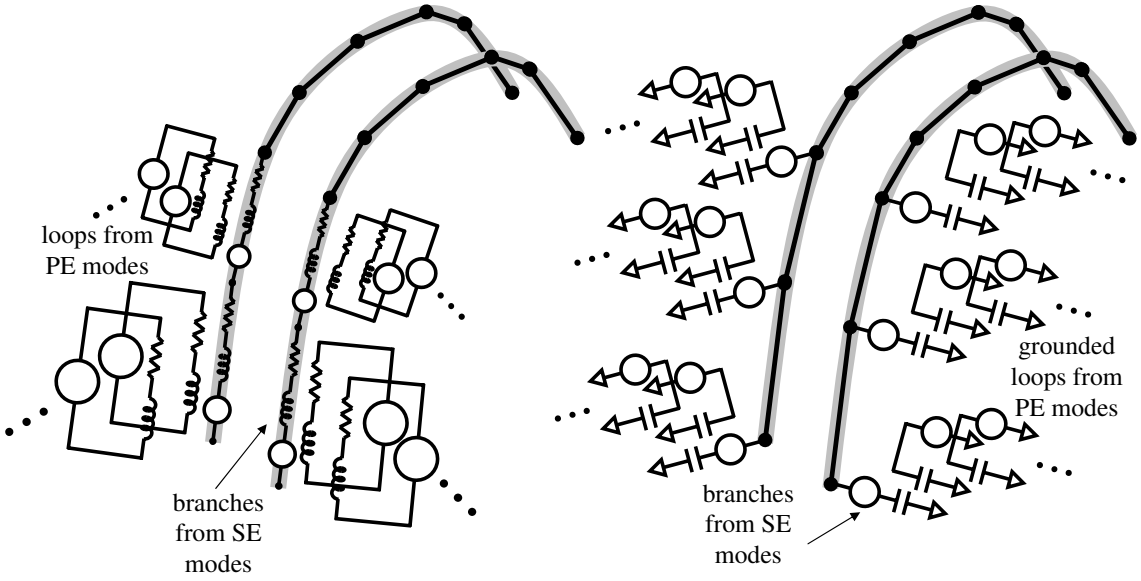


Figure 35. Modal RLC equivalent circuit model of two bonding wires. RL network and C network are separated for clarity.

following approximate matrix form of the continuity equation or Kirchhoff's Current Law (KCL) for each node:

$$\begin{pmatrix} -\mathbf{E} & \mathbf{\Delta_I} \\ \mathbf{0} & \end{pmatrix} \begin{pmatrix} \mathbf{I_t} \\ \mathbf{I_i} \end{pmatrix} + j\omega \mathbf{Q_s} = \mathbf{0}, \tag{61}$$

where $\mathbf{I_t}$ is a terminal current vector, $\mathbf{I_i}$ is an internal current vector, $\mathbf{E}$ is an identity matrix, and $\mathbf{Q_s}$ is the SE-mode charge vector. The internal current vector $\mathbf{I_i}$ is identical to the SE-mode current vector $\mathbf{I_s}$. $\mathbf{\Delta_I}$ contains the information of incoming and outgoing currents for each node. The matrix form of the continuity equation and the voltage equations (59, 60) constitute the entire matrix equation to compute the network parameters of the equivalent circuit. The terminal current $\mathbf{I_t}$, a known variable representing the excitation condition, appears on the right side of the following

combined matrix equation.

$$\begin{pmatrix} \mathbf{Z_{ss}} & \mathbf{Z_{sp}} & -\mathbf{\Delta_V} & \mathbf{0} & \mathbf{0} \\ \mathbf{Z_{ps}} & \mathbf{Z_{pp}} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{\Delta_I} & \mathbf{0} & \mathbf{0} & j\omega\mathbf{E} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & -\mathbf{E} & \mathbf{P_{ss}} & \mathbf{P_{sp}} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{P_{ps}} & \mathbf{P_{pp}} \end{pmatrix} \begin{pmatrix} \mathbf{I_s} \\ \mathbf{I_p} \\ \mathbf{\Phi_t} \\ \mathbf{\Phi_i} \\ \mathbf{Q_s} \\ \mathbf{Q_p} \end{pmatrix} = \begin{pmatrix} \mathbf{0} \\ \mathbf{0} \\ \mathbf{I_t} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \end{pmatrix}. \tag{62}$$

In the above equation, $\mathbf{\Delta_V}$ contains the information of voltage differences for each branch. $[\mathbf{\Phi_t}\mathbf{\Phi_i}]^T$ and $\mathbf{Q_s}$ are re-arranged to collect the terminal variables, so a permutation matrix multiplies $\mathbf{\Delta_V}$, $\mathbf{P_{ss}}$, $\mathbf{P_{sp}}$, and $\mathbf{P_{ps}}$. The solutions $\mathbf{\Phi_t}$ of (62) for each terminal current excitation provides the Z-parameter matrix $\mathbf{Z}$, which can be converted to an S-parameter matrix $\mathbf{S}$ using the following relation [71].

$$\mathbf{S} = \big(\mathbf{Z} + Z_0\mathbf{E}\big)^{-1}\big(\mathbf{Z} - Z_0\mathbf{E}\big), \tag{63}$$

where Z_0 is a characteristic impedance. Examples of using the combined RLC network to obtain S-parameters of bonding wires and TSV interconnections will be shown in the next two chapters.

3.5 Capacitance Computation Examples

This section presents two examples to validate the capacitance computation approach proposed in Section 3.1 and 3.2. The first example is the calculation of even- and odd-mode capacitances of three conductors in parallel [68]. The second example is the calculation of the turn-to-turn stray capacitance of a solenoidal coil inductor [72], which is a rather complicated 3-D structure.

3.5.1 Even- and Odd-Mode Capacitances of a Triplex Cable

Figure 36 shows the configuration of three cylindrical conductors in parallel. This structure represents a typical low-voltage indoor triplex cable used for electric power

transmission in buildings, where two of the conductors are active and the third cable is grounded [68]. In this case, the following analytic expression of capacitance between two parallel cylindrical conductors is not accurate since it does not consider the proximity effect from the third conductor.

$$C = \frac{\pi\epsilon}{\cosh^{-1}\frac{d}{2R}}, \tag{64}$$

In (64), d is the distance between two cylinders and R is the radius of each conductor, as shown in Figure 36. By using the cylindrical AMBF-based approach, this section shows even- and odd-mode capacitances for varying distances of the third conductor from the center of the other two conductors. The capacitance calculation results will be compared with the results from a similar analytic approach using harmonic functions [68].

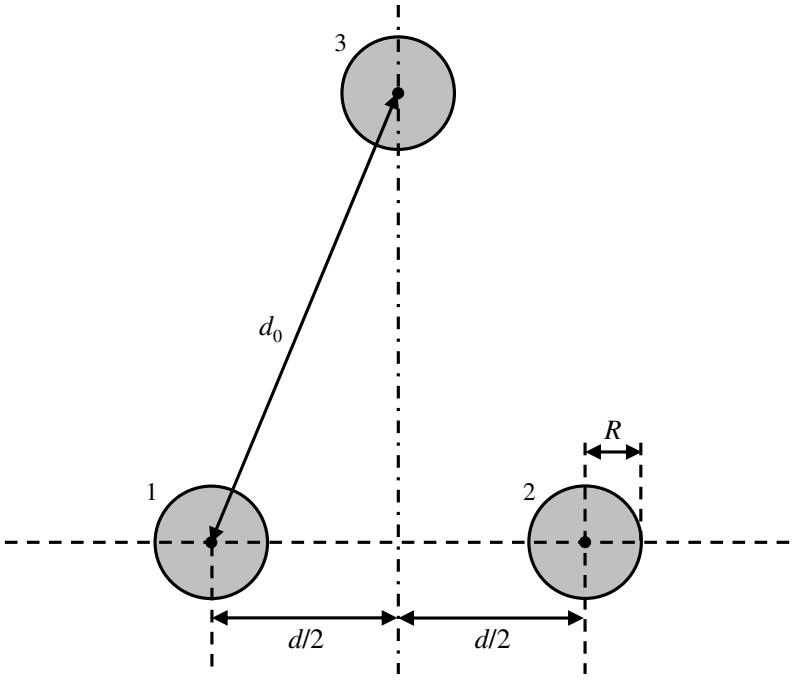


Figure 36. Three conductors in parallel.

The first example is the capacitance between two parallel cylinders, defined by the analytic expression in (64). The analytic formula was compared with the calculated values of capacitance between two cylinders, which can be found by using the following

definition of odd-mode capacitance:

$$C_{odd} = \left.\frac{q_1}{V_1 - V_2}\right|_{q_1=-q_2,q_3=0}, \tag{65}$$

where q_i and V_i $(i = 1, 2, 3)$ are the total charge and the voltage on each conductor, respectively. Figure 37 compares the calculated odd-mode capacitances with the analytic expression while varying the distance of the grounded third conductor. As expected, the odd-mode capacitance converges to the value of (64) when the grounded conductor is sufficiently far away. On the other hand, the calculated capacitance value is about twice the analytic capacitance value when the charge proximity effect is significant.

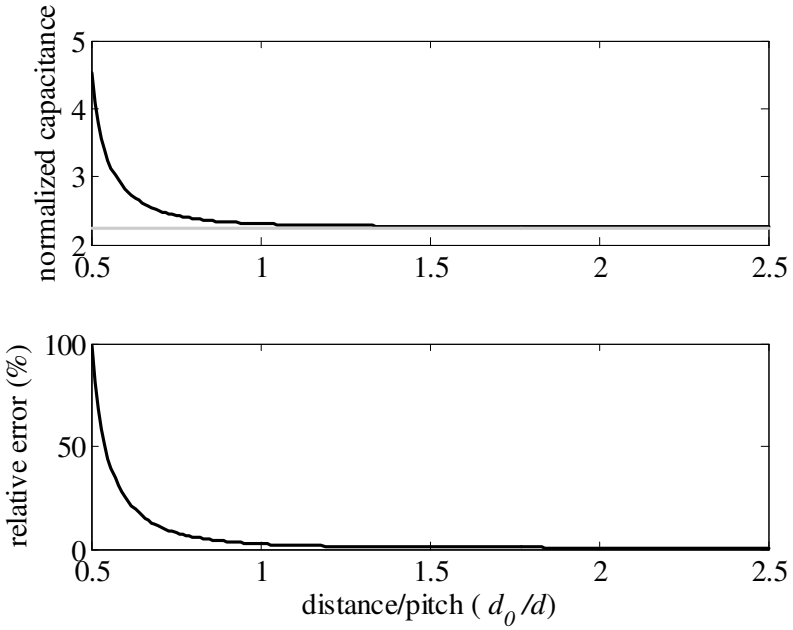


Figure 37. Comparison of calculated odd-mode capacitances (black) and the analytic results (grey) with increasing distance of the conductor 3.

Figure 38 shows the elements of the capacitance matrix and the even-mode capacitance, which is defined as follows:

$$C_{even} = \left.\frac{2q_1}{V_1 - V_3}\right|_{q_1=q_2,q_3=-2q_1}. \tag{66}$$

All the calculated values obtained by using the cylindrical AMBFs are matched well with the calculated data in [68] because both methods are based on the expression

of charge density distribution on cylinders using a linear combination of harmonic functions. As the distance of the third conductor increases, the variation of each capacitance becomes small.

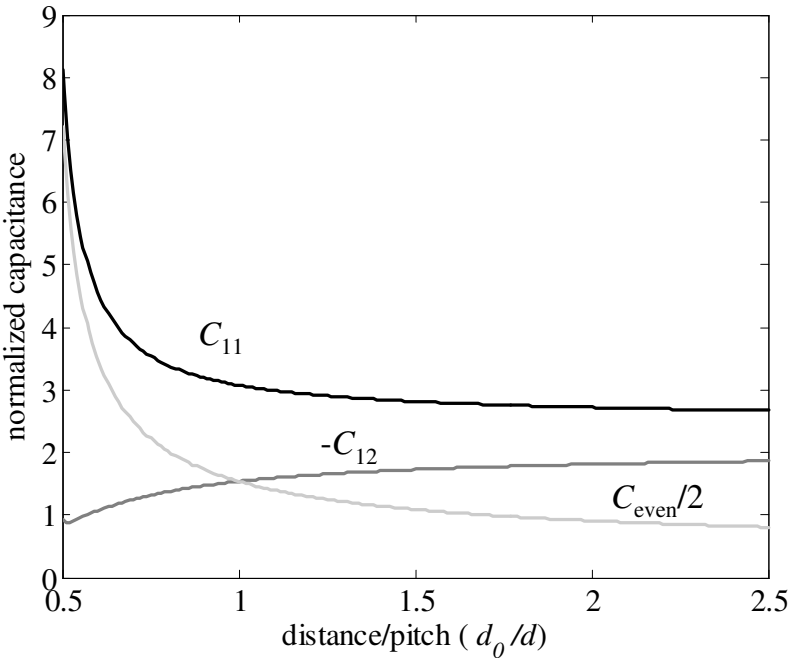


Figure 38. Elements of the capacitance matrix and the even-mode capacitance of the three conductor structure with increasing distance of the conductor 3.

In Figure 39, the distance of the third conductor is fixed to $d_0 = d$, and the odd-mode capacitances are calculated with different radii of conductors. Compared to the plots in [68], the calculated capacitance values are accurate when $d/R \geq 2.5$. The difference comes from using different number of basis functions. The maximum order of the AMBFs used in the calculation is three, however, basis functions up to the 15^{th} order may be necessary to obtain accurate results when $d/R \leq 2.5$. It is important to note that $d/R = 2.5$ is already a sufficiently small pitch in current interconnection design applications.

3.5.2 Stray Capacitance of a Two-Turn Solenoidal Inductor

All the inductors have parasitic resistances and capacitances, the effects of which become dominant as frequency increases. The parasitic extraction method in this

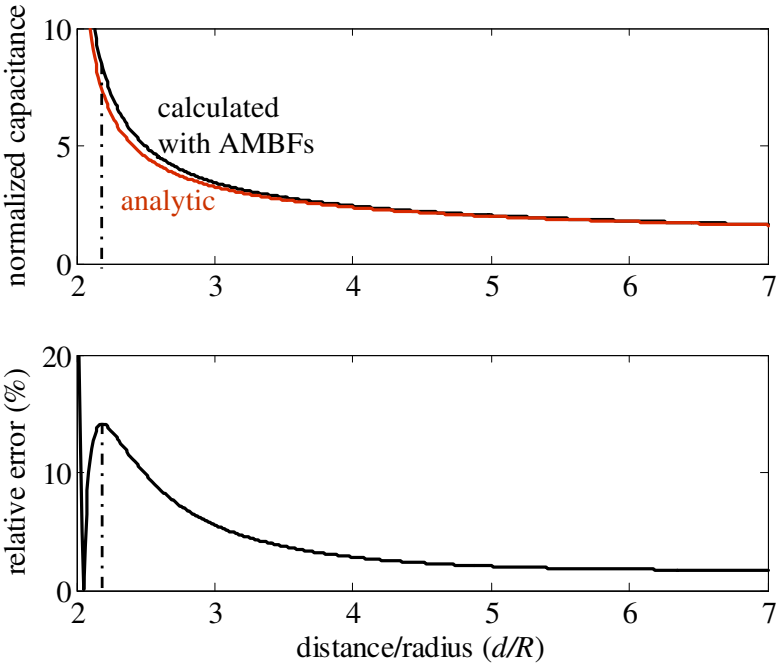


Figure 39. Odd-mode capacitances with different radii of conductors.

chapter is also valid for other passive structures. In this subsection, the stray capacitances of solenoidal type inductors are calculated and compared with published research [72].

A two-turn solenoidal air-core inductor shown in Figure 40 is a popular structure in EMC and analog applications. Main design parameters include ring diameter (D), wire radius (r_w), pitch (p), and the number of turns. The ring structures are approximated by a straight line segment model as in the case of bonding wire modeling. In the line segment model, each conductor segment is coupled to other conductors with varying orientations, so the ring structure is a good example to validate the accuracy of the 3-D capacitance calculation. From any two identical rings, the turn-to-turn capacitance can be calculated, and then the combination of the turn-to-turn capacitances provides the overall capacitance of an inductor.

Table 6 shows the turn-to-turn capacitances of the two-turn inductor for three different pitches when D and r_w are fixed at 47.2 mm and 3.25 mm, respectively.

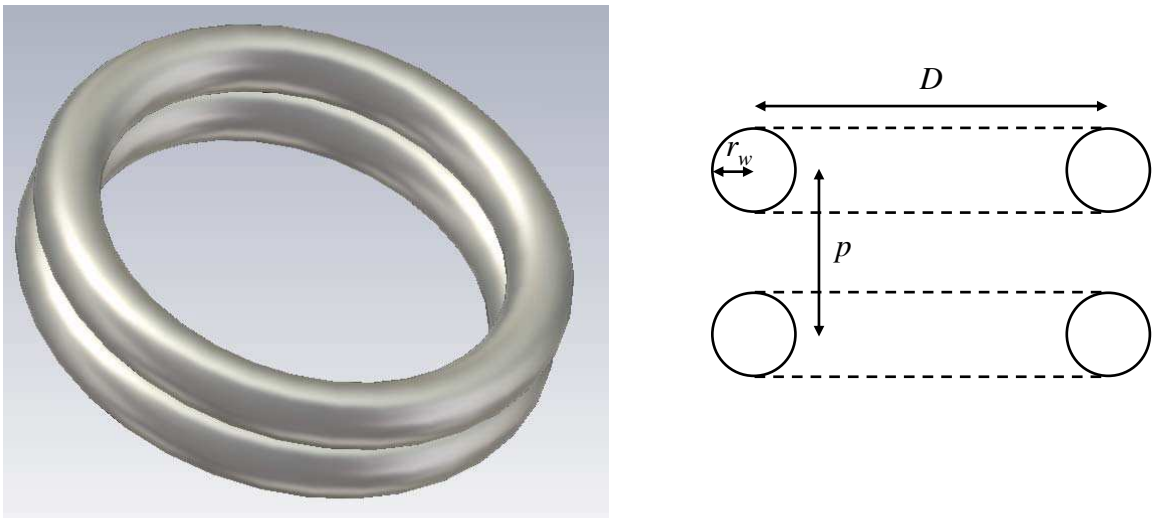


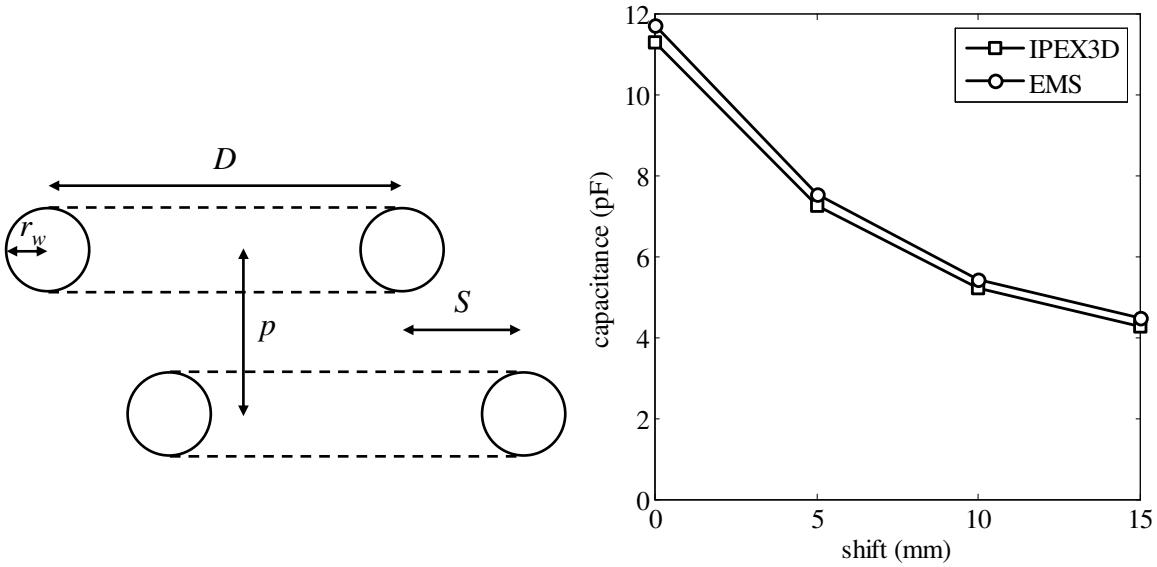
Figure 40. Two-turn solenoidal air-core inductor with the main design parameters.

The analytic results come from the capacitance of two parallel straight cylinders with length equal to the circumference of rings [72]. The capacitance values from CST EM Studio (EMS) [73] are a little smaller than the analytical results. The results from IPEX3D shows the maximum error of 3.5 % as compared to the 3-D EM simulation results. Since the ratio of the wire radius to pitch is very small, the required number of basis functions exceeds five in this example.

Table 6. Turn-to-turn capacitance of the two-turn inductor for different ring pitches

Pitch	Capacitances (pF)		
(mm)	Analytic	EMS	IPEX3D
6.90	11.82	11.73	11.32
7.32	8.30	8.24	8.07
9.00	4.85	4.81	4.73

Figure 41 shows the variation of the turn-to-turn capacitances when the rings are not aligned. Geometry parameters D, r_w, and p are fixed to 47.2 mm, 3.25 mm, and 6.90 mm, but the relative shift S between two rings is variable, as shown in Figure 41 (a). In this case, estimating the capacitances is difficult with the analytical expression. The IPEX3D results are well matched with EMS results.



(a) Geometry parameters including shift (S). (b) Turn-to-turn capacitances.

Figure 41. Turn-to-turn stray capacitances of two-turn inductance when the two rings are not aligned.

3.6 Summary

To construct a broadband RLC model of 3-D interconnections, this chapter presented a method to extract the capacitive coupling in a cylindrical conductor system. The proposed method approximates charge density on conductors by a linear combination of cylindrical AMBFs and derives a modal equivalent circuit equation from the SPIE. Similar to cylindrical CMBFs, the cylindrical AMBFs are efficient for modeling a large number of cylindrical interconnections. During the SPIE formulation, the effect of background dielectric material on the capacitance and other parasitic elements was also considered. The capacitance extraction method can be combined with the RL extraction method in Chapter 2, and the combined broadband RLC model provides the multi-port network parameters. At the end of this chapter, two examples of capacitance calculation were shown to validate the proposed capacitance extraction method.

CHAPTER 4

MODELING OF BONDING WIRE INTERCONNECTIONS IN STACKED ICS

As discussed in Chapter 1, bonding wire interconnections have limitations in their use for high-speed applications because of long interconnection length. In addition, interconnecting between vertically stacked chips is rather difficult with bonding wires, since the peripheral wiring cannot optimize high-density 3-D integration. Nevertheless, bonding wire interconnections are still useful for low-frequency and consumer electronic applications since their mature process ensures low production cost. Even for high-speed applications, optimized wiring design enables the use of bonding wire interconnections, as reported in recent design research [74, 75, 76]. If the electrical coupling model of bonding wires in 3-D integration can be found easily, the application range of the bonding wires can be extended further.

The *RLC* extraction approach presented in Chapter 2 and 3 is the basis of bonding wire modeling in this chapter. Partial impedances and potential coefficients are calculated, and their combined equivalent network can be converted to frequency-domain scattering parameters. However, the wire *RLC* model captures parasitic elements among interconnections only. In real situations, the bonding wires are influenced by various planar structures. Thus, the coupling effects of the planar structures should be considered to construct the complete bonding wire package model.

This chapter discusses how the *RLC* extraction method can generate a model of bonding wires in stacked ICs, including the effect of various planar couplings. Section 4.1 suggests a typical wired packaging structure with a defined signal and ground configuration. Section 4.2 revises the integral equation formulation to include coupling from planar structures such as wire pads and presents an image method for the approximate description of a solid ground plane. Section 4.3 validates the

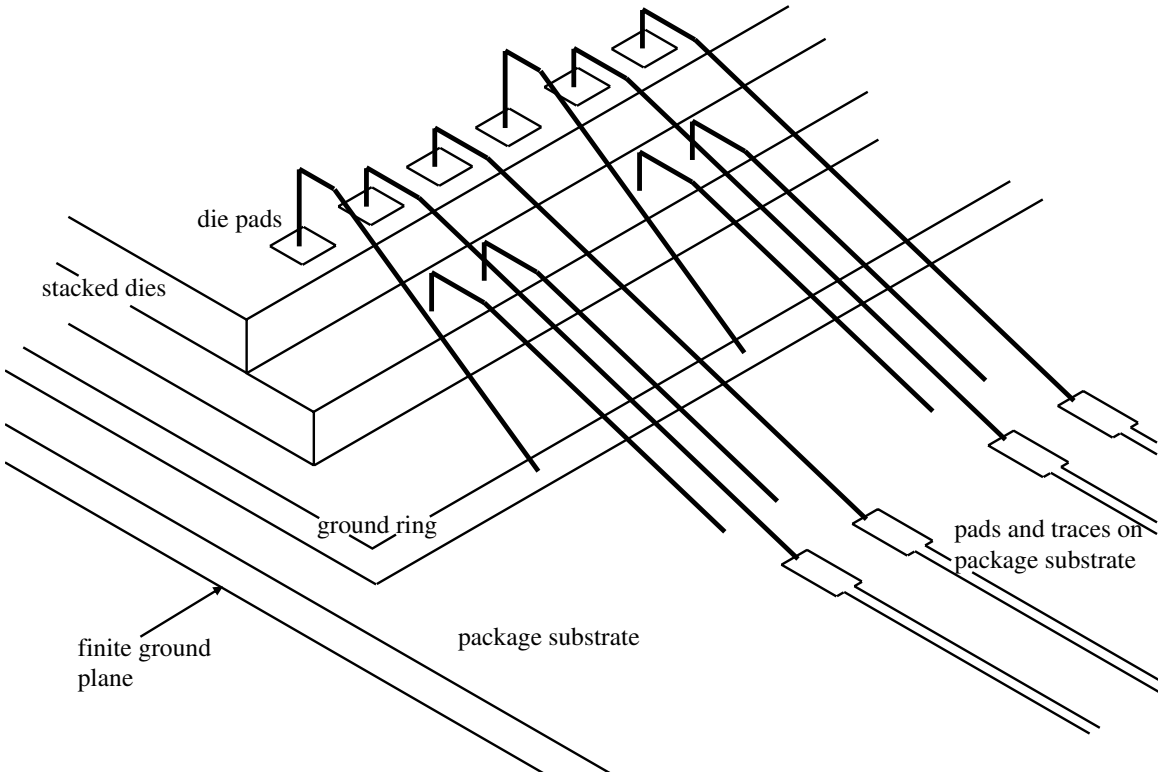


Figure 42. Typical bonding wires in stacked dies with various planar structures.

proposed method for three bonding wire examples.

4.1 Typical Bonding Wire Configuration in Stacked ICs

Figure 42 illustrates a typical bonding wire structure that is mounted on stacked dies and a package substrate [74, 77]. The bonding wires are mainly inductive components, and their partial inductance and resistance can be calculated by using the method in Chapter 2. The capacitive coupling can be found by computing the partial coefficients of potentials, as discussed in Chapter 3. However, the complete electrical behavior of the bonding wires is also dominated by several other factors.

The first factor that influences bonding wire characteristic is the substrate ground plane. The actual inductance of a bonding wire in a package is the loop inductance formed by the signal line current and return current on the ground. Therefore, the location of the ground determines the total loop inductance. If the ground plane is

finite or has irregular shapes with holes and slots, the loop inductance is also modified due to the increased return current path. Similarly, the capacitance of the bonding wire is also determined by the location of the ground, and the resultant characteristic impedance of the wire depends on the loop inductance and the capacitance between the wire and ground.

The other factor is coupling from various planar structures, including bonding pads, power/ground rings, and planar-type interconnections such as microstrip or strip lines. The bonding pad, which is another discontinuity in the signal path, may increase the capacitive coupling to neighboring wires and ground [37]. The power/ground rings are usually designed to ensure equipotential for all power/ground wires, but their high frequency effects on the bonding wires might be undesirable. The location of power/ground wires also influences the characteristics of signal propagation.

In summary, the complete modeling of 3-D bonding wire structures requires not only the partial parasitic components of bonding wires but also various planar structure models.

4.2 Coupling from Planar Structures

This section presents two methods to model the coupling from various planar structures. The first method is a general approach that combines conventional PEEC method [46] with the proposed modal equivalent circuit method. Since the PEEC method is able to extract the equivalent network of any finite planar structure, we can couple the effect of a finite ground plane, ground ring, and boding pads to bond wires. In case of modeling large solid ground planes, the image method can be used alternatively. By using a simple simulation example, the two methods are validated with analytic and 3-D EM simulation results.

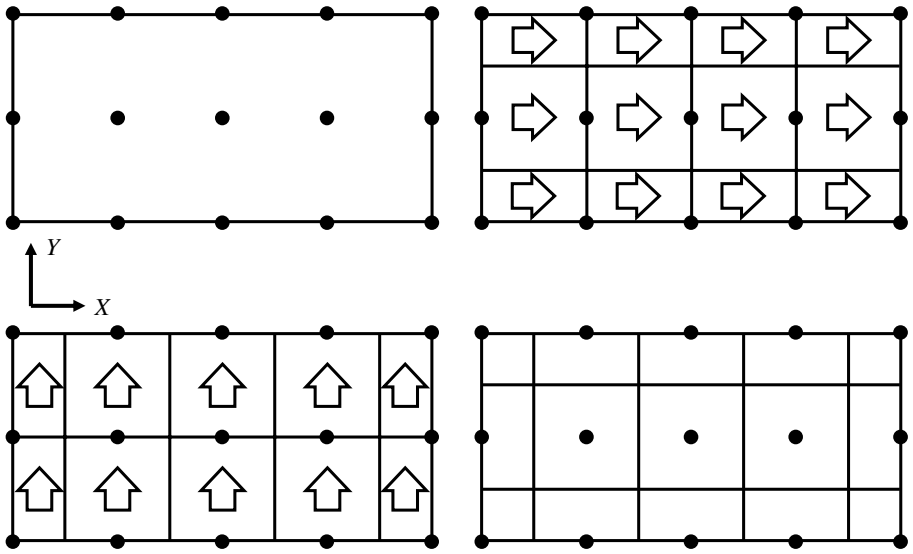


Figure 43. Planar structure cell generation. (upper left: node definition. upper right: inductive cells in X direction. lower left: inductive cells in Y direction. lower right: capacitive cells.)

4.2.1 Combination with Conventional PEEC Method

For considering the coupling from planar structures, the conventional PEEC method can be combined with the proposed method. In the context of solving an integral equation, this combination is completed by computing additional partial elements involving the interaction between piecewise planar basis functions and cylindrical modal basis functions.

Inductive and capacitive couplings among planes can be found from the conventional PEEC method. For inductive cells, each planar structure is discretized so that X-directional and Y-directional cells form a grid model as shown in Figure 43 [78]. For the self inductance calculation of inductive cells, several analytical formula can be used [79, 8]. For the mutual inductance between two parallel bricks, a combination of virtual self inductance provides good analytical results [8]. Capacitive cells are defined to cover a node, where X- and Y-directional conduction currents and displacement current through the capacitor should satisfy KCL. The analytical formula of mutual coefficients of potential between two conducting panels are used [9]. All

the closed-form formula of partial elements used are summarized in Appendix D.

In general, the capacitive cells should cover the entire surface of a planar structure, which is composed of six faces. However, if we can assume the plane is sufficiently thin, four capacitive cells on the lateral surface can be omitted. In addition, the charge distribution on the upper and the lower surfaces can be considered at the same time under the assumption that the mutual coefficients of potential between the upper and lower plates are the same as those of the self coefficients of potential. In this case, simply doubling the coefficient of potential on the upper plane approximates the total planar capacitive coupling.

Computing the electrical coupling between a plane segment and a cylindrical conductor requires an additional integral involving piecewise constant basis function and cylindrical CMBF. Figure 44 shows the typical configuration of a cylinder segment and a planar conductor segment with their geometrical parameters. Similar to the integral calculations used in Chapter 2 and 3, the following partial inductances and coefficients of potentials can be found by using the combination of analytical and numerical integrals:

$$L_{i,jnq} = \frac{\mu}{4\pi} \int_{V_i} \int_{V_j} \hat{l}_i \cdot \vec{w}_{jnq}(\vec{r_j}, \omega) \frac{1}{|\vec{r_i} - \vec{r_j}|} \mathrm{d}V_j \mathrm{d}V_i. \tag{67}$$

$$P_{i,jnq} = \frac{1}{4\pi\epsilon} \int_{S_i} \int_{S_j} v_{jnq}(\vec{r_j}) \frac{1}{|\vec{r_i} - \vec{r_j}|} \mathrm{d}S_j \mathrm{d}S_i. \tag{68}$$

For example, the integral corresponding to inductive coupling (67) is reduced to the following form after the analytical integration over the axial variable of the cylinder (z_j):

$$L_{i,jnq} = \frac{\mu}{4\pi} \int_{x_i,y_i} \int_{\rho_j,\varphi_j} \big(\hat{l}_i \cdot \vec{w}_{jnq}(\vec{r_j}, \omega)\big) I_z(x_i, y_i, \rho_j, \varphi_j) \rho_j \mathrm{d}\rho_j \mathrm{d}\varphi_j \mathrm{d}x_i \mathrm{d}y_i. \tag{69}$$

In the above expression, we simplified the integral over z_i under the assumption that the thickness of the planar structure is negligibly small. Another expression similar

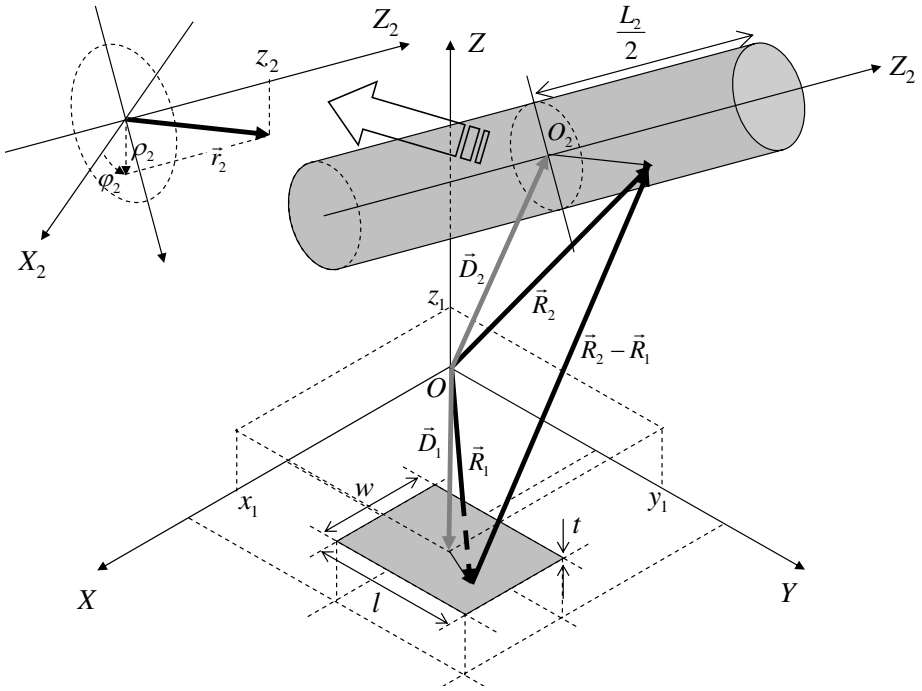


Figure 44. Definition of the orientation parameters of a plane and a cylinder segment.

to (69) can be obtained from (68) for the capacitive coupling. The details of deriving the analytical integral over the axial variable (I_z) are discussed in Appendix E.

After computing all the partial element matrices of wires and planes, continuity equations (KCL) are applied for each wire and plane, and the following global matrix can be generated:

$$\begin{pmatrix} \mathbf{Z^{pl}} & \mathbf{Z_s^{pl,w}} & \mathbf{Z_p^{pl,w}} & -\mathbf{\Delta_v^{pl}} & & & & & \\ \mathbf{Z_s^{w,pl}} & \mathbf{Z_{ss}} & \mathbf{Z_{sp}} & & -\mathbf{\Delta_v^{w}} & & & & \\ \mathbf{Z_p^{w,pl}} & \mathbf{Z_{ps}} & \mathbf{Z_{pp}} & & & & & & \\ \mathbf{\Delta_I^{pl}} & & & & & j\omega\mathbf{E} & & & \\ & \mathbf{\Delta_I^{w}} & & & & & j\omega\mathbf{E} & & \\ & & & -\mathbf{E} & & \mathbf{P^{pl}} & \mathbf{P_s^{pl,w}} & \mathbf{P_p^{pl,w}} & \\ & & & & -\mathbf{E} & \mathbf{P_s^{w,pl}} & \mathbf{P_{ss}} & \mathbf{P_{sp}} & \\ & & & & & \mathbf{P_p^{w,pl}} & \mathbf{P_{ps}} & \mathbf{P_{pp}} & \end{pmatrix} \begin{pmatrix} \mathbf{I^{pl}} \\ \mathbf{I_s^{w}} \\ \mathbf{I_p^{w}} \\ \mathbf{\Phi^{pl}} \\ \mathbf{\Phi^{w}} \\ \mathbf{Q_{pl}} \\ \mathbf{Q_s^{w}} \\ \mathbf{Q_p^{w}} \end{pmatrix} = \begin{pmatrix} \\ \\ \\ \mathbf{I_t^{pl}} \\ \mathbf{I_t^{w}} \\ \\ \\ \\ \end{pmatrix}, \tag{70}$$

where the terminal currents $\mathbf{I_t^{pl}}$ and $\mathbf{I_t^{w}}$ are from planes and wires, respectively. With

the defined terminal excitation currents, network parameters are obtained in the same way as discussed in Section 3.4. The ports on planes and wires can be connected to each other to obtain the network parameter of the entire interconnection signal path.

4.2.2 Image Method for Modeling Infinite Ground

Although the reference or ground plane in a package is a finite and irregularly shaped structure including discontinuities such as holes and slots, approximating the ground as a perfect and infinite one is sometimes useful to analyze bonding wires in a package. Thus, together with the classical PEEC method to model small finite planar structures, the image method can be employed to capture the effect of relatively large ground planes [42]. Compared to the rigorous use of the conventional PEEC method, the image method reduces the computational cost.

As shown in Figure 45, symmetric image conductors are defined in the opposite side of the ideal ground plane. Since the image conductor has the identical shape of the original conductor, we can use the same resistance, inductance, and coefficients of potential matrices of the original conductor. However, the inductive and capacitive coupling between the original and the image conductors need to be calculated.

The simulation setup with the image conductors provides a network parameter with a doubled port number, which can be converted to single-ended S parameter with ideal ground by using the following modal conversion matrix [80]:

$$\begin{pmatrix} a_d \\ a_c \end{pmatrix} = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & -1 \\ 1 & 1 \end{pmatrix} \begin{pmatrix} a_r \\ a_i \end{pmatrix}, \tag{71}$$

where a_r and a_i are incoming or reflected power waves of the actual port and the image port, and a_d and a_c are differential and common mode power waves, respectively. The differential power wave will be used as the resultant incoming wave. By stamping (71) into a global conversion matrix $\mathbf{M}$, the following transform leads to the total S

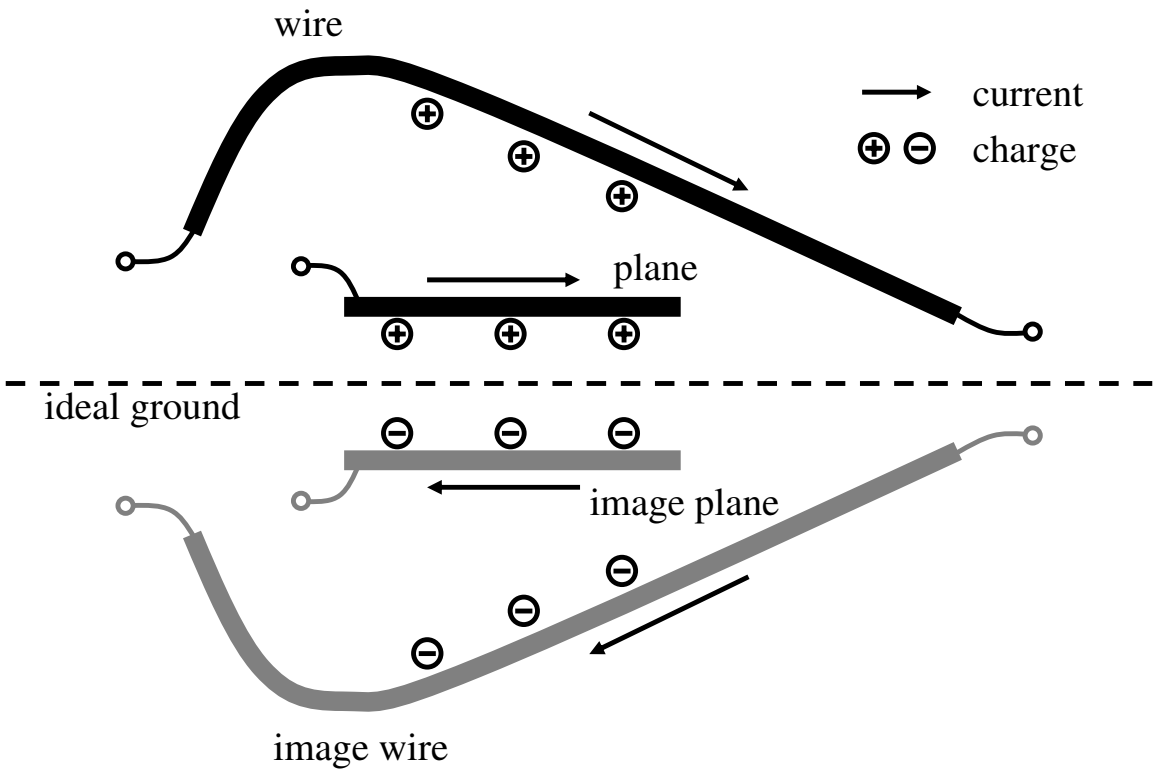


Figure 45. Example of image conductors and port definition.

parameter:

$$\begin{pmatrix} \mathbf{S_{dd}} & \mathbf{S_{dc}} \\ \mathbf{S_{cd}} & \mathbf{S_{cc}} \end{pmatrix} = \mathbf{MSM^{-1}}, \tag{72}$$

where $\mathbf{S_{dd}}$ is the resultant S parameter that characterizes the original interconnections.

4.2.3 Validation: Single Cylinder on Ground

For validation of the modeling method to capture coupling effect from planar structures, a cylindrical conductor on ground is modeled and compared with analytical and 3-D EM simulation results.

As discussed in the previous subsection, the ground plane can be considered with the image method (ideal infinite ground) or the combination with a conventional PEEC method (finite ground). Figure 46 illustrates a cylinder with a finite ground model, the length of which is the same as that of the cylinder. The plane is discretized

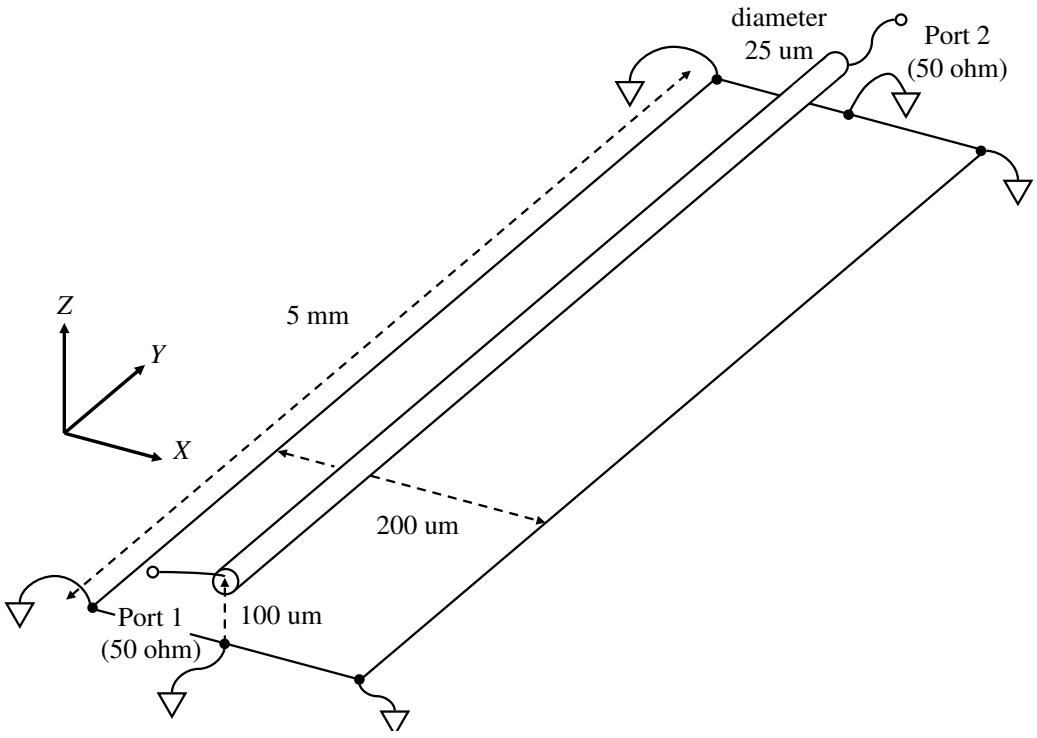


Figure 46. IPEX3D model of a cylinder on a finite ground plane.

to 11 (X) by 21 (Y) nodes, and four edge points and two points at ports are grounded.

Figure 47 shows the magnitude of S parameters of the cylindrical interconnection on the ideal and finite ground plane. Compared to the ideal grounded case, the capacitive coupling from the finite ground weakens, resulting in the increase of the characteristic impedance of the interconnection. Therefore, $|S_{11}|$ of the cylinder on the finite plane is higher than that of the cylinder on the ideal ground. Nevertheless, the return loss is still smaller than that of the cylinder without any ground plane, which has minimum capacitance.

For validation of the cylinder with ideal ground, the scattering parameters were calculated from 2-D lossless transmission line model of a cylinder on ideal ground, which has the following analytical expression for per-unit-length inductance and capacitance [59]:

$$C = \frac{2\pi\epsilon}{\cosh^{-1} H/r}, \tag{73}$$

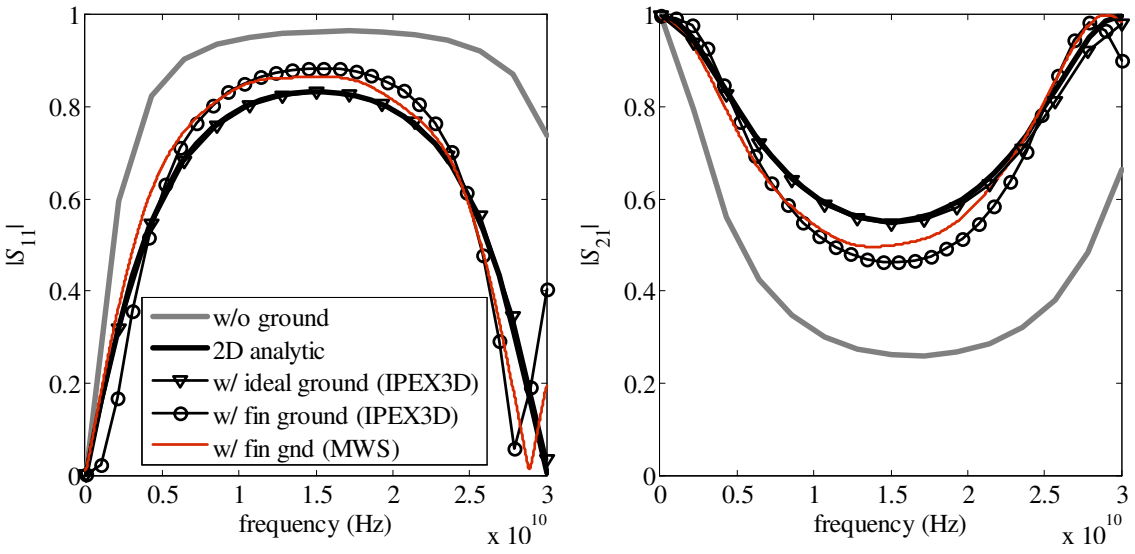


Figure 47. Magnitudes of S parameters of a cylinder on ground plane.

$$L = \frac{\mu_0}{\pi\epsilon} \cosh^{-1} H/r, \tag{74}$$

where r and H are the cylinder radius and height of the cylinder from the ground plane, respectively. The capacitance formula is identical to (64), with a different definition of distance of the conductor to the ground. Figure 47 shows that the magnitude of S parameters from IPEX3D model is well matched with the analytical results, except for the additional insertion loss from the cylinder resistance.

The cylinder on finite ground is compared to the S parameters from the simulation of the identical structure using CST Microwave Studio (MWS) [81]. Although some differences between the two results are shown in Figure 47, the overall level of the insertion and return losses are well matched. In addition, both the simulation results indicate the increase in the effective electrical length of the interconnection, compared to the ideal ground case.

The accuracy of modeling the finite ground plane improves with an increase in the number of cells. However, the discretization process requires more memory, and computing the coupling among all the planar bases and frequency-dependent modal increases the computational cost considerably. Thus, a more practical way will be to

approximate the large finite ground with the ideal ground plane. Nevertheless, the conventional PEEC-based planar coupling model is still useful when modeling small structures such as bonding wire pads. Several practical examples will be shown in the next section.

4.3 Bonding Wire Modeling Examples

This section presents three bonding wire modeling examples to observe various coupling effects. Frequency-domain S parameters are extracted from RLC models of JEDEC4 type bonding wires, bonding wires in a plastic ball grid array package, and wires in stacked ICs. Through these examples, we can find how electrical coupling from planar structures modifies the expected characteristics of bonding wires. In addition, the effects of signaling and grounding design schemes can be observed, and the complicated contribution of coupling from horizontal and vertical wires can be quantified. This section validates the examples with a 3-D full-wave EM simulator.

4.3.1 Three JEDEC4 Type Bonding Wires

The bonding wire structure shown in Figure 48 is adopted from low-frequency package applications such as thin quad flat pack (TQFP) and lead-frame type packaging. The length of wires is about 5 mm, which is rather long in the current technology trend. The shape of each wire is constructed from the simplified model of EIA/JEDEC standard (JEDEC4) [82]. The coordinate values of each wire segmentation point are also shown in Figure 48. The diameter of wires is 25 μm. For wire and plane conductivities, gold and copper are used, respectively.

To observe the effect of ground, the three bonding wires were simulated with and without ideal ground. As discussed in the previous section, additional image wires were defined to describe the ideal ground effect, and then the resultant single-ended S parameter matrix is converted to differential- and common-mode S parameter matrix. Figure 49 and 50 compares the magnitudes of all S-parameters, where we

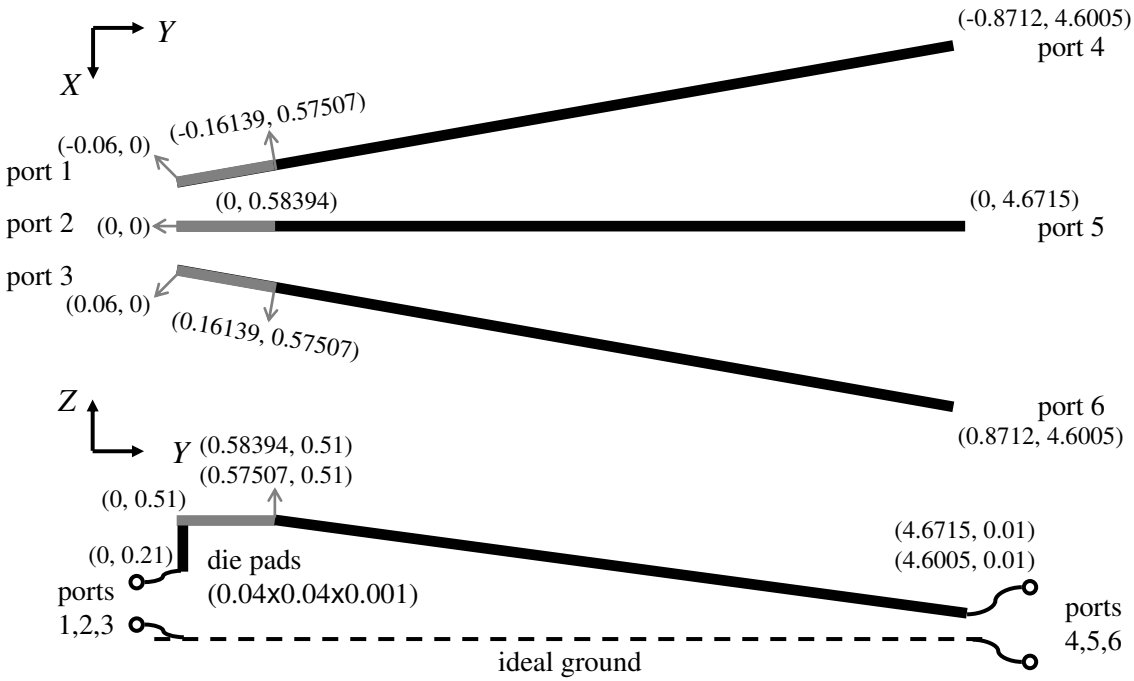


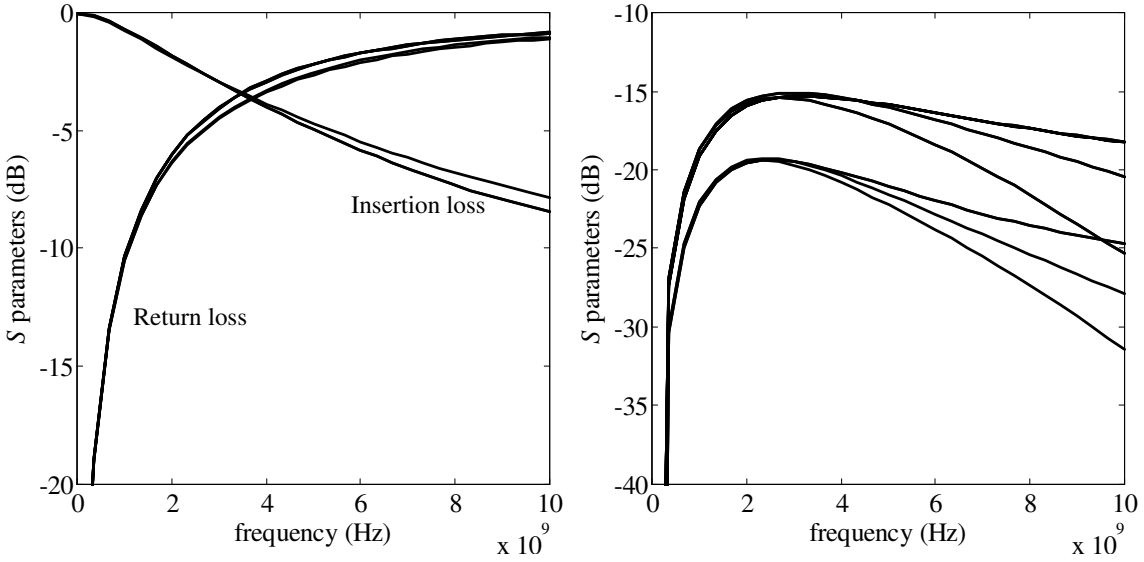
Figure 48. Configuration of three JEDEC4 type bonding wires.

can find that both the insertion loss and return loss are improved when ideal ground is applied. This is because the ground reduces the total loop inductance of wires, and the inductance reduction is more dominant than the capacitance increase. The comparison of IPEX3D results of the grounded wires with CST MWS simulation results show good match, although small errors are shown in the couplings.

To observe the effects of planar structures, another configuration of wires with a long planar structure (in Figure 51) was simulated. The inclusion of the finite conductor segment breaks the geometrical symmetry of the original bonding wire structure because the level of coupling from the planar structure is different for each wire. Therefore, in the resultant S parameters shown in Figure 52, the insertion loss of the wire that is the closest to the plane is better than other wires.

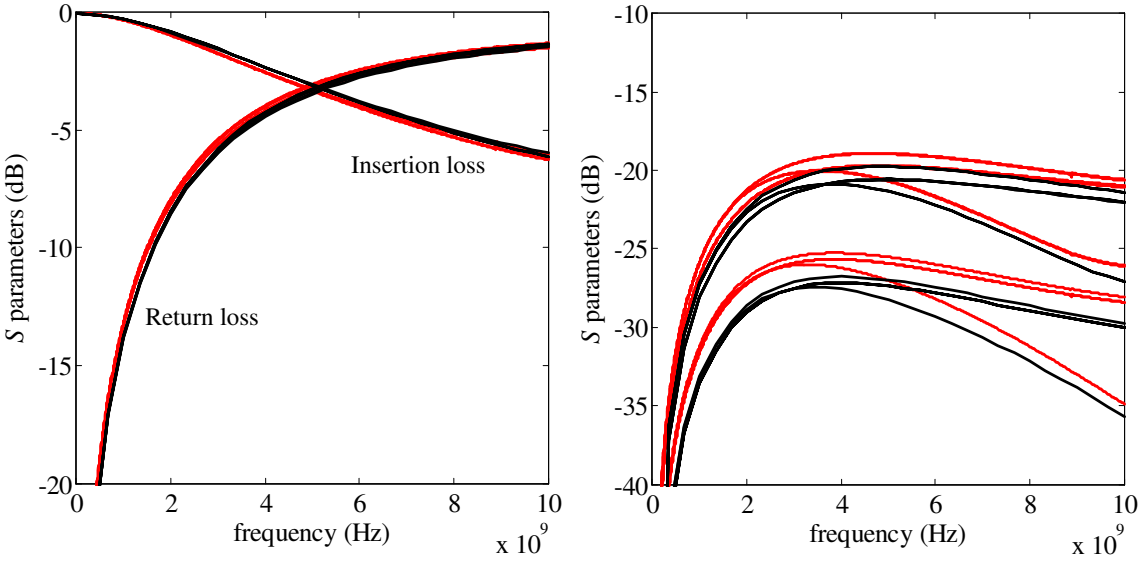
4.3.2 Bonding Wires in a Plastic Ball Grid Array (PBGA) Package

In this subsection, bonding wire structures in wire-bonded PBGA [74] were simulated. By using the proposed method, the characteristics of different signaling structures



(a) Insertion and return losses. (b) Couplings.

Figure 49. S **parameters of three JEDEC4 type bonding wires without the ideal ground.**



(a) Insertion and return losses. (b) Couplings.

Figure 50. S **parameters of three JEDEC4 type bonding wires on the ideal ground without pads (black: IPEX3D, red: MWS).**

were validated and compared with 3-D full-wave EM simulation data. Simulation results showed that a proper choice of signaling scheme as well as the wire structure design determine interconnection bandwidth.

Figure 53 shows the configuration of wires and grounds to be simulated. All

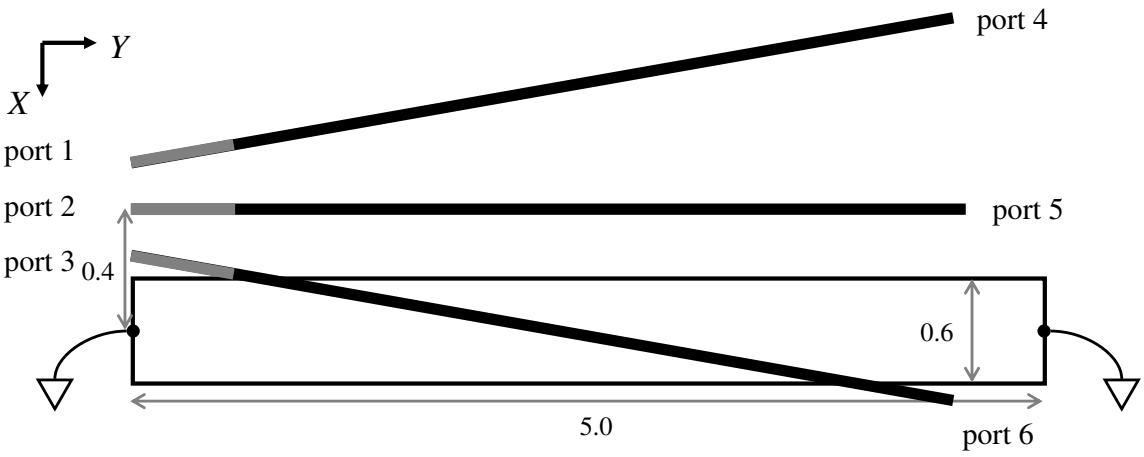
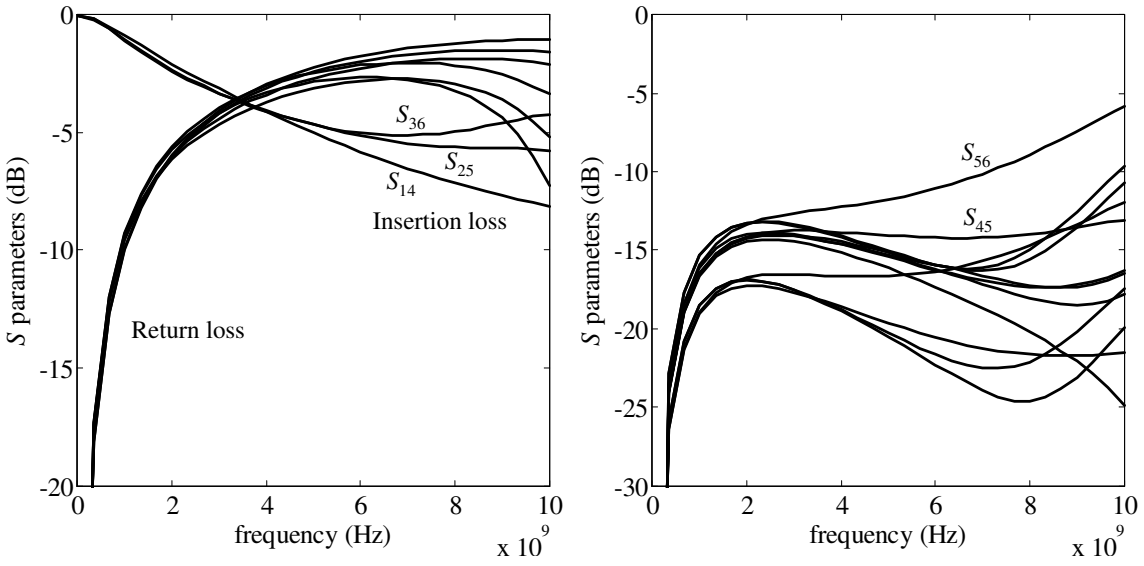


Figure 51. Configuration of three JEDEC4 bonding wires with a finite plane segment.



(a) Insertion and return losses.

(b) Couplings.

Figure 52. S **parameters of three JEDEC4 type bonding wires with a finite plane segment.**

the structures are based on differential signaling, and ground-signal-signal-ground (GSSG) structures have additional ground wires. In case of GSSG signaling, the ground wires can be assigned on a separate region of the package or can be tied to a common ground ring as shown in GSSG-2 structure.

For considering the effect of plastic molding around the wires, the dielectric constant of molding compound is defined as 4.3 [83]. An ideal ground is assumed at a

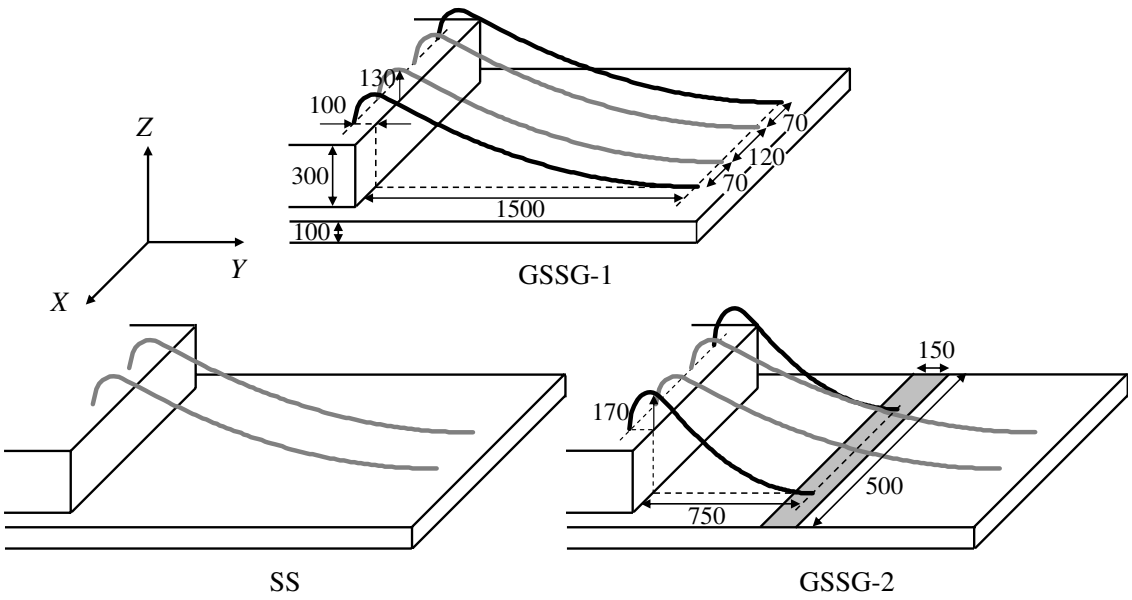


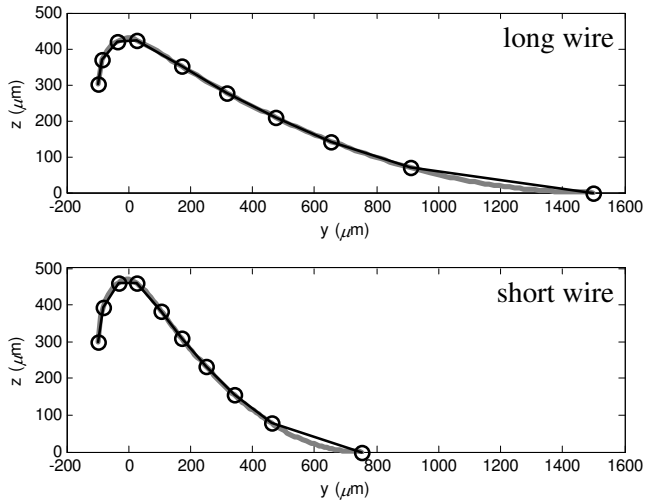
Figure 53. Bonding wire configurations in PBGA package to be simulated.

location of 100 μm below the package surface. To capture wire shapes more accurately, we used the following curves that describe wedge-ball bonding wires [84].

$$\begin{array}{ll} z = H\frac{\xi^2-\xi^n}{\xi_y^2-\xi_y^n} & 0 \le y \le Y \\ \frac{(y-y^*)^2}{a^2} + \frac{(z-z^*)^2}{b^2} = 1 & Y \le y \le L \end{array}, \tag{75}$$

where $\xi = \frac{y}{L}$, $\xi_y = \frac{Y}{L} = (\frac{2}{n})^{\frac{1}{n-2}}$, $y^* = Y$, $z^* = 0$, $a = L - Y$, $b = H$, and H, Y, L are the height and the lengths of the bonding wire, respectively. The curves ensure both zero slope at the wedge bonding on the package and an infinite slope at the ball bonding on the die. After obtaining the curves with pad distances and die/wire heights, approximate conductor segments were generated as shown in Figure 54. The long wires will be used for signal and ground wires in GSSG-1 and signal-signal (SS) structures, and the short wires will be used for ground wires on the ground ring in GSSG-2. The lengths of the long and the short wires are 1.75 mm and 1.12 mm, respectively.

Before the simulation of the structures in Figure 53, the effects of bonding pads were studied for the SS signaling case. The bonding pads with a size of 200 μm $\times$ 75 μm were attached at the ends of the bonding wires, as shown in Figure 55 (a).



long wire

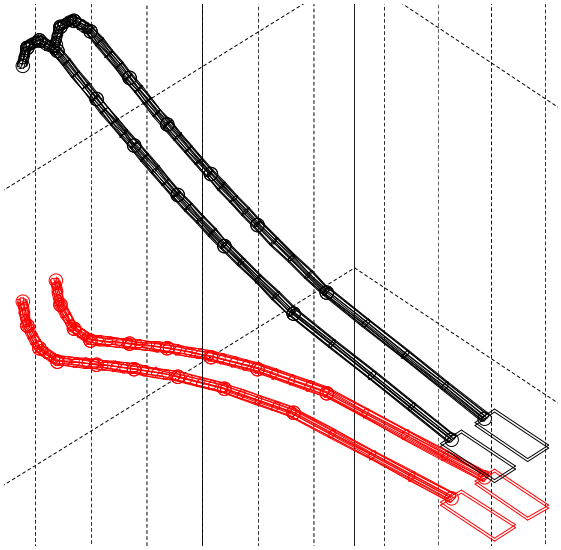
y (um)	z (um)
-100.0	400.00
-84.0	470.54
-36.0	521.28
28.0	524.15
172.0	450.31
316.0	378.48
476.0	308.30
652.0	242.85
908.0	169.62
1500.0	100.00

short wire

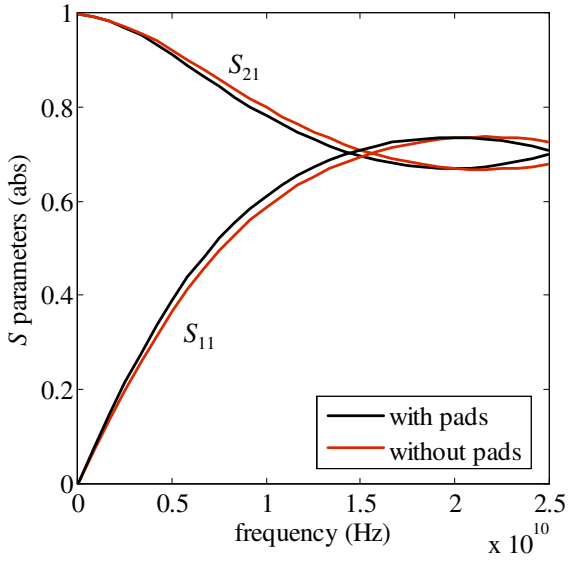
y (um)	z (um)
-100.0	400.00
-83.0	494.82
-32.0	561.06
27.5	559.63
104.0	483.77
172.0	408.84
248.5	332.66
342.0	254 .00
461.0	177.27
750.0	100.00

Figure 54. Smooth wedge-ball Bonding wire curves (grey) and their segment approximations (dotted black) with segmentation points.

In Figure 55 (b), which compares the S parameters of SS bonding wires with and without the bonding pads, the effect of the bonding pads is similar to the response obtained with a slight increase of electrical length. Since the bonding pad effect on the bonding wire characteristic is small in this case, we can neglect them in the following simulations.



(a) Bonding wires with pads (including image conductor).



(b) S parameters.

Figure 55. Effect of bonding pads on S parameters of wires.

Figure 56 shows the magnitude of scattering parameters for the three structures in Figure 53. As discussed in research on PBGA package design [74], the GSSG structure (especially GSSG-1) is better for signal transmission than the SS structure. However, the S parameters of the GSSG-2 structure indicate that only designing the signal/ground wiring in schematics does not ensure the improvement of signal transmission. For GSSG design to work effectively, ground wires should guide signal wires in parallel. Comparison with CST MWS results show good accuracy of IPEX3D, but error increases beyond 15 GHz.

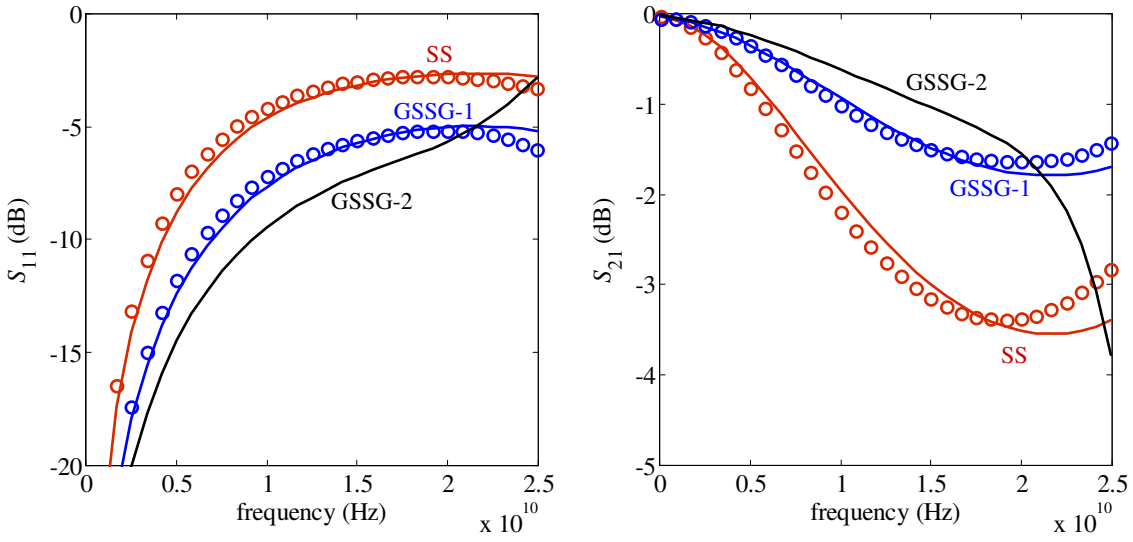
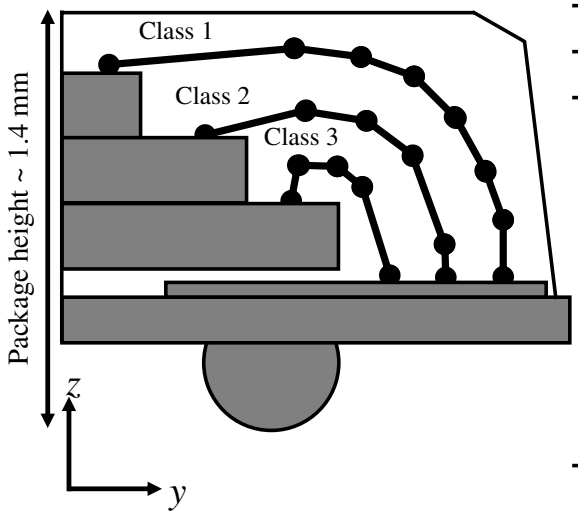


Figure 56. Scattering parameters of different wiring structures (lines: IPEX3D, circles: MWS).

4.3.3 Bonding Wires in Three Stacked ICs: The Effect of Vertical Coupling

In this section, parasitic elements of bonding wires on three stacked ICs are extracted. The bonding wire structure in Figure 57 has been obtained approximately from the model of a triple-chip stacked chip-scale package (CSP) [14]. Wire diameter is 25 μm, and the pitch between adjacent wires is 60 or 80 μm [15]. All wires are in parallel. The approximate lengths of wires are 1.26 mm (class 1), 0.82 mm (class 2), and 0.48 mm (class 3), respectively.



Class 1		Class 2		Class 3	
Y	*Z*	*Y*	*Z*	*Y*	*Z*
86.1,	472.1	309.8,	324.6	511.5,	177.0
516.4,	538.5	543.4,	395.9	523.8,	270.5
671.3,	518.9	683.6,	371.3	617.2,	260.7
794.3,	474.6	786.9,	290.2	673.8,	211.8
885.2,	378.7	865.6,	78.7	737.7,	2.5
956.6,	255.7	868.0,	2.5		
998.4,	145.1				
998.4,	2.5				

Figure 57. Side view and segmentation geometry (in μm) of gold bonding wires on three stacked ICs.

For validation, inductance and resistance values of six bonding wire structures in Figure 58 were extracted, and S parameters from the R-L equivalent circuit model were compared with values from CST Microwave Studio (MWS), a commercial full-wave EM simulator [81]. In the simulation setup, six ports were defined as shown in Figure 58, which assumes each wire as a signal or a ground wire. Simulation results in Figures 59 and 60 indicate good correlation, except at high-frequencies. This high-frequency error can be attributed to the quasi-static assumption used in IPEX3D, which does not include capacitive coupling. Since bonding wires are dominated by inductive coupling, the absence of capacitive coupling is expected to have a small effect on the typical structure. The other source of error is the approximation of conductor segments. As discussed in Section 2.1.2.3, the 1-D current assumption in IPEX3D may be inaccurate, especially at the sharp edges of adjoining conductor segments. For example, the sharp edge shown in class 3 wire of Figure 57 will generate some high-frequency error. The two combined error effects translate to a maximum error of 15.1 % for $|S_{3,3}|$ in Figure 59, but this maximum error is acceptable, since it occurs at small return loss values.

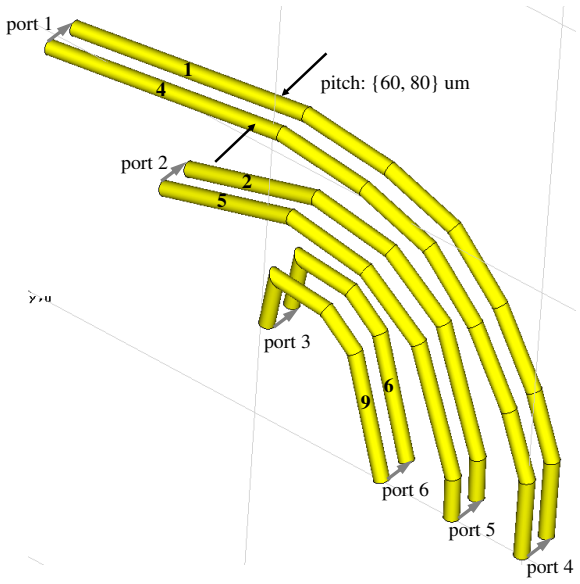


Figure 58. Six bonding wire structure and port configuration.

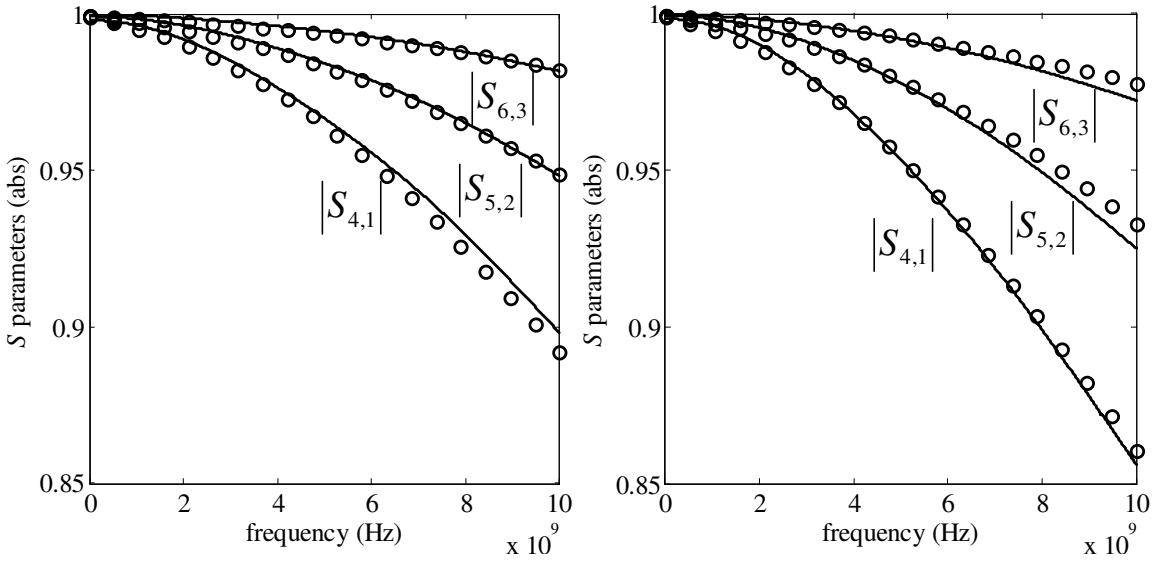


Figure 59. $S-$parameters of six bonding wires. (circles: IPEX3D, lines: CST MWS) Insertion losses. (left: 60 μm pitch, right: 80 μm pitch)

The next example consists of 102 bonding wires as shown in Figure 61, where 34 wires are mounted for each stack. Figure 62 (b) and (c) show resistances and self inductances of all bonding wires at 10 GHz, with one conductor of class 2 grounded. The ground conductor influences adjacent wires as well as upper and lower wires, so the resultant high-frequency resistances and inductances change. Figure 62 also

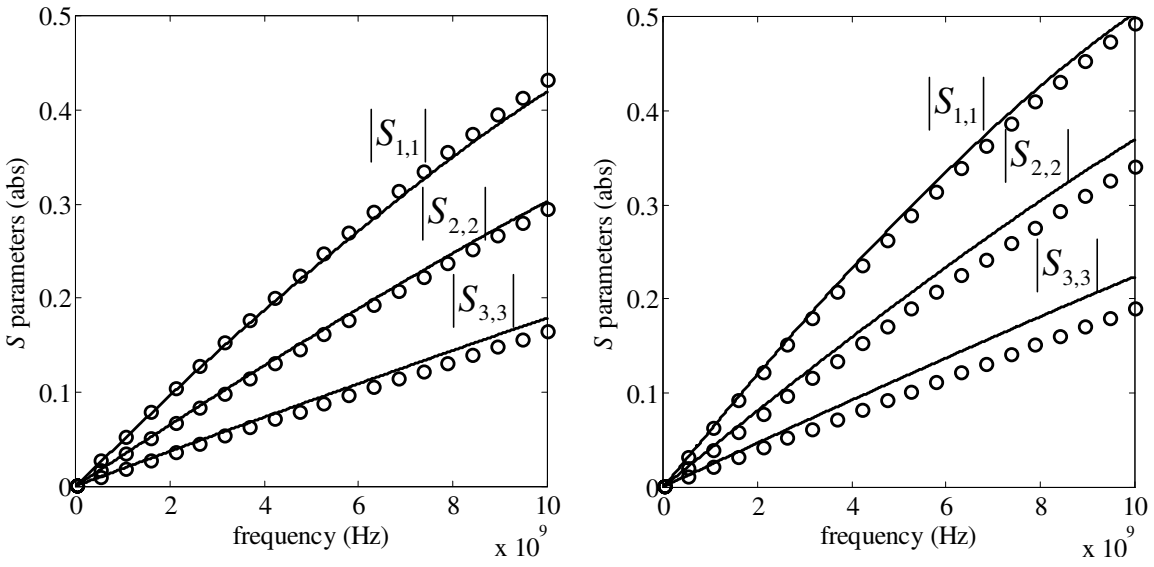


Figure 60. $S-$**parameters of six bonding wires. (circles: IPEX3D, lines: CST MWS) Return losses. (left: 60** μ**m pitch, right: 80** μ**m pitch)**

shows small variations of wire impedances at the edge of the structure, where proximity effects are smaller than those at the middle of the structure. Capturing these parasitic variations at high-frequencies is useful for efficient design of high-density 3-D interconnections for broadband applications.

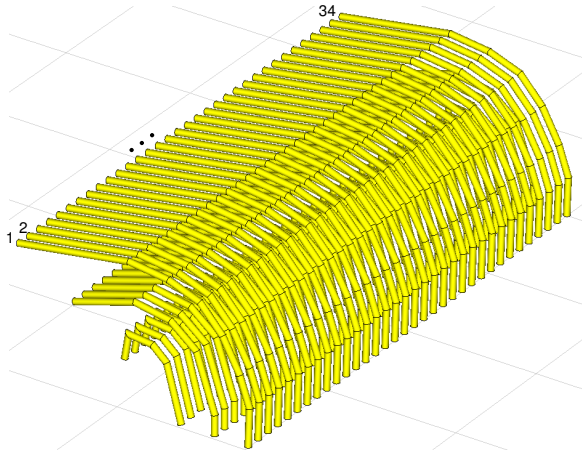
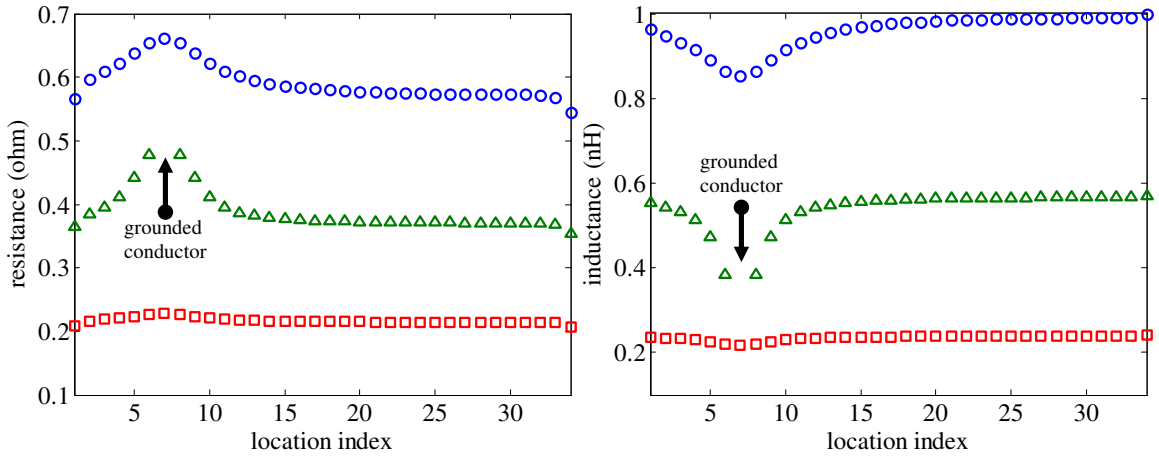


Figure 61. 102 bonding wire structure with index.

Finally, an *RLC* model of thirty bonding wires (10 wires for each stacked die) was generated to observe the inductive and capacitive coupling effects from horizontally and vertically located wires. To model an ideal ground, an additional 30 image wires



(a) Wire resistances. (b) Wire self inductances.

Figure 62. Extracted bonding wire parasitics at 10 GHz with a wire of class 2 grounded.

were included in the simulation setup. Differential ports were defined based on GSSG signaling, so the total number of differential ports is 18, as shown in Figure 63. The comparison of the simulation results with other full-wave simulators is not available because of the huge simulation times involved.

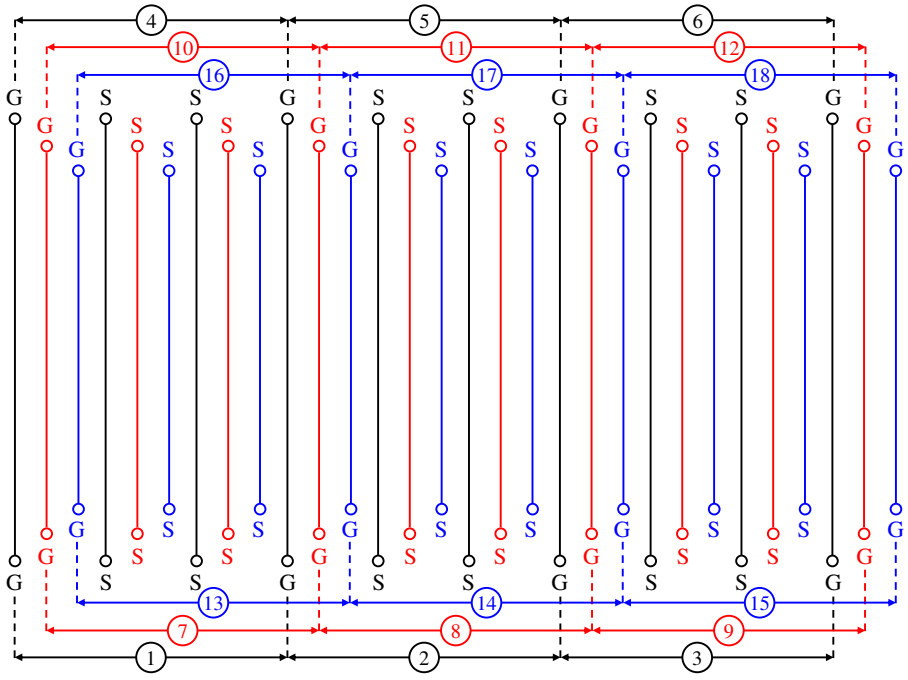
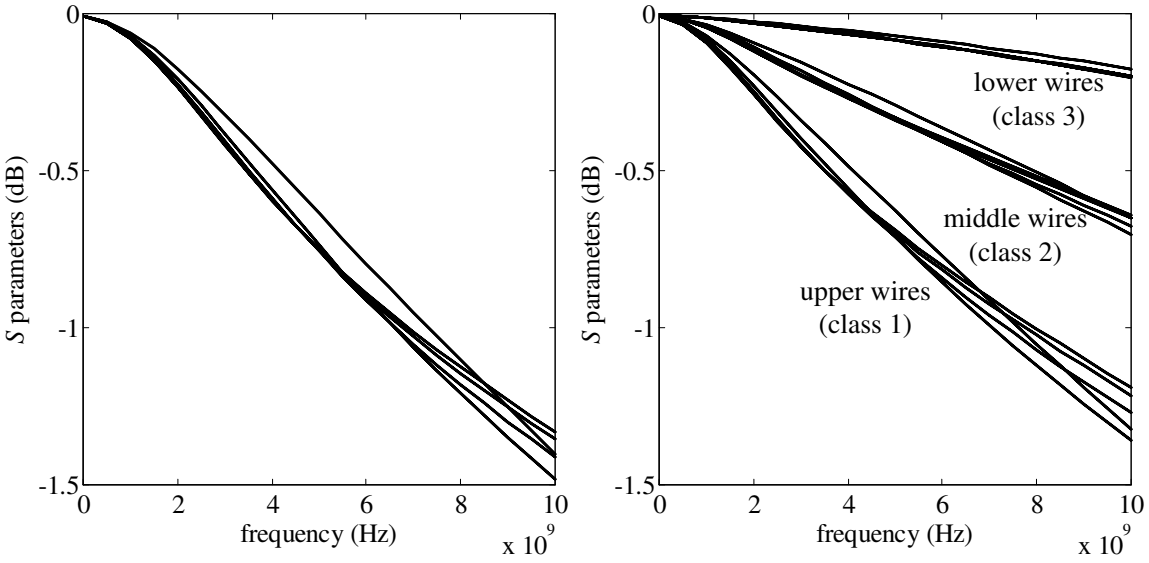


Figure 63. Port definitions of 30 bonding wires based on GSSG signaling.



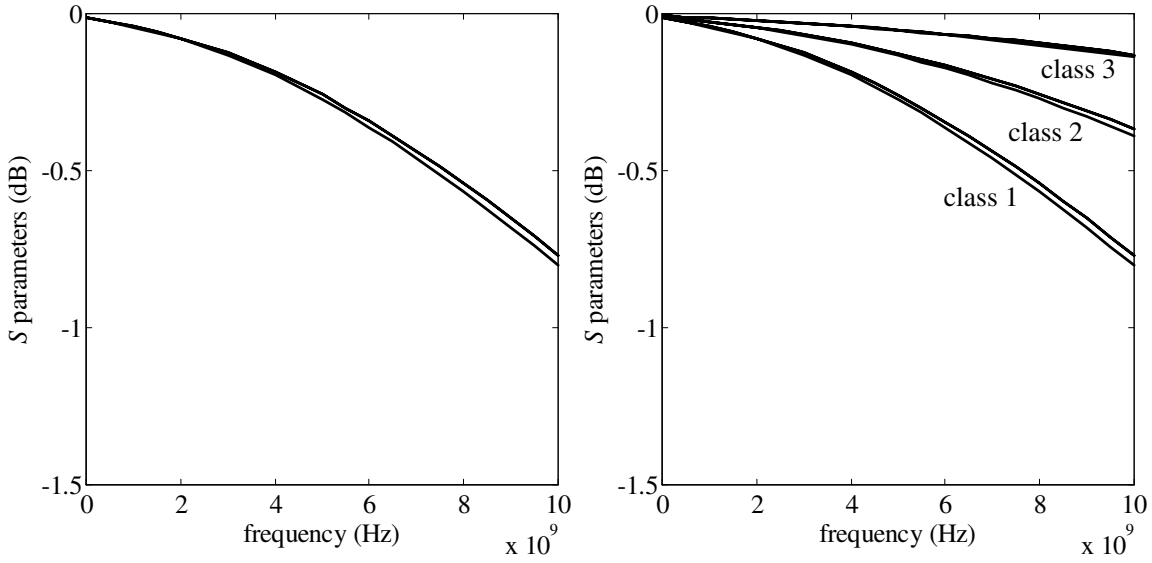
(a) When only upper wires are simulated without lower wires.

(b) When all the wires are simulated.

Figure 64. Single-ended port insertion losses of 30 bonding wires.

Figure 64 shows the insertion loss of bonding wires when all the wires were assumed to be single ended. The entire structure was simulated (Figure 64 (b)), and then the upper wires (class 1) were simulated with the lower wires removed (Figure 64 (a)) to observe the effect of vertical coupling. The maximum loss is about -1.5 dB at 10 GHz, and the variations in the insertion losses are shown for both cases. The single-ended insertion loss of the upper wires is improved when the middle and lower wires are present, but the difference of insertion loss is removed when applying the GSSG signaling, as shown in Figure 65.

Figure 66 shows the coupling (in S parameters) from all the wire ports to ports 1 and 2 at 10 GHz. Since the distances between upper and lower wires are smaller than those between upper wire ports, the vertical coupling is relatively small. However, the maximum coupling from middle wires to upper wires can be about -35 dB, which may not be negligible in mixed-signal and RF applications. Using the GSSG differential signaling improves the balance between outer and inner ports, but the change of signaling method to single-ended signaling can be significantly affected by unbalanced



(a) When only upper wires are simulated without lower wires.

(b) When all the wires are simulated.

Figure 65. GSSG port insertion losses of 30 bonding wires.

vertical coupling.

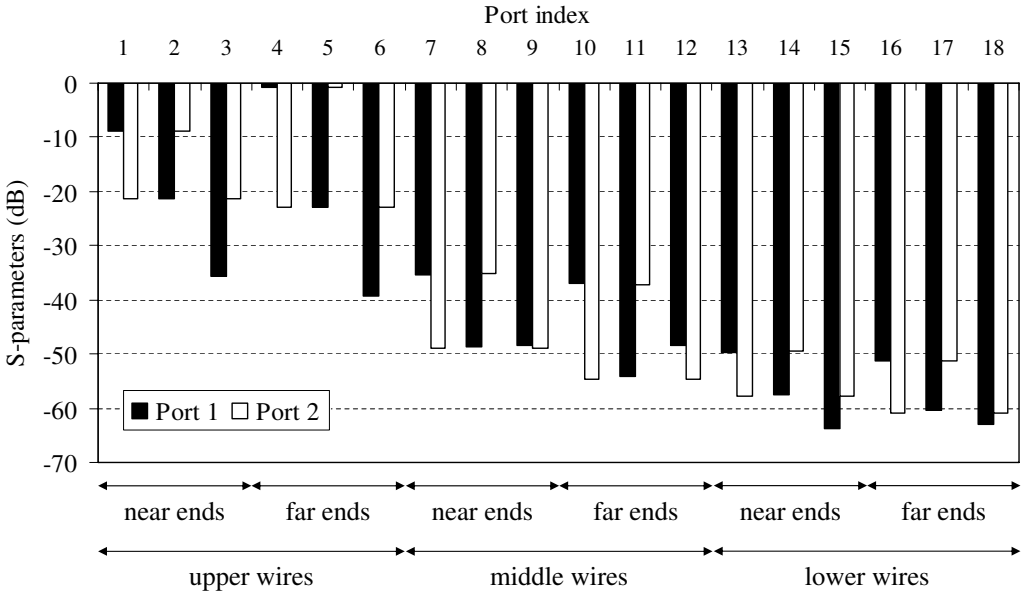


Figure 66. Couplings from ports 1 and 2 (GSSG) to other ports.

4.3.4 Comparison of Simulation Time with a Full-Wave EM Simulator

Table 7 shows the simulation times of IPEX3D and MWS for four structures in the previous sections. All simulations were performed using an Intel Xeon 3 GHz CPU with 3.25 GB RAM. Simulation time of IPEX3D depends on the number of frequency points and the maximum modeling frequency. Simulation time of MWS is not influenced by frequency points, but it depends on the error threshold to converge solutions. Except for the single cylinder case, IPEX3D requires less simulation times than MWS.

Table 7. Simulation times of bonding wire structures

Example name	MWS	IPEX3D		
	Total simulation time (sec.)	Total simulation time (sec.)	Number of frequency points	Maximum frequency (GHz)
Single cylinder on ground (Sec. 4.2.3)	871.00	6177.01	30	30
Three JEDEC4 bonding wires (Sec. 4.3.1)	30009.00	3324.90	30	10
PBGA wires (SS) (Sec. 4.3.2)	54206.00	5946.25	31	25
PBGA wires (GSSG-1) (Sec. 4.3.2)	82163.00	16466.32	31	25

4.4 Summary

To model practical configurations of bonding wires in stacked ICs, this chapter presented a method to couple planar coupling effects into the modal *RLC* interconnection model discussed in Chapter 2 and 3. Combination with the PEEC method enables the modeling of finite planar structures such as bonding pads and finite ground structures. In addition, the image method approximates large solid ground planes. The proposed method was validated for various bonding wire structures with a 3-D full-wave EM simulator, and showed good accuracy and efficiency.

CHAPTER 5

MODELING OF THROUGH SILICON VIA (TSV) INTERCONNECTIONS

To increase 3-D integration density, TSV interconnections are emerging as major interconnection elements. Compared to bonding wires, TSV interconnections are much more efficient to reduce interconnection pitch since they are fabricated in silicon substrate. In addition, the direct vertical connection by TSVs shortens electrical length, especially for communication between stacked chips. With these features, the use of TSV interconnections can be extended to various integrated mixed-signal system designs.

In spite of these merits, the commercialization of TSV-based integration is facing technical barriers. Until now, the main interest has been on the fabrication process, but the electrical design methodology is becoming a major issue. Characterizing TSV interconnections needs more consideration than other types of interconnections. Unlike bonding wires, the TSVs are embedded in a multilayered lossy silicon substrate, which generates additional loss and distortion. Furthermore, the oxide coating structure around the TSV is another important design parameter. Need for controlling these parameters makes TSV modeling more challenging and costly.

As in the case of bonding wires in 3-D integration, the electrical coupling of a large number of TSVs is difficult to obtain with existing methods. A typical number of TSV interconnections in SiP applications may exceed several hundreds or thousands, as shown in a recent realization in memory chip stacking [22]. Another estimate indicates that I/O interconnection density will be $10^5 - 10^8$ /cm^2, which is compatible with the on-chip density [18]. As discussed in Chapter 1, simple analytical methods [6] are available for characterizing one or two TSVs, but they cannot address general multi-TSV problems. Another way of modeling a large number of TSV interconnections is

using EM simulation tools [85], but computational cost can increase since the meshing of a thin oxide region around a thick and long conductor can lead to a large number of elements.

In order to address the current TSV modeling issues, this chapter proposes an efficient approach that is extended from the integral equation method in Chapters 2 and 3. To consider the oxide coating effect, a new kind of basis function is developed, and a generalized modal equivalent network is constructed. The lossy substrate effect is incorporated by using a complex permittivity model in the SPIE, under the assumption that TSVs are in homogeneous silicon media. The error from neglecting the effect of multilayered substrate is discussed in future work.

The following section introduces a typical TSV structure with its geometrical descriptions and design parameters. Section 5.2 discusses the silicon permittivity model and operation modes of interconnections on silicon substrate. Section 5.3 presents the formulation of integral equation for modeling the oxide coating effects with an extended equivalent circuit model. Section 5.4 shows several TSV modeling examples to validate the proposed method.

5.1 Structure Description

Figure 67 shows a typical direct copper-plug TSV structure in a single silicon substrate. The upper and lower sides of the silicon substrate are covered by oxide layers. Annular oxide coating also fills the gap between conductor and silicon. Since the oxide is a pure insulator, the oxide layers and coating form capacitances that blocks DC current leakage. Usually, the TSV interconnections are fabricated as an array in a silicon carrier and stacked vertically to construct a SiP, as shown in Figure 68.

Fabrication constraints define the available range of TSV dimensions. For example, the oxide thickness is usually from 0.5 to 2 μm, but realizing an oxide layer that is thicker than a few microns is difficult. The height of via conductor depends on the

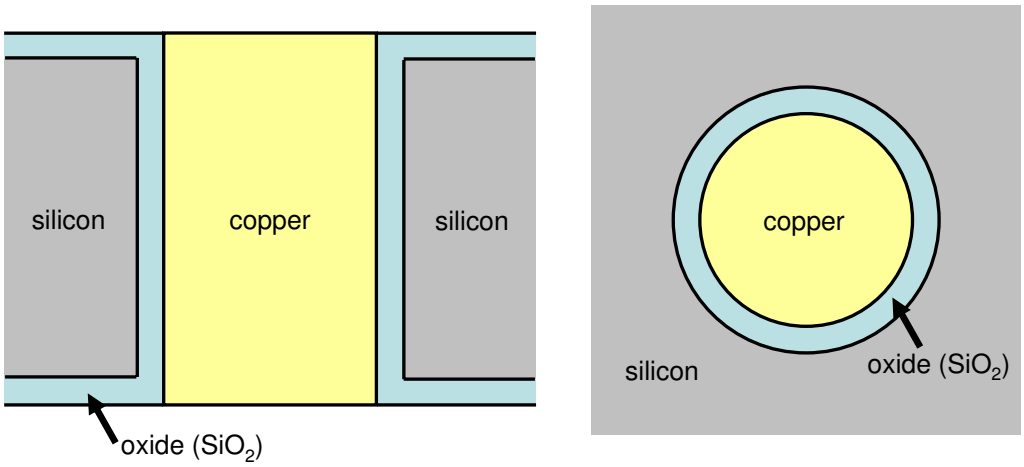


Figure 67. Typical direct Cu-plug TSV structure (left: side view, right: top cross sectional view.)

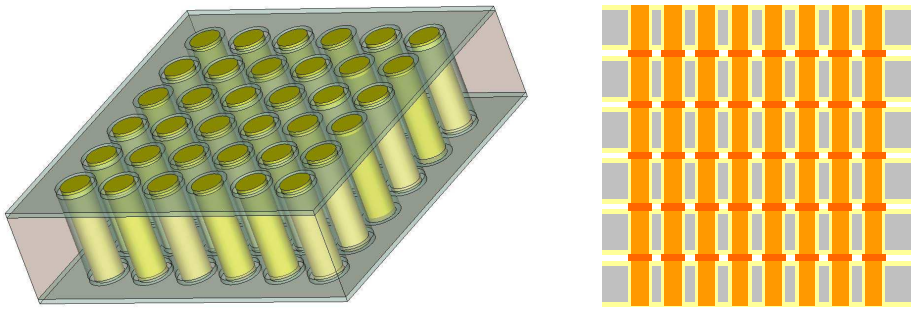


Figure 68. TSV array in a silicon carrier (left) and a stacked ICs with TSV interconnections (right).

substrate thickness, ranging from 20 to 100 μm. The diameter of TSV interconnections can have a diverse range, and a typical interconnection diameter of 25 μm is also popular in TSV design.

An important parameter to characterize TSV performance is the resistivity (or conductivity) of silicon substrate. According to the level of doping, the silicon substrate can be categorized as high resistivity silicon (HRS) or low resistivity silicon (LRS). The electrical behavior of interconnections in silicon strongly depends on the silicon resistivity and frequency, which determine the operation modes of silicon interconnections [25].

5.2 Silicon Permittivity Model and Operation Modes

A major difference between silicon substrate and other (organic or ceramic) packaging substrates is that the silicon substrate has a finite conductivity induced by doping, which may range from 10 to 100 S/m. When constant conductivity is used, the complex permittivity of silicon substrate cannot be expressed by using dielectric loss tangent only, but it should include another complex term that originates from the constant conductivity as follows [86]:

$$\epsilon_{\mathrm{Si}} = \epsilon_0 \epsilon_{\mathrm{Si},i}(1 - j\tan\delta - j\frac{\sigma_{\mathrm{Si}}}{\omega\epsilon_0\epsilon_{\mathrm{Si},i}}), \tag{76}$$

where $\epsilon_{\mathrm{Si},i}$ is the dielectric constant (the real part of complex permittivity), $\tan\delta$ is the intrinsic loss tangent, and σ_{Si} is the conductivity of silicon.

The intrinsic loss tangent ($\tan\delta$) is originated from the dielectric loss of an intrinsic silicon without doping. Thus, $\tan\delta$ represents a loss characteristic of general low-loss dielectrics, which can be expressed by causal dielectric models such as the Debye, Lorentz [87], and Djordjevic-Sarkar models [88]. For simplicity in frequency-domain simulation, a constant $\tan\delta$ model is also effective since the effect of the conductivity σ_{Si} is more significant than the loss tangent in the electrical behavior of TSVs.

The silicon conductivity is determined by the level of doping. Low-doped silicon substrates have similar characteristics to low-loss dielectrics, so their dielectric loss is significant only at high frequencies. Nevertheless, highly-doped silicon (LRS) substrate needs to be used sometimes because of cost considerations in system design. However, the electrical design with LRS-based TSV interconnections is difficult since considerable loss and substrate coupling should be compensated.

The electrical behavior of interconnection on silicon is classified by the following three operation modes [25], according to the operation frequency and resistivity of silicon layer.

- Dielectric quasi-TEM mode: When the resistivity of silicon is high, the high-frequency characteristic of the silicon substrate is almost the same as those of low-loss dielectric substrate. At high frequencies, the effect of conductivity becomes smaller ($\frac{\sigma}{\omega\epsilon}$), and the equivalent interconnection model is similar to the $RLGC$ network of conventional low-loss transmission lines.

- Skin effect mode: When the resistivity of silicon is low, conduction current in the silicon substrate exhibits a crowding distribution as in the case of current in a good conductor at high frequencies. Thus, the return currents flow on the boundary surface of silicon and oxide, and the per-unit-length capacitance of interconnection becomes identical to oxide capacitance.

- Slow-wave mode: For both the low and high resistivity silicon substrate, the low-frequency behavior of interconnections is influenced by the combination of oxide capacitance and silicon conductance. The resultant effect is a large effective dielectric constant, which makes the phase velocity of the interconnection considerably lower.

5.3 TSV Modeling with Cylindrical Modal Basis Functions

For the complete modeling of TSV interconnections, the following interconnection parasitic elements need to be found.

1. Loss and inductive coupling in copper conductors.

2. Substrate loss and capacitive coupling on copper conductor surfaces.

3. Substrate loss and Capacitive coupling on oxide surfaces.

4. Excess capacitance in annular oxide structures.

For extracting conductor loss and inductive coupling (1), the EFIE formulation with cylindrical CMBFs (Chapter 2) can be used directly. Thus, R-L models of the THV

interconnection examples in Section 2.3 can be a part of the TSV interconnection model. After replacing the free-space permittivity with the silicon permittivity, capacitive couplings (2 and 3) can be found from the SPIE with cylindrical AMBFs, which was discussed in Chapter 3. Therefore, this section does not discuss 1, 2 and 3 in detail, and mainly focuses on the excess capacitance extraction in the oxide structure.

The oxide coating between the substrate and TSVs should be considered for accurate analysis of the TSV structures. In the case of planar interconnections mounted on silicon substrate, the planar oxide layer forms a capacitance between the line and silicon, so the oxide effect can be included by using a multilayered Green's function, the transverse resonance method [89], or a spectral domain approach [90]. However, the oxide coating that covers the cylindrical TSV interconnection cannot be expressed with the above methods easily, especially when the number of TSVs is more than two. Thus, the annular oxide structure should be considered as a part of interconnections, but these dielectric interconnections need additional computation to obtain the equivalent circuit parameters. To use the benefit of the reduced number of basis functions, this section extends the original modal basis functions for modeling the annular oxide structures. The idea of modeling TSV interconnections is summarized in Figure 69.

5.3.1 EFIE Formulation in Oxide Region and Cylindrical PMBF

Since no conduction current flows in a dielectric insulator, the electric field based on Ohm's law is not included in the following EFIE [48]:

$$\vec{E}(\vec{r}) + j\omega\frac{\mu}{4\pi}\int_{v'} G(\vec{r},\vec{r'})\vec{J^C}(\vec{r'})dv' + j\omega\frac{\mu}{4\pi}\int_{v'} G(\vec{r},\vec{r'})\epsilon_0(\epsilon_{ox}-\epsilon_{\mathrm{Si}})j\omega\vec{E}dv' = -\nabla\Phi, \tag{77}$$

where $\vec{E}(\vec{r})$ is the electric field in the oxide region. Since the oxide thickness is usually thin relative to the other dimensions of a TSV structure, the electric field is assumed to have radial (ρ) and angular (φ) directions only. Thus, the conduction

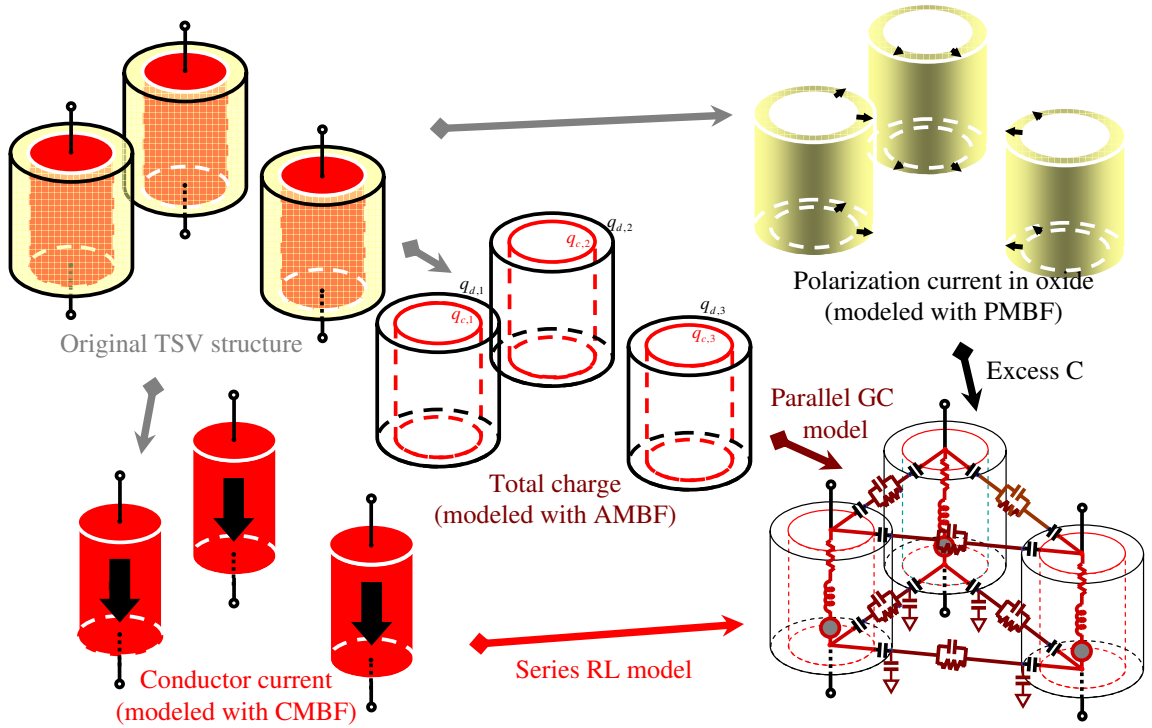


Figure 69. TSV modeling idea using cylindrical modal basis functions. (Some of components in the equivalent circuit are omitted for simplicity.)

current $\vec{J^C}(\vec{r'},\omega)$ is perpendicular to the polarization current, and the first integral term becomes zero. After replacing the polarization current by $\vec{J^P}(\vec{r},\omega) = j\omega\epsilon_0(\epsilon_{ox} - \epsilon_{\mathrm{Si}})\vec{E}(\vec{r})$, (77) is reduced to the following form:

$$\frac{\vec{J^P}(\vec{r},\omega)}{j\omega\epsilon_0(\epsilon_{ox}-\epsilon_{\mathrm{Si}})} + j\omega\frac{\mu}{4\pi}\int_{v'} G(\vec{r},\vec{r'})\vec{J^P}(\vec{r},\omega)dv' = -\nabla\Phi. \tag{78}$$

Extending the modal basis concept, we can approximate the polarization current density as follows:

$$\vec{J^P}(\vec{r},\omega) \simeq \sum_{j,n,q} I_{jnq}\vec{u}_{jnq}(\vec{r}_j). \tag{79}$$

By applying the inner product based on Galerkin's method, following equation is obtained:

$$\sum_{j,n,q} I_{jnq}\frac{1}{j\omega C^{ex}_{imd,jnq}} + \sum_{j,n,q} j\omega L_{imd,jnq}I_{jnq} = \int_{V_i}\vec{u}_{imd}\cdot(-\nabla\Phi)dV_i, \tag{80}$$

where

$$C^{ex}_{imd,jnq} = \frac{\epsilon_0(\epsilon_{ox}-\epsilon_{\mathrm{Si}})}{\int_{V_i}\vec{u}_{imd}\cdot\vec{u}_{jnq}dV_i},$$

$$L_{imd,jnq} = \frac{\mu}{4\pi}\int_{V_i}\int_{V_j} G(\vec{r_i},\vec{r_j})\vec{u}_{imd}(\vec{r_i})\cdot\vec{u}_{jnq}(\vec{r_j})dV_j dV_i.$$

Here, we have to define proper basis functions and terminal voltage terms. In the annular insulators, the inner surface of which contacts the conductor, the solution of the Laplace's equation is expressed as follows [65]:

$$\Phi_n(\rho,\varphi) = \begin{cases} A_0 + B_0 \ln\rho & n = 0 \\ \big(-(\frac{\rho}{\rho_c})^n + (\frac{\rho}{\rho_c})^{-n}\big)(A_n\cos n\varphi + B_n \sin n\varphi) & n > 0 \end{cases}. \quad (81)$$

These potential components contribute to a capacitive voltage drop, not the total voltage drop across the interconnect. The electric field from the above potential is expressed as follows:

$$-\nabla\Phi_n(\rho,\varphi) = \begin{cases} \frac{B_0}{\rho}\hat{\rho} & n = 0 \\ n\{\frac{\rho^{n-1}}{\rho_c^n} + \frac{\rho^{-n-1}}{\rho_c^{-n}}\}(A_n\cos n\varphi + B_n\sin n\varphi)\hat{\rho} & \\ \quad + n\{\frac{\rho^{n-1}}{\rho_c^n} - \frac{\rho^{-n-1}}{\rho_c^{-n}}\}(-A_n\sin n\varphi + B_n\cos n\varphi)\hat{\varphi} & n > 0 \end{cases}. \quad (82)$$

For higher-order modes ($n > 0$), we can rewrite the following "direct" and "quadrature" fields:

$$-\nabla\Phi_n(\rho,\varphi) = \vec{E}_d + \vec{E}_q, \quad (83)$$

where

$$\vec{E}_d = \frac{P_n(\rho/\rho_c)}{\rho}\cos n\varphi\hat{\rho} - \frac{Q_n(\rho/\rho_c)}{\rho}\sin n\varphi\hat{\varphi},$$

$$\vec{E}_q = \frac{P_n(\rho/\rho_c)}{\rho}\sin n\varphi\hat{\rho} + \frac{Q_n(\rho/\rho_c)}{\rho}\cos n\varphi\hat{\varphi},$$

$$P_n(\rho/\rho_c) = n\{\frac{\rho^n}{\rho_c^n} + \frac{\rho^{-n}}{\rho_c^{-n}}\},$$

and

$$Q_n(\rho/\rho_c) = n\{\frac{\rho^n}{\rho_c^n} - \frac{\rho^{-n}}{\rho_c^{-n}}\}.$$

Therefore, we can define the following modal basis functions:

$$\vec{u}_{imd}(\rho,\varphi)=\begin{cases}\frac{1}{A_{i0}}\frac{\rho_c}{\rho}\hat{\rho} & m=0\\ \frac{1}{A_{imd}\times\rho}\big\{[P_m(\rho/\rho_c)\cos m\varphi]\hat{\rho}-[Q_m(\rho/\rho_c)\sin m\varphi]\hat{\varphi}\big\} & m>0, d-\text{mode}\\ \frac{1}{A_{imq}\times\rho}\big\{[P_m(\rho/\rho_c)\sin m\varphi]\hat{\rho}+[Q_m(\rho/\rho_c)\cos m\varphi]\hat{\varphi}\big\} & m>0, q-\text{mode}\end{cases}. \tag{84}$$

The normalization parameters $A_{i0} and A_{imd}$ are found so that the coefficient I_{imd} is an actual modal polarization current in amperes. For $m=0$,

$$\int_{S_d}\vec{u}_{i0}\cdot d\vec{S}=1, \tag{85}$$

where S_d is the surface boundary between the thin dielectric and the surrounding media. Although the integration surface can be defined as the boundary between the insulator and the conductor, using S_d makes the final formulation more simple. The resultant normalization coefficient is:

$$A_{i0}=2\pi\rho_c l_i. \tag{86}$$

In case of higher-order modes, the same integral over the entire peripheral region is zero, so we define the normalization factor as follows:

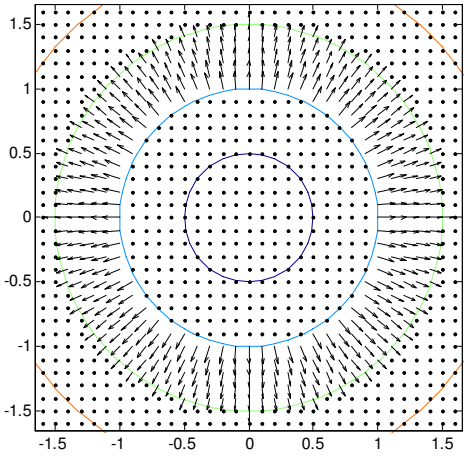
$$\int_{S_d^+}\vec{u}_{imd}\cdot d\vec{S}=\frac{1}{2m}. \tag{87}$$

Therefore,

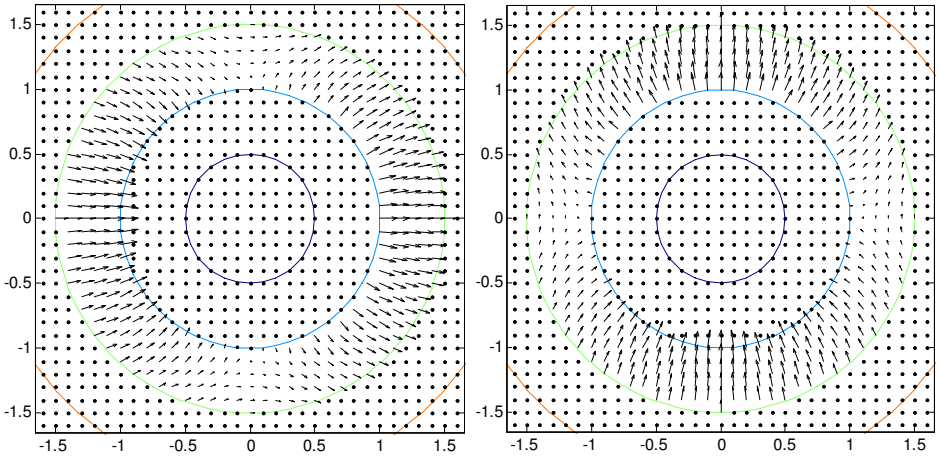
$$A_{imd}=4l_iP_m\big(\frac{\rho_d}{\rho_c}\big)=4l_im\big\{\frac{\rho_d^m}{\rho_c^m}+\frac{\rho_d^{-m}}{\rho_c^{-m}}\big\}. \tag{88}$$

The new modal basis functions capture polarization current density in the insulator region, and therefore can be called cylindrical polarization mode basis functions (PMBFs). Figure 70 shows plots of the PMBF from the fundamental to the second mode.

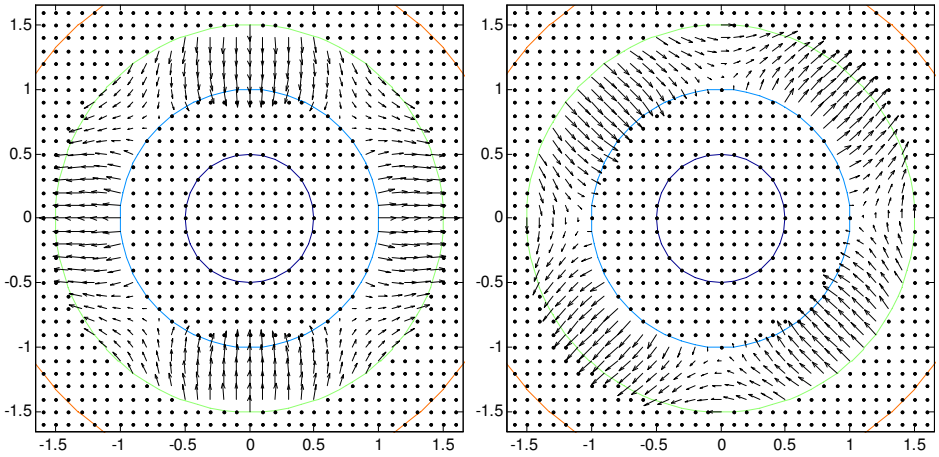
Using the defined normalization factors, we obtain the following modal excess capacitances. From the orthogonal and local properties of basis functions, there are



(a) fundamental



(b) first order



(c) second order

Figure 70. Example plots of cylindrical PMBFs when conductor radius is 1 and insulator radius is 1.5.

no off-diagonal terms.

$$C_{ex,imd} = \frac{\epsilon_0[\epsilon_r - \epsilon_B]}{\int_{V_i} \vec{u}_{imd} \cdot \vec{u}_{imd} dV_i} = \begin{cases} \frac{2\pi l_i \epsilon_0(\epsilon_r - \epsilon_B)}{\ln \frac{\rho_d}{\rho_c}} & m = 0 \\ \frac{16 m l_i \epsilon_0(\epsilon_r - \epsilon_B)}{\pi \frac{Q_m(\rho_d/\rho_c)}{P_m(\rho_d/\rho_c)}} & m > 0 \end{cases} . \tag{89}$$

Interestingly, the fundamental mode excess capacitance is identical to the capacitance of a coaxial cylinder having an inner radius of ρ_c and an outer radius of ρ_d.

The following modal self and mutual inductance can be calculated using techniques similar to those used in the calculations where the conduction mode basis functions are involved:

$$L_{imd,jnq} = \frac{\mu}{4\pi} \int_{V_i} \int_{V_j} G(\vec{r_i}, \vec{r_j}) \vec{u}_{imd}(\vec{r_i}) \cdot \vec{u}_{jnq}(\vec{r_j}) dV_j dV_i. \tag{90}$$

However, the inductance across the thin insulator is negligible since the ratio of the oxide thickness to the cylindrical area is small. In the TSV design, the oxide thickness cannot exceed a few microns, but the cylindrical area can be over 1000 μm^2. Therefore, the oxide inductances can be considered as a secondary effect.

The modal voltage difference is formulated as follows, by using the vector identity $\nabla \cdot (\Psi \vec{A}) = \Psi \nabla \cdot \vec{A} + \vec{A} \cdot \nabla \Psi$:

$$\int_{V_i} \vec{u}_{imd} \cdot (-\nabla \Phi) dV_i = \int_{V_i} \Phi \nabla \cdot \vec{u}_{imd} - \nabla \cdot (\Phi \vec{u}_{imd}) dV_i. \tag{91}$$

Since $\nabla \cdot \vec{u}_{imd}$ should be zero, only the second term of the right part of the above formula remains, and we can apply the divergence theorem. Therefore,

$$\int_{V_i} \vec{u}_{imd} \cdot (-\nabla \Phi) dV_i = - \oint_{S_i} (\Phi \vec{u}_{imd}) \cdot d\vec{S}. \tag{92}$$

Since we assume that the polarization current has no z component, (92) is reduced to surface integrals over S_c and S_d shown in Figure 71. On S_c, the electric potential is fixed to a constant value (Dirichlet boundary condition), which is defined as Φ_c^i. On the dielectric interface S_d, the potential cannot be fixed to a constant, but should be

a function of φ. Therefore, the final expression of the modal voltage difference is as follows:

$$\Delta V_{imd} = -\int_{S_C} \Phi_i^C \vec{u}_{imd} \cdot \hat{n}_c \rho_c d\varphi dz - \int_{S_D} \Phi_i^D(\varphi) \vec{u}_{imd} \cdot \hat{n}_d \rho_d d\varphi dz, \tag{93}$$

where $\Phi_i^D(\varphi) = \Phi_{i0}^D + \frac{4}{\pi} \sum_{m=1} [\Phi_{imd}^D \cos n\varphi + \Phi_{imq}^D \sin m\varphi]$.

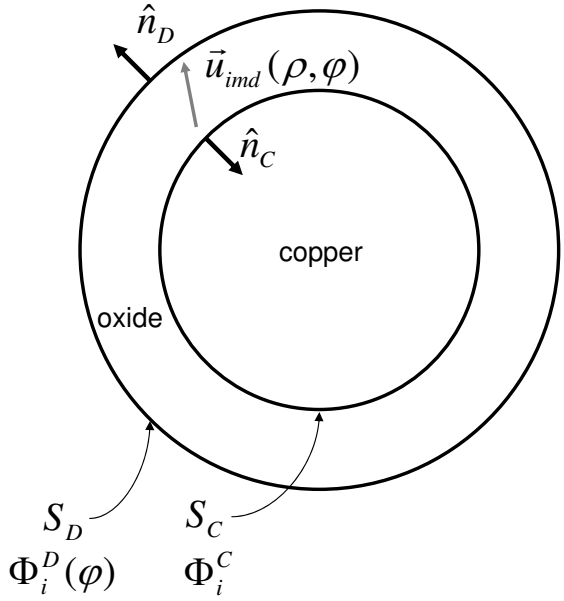


Figure 71. Potential definitions on surfaces in a TSV cross section.

When $m = 0$,

$$\Delta V_{imd} = +\Phi^C - \Phi_{i0}^D, \tag{94}$$

which means that the modal voltage difference is the difference between the actual conductor voltage and the fundamental mode of the dielectric interface potential. When $m > 0$,

$$\Delta V_{imd} = 0 - \frac{1}{A_{imd}} \int_{S_D} \Phi_i^D(\varphi) P_m(\rho_d/\rho_c) \cos m\varphi d\varphi dz = -\Phi_{imd}^D. \tag{95}$$

In case of good conductor interconnections, the modal voltage difference involving the higher-order basis is zero, so the equivalent circuit forms a closed loop, as discussed in Chapter 2. However, when an insulator is involved, the higher-order modal voltage difference is the higher-order voltage drop of the dielectric interface. The actual

value of the higher-order voltage is not determined here, but can be found from the formulation combined with the SPIE involving the bound charges in the insulator boundary.

5.3.2 SPIE Formulation on Conductor and Insulator Surfaces

Equation (53) in Section 3.3 shows that SPIE involves the total charge that includes free and bound charge. In the case of TSV interconnections, the conductor boundary contains free charge and bound charge, but the insulator boundary contains bound charge only. Therefore, total charge density distributions on conductor and insulator boundary are assigned as follows:

$$q^C = \sum_{kmd} Q^C_{kmd} v^C_{kmd}, \tag{96}$$

$$q^D = \sum_{kmd} Q^D_{kmd} v^D_{kmd}, \tag{97}$$

where $q^{C,D}$ is total surface charge density distributions, $v^{C,D}_{kmd}$ is cylindrical AMBFs, and superscripts C and D represent the conductor surface (S_C) and the insulator surface (S_D), respectively.

Using the above modal expansions, the coefficients of potential are obtained in the same way as discussed in Chapter 3, except that the modal potential expression in the insulator boundary is not the same as that in the conductor boundary. That is, the equivalent circuit equation for the kmd-th mode is as follows:

$$\sum_{lnq} P^D_{kmd,lnq} Q_{lnq} = \Phi^D_{kmd}. \tag{98}$$

Therefore, the capacitive coupling expressed in (98) is directly connected to the voltage difference in (95).

5.3.3 Equivalent Circuit and Matrix Formulation

Summarizing all the relations of modal circuit elements regarding conductor R-L model, insulator excess capacitance model, and coefficient of potential models, we obtain the following matrix equations.

1. Conductor series impedance equation: The series resistance and inductance results in the voltage drop across a via conductor, which represents the same equivalent model shown in Chapter 2.

$$\begin{pmatrix} \mathbf{Z_{ss}} & \mathbf{Z_{sp}} \\ \mathbf{Z_{ps}} & \mathbf{Z_{pp}} \end{pmatrix} \begin{pmatrix} \mathbf{I_s} \\ \mathbf{I_p} \end{pmatrix} = \begin{pmatrix} \mathbf{\Delta \Phi^C} \\ \mathbf{0} \end{pmatrix}. \tag{99}$$

2. Insulator parallel impedance equation: The equivalent modal impedance shown in Section 5.3.1 contributes to the voltage drop across the oxide coating as follows:

$$\begin{pmatrix} \mathbf{Z_{ss}^{ex}} & \mathbf{Z_{sp}^{ex}} \\ \mathbf{Z_{ps}^{ex}} & \mathbf{Z_{pp}^{ex}} \end{pmatrix} \begin{pmatrix} \mathbf{I_s^{pol}} \\ \mathbf{I_p^{pol}} \end{pmatrix} = \begin{pmatrix} \mathbf{\Phi^C - \Phi_s^D} \\ \mathbf{-\Phi_p^D} \end{pmatrix}, \tag{100}$$

where

$$\mathbf{Z^{ex}} \simeq \frac{1}{j\omega} \mathbf{C^{ex-1}}$$

and $\mathbf{I_{s,p}^{pol}}$ are the modal polarization current vectors.

3. Coefficients of potential equation: Equations (96) and (97) are combined to the following matrix equation, which represents the capacitive coupling among charges on conductor insulator surfaces. The fundamental modes and higher-order modes are also indicated.

$$\begin{pmatrix} \mathbf{P_{ss}^{C}} & \mathbf{P_{sp}^{C}} & \mathbf{P_{ss}^{CD}} & \mathbf{P_{sp}^{CD}} \\ \mathbf{P_{ps}^{C}} & \mathbf{P_{pp}^{C}} & \mathbf{P_{ps}^{CD}} & \mathbf{P_{pp}^{CD}} \\ \mathbf{P_{ss}^{DC}} & \mathbf{P_{sp}^{DC}} & \mathbf{P_{ss}^{D}} & \mathbf{P_{sp}^{D}} \\ \mathbf{P_{ps}^{DC}} & \mathbf{P_{pp}^{DC}} & \mathbf{P_{ps}^{D}} & \mathbf{P_{pp}^{D}} \end{pmatrix} \begin{pmatrix} \mathbf{Q_s^C} \\ \mathbf{Q_p^C} \\ \mathbf{Q_s^D} \\ \mathbf{Q_p^D} \end{pmatrix} = \begin{pmatrix} \mathbf{\Phi_s^C} \\ \mathbf{0} \\ \mathbf{\Phi_s^D} \\ \mathbf{\Phi_p^D} \end{pmatrix}. \tag{101}$$

4. Matrix form of continuity equations: The matrix equations from (99) to (101), which come from EFIEs and SPIEs, are linked to the continuity equations or KCL. Firstly, current in conductor cells should satisfy the continuity relation

with the free charge on the conductor surface. Therefore,

$$\begin{pmatrix} -\mathbf{E} & \boldsymbol{\Delta}_\mathbf{i} \end{pmatrix} \begin{pmatrix} \mathbf{I_t} \\ \mathbf{I_s} \end{pmatrix} + j\omega(\mathbf{Q_s^C} + \mathbf{Q_s^D}) = 0, \tag{102}$$

where $\mathbf{Q_s^C} + \mathbf{Q_s^D}$ is the free charge on the conductor surface. The above equation is identical to (61) in Chapter 3, where the terminal current $\mathbf{I_t}$ becomes the forcing term in the global matrix equation. The other continuity relation should be satisfied on the insulator surface as follows:

$$\begin{pmatrix} \mathbf{I_s^{pol}} \\ \mathbf{I_p^{pol}} \end{pmatrix} + j\omega \begin{pmatrix} \mathbf{Q_s^D} \\ \mathbf{Q_p^D} \end{pmatrix} = 0. \tag{103}$$

The above equation indicates that the polarization currents should be continuous with the time variation of the bound charge on the insulator surface.

For obtaining Z parameters, we assign the terminal current $\mathbf{I_t}$ as a known value, and then solve the following combined matrix equation:

$$\begin{pmatrix}
\mathbf{Z_{ss}} & \mathbf{Z_{sp}} & & & -\boldsymbol{\Delta}_\mathbf{v} & & & & & & \\
\mathbf{Z_{ps}} & \mathbf{Z_{pp}} & & & & & & & & & \\
 & & \mathbf{Z_{ss}^{ex}} & \mathbf{Z_{sp}^{ex}} & -\mathbf{E} & \mathbf{E} & & & & & \\
 & & \mathbf{Z_{ps}^{ex}} & \mathbf{Z_{pp}^{ex}} & & & \mathbf{E} & & & & \\
\boldsymbol{\Delta}_\mathbf{i} & & & & & & & j\omega\mathbf{E} & & j\omega\mathbf{E} & \\
 & & \mathbf{E} & & & & & & & -j\omega\mathbf{E} & \\
 & & & \mathbf{E} & & & & & & & -j\omega\mathbf{E} \\
 & & & & -\mathbf{E} & & & \mathbf{P_{ss}^C} & \mathbf{P_{sp}^C} & \mathbf{P_{ss}^{CD}} & \mathbf{P_{sp}^{CD}} \\
 & & & & & & & \mathbf{P_{ps}^C} & \mathbf{P_{pp}^C} & \mathbf{P_{ps}^{CD}} & \mathbf{P_{pp}^{CD}} \\
 & & & & & -\mathbf{E} & & \mathbf{P_{ss}^{DC}} & \mathbf{P_{sp}^{DC}} & \mathbf{P_{ss}^D} & \mathbf{P_{sp}^D} \\
 & & & & & & -\mathbf{E} & \mathbf{P_{ps}^{DC}} & \mathbf{P_{pp}^{DC}} & \mathbf{P_{ps}^D} & \mathbf{P_{pp}^D}
\end{pmatrix}
\begin{pmatrix} \mathbf{I_s} \\ \mathbf{I_p} \\ \mathbf{I_s^{pol}} \\ \mathbf{I_p^{pol}} \\ \boldsymbol{\Phi}^\mathbf{C} \\ \boldsymbol{\Phi}_\mathbf{s}^\mathbf{D} \\ \boldsymbol{\Phi}_\mathbf{p}^\mathbf{D} \\ \mathbf{Q_s^C} \\ \mathbf{Q_p^C} \\ \mathbf{Q_s^D} \\ \mathbf{Q_p^D} \end{pmatrix}
= \begin{pmatrix} \\ \\ \\ \\ \mathbf{I_t} \\ \\ \\ \\ \\ \\ \end{pmatrix}, \tag{104}$$

where unassigned elements are all zeros. The matrix equations can be expressed by an equivalent circuit model shown in Figure 72, which includes series conductor impedances, capacitive couplings, and excess capacitance in the oxide coating. The addition of the excess capacitance and the capacitance from SPIEs should provide the actual oxide capacitance depending on the oxide permittivity only. However, the

assumption that no axial electric field exists in the oxide region may not match with the full capacitive coupling model from SPIE. This mismatch causes fictitious loss, which should be corrected.

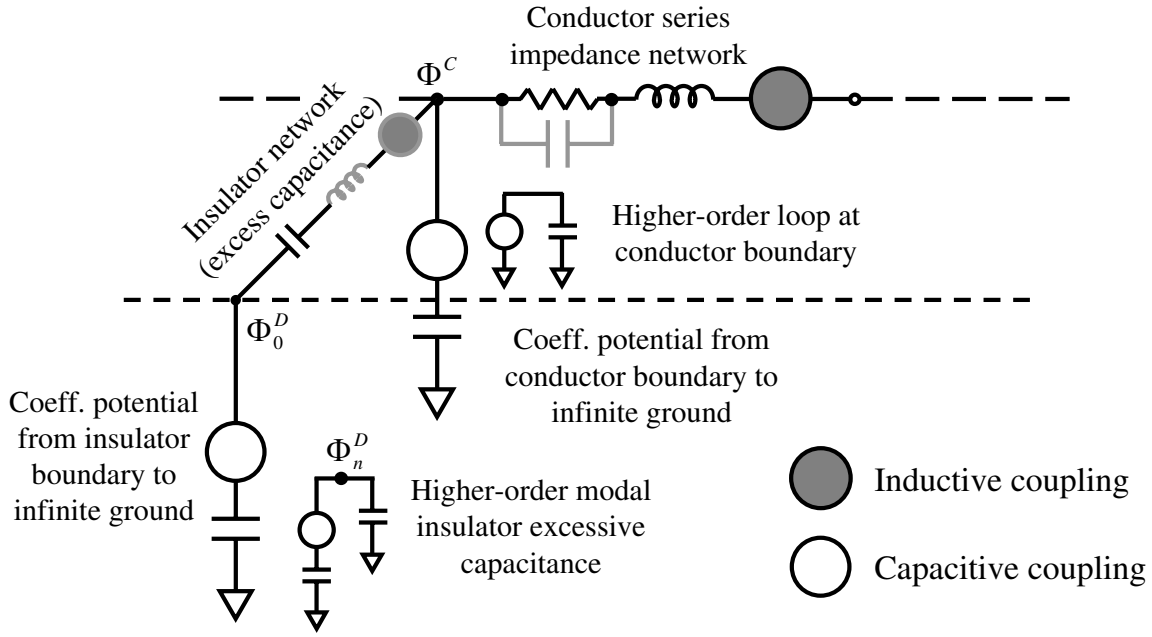


Figure 72. Modal equivalent circuit of TSV interconnections.(Higher-order loops for inductive proximity effect are omitted.)

5.3.4 Generalized Excess Modal Capacitances

The modal excess capacitor in the oxide region (89) is obtained under the assumption that the electric field has radial and angular directional components only. However, the assumption is not correct when a TSV interconnection is divided into several capacitive cells. The neighboring cells have capacitive couplings coming from the axial electric fields, so the additional coupling should be compensated with more accurate excess capacitances. The alternative way to obtain the excess capacitances is discussed by reformulating the matrix equations in the previous subsection.

Instead of solving the global matrix equation (104) directly, we can eliminate the internal current and charge vectors in (99-102) to obtain the following reduced matrix

equation relating the terminal currents and conductor potentials:

$$(\mathbf{Y_c} + j\omega\mathbf{C^{eq}})\mathbf{\Phi^C} = \mathbf{I^t}. \tag{105}$$

$\mathbf{Y_c}$ is an admittance matrix contributed by the conductor impedances and is defined as follows.

$$\mathbf{Y_c} = \mathbf{\Delta_{I,T}}\mathbf{Z_c^{-1}}\mathbf{\Delta_{V,T}}, \tag{106}$$

where

$$\mathbf{\Delta_{I,T}} = \begin{pmatrix} \mathbf{\Delta_I} & \mathbf{0} \end{pmatrix}, \mathbf{\Delta_{V,T}} = \begin{pmatrix} \mathbf{\Delta_V} \\ \mathbf{0} \end{pmatrix},$$

and

$$\mathbf{Z_c} = \begin{pmatrix} \mathbf{Z_{ss}} & \mathbf{Z_{sp}} \\ \mathbf{Z_{ps}} & \mathbf{Z_{pp}} \end{pmatrix}.$$

$\mathbf{C^{eq}}$ represents the matrix including all the capacitances from the conductor and the insulator cells, and the excess oxide capacitances.

$$\mathbf{C^{eq}} = \mathbf{C_C^{eq}} - \mathbf{C_{CD}^{eq}}\mathbf{C_D^{eq-1}}\mathbf{C_{DC}^{eq}}, \tag{107}$$

where

$$\begin{pmatrix} \mathbf{C_C^{eq}} & \mathbf{C_{CD}^{eq}} \\ \mathbf{C_{DC}^{eq}} & \mathbf{C_D^{eq}} \end{pmatrix} = \begin{pmatrix} \mathbf{Cp^C} & \mathbf{Cp^{CD}} \\ \mathbf{Cp^{DC}} & \mathbf{Cp^D} \end{pmatrix} + \begin{pmatrix} \mathbf{C^{ex}} & \mathbf{-C^{ex}} \\ \mathbf{-C^{ex}} & \mathbf{C^{ex}} \end{pmatrix}$$

and

$$\begin{pmatrix} \mathbf{Cp^C} & \mathbf{Cp^{CD}} \\ \mathbf{Cp^{DC}} & \mathbf{Cp^D} \end{pmatrix} = \begin{pmatrix} \mathbf{P_{ss}^C} & \mathbf{P_{sp}^C} & \mathbf{P_{ss}^{CD}} & \mathbf{P_{sp}^{CD}} \\ \mathbf{P_{ps}^C} & \mathbf{P_{pp}^C} & \mathbf{P_{ps}^{CD}} & \mathbf{P_{pp}^{CD}} \\ \mathbf{P_{ss}^{DC}} & \mathbf{P_{sp}^{DC}} & \mathbf{P_{ss}^D} & \mathbf{P_{sp}^D} \\ \mathbf{P_{ps}^{DC}} & \mathbf{P_{pp}^{DC}} & \mathbf{P_{ps}^D} & \mathbf{P_{pp}^D} \end{pmatrix}^{-1}.$$

Equation (107) shows that the capacitance between the conductor and the insulator cells are replaced by the excess capacitance. Thus, the oxide capacitance with the permittivity of ϵ_{ox} connects the connector nodes and the insulator nodes. If the excess capacitance matrix is considering only the direct coupling between two facing

cells, the resulting matrix $\mathbf{C^{eq}}$ has the complex permittivity in the oxide capacitor, which provides additional loss. This modeling defect can be addressed by redefining the excess capacitance matrix as follows.

$$\mathbf{C^{ex}} = -\frac{\epsilon_{ox} - \epsilon_{\mathrm{Si}}}{\epsilon_{\mathrm{Si}}}\mathbf{Cp^{CD}}. \tag{108}$$

By using the above expression, the excess capacitance completely removes the complex permittivity in the oxide region.

5.4 Validation

This section applies the proposed TSV modeling method to various structures. At first, to observe the effect of the oxide coating, cylindrical structures with annular oxide coatings are validated in free space. Then the silicon background is included, and three TSV interconnections are simulated and compared with data in existing references or measurement data. Finally, in order to show the generality of the proposed method, TSV array structures are simulated. The origins of the errors from the proposed method are also discussed.

5.4.1 Effect of Oxide Coating without Silicon Substrate

Figure 73 shows the geometry of two oxide-coated cylindrical interconnections. In free space, we can observe the pure effect of oxide coating on the characteristics of via interconnections by testing the cases with or without the oxide coating. The thickness of oxide (d_{ox}) is 20 μm, which is rather thick compared to the diameter of conductor ($D = 100\mu$m). Interconnection length (L) and pitch (D) are 1000 μm and 150 μm, respectively.

2-D analytical methods to calculate the capacitance between two parallel conductors can be used to obtain analytical results. When the oxide layer is removed, the problem is reduced to a simple two cylindrical conductor problem, the analytical

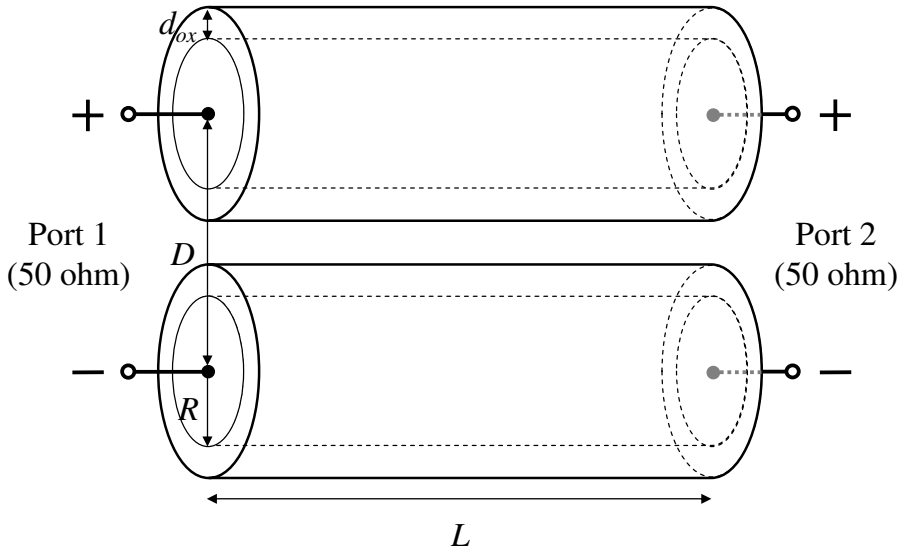


Figure 73. Geometry and electrical configuration of two via interconnections with oxide coating in free space.

solution of which is well known [59]. Two parallel cylindrical conductors with annular dielectrics can be calculated by using a conformal mapping technique [91]. For both cases, the per-unit-length inductances are assumed to be identical because the inductive coupling is not influenced by the oxide coating.

Comparing S parameter data of the proposed method to the analytical formula shows good correlation, as shown in Figure 74. Since the addition of the oxide coating modifies the capacitance between two interconnections, the characteristic impedance is changed. Although the effect of oxide coating on the variation of S parameters seems small in this example, the effect can be emphasized in lossy dielectric surroundings as shown in the next example.

5.4.2 Three TSV Interconnections

The proposed method with the silicon permittivity model was applied to a three-TSV structure problem, which is shown in Figure 75. The original setup of the geometry and electrical configuration can be found in [6], where S parameters are obtained from measurements and simulations with a commercial 3-D EM simulator. As the background media, silicon substrate has the conductivity of 10 S/m and dielectric

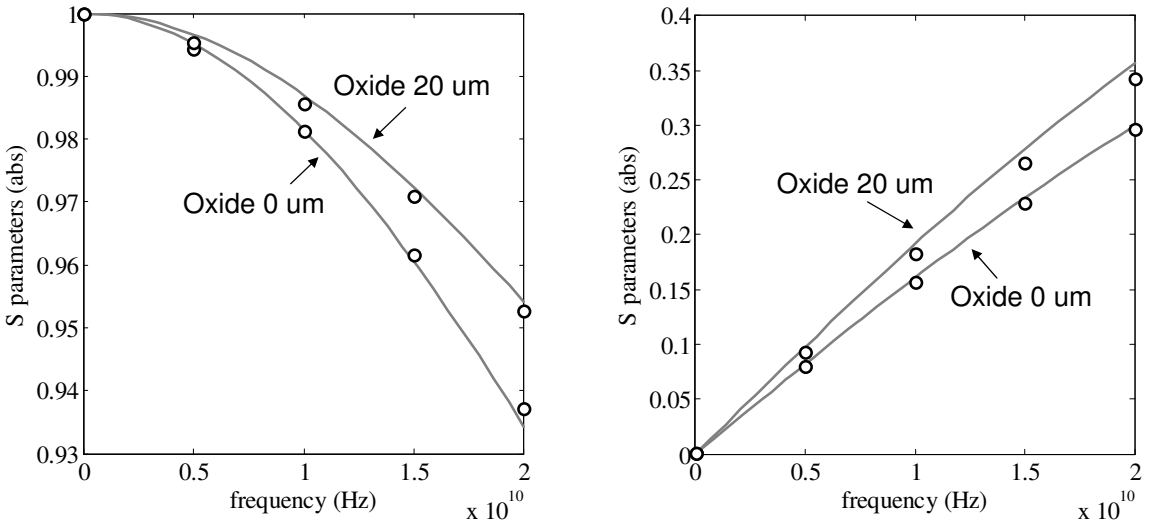


Figure 74. S-parameter results (left: insertion loss, right: return loss, solid lines: analytic transmission line, dots: proposed method).

constant of 11.9. These material parameters were used in the complex permittivity formula (76). Copper radius (R), pitch (D), and conductor length (L) were fixed to 50 μm, 150 μm, and 100 μm, respectively. To observe the effect of the oxide layer, three cases (0.1, 1, and 10 μm) of the oxide thickness (d_{ox}) were simulated. As shown in Figure 75, the center via interconnection was used as a signal path, and the other two vias were used as ground path. From the GSG signaling, 2-port S parameters were obtained.

Figure 76 shows insertion losses obtained from the proposed modeling method for three TSV interconnections with three different oxide thicknesses. The frequency-dependent behaviors show the effects of various oxide thicknesses clearly, and they show similar trends with the 3-D EM simulation results in [6]. When the oxide thickness is small (0.1 μm), the insertion loss increases sharply at low frequencies, but the increase becomes slower from about 1 GHz. The high-frequency insertion loss is about 1.8 dB, which is a rather high value for the interconnection length of 100-μm. As the oxide thickness increases, the trend of insertion loss over frequency becomes smooth like interconnections in low-loss dielectric substrates.

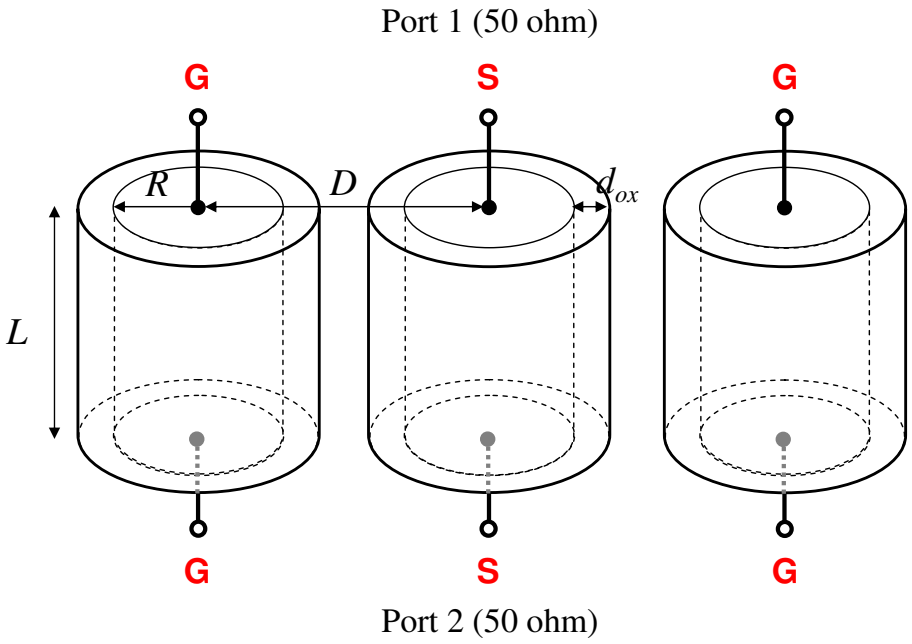


Figure 75. Three TSV interconnections.

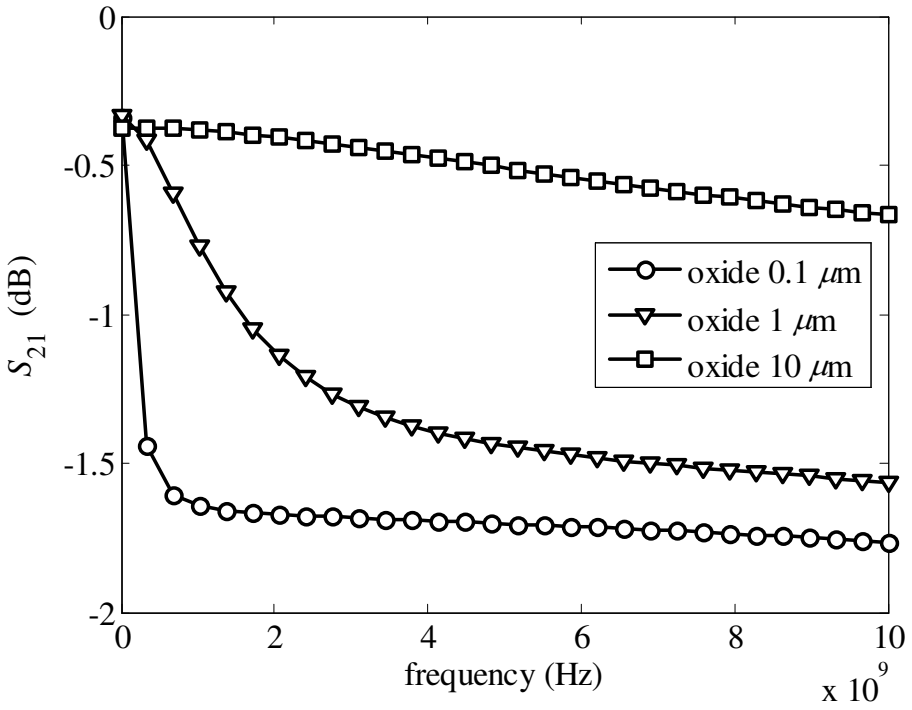


Figure 76. Insertion losses of the three TSV interconnections with different oxide thicknesses.

A main difference between the results of the proposed method and 3-D EM simulation results is the non-zero loss of about -0.4 dB at DC. Although the conductor DC

resistance may contribute to the DC loss, its high conductivity makes the conductor DC loss negligible. The origin of the finite DC loss is from the use of the homogeneous media Green's function. With the homogeneous media assumption, the TSV interconnections are surrounded by the lossy silicon, and the two ends of the copper conductor are exposed to silicon directly. Thus, DC leakage currents flow through the edge of the interconnections, causing DC loss due to the silicon conductance. However, the TSV structure is exposed to the oxide layer and air as shown in Figure 67, so the DC leakage current does not exist.

5.4.3 Coupling Characteristics of TSV Array

Extending the previous example, a 5-by-5 TSV array structure shown in Figure 77 was simulated to observe the coupling effects from nearby via interconnections. Based on the same via dimensions as the previous example, the following cases were tested for comparison.

1. THV array (in free space).
2. TSV array with thin oxide layer ($\sigma_{\mathrm{Si}} = 10$ S/m, oxide thickness $= 0.1\mu$m).
3. TSV array with thick oxide layer ($\sigma_{\mathrm{Si}} = 10$ S/m, oxide thickness $= 10\mu$m).

For all cases, the length and diameter of each via interconnection were 100 μm and 30 μm, respectively. The pitch between via interconnections is 60 μm.

Figure 78 compares insertion losses of all via interconnections for three cases. Assuming all the via interconnections as single-ended interconnections, the resultant 50-port S parameters were calculated. The negligible insertion losses of the THV array are predictable since the interconnection length is too small to have significant parasitic effects. However, the insertion losses of TSV arrays are much higher with the same interconnection length because of the effect of substrate conductivity. As shown in the three-TSV case of the previous subsection, the oxide thickness also decides the

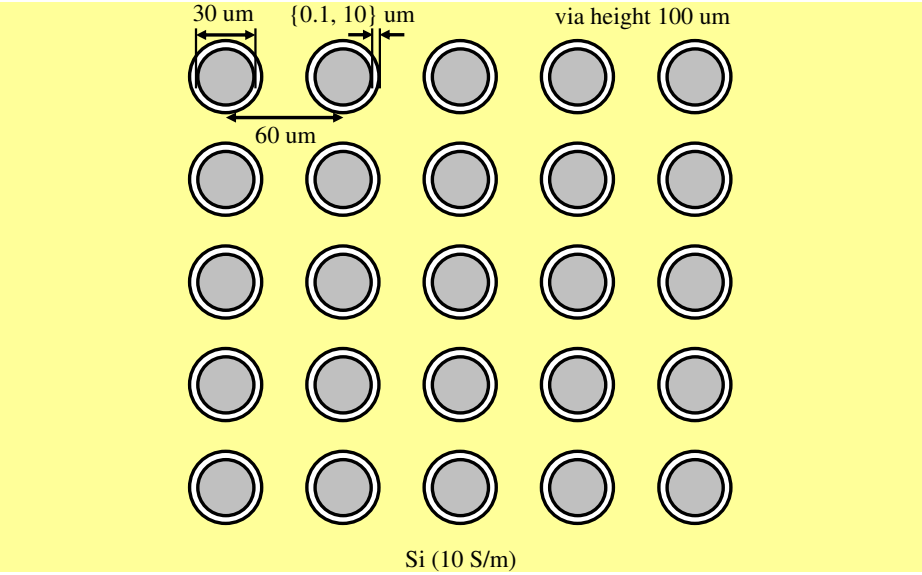


Figure 77. 5-by-5 TSV array configuration.

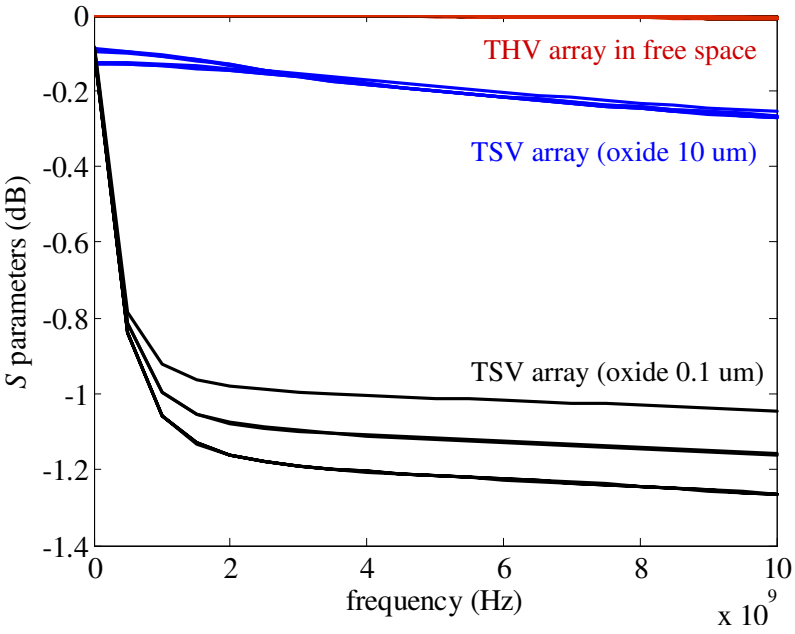


Figure 78. Insertion losses of THV and TSV arrays.

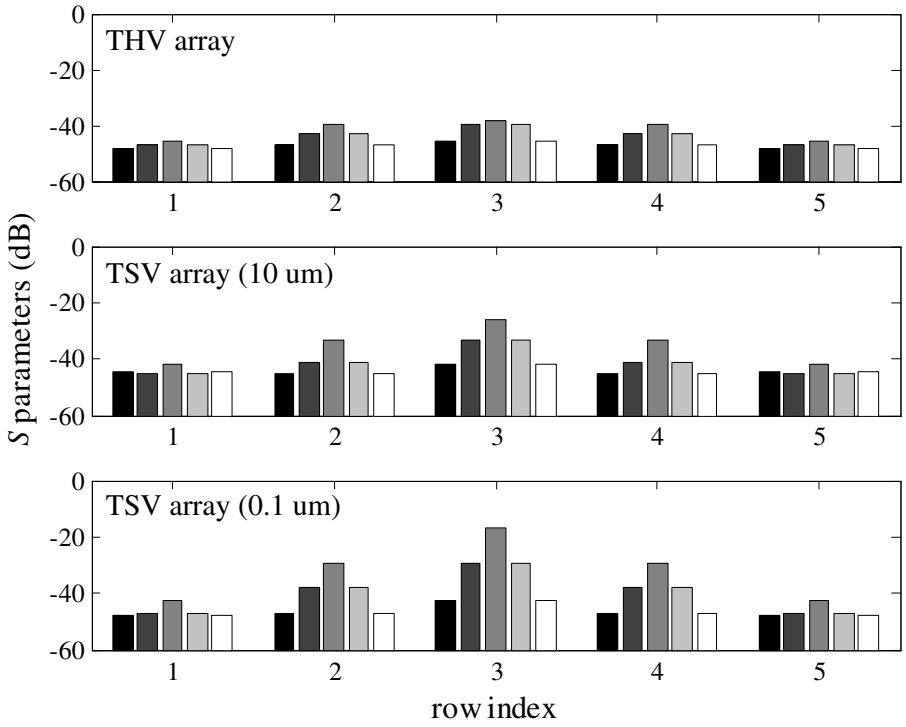
level of the insertion loss. Figure 78 shows that using the thicker oxide layer is helpful to reduce the insertion loss.

Figure 79 shows the entire S parameters at 10 GHz to observe the coupling between via interconnections. Since the coupling levels are related to the insertion losses in Figure 78, the coupling from TSV interconnections are higher than those of THV

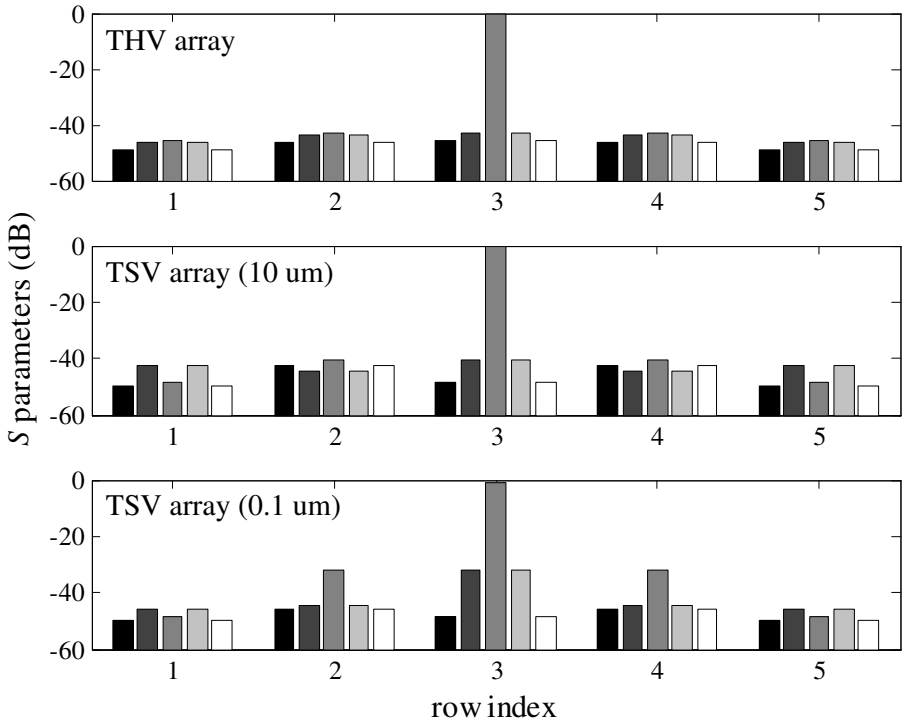
array in free space. In case of the TSV array with the oxide thickness of 0.1 μm, the maximum coupling level is about -29 dB. The coupling level can be worse when the silicon conductivity is higher, and the electrical design of TSV becomes challenging because of the increased coupling level as well as increased signal loss.

5.5 Summary

This chapter discussed a method to model TSV interconnection, which is a new silicon-based 3-D packaging structure that promises high density integration. After introducing typical structure and electrical operations, this chapter presented the use of cylindrical modal basis functions to model TSV structures. In addition, to capture the effect of annular oxide structure of TSV, this chapter proposed a new modal basis function called cylindrical PMBF. The proposed method, which is an extension of the modal equivalent modeling method in this dissertation, has the benefit that it can generate the model for a large number of TSV interconnections. The validation of the proposed approach showed good correlation with 3-D EM simulation and analytical methods. However, because of the limitation due to the use of the homogeneous media Green's function, the low-frequency accuracy of the proposed method needs to be improved in future work. Nevertheless, the modal equivalent circuit modeling is the first systematic approach that can be efficiently used for modeling TSV interconnections in practice.



(a) near-end S parameters



(b) far-end S parameters

Figure 79. S parameters at 10 GHz of the center conductor to observe near- and far-end couplings.

CHAPTER 6
CONCLUSIONS

For the realization of high-density mixed-signal systems, 3-D integration is becoming a fundamental design concept. Successful 3-D integration should be based on high-yield chip stacking process, reliable thermal management, and efficient electrical design. However, all the prerequisites for 3-D integration are challenging with current technologies, which therefore needs to be supported by systematic design methodologies.

Throughout the previous four chapters, this dissertation focused on developing an efficient CAD tool that enables the electrical characterization of interconnections in 3-D integration. Optimized to cylindrical interconnections such as bonding wire and through-via interconnections, the proposed method can extract parasitic elements and coupling of large number of interconnections in 3-D integration with minimum computational cost. Therefore, the new method demonstrates the modeling of bonding wires in stacked ICs and TSV interconnections efficiently.

In conclusion, the following section clarifies the major contributions in this dissertation, emphasizing the usefulness of the proposed method for electrical design of 3-D integrated systems. For further improvement of the modeling tool, Section 6.2 presents the current limitations of the developed method and suggests future work to address the limitations. The final section shows papers and inventions published through the dissertation research.

6.1 Contributions

The research objective of developing a method to obtain a broadband model of a large number of 3-D interconnections is achieved by the development of IPEX3D, a interconnection modeling tool focusing on 3-D design. By listing the main features of

IPEX3D, the details of the contributions in this research can be clarified as follows.

- **Efficient series impedance (R-L) extraction using cylindrical CMBF**: A main feature of IPEX3D is to extract frequency-dependent resistance and inductance of cylindrical-type interconnections. To capture the inductive coupling of large number of interconnections without causing much computational cost due to conductor discretization, this research proposed the cylindrical CMBF. The use of cylindrical CMBF to compute mutual inductances is further improved by controlling the required number of PE-mode basis functions. Therefore, the proposed method can obtain frequency-dependent resistances and inductances of a hundred of strongly coupled bonding wires in stacked ICs.

- **Parallel capacitance extraction using cylindrical AMBF**: The feature of capacitance extraction is included to extend modeling bandwidth since the capacitive coupling is important to ensure high-frequency accuracy. As a match with the cylindrical CMBF for impedance calculations, this research proposed the cylindrical AMBF, which can be utilized in a similar way for calculating integrals. In addition, this research revisited the integral equation to consider the case when the background material is a lossless (non-free-space) dielectric, and showed that the simple substitution of permittivity enables the capacitance calculation in the molding compound. Without breaking the efficiency of the $R-L$ calculation, the proposed method can obtain the broadband $RLGC$ model of large number of interconnections.

- **Inclusion of planar coupling by a combination with the PEEC method**: Although the proposed cylindrical modal basis functions (CMBF and AMBF) are suitable for modeling cylindrical structures such as bonding wires and via interconnections, real design environment is composed of cylindrical interconnections as well as various planar structures including strip-type interconnections,

bonding pads, and finite ground structures. To consider the coupling from planar structures, this research used the combined integral-equation-based model by adding staircase (piecewise constant) basis functions used in the conventional PEEC method.

- **TSV modeling using modal excess capacitance extraction**: To extend the method based on the modal basis functions for the TSV interconnection modeling, this research proposed to use the modal excess capacitance, which captures the capacitance in the annular oxide coating around the via conductor. By computing the additional capacitive coupling from the insulator surfaces, an equivalent model including the excess modal capacitance can be obtained. The modal equivalent model in this research is the first proposed method for modeling a large number of TSV interconnections in a systematic way, although further work is necessary to improve model accuracy.

6.1.1 Mixed-Signal System Design Using IPEX3D

Since IPEX3D provides the model of a large number of interconnections, we can utilize the generated model in the design flow of practical mixed-signal system. For a given interconnection structure, IPEX3D produces a generic multi-port equivalent circuit or network parameter, which does not depend on any specific excitation design. Thus, we can observe the effects of different excitation schemes using the multi-port network model and decide a specific signaling scheme that reduces parasitic effects. For example, the loss and coupling of transmitted signal are influenced by the location of power and ground wires, which can be in the middle or at the edge of a chip. If a large number of power, ground, and signal wires should be assigned, an additional CAD tool can be used to designate each wire port so that electrical performance is optimized.

6.2 Future Work

The current contributions of this dissertation can be improved in their applicability to practical 3-D interconnection designs by completing the following future work. The future work is specific to TSV interconnection and bonding wire applications.

6.2.1 Modeling of TSV Interconnections

The most important work to be done for more accurate TSV modeling is to consider the multilayered silicon substrate. Although the preliminary research in Chapter 5 shows fair model accuracy, the assumption of a homogeneous silicon background reduces the accuracy, especially when the silicon conductivity is high. The error comes from the DC leakage current flowing though the homogeneous conducting media, which should be modeled more accurately by using a multilayered Green's function [92]. Since the multilayered Green's function includes the information of oxide layers and free space region in the upper and lower parts of the silicon, the improved model will accurately incorporate the effect that DC leakage current can be blocked with the oxide and free space.

After improving the TSV modeling method with the multilayered Green's function, we can extend the modeling for further design applications. One of the interesting TSV applications is to utilize the effect of bias voltage to adjust the capacitance of TSV interconnections. Controlling the bias voltage changes the value of TSV capacitance, which can be used for control circuits in RF and digital applications like a varactor. By including the variable capacitance effect, the TSV modeling tool will be able to provide a design guideline for controlled TSV applications.

Finally, a future TSV modeling tool should address various shapes of TSV structures since the TSV technology is still evolving for improved process yield and better electrical performance. Some of the possible structures include coaxial TSV [85], annular type TSV, and square type TSV structures. To generalize the modeling approach proposed in Chapter 5, a new kind of basis function may be necessary.

6.2.2 Modeling of Bonding Wires in Stacked ICs

As discussed in this dissertation, the generated interconnection models are basically composed of RLC elements. Nevertheless, the direct use of the RLC model in SPICE-type simulators is not available in the current status because the model is the combination of frequency-dependent R-Ls and frequency-independent Cs, which might violate causality. Therefore, for the time-domain co-simulation with other subsystems, the series R-Ls should be converted to an equivalent network of fixed-valued components like a ladder circuit.

Further improvements in computing the effect of planar coupling is also necessary. The combination with the PEEC method (Chapter 4) can capture the planar coupling, but computing integrations involving the modal basis functions and the discretized cells from the planar structure may require increased computational cost. Therefore, the efficiency enhancement of computing the coupling between planer and modal basis functions is required. For another solution, a more efficient method of combining planar coupling can be sought. For example, the plane modeling methods such as MFDM [93] and MFEM [94] can be linked to the integral-equation based method, and the generalized modal decomposition can be developed.

To extend the modeling bandwidth of the current modeling method up to the millimeter wave range, more generalized modeling is necessary. A main issue with bonding wires at millimeter wave frequencies is the radiation effect, which means that wires act like antennas. The integral equation should be reformulated as in the case of the generalized full-wave PEEC method. The radiation effect may be incorporated as additional radiation resistance in the interconnection model.

6.3 Publications

In the course of the dissertation research, the following journal articles, conference papers, and invention disclosures have been published.

6.3.1 Refereed Journal Articles

• **K. J. Han**, H. Takeuchi, M. Swaminathan, "Eye-Pattern Design for High-Speed Differential Links using Extended Passive Equalization," *IEEE Trans. Advanced Packaging*, Vol. 31, No. 2, pp. 246-257, May 2008.

• **K. J. Han**, M. Swaminathan, "Inductance and Resistance Calculations in Three-Dimensional Packaging Using Cylindrical Conduction Mode Basis Functions," to be published in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol. 28, No. 6, Jun. 2009.

• **K. J. Han**, M. Swaminathan, "Modal Element Equivalent Circuit (MEEC) Method for Modeling of Interconnection Parasitics in 3-D Integration," to be submitted to *IEEE Trans. Electromagnetic Compatibility.*

• **K. J. Han**, M. Swaminathan, "Wide-Band Modeling of Through-Silicon Via Interconnections," to be submitted to *IEEE Trans. Advanced Packaging.*

6.3.2 Conference Papers

• **K. J. Han**, H. Takeuchi, E. Engin, M. Swaminathan, "Eye-Pattern Improvement for Design of High-Speed Differential Links," Proc. Topical Meeting on Electrical Performance of Electronic Packaging (EPEP '06), pp. 241 - 244, Scottdale, USA, Oct. 2006.

• **K. J. Han**, E. Engin, M. Swaminathan, "Cylindrical Conduction Mode Basis Functions for Modeling of Inductive Couplings in System-in-Package (SiP)," Proc. Topical Meeting on Electrical Performance of Electronic Packaging (EPEP '07), pp. 361 - 364, Atlanta, USA, Oct. 2007.

• **K. J. Han**, M. Swaminathan, E. Engin, "Analysis of Horizontal and Vertical Couplings in Bonding Wire Interconnections Using EFIE with Cylindrical Conduction Mode Basis Functions," Proc. 12th Workshop on Signal Propagation on Interconnects (SPI '08), May 2008.

• **K. J. Han**, M. Swaminathan, E. Engin, "Electrical Modeling of Wirebonds in

Stacked ICs Using Cylindrical Conduction Mode Basis Functions," Proc. Electronic Components and Technology Conference (ECTC '08), pp. 1225-1230, Orlando, May 2008.

• **K. J. Han**, M. Swaminathan, E. Engin, "Electric Field Integral Equation Combined with Cylindrical Conduction Mode Basis Functions for Electrical Modeling of Three-dimensional Interconnects," Proc. 45th Design Automation Conference (DAC '08), pp. 421-424, Anaheim, Jun. 2008.

• **K. J. Han**, M. Swaminathan, E. Engin, "Wideband Electrical Modeling of Large Three-Dimensional Interconnects using Accelerated Generation of Partial Impedances with Cylindrical Conduction Mode Basis Functions," International Microwave Symposium (IMS '08) Digest, pp. 1297-1300, Atlanta, Jun. 2008.

• **K. J. Han**, M. Swaminathan, "Parasitic Extraction of Interconnections in 3-D Packaging Using Mixed Potential Integral Equation with Global Basis Functions," Proc. Asia-Pacific Microwave Conference (APMC '08), pp. F2-08, Hong Kong, China, Dec. 2008.

• **K. J. Han** , M. Swaminathan, "Polarization Mode Basis Functions for Modeling Insulator-Coated Through-Silicon Via (TSV) Interconnections," to be presented in 13th Workshop on Signal Propagation on Interconnect (SPI '09), May 2009.

6.3.3 Invention Disclosure

• **K. J. Han** , M. Swaminathan, "Efficient Electrical Modeling of Coupling in System-in-Package," Invention Disclosure ID: 4255, Oct. 2007, Provisional Patent Application filed by Georgia Tech.

APPENDIX A

DERIVATION OF PARTIAL RESISTANCE FORMULA

Partial resistances formula (26) can be calculated directly from the following definition of partial resistances.

$$R_{imd,jnq} = \frac{1}{\sigma}\int_{V_i} \vec{w}^*_{imd}(\vec{r},\omega)\cdot\vec{w}_{jnq}(\vec{r},\omega)dV_i. \tag{109}$$

When $i \neq j$, the inner product of $\vec{w}_{imd}$ and $\vec{w}_{jnq}$ is zero since the cylindrical CMBFs are localized to the conductors i and j. Thus, $R_{imd,jnq}$ becomes zero when $i \neq j$.

When $i = j$, the inner product can be written as follows.

$$\begin{aligned}\vec{w}^*_{imd}(\vec{r},\omega)\cdot\vec{w}_{inq}(\vec{r},\omega) =& \frac{\hat{z}_i\cdot\hat{z}_i}{A^*_{im}A_{in}} J_m(\alpha^*(\vec{r}-\vec{r}_i)\cdot\hat{\rho}_i)J_n(\alpha(\vec{r}-\vec{r}_i)\cdot\hat{\rho}_i) \\ & \cos(m\varphi_i-\varphi_d)\cos(n\varphi_i-\varphi_q),\end{aligned} \tag{110}$$

where $\varphi_{d,q}$ can be zero (PE-d mode) or $\pi/2$ (PE-q mode). Since the inner product involves a single conductor i, global vectors in Bessel functions are simplified to local variables ρ and φ. By the same reason, the inner product of unit axial vectors becomes unity. Therefore,

$$\vec{w}^*_{imd}(\vec{r},\omega)\cdot\vec{w}_{inq}(\vec{r},\omega) = \frac{1}{A^*_{im}A_{in}} J_m(\alpha^*\rho)J_n(\alpha\rho)\cos(m\varphi_i-\varphi_d)\cos(n\varphi_i-\varphi_q). \tag{111}$$

Plugging (111) into (109) results in

$$R_{imd,jnq} = \frac{l_i}{\sigma A^*_{im}A_{in}}\left(\int_0^{2\pi}\cos(m\varphi_i-\varphi_d)\cos(n\varphi_i-\varphi_q)d\varphi\right)\left(\int_0^{\rho_i}\rho J_m(\alpha^*\rho)J_n(\alpha\rho)d\rho\right). \tag{112}$$

The above formula shows that we can integrate for variables ρ and φ separately. Firstly, the integration over φ is reduced as follows because of the orthogonal property

of harmonic functions.

$$\int_0^{2\pi} \cos(m\varphi_i - \varphi_d)\cos(n\varphi_i - \varphi_q)d\varphi = \begin{cases} 2\pi & m = n = 0(\text{SE mode}) \\ \pi & m = n \neq 0, d = q \\ 0 & m = n \neq 0, d \neq q \\ 0 & m \neq n \end{cases} \tag{113}$$

(113) indicates that mutual resistances between different modes are all zeros, and we only need to calculate integral over ρ when $m = n$ and $d = q$. For SE ($m = 0$) and PE modes ($m \neq 0$), the integral over ρ is as follows.

$$\int_0^{\rho_i} \rho J_m(\alpha^*\rho)J_m(\alpha\rho)d\rho = \begin{cases} \frac{2j\rho_i}{-\alpha^2+\alpha^{*2}}\Im[\alpha^* J_0(\alpha\rho_i)J_1(\alpha^*\rho_i)] & m = 0(\text{SE mode}) \\ \frac{2j\rho_i}{-\alpha^2+\alpha^{*2}}\Im[\alpha J_{n-1}(\alpha\rho_i)J_n(\alpha^*\rho_i)] & m \neq 0(\text{PE mode}) \end{cases} \tag{114}$$

By substituting $\alpha^2 = -2j/\delta^2$ in (114) and combining (113) and (114) in (112), we can obtain the following expression of partial resistance.

$$R_{imd,jnq} = \begin{cases} \frac{\pi\delta^2\rho_i l_i}{\sigma|A_{i0}|^2}\Im(\alpha J_0^*(\alpha\rho_i)J_1(\alpha\rho_i)) & i = j, m = n = 0 \\ \frac{\pi\delta^2\rho_i l_i}{2\sigma|A_{im}|^2}\Im(\alpha^* J_{m-1}^*(\alpha\rho_i)J_m(\alpha\rho_i)) & i = j, m = n \neq 0, d = q \\ 0 & \text{otherwise} \end{cases} . \tag{115}$$

APPENDIX B

DERIVATION OF INTEGRANDS IN PARTIAL SELF INDUCTANCE FORMULA

As in the case of partial resistance in Appendix A, global coordinate expression of partial inductance can be reduced to the following local coordinate expression when self inductance ($i = j$) is considered.

$$\begin{aligned} L_{imd,inq} &= \frac{\mu}{4\pi}\int_{V_i'}\int_{V_i} \vec{w}^*_{imd}(\vec{r},\omega)\cdot\vec{w}_{inq}(\vec{r'},\omega)\frac{1}{|\vec{r}-\vec{r'}|}dV_i dV_i^{'} \\ &= \frac{\mu}{4\pi A^*_{im}A_{in}}\int_{V_i'}\int_{V_i} J_m(\alpha^*\rho)J_n(\alpha\rho')\cos(m\varphi-\varphi_d)\cos(n\varphi'-\varphi_q)\frac{1}{|\vec{r}-\vec{r'}|}dV_i dV_i^{'}, \end{aligned} \tag{116}$$

where

$$|\vec{r}-\vec{r'}| = \sqrt{D_i^2(\rho,\rho',\varphi,\varphi') + (z-z')^2}$$

and

$$D_i^2(\rho,\rho',\varphi,\varphi') = \rho^2 + \rho^{'2} - 2\rho\rho'\cos(\varphi-\varphi')$$

is the distance between two points on the cross sectional plane, as shown in Figure 80.

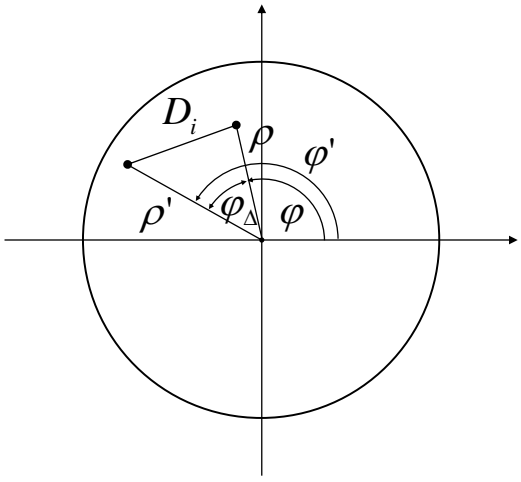


Figure 80. Local coordinate variables in the cross section of a cylinder.

Since the axial variables (z and z') are found in $1/|\vec{r}-\vec{r'}|$ only, an indefinite integral over (z, z') can be found as follows.

$$\begin{aligned} I_z(D_i, l_i) &= \int_{-l_i/2}^{+l_i/2} \int_{-l_i/2}^{+l_i/2} \frac{1}{|\vec{r}-\vec{r'}|} dz dz' \\ &= \int_{-l_i/2}^{+l_i/2} \int_{-l_i/2}^{+l_i/2} \frac{1}{\sqrt{D_i^2+(z-z')^2}} dz dz' \\ &= 2(\sqrt{D_i^2} - \sqrt{l_i^2+D_i^2}) + l_i \log\left[\frac{l_i^2+\sqrt{l_i^2+D_i^2}}{-l_i^2+\sqrt{l_i^2+D_i^2}}\right]. \end{aligned} \tag{117}$$

By inserting the above formula, (116) is reduced to the integration involving radial and angular variables.

$$\begin{aligned} L_{imd,inq} =& \frac{\mu}{4\pi A_{im}^* A_{in}} \int_{\rho'} \int_{\rho} \rho\rho' J_m(\alpha^*\rho) J_n(\alpha\rho') \\ & \times \int_{\varphi'} \int_{\varphi} \cos(m\varphi' - \varphi_d) \cos(n\varphi - \varphi_q) I_z(D_i, l_i) d\varphi d\varphi' d\rho d\rho'. \end{aligned} \tag{118}$$

In (118), the sum of two angular variables ($\varphi+\varphi'$) is involved with harmonic functions only, so analytical integral over $(\varphi + \varphi')$ is possible. Thus, we apply the following coordinate transform.

$$\begin{pmatrix} \varphi_\Delta \\ \varphi_\Sigma \end{pmatrix} = \begin{pmatrix} 1 & -1 \\ 1 & 1 \end{pmatrix} \begin{pmatrix} \varphi \\ \varphi' \end{pmatrix}. \tag{119}$$

When defining the integration region for (φ, φ') as $[-\pi+\pi, -\pi+\pi]$ as shown in Figure 81, the integration of any function $f(\varphi, \varphi')$ is rewritten as follows.

$$\begin{aligned} \int_{-\pi}^{+\pi} \int_{-\pi}^{+\pi} f(\varphi, \varphi') d\varphi d\varphi' =& \int_{0}^{+2\pi} \int_{-2\pi+\varphi_\Delta}^{+2\pi-\varphi_\Delta} f(\varphi(\varphi_\Delta, \varphi_\Sigma), \varphi'(\varphi_\Delta, \varphi_\Sigma)) \frac{1}{2} d\varphi_\Sigma d\varphi_\Delta \\ &+ \int_{-2\pi}^{0} \int_{-2\pi-\varphi_\Delta}^{+2\pi+\varphi_\Delta} f(\varphi(\varphi_\Delta, \varphi_\Sigma), \varphi'(\varphi_\Delta, \varphi_\Sigma)) \frac{1}{2} d\varphi_\Sigma d\varphi_\Delta \\ =& \frac{1}{2} \int_{0}^{+2\pi} \int_{-2\pi+\varphi_\Delta}^{+2\pi-\varphi_\Delta} f(\varphi(\varphi_\Delta, \varphi_\Sigma), \varphi'(\varphi_\Delta, \varphi_\Sigma)) \\ &+ f(\varphi(-\varphi_\Delta, \varphi_\Sigma), \varphi'(-\varphi_\Delta, \varphi_\Sigma)) d\varphi_\Sigma d\varphi_\Delta. \end{aligned} \tag{120}$$

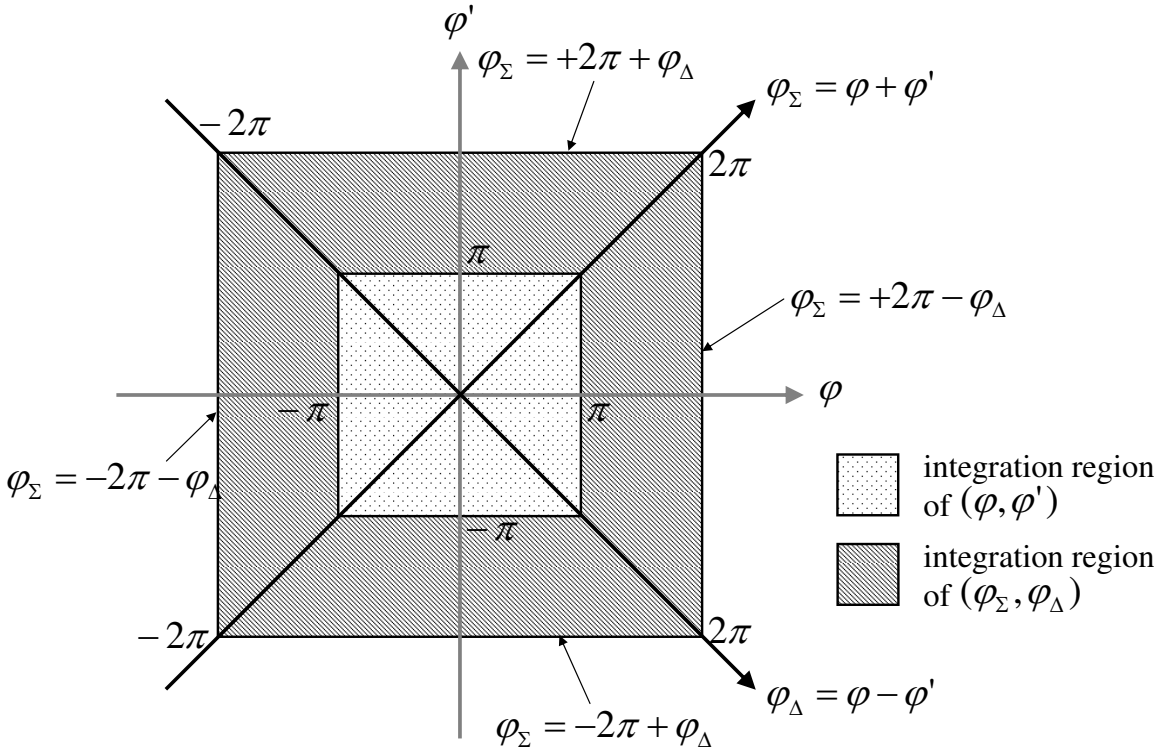


Figure 81. Coordinate transform of angular variables and integration region.

By substituting $f(\varphi(\varphi_\Delta,\varphi_\Sigma),\varphi'(\varphi_\Delta,\varphi_\Sigma)) = \cos(m(\varphi_\Delta+\varphi_\Sigma)/2-\varphi_d)\cos(n(-\varphi_\Delta+\varphi_\Sigma)/2-\varphi_q)$ in (118), we can obtain the integral over φ_Σ that can be calculated analytically.

$$
\begin{aligned}
I_{\varphi_\Sigma}(\varphi_\Delta) = &\int_{-2\pi+\varphi_\Delta}^{+2\pi-\varphi_\Delta} \cos(m(\varphi_\Delta+\varphi_\Sigma)/2-\varphi_d)\cos(n(-\varphi_\Delta+\varphi_\Sigma)/2-\varphi_q) \\
&+ \cos(m(-\varphi_\Delta+\varphi_\Sigma)/2-\varphi_d)\cos(n(\varphi_\Delta+\varphi_\Sigma)/2-\varphi_q)d\varphi_\Sigma \\
= &\begin{cases}
8\pi - 4\varphi_\Delta & m=n=0 \\
2(2\pi-\varphi_\Delta)\cos(n\varphi_\Delta) - \frac{2}{n}\sin(n\varphi_\Delta)\cos(2\varphi_d) & m=n\neq 0, d=q \\
\frac{4(-1)^{m+n+1}}{m^2-n^2}[m\sin(m\varphi_\Delta) - n\sin(n\varphi_\Delta)] & m\neq n, d=q(\text{PE-}d) \\
\frac{4(-1)^{m+n+1}}{m^2-n^2}[n\sin(m\varphi_\Delta) - m\sin(n\varphi_\Delta)] & m\neq n, d=q(\text{PE-}q) \\
0 & \text{otherwise}
\end{cases}
\end{aligned}
\tag{121}
$$

By inserting I_{φ_Σ} into (118), the triple integral (27) can be obtained.

APPENDIX C

INDEFINITE INTEGRAL FOR AXIAL VARIABLES IN MUTUAL INDUCTANCE FORMULA

With the variables that are defined in Figure 15, the distance between two points is formulated as follows.

$$R_{12} = |\vec{R_2} - \vec{R_1}| = \sqrt{z_1^2 + 2bz_1z_2 + z_2^2 + 2dz_1 + 2fz_2 + g}, \tag{122}$$

where

$$b = -\sin\beta_1 \sin\beta_2 \cos(\alpha_2 - \alpha_1) - \cos\beta_1 \cos\beta_2,$$

$$\begin{aligned} d = {} & \rho_{2x}[\sin\beta_1 \sin(\alpha_2 - \alpha_1)] + \rho_{2y}[\sin\beta_1 \cos\beta_2 \cos(\alpha_2 - \alpha_1) - \sin\beta_2 \cos\beta_1] \\ & - D_x \sin\beta_1 \sin\alpha_1 + D_y \cos\alpha_1 \sin\beta_1 - D_z \cos\beta_1, \end{aligned}$$

$$\begin{aligned} f = {} & \rho_{1x}[-\sin\beta_2 \sin(\alpha_2 - \alpha_1)] + \rho_{1y}[\cos\beta_1 \sin\beta_2 \cos(\alpha_2 - \alpha_1) - \sin\beta_1 \cos\beta_2] \\ & + D_x \sin\beta_2 \sin\alpha_2 - D_y \cos\alpha_2 \sin\beta_2 + D_z \cos\beta_2, \end{aligned}$$

$$\begin{aligned} g = {} & D_{21}^2 + \rho_1^2 + \rho_2^2 + 2[-\rho_{1x}\rho_{2x} \cos(\alpha_2 - \alpha_1) \\ & - \rho_{1y}\rho_{2y}(\cos\beta_1 \cos\beta_2 \cos(\alpha_2 - \alpha_1) + \sin\beta_1 \sin\beta_2) - \rho_{1y}\rho_{2x} \cos\beta_1 \sin(\alpha_2 - \alpha_1) \\ & + \rho_{1x}\rho_{2y} \cos\beta_2 \sin(\alpha_2 - \alpha_1)] + 2\rho_{1x}[-D_x \cos\alpha_1 - D_y \sin\alpha_1] \\ & + 2\rho_{1y}[D_x \cos\beta_1 \sin\alpha_1 - D_y \cos\alpha_1 \cos\beta_1 - D_z \sin\beta_1] \\ & + 2\rho_{2x}[D_x \cos\alpha_2 + D_y \sin\alpha_2] \\ & + 2\rho_{2y}[-D_x \cos\beta_2 \sin\alpha_2 + D_y \cos\alpha_2 \cos\beta_2 + D_z \sin\beta_2] \end{aligned}$$

,

$\rho_{nx} = \rho_n \cos\varphi_n$, $\rho_{nx} = \rho_n \sin\varphi_n$, and α_n, β_n are the rotation angles of conductors based on Euler angles ($n = 1, 2$).

Plugging (127) into the integral over (z_i, z_j) in (29) and finding indefinite integral result in following formula.

$$I_z(\rho_i, \rho_j, \varphi_i, \varphi_j) = \int_{z_i, z_j} \frac{1}{R_{i,j}} dz_i dz_j = I_{z1} - I_{z2}, \tag{123}$$

where

$$I_{z1} = I(B_1, C_1, D_1, -bL_2/2 + d + L_1/2, +bL_2/2 + d + L_1/2),$$

$$I_{z2} = I(B_2, C_2, D_2, -bL_2/2 + d - L_1/2, +bL_2/2 + d - L_1/2),$$

$$I(B, C, D, x^-, x^+) = \frac{1}{b}\int_{x^-}^{x^+} \log[x + C\sqrt{(x-B)^2 + D^2}]dx,$$

$$B_1 = +(1-b^2)\frac{L_1}{2} - bf + d,$$

$$B_2 = -(1-b^2)\frac{L_1}{2} - bf + d,$$

$$C_1 = C_2 = |\frac{1}{b}| = |\sec\theta_0|,$$

$$D_1^2 = b^2\{\frac{1-b^2}{4}L_1^2 + (d-bf)L_1 + g - f^2\},$$

and

$$D_2^2 = b^2\{\frac{1-b^2}{4}L_1^2 - (d-bf)L_1 + g - f^2\}.$$

Detailed analytic expressions of $I(B, C, D, x^-, x^+)$ depend on the specific values of B, C, and D.

APPENDIX D

PARTIAL ELEMENT FORMULA OF BRICK-TYPE CONDUCTORS

D.1 Partial Self Inductance

The partial self inductance of a brick element can be found from the following formula [79].

$$\begin{aligned}\frac{Lp_{ii}}{l} = \frac{2\pi}{\pi}\Big\{ & \frac{\omega^2}{24u}\big[\ln\big(\frac{1+A_2}{\omega}\big) - A_5\big] + \frac{1}{24u\omega}[\ln(\omega + A_2) - A_6] \\ & + \frac{\omega^2}{60u}(A_4 - A_3) + \frac{\omega^2}{24}\big[\ln\frac{u+A_3}{\omega} - A_7\big] + \frac{\omega^2}{60u}(\omega - A_2) \\ & + \frac{1}{20u}(A_2 - A_4) + \frac{u}{4}A_5 - \frac{u^2}{6\omega}\tan^{-1}\big(\frac{\omega}{uA_4}\big) + \frac{u}{4\omega}A_6 - \frac{\omega}{6}\tan^{-1}\big(\frac{u}{\omega A_4}\big) \\ & + \frac{A_7}{4} - \frac{1}{6\omega}\tan^{-1}\big(\frac{u\omega}{A_4}\big) + \frac{1}{24\omega^2}[\ln(u + A_1) - A_7] + \frac{u}{20\omega^2}(A_1 - A_4) \\ & + \frac{1}{60\omega^2 u}(1 - A_2) + \frac{1}{60u\omega^2}(A_4 - A_1) + \frac{u}{20}(A_3 - A_4) \\ & + \frac{u^3}{24\omega^2}\big[\ln\big(\frac{1+A_1}{u}\big) - A_5\big] + \frac{u^3}{24\omega}\big[\ln\big(\frac{\omega + A_3}{u}\big) - A_6\big] \\ & + \frac{u^3}{60\omega^2}[(A_4 - A_1) + (u - A_3)]\Big\}\end{aligned} \quad , \quad (124)$$

where $A_1 = (1+u^2)^{\frac{1}{2}}$, $A_2 = (1+\omega^2)^{\frac{1}{2}}$, $A_3 = (\omega^2+u^2)^{\frac{1}{2}}$, $A_4 = (1+\omega^2+u^2)^{\frac{1}{2}}$, $A_5 = \ln\big(\frac{1+A_4}{A_3}\big)$, $A_6 = \ln\big(\frac{\omega+A_4}{A_1}\big)$, $A_7 = \ln\big(\frac{u+A_4}{A_2}\big)$, $u = \frac{l}{W}$, $\omega = \frac{T}{W}$, and l, T, and W are the length, the thickness, and the width of a rectangular conductor segment, respectively. If the thickness T is negligible, a simple self inductance formula can be used instead [79].

D.2 Partial Mutual Inductance between Parallel Conductors

When two rectangular conductors are in parallel, the partial mutual inductance between the two conductors can be found by using the following weighted sum of the self inductances of 64 virtual conductor segments, as shown in the following formula

[8].

$$M = \frac{1}{W_0 T_0 W_1 T_1} \frac{1}{8} \sum_{i_0,i_1,j_0,j_1,k_0,k_1=0}^{1} (-1)^{i_0+i_1+j_0+j_1+k_0+k_1+1} \times A^2_{p_{i_0,j_0,k_0},q_{i_1,j_1,k_1}} L_{p_{i_0,j_0,k_0},q_{i_1,j_1,k_1}}, \tag{125}$$

where $L_{p_{i_0,j_0,k_0},q_{i_1,j_1,k_1}}$ represents the self inductance of a brick element that has the two diagonal end points p_{i_0,j_0,k_0} and q_{i_1,j_1,k_1}. All the point indices are shown in Figure 82. The partial self inductance formula can be found in the previous section of this appendix.

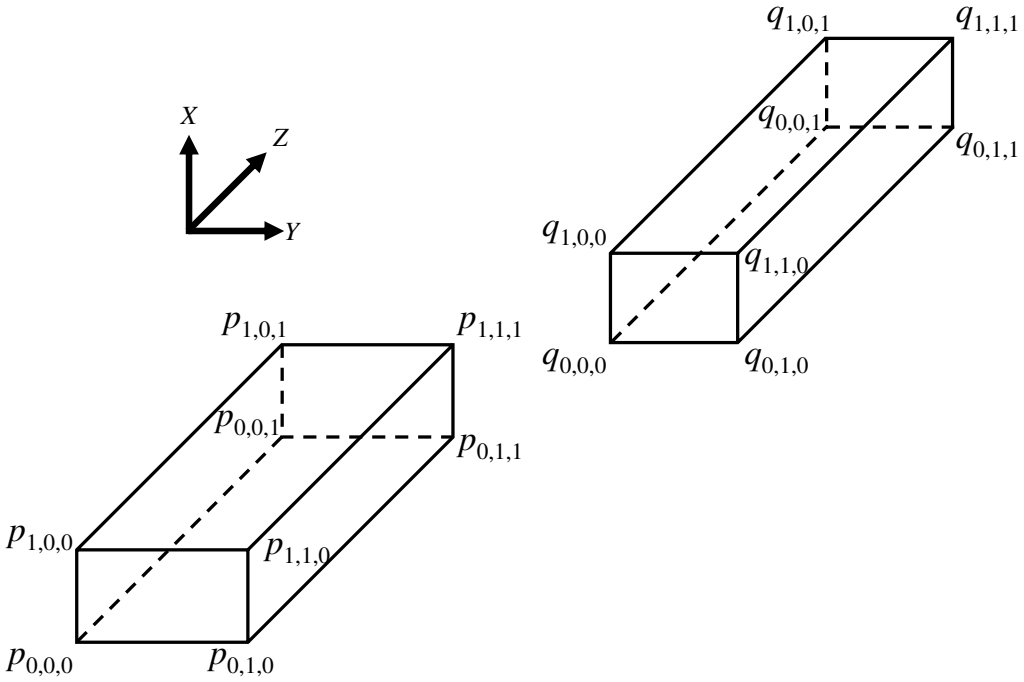


Figure 82. Two parallel brick elements and their point indices to calculate partial mutual inductance [8].

D.3 Partial Coefficient of Potential between Parallel Conductors

For computing the capacitive coupling between two parallel capacitive cells, the following formula can be used [9].

$$4\pi\epsilon Pp_{i,j} = \frac{1}{f_a f_b s_a s_b}\sum_{k=1}^{4}\sum_{m=1}^{4}(-1)^{k+m}\Big[\frac{b_m^2-C^2}{2}a_k\ln(a_k+\rho) + \frac{a_k^2-C^2}{2}b_m\ln(b_m+\rho) - \frac{1}{6}(b_m^2-2C+a_k^2)\rho - b_m C a_k\tan^{-1}\frac{a_k b_m}{\rho C}\Big] \quad , \tag{126}$$

where $\rho=\sqrt{a_k^2+b_m^2+C^2}$, $\{a,b\}_1=\{a,b\}_{ij}-\frac{f_{\{a,b\}}}{2}-\frac{s_{\{a,b\}}}{2}$, $\{a,b\}_2=\{a,b\}_{ij}+\frac{f_{\{a,b\}}}{2}-\frac{s_{\{a,b\}}}{2}$, $\{a,b\}_3=\{a,b\}_{ij}+\frac{f_{\{a,b\}}}{2}+\frac{s_{\{a,b\}}}{2}$, $\{a,b\}_4=\{a,b\}_{ij}-\frac{f_{\{a,b\}}}{2}+\frac{s_{\{a,b\}}}{2}$, $\{a,b\}_{ij}$s are the relative distances between cells in a and b directions, C is the relative vertical distance between cells, and $\{f,s\}_{\{a,b\}}$s are the sizes of cells shown in Figure 83.

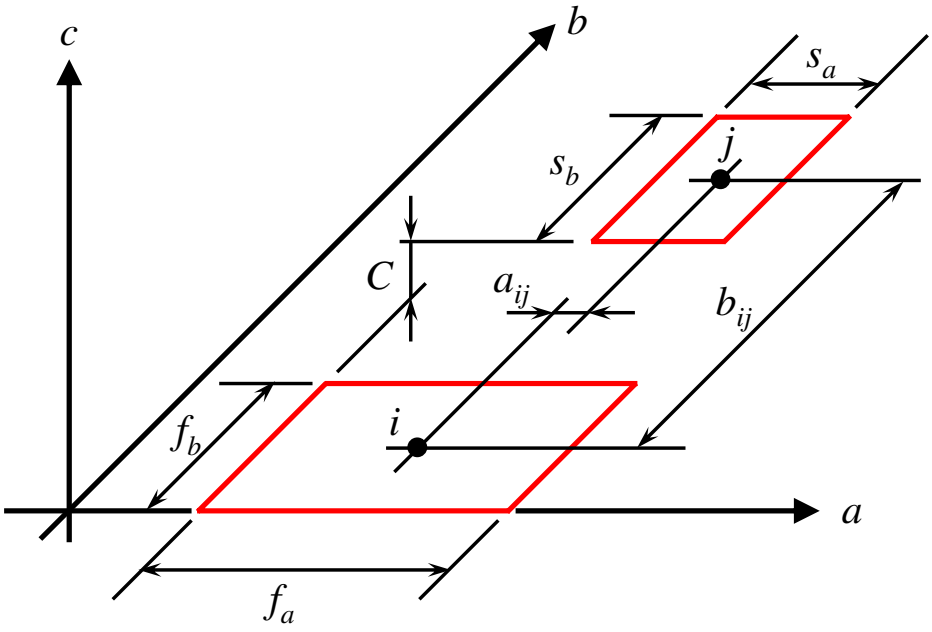


Figure 83. Two parallel panel cell elements and their coordinate variables to calculate partial mutual coefficient of potential [9].

APPENDIX E

INDEFINITE INTEGRAL FOR AXIAL VARIABLES IN MUTUAL INDUCTANCE BETWEEN A CYLINDER AND A PLANE

With the variables that are defined in Figure 44, the distance between two points is formulated as follows.

$$R_{12} = |\vec{R_2} - \vec{R_1}| = \sqrt{z_2^2 + 2fz_2 + g}, \tag{127}$$

where

$$f = [(D_x - x_1)\sin\alpha - (D_y - y_1)\cos\alpha]\sin\beta + (D_z - z_1)\cos\beta,$$

$$\begin{aligned} g = {} & D_{21}^2 + \rho^2 + x_1^2 + x_1^2 + x_1^2 \\ & + 2\rho[-\cos\varphi(x_1\cos\alpha + y_1\sin\alpha) + \sin\varphi(x_1\sin\alpha - y_1\cos\alpha)\cos\beta - \sin\varphi z_1\sin\beta \\ & + (D_x\cos\alpha + D_y\sin\alpha)\cos\varphi + D_z\sin\beta sin\varphi + (-D_x\sin\alpha + D_y\cos\alpha)\sin\varphi\cos\beta] \\ & - 2x_1D_z - 2y_1D_y - 2z_1D_z, \end{aligned}$$

$\rho_{nx} = \rho_n\cos\varphi_n$, $\rho_{nx} = \rho_n\sin\varphi_n$, and α, β are the rotation angles of conductors based on Euler angles $(n = 1, 2)$.

By using (127) in the integral over (z_2), the following indefinite integral can be found.

$$I_z(\rho_2, \varphi_2, x_1, y_1) = \int_{-\frac{L_2}{2}}^{+\frac{L_2}{2}} \frac{1}{R_{12}} dz_2 = -\sinh^{-1}\frac{f - 0.5L_2}{\sqrt{-f^2 + g}} + \sinh^{-1}\frac{f + 0.5L_2}{\sqrt{-f^2 + g}}. \tag{128}$$

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