DESIGN, MODELING, AND CHARACTERIZATION OF EMBEDDED PASSIVES AND INTERCONNECTS IN INHOMOGENEOUS LIQUID CRYSTALLINE POLYMER (LCP) SUBSTRATES

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DESIGN, MODELING, AND CHARACTERIZATION OF EMBEDDED PASSIVES AND INTERCONNECTS IN INHOMOGENEOUS LIQUID CRYSTALLINE POLYMER (LCP) SUBSTRATES

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

The goal of the research in this dissertation is to design and characterize embedded passive components, interconnects, and circuits in inhomogeneous, multi-layer liquid crystalline polymer (LCP) substrates.

The attenuation properties of inhomogeneous multi-layer LCP substrates were extracted up to 40 GHz. This is the first result for an inhomogeneous LCP stack-up that has been reported. The characterization results show excellent loss characteristics, much better than FR-4-based technology, and they are similar to LTCC and homogeneous LCP-based technology.

A two-port characterization method based on measurements of multiple arrays of vias is proposed. The method overcomes the drawbacks of the one-port and other two-port characterizations. Model-to-hardware correlation was verified using multi-layer model in Agilent ADS and measurement-based via model using arrays of the vias. The resulting correlations show that this method can be readily applied to other vertical interconnect structures besides via structures.

Comprehensive characterizations have been conducted for the efficient 3D integration of high-Q passives using a balanced LCP substrate. At two different locations from three different large M-LCP panels, 76 inductors and 16 3D capacitors were designed and measured. The parameters for the measurement-based inductor model were extracted from the measured results. The results validate the large panel process of the M-LCP substrate. To reduce the lateral size, multi-layer 3D capacitors were designed. The designed 3D capacitors with inductors can provide optimized solutions for more

efficient RF front-end module integration. In addition, the parameters for the measurement-based capacitor model were extracted.

Various RF front-end modules have been designed and implemented using high-Q embedded passive components in inhomogeneous multi-layer LCP substrates. A C-band filter using lumped elements has been designed and measured. The lumped baluns were used to design a double balnced-mixer for 5 GHz WLAN application and a doubly double-balanced mixer for 1.78 GHz CDMA receiver miniaturization. Finally, to overcome the limitations of the lumped component circuits, a 30 GHz gap-coupled band-pass filter in inhomogeneous multi-layer LCP substrates, and the measured results using SOLT and TRL calibrations have been compared to the simulation results.

CHAPTER 1

INTRODUCTION

The goal of the research in this dissertation is to design and characterize embedded passive components, interconnects, and circuits in inhomogeneous, multi-layer liquid crystalline polymer (LCP) substrates. To achieve this goal, three main tasks are performed: (1) the characterization of inhomogeneous multi-layer LCP stack-ups; (2) the development of measurement-based via characterization using periodic arrays of vias; and (3) the design and characterization of high-quality factor (Q) embedded passive components in inhomogeneous multi-layer LCP substrates for system-on-package (SOP) technology. In addition, to validate inhomogeneous, multi-layer LCP substrates as a promising SOP solution for RF and microwave applications, lumped and distributed RF circuits based on embedded passive components were designed, fabricated, and measured.

The trend in wireless systems is toward multi-functionality and higher miniaturization at higher speeds and lower cost. System-on-chip (SOC), system-in-package (SIP), and multiple-chip-module (MCM) are the system platforms that are currently being widely pursued by industry to accommodate such challenging tasks. Even though complementary metal–oxide–semiconductor (CMOS) technology can be the most cost-effective solution for certain digital and RF applications, it is not an optimal technology for entire RF and digital applications. As the number of components in a multi-band system has increased exponentially, as shown in Figure 1.1, new system integration platforms such as SOC and SOP are critical.

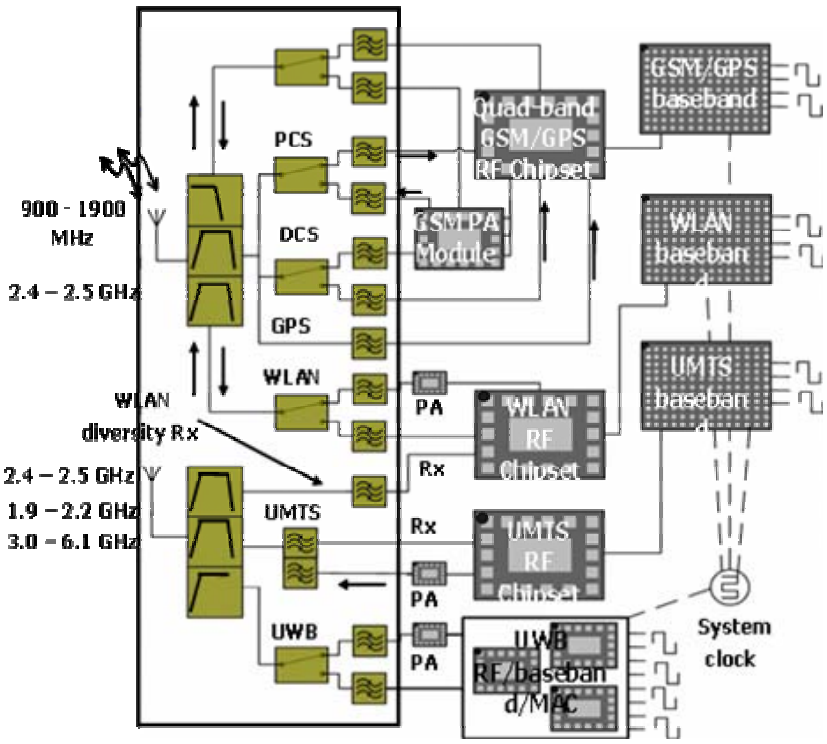


Figure 1.1. Multi-band system architecture

SIP and SOP have been known as attractive system platforms for wireless communication systems because they can provide benefits such as cost reduction, fast time to market, compact size, low profile, and high performance. SIP and SOP provide functionality in a package through the integration of passive components such as inductors [1], 0 capacitors, and resistors. Therefore, highly-integrated SIP and SOP can provide a multi-band system solution with a compact size and high performance.

To support new system architectures, new high-performance and high-frequency packaging materials also have been intensely researched. The first method for determining the feasibility of these packaging materials is to examine their performance. . An electrical characterization using various methods has been performed along with mechanical and thermal characterizations. For the microwave frequency range, extremely

accurate calibration, de-embedding, measurement, and modeling methods are required to properly characterize new materials. Component and circuit realizations using new materials are another way to show their feasibility as high-frequency materials while minimizing size and cost and maximizing performance.

Section 1.1 addresses the advantages and disadvantages of SOP as a new mixed-signal system platform, and Section 1.2 presents the characterization of high-frequency materials. Section 1.3 reviews the characterization of vias, and Section 1.4 examines embedded passive technology. Section 1.5 presents embedded passive-based circuits up to the microwave frequency range, and finally, Section 1.6 provides the goal of this dissertation.

1.1. System on Package

SOC is an approach to incorporate every component using silicon technology. SOC can achieve very high density components, leading to size reduction. However, SOC has certain limitations, such as low-Q passive, substrate coupling, and testing. Using SOC alone, it is difficult to realize filters, duplexers, power amplifiers, and antennas. In addition, the nano-scale integration trend increases wiring resistance, leading to delay, causing increased latency in digital circuits.

SOP combines the best of on-chip integration with the best of package integration for convergent and microminiaturized mobile systems. The SOP concept overcomes a number of the engineering limits of SOC. To reduce the delay latency in SOC technology, SOP can provide global wiring on the package. The wireless integration limits of SOC are also handled effectively through SOP. Figure 2 shows the state-of-the-

art mixed-signal SOP technology. RF components such as capacitors, filters, antennas, switches, and high-frequency and high-Q inductors are best fabricated in the package rather than on silicon. The highest Q factors of inductors reported on silicon are about 10-25, in contrast to 100-400 achieved in the SOP package. SOP has proven that it is an effective system with low cost, high performance, and small form factor [3], [4], [5], [6], [7], [8], and [9]. As shown in Figure 1.2, the high-Q embedded passive serves not only as RF components, including filters, baluns, and antennas, but also as low parasitic and low insertion loss interconnects using high-Q passives in the substrate.

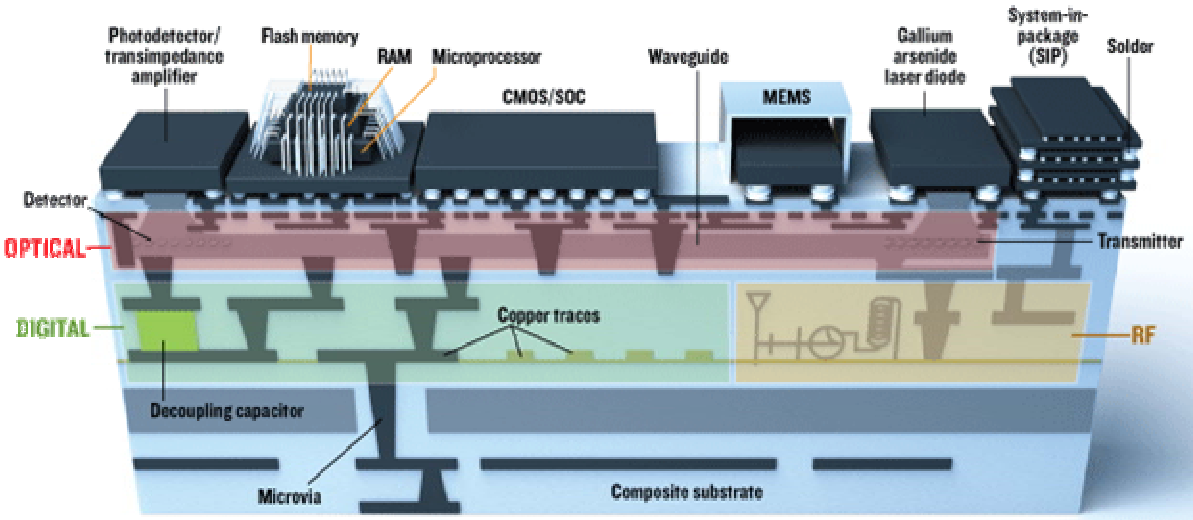


Figure 1.2. The state-of-the-art mixed-signal SOP technology [10]

1.2. Characterization of High-frequency Materials

Embedded-passive technology plays a crucial role in the SOP platform because the passive component often occupies more than 80% of the real estate in the board,

while the assembly cost accounts for around 70% of product assembly cost [11]. The embedded-passive technology makes an overall board size smaller, leading to higher throughput. It also helps improve the electrical performance because it eliminates soldering, which in turn improves system reliability while achieving both cost reduction and fast time to market by removing surface-mount devices (SMDs). Such advantages as lower cost, compactness, reliability, and higher performance make the embedded-passive technology a suitable package solution for systems as well as a key technology for higher integration.

Accordingly, the need for an extended supply of high-frequency packaging materials with high performance has become critical. Teflon and ceramic-based materials have been commonly used in high-frequency applications for many years [12]. Recently, the use of low-temperature, co-fired ceramic (LTCC) technology, or MCM-D technology [1], [3], [4], [5], [6], [7], and [8] in RF circuit design, has become very popular because of its advantages, including low loss, high integration density, and high reliability. LTCC, a multi-layer ceramic technology, enables the embedding of passive components into multiple layers while active elements are mounted on the surface layer. Although LTCC can provide high-Q passives, it cannot be used as a final substrate for systems. In addition, because of its coefficient of thermal expansion (CTE) mismatch with printed wiring board (PWB), it can lead to reliability issues.

In contrast, liquid crystalline polymer (LCP) can provide high-Q passives embedded in the packaging substrate [13]. However, unlike LTCC, LCP allows designers to achieve completely integrated wireless systems [4] since the LCP process is compatible with PWB processes such as FR-4. Therefore, LCP can ultimately become

the final PWB. If used as a module, LCP has a similar CTE as PWB. To effectively integrate the entire system into a package, multi-layer integration is essential due to its vertical integration capability in addition to lateral integration. A typical multi-layer substrate is composed of homogeneous materials, including LCP. However, a homogeneous LCP process requires a higher temperature process (290 °C) than inhomogeneous LCP process (less than 200 °C). In addition, the difficulty in controlling the flow of bonding film causes registration problems, which limit the number of layers.

Other organic materials besides LCP also have been used for integration. Sanmina ZBC2000 in [14] provides improved electromagnetic interference (EMI), improved reliability, and improved manufacturability with lower cost. While LCP has a loss tangent of 0.002, ZBC 2000 has a loss tangent of 0.015, resulting in higher losses compared to LCP losses for embedded RF circuits. Dupont HK04 is an all polyimide, unfilled dielectric. Even though it provides excellent voltage resistance, its water absorption of 0.8% is much higher than that of LCP, which is 0.04% [15], and hence, Dupont HK04 causes large variations in RF performance. Since the circuit size decreases as operating frequency increases, the impact of water absorption on RF performance can be significant for most organic materials.

As an alternative solution to homogeneous LCP technology, inhomogeneous, multi-layer LCP-based substrates were developed, and they have demonstrated their manufacturability and high performance [1], [16], [17], [18], [19], and [20]. To fully utilize this new multi-layer inhomogeneous LCP substrate, a thorough characterization of the entire stack-up is required. Unlike the characterization of homogeneous multi-layer stack-ups such as LTCC, the characterization of inhomogeneous multi-layer LCP

substrates requires the characterization of embedded structures, including transmission lines, vias, inductors, and capacitors.

The characterization of LCP for multi-chip module technology was introduced in [21]. This approach was based on exploiting the barrier and dielectric properties of LCP to interconnect and package MMICs. For RF characterization, LCP films were bonded onto a 20-mil thick alumina substrate having metallization on one side and laminated with conventional 9-um copper foil. Transmission lines, CPW, cavity backed CPW, and ring resonator were characterized for extracting the electrical properties of this homogeneous LCP substrate. The attenuation of 0.3dB/cm was achieved at 35 GHz, which was low enough for packaging applications even though it is not low enough in comparison to Duroid. A 125-um homogeneous LCP BIAC copper clad laminate with 18um copper foil was characterized in [12].

A ring resonator was used to extract the relative dielectric constant at discrete frequency points up to 35 GHz in [22]. A 125um LCP using CPW structures up to 50 GHz was also characterized in [22]. Line-reflect-match (LRM) calibration was performed and the results showed attenuation of 1dB/cm at 50GHz, but only one CPW structure was used. The authors in [23] and [24] did more intensive characterization on a homogeneous LCP substrate. The authors in [24] used a 50um LCP with 18um copper foil on both sides to characterize attenuation and effective dielectric constant using a cavity-backed CPW structure up to 110 GHz. This work was extended by comparing the results with results using the cavity resonator method in [24]. Although the above mentioned characterizations are valid up to the millimeter-wave region, they only have characterized single-layered LCP substrate. This is because most research has been based on

homogeneous multi-layer LCP technology such as in [11], [25], and [26]. However, homogeneous multi-layer LCP has not been used for product manufacturing because of its processing difficulties and higher cost resulting from smaller board size and melt temperature.

1.3. Characterization of Vias

A via, a widely used vertical structure, connects separate layers in chips, packages, and boards. Figure 1.3 shows the vias in a system-on-package (SOP) structure, in which the package-level vias are circled. It consists of a barrel, a pad, and an anti-pad, as shown in Figure 1.4. The barrel is a structure that connects the layers with conductive materials, and the via pad connects the barrel to other traces or components. An anti-pad is a clearance between the via pad and the nearest metal on the layer.

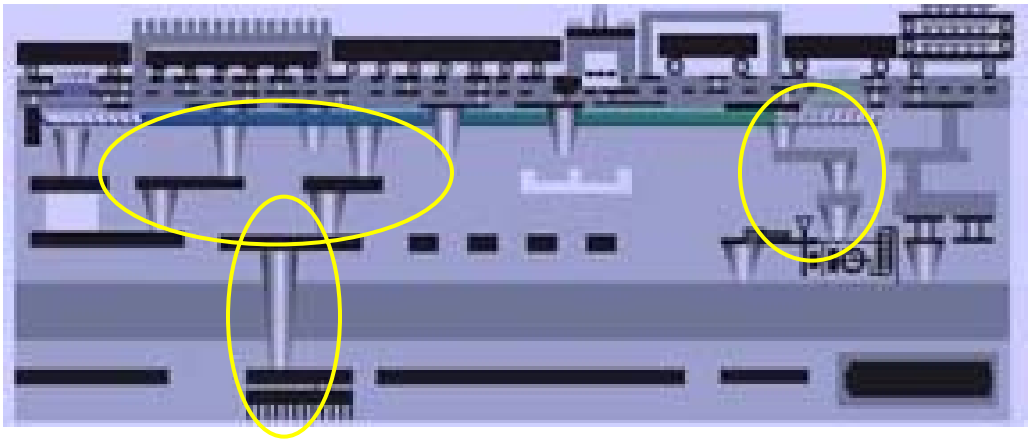


Figure 1.3. The vertical interconnects in SOP

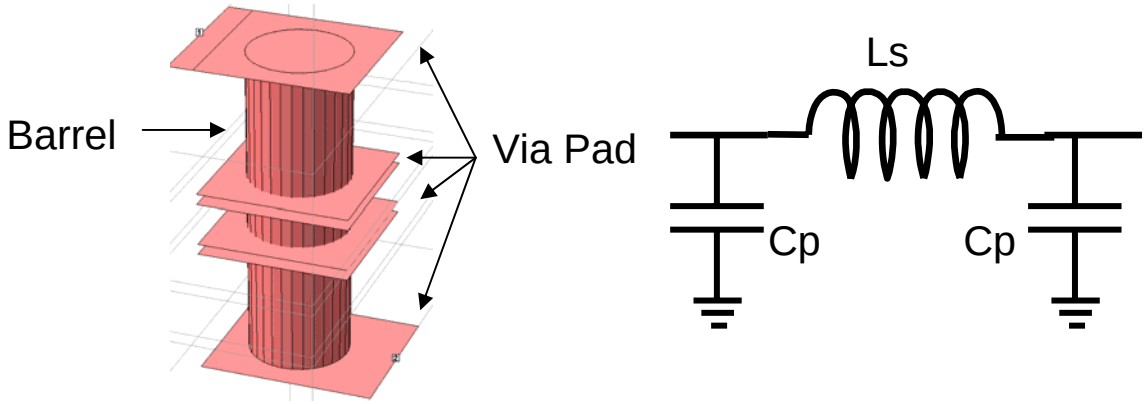


Figure 1.4. The structure of a via and its equivalent circuit model

Figure 1.4 also shows an equivalent circuit model composed of a series inductor representing the barrel inductance and parallel capacitors representing the capacitances between the pads and the ground. The approximate value of capacitance can be calculated from [27]:

$$C_{via} \approx \frac{1.41\varepsilon_r D_1 T}{D_2 - D_1} \text{ pF}, \tag{1-1}$$

where D_1 is the diameter of the via pad, D_2 is the diameter of the anti-pad, T is the thickness of the board, and ε_r is the relative dielectric constant. The approximate value of inductance can be calculated from [27]:

$$L_{via} \approx 5.08h[\ln(\frac{4h}{d}) + 1] \text{ nH}, \tag{1-2}$$

in which h is the via length and d is the barrel diameter with units of inches. The rule of thumb for the inductance is 25nH per inch for a 1mil diameter rod. The inductance is inversely proportional to the natural log of the diameter [28].

Importance of accurate modeling of vias increases as the operating frequency and data rates increase. Small parasitics in the signal path cause signal distortions that can lead to system failure. In [13], [29], and [30], the authors used 8 mil through holes for vertical connections because of easy processing and fast fabrication time, even though micro vias, the diameter of which is less than 4 mil, were available for inhomogeneous multi-layer LCP stack-ups. However, 8 mil through holes introduce unwanted parasitics to the precise high-frequency and high-speed circuits, leading to deviations in the responses between electromagnetic (EM) simulations and circuit-based simulations using Agilent Advanced Design System (ADS). The expected response therefore requires many iterations. To avoid time-consuming iteration in the EM simulation, both accurate modeling and the measurement of through holes are required.

Research on via characterization has focused on the modeling of vias using numerical methods such as the quasi-static and full-wave techniques. Although numerical methods can model and analyze vias, an EM solver can accurately model and optimize via structures more practically. In [31], the authors analyzed vias according to height, diameter, and ground openings using Maxwell Strata [32], a field solver based on the mixed potential integration equation. An equivalent circuit of a circular via in a stripline-to-stripline interconnect structure was modeled as a lumped inductance and a lumped capacitance. Then, the overall inductance and capacitance were obtained from the

simulated S parameters. Even though inductance and capacitance of the via were extracted, the simulated results were not confirmed with any measurement results.

The measurement-based via modeling approach was used in [33]. In that paper, a half-wavelength T-resonator was used to characterize a single via structure up to 20 GHz, as shown in Figure 1.5. The pad capacitance was removed using an open dummy structure as in equations (1-3) and (1-4):

$$Y_{deemb} = Y_{meas} - Y_{open\_pad} \tag{1-3}$$

$$Z_{test\_via} = Z_{deemb} - 0.5 \cdot Z_{pad\_via} \tag{1-4}$$

Single, double, and quadruple vias were characterized up to 20 GHz. The above mentioned de-embedding method is not as accurate as the through-reflect-line (TRL) calibration method at higher frequencies.

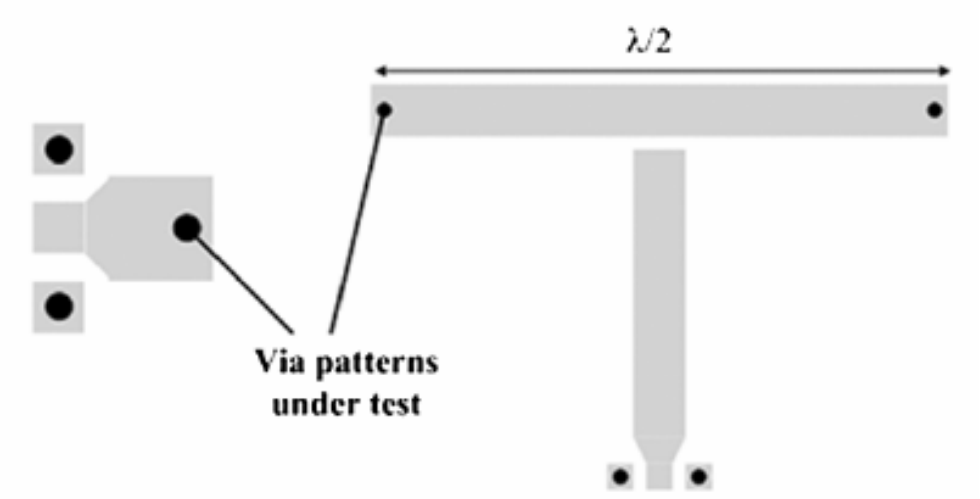


Figure 1.5. T-resonator for characterizing single via

1.4. Embedded Passive Technology; High-Q Passive Design

The improvements of Q-factor in LTCC-based, embedded-passive technology have been shown in [12], [34], and [35]. Vertically stacked helical inductors have a Q of 70 but need multiple layers (up to 19) to reduce the parasitic capacitance between spiral lines in [12] and [34]. The multi-layer inductor in [35] also achieved a Q of 60, but the placement of each spiral line of the inductor restricts effective utilization of the space in multi-layer RF SOP. In [36], the authors adopted an air cavity in multi-layer LTCC and showed a maximum Q of 51 and self-resonant frequency (SRF) of 9.1 GHz, while conventional spiral inductors showed a maximum Q of 43 and SRF of 8 GHz with an effective inductance of 2.7 nH. In [36], the air cavity reduced the capacitance between the spiral inductor line and ground plane, but it introduced additional processing, resulting in a cost increase and poor yield.

Although LTCC also can provide high-Q passives, it cannot be used as a substrate for systems because of its CTE mismatch. In addition, it has disadvantages, including wide line width and line-to-line spacing limitations, small processing area (typically 8″ x 8″), and high cost per component. Finally, the high roughness of metal lines also causes high loss because of skin effect, causing high power consumption.

LCP can provide high-Q passives embedded in the packaging substrate [1], allowing the designer to achieve completely integrated wireless systems [4]. LCP-based technology using fewer layers can achieve a lower profile than LTCC does. Such a low-profile characteristic is critical in RF-digital integration because stacking RF and digital modules on top of each other is an attractive option.

Low loss, minimal dependency on temperature, and the near hermiticity of LCP make it an excellent candidate for RF applications [37]. In [24], a single-layer LCP showed excellent material characteristics up to 110 GHz.

1.5. RF Front-end Modules using High-Q Embedded Passive Components

A filter is widely considered as an essential circuit in wireless communication and electronic systems. As a new standard is developed every year, the center frequency of new standards continues to increase, resulting in an increase of loaded Q in the filter. Such an increase in loaded Q places a lot of pressure on the unloaded Q of components, including inductors and capacitors. Mono-block and ceramic-cavity filters have been widely used for their high performance [11] because they can provide such high-Qs. Their benefits include sharp roll-off, low loss, and high performance [38]. However, they suffer from high manufacturing costs.

Rapid growth and advances in filter design result from the development of multi-layer, high-frequency substrates such as LTCC and LCP, together with the development of embedded passive components. Much research has already been conducted for the RF filter design in LTCC [39] and [40], but relatively few designs have been researched and implemented in the LCP substrate using embedded passive components [1], [1], [3], [4], and [41].

The single-layer LCP substrate for RF front ends has been characterized and applied to various applications such as low-noise amplifiers (LNAs) [42], filters, baluns [5], and voltage-controlled oscillators (VCOs) [43].

Lumped-element circuits can achieve a very compact size while maintaining good performance up to 10 GHz. The disadvantage of this approach is that it is not feasible to design a filter operating over 10 GHz because most of the embedded passive components resonate below 10 GHz, resulting in a decrease in Q as the frequency approaches SRF. This phenomenon also limits embedded passive values less than 20 nH for inductors and less than 10 pF for capacitors.

However, distributed circuits can overcome this frequency limitation. Large size, the main disadvantage of distributed circuits, can be less of a problem than at low frequency because the electrical wavelength gets shorter as the frequency increases. Many researchers have started designing 30-60 GHz filters in LTCC and LCP [26], [44]. All of the designs utilize single or homogeneous multi-layer substrates. It is still questionable whether these designs are suitable for mass manufacturing with low cost.

1.6. Completed Research

The goal of the research is to design and characterize the embedded RF passive components and circuits in inhomogeneous multi-layer LCP substrates up to 40 GHz.

For the characterization of inhomogeneous multi-layer LCP substrates, the embedded transmission lines in the substrates were characterized and attenuation per unit length was extracted. To validate the inhomogeneous multi-layer LCP substrate as a high-frequency material, this study compared the characterized attenuation characteristics to other high-frequency materials such as FR-4, LTCC and the homogeneous LCP substrate. This is the first characterization of inhomogeneous multi-layer LCP substrates

up to 30 GHz that has been reported in the open literature. In contrast, the characterization of the homogeneous multi-layer configuration has been reported [24].

For the characterization of via holes in the inhomogeneous multi-layer LCP substrate, this research proposes measurement-based via-hole characterization methods using periodic arrays of via holes. The extracted parameters are series inductance and parallel capacitances, with excellent model-to-hardware correlations in S parameters, characteristic impedance, and propagation constant.

For the design and characterization of embedded high-Q passives, inductors and capacitors were designed and characterized in this stack-up, and various components at two locations in three 12”x9” panels were characterized to test the process variations. The model-to-hardware correlation was verified after de-embedding and calibration techniques were applied.

The designed high-Q passives were incorporated with lumped-element RF circuit designs. A 5 GHz filter in triple-balanced inhomogeneous LCP substrate was designed. The lumped baluns and mixers were designed, fabricated, and measured in triple- and double-balanced inhomogeneous multi-layer LCP substrates for frequency ranges from 780 MHz to 5.8 GHz.

Finally, for millimeter wave application, a 30 GHz distributed band-pass filter was designed in multi-layer LCP substrate. The designed band-pass filters showed excellent model-to-hardware correlation with TRL calibration.

A major contribution of this dissertation is the development of interconnect, via, and embedded passive models that have been characterized up to 40 GHz in inhomogeneous multi-layer LCP substrates.

1.7. Dissertation Outline

The rest of this dissertation is divided into four main Chapters. Chapter 2 addresses the characterization of the material properties of inhomogeneous multi-layer LCP substrates. Section 3 presents the characterization methods of vias using periodic arrays of vias. Section 4 discusses the characterization of high-Q inductors and capacitors in inhomogeneous multi-layer LCP substrates and shows the scalability of Q by 3D integration. Section 5 presents designed lumped-element circuits such as filters, baluns, and mixers using high-Q embedded passive components, and a distributed gap-coupled 30 GHz band-pass filter. Finally, the conclusions and future work are discussed in Chapter 6.

CHAPTER 2

CHARACTERIZATION OF INHOMOGENEOUS LCP SUBSTRATES

2.1. Introduction

SOP provides an excellent system platform in that it can provide high-quality embedded passive components. The realization of high-Q embedded passives in SOP depends highly on the substrate material, and therefore, new high-frequency materials have been studied by several researchers. Inorganic (ceramic) substrates have been used for last few decades. It is high-k, low-loss and multi-layer solutions, and it can provide high-Q passives. However, it is relatively small-size process, 8" x 8", resulting in higher cost solution than large panel process. High-temperature requirement for the process and tape shrinkage are another drawbacks of the inorganic-based technology. Organic-based technology can be divided into homogeneous and inhomogeneous substrates. One promising high-frequency organic material is LCP, which presents excellent high-frequency electrical characteristics, including low loss and low-moisture uptake. One possible multi-layer LCP structure is homogeneous LCP, as shown in Figure 2.1.

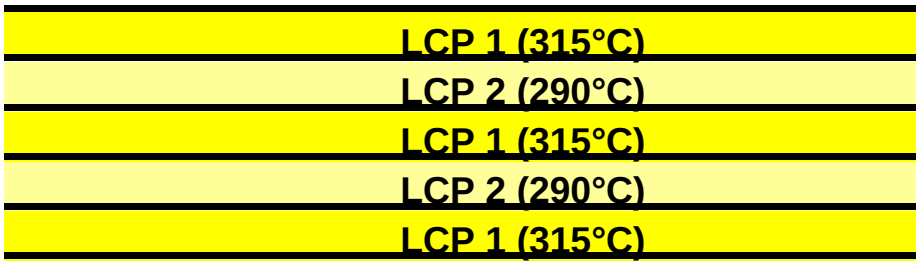


Figure 2.1. Cross-section of the homogeneous LCP substrate with melt temperatures

It is composed of multiple LCP layers that have different melting temperatures that are stacked together. Homogeneous LCP can provide high-Q passive components and excellent electrical performance since it utilizes homogeneous substrates. In addition, thinner multi-layer solution is possible using thin LCP sheets. However, it is difficult to control the flow of the bonding film, which leads to registration problems. The registration problem limits the total number of layers in multi-layer solution. It is also not suitable for large-panel processing due to its manufacturability. As an alternative multi-layer structure, inhomogeneous multi-layer LCP substrates have proven to have excellent high-frequency properties with manufacturability related issues such as alignment tolerances. The inhomogeneous stack-ups are shown in Figure 2.2.

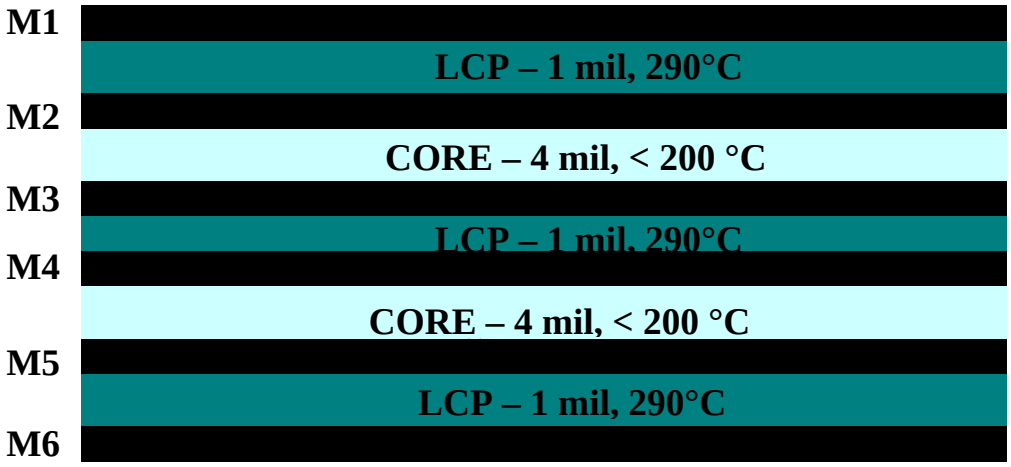


Figure 2.2. Cross-section of the inhomogeneous three-layer LCP substrate with melt temperatures

If the electrical properties of inhomogeneous LCP structure are to be fully exploited, conventional single-layer characterization, which was described in the previous chapter, cannot be used. Therefore, new research is needed to (1) characterize inhomogeneous multi-layer LCP substrates and (2) design and characterize high-Q embedded passives in inhomogeneous multi-layer LCP substrates. Furthermore,

measurement-based rigorous multiple via-hole characterization has to be performed because virtually every vertical interconnect is made using vias or thru-holes in 3D SOP technology.

Figure 2.3 shows a comparison of the process flows of LCP-based technology and LTCC-based technology. LTCC uses 18 to 24 layers, which requires more processing time and cost. In contrast, because LCP-based technology uses three to six layers, it results in less processing time and cost. This also makes LCP-based technology more attractive for a low-profile mixed-signal system integration. In addition, LCP-based process has an advantage of the lower processing temperature of 177 to 280℃, while LTCC requires 450 to 850℃ (see Figure 2.3).

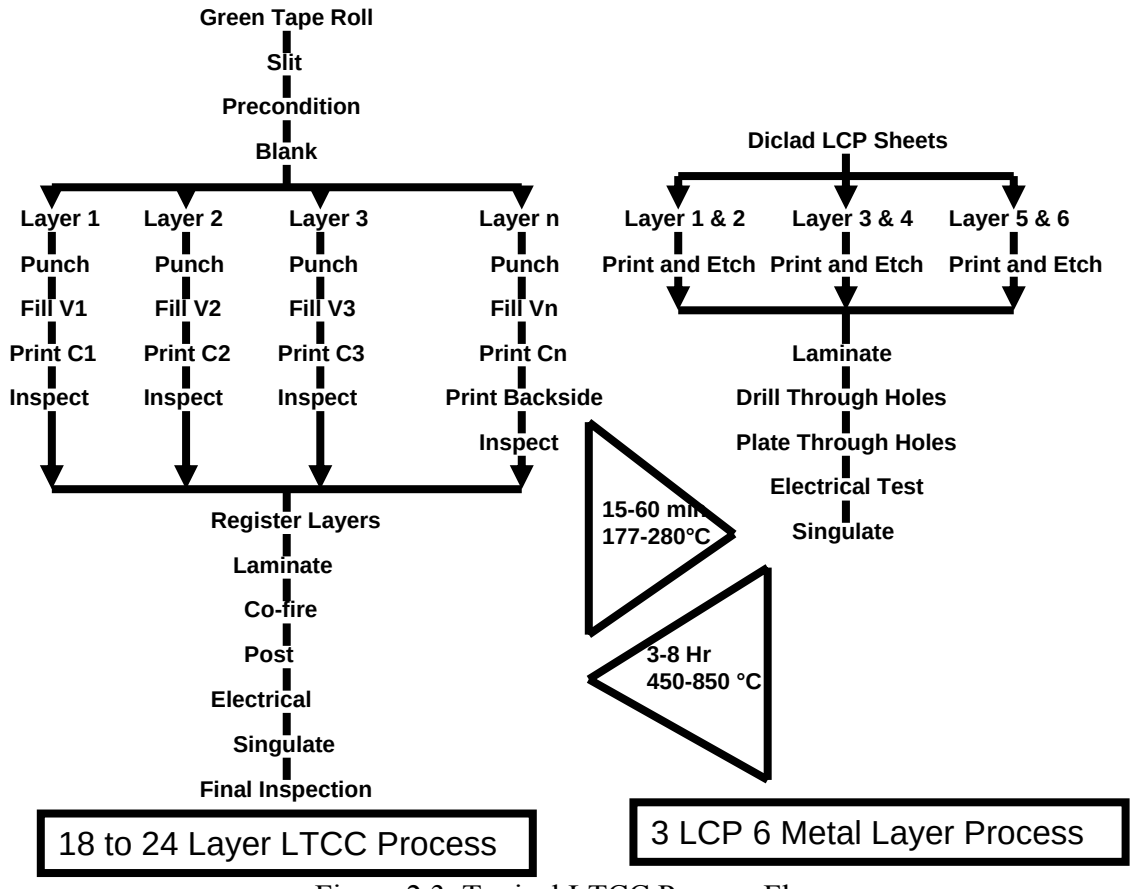


Figure 2.3. Typical LTCC Process Flow

This chapter focuses on the characterization of inhomogeneous multi-layer LCP substrates. The embedded transmission lines in the multi-layer substrates were characterized and attenuation per unit length were extracted. To validate the inhomogeneous multi-layer LCP substrates as a high-frequency material, characterized attenuation characteristics were compared with other high-frequency materials such as FR-4, LTCC and homogeneous LCP stack-ups.

2.2. Inhomogeneous LCP Technology

Both LCP and LTCC can consist of vertically integrated layers that allow for 3D integration. However, LCP can be integrated inside printed circuit boards (PCBs), while LTCC is not compatible with PCB processes. The LCP-based technology is available in single-layer [3], [4], [9], [37], three-layer [5], [6], [30]and balanced configurations[6], [13], [41]. The inhomogeneous multi-layer LCP structure was introduced in [30], in which a 5 GHz double-balanced mixer was designed using embedded passive components in a triple-layer inhomogeneous LCP substrate. The inhomogeneous multi-layer LCP technology is a low-cost, low-temperature, high-performance, and large panel process alternative to homogeneous LCP substrates and therefore can be used for high-frequency applications. The inhomogeneous LCP technology was invented and developed at Georgia Tech. Packaging Research Center (PRC). In [13], high-Q embedded passive components were characterized in inhomogeneous multi-layer LCP substrates and showed a high-Q factor. Since inhomogeneous multi-layer LCP stack-ups utilize different core and pre-preg materials with 25 um-LCP layers in between, the characterization of such inhomogeneous LCP stack-ups are necessary, which is the focus

of this chapter.

A three-layer LCP cross-section is shown in Figure 2.2. Three LCP layers are bonded together by lower-melt adhesives (CORE). This process combines 25 um thick LCP dielectrics with low-loss tangent glass-reinforced organic prepregs in a multi-layer stack-up. Based on this process, four to ten metal layer laminates can be fabricated. The LCP layers have a dielectric constant of 2.9 and a loss tangent of 0.002 at 10GHz and 23°C. The adhesive layers have a loss tangent of 0.0035 with a dielectric constant of 3.38. The top-metal layer (M1) of the cross-section can be used for SMDs and for high Q (>100) inductors in [11]. The thickness of the copper layers (M1-M8) is 17 um. The bottom-metal layer (M6) can be used as a microstrip ground. The ability to form micro-vias in the stack up represents an improvement in component and routing density.

The cross-section of the balanced-LCP substrate is shown in Figure 2.4. Two balanced-LCP layers were circuitized separately, followed by the lamination of LCP layers using organic pre-preg layers. Thru-holes were mechanically drilled and plated to form interconnections. A liquid-photoimageable solder mask was used, and an electroless nickel immersion gold finish was plated on the bond pads and terminals. All processes, including lamination (<200°C), electroless and electrolytic copper plating, and dry film photoresists, are compatible with standard FR-4 and PCB processes. The panels were fabricated on 12" x 18" and 9" x 12" panels using large-area PCB tooling. The large-panel process results in low-cost implementation that can be easily scaled to an 18" x 24" panel for further cost reduction. Typically, ceramic or LTCC components are manufactured on a panel size of 8" x 8". The fabrication of components on 18" x 24" panels can yield more than 5,400 devices of 5mm x 5mm size, which results in more than

a ten-fold increase in number of components for a given board over ceramic-based processes.

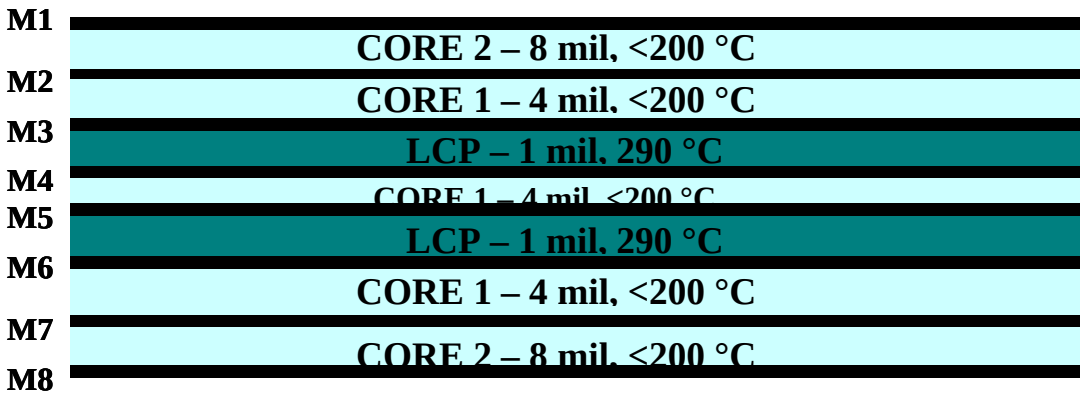


Figure 2.4. Cross-section of two-layer balanced LCP substrate with melt temperature

The high-precision RF passive components in the LCP layers are packaged using laminate layers, providing mechanical strength and enhanced reliability. Unlike conventional PCB materials, the proprietary process technology utilizes organic dielectrics with extremely low moisture uptake comparable to ceramic dielectrics. Typical moisture uptake rates for the packaging materials are less than 0.05%, leading to ceramic-like near-hermetic packaging at organic PCB manufacturing costs. The fully-packaged substrate has CTE matched to the typical organic materials used in PCB technology such as FR-4 with CTE around 18-20ppm/°C.

The CTE match allows for large modules to be implemented with very high reliability. The material set can be adjusted to tailor the CTE of the package in the 3-20ppm/C range, resulting in expansion-matched packages and modules for various RF IC platforms, including Si CMOS, SiGe, and GaAs. IC assemblies, high-frequency electrical and full functional testings, and over-molding operations are performed on the sub-panels of 6" x 6" prior to dicing the individual modules. A novel and proprietary

structure, developed as a part of this research, allows for the on-board RF shielding of each of the devices prior to singulation, in turn precludes the need for EMI cans, which increase both cost and size. This novel and patented approach results in higher performance with a much lower cost than ceramic-based technology [45]. Figure 2.5 shows the processing flow of multi-layer LCP technology.

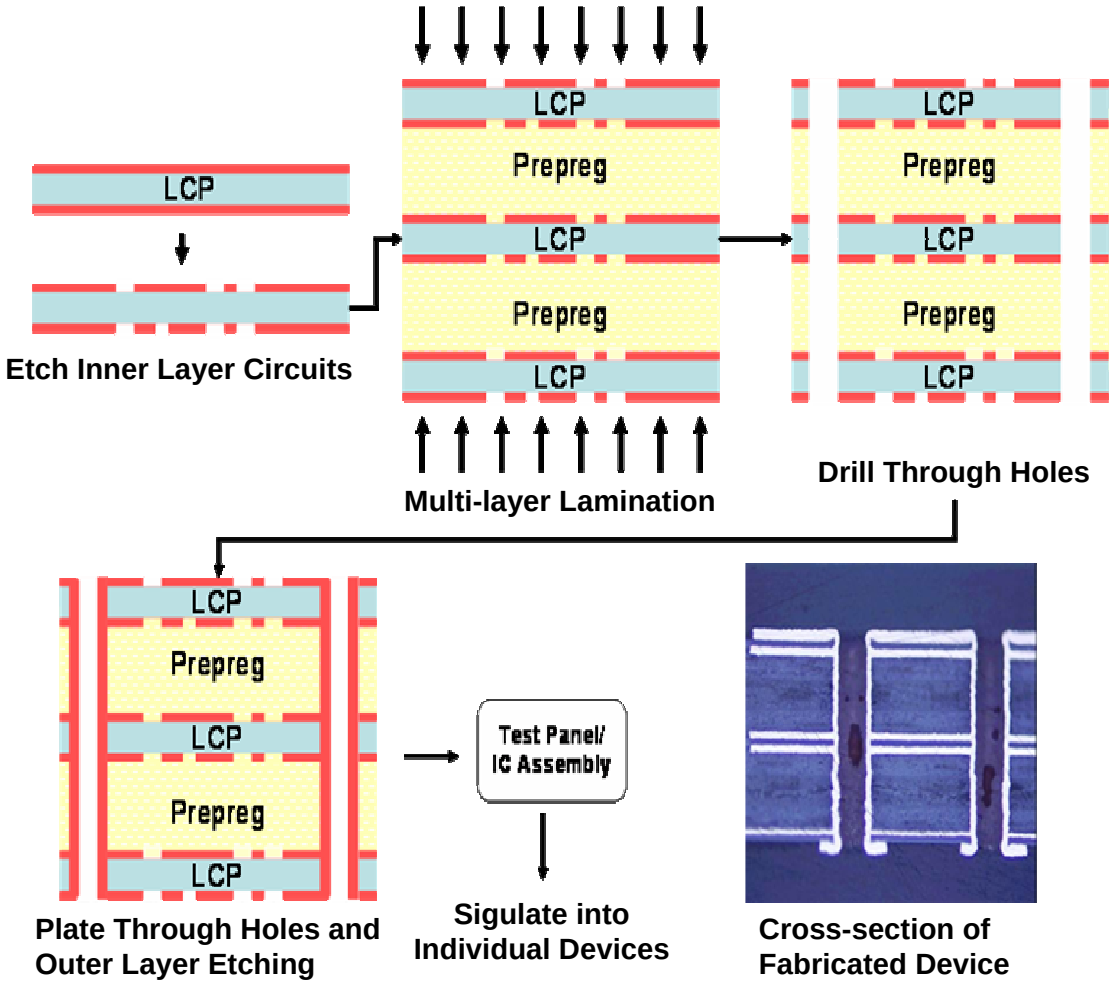


Figure 2.5. Multiple LCP Layer Process Flow

2.3. Loss Characterization of Inhomogeneous LCP substrates

In Figure 2.4, the top metal layer (M1) of the cross-section can be used for surface

mount components while the bottom metal (M8) can be used for the microstrip ground layer. M2 and M7 have not been used in the design, but additional metal layers can be used as needed. Three different transmission lines of 214, 814, and 3214 mil were characterized in M3, M4, M5, and M6. Figure 2.6 shows x-rays of the designed embedded transmission lines. In M3 and M5, the ground clearances for the signal via are shown, and the line-width of the transmission lines decrease as lines are closer to the ground layers because the characteristic impedances of the lines decrease.

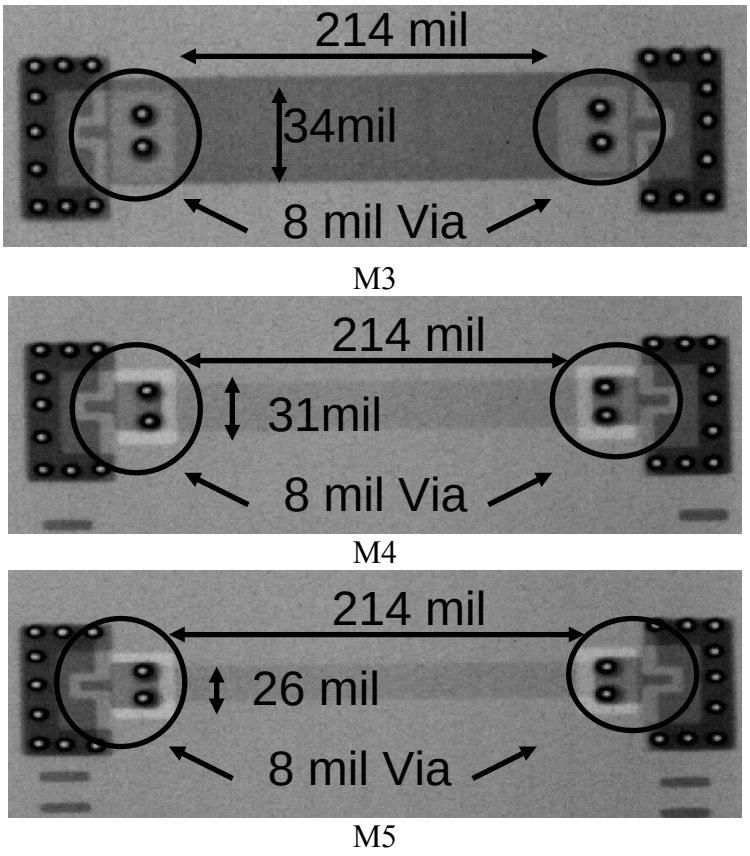


Figure 2.6. X-rays of the 214 mil transmission lines in M3, M4, and M5 in inhomogeneous multi-layer LCP substrates

To achieve 50 Ω characteristic impedance up to 40 GHz, each transmission line in M3 to M6 was simulated in full wave solver SONNET [46]. Short-open-load-through

(SOLT) calibration was conducted up to 40GHz with the Cascade 250 um GSG probes. S11 and S21 were measured using the Agilent PNA 8363B and the Cascade probe station. Figures 2.7 and 2.8 show the measured S11 and S21 of three fabricated embedded transmission lines with three different lengths on M3 and M5.

Figure 2.7 shows the signal flow graph of the measurement setup including input and output transition indicated as circles. The signal flow graph analysis below shows that the S_{21} of transmission lines with lengths of L1 and L2 (L1≠L2) can be expressed as (2-1), and (2-2). The transmission line section of the structure can be expressed as (2-3).

$$S_{21,L1} = \frac{b_2}{a_1} = \frac{S_{21,IN} \cdot S_{21,DUT1} \cdot S_{21,out}}{1 - S_{22,IN} \cdot S_{21,DUT1} \cdot S_{22,out} \cdot S_{12,DUT1}} \tag{2-1}$$

$$S_{21,L2} = \frac{b_2}{a_1} = \frac{S_{21,IN} \cdot S_{21,DUT2} \cdot S_{21,out}}{1 - S_{22,IN} \cdot S_{21,DUT2} \cdot S_{22,out} \cdot S_{12,DUT1}} \tag{2-2}$$

$$S_{21,\,DUT1} = e^{-\gamma L1},\ S_{21,\,DUT2} = e^{-\gamma L2} \tag{2-3}$$

To obtain the attenuation constant, (2-1), (2-2), and (2-3) can be combined such that:

$$e^{-\gamma(L2-L1)} = \frac{S_{21,\,L2}}{S_{21,\,L1}} \cdot \left(\frac{1 - e^{-\gamma L1} \cdot S_{22,\,IN} \cdot S_{22,\,OUT}}{1 - e^{-\gamma L2} \cdot S_{22,\,IN} \cdot S_{22,\,OUT}} \right) \tag{2-4}$$

If $\left| e^{-2\gamma L} \cdot S_{22,\,IN} \cdot S_{22,OUT} \right| << 1$ (assuming good match),

then,

$$e^{-\gamma(L2-L1)} = \frac{S_{21,L2}}{S_{21,L1}} \Rightarrow \alpha = real\left[\frac{S_{21,L2}(dB) - S_{21,L1}(dB)}{L_2 - L_1} \right] \tag{2-5}$$

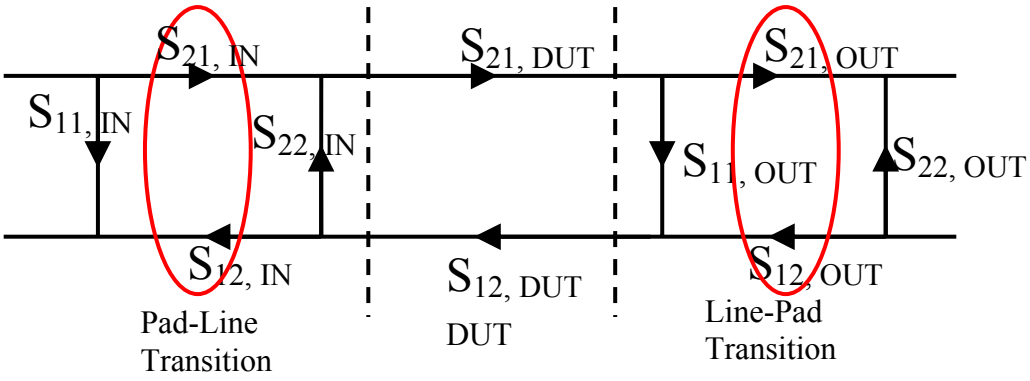


Figure 2.7. Signal flow graph of the measurement set up for embedded transmission lines

Attenuations per unit length can be extracted from equation (2-5). 250 um GSG pads were carefully designed to guarantee a good match between the probes and pads. A full wave solver, SONNET [46] was used to simulate the pads to minimize the return loss from the input and output pads.

The top metal layer (M1) of the cross-section (See Figure 2.2) can be used for surface mount components, while the bottom metal (M8) can be used for the microstrip ground layer. M2 and M7 have not been used in the design, but additional metal layers can be used as needed. Three different-length transmission lines of 0.615 cm, 2.15 cm, and 8.12 cm, as shown in Figure 2.6, were characterized on metal layers M3 through M6. To ensure 50 Ω up to 40 GHz, each transmission line was simulated in SONNET [46]. The short-open-load-through (SOLT) calibration was conducted up to 30GHz with Cascade 250 um GSG probes. S11 and S21 parameters were measured using an Agilent PNA 8363B and a Cascade probe station. Figures 2.8 to 2.11 show the measured S11 and S21 of three fabricated embedded transmission lines with three different lengths on layers M3 and M5.

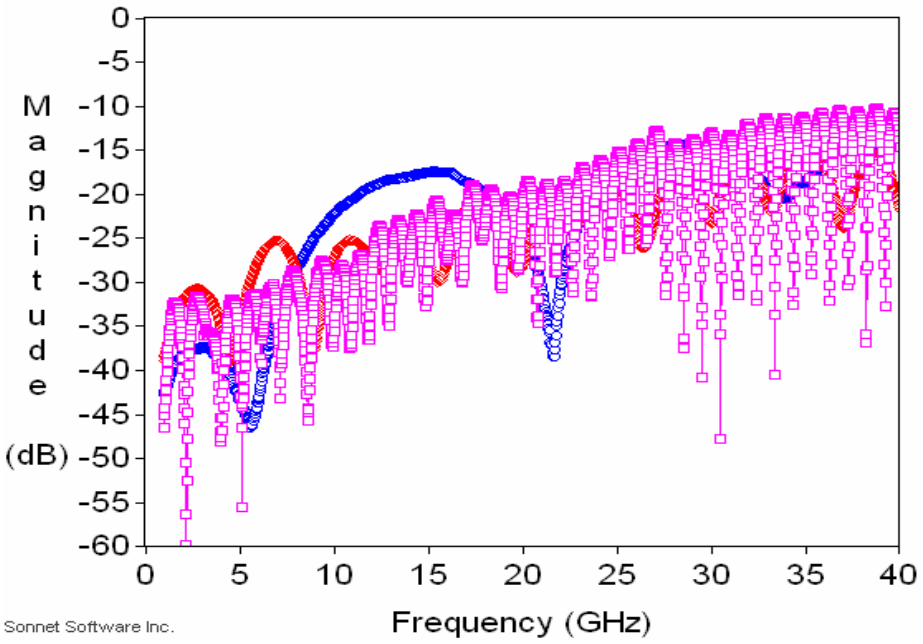


Figure 2.8. Measured S11 of the embedded transmission lines in M3

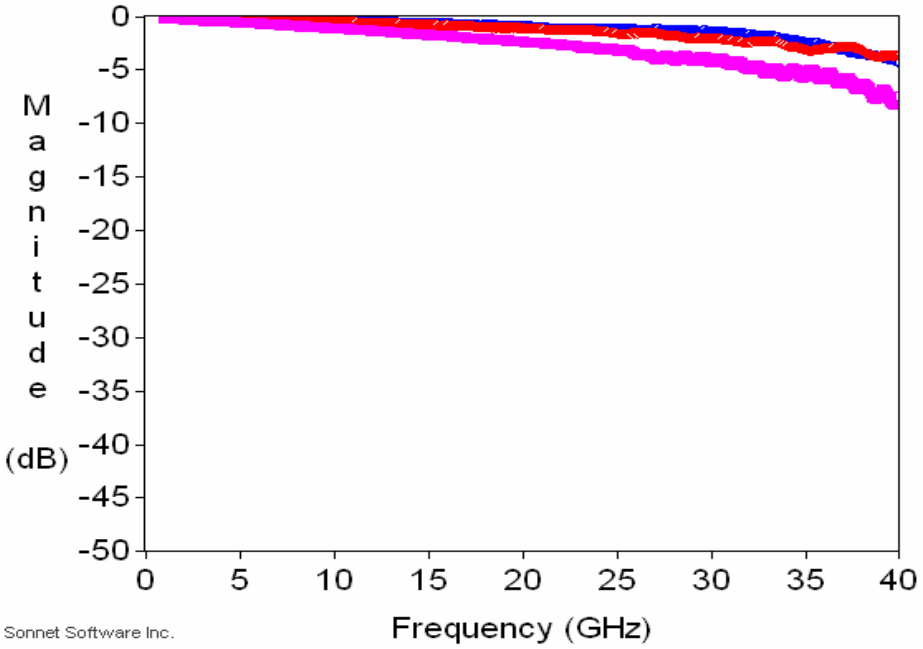


Figure 2.9. Measured S21 of the embedded transmission lines in M3

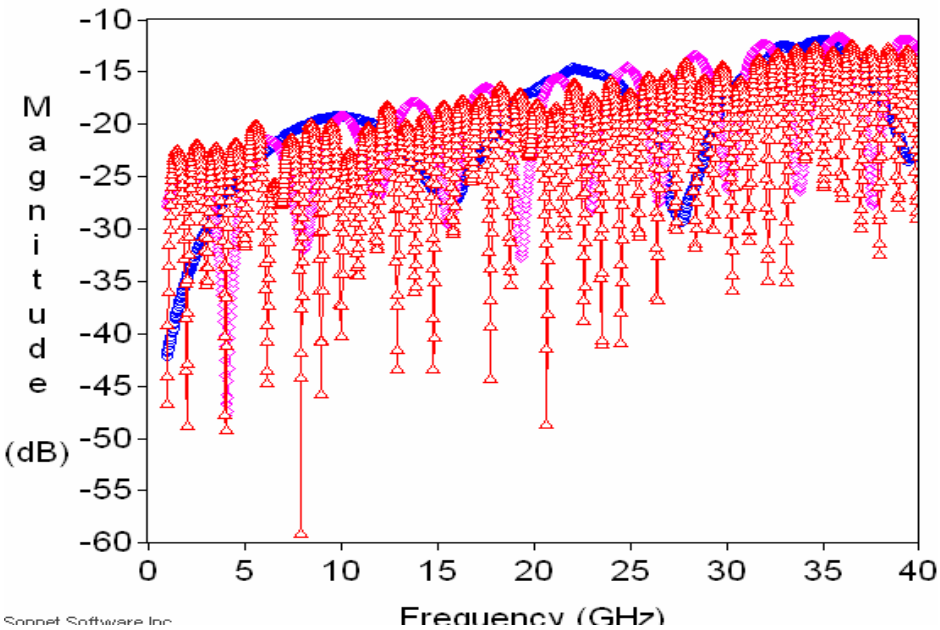


Figure 2.10. Measured S11 of the embedded transmission lines in M5

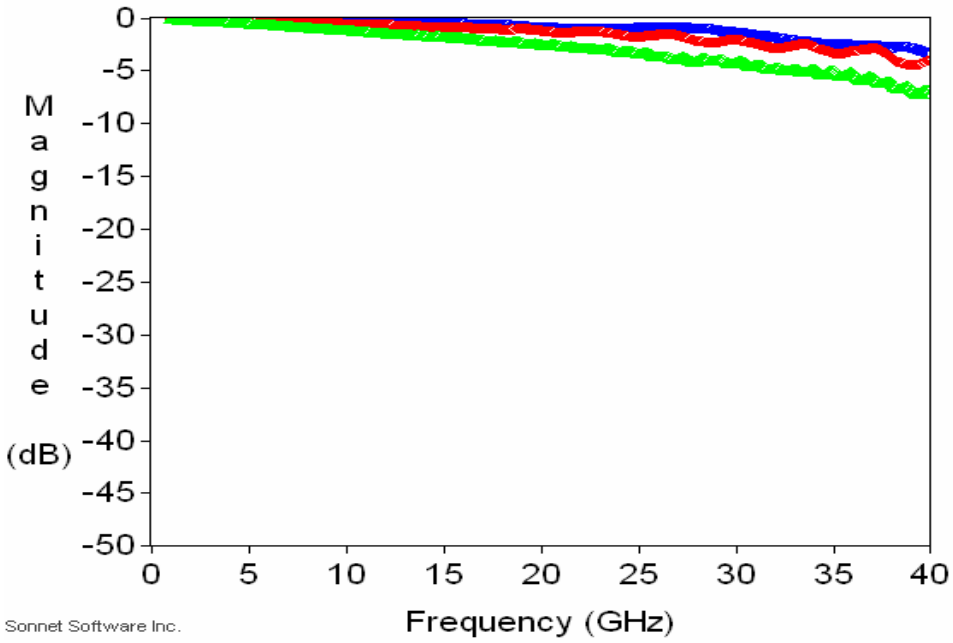


Figure 2.11. Measured S21 of the embedded transmission lines in M5

As shown in Figure 2.12, the attenuation per inch on each layer was extracted from equation (5) using the individual measurements of embedded transmission lines with three different lengths on M3-M6 layers in Figure 2.2. Figure 2.12 also shows the attenuation characteristics of other high-frequency materials, including FR-4 [47], homogeneous LCP substrate [24], Dupont 951 Ag and the Dupont 943 Low Loss Ag system [48]. The dotted line is the loss of the 12 mil homogeneous LCP substrate, which was interpolated from [24]. The measured attenuation characteristics are much better than FR-4, and compatible with LTCC and homogeneous LCP substrates.

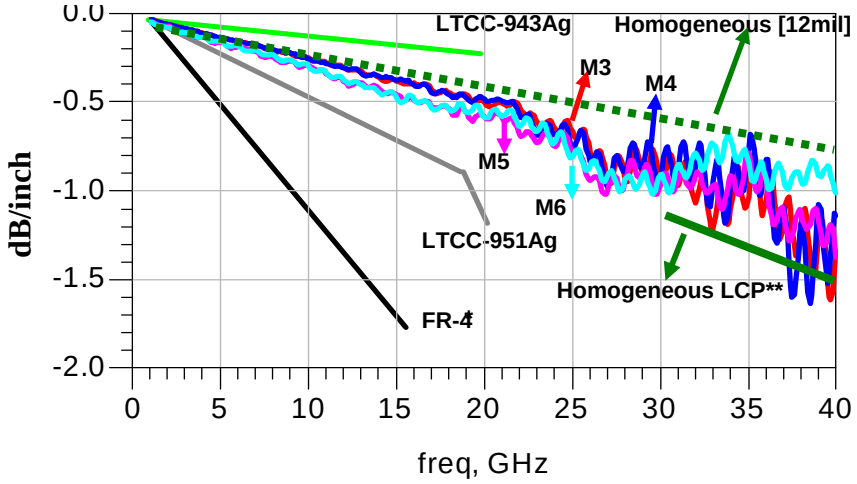


Figure 2.12. Attenuation characteristics [dB/inch] of inhomogeneous multi-layer LCP substrates, compared with other high-frequency materials

2.4. Model-to-hardware Correlation

The extracted characteristics of the embedded transmission lines were compared to the model using multi-layer model in Agilent ADS, combined together with via model from the same stack-ups. The inductance and capacitance of the identical through via (30 mil long, 8mil diameter) were characterized using measurement-based methods utilizing

multiple arrays of the vias from 20 to 40 GHz. The detailed method for via characterization is discussed in Chapter 3. The entire models for the embedded transmission lines are shown in Figure 2.13.

Since the embedded transmission lines were connected in the middle of the through via, the inductance values were scaled according to the corresponding length. The values of the inductances and capacitances for via connections are shown in Table 2.2. Figure 2.14 shows the model for via connections. A series inductor and parallel capacitor represent partial via connection between signal lines. The series inductance and capacitance to the ground represent the hanging via, connected to the ground through capacitive coupling. Figure 2.15 through 2.18 show the model-to-hardware correlation in loss characteristics for the transmission lines in M3 through M6.

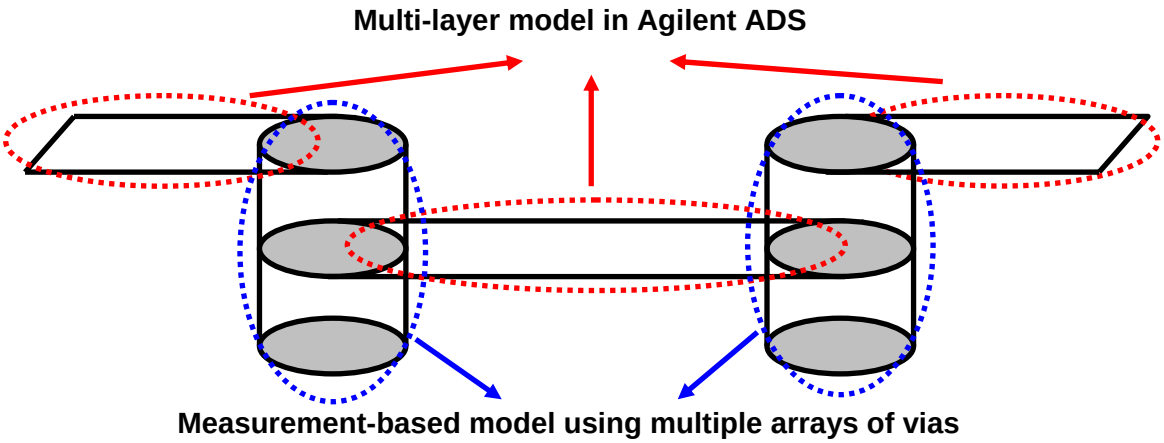


Figure 2.13. Model of the embedded transmission lines including through-via connections

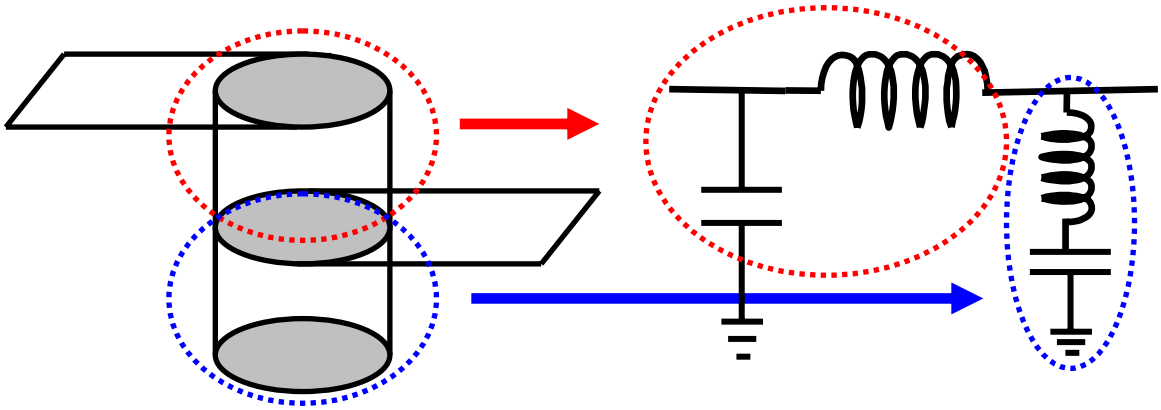


Figure 2.14. Model for the via interconnection between signal lines including parasitics to the ground because of the hanging portion of the through via

Excellent correlations are achieved between model and measured values up to 25 GHz. The deviations in the correlation after 25 GHz are resulted from model limitation, possible higher-order modes and surface roughness. At these high frequency, the height of the surface roughness are much profound compared to skin depth, the losses are significantly affected by the roughness of the conductor.

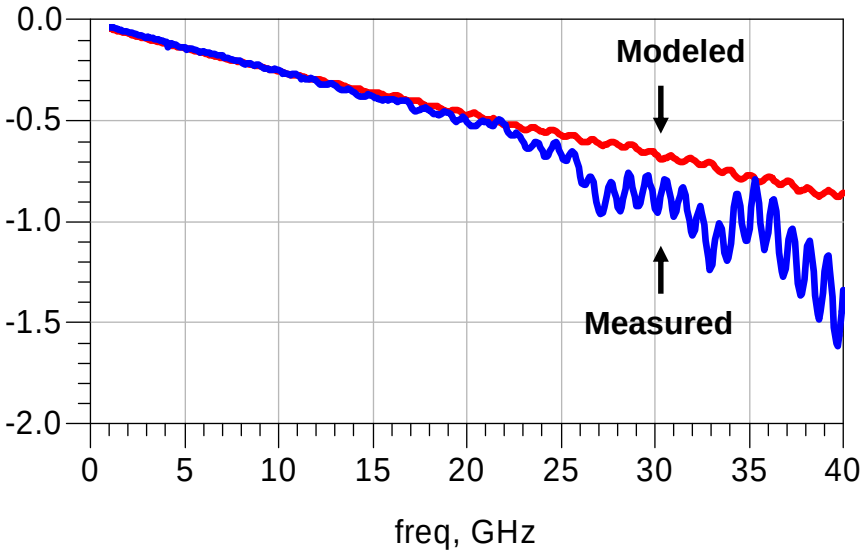


Figure 2.15. Model-to-hardware correlation of the transmission lines in M3

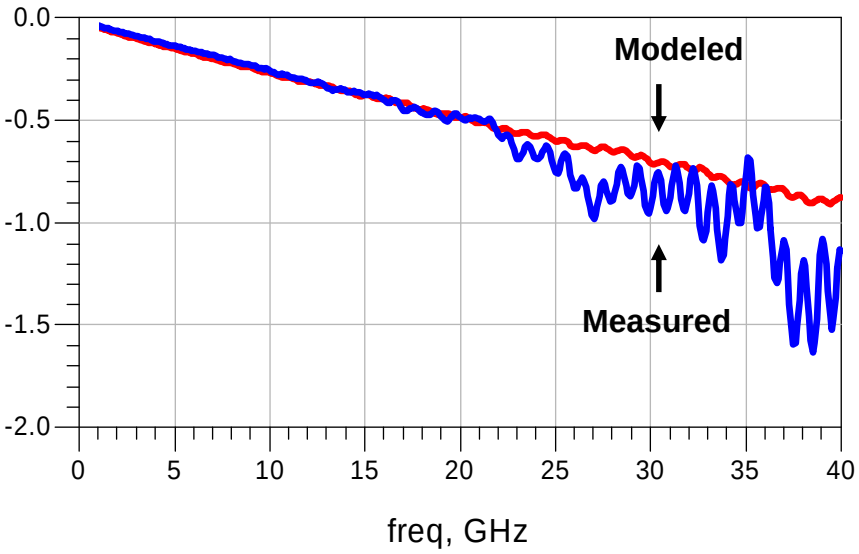


Figure 2.16. Model-to-hardware correlation of the transmission lines in M4

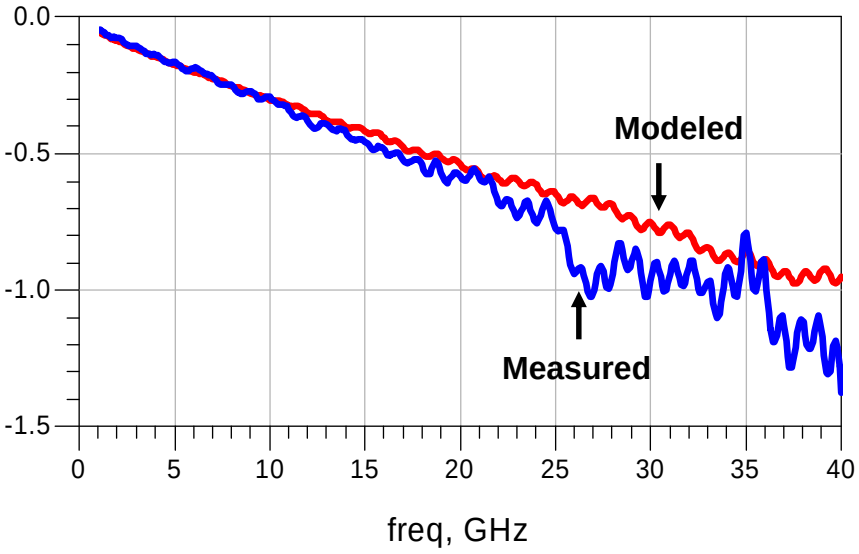


Figure 2.17. Model-to-hardware correlation of the transmission lines in M5

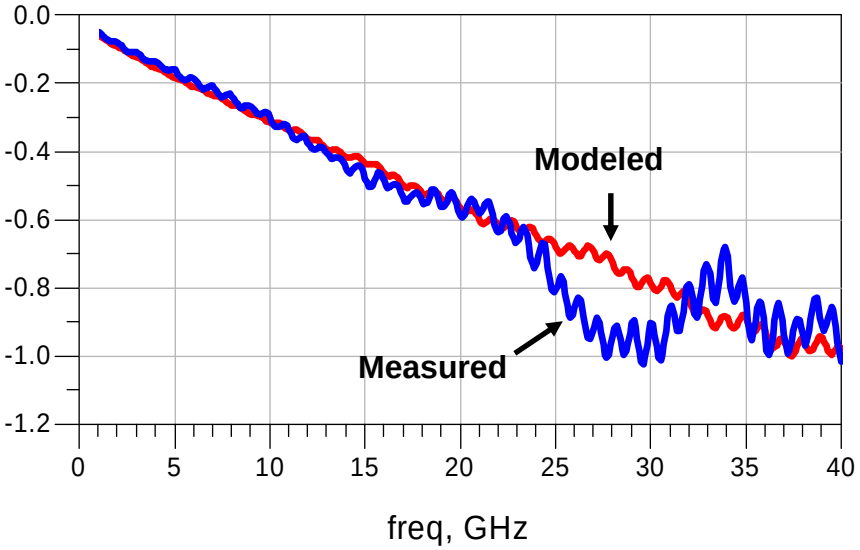


Figure 2.18. Model-to-hardware correlation of the transmission lines in M6

2.5. Summary

The attenuation properties of inhomogeneous multi-layer LCP substrates were extracted up to 40 GHz. This is the first result for an inhomogeneous LCP stack-up that has been reported. The characterization results show excellent loss characteristics, much better than FR-4-based technology, and they are similar to LTCC and homogeneous LCP-based technology. This result confirms that such a stack-up, which is more easily manufacturable, can be used to design RF and microwave circuits.

Model-to-hardware correlation was verified using multi-layer model in Agilent ADS and measurement-based via model using arrays of the vias. To apply through via values to the designed via connections, the extracted inductor values were scale according to the corresponding length of vias between the transmission lines. This showed the excellent model-to-hardware correlation.

CHAPTER 3

MEASUREMENT-BASED TWO-PORT CHARACTERIZATION OF VERTICAL INTERCONNECTS

3.1. Introduction

An increasing demand for multi-function, high-performance, and small form-factor systems necessitates highly-integrated systems. In addition, as demand for higher bandwidth has continued to increase, more fine-pitch arrays of interconnects between chip to chip, chip to substrate are required [49]. To support such a demand, a promising candidate is three-dimensional (3D) integration. In 3D integration, vertical interconnects play an important role for high-frequency and high-speed applications such as communication devices and high-performance computing systems, as shown in Figure 3.1.

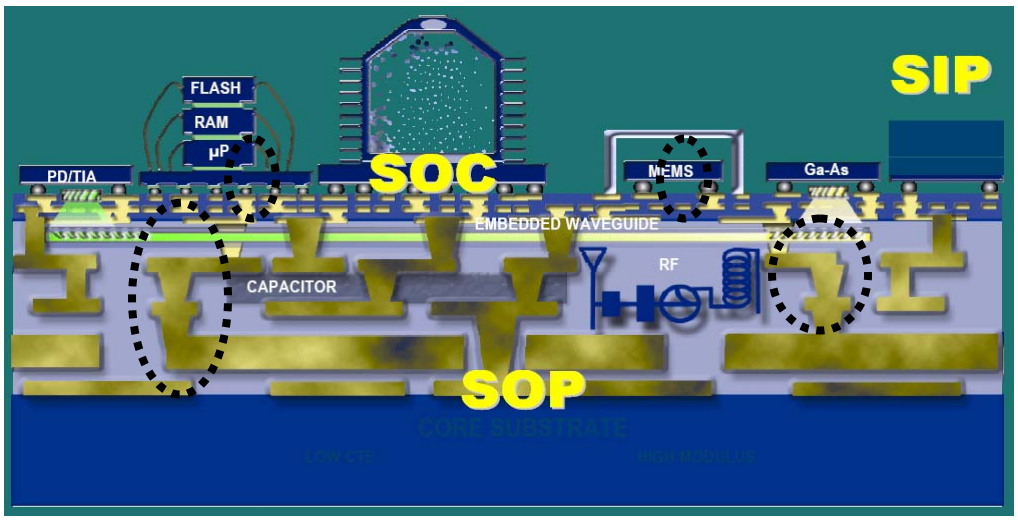


Figure 3.1. Vertical interconnects in 3D integration using SOP

As operating frequencies and data rates increase, both horizontal and vertical interconnects should be controlled to maintain their electrical characteristics, including characteristic impedances, delays, and parasitics. Impedance mismatches and delays can affect signal quality by decreasing the edge rates in high-speed systems and by increasing the return loss in high-frequency circuits. However, in general, vertical interconnects have not been designed to precisely meet the rigid specifications because of routing complexities and processing limitations. Therefore, interconnects must be designed so that they are more accurately characterized, and the extracted parameters can be referenced for future designs. The characterization of more fine-pitch interconnects with low parasitics, such as G-helix in [49] is very challenging, but it is very critical at high-speed and high-frequency applications. Accurate method is required to properly extract the electrical properties of vertical interconnects such as vias and G-helix [49].

This chapter focuses on the development of the measurement-based characterization methods for vertical interconnects. The advantages and disadvantages of the current methods are addressed and measurement-based via characterization using arrays of vias are introduced in following section. The parasitic inductance and capacitance were extracted using this method and the extracted values were compared to the simulated values. Finally, the equivalent model and the extracted values are presented.

3.1.1. One-Port Characterization

The simplest characterization of vias is one-port characterization because it requires a single calibration for measurement. However, since it relies on S11 to extract the inductance and the capacitances, it is not suitable for very low impedance structures, including vias, power distribution networks (PDN), and de-coupling capacitors [28]. The

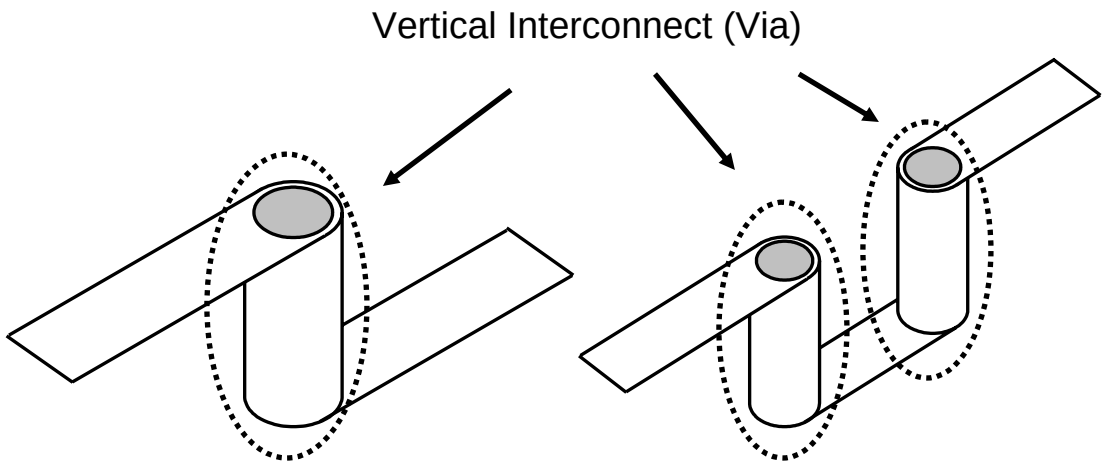
impedance of the device under test (DUT) can be obtained as (3-1):

$$S_{11} = \frac{Z_{DUT} - Z_0}{Z_{DUT} + Z_0} = \frac{Z_{DUT} - 50}{Z_{DUT} + 50} \tag{3-1}$$

For 1Ω impedance, S_{11} is -0.35dB, which is acceptable, but for 0.1Ω impedance, S_{11} is -0.035dB, which is close to the tolerance of calibration errors in most vector network analyzers (VNA).

3.1.2. Two-Port Characterization

The previously discussed limitations of one-port characterization can be overcome using two-port characterization. Figure 3.2 shows two possible configurations of the two-port characterization of vias. Configuration 1, the simplest one, allows the effects of the input and the output transmission lines to be easily removed using either measurements or simulations. The drawback of this approach is that it requires two-sided probing that cannot be performed with a general probe station. This limitation can be overcome if Configuration 2 is used. This configuration is well suited for a conventional one-sided probe station. However, another limitation for one- and two port (both configurations) measurements for very low impedance structures is the parasitic effects on the overall characterization. Even with a very precise high-frequency probe, it still has a few residual, uncompensated inductances because of over-travel (downward movement of the probe after initial touchdown on the substrate) [28].



(a) Configuration 1 (b) Configuration 2

Figure 3.2. Two possible configurations for the two-port characterization of a vertical interconnect

Given an approximate inductance of 25 pH per mil for one-mil over-travel, the residual inductances of a 250 um GSG probe range from 75 to 125 pH since its calibration is based on an over-travel of 3 to 5 mil. The contact resistance varies from 0.01 Ω to 0.1 Ω, depending on the metallization of the probe tip and the surface of the pad [28].

During the characterization, the variation of the vias throughout the board must also be considered. That is, obtaining the average of the values from various vias in the one- and two-port characterization requires multiple measurements. In summary, one- and two-port characterizations have the following limitations.

(1) One-port characterization relies on S11 for the impedance measurement, which is not suitable for very low impedance measurements.

(2) One- and two-port measurements suffer from uncompensated residual inductances and contact resistances even with the microprobe.

(3) Two-port configuration 1 requires a two-sided probe station.

(4) Multiple one- and two-port characterizations are required for averaging the effects of process variations.

3.2. Principle of a Measurement-Based Two-Port Via Characterization

To overcome the previously mentioned limitations in the characterization of the vertical interconnects, this chapter provides a measurement-based two-port via characterization. The proposed characterization of the vertical interconnects does not require two-sided probing, and it is a two-port characterization, which does not suffer from the same limitations as the one-port characterization. In addition, it can significantly reduce the effects of the variation of residual inductances and contact impedances by a single characterization of via arrays.

Several challenges in two-port characterization are removing the effects of measurement setup and extracting pure interconnect data. To address these issues, the proposed characterization method extracts interconnect data from a periodic network with an assumption that interconnects are manufactured within a reasonable tolerance.

Figure 3.2 shows the general procedure for the proposed method. First, we convert a periodic structure composed of several identical unit networks, including unknown interconnects with two short line sections, to an equivalent lossy transmission line with the same length as that of the entire periodic network. A required measurement datum for this process is a transmission matrix (*ABCD* matrix) of the entire periodic network, which is modeled as a lossy transmission, as shown in Figure 3-4. That is,

$$A_T = \begin{bmatrix} \cosh \gamma' L & Z_0' \sinh \gamma' L \\ Y_0' \sinh \gamma' L & \cosh \gamma' L \end{bmatrix}, \tag{3-2}$$

in which $A_T = \begin{bmatrix} A_t & B_t \\ C_t & D_t \end{bmatrix}$ is the measured transmission matrix, γ', Z_0' are the propagation constant and the characteristic impedance of a lossy transmission line, and $L = Nl$ is the total length of the entire network, which is N times as long as section length l. The equivalent lossy transmission line is specified by its virtual characteristic impedance and complex propagation constant. These electrical parameters are obtained from the following formula [50]:

$$Z_0'^2 = B_t / C_t, \tag{3-3}$$

$$\gamma' = \frac{1}{L}\ln\left|A_t + \sqrt{B_t C_t}\right| + j\frac{1}{L}\left[\arg\left(A_t + \sqrt{B_t C_t}\right) + 2n\pi\right], \quad n = 0, \cdots, N-1. \tag{3-4}$$

The condition according to which the real value of the characteristic impedance should be positive in passive structures enables us to select one from two possible solutions in (3-3). Among N solutions of the propagation constant in (3-4), to choose one physically reasonable solution, the interconnect or via network was assumed to have small resistive values such that the imaginary part of the propagation constant is close to the propagation constant of the uniform transmission line. Thus, the selected propagation constant minimizes:

$$\left|\mathrm{Im}(\gamma') - \beta\right| \tag{3-5}$$

where, β is the propagation constant of the uniform line, obtained from the following formula:

$$\beta = \frac{2}{l}\arg\left(\frac{1 - S_{22}}{S_{21}}\right) \tag{3-6}$$

In (3-6), the S-parameters are the measured or simulated data of a transmission line

section. The selection criteria finds physically reasonable parameters more effectively than solving the N^{th} order equation or using other numerical iterative procedures.

With the virtual parameters, the length of the equivalent line can be scaled down to that of the short line section, which becomes a lossy equivalent model of a single unit section. Since the unit contains two line sections with length of $l/2$, the transmission matrix of the unit section can be expressed as follows:

$$A_{l/2}\begin{bmatrix} 1+YZ & Z \\ 2Y+ZY^2 & 1+YZ \end{bmatrix}A_{l/2} = \begin{bmatrix} \cosh\gamma' l & Z_0^{'}\sinh\gamma' l \\ Y_0^{'}\sinh\gamma' l & \cosh\gamma' l \end{bmatrix} \tag{3-7}$$

where $A_{l/2}$ is the transmission matrix of the $l/2$ line and the interconnect network is assumed as a symmetric π-network, parameters of which are described in Figure 3.3.

Finally, the short-line effects are peeled off from the lossy model in (3-7) to extract the frequency response data of the interconnect. From simulation or measurement in this step, we need additional data for the transmission line section with a length of $l/2$. Since γ' and $Z_0^{'}$ are already known values from (3-3) and (3-4), the unknown values in (3-7) are Y and Z of the interconnect model. They can be found from the following de-embedding process:

$$\begin{bmatrix} 1+YZ & Z \\ 2Y+ZY^2 & 1+YZ \end{bmatrix} = A_{l/2}^{-1}\begin{bmatrix} \cosh\gamma' l & Z_0^{'}\sinh\gamma' l \\ Y_0^{'}\sinh\gamma' l & \cosh\gamma' l \end{bmatrix}A_{l/2}^{-1} \tag{3-8}$$

Generally, the left side matrix of (3-8) can be any other transmission matrix such as T-network. In a typical case, in which the serial impedance is dominant in the interconnect model, we can simply find the value of Z from the (1, 2) element of the left side matrix in (3-8).

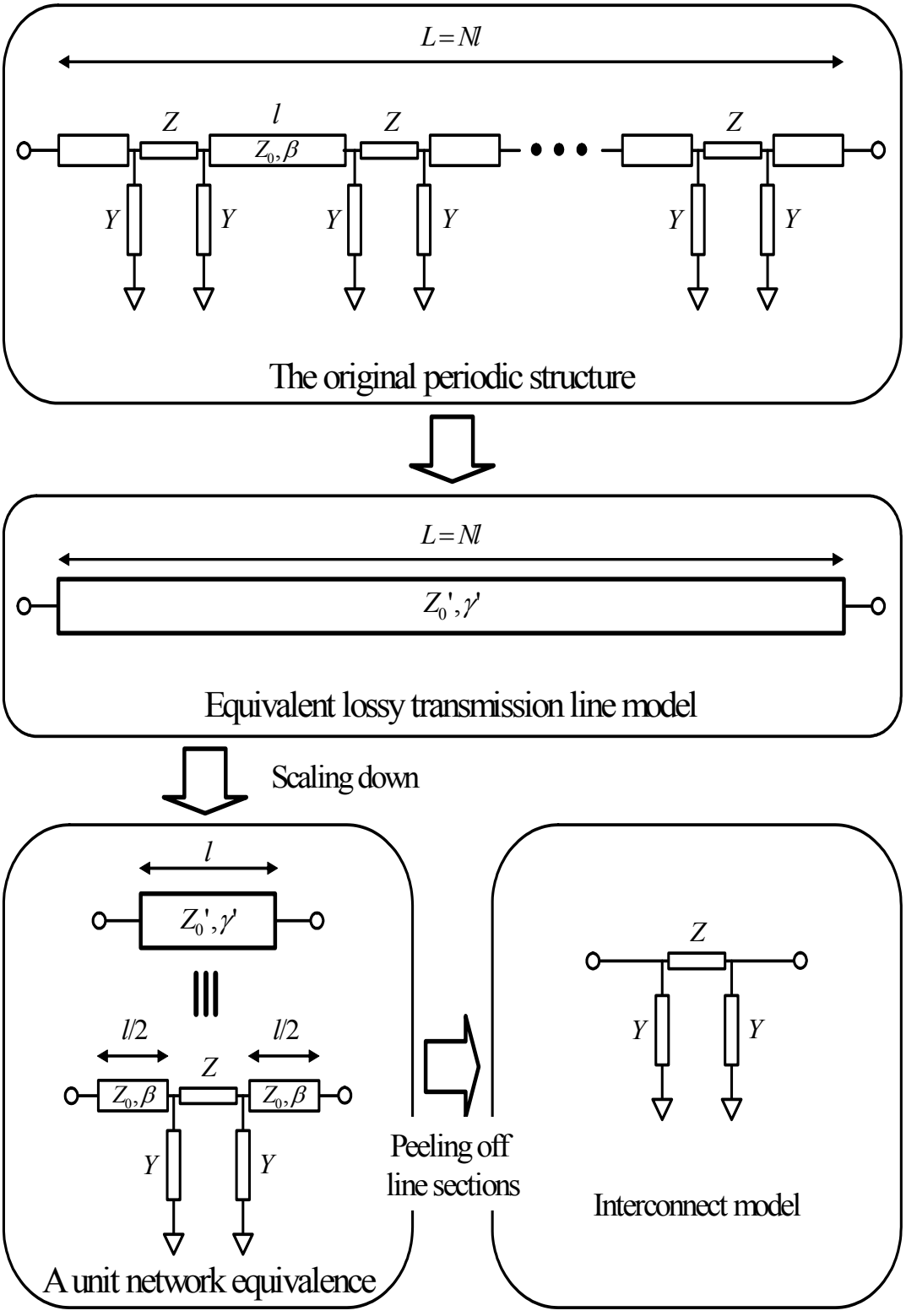


Figure 3.3. The procedure for characterizing vertical interconnect

3.3. Design of Test Vehicle

The proposed characterization was conducted at frequencies ranging from 1 to 40 GHz. To remove the effects of the parasitics in the feed structures, a Through-Reflect-Line (TRL) calibration was performed with a through, an open reflect, and six delay lines [51]. An Agilent PNA 8636B and Cascade Microtech 250um probe pitch GSG probes (APC-50) were used for the calibration with data points of 1601 and an IF bandwidth of 300 Hz. The TRL standards used in the calibration are shown in Table 3.1. The length of the feed structures were designed to minimize the mismatch and the higher-order mode coupling between the ports, which could produce unwanted variations during the error-corrected measurements [52]. As shown in Figure 3.4, the test vehicle (TV) also utilized a coplanar waveguide (CPW) structure for maintaining symmetry between the upper and lower transitions, enabling the entire structure to be de-embedded with a single half-length transmission line.

Table 3.1. TRL lines

TRL Lines	Through	Delay1	Delay2	Delay3	Delay4	Delay5	Delay6	Open Reflect
Length [mil]	382	1569	976	679	530	456	419	191

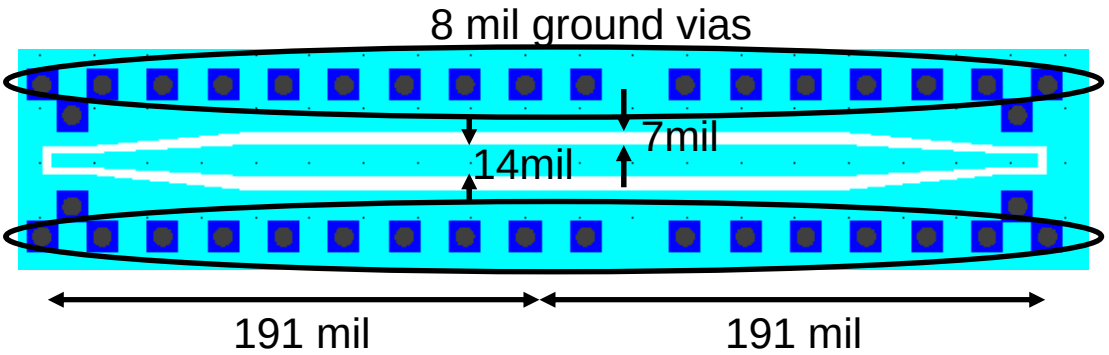
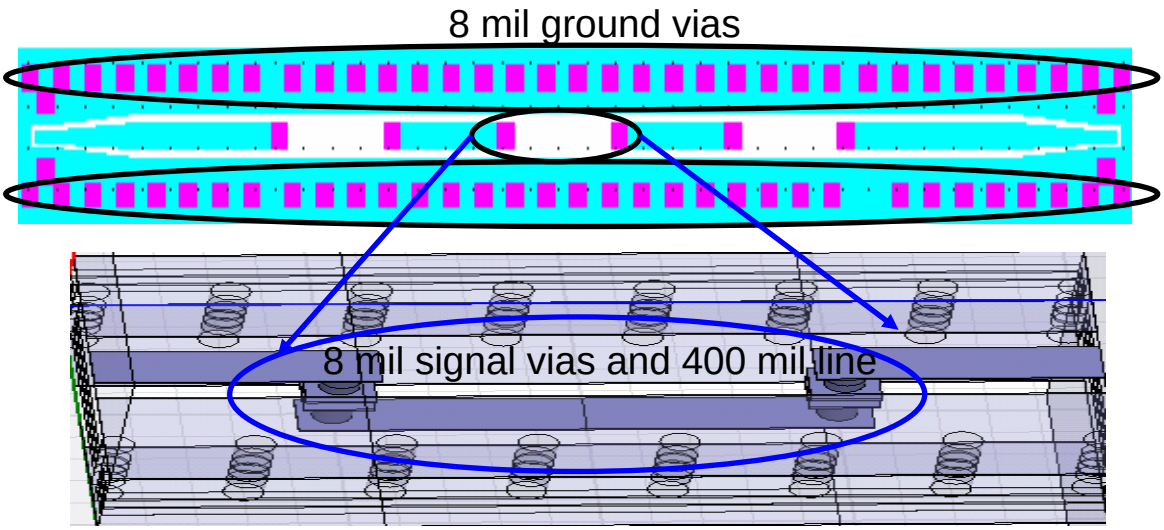
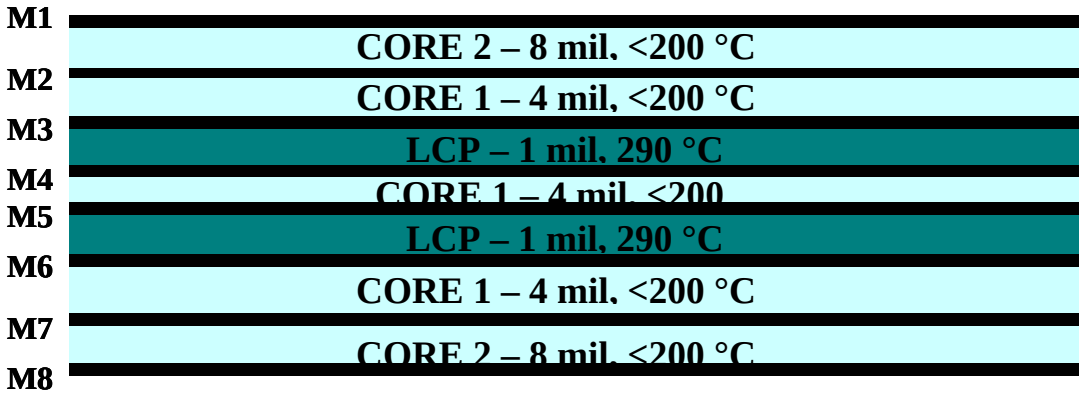


Figure 3.4. The layout of the through standard

To reduce unwanted variations of the residual parasitics and to average the processing variations, the arrays of the through-vias were designed for a single measurement. Each via was designed with a length of 30 mil and a diameter of 8 mil. The size of the square anti-pads was 14 mil x 14 mil. The proposed characterization method was verified by designing the three TVs with different lengths of the transmission lines, which connect the vias, as shown in Table 3.2. Each TV was fabricated on six different coupons in two separate 10” x 12” boards. In addition, half-length transmission lines were designed for extracting the via characteristics for each TV. Figure 3.5 depicts the layout of the designed TV 1 design.



(a)



(b)

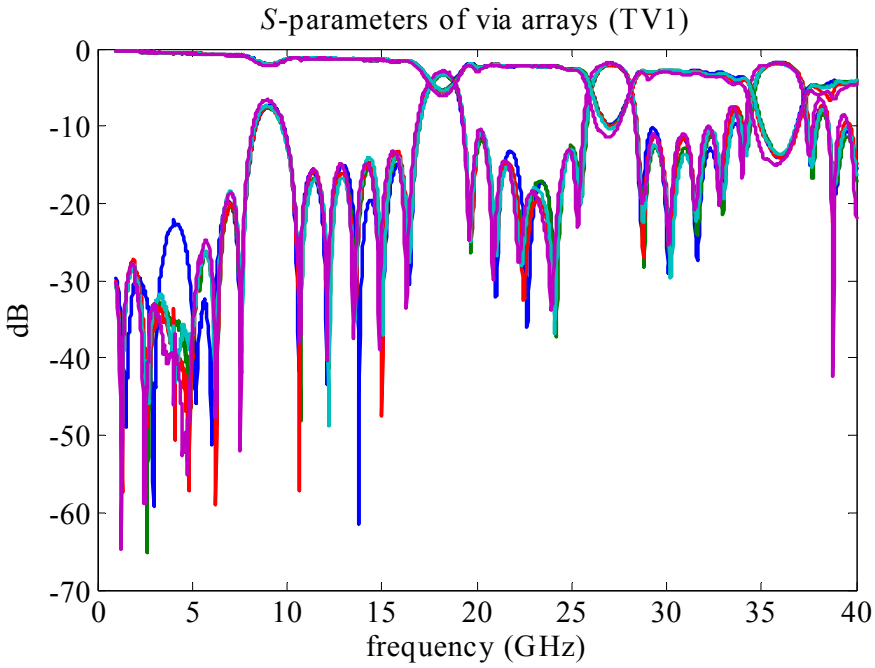
Figure 3.5. The designed TV 1: (a) layout and (b) Inhomogeneous LCP stack-up

Table 3.2. Specifications of the TVs

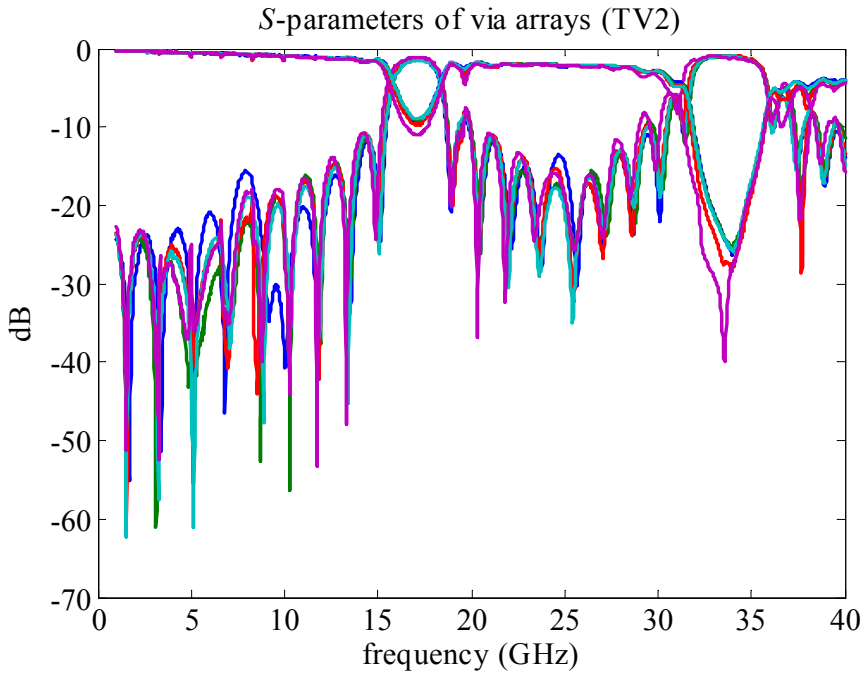
TV	1	2	3
Number of Vias	6	10	10
Transmission Line Length [mil]	400	200	100
Total Length [mil]	2400	2000	1000

3.4. Measured Results

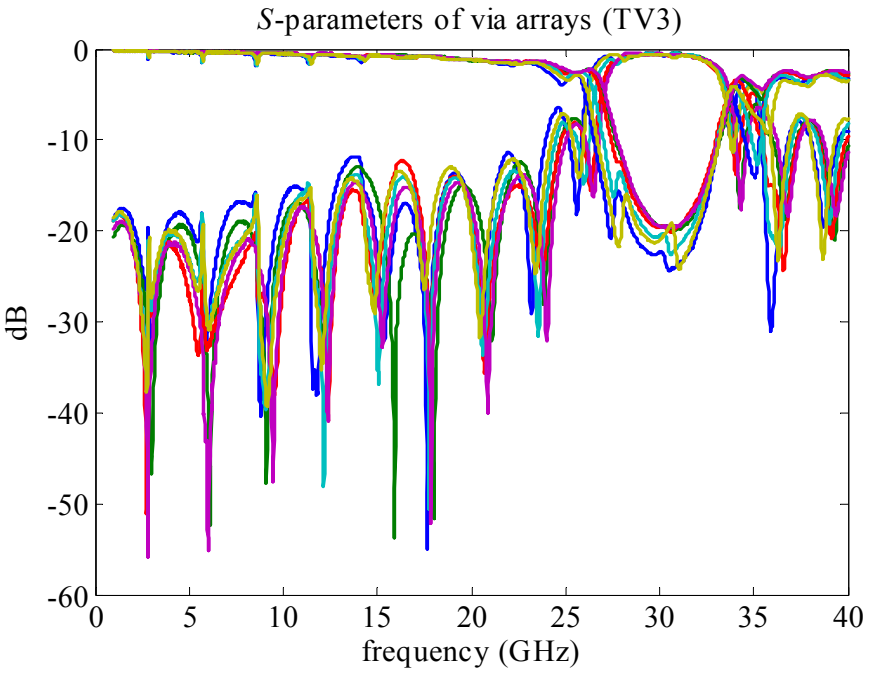
Figure 3.6 shows the S parameters of each TV. Different lengths of the entire structures resulted in different resonant frequencies.



(a)



(b)



(c)

Figure 3.6. Measured S parameters of (a) TV1, (b) TV 2, and (c) TV3

Figure 3.7 shows the methods to choose the propagation constants of TV 1 as an example. The closest propagation constant of the entire structure to that of the single section was selected. In Figure 3.7, it can be confirmed that the phase velocity of the entire structure is slightly slower than that of a single section because series inductance and parallel capacitance slow down the signal propagation.

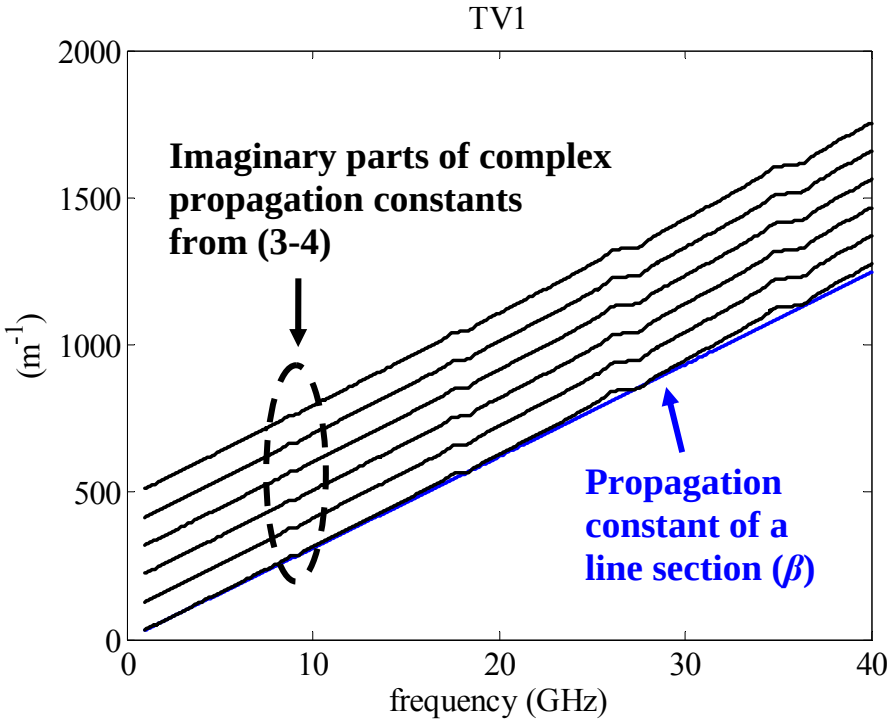
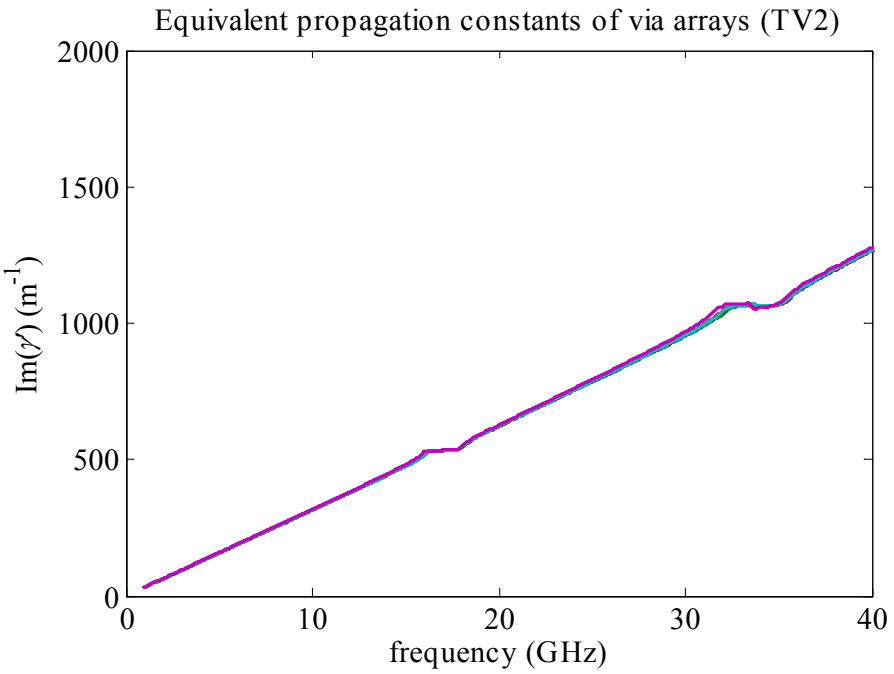
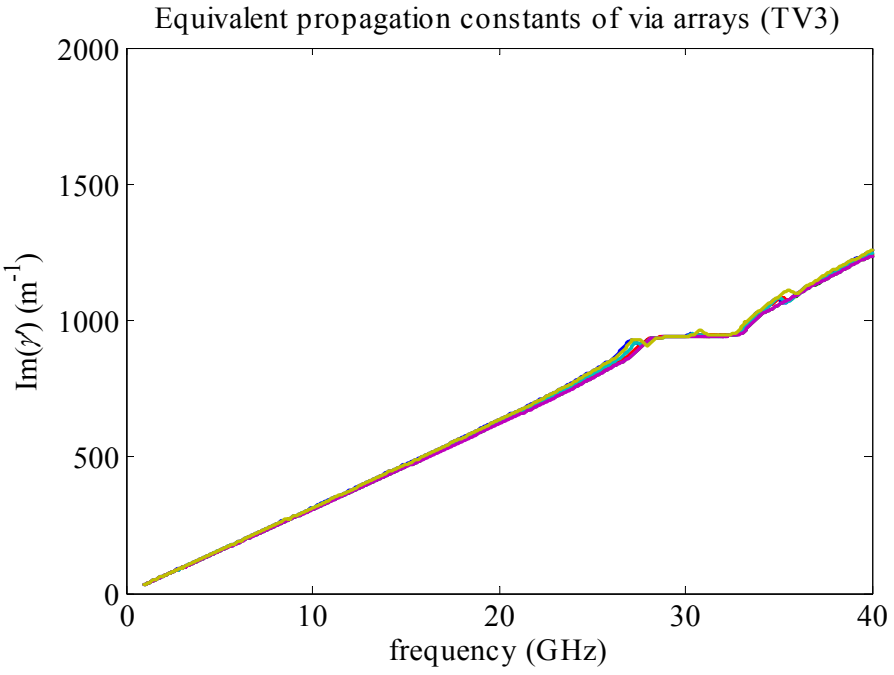


Figure 3.7. Physical propagation constant of TV1 among solutions

To verify the proposed methods, the imaginary part of the propagation constants of the TV's are compared. The results of the comparison show constant values among TV's with different lengths, shown in Figures 3.8. The flat regions in Figure 3.8 are caused by the resonances because of the overall lengths of the structures, as explained above.



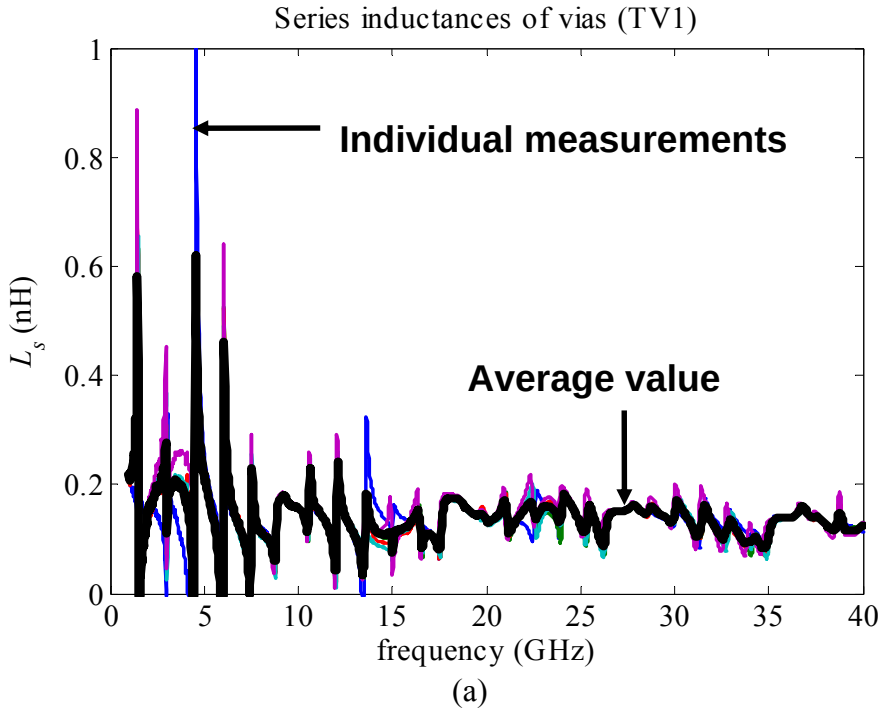
(a)



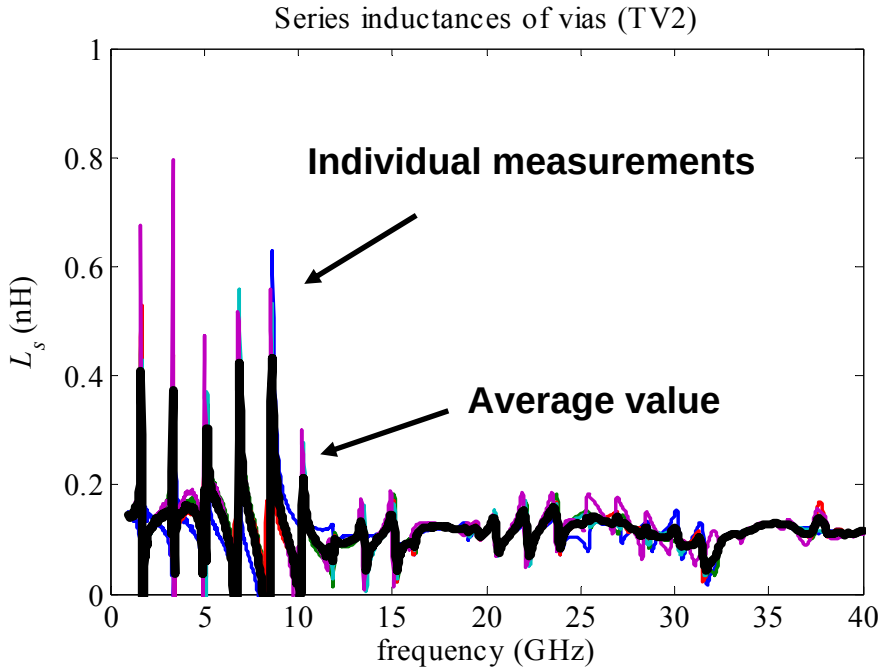
(b)

Figure 3.8. Extracted propagation constants of TVs 2 and 3 from the measurements

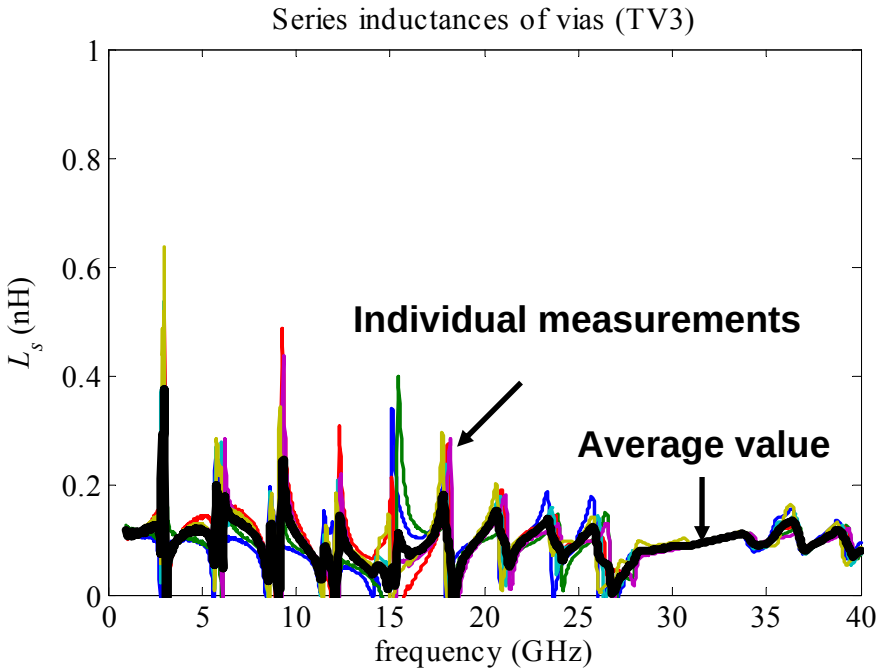
The proposed characterization method provides the extracted values of series inductance (Ls) and parallel capacitances (Cp) in the equivalent circuit model shown in Figures 3.9 and 3.10, respectively. From 20 to 40 GHz, the average inductance ranges from 0.106 to 0.121 nH, and the capacitances from 0.056 to 0.076 pF. The various ringing in the values are caused by the resonance of the entire structure, which differ for each TV. To reduce this effect at low frequency, more number of interconnects can be used for a longer overall size, which is resonating at lower frequency, but it is limited by overall size, which should fit into the measurement set-up. To move this ringing into very high frequency, very short transmission line, connecting the vertical interconnects may be used. However, this may lead to mutual coupling between interconnects. Each TV, which had six structures from different locations on several boards, provided consistent values. Relatively high values of the parallel capacitances are obtained because the via pads were placed on every layer for the connections, as shown in Figure 3.5.



(a)

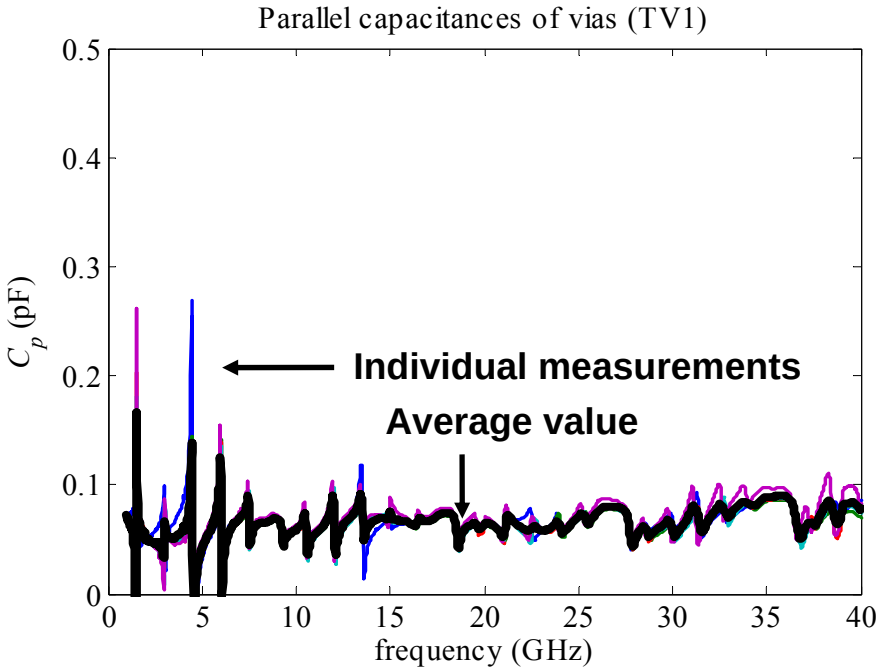


(b)

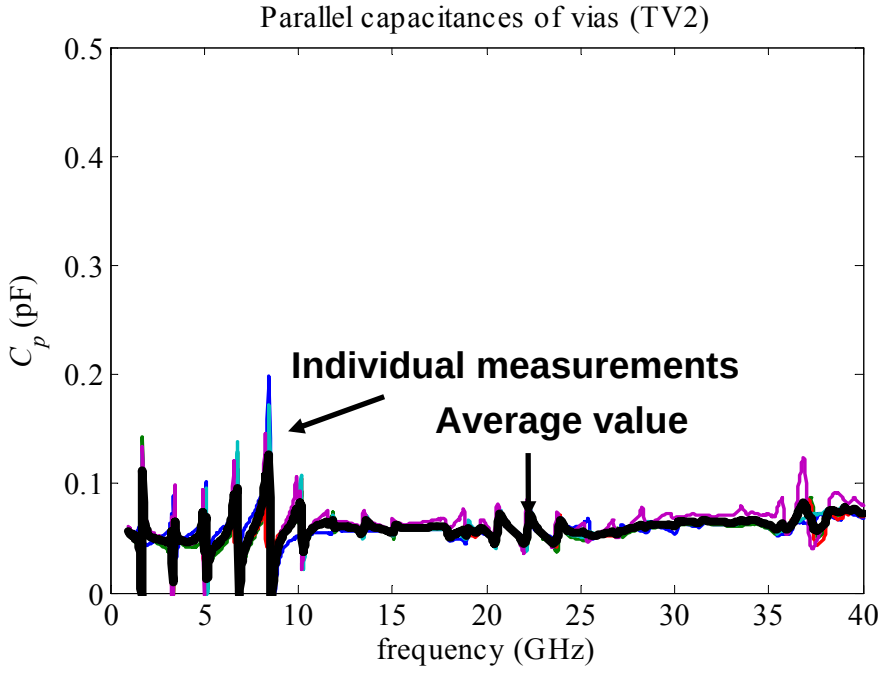


(c)

Figure 3.9. Extracted series inductances (Ls) of (a) TV1, (b) TV 2, and (c) TV 3 from the measurements


Parallel capacitances of vias (TV1)
0.5
0.4
0.3
0.2
0.1
0
C_p (pF)
Individual measurements
Average value
0
5
10
15
20
25
30
35
40
frequency (GHz)

(a)


Parallel capacitances of vias (TV2)
0.5
0.4
0.3
0.2
0.1
0
C_p (pF)
Individual measurements
Average value
0
5
10
15
20
25
30
35
40
frequency (GHz)

(b)

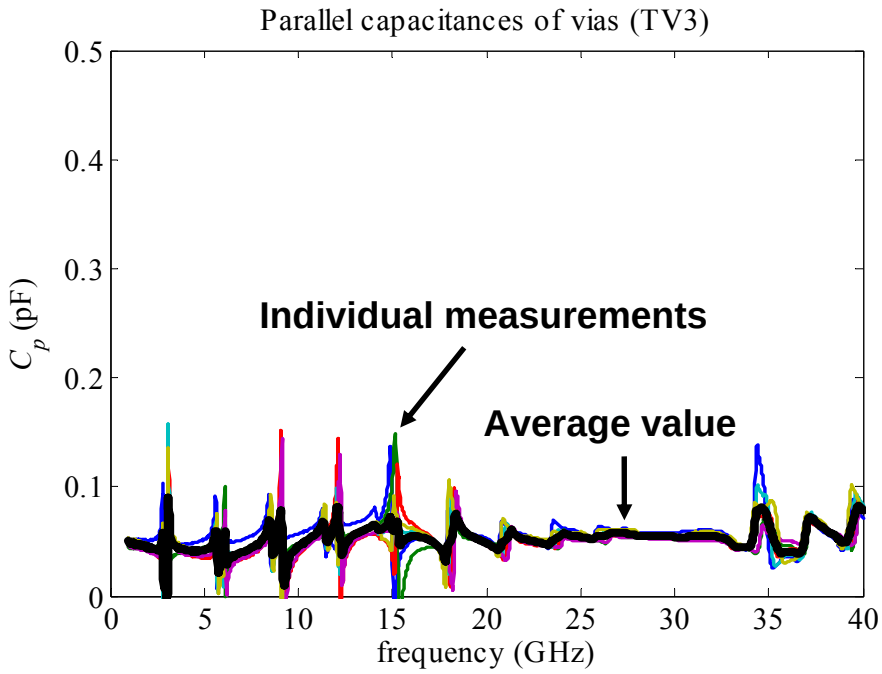


Figure 3.10. Extracted parallel capacitances (Cp) of (a) TV1, (b) TV 2, and (c) TV 3 from the measurements

3.5. Model-to-Hardware Correlation

The extracted S parameters of the entire structure, propagation constants, S parameters of the single section, Ls, and Cp of TV3 were compared with those of the models, which were simulated using Ansoft HFSS [53], a 3D full-wave solver. Figure 3.11 shows the S parameters of the entire structure, and Figure 3.12 shows the propagation constants of the structures. Finally, Figure 3.13 and 3.14 shows the model-to-hardware correlation of the extracted Ls and Cp, which resulted in excellent correlation. From 20 to 40 GHz, more consistent values were extracted because the low frequency ringing does not have significant effects at these frequencies, as shown in Figure 3.13 (b) and 3.14 (b). The dark lines are the results by HFSS [53], compared to six measurement data of TV 3.

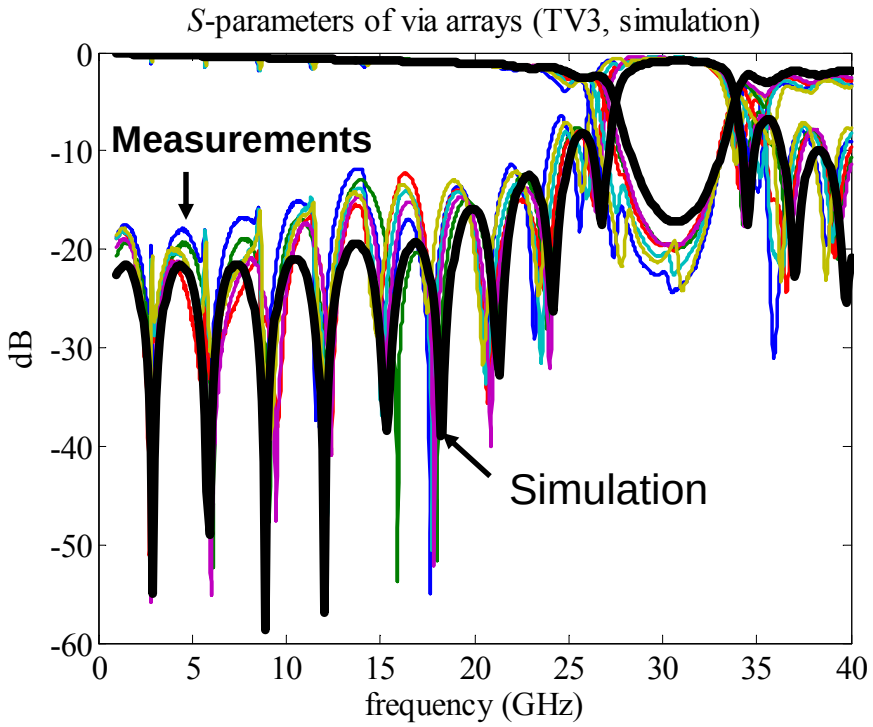


Figure 3.11. Model-to-hardware correlation of the S parameters for the entire structure

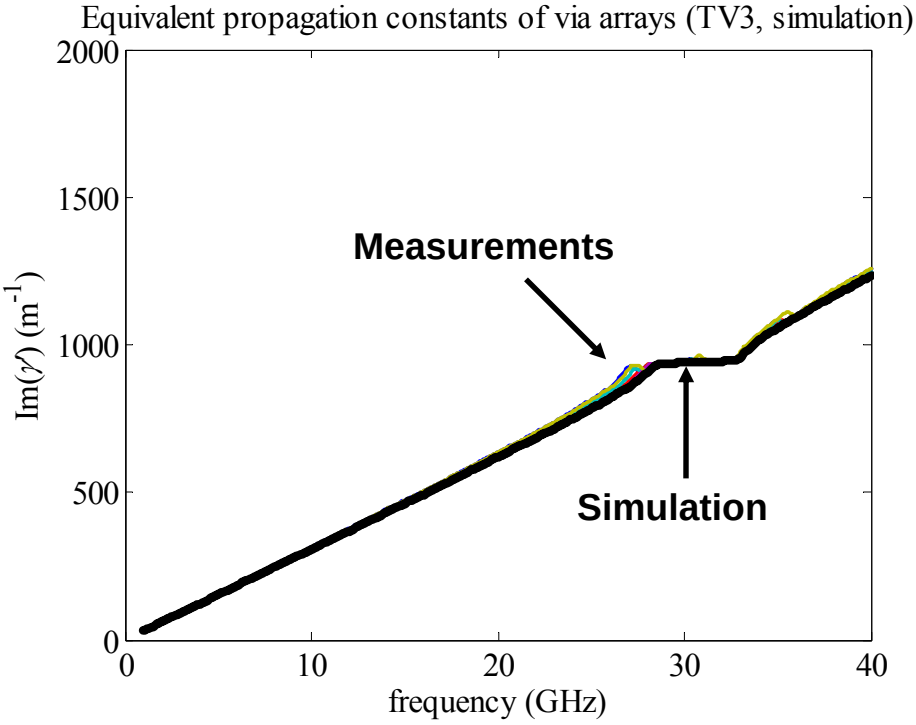
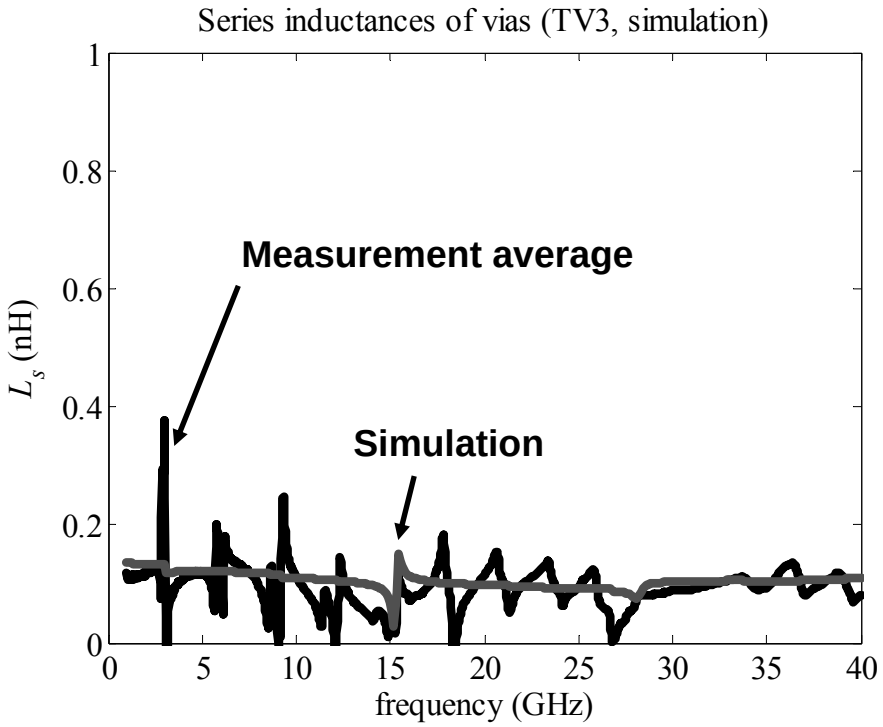
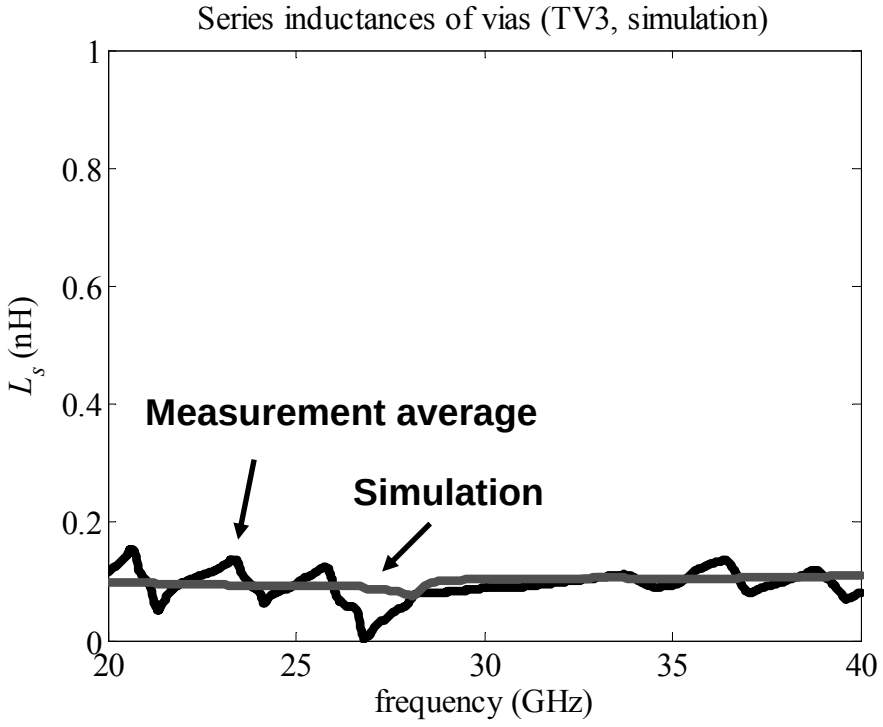


Figure 3.12. Model-to-hardware correlation of propagation constants

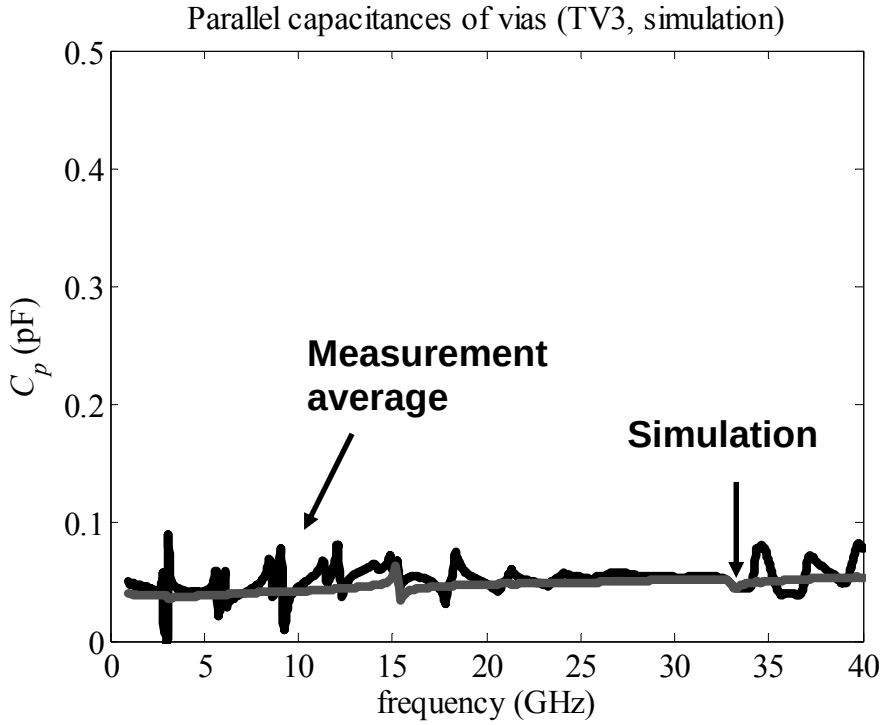


(a)

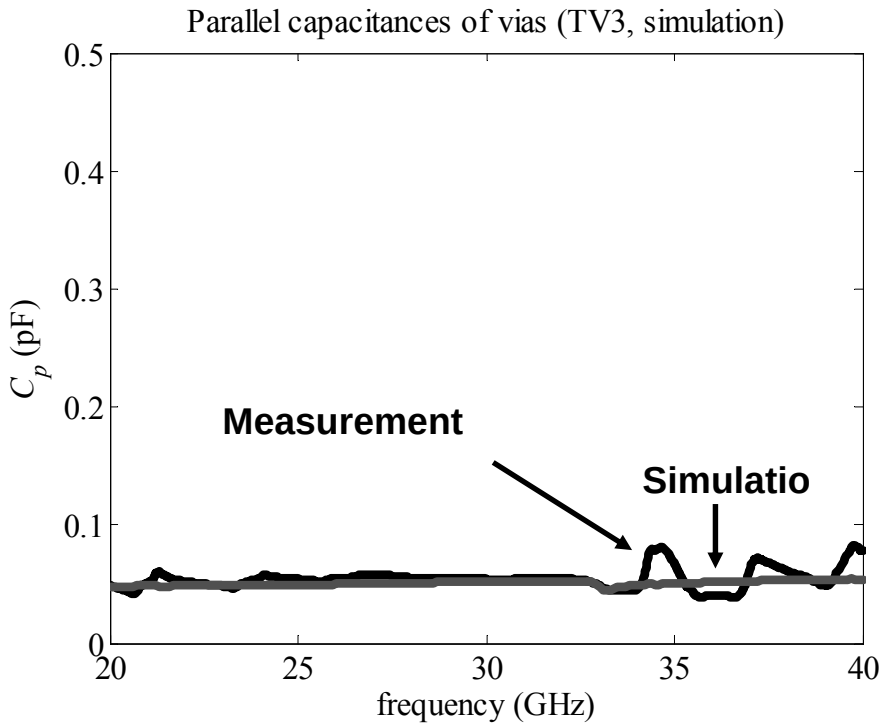


(b)

Figure 3.13. Model-to-hardware correlation of Ls (a) 1-40 GHz and (b) 20-40 GHz



(a)



(b)

Figure 3.14. Model-to-hardware correlation of Cp (a) 1-40 GHz and (b) 20-40GHz

3.6. Via Model

Figure 3.15 shows an equivalent model of via, which consists of series inductance (Ls), and parallel capacitances (Cp). Ls and Cp values from 20 to 40 GHz are shown in Table 3.3. This higher frequency range did not have ringing effect because of the overall structures as discussed in Section 3.4. Since each test vehicle has different resonances, some variations at specific frequencies have been observed. However, overall response is consistent as shown in the previous Figures. The extracted values are plotted in Figure 3.16 and 3.17.

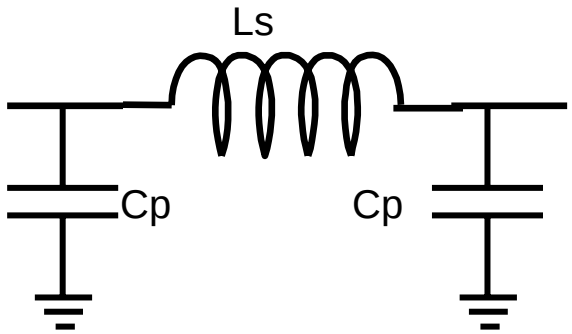


Figure 3.15. Equivalent circuit model of via

Table 3.3. Extracted values of the via

	GHz	nH/pF	TV1	TV2	TV3	Overall
Frequency (GHz)	20	Ls	0.135	0.115	0.115	0.121
		Cp	0.063	0.056	0.049	0.056
	25	Ls	0.123	0.129	0.096	0.115
		Cp	0.071	0.055	0.054	0.060
	30	Ls	0.146	0.122	0.089	0.117
		Cp	0.059	0.061	0.054	0.058
	35	Ls	0.106	0.128	0.094	0.108
		Cp	0.089	0.062	0.066	0.072
	40	Ls	0.124	0.116	0.082	0.106
		Cp	0.078	0.072	0.078	0.076

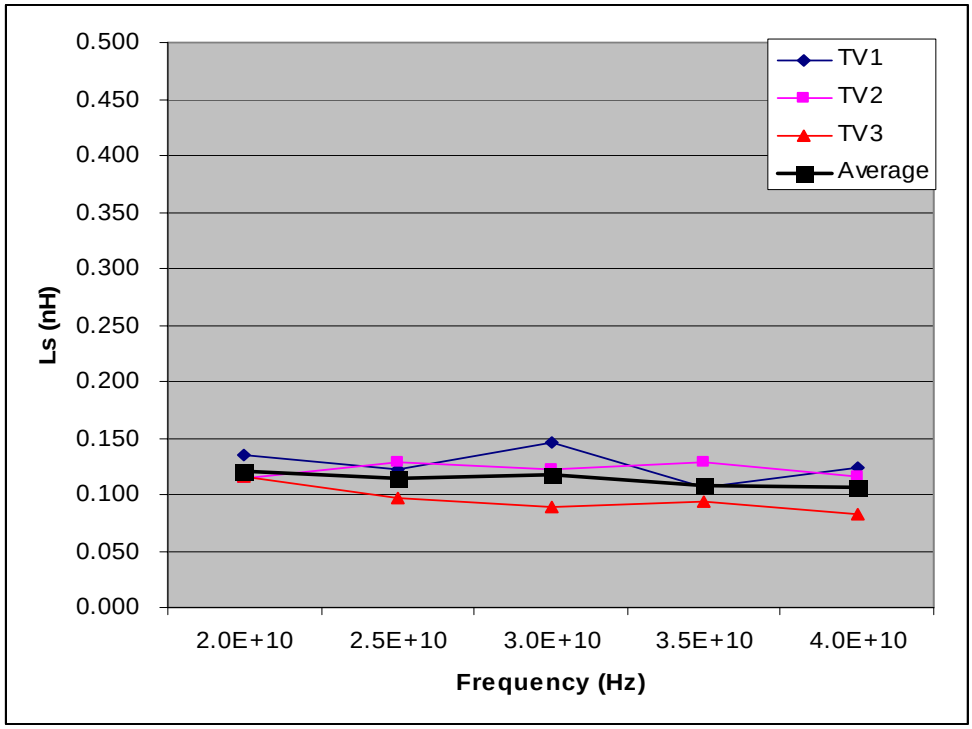


Figure 3.16. Extracted series inductance (Ls) values for each TV and average value

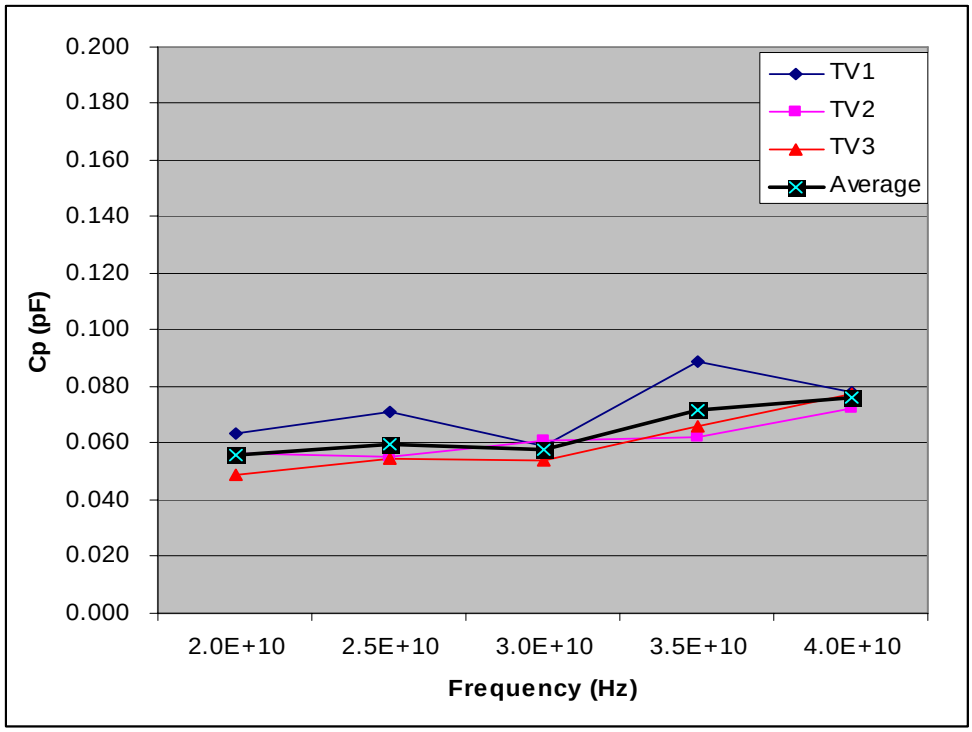


Figure 3.17. Extracted parallel capacitance (Cp) values for each TV and average value

3.6. Summary

This chapter presented a two-port characterization method based on measurements of multiple arrays of vias. The method overcomes the drawbacks of the one-port and other two-port characterizations. A single measurement decreases the residual inductances and contact resistances, and the arrays of the vias average the process variations of the vias.

Three TV's were measured using the TRL calibration, which ensures the proper de-embedding of the feeding structures. The S parameters along with the propagation constants of the entire structures have been shown. Finally, the series inductances and parallel capacitors were extracted. The characterized values, compared among the different TV's and coupons, showed consistent values.

A comparison of the extracted inductances and capacitances, S parameters, and propagation constants with those of the simulated results by Ansoft HFSS [53], a 3D full-wave solver, provided the model-to-hardware correlations. The resulting correlations show that this method can be readily applied to other vertical interconnect structures besides via structures such as G-helix [49].

CHAPTER 4

DESIGN AND CHARACTERIZATION OF HIGH-Q EMBEDDED PASSIVES IN INHOMOGENEOUS MULTI-LAYER LCP SUBSTRATES

4.1 Introduction

In modern communication systems, high-Q passive components play a critical role in system performance, such as phase noise and noise figure. The Q of inductors directly affects these system performances. The embedded passives can provide very high-Q passives for the critical components such as inductor in tank circuits in VCO and gate inductor in source-degenerated LNA, leading to high performance circuits. In addition, if inductor is realized on silicon, it can occupy most of the die real estate (up to 70 to 80 %). Therefore, SOP can provide compact, low-profile solution without degrading system performance.

As mentioned in previous chapters, unlike LTCC, LCP technology cannot only be used as integrated passive devices (IPD) or modules, but also be used as the final substrate for systems. Due to the increasing demand for higher integration, both RF front-end integration as well as RF–digital integration are essential. In Figure 1-1, the front-end module, i.e., the components inside the box, can be integrated as modules, which can then be incorporated with the rest of the RF and base-band modules. Therefore, the vertical integration by 3D design with multi-layer substrates can be a good solution for RF-digital integration. The thickness of a system in compact-size portable

devices can be a major restriction as the integration trend continues. In addition, the overall integration cost is a key consideration. The 3D multi-layer LCP (M-LCP)-based integration can provide multi-functional, low-profile, low-cost, and high-performance systems.

In [41], 12 inductors showing the scalability of Qs using the M-LCP process at two different locations in one board were characterized. In this chapter, more comprehensive characterization with a de-embedding technique has been conducted. 3D capacitors have been designed and characterized. Therefore, the 3D integration and characterization of high-Q passives have been demonstrated in this chapter. The main contributions of this chapter are as follows**:**

1) Characterization of 76 high-Q inductors and 16 multi-layer capacitors using the M-LCP-based process with model-to-hardware correlation

2) Demonstration of the scalability of the Qs in 3D integration

3) Validation for two different locations in three large panels to show repeatability

4) Model-to-measurement correlation using a two-step de-embedding technique

4.2 High-Q Embedded Inductor Characterization in Test Vehicle 1

Figure 4.1 shows the balanced configuration, which was characterized in Chapter 2, and Figure 4.2 shows the layout and photograph of the designed inductor. TV 1 was fabricated on a 12" x 9" LCP panel. Figure 4.3 shows the photograph of Test Vehicle 1 (TV1) in the balanced configuration shown in Figure 4.1. It has two different Test Sets: one in the center and the other at the edge. Twelve different rectangular spiral inductors were characterized in two different locations in TV 1. Figure 4.2 also shows the layout

and photograph of the designed inductor with a GSG pad. The metal width (W) and line space (S) were set at 3 mils. The inductors were designed for 3D integration and high-Q using different layers. To show the scalability of Qs, eight similar-size inductors were designed in two different layers: one in the top-most layer (M1), and the other in the top LCP layer (M3) (which is embedded in the LCP substrate, as shown in Figure 4.1. Inductors were designed using an EM simulator, SONNET [46], and verified using measurement results. The measurements were taken using a GSG 500 um Air Coplanar™ probe (ACP) with a vector network analyzer.

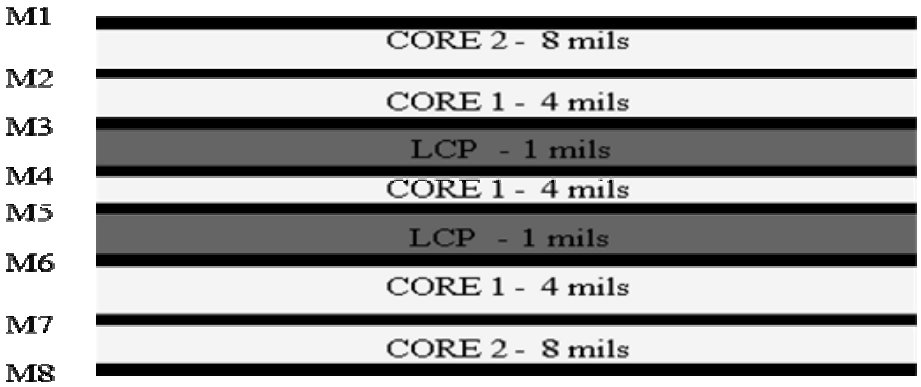


Figure 4.1. Cross-section of the balanced-LCP substrate

The effective inductance and the quality factor (Q) of the inductors were calculated from the measured S parameters. First, the Y_{11} of the inductor was extracted from the measured $S_{11,}$ and then the effective inductance (L_{eff}) and Q were calculated as equation (4-1) and (4-2) using SONNET.

$$L_{eff} = \frac{imaginary(1/Y_{11})}{2\pi f} \tag{4-1}$$

$$Q = \frac{imaginary(1/Y_{11})}{real(1/Y_{11})} \tag{4-2}$$

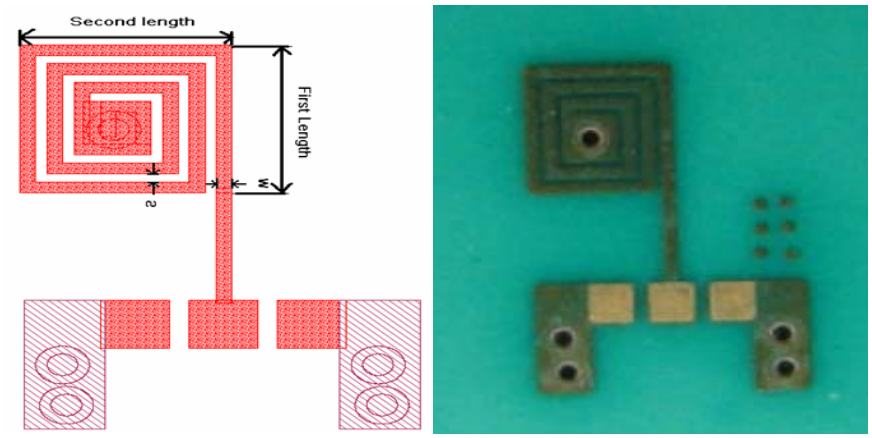


Figure 4.2. Layout and photograph of the designed inductor

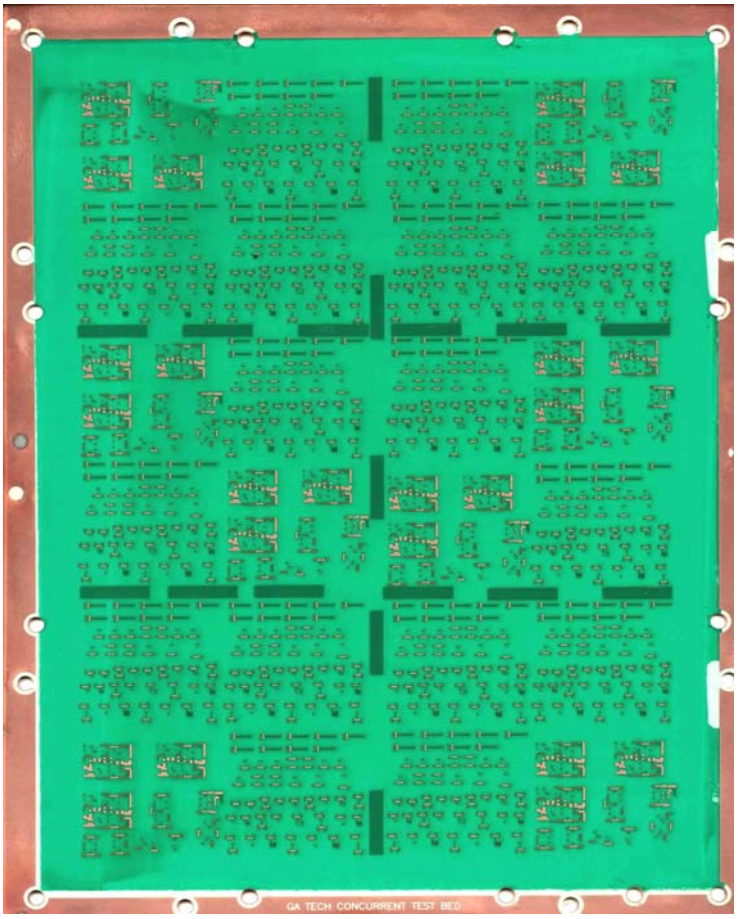
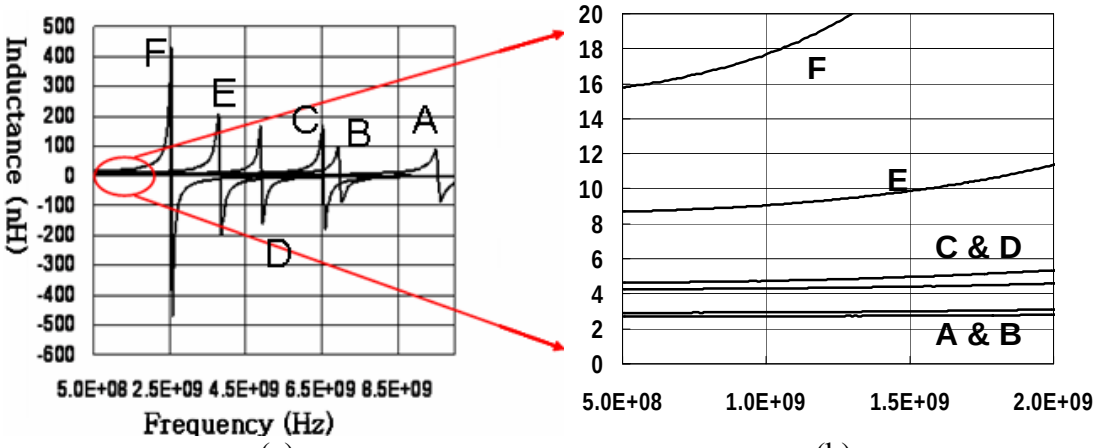


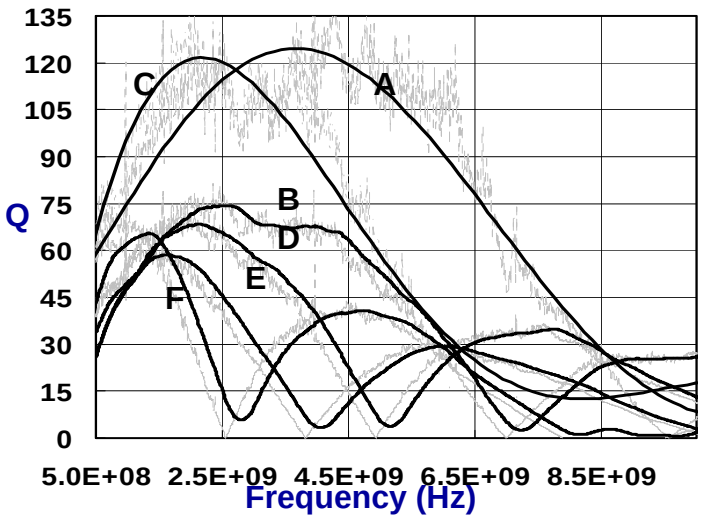
Figure 4.3. Photograph of the TV1 (12” x 9”)

Figure 4.4 (a) shows inductance profiles, which also show the self-resonant frequencies (SRFs) of the inductors. Figure 4.4 (b) shows inductances from Set 2: A (2.7 nH @ 1 GHz), B (3.0 nH), C (4.3 nH), D (4.7 nH), E (9.1 nH), and F (17.7 nH). All inductors have 3 mil line width of rectangular spirals with varying length. Inductors A (M1) and B (M3) and inductors C (M1) and D (M3) are the same size, but they are in different layers. Inductors E and F are in the top-most layer (M1).

Figure 4.4(c) shows the averaged measured Q factors up to 10 GHz. The Q of the Inductor A is 126 at 3.68 GHz, while Q of the inductor B is 75 at 2.52 GHz. Compared to the Qs of FR-4 and LTCC (100 with 1.2 nH at 1.9 GHz in [35]), the results of the inductor Q in the LCP show much better performance.



(a) (b)



(c)

Figure 4.4. Measured results of Set 1 in TV1: (a) inductance profile, (b) sampled inductance, and (c) quality factor

The results also show the scalability of inductor Qs using 3D integration. While the Q of Inductor B (75) is also high enough for general applications, this higher-Q (126) of Inductor A can be used for few critical components in various applications. High-Q passives in the critical components reduce the phase noise of VCOs [9], the noise of LNAs [42], and the insertion loss of band-pass filters [54]. For example, only one inductor in the VCO was critical to achieve low-phase noise in [43]. Therefore, in an RF front-end module, only few critical components requiring high Q can be optimized in 3D integration, and other components can be integrated elsewhere with lower Q. The optimization of 3D integration in multi-layer LCP substrates provides high performance with a compact size and low profile.

The SRF increases from 2.56 GHz (A) to 9.57 GHz (F) as inductance increases. The inductances of inductors in M3 (B and D) are reduced from those of inductors in M1 (A and C) because the lower distance to the ground increases parasitic capacitances, resulting in reduction of inductance at a given frequency. These inductor

characterizations show promising results for high-Q inductors allowing scalability; from Q of 126 (2.75nH) to 58 (9.3nH).

All inductors were located in two different locations on a 9" x 12" balanced double LCP panel, as shown in Figure 4.3. For preliminary verification of the large-panel process over different locations on a single board, two sets of inductors were measured in a balanced LCP board, as shown in Figure 4.1. The variation of the performance was minimal and the summary of the characterization results are shown in Table 4.1.

Table 4.1. Summary of inductors at two different locations in TV1

	# of Turn	Size (mils)	Metal Layer	Inductance (nH)		SRF (GHz)		Q @ GHz	
				Set 1	Set 2	Set 1	Set 2	Set 1	Set 2
A	1	54X30	M1	2.74	2.74	9.57	9.52	126 @ 3.68	122@3.6
B	1	54X30	M3	2.97	2.92	6.99	6.91	75 @ 2.52	74@2.33
C	1	75X51	M1	4.32	4.32	6.57	6.57	122 @ 2.19	119@2.18
D	1	75X51	M3	4.74	4.72	4.93	4.88	69 @ 2.12	67@2.01
E	2	45X45	M1	9.05	9.33	3.82	3.81	58 @ 1.7	65@1.5
F	3.5	60X61	M1	17.7	17.8	2.56	2.55	65 @ 1.38	65@1.05

4.3. High-Q Embedded Inductor Characterization in TVs 2 and 3

For more comprehensive characterization, 64 inductors were characterized in two large panel test vehicles, as shown in Figure 4.5. To achieve higher Qs in these test vehicles, the ground layers below the inductor were removed. The absence of ground resulted in low parasitic capacitance through the ground layers, leading to higher Qs in the new test vehicle. Eight different inductors were designed and then located on two different layers, M1 and M3, in Figure 4.1.

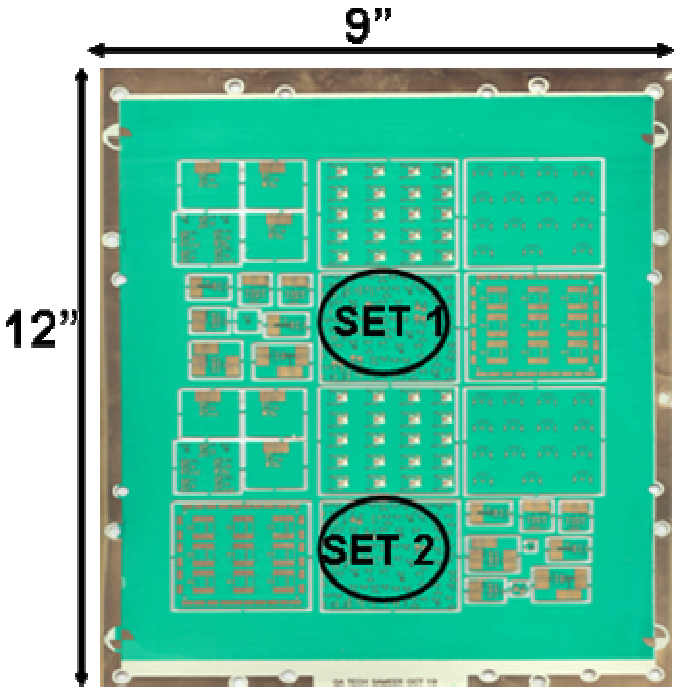


Figure 4.5. Photograph of TV 2 and 3

Table 4.2 summarizes the design parameters of these characterized inductors. The metal width and space were 3 mils. Figure 4.6 shows the X-ray picture of Inductor 3.

Table 4.2. Physical dimensions and locations of the inductors in TV2 and TV3

	Turn	Size (mil^2)	Layer
1	1	22 x 30	M1
1_Top	1	22 x 30	M3
2	1	12 x 39	M1
2_Top	1	12 x 39	M3
3	1	30 x 54	M1
3_Top	1	30 x 54	M3
4	2	45 x 45	M1
4_Top	2	45 x 45	M3
5	1	51 x 75	M1
5_Top	1	51 x 75	M3
6	2.5	55 x 55	M1
6_Top	2.5	55 x 55	M3
7	3	61 x 60	M1
7_Top	3	61 x 60	M3
8	3.5	65 x 65	M1
8_Top	3.5	65 x 65	M3

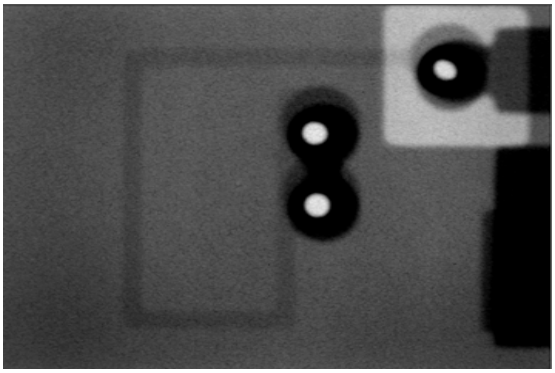
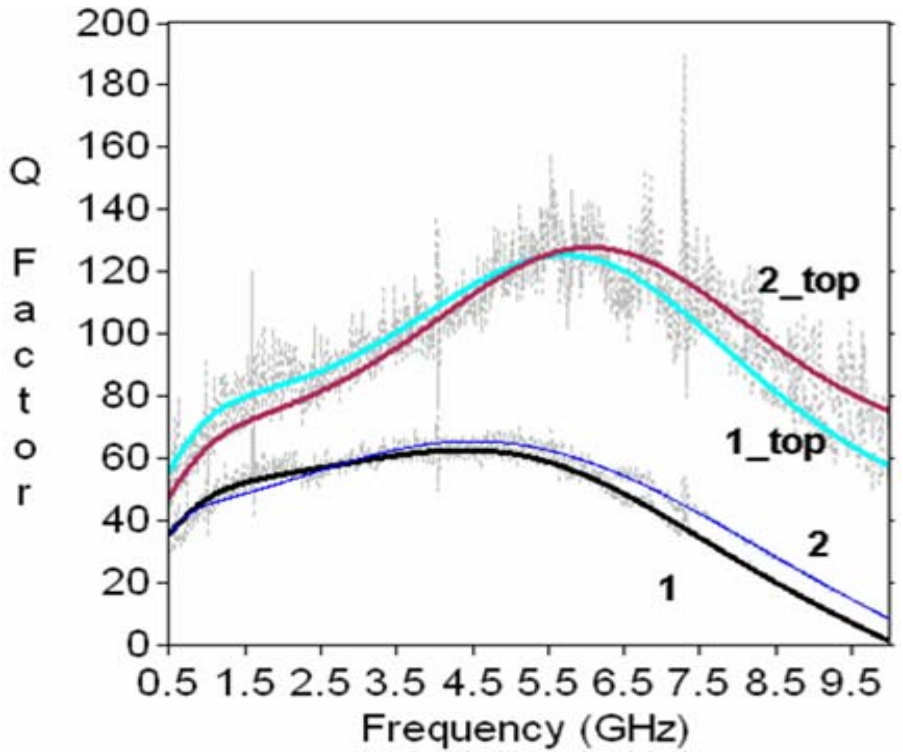
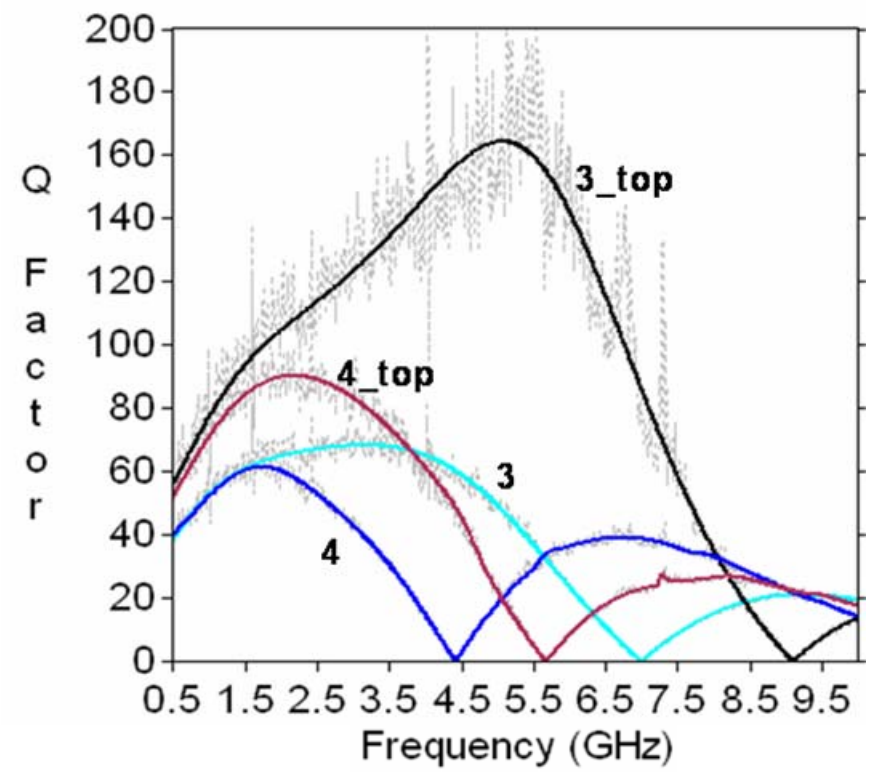


Figure 4.6. X-ray of Inductor 3 in TV2

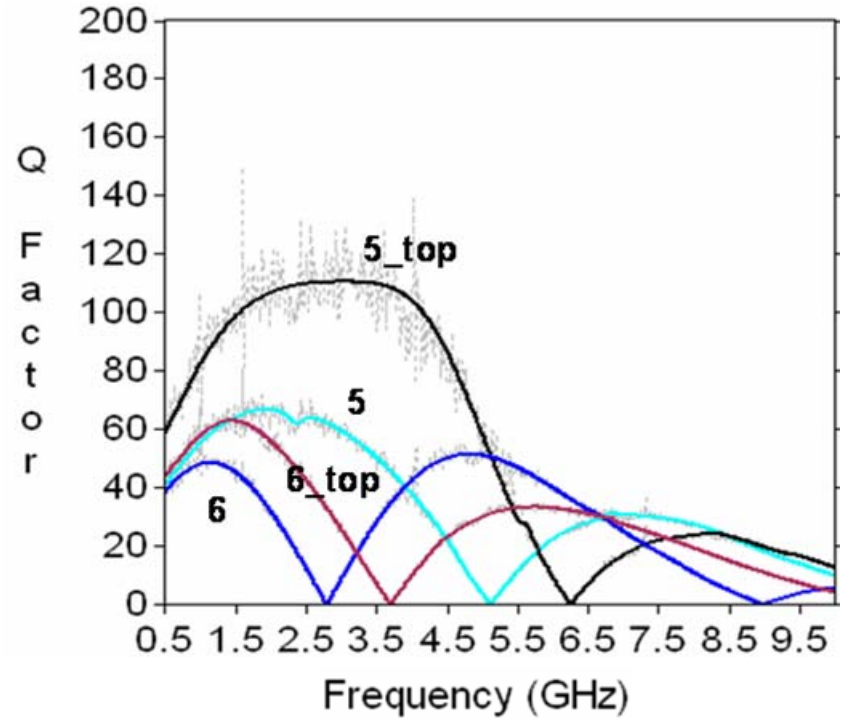
Figure 4.7 shows the averaged Q profiles of 16 inductors at Location 1 from TV 3. The inductance ranges from 1.45 nH to 23.11 nH. While Inductors 1 and 2 have similar inductances, Inductor 2 has been designed to have a higher SRF using different size. The highest averaged Q of 164 has been achieved for the 2.53 nH inductor on M1 from the edge location in test vehicle 3. Compared to TV 1, this Q shows improvement of over 30% from 126 for the 2.75 nH inductor. Such an increase of Q results from lower parasitic capacitance by the removal of the ground layer under the inductor. Similar to TV 1, TV 2 and 3 also show the scalability of Qs using different layers. For example, Inductor 5 has lower Q (~60) than Q (110) of Inductor 5_top because inductor 5 has a larger parasitic capacitance because it is closer to the ground layer. This parasitic capacitance also has an effect on lowering the SRF of Inductor 5. Through-hole interconnections used in the embedded inductors (Inductor 1 to 8) contributed to a slight increase in inductance compared to the top-layer inductors (Inductor 1_top to Inductor 8_top). Table 4.3 shows the measured results of the selected inductors at four locations from test vehicles 2 and 3.


Q Factor
200
180
160
140
120
100
80
60
40
20
0
0.5 1.5 2.5 3.5 4.5 5.5 6.5 7.5 8.5 9.5
Frequency (GHz)
2_top
1_top
2
1

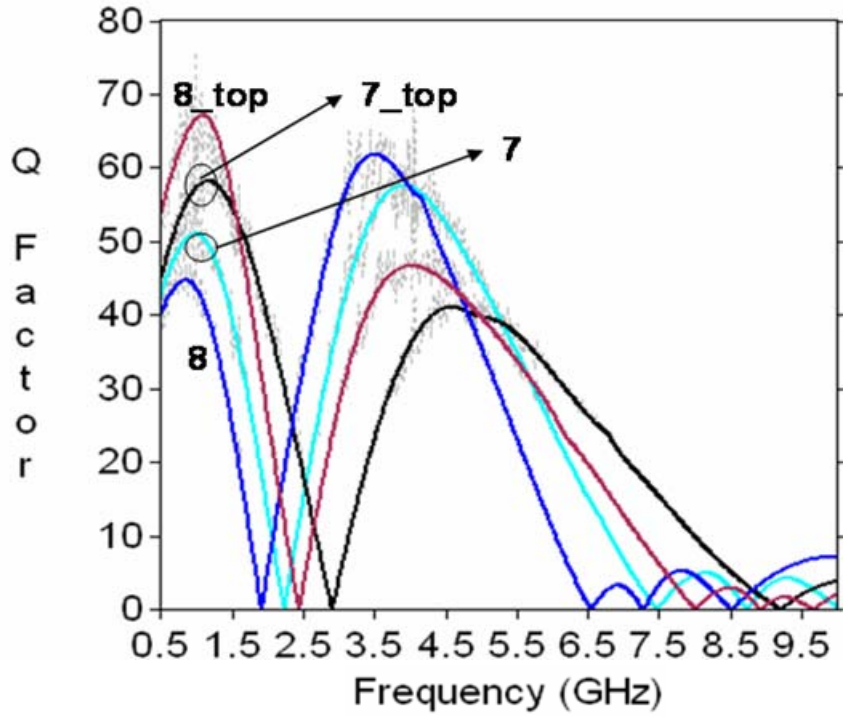
(a)


Q Factor
200
180
160
140
120
100
80
60
40
20
0
0.5 1.5 2.5 3.5 4.5 5.5 6.5 7.5 8.5 9.5
Frequency (GHz)
3_top
4_top
3
4

(b)



(c)



(d)

Figure 4.7. Measurement results of Qs of the designed inductors: (a) Inductor 1 and 2, (b) Inductor 3 and 4, (c) Inductor 5 and 6, and (d) Inductor 7 and 8

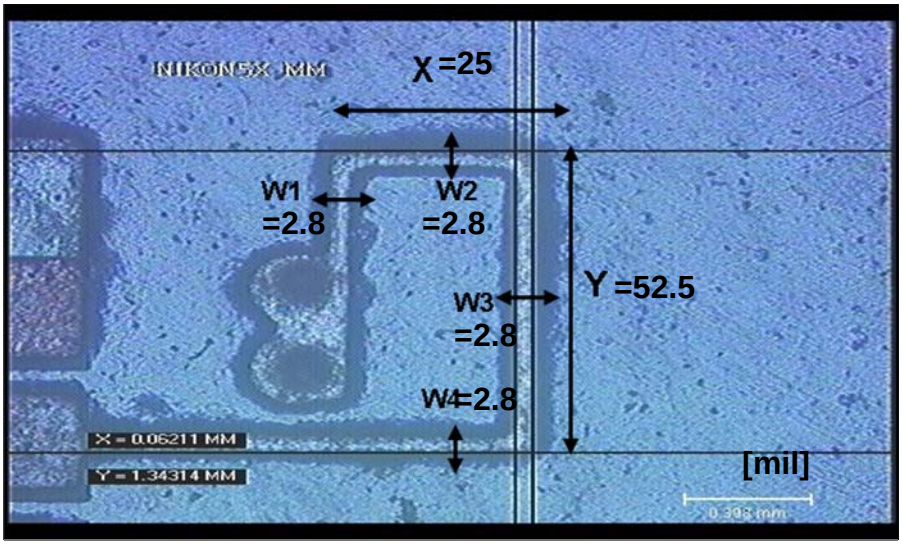
As Table 4.3 shows, different locations and different TVs create only a small variation in inductance and SRF.

Table 4.3. Measurement results of the selected inductors in TV2 and TV3

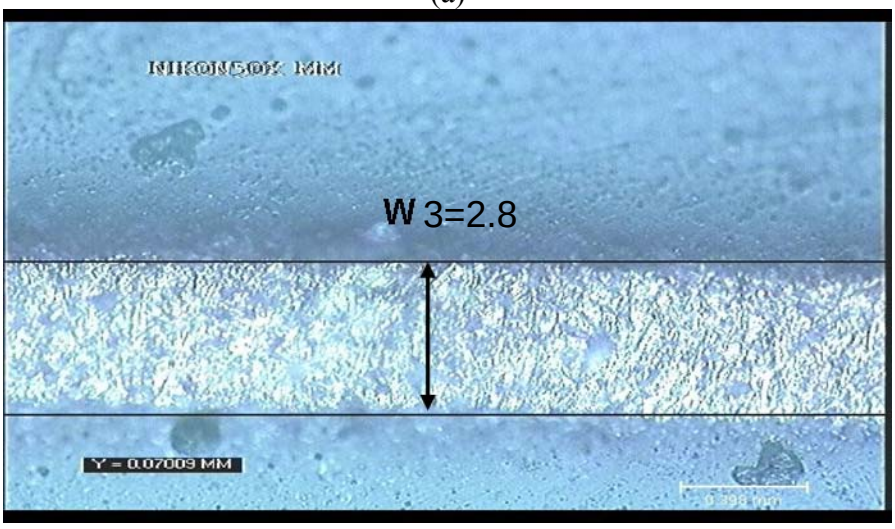
	Inductance (nH)				Q @ GHz				SRF (GHz)			
	TV2 Set1	TV2 Set2	TV3 Set1	TV3 Set2	TV2 Set1	TV2 Set2	TV3 Set1	TV3 Set2	TV2 Set1	TV2 Set2	TV3 Set1	TV3 Set2
1	1.6	1.6	1.7	1.6	61 @ 4.7	61 @ 4.7	61 @ 4.5	63 @ 4.4	10.01	9.92	10.10	10.03
1 Top	1.5	1.5	1.5	1.5	121 @ 5.2	120 @ 5.4	110 @ 5.6	125 @ 5.7	13.45	12.89	13.08	13.17
3	2.7	2.7	2.7	2.7	65 @ 2.9	73 @ 4.7	66 @ 3.0	68 @ 3.2	6.83	6.73	6.92	6.94
3 Top	2.5	2.5	2.5	2.6	157 @ 4.8	149 @ 4.6	135 @ 4.9	164 @ 5.1	8.91	8.71	8.98	9.07
4	5.4	5.4	5.5	5.5	57 @ 1.7	55 @ 1.6	55 @ 1.6	61 @ 1.7	4.30	4.24	4.30	4.39
4 Top	4.7	4.6	4.8	4.7	84 @ 2.4	84 @ 2.2	81 @ 2.2	90 @ 2.2	5.57	5.50	5.67	5.63
6	11.1	11.1	11.2	11.2	48 @ 1.1	45 @ 1.1	46 @ 1.2	51 @ 1.8	2.74	2.72	2.80	2.80
6 Top	8.7	8.5	8.8	8.5	57 @ 1.4	53 @ 1.4	59 @ 1.4	63 @ 1.4	3.61	3.57	3.69	3.67
7	16.5	16.4	16.3	16.3	51 @ 1.0	49 @ 1.0	48 @ 0.93	52 @ 1.0	2.20	2.19	2.21	2.21
8	23.1	22.9	23.1	22.8	44 @ 0.8	43 @ 0.8	43 @ 0.8	45 @ 0.9	1.87	1.87	1.88	1.89

4.4. Accuracy and Sensitivity of Quality-Factor Measurement

The measured results in the previous section present a greater variation in Qs. The measurement sensitivity rather than the characteristic variance of the large panel can cause such variations. To verify this, Figure 4.8 and Table 4.4 show the pictures and the measurements of the dimensions of Inductors 3_top, which have the highest Qs. The results reveal very few variations were found among different locations and boards.



(a)



(b)

Figure 4.8. (a) Photographs of Inductor 3_top (M1), and (b) W3 of TV3 Set 1

Table 4.4. Dimensions of the fabricated Inductor 3_tops in TV2 and 3

	TV2 Set1	TV2 Set2	TV3 Set1	TV3 Set2
Q@GHz	157@4.8	149@4.6	135@4.9	164@5.1
X	28.4	28.4	25	28.4
Y	52.5	53.8	52.9	52.7
W1	2.8	2.8	2.7	2.9
W2	2.8	2.8	2.7	2.8
W3	2.8	2.8	2.8	2.8
W4	2.8	2.7	2.8	2.9

In [55], additional 0.01 pF parasitic capacitance at the input, which can be generated by slightly different probing points, changes the Q by 23%, and the SRF by less than 10%. One of the main reasons for the variation of Qs is due to the variation of the parasitic capacitances in the measurements. Depending on the probing positions, parasitic capacitances from pads can vary from 0.02 to 0.03 pF. In Figure 4.9, the effects of parasitic capacitance on the input of inductors are shown. The parasitic capacitances, which vary from 0 to 0.05 pF, were connected to the input of Inductor 3_top in TV 3, Set 2. This particular inductor has the highest Q of 164. The Q of Inductor 3_top was reduced to 138 with 0.05 pF capacitance at the input. With a variation from 0.02 to 0.03 pF of the parasitic capacitances at the input, the Q decreased from 164 to 145, resulting in a decrease of Q by 15%. Even though the parasitic inductance associated with pads would also reduce Q, the effect would be minimal compared to the effects of the parasitic

capacitances. Aside from the effects of the parasitic capacitances on the input pad, additional variations also result from the effects of averaging the measured Qs.

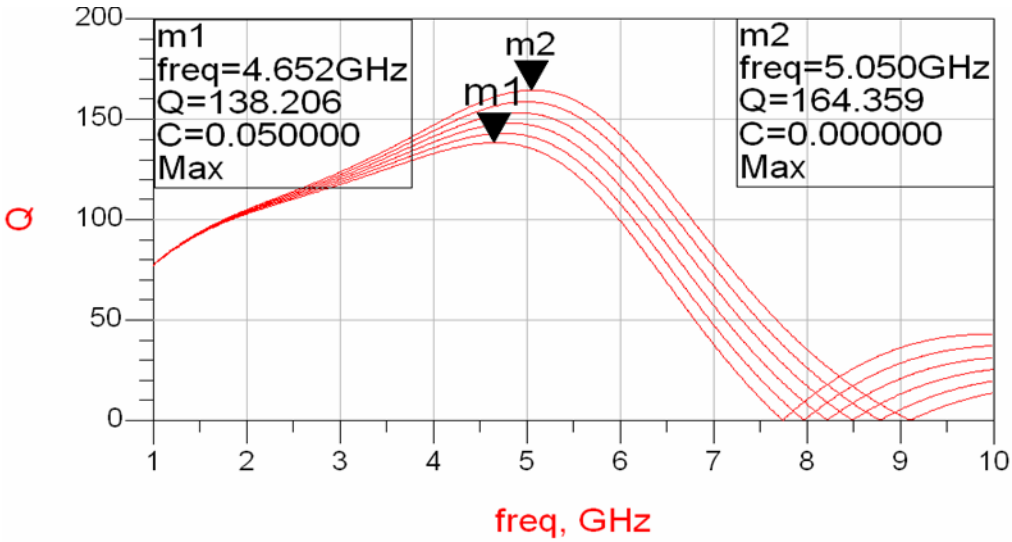


Figure 4.9. Effects of the parasitic capacitances at input of Inductor 3_top of TV3, Set 2

Another issue with high-Q measurement is accuracy of the measurement using VNA. As discussed in Chapter 1, one-port measurement using VNA has a limitation to measure very low impedance. The impedance of the designed inductors are as low as 0.4 Ω, which is equal to -0.15dB. Even though this is larger than the nominal calibration error (around 0.04 dB), this still affects the accuracy of the Q measurement. However, more accurate measurement equipment (such as impedance analyzer) cannot be used at the frequency above 3 GHz. To reduced error, the measurement was done with 100 Hz IF frequency in Agilent PNA 8363B.

4.5. Two-Step de-embedding technique

A two-step "open-short" de-embedding technique was originally developed for the high-frequency characterization of bipolar transistors [56]. This de-embedding technique assumes all parallel parasitics are in the signal pads and all series parasitics are in the interconnect lines. The de-embedding procedure begins with the "open" correction, followed by the "short" correction:

$$Y_{dut,os} = ((Y_{meas} - Y_{open})^{-1} - (Z_{short}^{-1} - Y_{open})^{-1})^{-1} \quad (4\text{-}3)$$

In the above equation, Y_{open} is a one-port admittance parameter measured on the "open" dummy structure, and Z_{short} is a one-port impedance parameter measured on the "short" dummy structure. Although de-embedding techniques such as in [57], [57], [59], and [60] have been thoroughly researched, the two-step de-embedding technique has been chosen for its simplicity and good matching characteristics. In this paper, 32 inductors on M3 layer, which has thru-hole interconnections with GSG pads, were de-embedded to remove the effect of pads and thru-holes using the two-step de-embedding technique. In Figure 4.10, the line with circles is the measured result of Inductor 6 (55x55, 1turn on M1), while the solid line is the simulated result of this inductor. As Figure 4.10 shows, the SRF of simulated and measured results differ significantly because of the parasitics from pads and thru-holes. The line with squares is the measured result after the two-step de-embedding procedure was applied using the open-short technique. After the de-embedding procedure was applied, the SRF is well matched, and the inductance value also shows good model-to-hardware correlation, as shown in Table 4.5. The table shows a summary of the de-embedded inductances and the SRFs of 16 inductors from the two locations of TV 1. The SRFs of Inductors 1 and 2 were not measured because of

equipment limitations. The Qs were not de-embedded for these inductors because of measurement sensitivity.

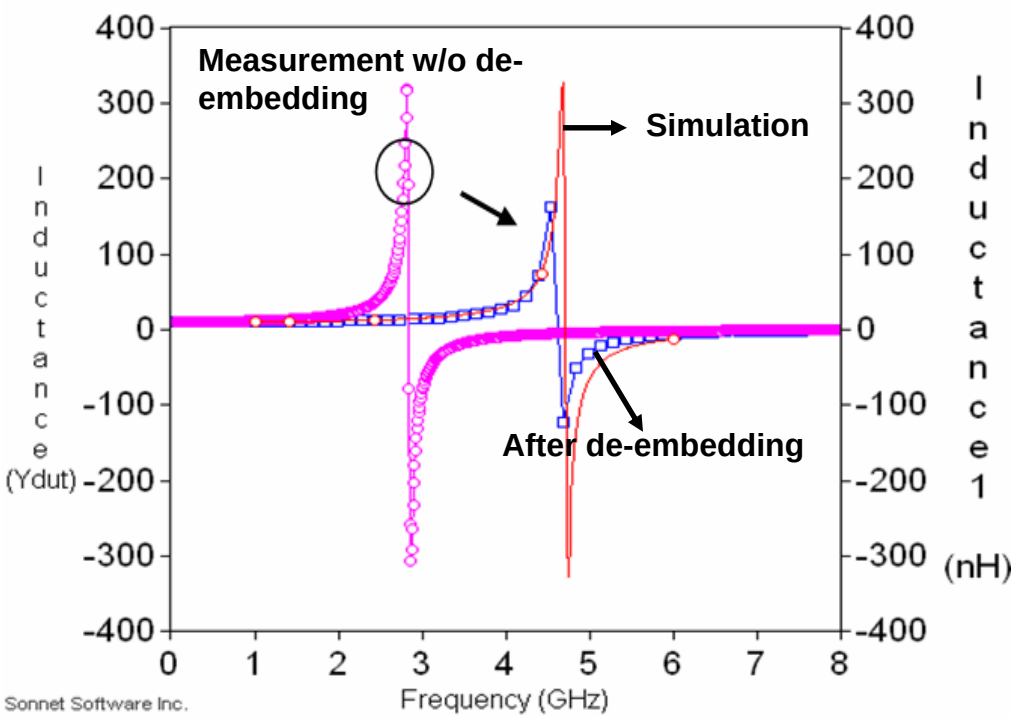


Figure 4.10. Measured results after de-embedding and correlation with simulation results

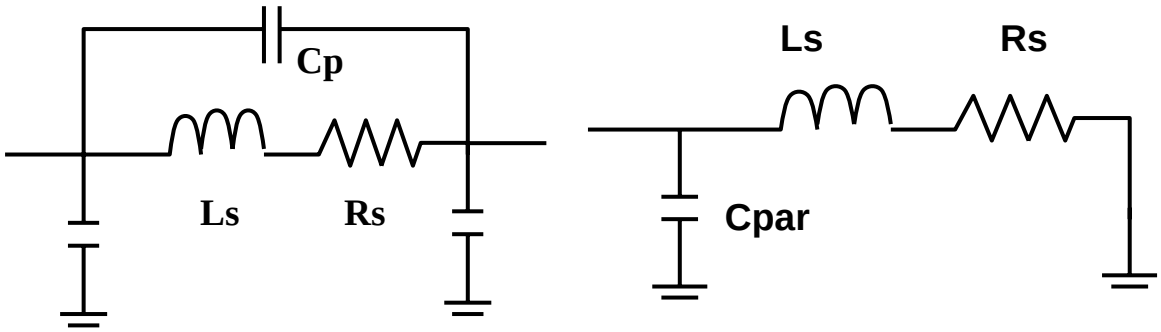
TABLE 4.5. Measured results of the inductors after de-embedding and correlation with simulated results.

Inductors	Inductance (nH)			Self Resonance Frequency (SRF) (GHz)		
	Simulation	Measurement		Simulation	Measurement	
		Set1 TV1	Set2 TV1		Set1 TV1	Set2 TV1
1	0.8	0.8	0.8	31.2	N/A	N/A
2	1.0	1.0	1.0	23.7	N/A	N/A
3	2.3	2.2	2.2	12.6	11.0	12.6
4	5.4	5.0	5.1	6.7	6.6	6.9
5	4.2	3.9	3.9	7.8	7.8	5.0
6	9.7	10.2	10.0	3.9	3.8	3.9
7	16.1	15.6	14.8	3.0	2.9	3.0
8	21.8	20.8	20.3	2.4	2.4	2.4

4.6. Measurement-Based Inductor Model

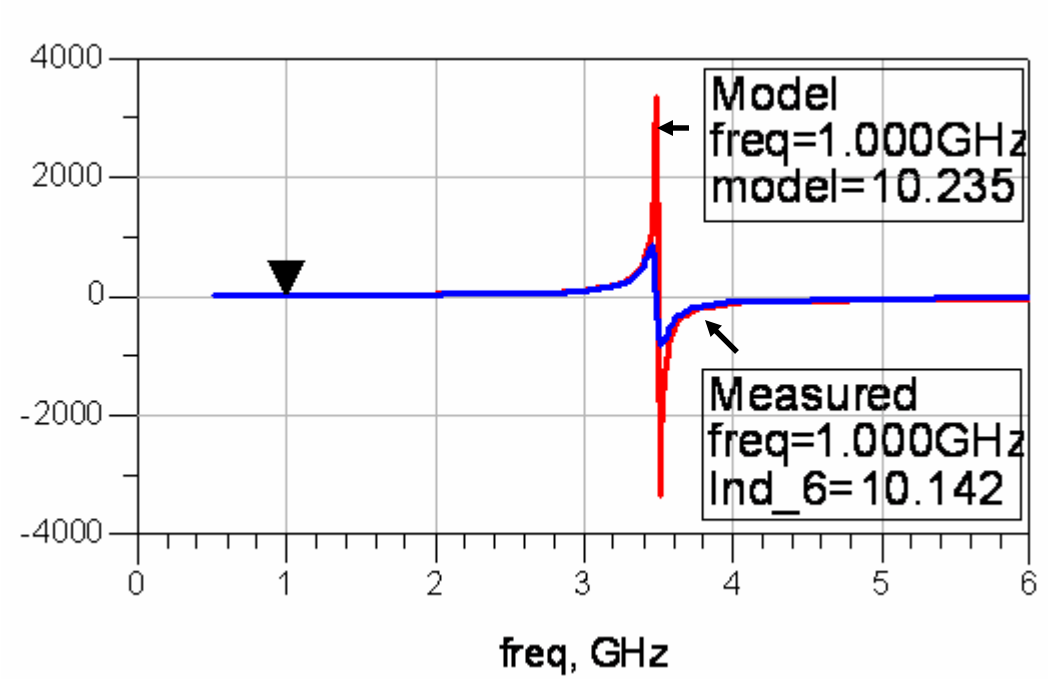
The designed inductors were measured using Agilent VNA with the SOLT calibration, combined with additional on-board open and short standards to implement the de-embedding procedure. Since the inhomogeneous LCP substrate can be assumed as lossless, the dielectric loss can be ignored and an equivalent model can be simplified as Figure 4.11. A parallel capacitance (Cp) can be determined from the SRF as in (4-4), and a series resistance (Rs) can be calculated from the Q as in (4-2). In (4-4), ω is the radian frequency, L is inductance, and Cp is the parallel capacitance. With the initial values of L and Cp, the values of L, Cp, and R for the designed inductors in TV1 were optimized in Agilent ADS, and model-to-hardware correlations are shown from Figures 4.12 to 4.14. The extracted parameters are shown in Table 4.5.

$$\omega^2 = \frac{1}{LC_p} \tag{4-4}$$

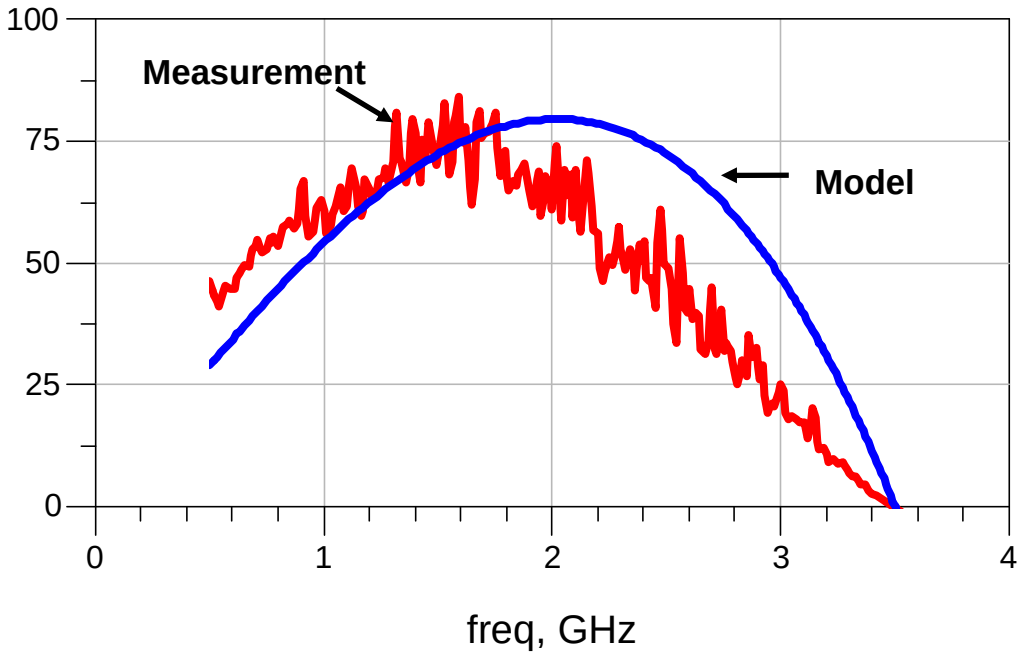


(a) (b)

Figure 4.11. Equivalent circuits of (a) two-port and (b)one-port inductor

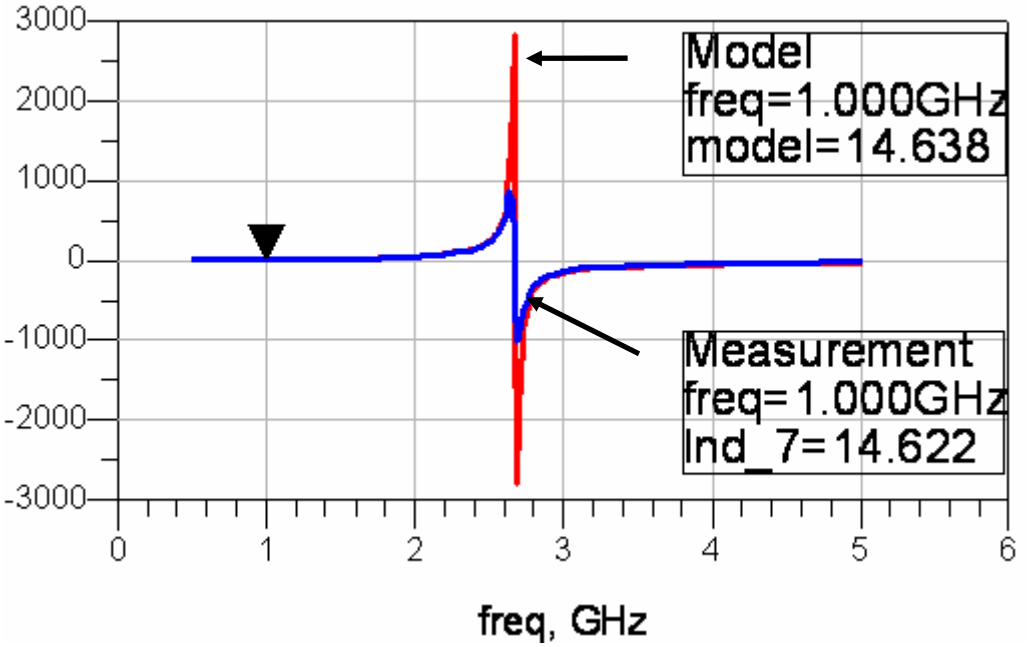


(a)

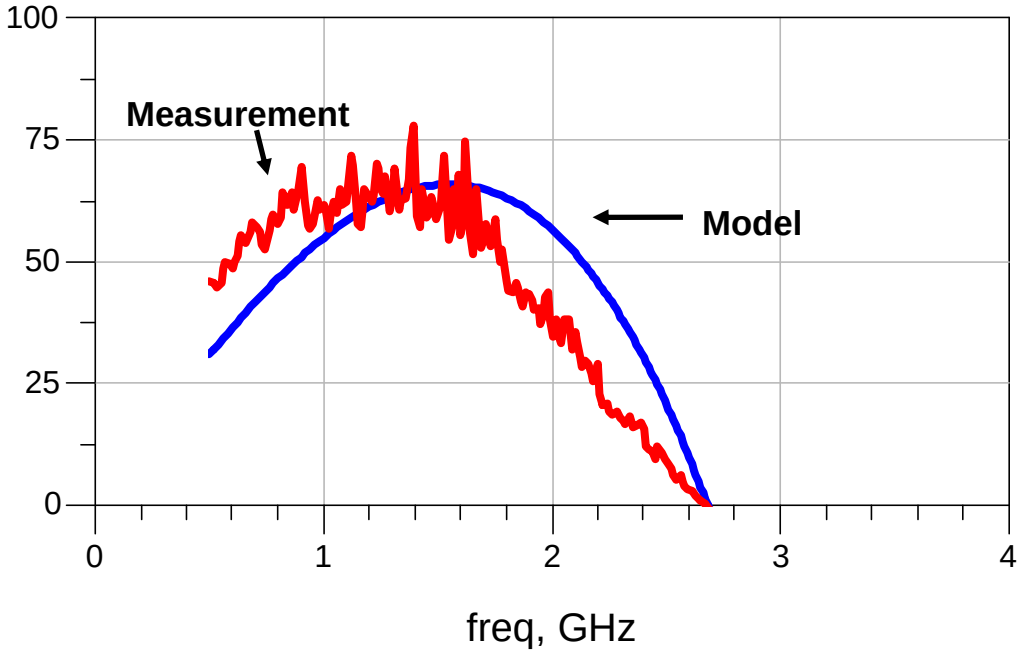


(b)

Figure 4.12. Model-to-hardware correlations in (a) Inductance and (b) Q of Inductor 6 at TV2, Set1

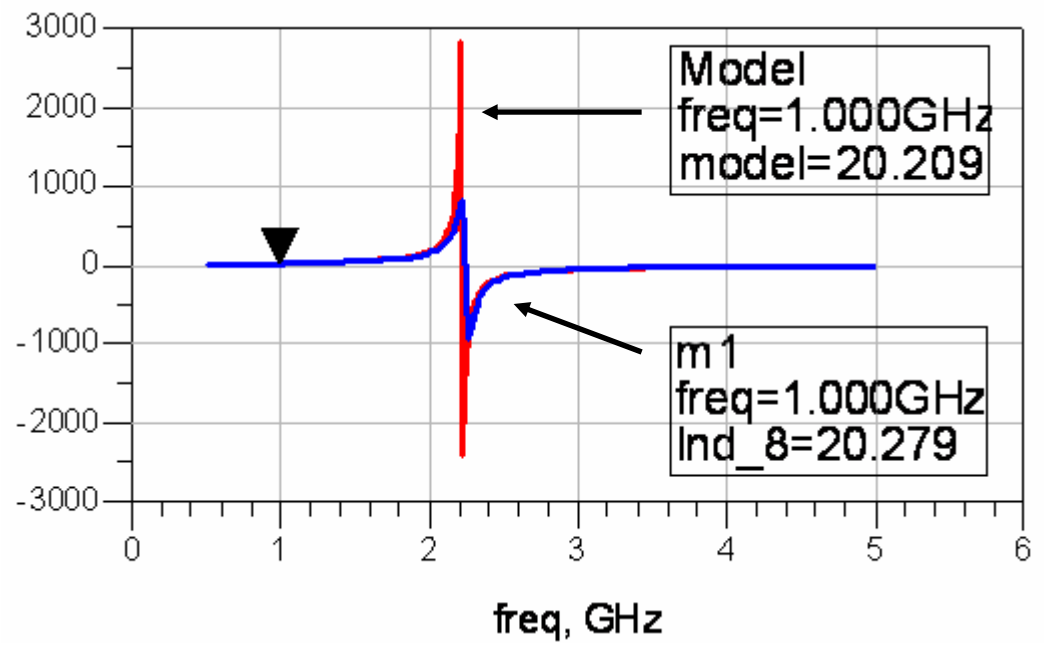


(a)

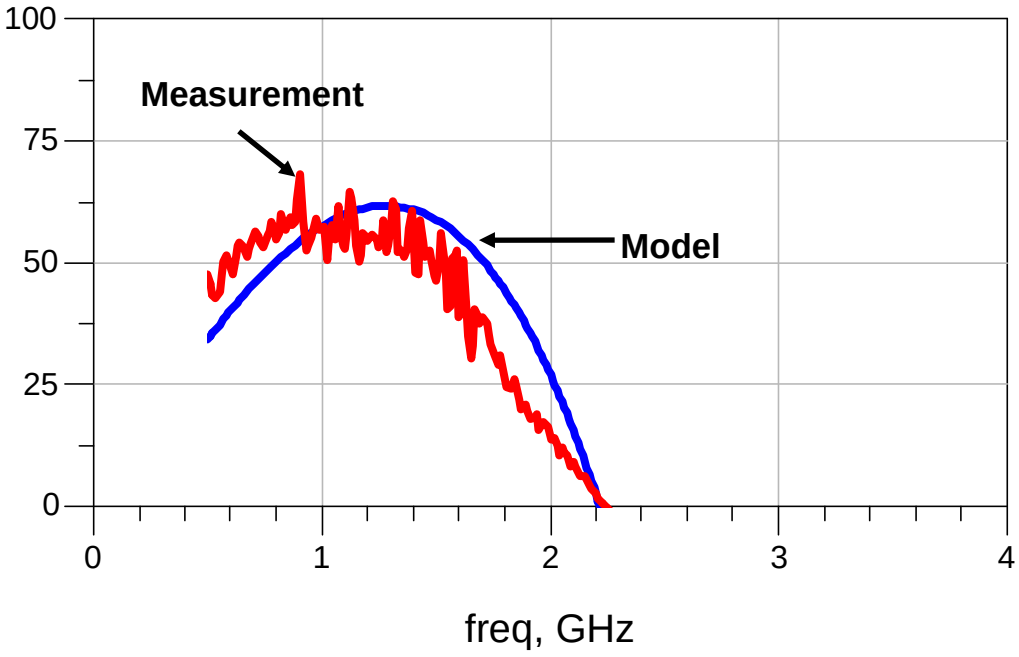


(b)

Figure 4.13. Model-to-hardware correlations in (a) Inductance and (b) Q of Inductor 7 at TV2, Set1



(a)



(b)

Figure 4.14. Model-to-hardware correlations in (a) Inductance and (b) Q of Inductor 8 at TV2, Set1

Table 4.6. Extracted parameters of the measurement-based one-port inductor model

	Rs (Ω)	Ls (nH)	Cp (pH)
Inductor 1_Top	0.4	1.54	0.1
Inductor 3_Top	0.4	2.5	0.12
Inductor 4_Top	0.8	4.65	0.17
Inductor 6_Top	1.25	8.2	0.22
Inductor 6	1	9.4	0.22
Inductor 7	1.24	12.6	0.28
Inductor 8	1.4	16.1	0.32

4.7. Design and Characterization of Compact 3D Capacitors

Along with inductors, capacitors are the basic building blocks in the integration of RF Front Ends. While high Q is the critical parameter in inductors, size is the main parameter in capacitors since the Q is limited by the loss tangent of the dielectric material. Table 4.7 shows the 3D capacitors used in this dissertation for reducing the size. Four different types of 3D capacitors were designed for characterization.

In Figure 4.15, Type 1 capacitor had port 1 on both M1 and M3 and ground layers on both M2 and M4. Vertical connections were realized using through holes. Table 4.8 summarizes the measurement results of the 3D capacitors in comparison with a similar-size single capacitor. 3D capacitors show more than two-fold increase in capacitance as compared to the single capacitor. 3D capacitors combined with 3D inductors provide for an optimal solution for implementing compact RF module designs because of high performance, low profile, and compact size. The same de-embedding procedure has been applied to the capacitors as the previous inductors. Figure 4.16 shows the profile of the capacitance and Q of the designed capacitors after de-embedding procedure was applied.

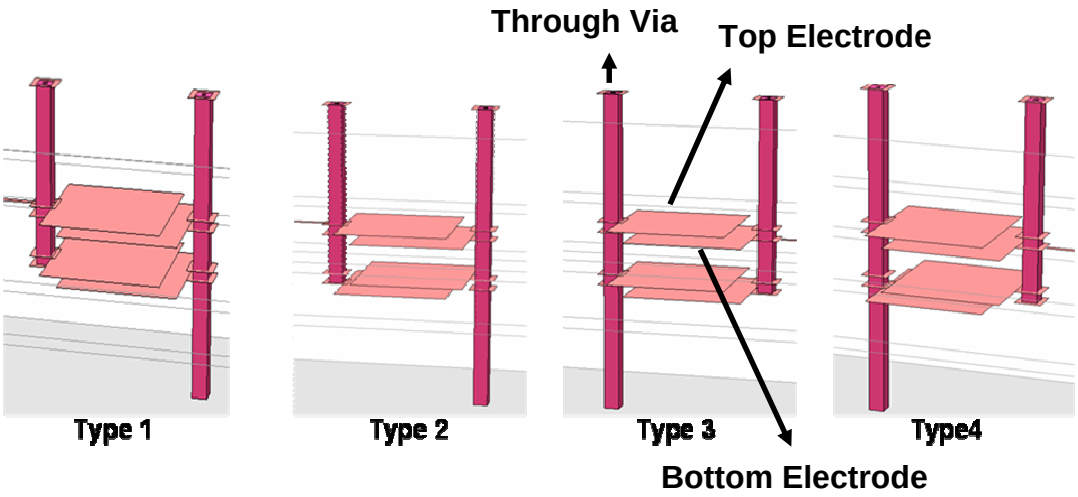


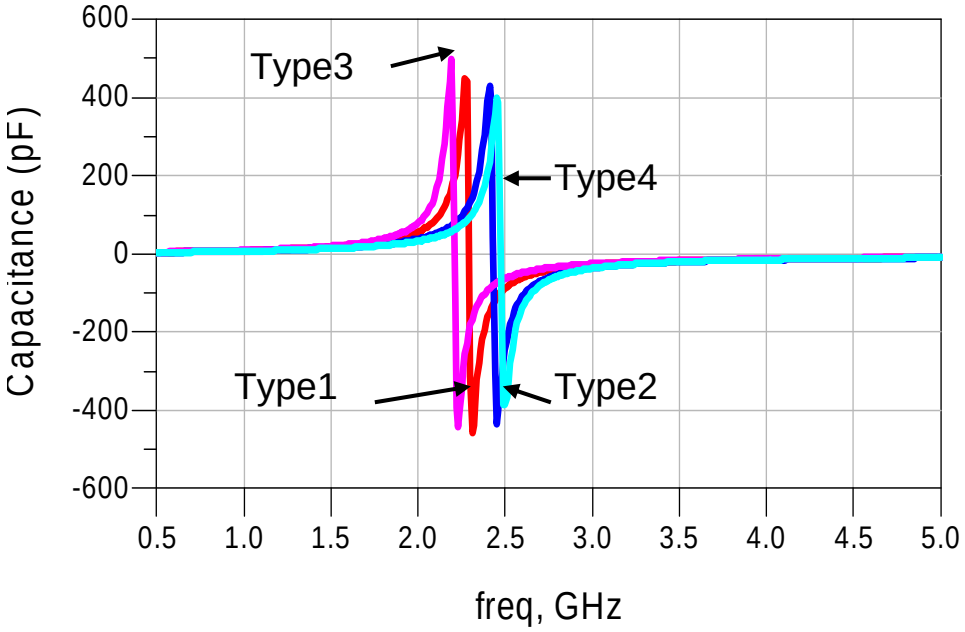
Figure 4.15. 3D layout of the four types of 3D capacitors

Table 4.7. Four types of 3D capacitors

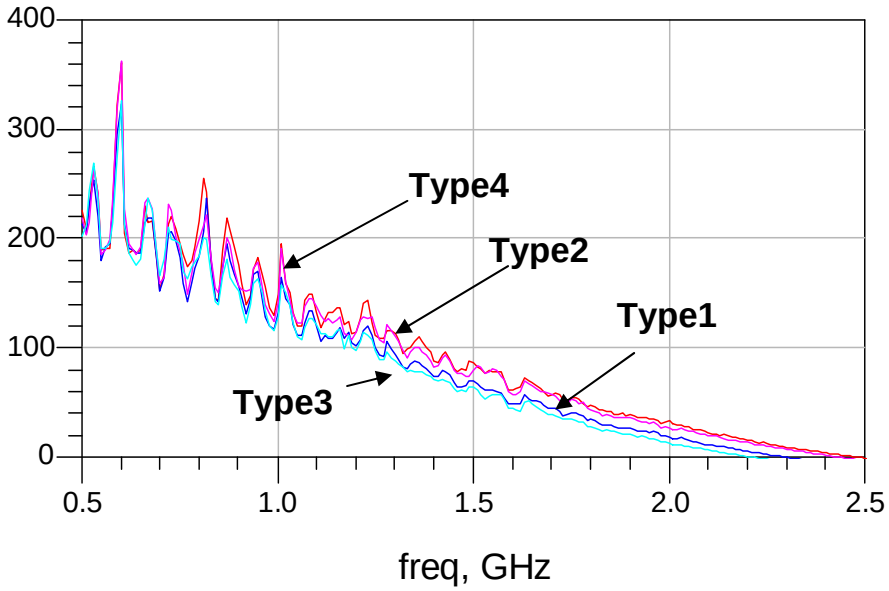
Types	Port 1	Ground
Type I	M1 and M3	M2 and M4
Type II	M1 and M4	M2 and M3
Type III	M2 and M4	M1 and M3
Type Iv	M2 and M3	M1 and M

Table 4.8. Summary of measured results of 3D capacitors

	Capacitance (pF)	Q	SRF (GHz)
Single	3.05	291	3.3
3D Type 1	6.75	235	2.4
3D Type 2	6.11	237	2.5
3D Type 3	7.27	232	2.2
3D Type 4	5.95	245	2.4



(a)



(b)

Figure 4.16. Measurement results of the designed capacitors after de-embedding: (a) capacitance and (b) Q

4.7. Measurement-Based Capacitor Model

A measurement-based capacitor model can provide an accurate model and its accuracy depends on the accuracy of the measurement system, calibrations, and de-embedding. The designed capacitors were measured using Agilent VNA with the SOLT calibration, which has been done for the measurement of the inductors. Two-step de-embedding procedure was applied after measurements. An equivalent model can be simplified as Figure 4.17. A series inductance (Ls) can be determined from the SRF as in (4-4), and a series resistance (Rs) from the Q. The initial values of Ls, and Rs are optimized in Agilent ADS, and Table 4.9 shows the extracted parameters. Figures 4.18 and 4.19 show good model-to-hardware correlation.

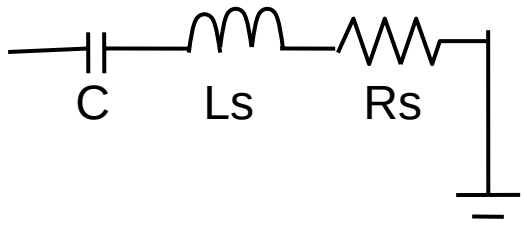
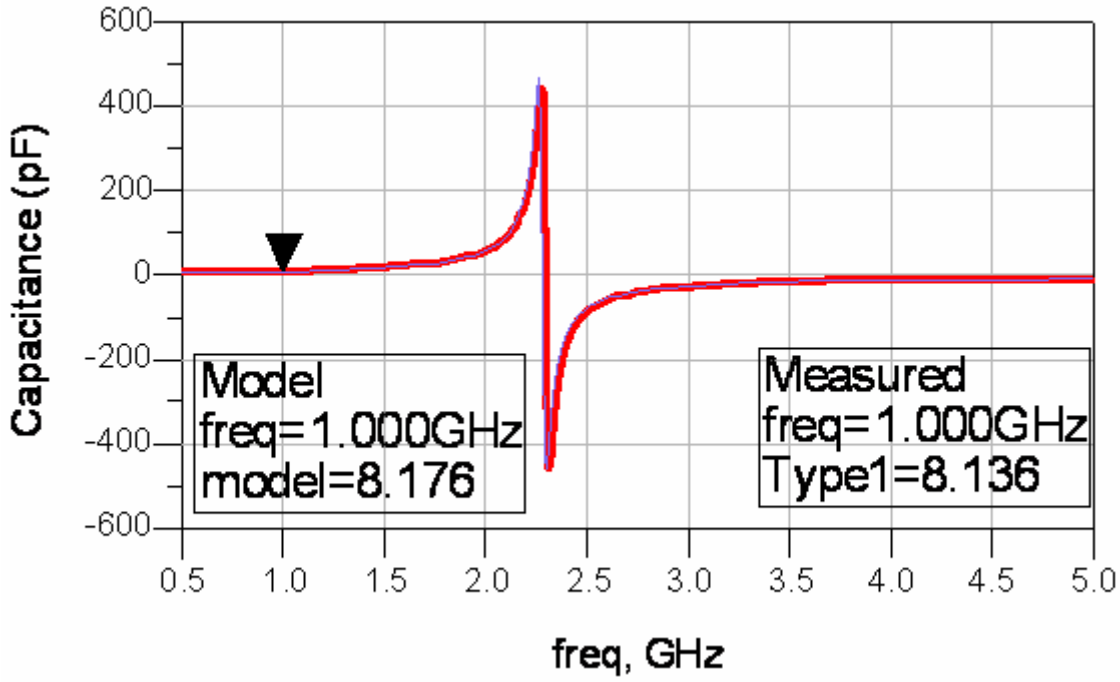


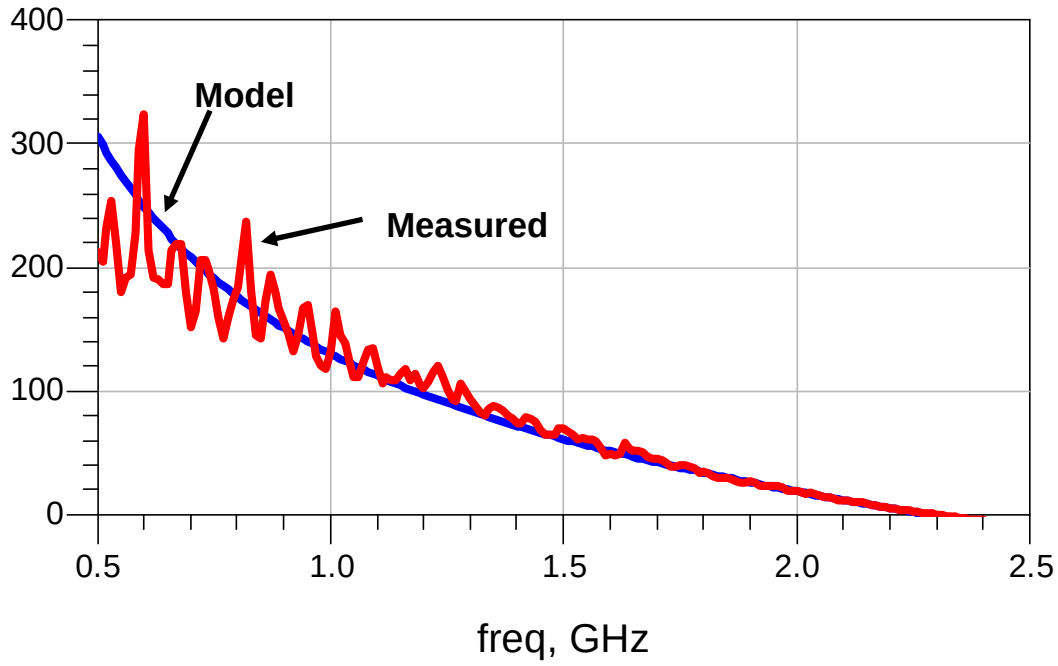
Figure 4.17. Equivalent circuit of one-port capacitor

Table 4.9. Extracted parameters of the measurement-based capacitor model

	C	Ls	Rs
Type 1	6.6	0.74	0.15
Type 2	6.05	0.7	0.17
Type 3	7.05	0.73	0.15
Type 4	5.6	0.74	0.18

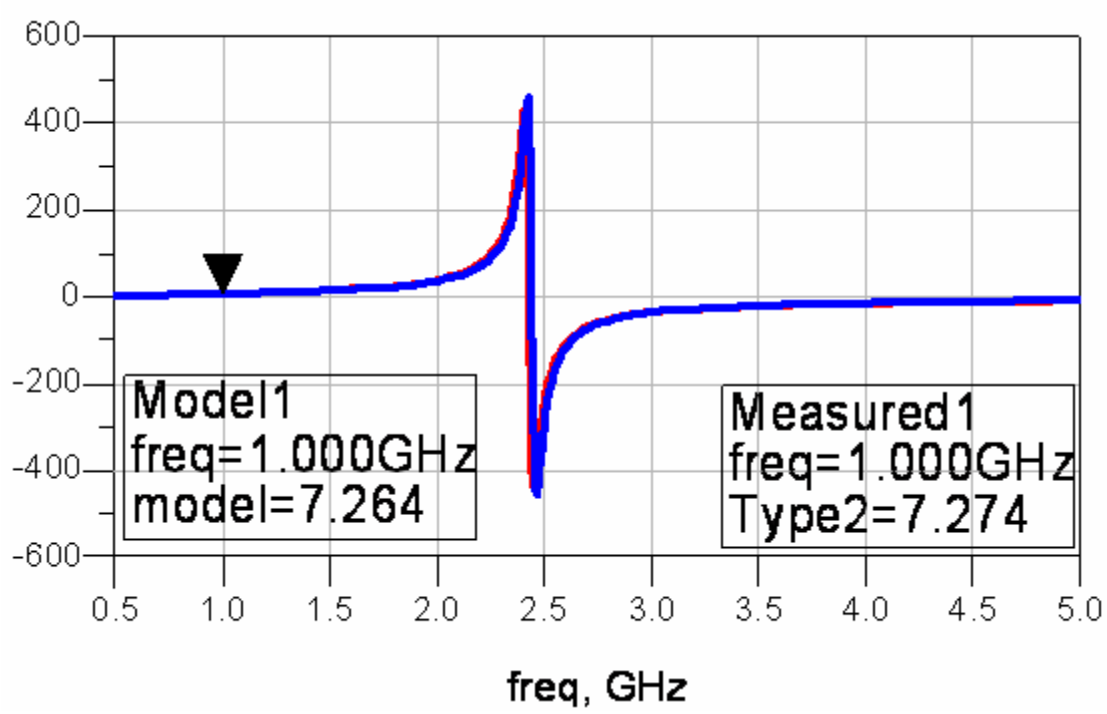


(a)

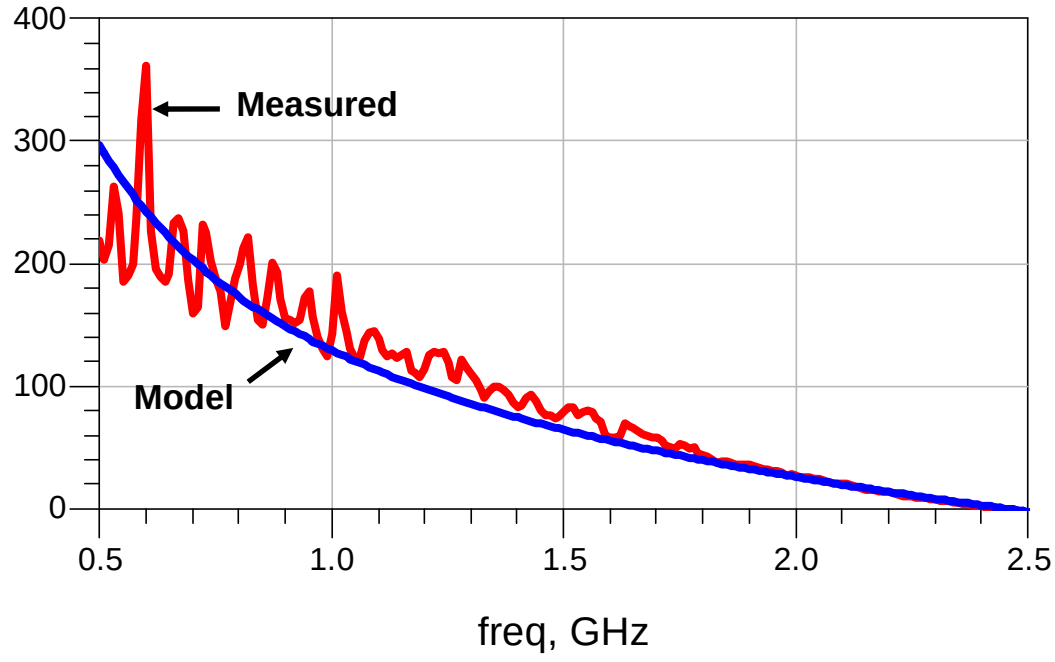


(b)

Figure 4.18. Model-to-hardware correlations in (a) Capacitance and (b) Q of capacitor Type 1



(a)



(b)

Figure 4.19. Model-to-hardware correlations in (a) Capacitance and (b) Q of capacitor Type 2

4.8. Summary

LCP substrates are attractive high-frequency materials due to their low loss, low water absorption, and low cost. The lower cost is realized through larger panel processing, which is also processed at much lower temperature because LCP process is compatible with standard PWB process. In this chapter, comprehensive characterizations have been conducted for the efficient 3D integration of high-Q passives using a balanced LCP substrate. At two different locations from three different large M-LCP panels, 76 inductors and 16 3D capacitors were designed and measured. Inductors on different layers (the top and third layers) clearly showed the scalability of Q, ranging from 43 to 164. In addition, the measured results show very little variations over the two different locations in each TV and among the three different TVs. Finally, the parameters for the measurement-based inductor model were extracted from the measured results. The results validate the large panel process of the M-LCP substrate.

To reduce the lateral size, multi-layer 3D capacitors were designed. The designed 3D capacitors with inductors can provide optimized solutions for more efficient RF front-end module integration. In addition, the parameters for the measurement-based capacitor model were extracted. Critical inductors for high performances can be achieved with the highest Qs in the top-most layer, while other inductors can be embedded on other layers. As discussed in this chapter, 3D capacitors can reduce the size more effectively than general parallel-plate capacitors. In addition, a two-step de-embedding technique was applied to remove the effect of pads and thru-hole interconnections. This technique resulted in closer correlation between simulation and measured results.

CHAPTER 5

DESIGN OF LUMPED ELEMENT RF CIRCUITS IN INHOMOGENEOUS MULTI-LAYER LCP SUBSTRATES

5.1 Introduction

Cost reduction, fast time to market, compact size, low profile, and high performance make SOP an attractive solution for RF front-end modules. As shown in Figure 1.1, as the number of components increase exponentially, higher integration is ciritical in a milti-band system.

Even though performance of RF front-end components is directly related to the quality factor (Q) of passives, this does not imply that every passive should have a high Q. In this regard, more efficient integration can be achieved using a variety of Qs in a single circuit. In other words, a few high-Q passives can be used for critical components while other relatively low-Q passives can be used for remaining components, which results in more efficient integration. 3D integration provides more flexibility in achieving higher Qs for the critical components than 2D integration. In 2D integration, the Qs are fixed due to the lateral area used.

RF receiver front-end modules have been developed in inhomogeneous multi-layer LCP. LNA [42], VCO [9], [43], band-passive filter [3], Marchant balun [5], and antenna [61] have been developed and reported. Figure 5.1 shows the simple RF receiver front end with developed modules in inhomogeneous LCP stack-ups. In this chapter, RF front-end modules, such as filter, balun, and mixers have been designed and measured

using high-Q embedded passive components in inhomogeneous multi-layer LCP substrates. Section 5.2 discusses a C-band filter using lumped elements, and Section 5.3 presents a double-balanced mixer for 5GHz wireless LAN application. A doubly double-balanced mixer is introduced in Section 5.4 for the miniaturization of the CDMA receiver. Finally, Section 5.5 shows a 30 GHz gap-coupled band-pass filter in inhomogeneous multi-layer LCP substrates.

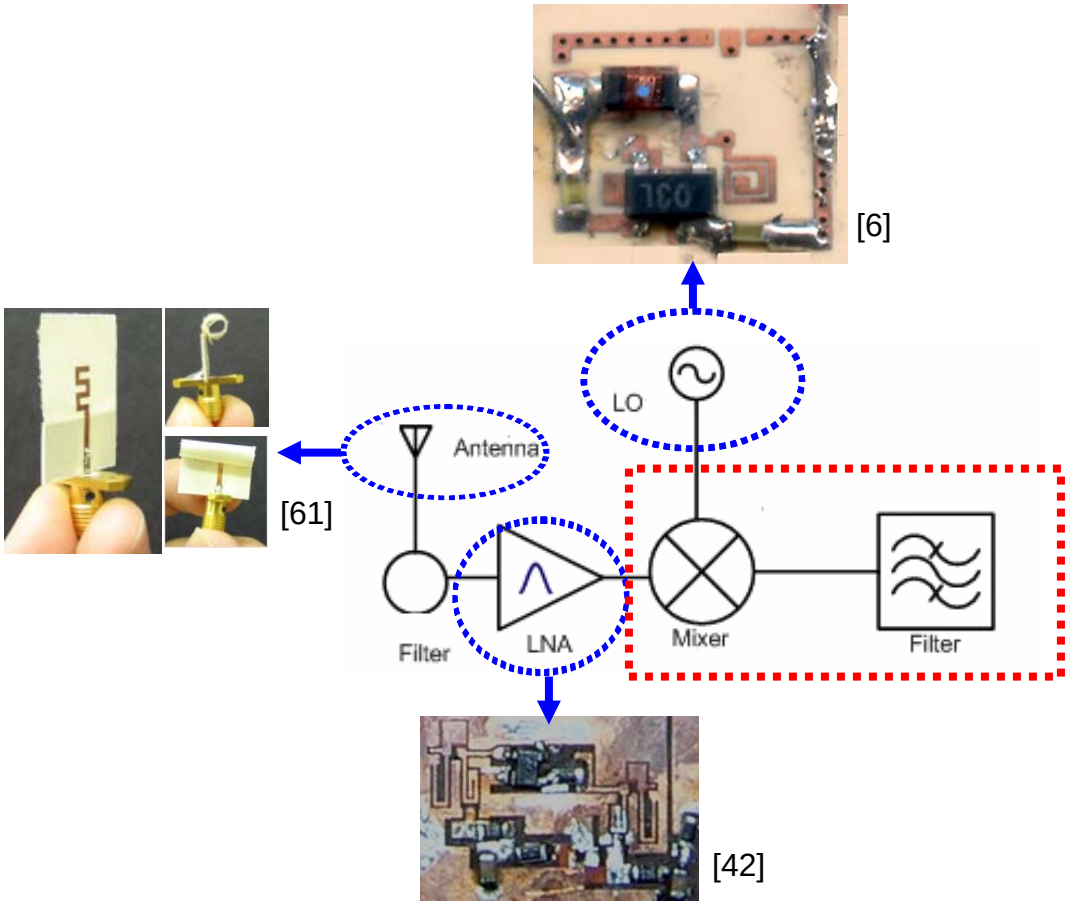


Figure 5.1. RF Receiver Front end in inhomogeneous multi-layer LCP substrates

5.2 C-Band Filter

The previously characterized inductors and capacitors in a tree-layer LCP substrate as shown in Figure 5.2 were used to design a C-band filter, shown in Figure 5.3.

The filter was designed in a stripline configuration, i.e., both top and bottom metal layers were used as the ground plane. The stripline configuration provides excellent EM shielding that prevents radiation loss. The filters were initially simulated using ADS with ideal components and then optimized with parasitics.

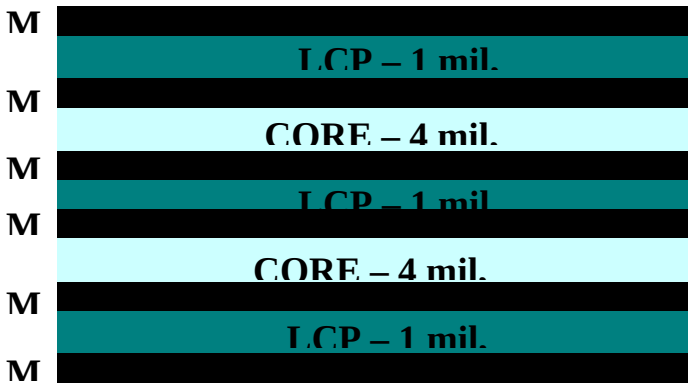


Figure 5.2. Cross-section of the three-layer LCP substrate

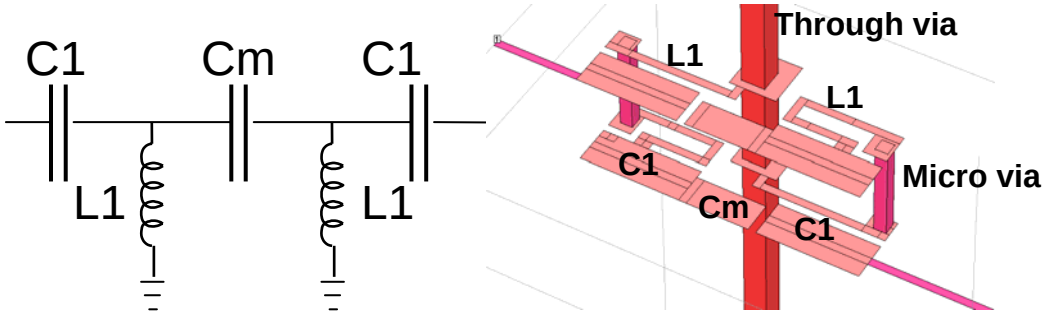


Figure 5.3. Schematic and layout of the designed filter

Once ADS simulations were finalized, EM simulations were performed using SONNET [46]. A circuit model and its 3D layout are shown in Figure 5.3, and the simulation results with SONNET are shown in Figure 5.4 with measured results. The target specs were 3dB bandwidth from 5 GHz with less than 0.8 dB insertion loss. The

simulation results show that 3 dB bandwidth starts at 4.93 GHz, but with the measured results, it starts at 5.23 GHz, the insertion loss of each being 0.98 dB and 1.03 dB, respectively. The mutual coupling between the inductors with opposite current directions decreased the effective inductance, which resulted in higher frequency than simulated frequency.

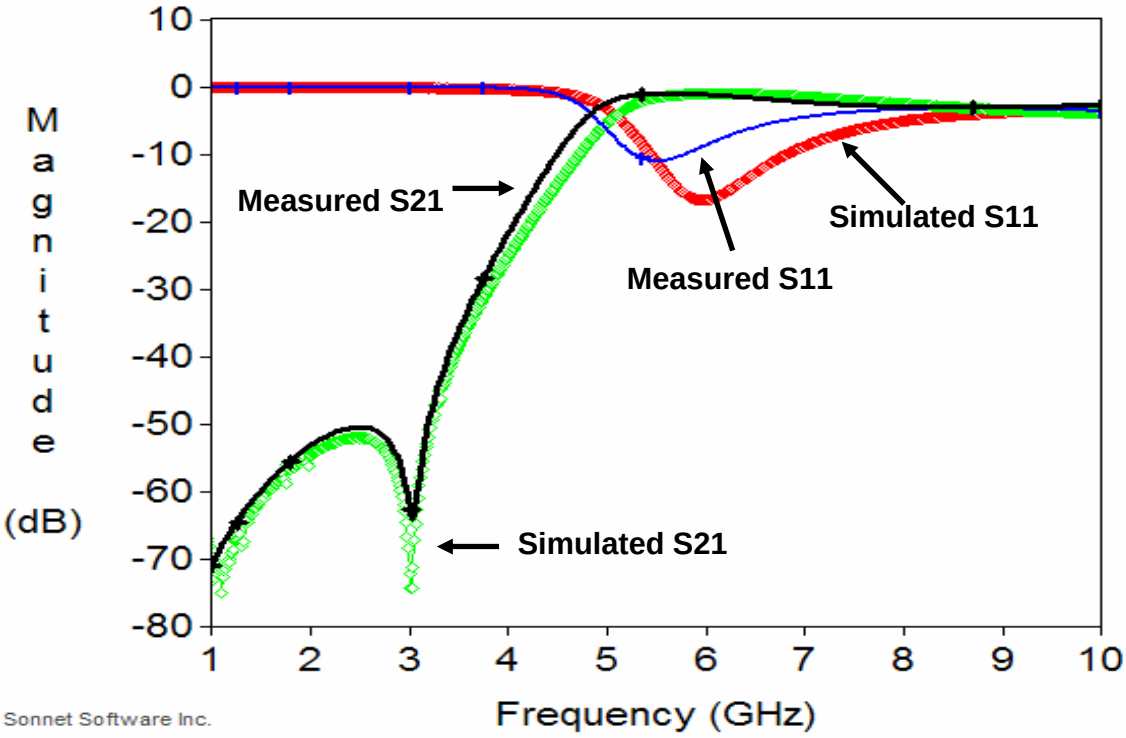


Figure 5.4. Measured and simulated results of the C-band filter

5.3 Double-balanced Mixer

Figure 5.5 shows the schematic of a lumped balun composed of two PI networks. Each PI network was designed to transfer impedance from a 50 Ω source to a 100 Ω load with ± 90 ° phase shift, which results in a 180° phase difference between the loads. Figure 5.4 also shows a photograph of the designed lumped balun. The size of the lumped balun is 2.6 x 1.58 mm^2.

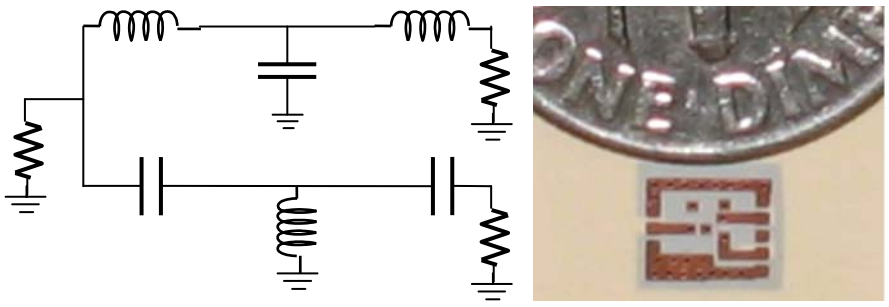
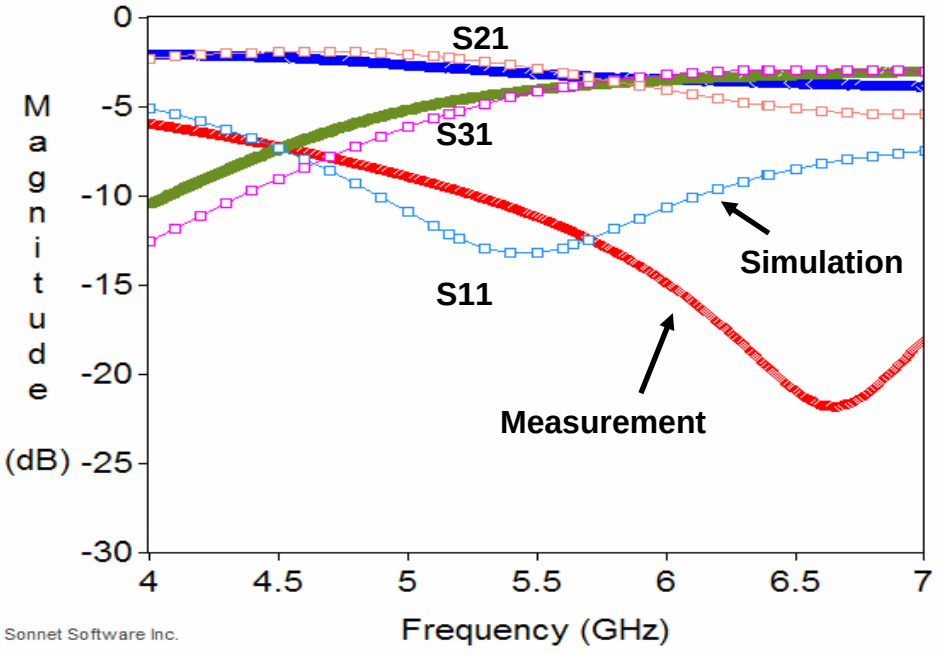
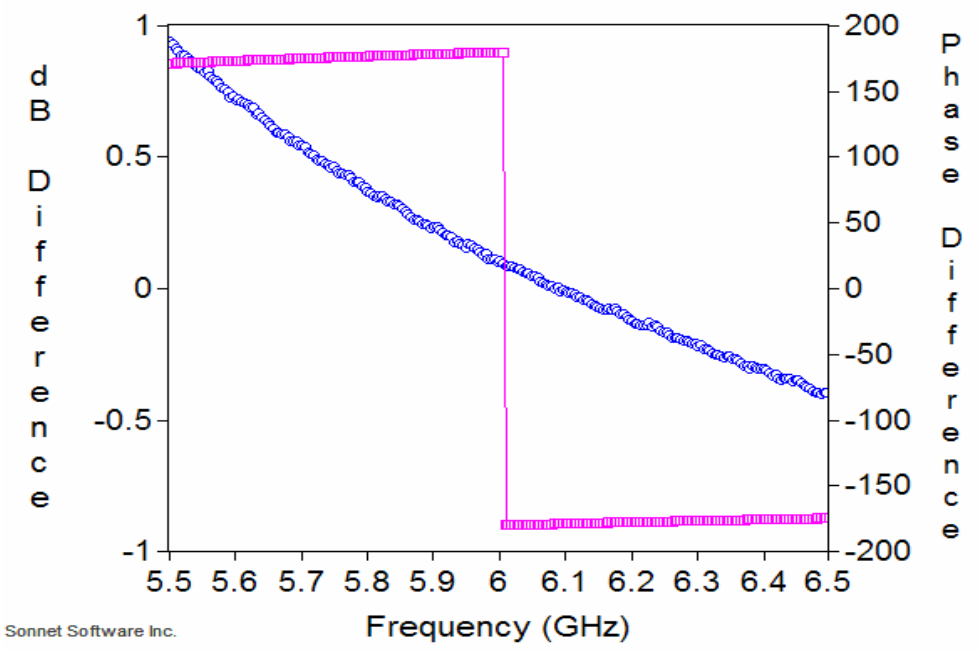


Figure 5.5. Schematic and photograph of a lumped balun

Figure 5.6 shows the measured results of the designed lumped balun. The target specs were 0.8dB insertion loss with less than 1 dB magnitude imbalance and less than 10 degrees of phase imbalance from 5.775 to 5.875 GHz. While the simulated results show 0.5 dB insertion loss at 5.78 GHz, the measured results show 0.52 dB at 6.08 GHz.



(a)



(b)

Figure 5.6. Measured results of the lumped balun: (a) S parameters and (b) Phase and magnitude imbalances

Both good phase imbalance and magnitude imbalance were achieved. From 5.6 GHz to 6.5 GHz, less than a 1 dB magnitude imbalance and less than 10 degrees of phase imbalance were achieved. The discrepancy between the measurement results and the simulation results can be attributed to the matching in port 3 because the openings in the ground plane and the multiple thru-hole connections cause a coupling between components.

A balun design using distributed elements such as Marchand balun exhibits wide bandwidth, low loss, and large size. Several studies were conducted to reduce the size of the Marchand balun using capacitive loading although the small size results in narrow bandwidth. However, a compact wide-band balun using multi-band theory was shown in [5]. Accordingly, the standard Marchand balun was designed to operate at two different frequency bands by adding lumped reactance in series with the output impedance [5].

The previously designed Marchand balun in [5] was used for the RF and IF ports in a double-balanced ring mixer [62]. The schematic of the mixer is shown in Figure 5.7. Since the designed balun had three ports, it was modified for a four-port device to accommodate an IF port. The LO balun was realized using the previously designed lumped balun in multi-layer LCP substrate. In addition, the designed mixer had an Agilent HSMS-8207 silicon Schottky ring diode, surface-mounted on the top-most layer, and it was directly connected to the embedded baluns using thru-holes. A photograph of the fabricated double balance mixer is also shown in Figure 5.7.

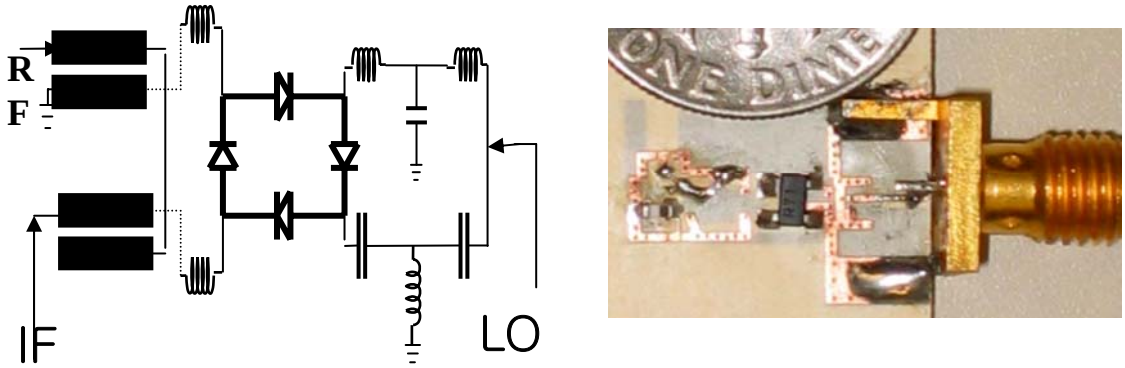


Figure 5.7. Double balanced mixer: schematic and photograph

The measured performance of the mixer is shown in Figure 5.8, which shows a conversion loss with an IF frequency of 20 MHz. The LO power varied from 11 dBm to 13 dBm. The conversion loss of 5.1 dB, achieved at 4GHz, varied from 5.1 dB to 8.6 dB from 3.5 GHz to 5.5 GHz. Figure 5.9 shows the conversion loss with respect to the RF input power at 4 GHz with 12 dBm of LO power. The conversion loss was approximately 5 dB. Figure 5.10 shows the conversion loss variation with respect to IF frequency. The conversion loss of 8.6 dB occurred with an IF frequency from DC to 500 MHz, and the 11 dB of conversion loss occurred at 1200 MHz of the IF frequency. Figure 5.11 shows the isolation of RF to LO and LO to IF.

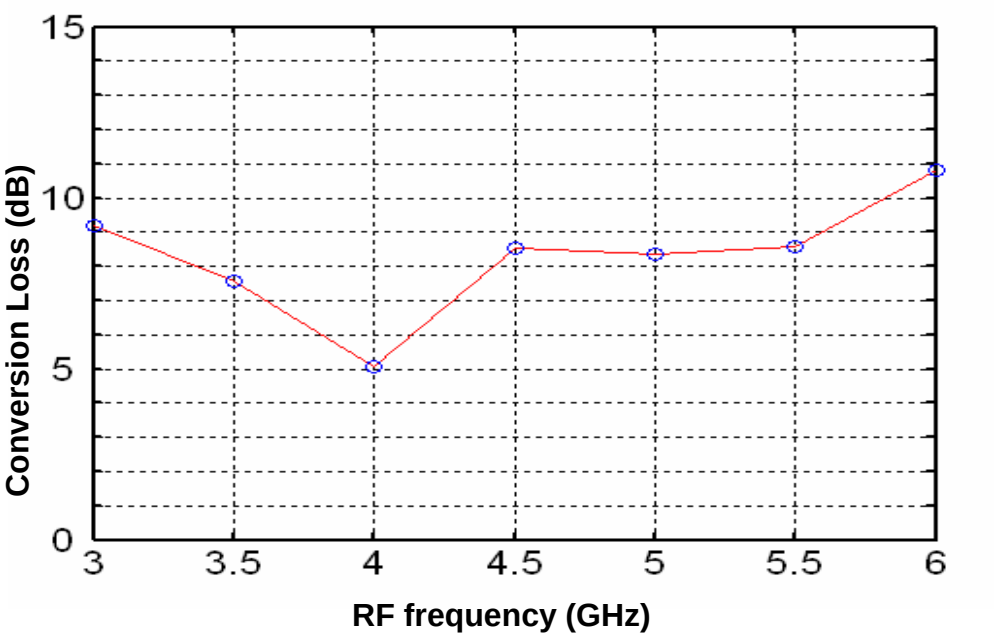


Figure 5.8. Measured results of the double balanced mixer: Conversion Loss vs RF Frequency

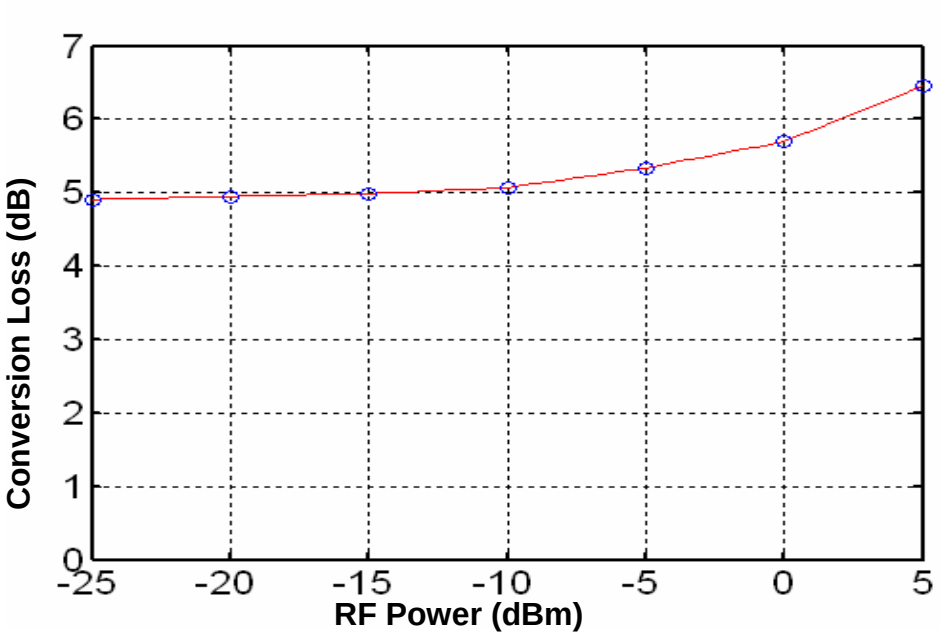


Figure 5.9. Measured results of the double balanced mixer: Conversion Loss vs RF Power

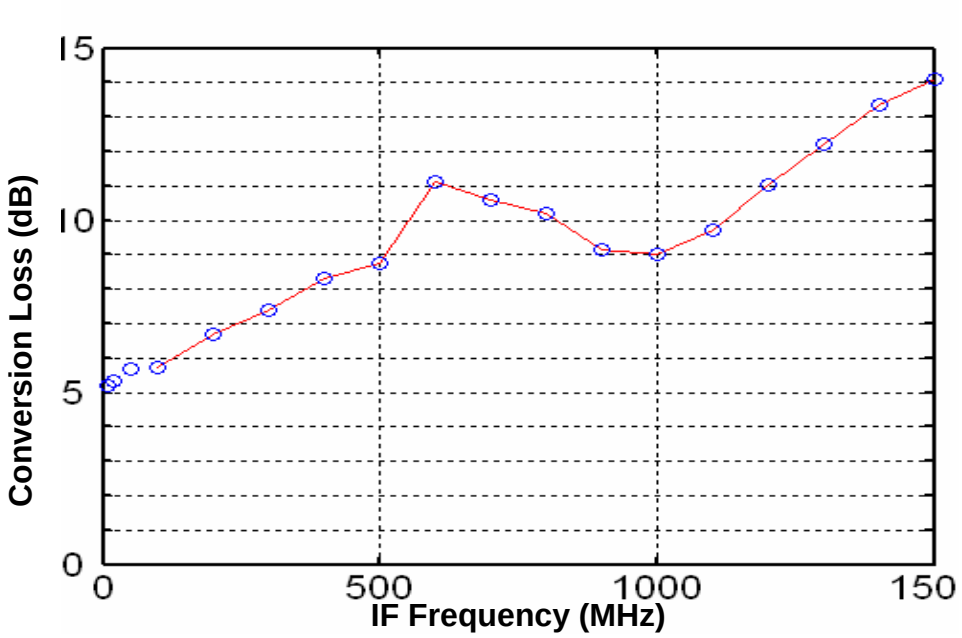


Figure 5.10. Measured results of the double balanced mixer: Conversion Loss vs IF Frequency

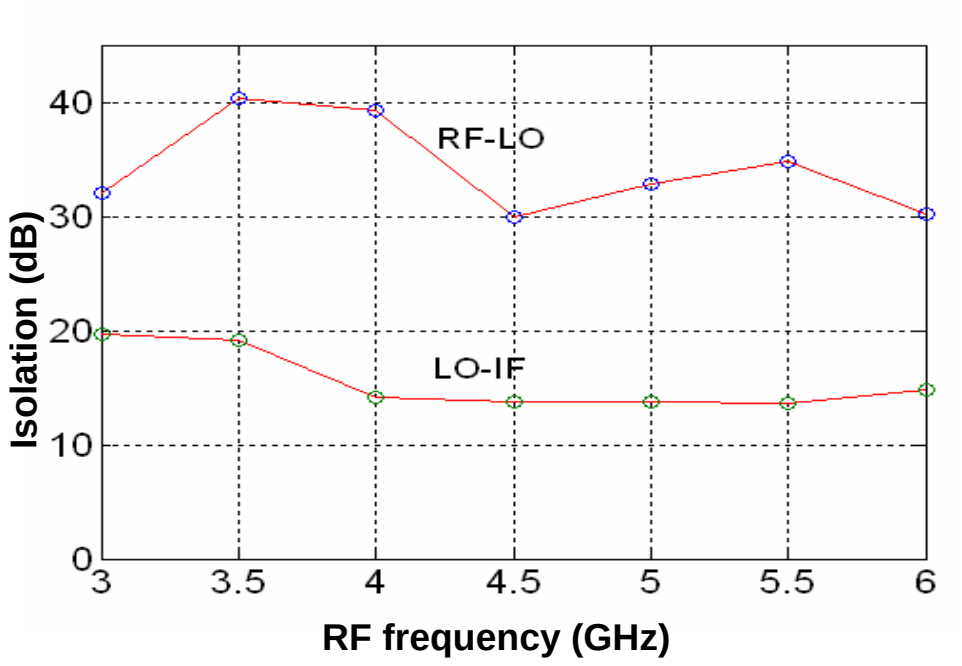


Figure 5.11. Measured results of the double balanced mixer: Isolation vs RF Frequency

5.4. Doubly Double-Balanced Mixer

This section presentes a compact doubly double-balanced mixer at 1.4 GHz RF frequency and 700 MHz LO frequency, resulting in 1 GHz of IF frequency. The mixer was composed of dual baluns at RF and LO ports and a single IF balun. The embedded passive integration technology, combined with inhomogeneous multi-layer LCP substrates, enables a designer to realize five integrated lumped baluns using 20 embedded passive components. With these baluns, two Agilent HSMS 2828 quad diodes were used. Figure 5.12 presents a schematic of the designed doubly double balanced mixer.

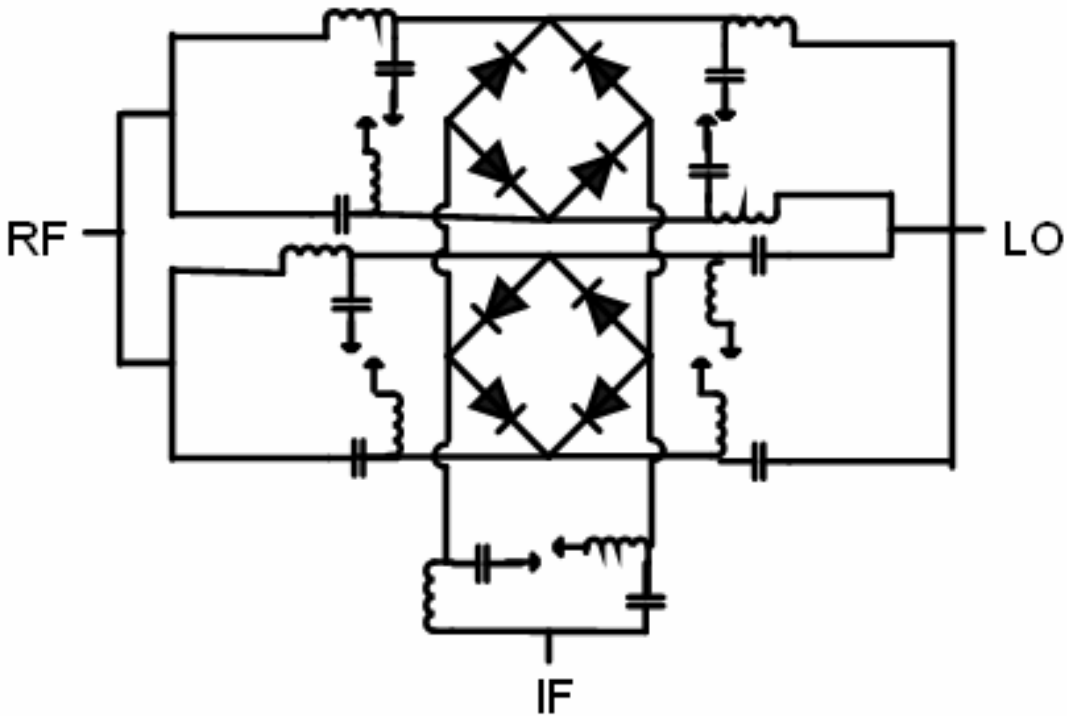
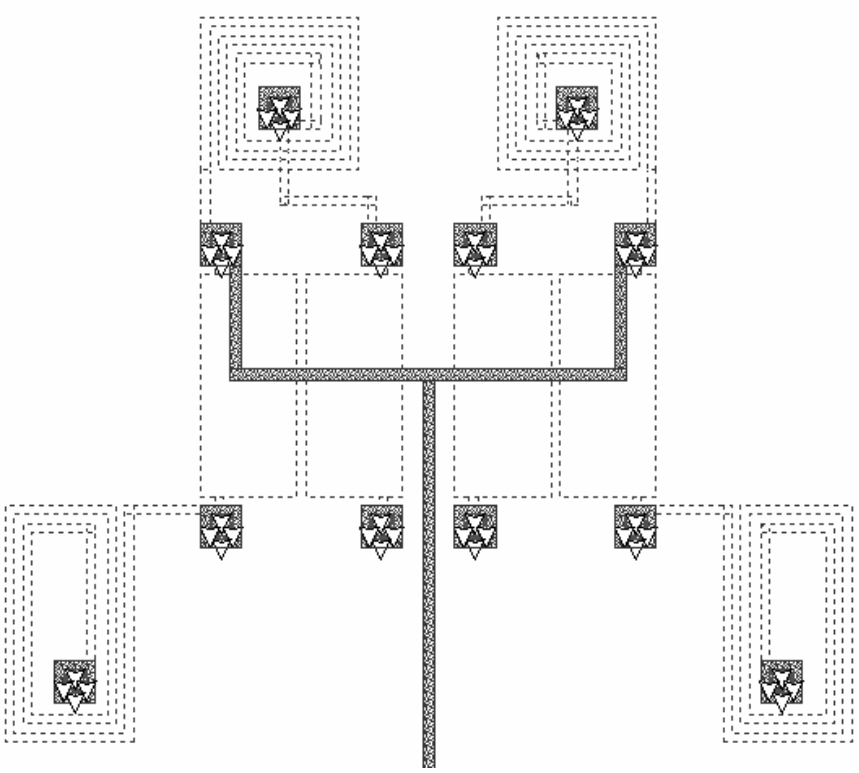


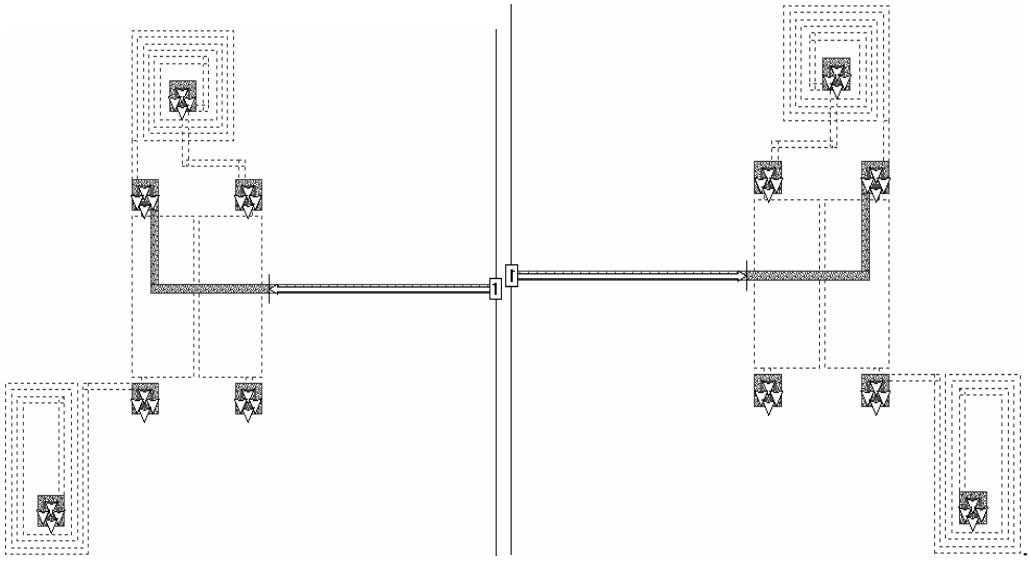
Figure 5.12. Schematic of a double doubly balanced mixer [63]

. The lumped baluns with 20 embedded passive components in multi-layer LCP substrates provide a compact-size mixer without performance degradation. The designed

mixer is composed of RF and LO baluns, which have two integrated lumped baluns, whose layouts are shown in Figure 5.13. The RF and LO baluns, which consist of two lumped baluns, were initially simulated by the circuit simulator, agilent advanced design system (ADS), with ideal components. Then, the designed baluns were simulated using an EM solver, SONNET [46]. The simulator cannot solve the entire RF or LO balun because of the electrically large size of the dual balun with a 3 mil minimum line width. This memory issue was solved by using the segmented simulation method, provided in the solver, as shown in Figure 5.13. Once all three simulations, including the simulation of the left half, the right half, and the feed line, were completed, the overall S parameter responses are shown in Figures 5.14 and 5.15.



(a)



(b)

Figure 5.12. Layout of LO balun and multi-section simulation in SONNET: (a) entire circuit and (b) multi-section simulation

Figures 5.13 and 5.14 shows the measured results of half of the LO and IF baluns, summarized in Table 5.1. For the LO balun, a 1 dB amplitude imbalance from 780 to 900 MHz was achieved. The main reason for the higher phase imbalance is the asymmetric layout of the compact mixer, which is discussed in the following section. Despite high S11, the IF balun achieved good amplitude and phase imbalance. The high S11 causes higher insertion loss. In Figures 5.13and 5.14 the circled lines represent the stimulation results, and the solid lines indicate the measurement results. Even though the S11s of both baluns were degraded, the S11 of the LO port still remains at less than -10 dB level.

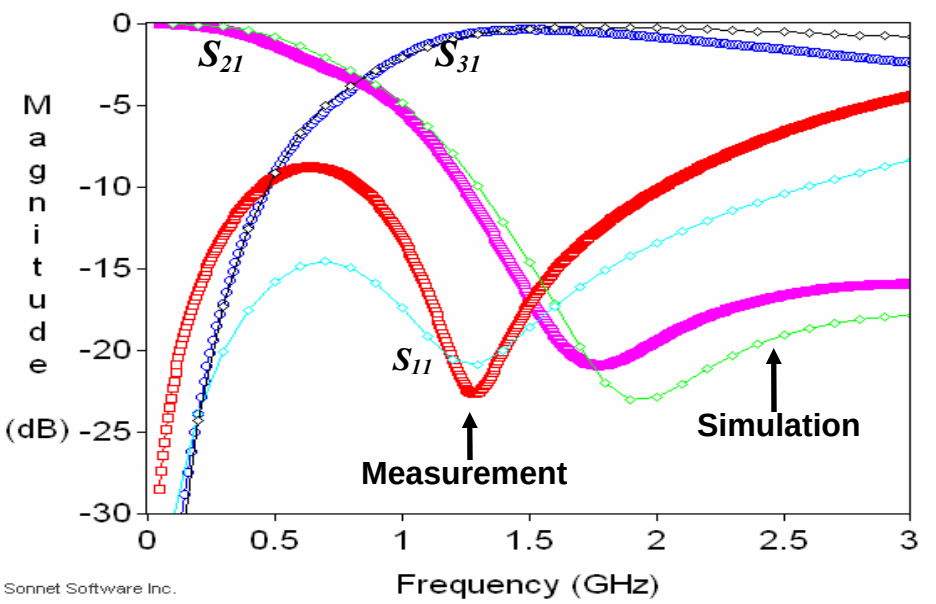


Figure 5.13. Measured S parameter results of LO balun

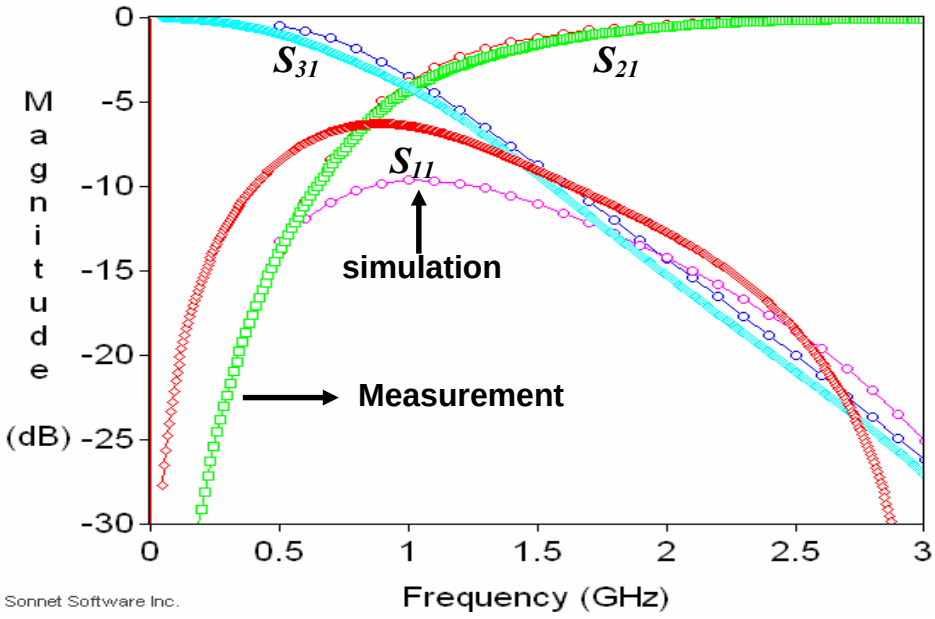


Figure 5.14. Measured S parameter results of IF balun

Table 5.1. Performance of the lumped baluns

Frequency (MHz)	840 (LO)	1000 (IF)
S11 (dB)	-10.1	-6.44
S21 (dB)	-3.64	-4.23
S31 (dB)	-3.74	-4.22
Amplitude Imbalance (dB)	0.21	0.1
Phase Imbalance (°)	9.2	0.2

Figure 5.15 shows the layout of the triple-balanced mixer and it also shows a X-ray picture of the designed mixer. In this picture, all 20 embedded inductors and capacitors can be seen, and a good layer-to-layer registration is also observed.

The previously designed lumped baluns with embedded passives were used for the mixer design, in which both the RF and LO baluns have dual baluns, while the IF balun has a single balun. Two Agilent HSMS-2829 silicon Schottky quad diodes, surface-mounted to the top and the bottom ground plane, were connected to the embedded baluns by thru-holes. A photograph of the fabricated double doubly balanced mixer is also shown in Figures 5.15. The size of the fabricated mixer is 7.9mm x 7.13mm x 2.1mm. Given the single diode size of 2.35mm x 2.9mm, the embedded passive technology with multi-layer LCP substrates played a key role in reducing the size and enhancing the performance.

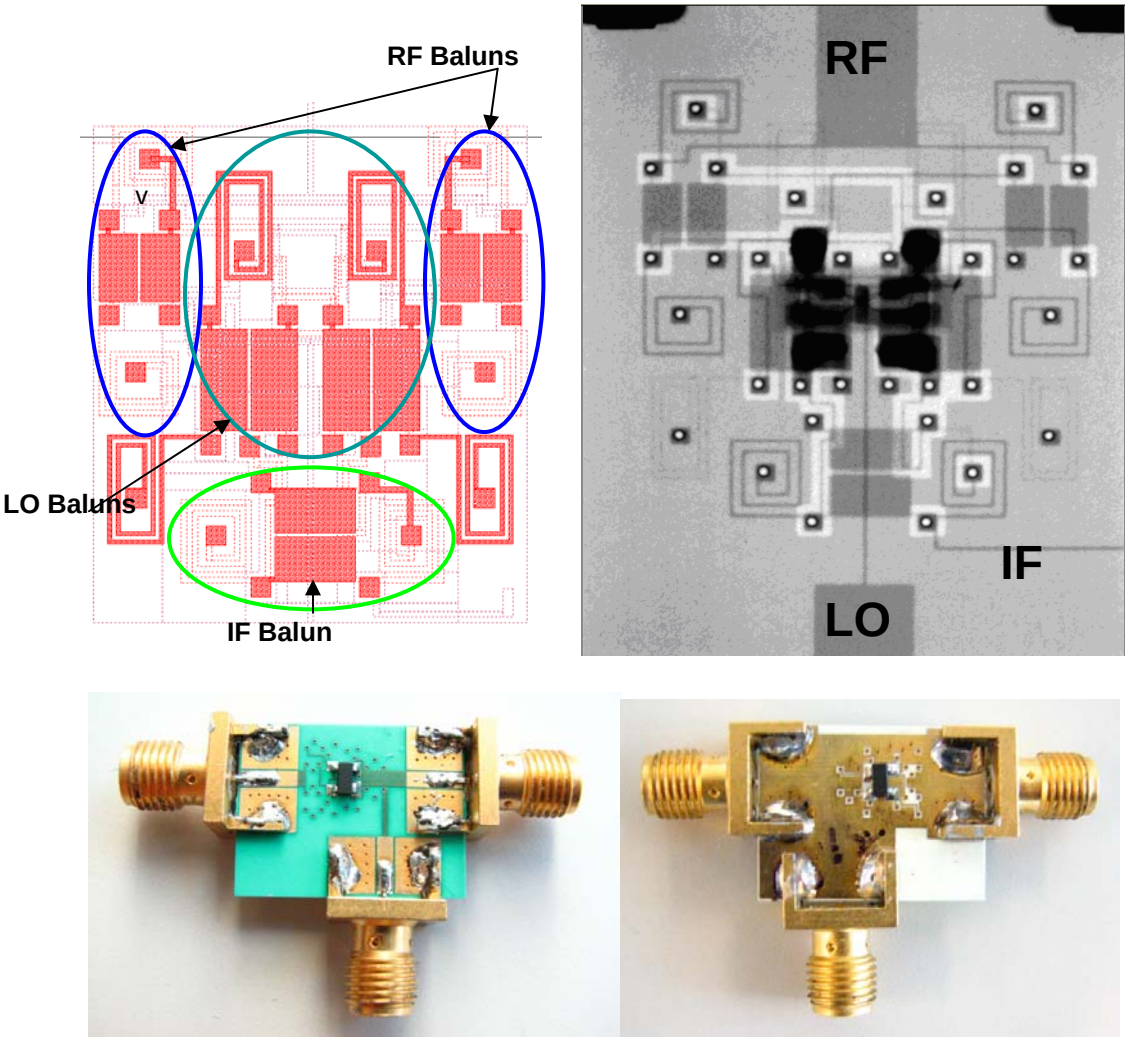


Figure 5.15. Layout, X-ray and photograph of the fabricated doubly double-balanced mixer

The measured performance of the mixer is presented in Figure 5.16, showing the conversion loss with 700 MHz IF frequency. An external signal generator provided the LO power of 13 dBm. The conversion loss from 6.3 dB to 8 dB occurred from 1260 MHz to 1490 MHz with an RF power of 30 dBm. Figure 5.17 shows approximately 6dB conversion loss with respect to the RF input power at 1430 MHz with the LO power of 13 dBm. The conversion loss of 7.1 dB with the RF power of 11 dBm resulted in an input P1dB compression point of 11 dBm.

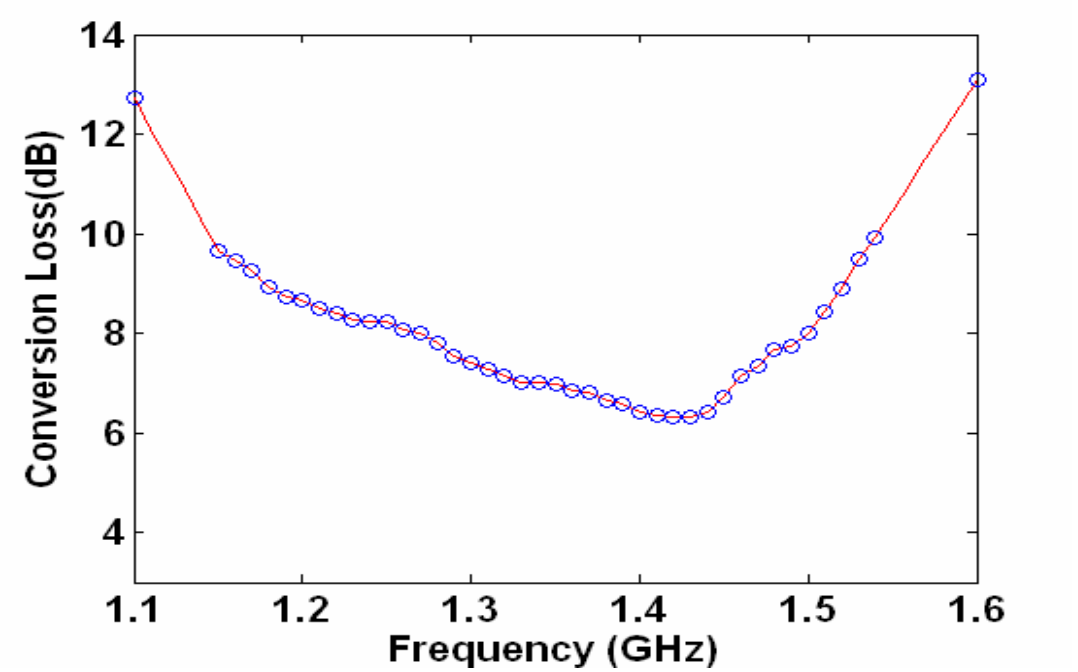


Figure 5.16. Measured performance of a doubly double-balanced mixer with embedded passive components: Conversion Loss vs. RF Frequency

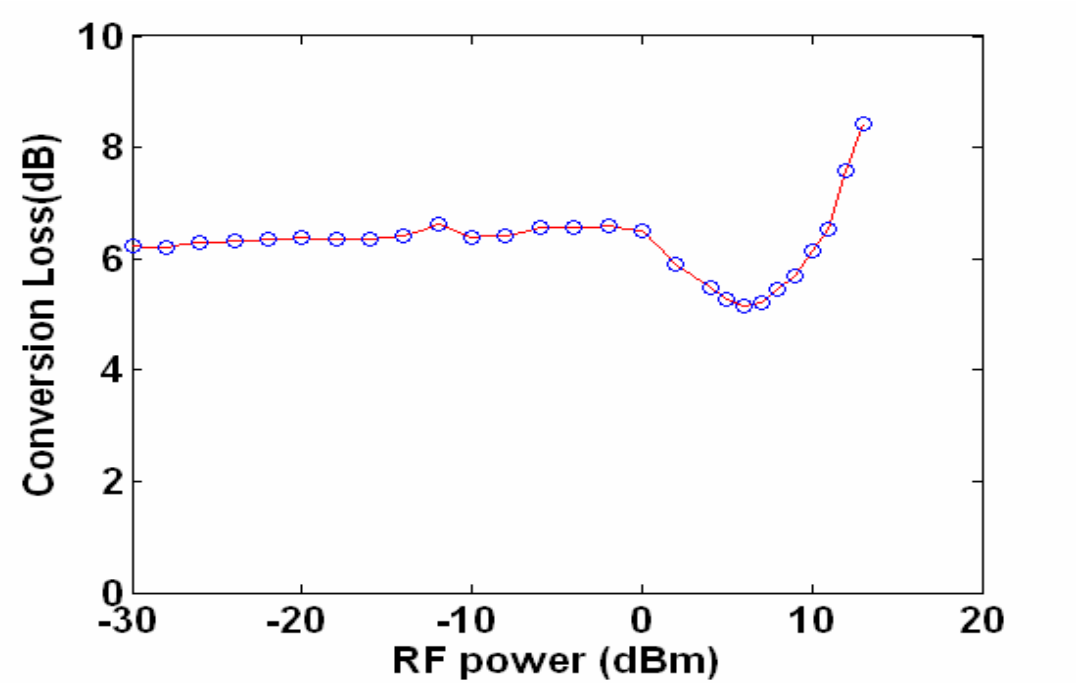


Figure 5.17. Measured performance of a doubly double-balanced mixer with embedded passive components: Conversion Loss vs. RF Power

Figure 5.18 shows the conversion loss variation with respect to IF frequency. From 600 to 920 MHz, better than 7 dB of the conversion loss was achieved. Better than 9 dB of the conversion loss was achieved from 480 to 960 MHz. Figure 5.19 shows the isolation of RF to LO and LO to IF. The isolation level of 20 to 35 dB from LO to RF and that of 20 to 46.8 dB from LO to IF were achieved. The designed double doubly balanced mixer was able to achieve at least 20 dB isolation when the RF and IF were overlapped. For the isolation of LO to RF, better than 24 dB isolation was achieved from 760 to 1900 MHz. Better than a 30 dB isolation level from the LO to the IF port was achieved from 480 to 1000 MHz. This high isolation was achieved mainly because of the baluns at each port.

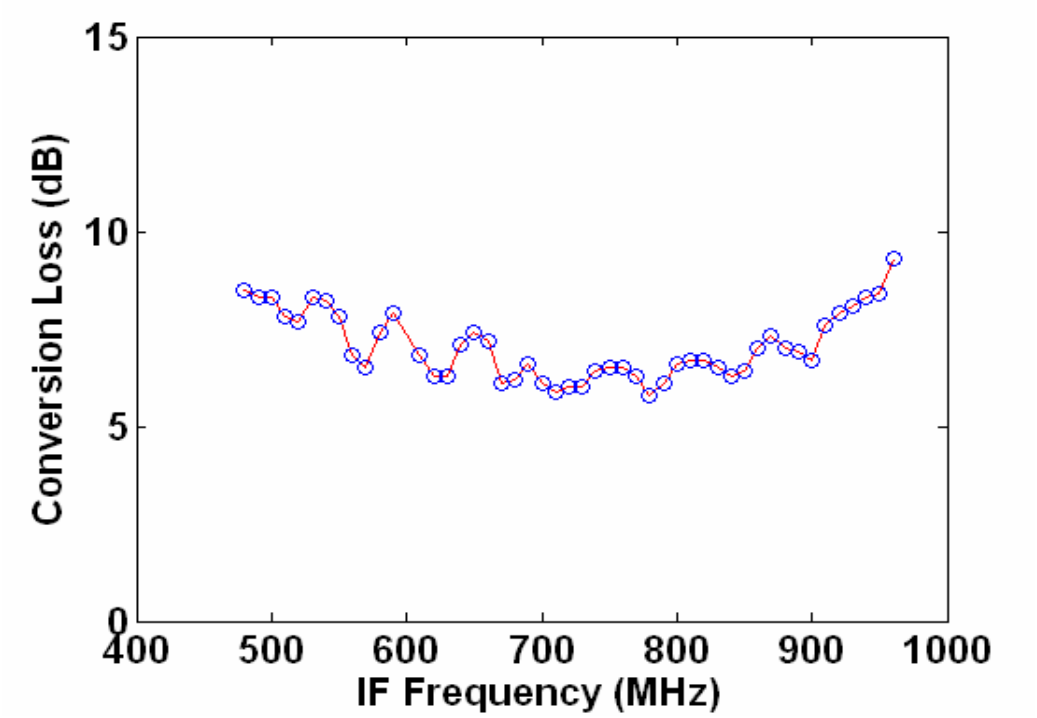


Figure 5.18. Measured performance of a doubly double-balanced mixer with embedded passive components: Conversion Loss vs. IF Frequency

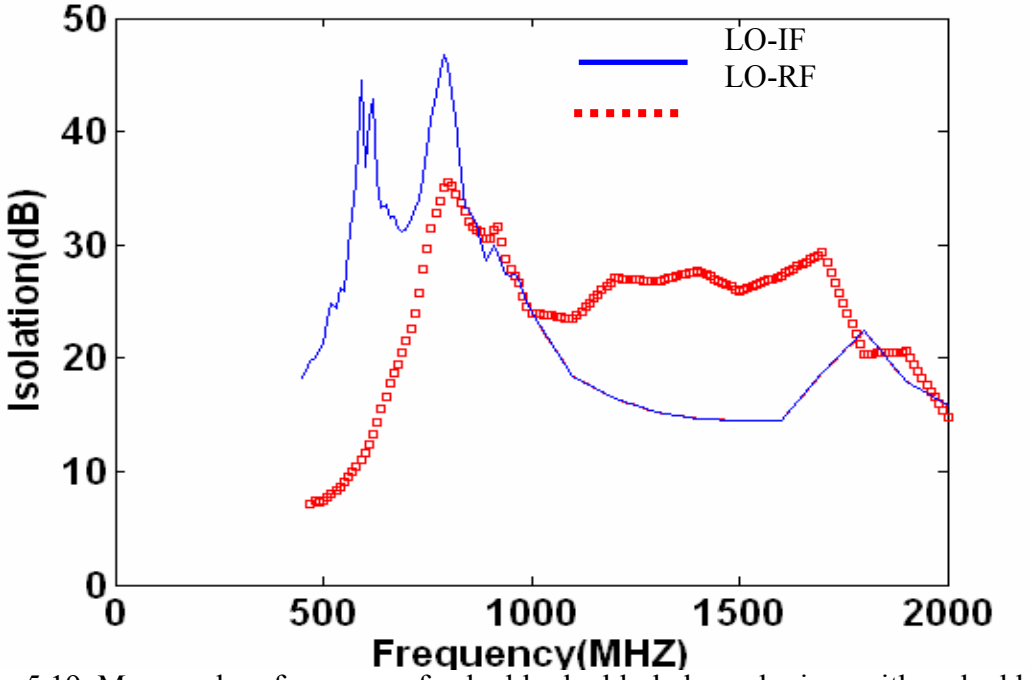


Figure 5.19. Measured performance of a doubly double-balanced mixer with embedded passive components: Isolation vs. RF Frequency

5.5. Design of 30 GHz Distributed Band-Pass Filter in Inhomogeneous Multi-layer LCP Substrates

The previous lumped element-based circuits are not suitable for frequencies above 10 GHz because of SRF limitations. The high-Q passive designs at 10 GHz are nearly infeasible because most inductors and capacitors approach the SRF at such high frequencies. This limitation can be overcome by a distributed-type design, which is presented in this section. One type of distributed filter is a gap-coupled filter whose schematic is shown in Figure 5.20. The design utilized the multi-layer structure to overcome the minimum line spacing so that a narrower gap could be achieved using locating the other transmission line on the other layer. This multi-layer configuration

could properly control the bandwidth, the insertion loss, and the transmission zeros in [64] and [65]. The design procedure for the filter is as follows. First, the prototype of low-pass filter was designed for the center frequency of 30 GHz and 0.5 dB ripple with 20 dB attenuation at 36 GHz. From [64], N=3 satisfies the attenuation specification. The low-pass prototype values are stated in the following equations.

$$Z_0 J_1 = \sqrt{\frac{\pi\Delta}{2g_1}} \tag{5-1}$$

$$Z_0 J_n = \frac{\pi\Delta}{2\sqrt{g_{n-1}g_n}}, \text{for, n} = 2, 3, ..., \text{N} \tag{5-2}$$

$$Z_0 J_{N+1} = \sqrt{\frac{\pi\Delta}{2g_N g_{N+1}}}, \tag{5-3}$$

$where \Delta = (w_2 - w_1)/w_0$ is the fractional bandwidth of the filter.

From the above equations, the following equations can provide coupling susceptances, capacitances, and resonator lengths.

$$B_i = \frac{J_i}{1-(Z_0 J_i)^2}, \qquad C_n = \frac{B_n}{w_0} \tag{5-4}$$

$$\phi_i = \pi - \frac{1}{2}\left[\left(\tan^{-1}(2Z_0 B_i\right) + \left(\tan^{-1}(2Z_0 B_{i+1})\right)\right]. \tag{5-5}$$

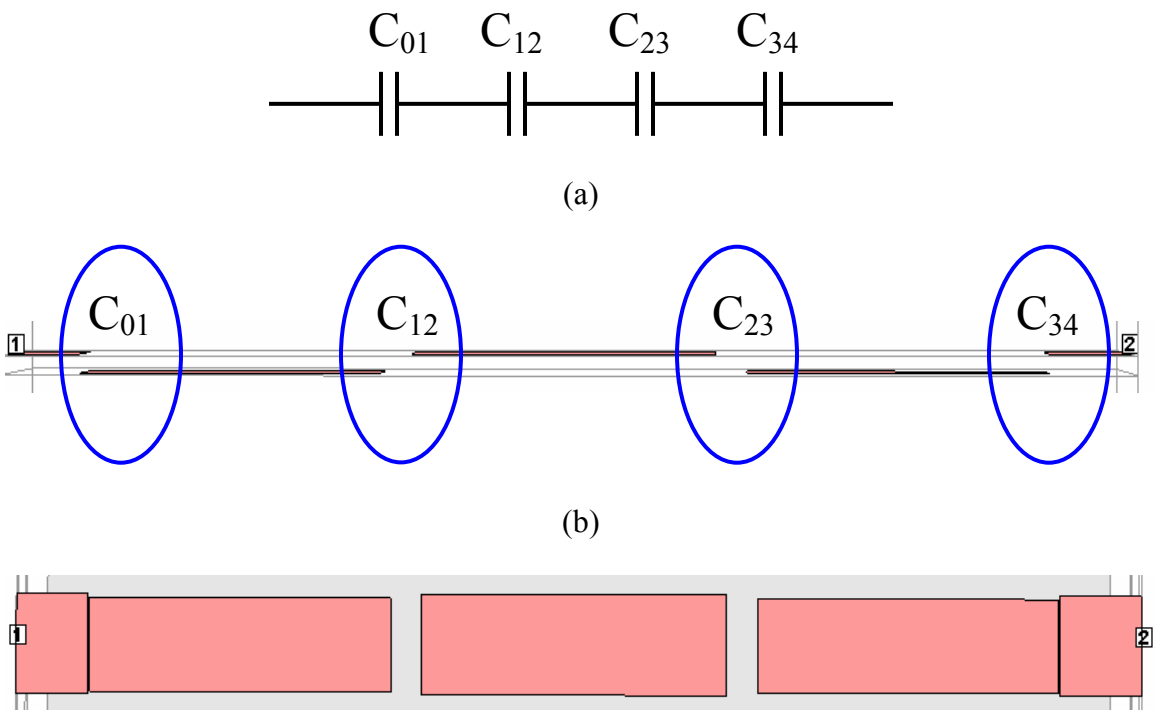


Figure 5.20. Schematic and cross-section of a gap-coupled band-pass filter with a layout in multi-layer LCP technology: (a) schematic, (b) cross section, (c) top view, and (d) stack-up

The calculated values are given in Table 5.2. The insertion loss in the simulated results was 1.38 dB, and the 3 dB bandwidth was from 26.7 to 32.1 GHz. The measured results indicate 2.28 dB of insertion loss, and 3 dB bandwidth of 24.8 to 30.4 GHz. The

frequency down shift of 6.67%, 2GHz, occurred from the simulation results, while the bandwidth of the measured results remained the same as that of the simulation results. The results are presented in Figure 5.21. The deviation from the simulation at 32.5 GHz came from calibration errors. The TRL calibration that was performed in Chapter 2 was applied to the revised design and the results show improved model-to-hardware correlation above 32.5 GHz, as shown in Figure 5.22. It had 2.48 dB insertion loss with 3 dB bandwidth ranging from 26.34 to 30.14 GHz. The center frequency was down- shifted about 1.9 GHz.

Table. 5.2.Design values of 30 GHz gap-coupled band-pass filter

N	g_N	$Z_0 J_n$	B_n	C_n	θ_n
1	1.5963	0.4209	$1.0229\text{x}10^{-2}$	$5.4267\text{x}10^{-14}$	148.3
2	1.0967	0.2137	$4.4783\text{x}10^{-3}$	$2.373\text{x}10^{-14}$	159.0
3	1.5963	0.2137	$4.4783\text{x}10^{-3}$	$2.373\text{x}10^{-14}$	148.3
4	0	0.4209	$1.0229\text{x}10^{-2}$	$5.4267\text{x}10^{-14}$	

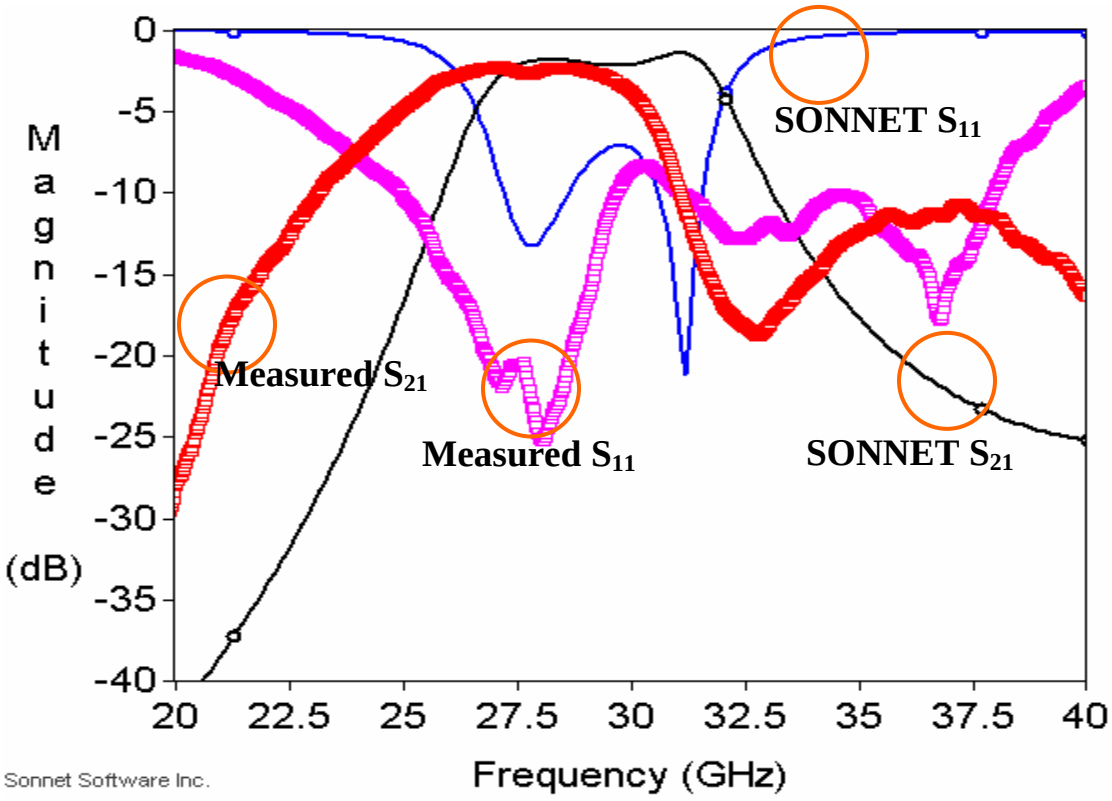


Figure 5.21. Simulated and measured results of 30 GHz gap-coupled band-pass filter

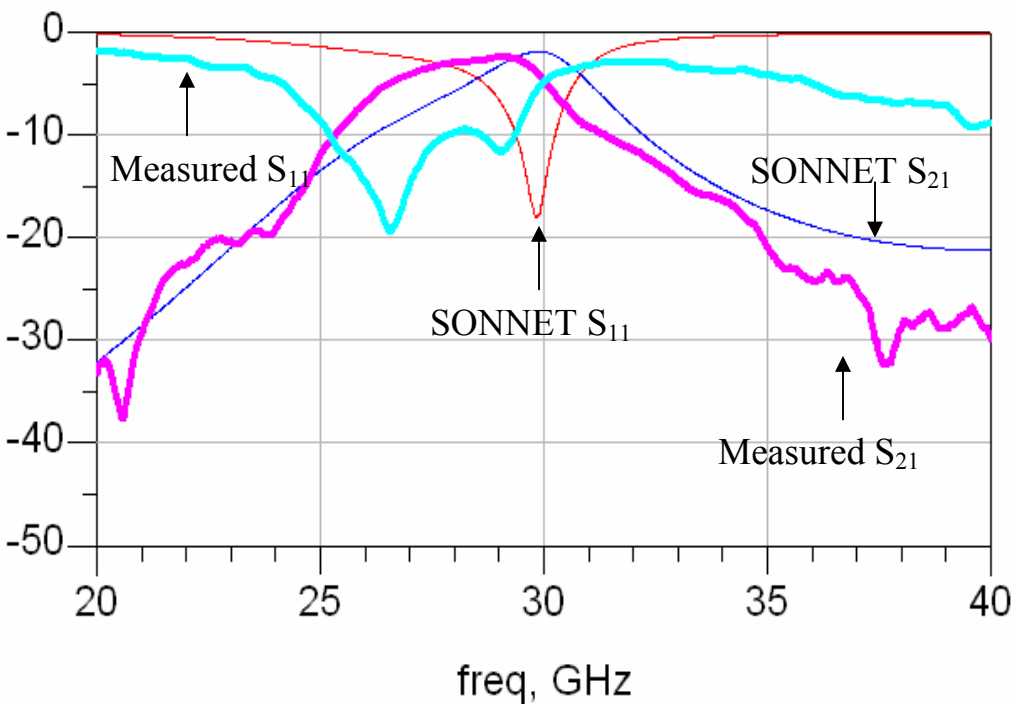


Figure 5.22. Model-to-hardware correlations of 30 GHz gap-coupled band-pass filter after TRL calibration

5.6. Summary

Various RF front-end modules have been designed and implemented using high-Q embedded passive components in inhomogeneous multi-layer LCP substrates. A C-band filter using lumped elements has been designed and measured. The lumped baluns were used to design a double balnced-mixer for 5 GHz WLAN application and a doubly double-balanced mixer for 1.78 GHz CDMA receiver miniaturization. Finally, to overcome the limitations of the lumped component circuits, a 30 GHz gap-coupled band-pass filter in inhomogeneous multi-layer LCP substrates, and the measured results using SOLT and TRL calibrations have been compared to the simulation results.

CHAPTER 6

CONCLUSION AND FUTURE WORK

Increasing demands in small, high performance, multi-functional wireless communication systems have resulted in new system platform, system on package (SOP) for integration of RF front-ends. The completely integrated wireless systems can be realized using a low loss, low cost, and high quality organic material, liquid crystalline polymer (LCP) substrate. Inhomogeneous multi-layer LCP substrate provides high-Q embedded passive components with low cost and low profile because of an excellent loss dielectric loss, a low water absorption, and a large area batch process. In this dissertation, the characterization of the inhomogeneous LCP stack-up has been performed and the characterization of the embedded passive components is also presented. The validation for large area batch process has also been conducted. In addition, the measurement-based via characterization using periodic arrays of vias were proposed. Finally, various RF front-end modules was developed using the characterized stack-ups and embedded passives.

6.1. Conclusion

Based on the work presented in Chapters 2 through 5, the contributions of this research can be listed as follows:

(a) The characterization of inhomogeneous multi-layer LCP substrates has been performed. The embedded transmission lines in the multi-layer

substrates were characterized and attenuations per unit length were extracted. To validate the inhomogeneous multi-layer LCP substrates as a high-frequency material, characterized loss characteristics were compared with other high-frequency materials such as FR-4, LTCC and homogeneous LCP substrate.

(b) A two-port characterization method based on measurements of multiple arrays of vias has been proposed. The method overcomes the drawbacks of the one-port and other two-port characterizations. A single measurement decreases the residual inductances and contact resistances, and the arrays of the vias average the process variations of the vias. Three TV's are measured using the TRL calibration, which ensures the proper de-embedding of the feeding structures. The S parameters along with the propagation constants of the entire structures have been shown. Finally, the series inductances and parallel capacitors were extracted. The characterized values, compared among the different TV's and coupons, showed consistent values. A comparison of the extracted inductances and capacitances, S parameters, and propagation constants with those of the simulated results by Ansoft HFSS, a 3D full-wave solver, provided the model-to-hardware correlations. The resulting correlations show that this method can be readily applied to other vertical interconnects besides via structures.

(c) Comprehensive characterizations have been conducted for the efficient 3D integration of high-Q passives using a balanced LCP substrate. At two different locations from three different large M-LCP panels, 76 inductors

and 16 3D capacitors were designed and measured. Inductors on different layers (the top and third layers) clearly showed the scalability of Q, ranging from 43 to 164. In addition, the measured results show very little variance over the two different locations in each TV and among the three different TVs. Finally, the parameters for the measurement-based inductor model were extracted from the measured results. The results validate the large panel process of the M-LCP substrate. To reduce the lateral size, multi-layer 3D capacitors were designed. The designed 3D capacitors with inductors can provide optimized solutions for more efficient RF front-end module integration. In addition, the parameters for the measurement-based capacitor model were extracted. Critical inductors for high performances can be achieved with the highest Qs in the top-most layer, while other inductors can be embedded on other layers. As discussed in this chapter, 3D capacitors can reduce the size more effectively than general parallel-plate capacitors. In addition, a two-step de-embedding technique was applied to remove the effect of pads and thru-hole interconnections. This technique resulted in closer correlations between simulation and measured results.

(d) Various RF front-end modules have been designed and measured using high-Q embedded passive components in inhomogeneous multi-layer LCP substrates. A C-band filter using lumped elements has been designed and measured. The lumped baluns were used to design a double balnced-mixer for 5 GHz WLAN application and a doubly double-balanced mixer for 1.78

GHz CDMA receiver miniaturization. Finally, to overcome the limitations of the lumped component circuits, a 30 GHz gap-coupled band-pass filter in inhomogeneous multi-layer LCP substrates, and the measured results using SOLT and TRL calibrations have been compared to the simulation results.

6.2. Future Works

The proposed methodologies to characterize inhomogeneous multi-layer LCP substrates can be extended to characterize new stack-ups. The measurement-based via characterization using the periodic arrays of vias can also be extended to characterize a differential interconnects. The consideration should be given to the tight coupling between the interconnects, and therefore, new modeling method to analyze the coupling can be investigated. In addition, the embedded passive technology and high-performance module design can be investigated in the system level to realize complete wireless system.

6.3. Publications

The following publications and invention disclosures have resulted during the course of the research.

- **Wansuk Yun**, Kijin Han, and Madhavan Swaminathan, "The Measurement-Based Via Characterization using Periodic Arrays of Vias from 1 to 40 GHz," to be submitted to *IEEE Trans. Microwave Theory and Tech.,* Oct. 2007
- **Wansuk Yun**, Venky Sundaram, and Madhavan Swaminathan, "Characterization of Inhomogeneous Multi-layer Liquid Crystalline Polymer Substrates," submitted to *IEEE Trans. Adv. Packaging,* Mar. 2007

- **Wansuk Yun**, Venky Sundaram, and Madhavan Swaminathan, "A Triple Balanced Mixer in Inhomogeneous Multilayer LCP substrates," presented at *Electro. Comp. and Technl. Conf., R*eno, NV, pp. 2000-2005, June 2007
- **Wansuk Yun**, Venky Sundaram, and Madhavan Swaminathan, "High-Q Embedded Passives on Large Panel Multi-layer Liquid Crystalline Polymer Based Substrate*," IEEE Trans. Adv. Packaging*, vol. 30, pp. 580-591, Aug. 2007
- **Wansuk Yun**, Amit Bavisi, Venky Sundaram, Madhavan Swaminathan, and Ege Engin, "3D integration and characterization of high-Q passives on multi-layer liquid crystalline polymer based substrate," in *Proc. Asia-Pacific Microwave Conf.*, Suzhou, China, pp. 327-330, Dec. 2005 **(Best Paper Award)**
- **Wansuk Yun**, Vinu Govind, Sid Dalmia, Venky Sundaram, Madhavan Swaminathan, and George White, "An Integrated Double Balanced Mixer on Multi-layer Liquid Crystalline Polymer Based Substrate," in *Proc. IEEE European Microwave Conf.*, vol.3, pp.1635-1638, Oct. 2005
- Amit Bavisi, **Wansuk Yun**, Venky Sundaram, Madhavn Swaminathan, "Design and applications of high-Q passive devices on multi-layered liquid crystalline polymer based substrates for handset applications," in *Proc. Asia-Pacific Microwave Conf.*, Suzhou, China, pp 1295-1298, Dec. 2005
- Vinu Govind, **Wansuk Yun**, Venky Sundaram, Madhavn Swaminathan, Sidharth Dalmia, George E. White, "Analysis and design of compact wideband baluns on multi-layer liquid crystalline polymer based substrates," in *Proc. IEEE Microwave Symp. Digest,* Long Beach, CA, pp. 543-547, June 2005

- Madhavn Swaminathan, Amit Bavisi, **Wansuk Yun**, Venky Sundaram, Vinu Govind, and Monajemi, P. "Design and fabrication of integrated RF modules in liquid crystalline polymer substrates," *Industrial Electronics Society, IECON 2005*, pp. 2346-2351, Nov. 2005

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