Modeling of Power Supply Noise in Large Chips using the Finite Difference Time Domain Method

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Modeling of Power Supply Noise in Large Chips using the Finite Difference Time Domain Method

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Chapter I

Introduction

The trend in electronic systems is towards faster transition speed, larger I/O count and higher circuit densities due to advances in fabrication technology. As a consequence, many signal integrity problems become increasingly important for design engineers [1,2]. Simultaneous switching noise falls into two categories, namely, I/O noise due to I/O switching and core noise due to internal logic switching. In the past, only I/O noise had been a major concern due to its association with signal and power integrity problems, while, since onchip inductance was considered negligible, core noise had less importance in the design of the system. However, today's high performance microprocessor has brought out the importance of on-chip inductance for the power and ground rails on a chip, necesitating a more hierarchical modeling of the system distributing power to the switching circuits.

Simultaneous switching noise characteristics and noise reduction methods have been investigated over many years for the design of high performance devices [3]-[5]. Also, for predicting the noise in electronic systems, numerous methods have been developed using equivalent circuit models [6]-[8].

This chapter briefly describes the details of the power distribution system for large chips, the simultaneous switching noise generated in highly integrated electronic systems and the proposed research.

I.1 Power Distribution System

As mentioned earlier, simultaneous switching noise (SSN) has become an important issue for maintaining the integrity of signals. This noise can be attributed to the parasitics in the power delivery system (PDS) of the chip, package (PKG), and printed circuit board (PCB). In modern CMOS technology, the design of the power delivery system is one of the most challenging areas in the implementation of future electronic systems.

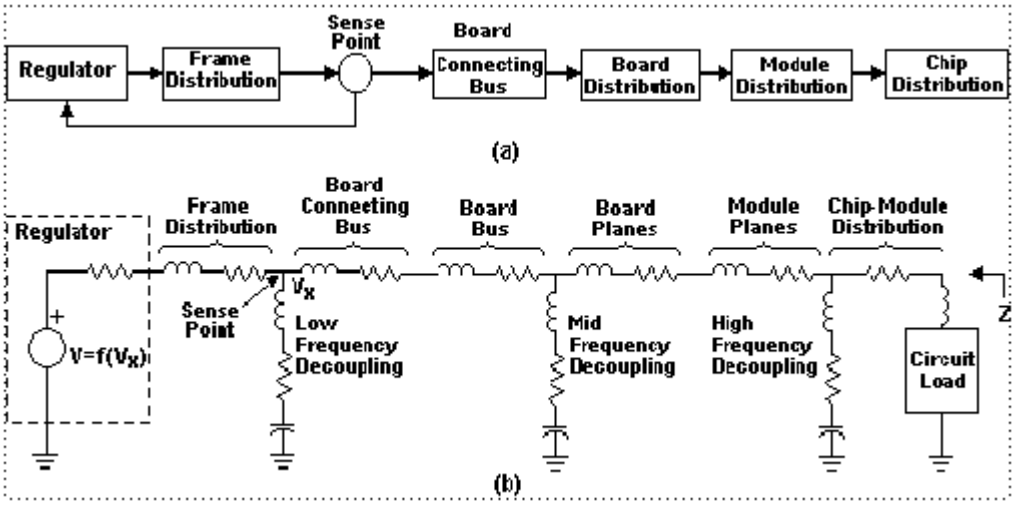


Figure 1.1.(a) Block diagram for typical power distribution system
(b) Equivalent circuit

A typical power distribution system for a high speed digital system is illustrated in Figure 1.1. The board configuration and the impedance seen from the chips over a frequency band for this system is shown in Figure 1.2 [3]. A large amount of decoupling capacitance is inserted between the regulated voltage supply and the boards for filtering the low frequency components of the current changes [9].

Capacitor card slots shown in Figure 1.2 are for accommodating low frequency decoupling capacitors. The first peak in the impedance plot in Figure 1.2, which is associated with the low frequency noise, is related to the time constants of the power regulator module, decoupling capacitors on the capacitor card and the capacitance at the power regulator output. This behavior should therefore be included in the modeling of DC voltage regulation for estimating the system performance. Sufficient low frequency capacitance is required to minimize the amplitude of this peak.

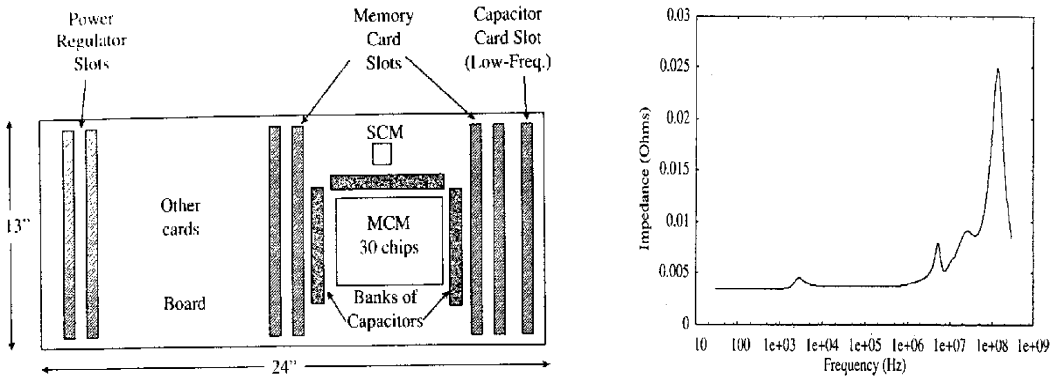


Figure 1.2. Layout of the back-plane of a system and the impedance seen from the chip circuit

Mid-frequency decoupling capacitors are mounted near the module(s) on the board (banks of capacitors in Figure 1.2) to filtering noise associated with charge in the current which flows from the module to the board. The second peak in the impedance plot represents mid-frequency noise and is controlled by the interaction of the first level package, the multi chip module (MCM) or single chip module (SCM) and the board into which it is plugged. This impedance peak is larger in amplitude in the frequency domain, but the effects are more localized

than the low frequency noise. The circuits can be sensitive to the voltage gradients at this frequency. Sufficient decoupling capacitance is therefore needed to minimize the noise in the mid-frequency range.

High frequency decoupling capacitors are located on the module or in the chips to decouple the current flowing from the chips to the module planes through vias. The third peak in the impedance plot, a result of the interaction between the chip and the first level package, is primarily dependent on the switching activity in the chip. Although this is the largest peak, the current change through this impedance is much smaller than the other two peaks. Dedicated on-chip decoupling capacitors and tightly coupled voltage and ground plane pairs are utilized to minimize this impedance. Each level of the system therefore requires decoupling to control the impedance and limit the noise amplitude. Hence, capacitors with low series inductance and resistance are required for proper decoupling of the system.

I.1.a Simultaneous switching noise (SSN) in a system

Simultaneous switching noise(SSN) is caused by the switching of logic in a digital system. It consists of voltage spikes which appear at the power supply terminals of the chip in response to switching activity of the logic circuits. To prevent the spikes from causing intermittent logic errors during the operation of the digital circuitry, the magnitude of these spikes must be below the noise tolerance of the logic family used [9]. SSN is caused by the inductance in the power distribution network of the chip, package and printed circuit board. This

finite inductance limits the speed at which the current is supplied to the switching circuits.

As an example, Figure 1.3 shows a set of active simultaneously switching OCDs (off chip drivers) modeled as a set of parallel transmission lines and one quiet (nonswitching) OCD connected to a single transmission line. In Figure 1.3, 300 CMOS external circuits are driving the transmission lines from low to high. When these drivers switch, a negative-going differential voltage(V_{DD} - V_{GND}) appears across the package inductance. This noise has two effects on the operation of the off-chip drivers, namely, larger net delays and loss of data at the receiver. The noise voltage generated by the simultaneous switching of N output drivers can be calculated using the equation

$$\Delta V = NL_{eff}\,\Delta i / \Delta t \qquad (1.1)$$

where L_{eff} is the effective inductance of the power and ground connection, $\Delta i / \Delta t$ is the peak rate of change of current, Δi is the current required by each driver during the switching event, and Δt is the rise or fall time of the signal. Thus, the magnitude of SSN is proportional to the total power supply current slew rate of the driver and the effective inductance of the power supply path. All of this simultaneous switching can cause hundreds or even thousands of milivolts (mV) of noise between the power supply voltages (V_{DD} and GND) [11]-[13]. When the amplitude of this noise approaches one-half of the CMOS signal swing (V_{DD}), which is the approximate noise tolerance of a static CMOS circuit, a signal error can occur. As CMOS drivers become faster, the noise glitches on the power

supply rails can increase in future systems, unless the power distribution network is designed appropriately.

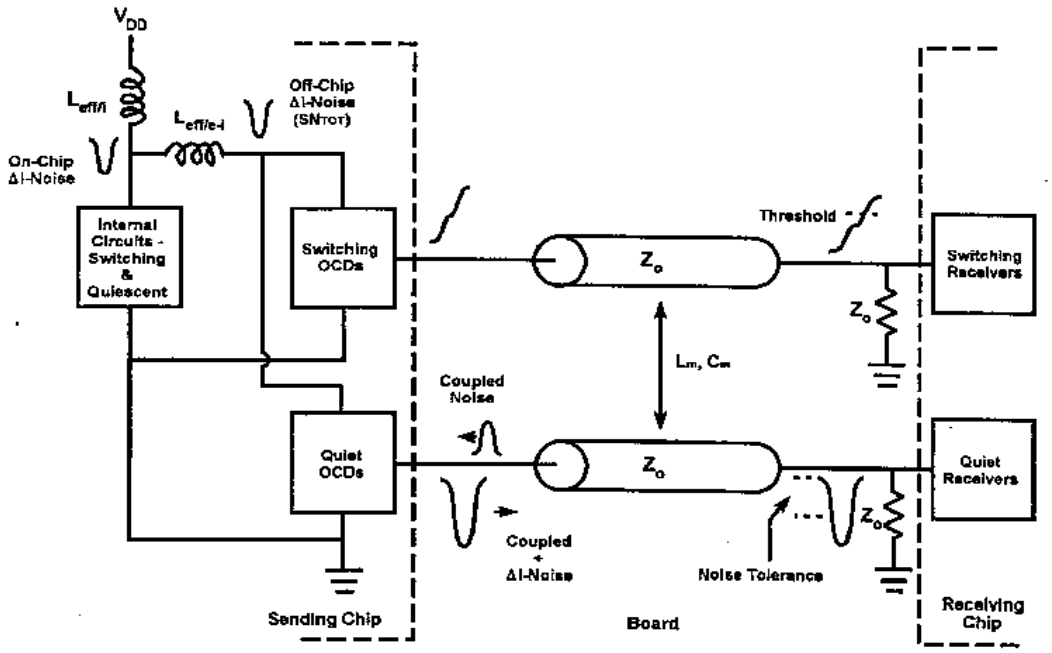


Figure 1.3. Causes and effects of Switching and Coupled Noise on Signal Lines[10]

I.1.b Delay due to SSN

When a large number of simultaneously switching circuits create a sufficient amount of differential power-supply noise such that the effective voltage across the switching circuits is reduced by a large percentage of its VDD value (greater than 30% of VDD for static CMOS circuits), then the circuit will slow down as the FET overdrive (V_{gate} -$V_{threshold}$) voltage is reduced. This causes the current slew rate (di/dt) to reduce, thereby reducing the incremental noise generated by the circuit. Upon this occurence, circuit delay increases. Hence, this condition should

be avoided by controlling the noise or by accounting for additional delay in the circuit.

I.1.c Logic error due to SSN

SSN can cause data errors to occur. Refering again to Fig.1.3, the negative noise generated by the OCDs causes a spurious signal to propagate through the quiet drivers and the transmission lines they are connected to, ultimately appearing at the quiet receiver's input [10]. When this noise exceeds the receiver's noise tolerance, the receiver's output will be greater than its input. As a result, the noise can travel through the logic circuits that the receiver is connected to, growing in amplitude until it finally sets a down stream latch in the wrong state, a system datum error. Depending on the type of CMOS circuits used, this type of datum error may or may not be recoverable. For static circuits, delaying the latch clock signal allows the noise to dissipate before the latch captures the error. This causes the system to slow down. For dynamic CMOS circuits, however, the data errors may not be recoverable because in many instances the clocks are self-generated and not adjustable. The use of " pulse-catching" circuits may also lead to nonrecoverable noise errors. For these cases, if the noise occurs at a critical time, changing the system clock rate will not necessarily allow the noise to time-out before a datum error occurs. For systems that use dynamic logic, the careful control of noise within acceptable levels in the system is therefore required.

I.1.d Considerations for SSN suppression

In Equation (1.1), L_{eff} is a figure of merit used to express the goodness of a package. There are two different values of L_{eff} for on-chip and off-chip circuits due to the difference in the current loop, namely, L_{effi} and L_{effe}. L_{effi} is generally smaller than L_{effe} because the current loop for the internal circuits in the SCM (single chip module) is made up of a large number of tightly coupled power and ground vias and planes, whereas the external current path consists of longer and more loosely coupled signal, power, and ground paths. A good methodology is therefore required in order to minimize the package power distribution L_{eff}. Minimizing L_{eff} requires that VDD and GND planes and vias are plentiful and placed very close to each other to maximize the mutual inductance between them. In the case of the off-chip current loop, the signal lines should be tightly coupled to the power and ground planes and vias for the same reason. For clock rates over 150MHz, it is a good practice to uniformly alternate the power (P), ground (G), and signal (S) conductors in P-G-S-P-G-S pattern for vias and connector pins. This mutually couples the power and ground paths and the signal paths together with the power and ground conductors shielding the signal conductors from each other to minimize cross talk. This pattern, however, is rarely feasible because it requires a 1:2 signal - to - power ratio. For module vias and contacts, the following top view pattern is desirable : .... S-G-S-S-G-S ... , ...S-P-S-S-P-S ... . Using these principles of negative mutual inductance coupling and capacitive shielding, a pattern that is optimum for a particular design can be chosen. L_{eff} can also be reduced through the use of decoupling capacitors [14].

They should be placed on the chip or as close to the chip (die) as possible on the package, to minimize the series inductance and resistance.

I.2 Dissertation Outline

The proposed research consists of the development of a numerical technique for the simulation of power supply noise in modern CMOS systems containing large chips. Due to the importance of the interaction between the chip-package and package-board for computing power supply noise, a method has been proposed for the simulation of the entire system consisting of the chip, package and printed circuit board. The method being proposed is the Finite Difference Time Domain (FDTD) method which has been applied to the circuit equations representing the power distribution network. Since the method is circuit-based, non-linear sources can be included in the simulator. The research consists of the following:

1. Modeling of multi layered on-chip power grids using FDTD method

The smaller wire spacing, combined with the longer wire length in large chips, the faster switching speed, shorter cycle time, and smaller power supply voltage, have led to significant noise problems in today's high performance circuits. In particular, the switching noise problem due to inductances, which traditionally only occurred on the package, can no longer be ignored at the chip level. Using circuit based FDTD, a large network representing the on-chip power grid has been constructed and simulated for computing the peak noise distribution [37]. The electromagnetic propagation of the power supply noise in large chips has

been quantified through numerous simulations. This analysis is important for determining the substrate coupling and placement of decoupling capacitors on the chip.

2. Modeling of non-linear current sources

Although, in Eq.(1.1), the power supply noise is linearly proportional to the current slew rate, this expression can give erroneous results for large noise voltages. This is because excessive power supply noise decreases the current slew rate due to the non-linear characteristics of the switching circuits. This is called the negative feed back effect [34,38] which can only be captured by including the non-linear behavior of the switching circuits.

In this study, a non-linear current source model has been developed for CMOS integrated circuits which has been simulated using FDTD. This model has been verified through comparison with SPICE, followed by the simulation of thousands of nonlinear circuits drawing power from a multi-layered interconnection network. Using the H-tree clock topology, various simulation results such as differential peak noise distribution, noise waveforms with different decoupling capacitance, peak noise with variable load capacitances and relationship between clock buffers and rise time have been computed. These simulations help in quantifying the usefulness of the FDTD method for these kinds of problems.

3. Analysis of bus structures

Devices driving long on-chip buses generate power supply noise based on the path of the return currents in the power distribution network. This is caused

due to the mutual inductance and coupling capacitance between the signal lines and the power bus. This problem is ideally suited for analysis using FDTD. FDTD algorithms which includes the mutual inductance and coupling capacitance have been developed and used to simulate long on-chip bus lines with emphasis on the causality of the solution.

4. Package and board power distribution

Due to the fast switching speed of circuits that result in sudden current demands, noise is generated in the system that can gate performance. A major source of this noise can be attributed to the power delivery system (PDS) of the package and board, which, if poorly designed, can result in ground bounce, power supply compression and electromagnetic inference (EMI). The effect of noise is amplified for small supply voltages that can lead to excessive increase in circuit delay, clock skew and PLL jitter. For future CMOS systems, one methodology to suppress noise is to design the PDS by identifying a target impedance that has to be met over a broad frequency range.

An integral part of the power distribution network in high-speed systems are planes in packages and boards. The physical phenomena occurring due to radial wave propagation [41-44] effects have been studied. Based on the cavity resonator model used for a single plane pair, a method for extending the model to multiple planes has been discussed in this dissertation [40]. This has been verified through measurements. The effect of decoupling capacitors on the power delivery system for gigahertz packages and boards has been studied by connecting them to the package planes [47].

5. Modeling package and board planes using FDTD

The cavity resonator model for multiple planes developed in the previous section has been implemented using FDTD method in this dissertation. This has been combined with the flip chip inductance, via inductance and solder ball inductance to capture the vertical and lateral parasitic inductance/capacitance in the package and board power distribution network.

6. Co-simulation of chip, package and board

An important effect that is often neglected in the computation of power supply noise is the interaction between the chip-package and package-board. This interaction can cause additional resonances in the system. If these resonances have sufficient magnitude and are triggered during system operation, excessive noise can be generated in the system. The purpose of the co-simulation is to capture these resonances that are otherwise absent when each section of the system is analyzed separately. The interaction between the various components of the power distribution network has been modeled using the FDTD method in this dissertation.

7. Simulation of wafer level chip scale package on an integrated board

Wafer level packages (WLP's) are defined as packages that are less than 1.2 times the size of the chip. WLP's offer a smaller foot print, lower parasitics and more inputs/outputs per unit area than a ball grid array, resulting in better electrical performance. As an application, the FDTD method has been applied to a wafer level chip scale package assembled on an integrated, high-density

printed circuit board in the dissertation. The results have been analyzed to understand the various interactions in the system hierarchy.

The remainder of this dissertation is organized as follows.

1. Chapter 2 presents modeling of multi-layered on-chip power grid using the FDTD method. In this chapter, the method has been verified through a simple example. The FDTD method has been applied to on-chip power grid simulation to demonstrate the characteristics of noise propagation and the effectiveness of on-chip decoupling capacitors.
2. In Chapter 3, a method for including the CMOS inverter characteristics within the FDTD simulation is presented. This model has been verified by comparing it with SPICE, followed by a large network simulation with both linear and nonlinear circuits. As an example of the application of this method, an H-tree clock network has been simulated to compute the power supply noise distribution across an entire chip. Scenarios with varying decoupling capacitances, load capacitances, number of clock buffers and rise time were analyzed to demonstrate the importance of circuit non-linearity on power supply noise.
3. In Chapter 4, the FDTD algorithm, which includes the mutual inductance and coupling capacitance, is discussed and used to simulate long on-chip bus lines.
4. Chapter 5 discusses package and board power distribution with emphasis on power planes. Using the cavity resonator model for a single plane pair,

the method has been extended to multiple planes using skin effect approximation.

5. The cavity resonator model for multiple planes developed in Chapter 5 has been implemented using FDTD in Chapter 6. This incorporates flip chip inductance, via inductance and solder ball inductance to capture both the vertical and lateral parasitic inductance/capacitance in the package and board power distribution network.
6. In Chapter 7, the FDTD method has been applied to a wafer level chip scale package assembled on an integrated, high-density printed circuit board being developed at the Packaging Research Center. The results have been analyzed to understand the various interactions in the system hierarchy.

Finally, the conclusion and comments on future work are discussed in Chapter 8.

Chapter II

Modeling of Multi-Layered On-Chip Power Grid using the FDTD Method

With the trend towards deep sub-micron technology, state-of-the-art interconnection feature sizes have been reduced to 1um or less. The smaller wire spacing, combined with the longer wire length in large chips, faster switching speed, shorter cycle time, and smaller power supply voltage, have led to significant noise problems in today's high performance circuits. In particular, the switching noise problem due to inductance, which traditionally only occurred on the package, can no longer be ignored at the chip level [15]. In addition, based on the International Technology Roadmap on Semiconductors (ITRS), future microprocessors are expected to be 30mm by 30mm in size, which is larger than a wavelength at 10 GHz. As clock frequencies approach 10 GHz, large chips can support electromagnetic waves, resulting in radiation and interference effects. These effects can occur through the power distribution network in the chip, package and board. Therefore, modeling the on-chip power grid and package power distribution as a distributed electromagnetic system is important.

For modeling the distributed effects of on-chip power grids, H. Chen *et al.* [16] from IBM have used a unit cell approach. The basic idea behind this

approach is the use of iso-potential areas within the chip. Hence the chip is first divided into many iso-potential areas. An equivalent circuit is generated for each iso-potential area to model the power supply fluctuations [9]. This method, though simple, creates an artificial boundary between areas and also assumes that the noise is uniform within an iso-potential area. This approximation can lead to erroneous results for large chips operating at high frequencies.

L. Zheng *et al.* [55] proposed a modeling technique for on-chip power distribution analysis for advanced ULSI circuits. The authors have modeled the power lines as a linear network of distributed RLC elements excited by constant voltage sources and switching capacitors. Based on the model, equations for peak noise and noise distribution are formulated and used to capture the on-chip distributed effect. However, this approach has a limitation on the grid size and has difficulty in the inclusion of the interaction between on-chip power grid and on-chip bus.

The simulation of very large networks consisting of large numbers of nodes is a major problem in the design of integrated circuits. Circuits of this size can typically require several days of CPU time on a workstation. Schutt-Aine [17] has developed the LIM (latency insertion method) for the simulation of large networks using the FDTD method. In his work, a finite difference formulation and reactive latency at all branches and nodes of a circuit were used to generate an update algorithm for the voltage and current quantities in the network. However, this method is currently limited to 2D electrical structures.

In this chapter, the LIM using the FDTD method has been extended to multi-level power grids. In this method, a branch capacitor has been used, which is different from [17]. The use of the branch capacitor is important for simulating multi-layered power grids. The current in the branch capacitor is extracted from Kirchhoff's current law. This provides a good model of the branch capacitor and does not require any latency and companion models during simulation.

This chapter is organized as follows. Section 1 describes the conventional FDTD (finite difference time domain) method and its application for solving circuit equations. Section 2 discusses the verification of the proposed method through a simple example. Section 3 discusses the on-chip power grid simulation, the characteristics of noise propagation and the effectiveness of on-chip decoupling capacitors. This is followed by a summary in Section 4. In this dissertation, the dimensions used in the power distribution network do not represent realistic dimension. In addition, the four level of metalization is used which may not represent the high level operating chip. Instead the goal of this dissertation is to demonstrate the feasibility of modeling large chips.

II.1 Finite Difference Time Domain method

The FDTD method, first presented by Yee in 1966 [18], numerically solves Maxwell's equations in the time domain on a spatial grid [19]. Because of its computational efficiency, accuracy and direct physical reference, the FDTD method has become increasingly popular for computation of electromagnetic wave propagation and scattering effects [20-22], including the FDTD analysis of

microwave circuits [23]. Also, the FDTD method has been successfully applied to MTL (Multi-conductor Transmission Lines) equations [24,25] and LIM (Latency insertion Method [17]) equations for solving the circuit equations. However, the FDTD method has a problem in the inclusion of loss effects such as skin effect, which varies with frequency with a $\sqrt{f}$ dependence. The representation of this frequency dependence in the time domain is a convolution that presents computational problems in a direct, time–domain solution [26]. In this chapter, the skin effect has been neglected. Instead, the focus of this chapter is on the simulation of large on-chip power distribution networks using the FDTD method.

A Modified Nodal Analysis (MNA) based SPICE simulator can create problems for simulating the on-chip power grid consisting of millions of passive elements. A primary reason is that it needs a matrix inversion requiring huge memory and computation time even though a sparse matrix technique can be used.

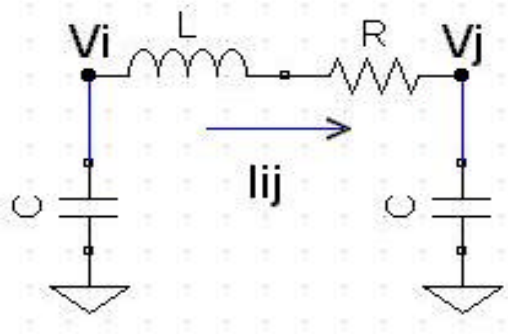


Figure 2.1 p -type equivalent circuit of a small-sectioned transmission line

An FDTD based solution for a passive network starts from the well-known p type equivalent circuit for a small-section of transmission line. From Figure 2.1,

applying Kirchhoff's law yields

$$V_i - L\frac{di_{ij}}{dt} - Ri_{ij} - V_j = 0 \qquad (2.2.a)$$

$$i_{ij} + C\frac{dV_i}{dt} = 0 \quad \text{for Node i} \qquad (2.2.b)$$

$$i_{ji} + C\frac{dV_j}{dt} = 0 \quad \text{for Node j} \qquad (2.2.c)$$

where V_i is the voltage at i-th node, V_j is the voltage at j-th node, i_{ij} is the current flow from i-th node to j-th node and C is the node capacitance.

Using the central difference approximation for time derivative as in the Yee algorithm [18], Eq. (2.a-c) can be written as

$$i_{ij}^{n+1} = i_{ij}^{n} + \frac{\Delta t}{L}(V_i^{n+1/2} - V_j^{n+1/2} - Ri_{ij}^{n}) \qquad (2.3.a)$$

$$V_i^{n+1/2} = V_i^{n-1/2} + \frac{\Delta t}{C} i_{ij}^{n} \qquad (2.3.b)$$

$$V_j^{n+1/2} = V_j^{n-1/2} + \frac{\Delta t}{C} i_{ji}^{n} \qquad (2.3.c)$$

In Eq. 2.3(a)-(c), the branch current and node voltage are calculated to update the values at time $n\Delta t$ and $(n+1/2)\Delta t$, respectively, where n is an integer. Using a technique similar to [17], the updating algorithm for the node voltages can be generalized for multiple branches as

$$V_i^{n+1/2} = V_i^{n-1/2} - \frac{\Delta t}{C}\sum_{k=1}^{M} i_{ik}^{n} \qquad (2.4)$$

where M is the number of branches connected to Node i. For multi-layered on-chip power grids, a branch capacitor between nodes can be included to update the voltage and current, as shown in Figures 2.2(a) and (b). This representation for multi-layered structures is different from the latency insertion method (LIM) proposed in [17].

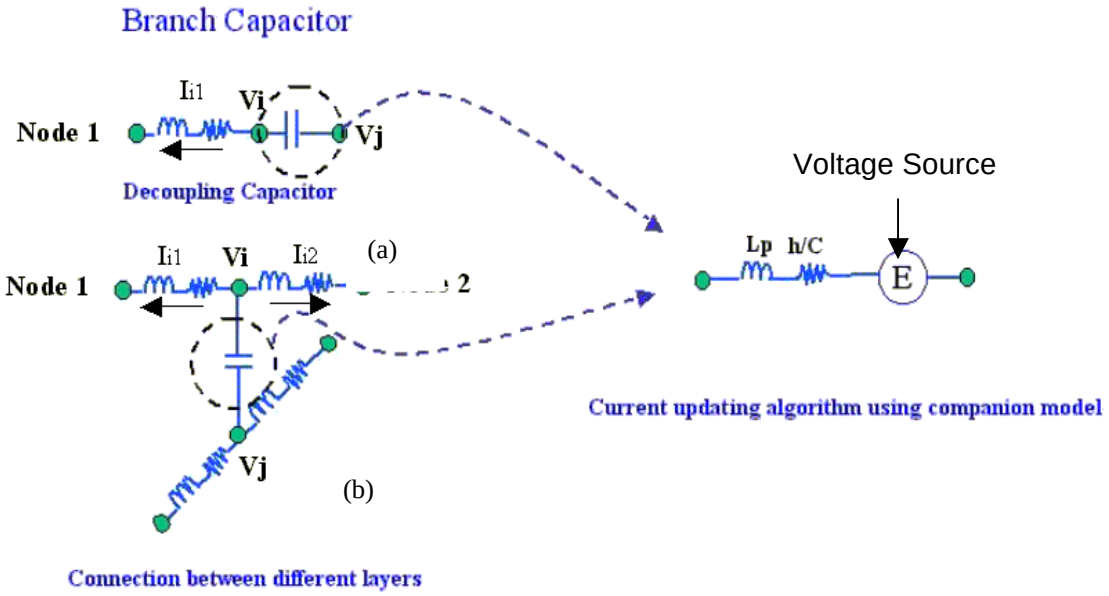


Figure 2.2 (a) Decoupling capacitor implemented as a branch capacitor
(b) Sandwiched capacitor between different layers implemented as a branch capacitor
(c) Companion model for a branch capacitor in LIM [17]

The branch capacitor in LIM (Latency Insertion Method) has been modeled using a companion model [27] with a finite difference approximation. This approximation is based on the Backward Euler formula or trapezoidal formula that is well known for approximating derivatives. The reason for the use of a companion model is because every branch requires current information for updating the node voltages. The usage of the companion model can lead to

erroneous results due to its incompatibility with the central difference based finite difference operator.

Numerical instability is an undesirable problem in finite difference modeling that can cause the computed results to spuriously increase without limit as time marching continues. According to [17], the condition for the numerical stability can be written as

$$\Delta t < \sqrt{LC} \tag{2.5}$$

where Δt is the time step, L is the inductance in a branch and C is the capacitance at a node. This inequality can be considered as a causality condition in tracking a propagation signal through a lattice of circuit elements. Eq. (2.5) is analogous to the Courant-Friedrichs-Lewy (CFL) criterion for wave propagation in a discrete grid and defines the upper bound on the time step, Δt , for computational stability while applying the FDTD based method.

II.2 Modeling the Branch Capacitor

The problem with LIM mentioned in the previous section can be solved using a branch capacitor as shown in Figure 2.2(a) and (b). Using the branch capacitors, the current at the next time step can be updated using the currents in neighboring branches by means of Kirchhoff's current law. This method completely eliminates the need for latency and companion model for the branch capacitor and gives a much better model of a branch capacitor. From Figure 2.2(a) and (b), the node voltages and branch currents for the branch capacitor can be written as

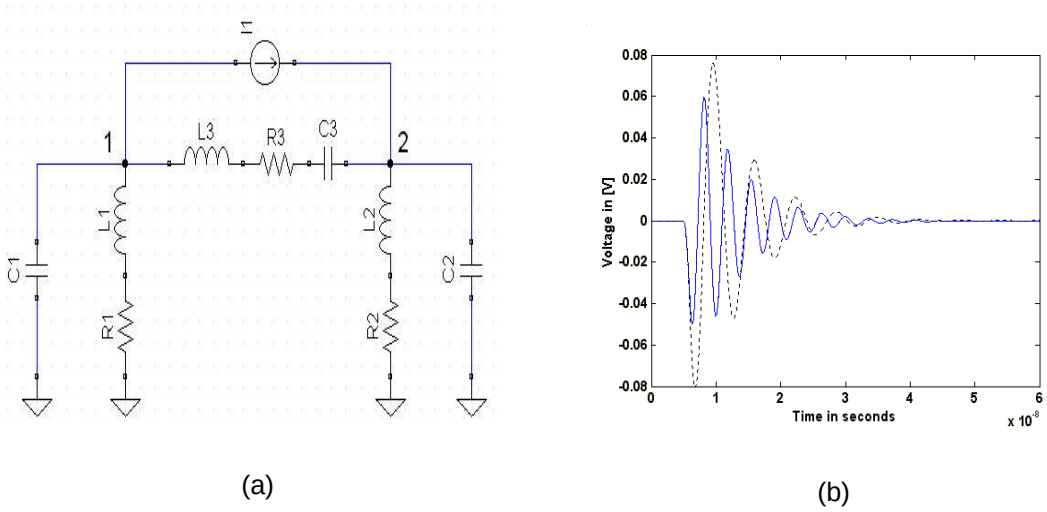
$$V_i^{n+1/2} = V_i^{n-1/2} + (V_j^{n+1/2} - V_j^{n-1/2}) - \frac{\Delta t}{C} \sum_{k=1}^{M} i_{ik}^{n} \qquad (2.6.a)$$

$$i_{ij}^{n+1} = \sum_{k=1}^{M} i_{ik}^{n+1} \qquad (2.6.b)$$

Figure 2.3(a) shows a simple example for the verification of the use of a branch capacitor to model multi-layered structures arising in on-chip power distribution network. In Figure 2.3(a), R1, R2, L1, and L2 are resistances and inductances of the power and ground rails. Capacitors C1 and C2 are the sandwiched capacitors between multiple levels. Components, C3, L3, and R3 are the capacitance, inductance and resistance of the on-chip decoupling capacitors. In Figure 2.3(a), the current source mimics a switching CMOS circuit. Figure 2.3(b) shows the noise waveforms measured at Node 1 using HSPICE, the proposed model, and the companion model in [17]. From Figure 2.3(b), it can be seen that good correlation has been obtained between HSPICE and the proposed model while the noise waveform from the companion model shows discrepancy with the results from HSPICE. The error is mainly due to the incompatibility of the interlaced FDTD algorithm with the interrelated finite difference approximations such as Backward Euler formula and Trapezoidal formula.

II.3 On-chip power distribution network

The on-chip power distribution network distributes power and ground voltage from C4 bumps to all gates and devices in a microprocessor. Higher device densities and faster switching frequencies cause large switching currents to flow in the power ground networks which degrade performance and reliability [28].



(a) (b)

Figure 2.3. (a) Example circuit for the branch capacitor
Current source: magnitude=0.1A, rising time=100ps and falling time=200ps
R1, R2, R3 = 0.3 Ohm, L1, L2, L3 =1nH, C1, C2 = 1nF, C3=0.1uF
(b) Transient voltage at Node 1
Dashed dot line: proposed approach, Solid line: HSPICE
Dotted line: Companion model in [17]

As mentioned earlier, the parasitic inductances from C4 bumps to the top metal layer have become very important in the design of power distribution system for high performance microprocessors. This is because large amounts of power have to be distributed through a hierarchy of many metal layers. Thus the detailed modeling of on-chip power grids is essential for understanding the power distribution effects in modern high performance microprocessors. Figure 2.4(a) and (b) show a power grid network consisting of 4 metal layers. The power grid is connected to the power supply using C4 technology. The four levels of metal are assumed to have continuous voltage and ground lines across the chip. The first and second metal layers have alternating voltage and ground lines that are 3 um wide on 60 um pitch. The third metal layer has 6 um wide lines on 120 um pitch,

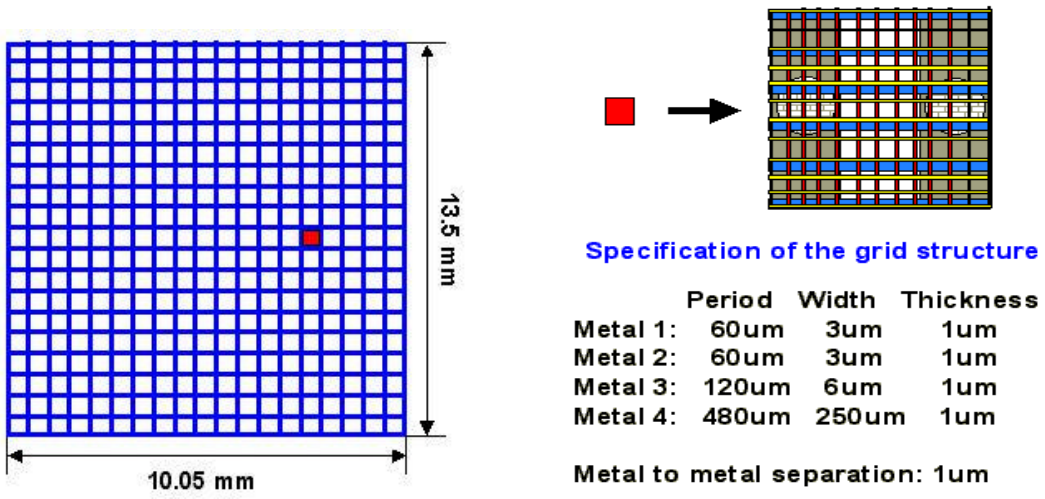


Figure 2.4(a) On-chip power grid structure (b) Detailed description of a unit cell

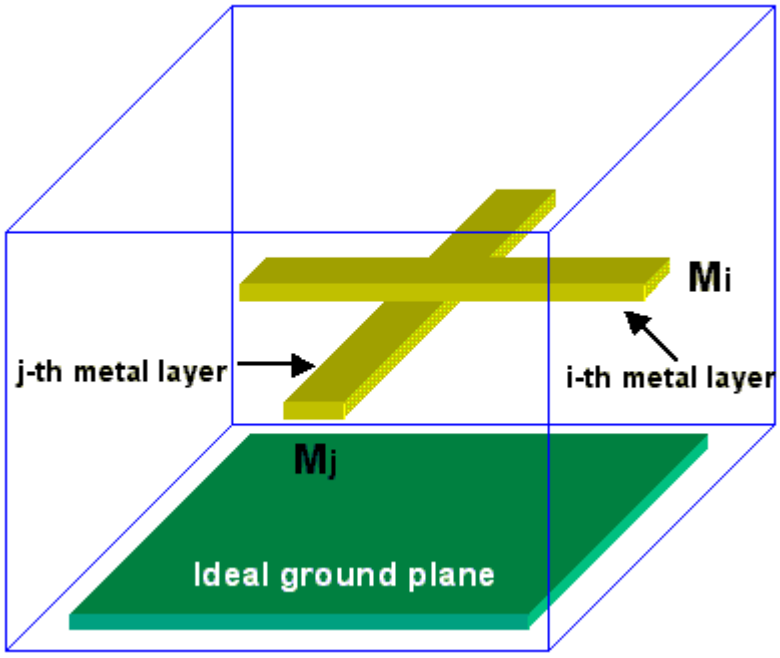


Figure 2.5 Small section of power grid used in ANSOFT MAXWELL 3D

and the fourth metal layer has 250 um wide lines on a 480 um pitch to match the periodicity of the area array foot print, 480um, that attaches the chip to the package. The size of the network is 13.5 X 10.5 mm^2 containing 0.5 million circuit elements, which is a realistic representation for modern microprocessors. In Figure 2.4, the power supply is assumed to be at the bottom of the C4 vias. The R, L, and C values were extracted using 3D field solver, namely, MAXWELL3D as shown in Figure 2.5 and were implemented into the FDTD based program. The extracted parameters are summarized in Table II.1. In Figure 2.5, it was assumed that the metal grids are embedded in silicon dioxide (e_r =3.6), the dimension of the metal box is 1cm in width, length and height, the ideal ground plane is 50um far from the small section of power grid, the metal used is copper (conductivity s : $5.8x10^5$ S/cm) and the length of the sectioned metal line follows the periodicity of the on-chip power grid.

Tabel II.1 Line parameters of the on-chip power grid used for the simualtion

	Resistance	Inductance	Capacitance
1^{st} metal layer	0.345 Ohm	47.2 pH	3.36 fF
2^{nd} metal layer	0.345 Ohm	47.2 pH	3.36 fF
3^{rd} metal layer	0.172 Ohm	41.2 pH	4.8 fF
4^{th} metal layer	0.345 mOhm	21.2 pH	45 fF

II. 3.a Characteristics of the on-chip power grid

One current source was placed at the center of the on-chip power grid to study the characteristics of the power grid. The current source has a rise time of

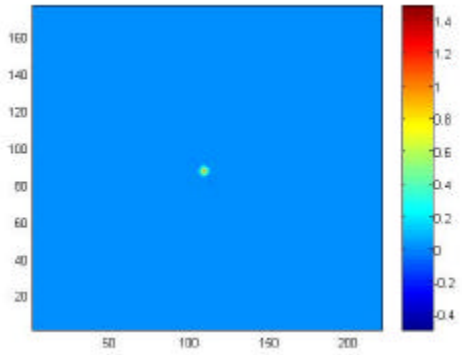


Figure 2.6(a) At t=110ps

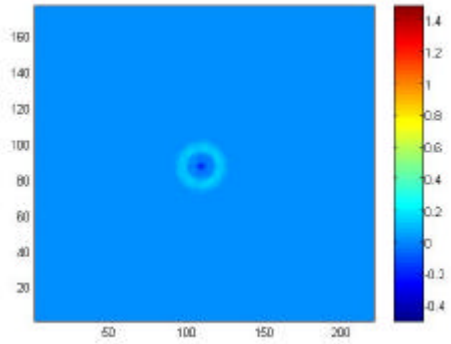


Figure 2.6 (b) At t=310ps

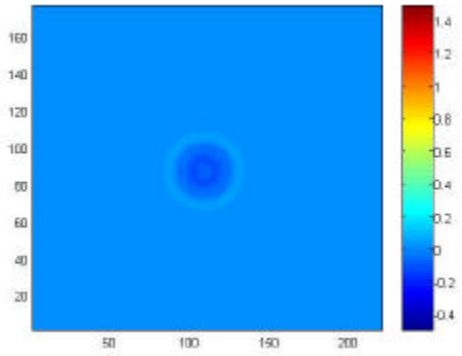


Figure 2.6 (c) At t=450ps

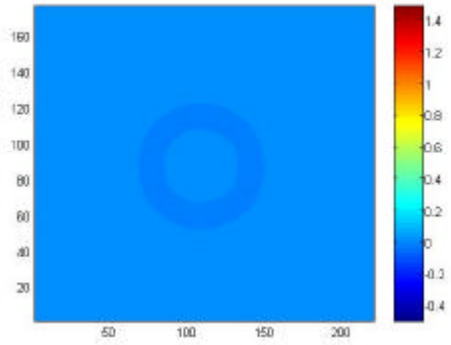


Figure 2.6 (d) At t=750ps

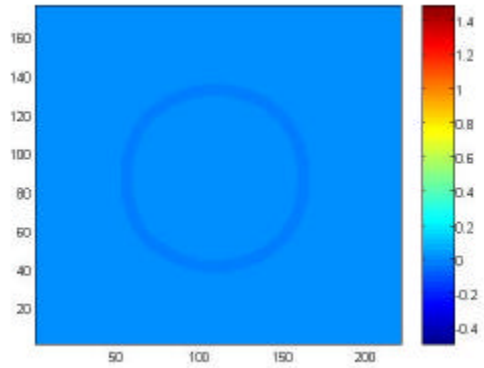


Figure 2.6 (e) At t=1000ps

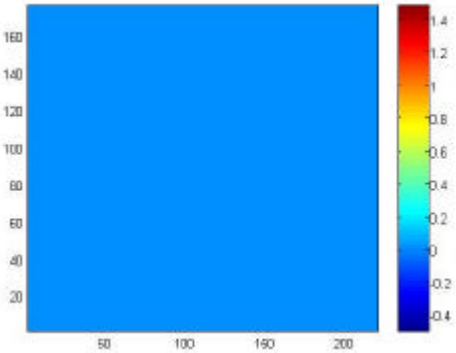


Figure 2.6 (f) At t=1160ps

Figure 2.6 Snap shots of the radial wave propagation due to single source excitation at the center of the on-chip power grid

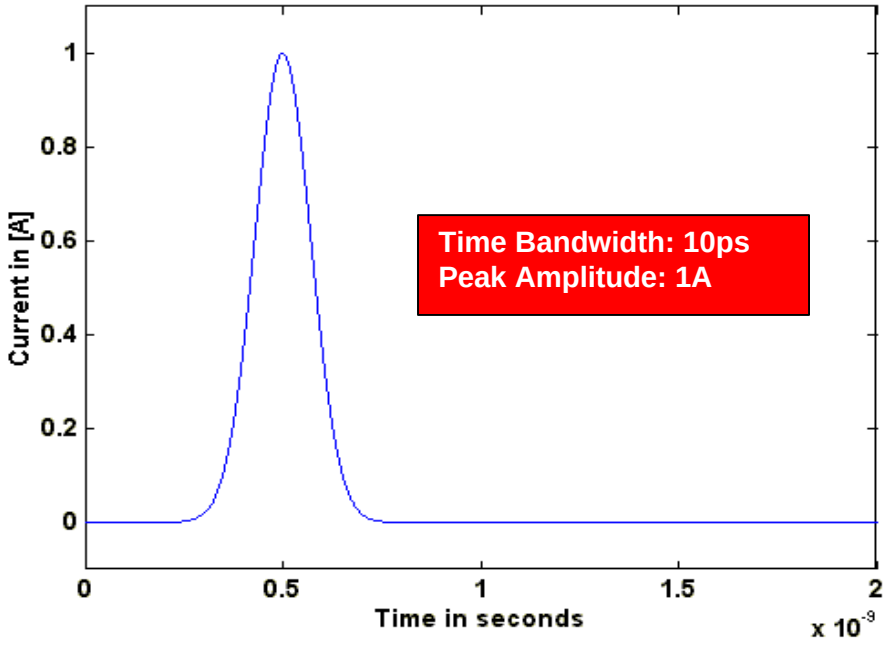


Figure 2.7(a) Gaussian current pulse used for the simulation

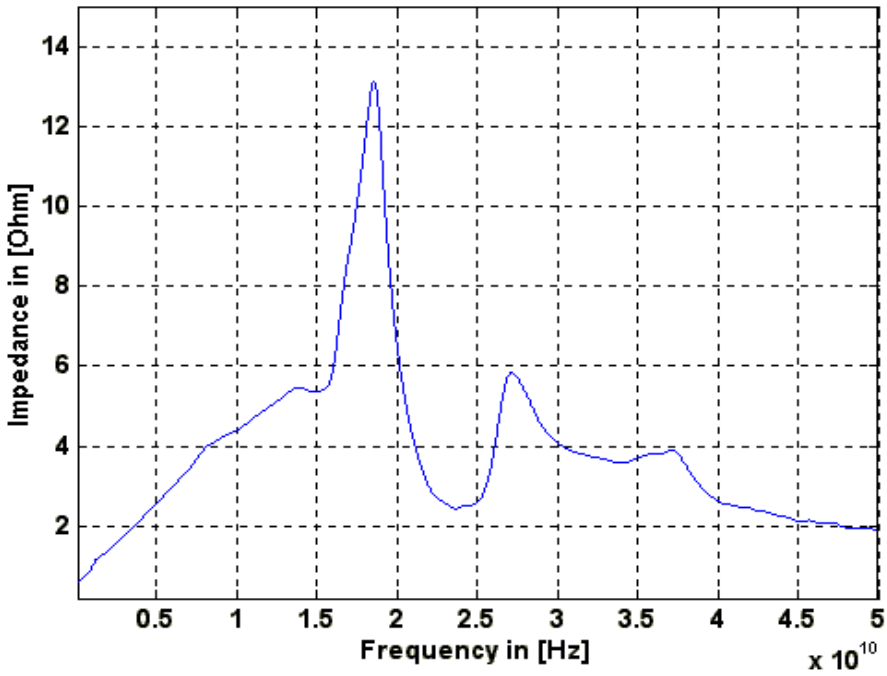


Figure 2.7(b) Self-impedance seen from the center of the on-chip power grid

100ps, a fall time of 200ps and peak current of 1A. A total of 38896 on-chip decoupling capacitors were uniformly distributed over the on-chip power grid. Each decoupling capacitor has 1.5pf of capacitance, 1pH of ESL (Equivalent Series Inductance) and 1mOhm of ESR (Equivalent Series Resistance). Figure 2.6(a)-(f) show the snapshots of the transient voltage response with one current source at different times. Figure 2.6(a) shows the differential noise due to the single source excitation at t=110ps, propagating outwards as shown in Figure 2.6(b)-(e). Finally, at time t=1160 ps, the radial wave propagation is totally attenuated, as shown in Figure 2.6(f). Based on the transient response, the propagation length is 3660um. At this distance, the energy in the radial wave is completely attenuated. This noise localization effect can be attributed to the low Q characteristic of the on-chip power grid. A Gaussian pulse with time bandwidth, 10ps, was used to capture the frequency response of the on-chip power grid. The pulse, as shown in Figure 2.7(a), was placed at the center of the power grid. Figure 2.7(b) shows the self-impedance seen from the center of the on-chip power grid which was obtained using the transformation. The on-chip inductance and decoupling capacitance form an RLC circuit that creates a resonant circuit. From Figure 2.7(b), the highest peak of the frequency spectrum occurs at 18.5GHz. As the circuit operation frequency approaches this peak, the resonance due to the RLC power grid can be a major concern in the on-chip power distribution network. From this section, it is important to note that the radial wave propagation or the on-chip resonance cannot be captured through a simple RC network, as was done previously.

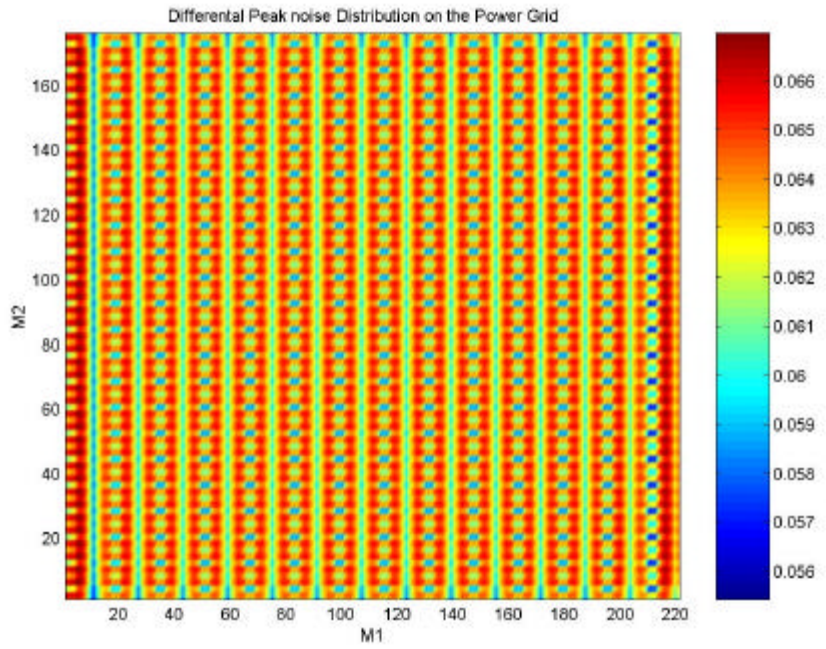


Figure 2.8 Differential peak noise distributions under uniform current distribution

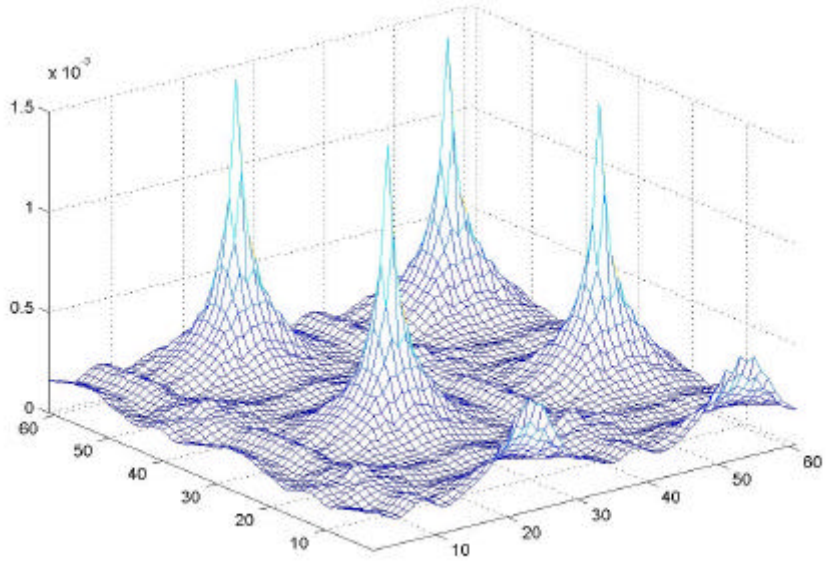


Figure 2.9 Part of differential peak noise distributions 3D under sparse switching condition

II. 3.b On-chip power distribution network

In order to compute the transient response for the on-chip power distribution network, intrinsic on-chip decoupling capacitors and approximately, 40000 current sources with amplitude 1mA, rise time 100ps and fall time 200ps were used to mimic the simultaneous switching circuits. The current sources were placed at the top metal layer with an interval of 60um. Figure 2.8 shows the differential peak noise distribution over the whole chip area under the uniform current source distribution. The CPU time for the peak noise calculation was 1hour and 20 minutes for 1 $x10^5$ time steps or 1 ns of time duration. From the figure, the cold spots(less noise) can be identified as C4 via positions and the hot spots(more noise) can be observed between the power and ground vias.

As another example, a sparse switching scenario was assumed for the peak noise simulation. A total of 56 current sources were placed on the power grid with an interval of 1.436 mm along the width and 2.250mm along the length. Figure 2.9 shows a part of the differential peak noise distribution on the power grid for the sparse current source distribution. It can be seen that the noise propagation on the on-chip power grid is localized due to a relatively high resistance on the top metal layer. However, when the noise propagation length is defined as a distance where 90 % of the peak noise is attenuated, the propagation radius is about 1200. Hence, for decoupling capacitors to be effective, they have to be placed within this radius.

II.4 Summary

In this chapter, the LIM using the FDTD method has been extended to multi-level power grids. In this method, a branch capacitor has been used, which is different from [17]. The use of the branch capacitor is important for simulating multi-layered power grids. The current in the branch capacitor is extracted from Kirchhoff's current law. This provides a good model of the branch capacitor and does not require any latency and companion models during simulation. The proposed model has been verified with SPICE through a simple example. The on-chip power grid simulation, the characteristics of noise propagation, and the effectiveness of on-chip decoupling capacitors have been discussed.

Chapter III

Modeling of On-Chip Power Grids with Nonlinear Circuits

In the previous chapter, the FDTD method was used to solve the circuit equations representing the on-chip power distribution network. However, the current sources were assumed to be linear. This assumption leads to a linear increase in the power supply noise voltage when either the number of drivers or the current slew rate increases. This can generate erroneous results since the power supply noise ultimately saturates due to the negative feed back effect of the driver circuitry [34]. Hence, the non-linearity of the circuits should be included while computing the power supply noise.

In this chapter, a method for including the CMOS inverter characteristics into the FDTD simulation is presented. This model has been verified by comparing it with SPICE, followed by a large network simulation with both linear and nonlinear circuits. As an example of the application of this method, an H-tree clock network has been simulated to compute the power supply noise distribution across an entire chip. Scenarios with varying decoupling capacitances, load capacitances,

number of clock buffers and rise time were analyzed to demonstrate the importance of circuit non-linearity on power supply noise.

III.1 FDTD compatible CMOS inverter model

When a network is large with lots of nonlinear drivers, the simulation of the power distribution network can create problems in SPICE. Usually, high level MOSFET models in SPICE such as the BSIM3 models have stability problems when combined with a large network.

In this section, the Shichman-Hodges model has been chosen for implementing the CMOS inverter in the FDTD algorithm. An alternate implementation will be the Sakurai's α -power model [35] which includes short channel effect such as velocity saturation. Shichman-Hodges current equations for PMOS and NMOS in 3 different regions, namely, Cutoff, Ohmic and Saturation region can be written as follows [36].

For PMOS,

$$I_{Dp} = 0 \qquad V_G - V_{DD} > V_T \ , \ V_O - V_{DD} \le 0 \qquad \text{(Cutoff)} \qquad \text{(3.7-a)}$$

$$-\frac{K_p W_p}{L_p}(V_G - V_{DD} - V_T - 0.5(V_O - V_{DD}))(V_O - V_{DD}) \qquad V_G - V_{DD} < V_T \ , \ 0 > V_G - V_{DD} > V_G - V_{DD} - V_T \qquad \text{(Ohmic)} \qquad \text{(3.7-b)}$$

$$-\frac{K_p W_p}{2L_p}(V_G - V_{DD} - V_T)^2 \qquad V_G - V_{DD} < V_T \ , \ V_G - V_{DD} < V_G - V_{DD} - V_T \qquad \text{(Saturation)} \qquad \text{(3.7-c)}$$

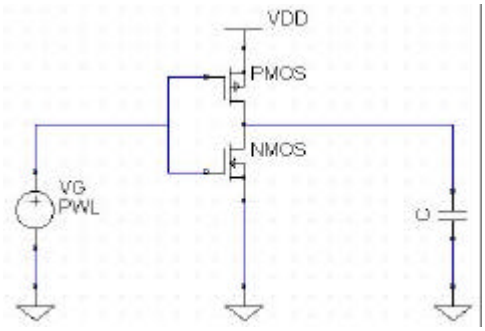
For NMOS,

$$I_{Dn} = 0 \qquad V_G - V_s < V_T \ , \ V_O - V_s \ge 0 \qquad \text{(Cutoff)} \qquad \text{(3.7-d)}$$

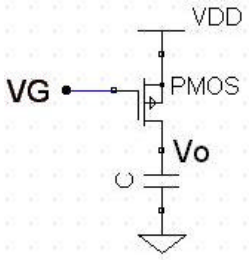
$$\frac{K_n W_n}{L_n}(V_G - V_S - V_T - 0.5(V_O - V_S))(V_O - V_S) \qquad V_G - V_S > V_T \ , \ 0 < V_G - V_S < V_G - V_S - V_T \qquad \text{(Ohmic)} \qquad \text{(3.7-e)}$$

$$\frac{K_n W_n}{2L_n}(V_G - V_S - V_T)^2 \qquad V_G - V_S > V_T \ , \ V_G - V_S > V_G - V_S - V_T \qquad \text{(Saturation)} \qquad \text{(3.7-f)}$$

where $I_{Dp,Dn}$ is the channel current of the MOSFET, $K_{p,n}$ is the transconductance prameter, $W_{p,n}$ is the channel width of the MOSFET, $L_{p,n}$ is the channel length of the MOSFET, V_O is the output voltage at load capacitors, V_G is the gate input voltage, V_S is the ground rail voltage and V_D is the power rail voltage. Figure 3.1.(a) shows an inverter model with a load capacitor. An FDTD compatible model can be obtained by separating the model into two scenarios, namely, High to Low transition of the gate voltage and Low to High transition of the gate voltage, as shown in Figures 3.1(b) and 3.1(c), respectively.

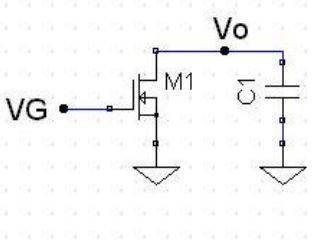


(a)



VG: High to Low Transition

(b)



VG: Low to High Transition

(c)

Figure 3.1 (a) CMOS inverter with a load capacitor
(b) Equivalent circuit under PMOS conduction
(c) Equivalent circuit under NMOS conduction

For the High-to-Low transition where the PMOS transistor is on and the NMOS transistor is off,

$$I_{Dp} + I_C = 0 \tag{3.8}$$

In the above equation, I_{Dp} is the current in the PMOS transistor and I_C is the current in the load capacitor. In the linear region, from Eq (3.7.b) and (3.8), an output voltage updating equation can be written as

$$V_O^{n+1/2} - V_S^{n+1/2} = V_O^{n-1/2} - V_S^{n-1/2}$$

$$+ \frac{C}{dt}\left(\frac{K_p W_p}{L_p}(V_G - V_{DD}^{n+1/2} - V_{Tp} - 0.5(V_O^{n+1/2} - V_{DD}^{n+1/2}))\right)(V_O^{n+1/2} - V_{DD}^{n+1/2}) \tag{3.9}$$

Rearranging Eq (3.9),

$$a(X^{n+1/2})^2 + bX^{n+1/2} + c = 0 \text{ for } X^{n+1/2} \equiv V_O^{n+1/2} - V_{DD}^{n+1/2} \tag{3.10}$$

where a, b and c are appropriate constants. From the solution of Eq (3.10),

$$V_O^{n+1/2} = X^{n+1/2} + V_{DD}^{n+1/2} \tag{3.11.a}$$

and $$I_{Dp}^{n+1} = \frac{K_p W_p}{L_p}(V_G - V_{DD}^{n+1/2} - V_{Tp} - 0.5(V_O^{n+1/2} - V_{DD}^{n+1/2}))(V_O^{n+1/2} - V_{DD}^{n+1/2}) \tag{3.11.b}$$

In the saturation region, from Eq. (3.7.c) and (3.8), the voltage updating equation can be written as

$$V_O^{n+1/2} - V_S^{n+1/2} = V_O^{n-1/2} - V_S^{n-1/2} + \frac{C}{dt}\left(\frac{K_p W_p}{2L_p}(V_G - V_{DD}^{n+1/2} - V_{Tp})^2\right) \tag{3.12}$$

$$aX^{n+1/2} + b = 0 \qquad \text{for } X^{n+1/2} \equiv V_O^{n+1/2} - V_{DD}^{n+1/2} \tag{3.13}$$

where a and b are appropriate constants. From the solution of Eq (3.13),

$$V_O^{n+1/2} = X^{n+1/2} + V_{DD}^{n+1/2} \tag{3.14.a}$$

$$I_{Dp}^{n+1} = \frac{K_p W_p}{2L_p}(V_G - V_{DD}^{n+1/2} - V_{Tp})^2 \qquad (3.14.b)$$

In a similar way, the voltage and current updating equations for the Low-to-High transition where the PMOS transistor is off and the NMOS transistor is on can be written as follows.

For the linear region,

$$V_o^{n+1/2} = X^{n+1/2} + V_s^{n+1/2} \qquad (3.15.a)$$

$$I_{dn}^{n+1} = \frac{K_n W_n}{L_n}(V_G - V_s^{n+1/2} - V_{Tn} - 0.5(V_o^{n+1/2} - V_s^{n+1/2}))(V_o^{n+1/2} - V_s^{n+1/2}) \qquad (3.15.b)$$

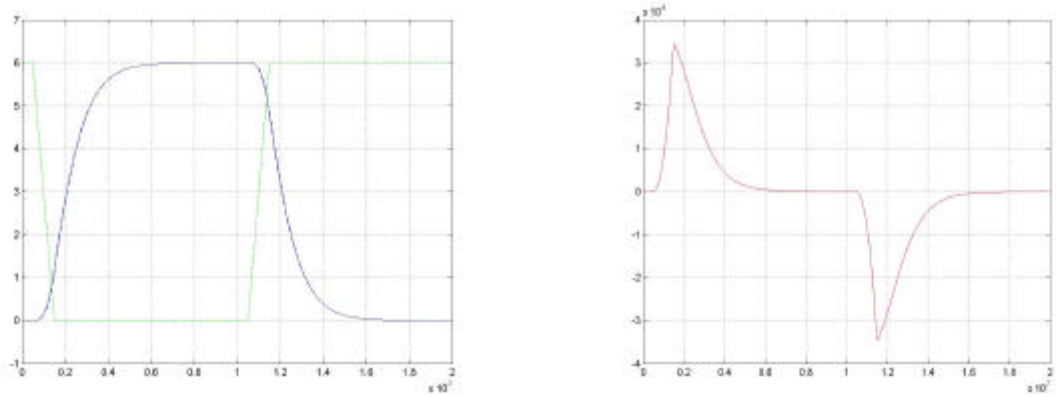
For the saturation region,

$$V_o^{n+1/2} = X^{n+1/2} + V_s^{n+1/2} \qquad (3.16.a)$$

$$I_{dn}^{n+1} = \frac{K_n W_n}{2L_n}(V_G - V_s^{n+1/2} - V_{Tn})^2 \qquad (3.16.b)$$

The inverter circuit implementation does not require an iterative method such as the Newton-Raphson algorithm for solution because of its analytical characteristics. In Figure 3.1(a), the rise and fall time are 10ns, the period is 200ns, the load capacitor is 1pF and the supply voltage is 6V. Using these parameters, the transient response of the circuit has been computed. Figure 3.2(a) and (b) show the comparison of the proposed model with SPICE, which shows good correlation. As a further comparison, R, L and C elements were included in the circuit, as shown in Figure 3.3(a). In this circuit, circuit elements R and L are power and ground rail resistance and inductance and C is a metal-to-metal intersection capacitance or decoupling capacitance. The CMOS transistors have the same characteristics as Figure 3.3(a) with L1=10nH, L2=10nH,

C2=0.1pF, C3=0.1pF, R1=0.5Ohm and R2=0.5Ohm. In Figure 3.3(b), the simulation results from FDTD and SPICE have been compared, which shows good correlation verifying the accuracy of the modeling approach.



(a) (b)

Figure 3.2 (a) Transient output voltage from FDTD and SPICE
Solid line: Vout from FDTD, Dashed-dot line:Vout from SPICE
(b) Transient current in load capacitor from FDTD and SPICE
Solid line: FDTD, Dotted line: SPICE

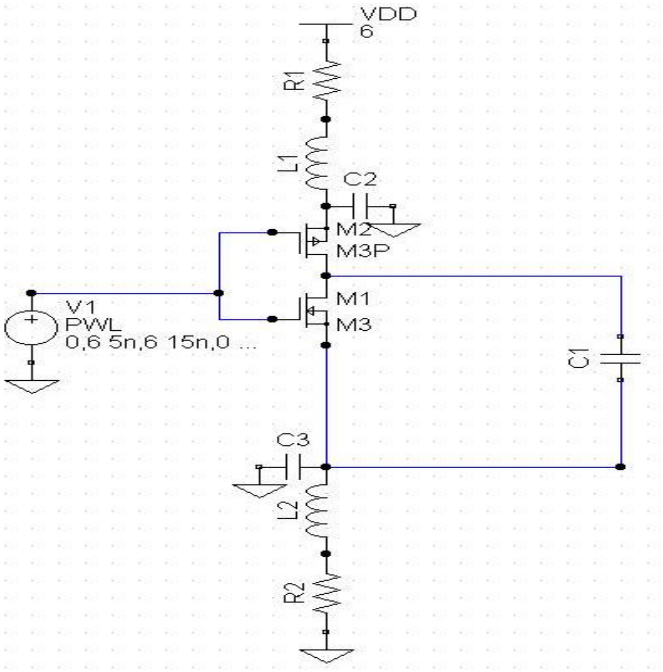


Figure 3.3 (a) CMOS inverter with some parasitic

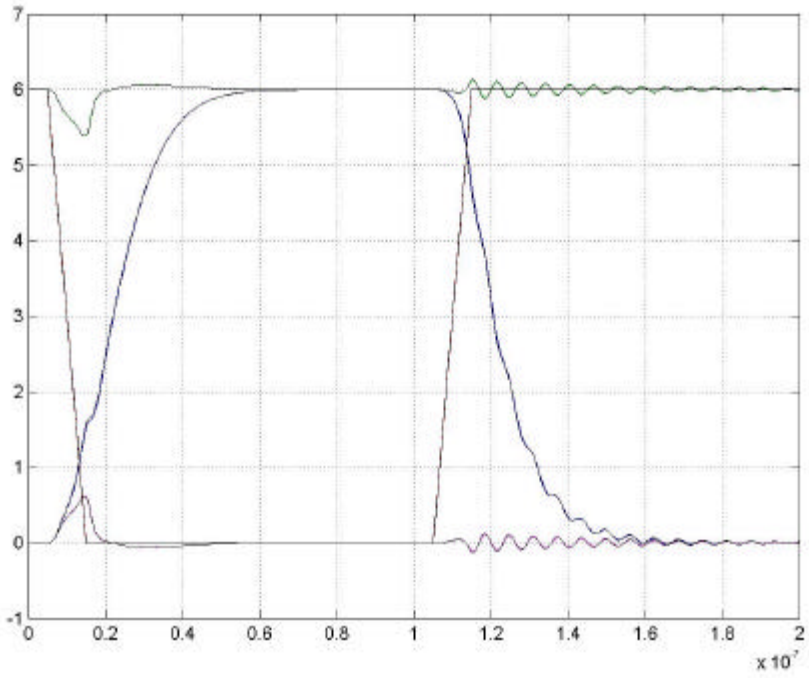


Figure 3.3(b) Transient voltage response and power and ground bounce
Dashed line: Vout, Dotted line: Power line noise,
Dashed dot line: Ground line noise from SPICE,
Solid line: all transient characteristics from FDTD.

III.2 Power supply noise computation with non-linear circuits

Figures 3.4(a) and (b) shows a power grid network consisting of 4 metal layers and C4 vias. The four levels of metal were assumed to have continuous voltage and ground lines across the surface of the chip. The first and second metal layers have alternating voltage and ground lines that are 3 um wide on a 60 um pitch. The third metal layer has 6 um wide lines on a 120 um pitch, and the fourth metal layer has 250 um wide lines on a 480 um pitch to match the periodicity of the area array foot print of 480 um, that attaches the chip to the package. The C4 via has a diameter of 250 um on a 480 um pitch and the size of the network was 13.5 X 10.5 mm^2 with 0.5 million passive elements, which represents a realistic

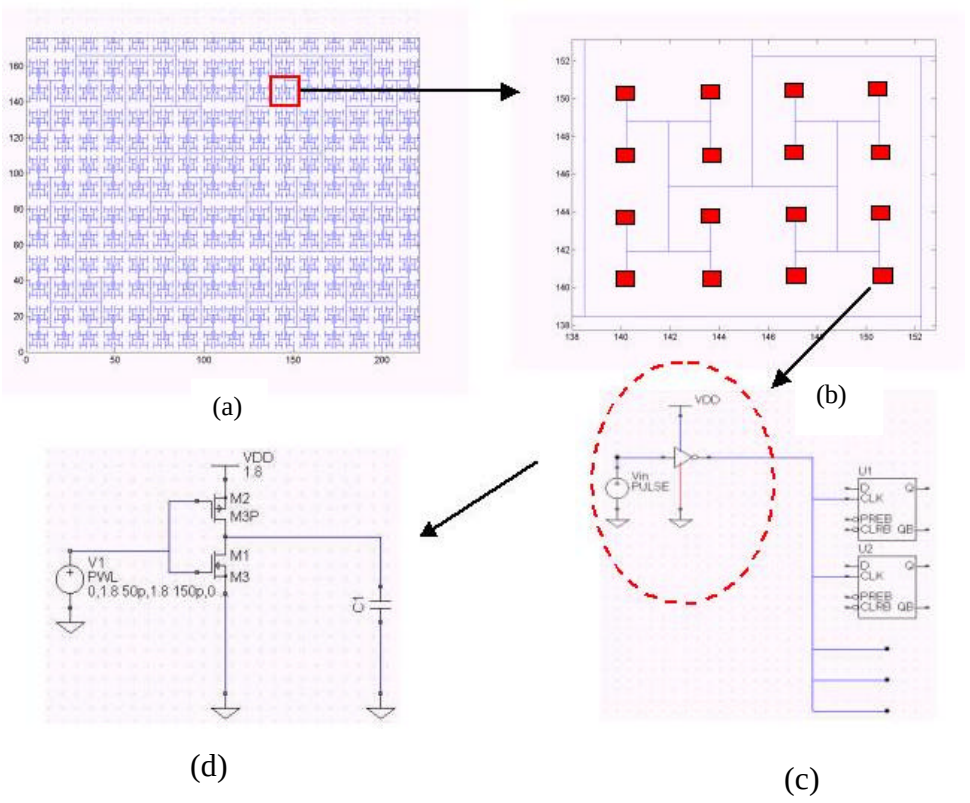
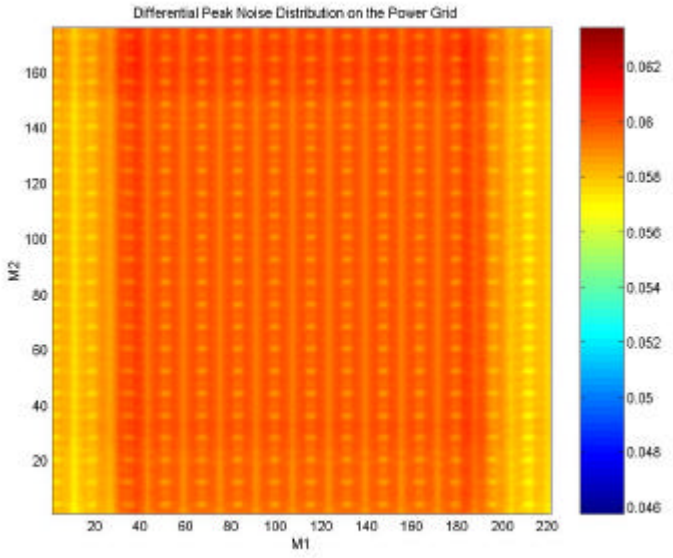


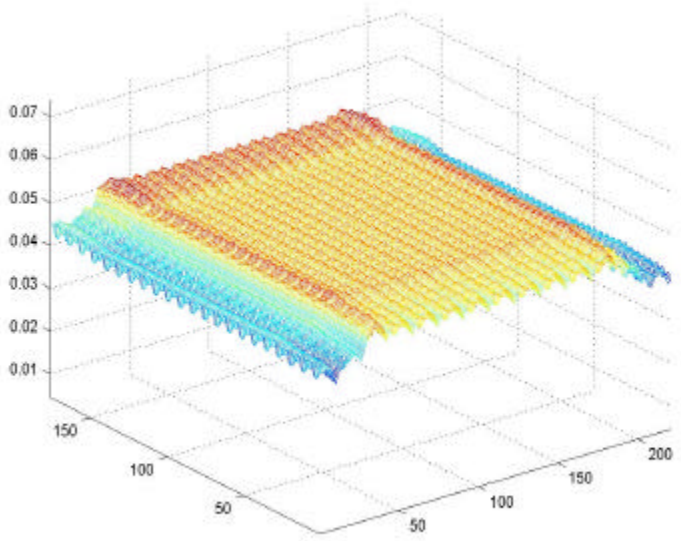
Figure 3.4(a) H-tree based clock network (b) Enlarged part of the clock network (c) Clock buffer connected to flip flops (d) Transistor model of the buffer

chip in modern systems. The R, L, and C values were extracted using a 3D field solver as shown in Figure 2.5 and incorporated into the FDTD code [37] with details, described in Chapter 2.

In a microprocessor, the clock buffers dissipate the maximum amount of power. Hence, for simulation purposes, a clock distribution network was chosen with an H-tree topology, as shown in Figure 3.4(a). Figure 3.4(b) is a magnification of a tiny area in the clock distribution network. At the nodal points on the clock net, 2376 clock buffers were placed, which were connected to flip flops as shown in Figure 3.4(c). Figure 3.4(d) shows the transistor model of the clock buffer, in which the signal at the gate has 100ps of rise and fall time with



(a)



(b)

Figure 3.5 (a) 2D differential peak noise distribution over the on-chip power grid
(b) 3D differential peak noise distribution over the on-chip power grid

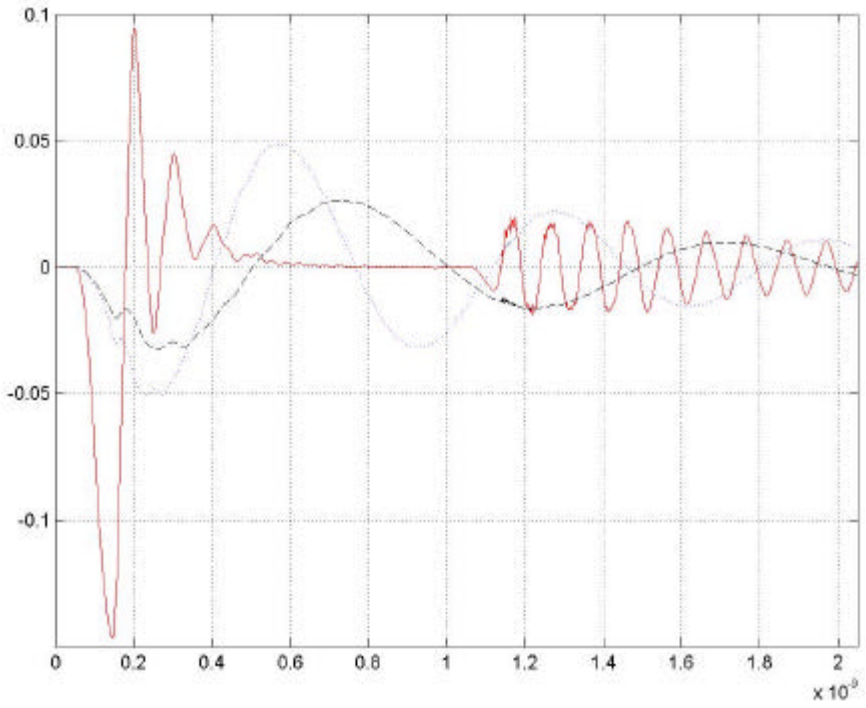


Figure 3.6 Differential noise waveforms with the different decoupling capacitors
Solid line: No decoupling capacitor,
Dashed line: Intrinsic decoupling capacitor (40nF)
Dotted line: Intrinsic decoupling capacitor (40nF) and extrinsic decoupling capacitor (40nF)

1.8V DC power supply and 1pF of load capacitance. The power supply is assumed to be at the bottom of the C4 vias.

The intrinsic decoupling capacitor is a built-in capacitor such as the n-well junction capacitor while the extrinsic decoupling capacitor is a add-on decoupling capacitor such as the thin-oxide capacitor or the trench capacitor [16]. With 40 nF intrinsic decoupling capacitance, the peak noise distribution on the chip was computed over the entire chip area. Figure 3.5(a) and (b) show the 2D and 3D differential peak noise distribution over the chip area due to the simultaneous switching of the clock buffers. The peak noise fluctuation at the chip edge can be

seen in Figure 3.5(b) due to the variation in the clock buffer density. Figure 3.6 shows the differential noise waveforms for 3 test cases, namely, with no decoupling capacitor, with an intrinsic decoupling capacitor, and with an intrinsic and extrinsic decoupling capacitor. From Figure 3.6, an 80% noise reduction can be seen when the peak noise from Test case 1 is compared with the peak noise from Test Case 3.

The three test cases were considered to demonstrate the importance of non-linearity in power supply noise computation. Peak noises were calculated with the variation of load capacitor (Test Case 1), number of clock buffers (Test Case 2) and rise time (Test Case 3). All these test cases were compared with the peak noise obtained when the current sources were assumed linear. Figure 3.7(a) shows the peak noise with varying load capacitance when 2376 linear (circled line) and non-linear (star-line) sources were used. Figure 3.7(b) shows the peak noise when the number of clock buffers driving 1pF load capacitance was varied. The peak noise as a function of rise time is shown in Figure 3.7(c). In Figure 3.7(a) and (b), an increase in the loading capacitance or increase in the number of inverters means that more charge is being switched in a given time period. In Figure 3.7(c), a decrease in the rise time means that charge is being supplied over a smaller time period. From Figure 3.7(a) and (b), noise saturation can be observed with the nonlinear circuit model unlike the linear circuit model. This phenomenon is caused by the negative feedback effect, as discussed in [34] and [38]. The terminology, negative feedback effect, means that, when the current slew rate is high in a CMOS circuit, the power supply voltge is compressed in

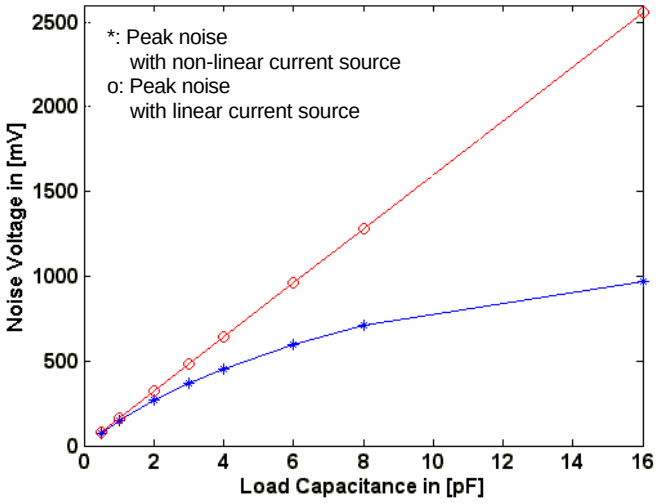


Figure 3.7 (a)

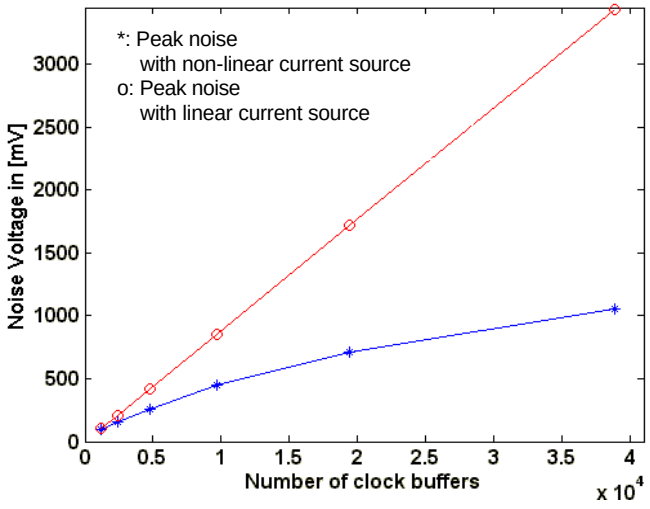


Figure 3.7 (b)

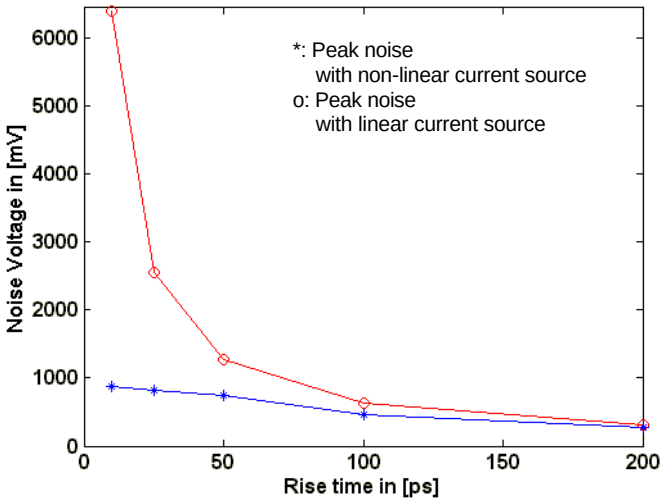


Figure 3.7 (c)

Figure 3.7 Differential peak noise plot with the variation of (a) load capacitor, (b) number of clock buffers and (c) rising time
Starred line: Peak noise with non-linear current source
Circled line: Peak noise with linear current source

such a way that the current in the CMOS channel is reduced, thereby causing the noise saturation in the power ground rails. According to Eq.(1.1), the peak noise is inversely proportional to rise time. However, in Figure 3.7(c), the peak noise with the non-linear circuit model varies linearly as rise time decreases. This behavior can be explained by the current decrease due to the negative feedback effect, as mentioned earlier.

III.3 Summary

In this chapter, a method for including the CMOS inverter characteristics into the FDTD simulation has been presented. This model was verified by comparing it with SPICE, followed by a large network simulation with both linear and nonlinear circuits. As an example of the application of this method, an H-tree

clock network was simulated to compute the power supply noise distribution across an entire chip. Various scenarios with varying decoupling capacitances, load capacitances, number of clock buffers and rise time have been analyzed to demonstrate the importance of circuit non-linearity on power supply noise.

Chapter IV

On-Chip Transmission Line Interconnections

Due to rapidly increasing clock frequencies, interconnect inductance is significantly affecting wire delay and cross talk. High-speed off-chip interconnects have nearly ideal return current paths because of nearby ground planes, but high-speed on-chip interconnects have non-ideal return current paths because of nearby orthogonal lines [56]. Devices driving long on-chip buses generate power supply noise based on the path of the return currents in the power distribution network. This is caused due to the mutual inductance and coupling capacitance between the signal lines and the power bus. This problem is ideally suited for analysis using FDTD. In this chapter, FDTD algorithms that include mutual inductance and coupling capacitance, are discussed and used to simulate long on-chip bus lines.

IV.1 Coupled n transmission lines

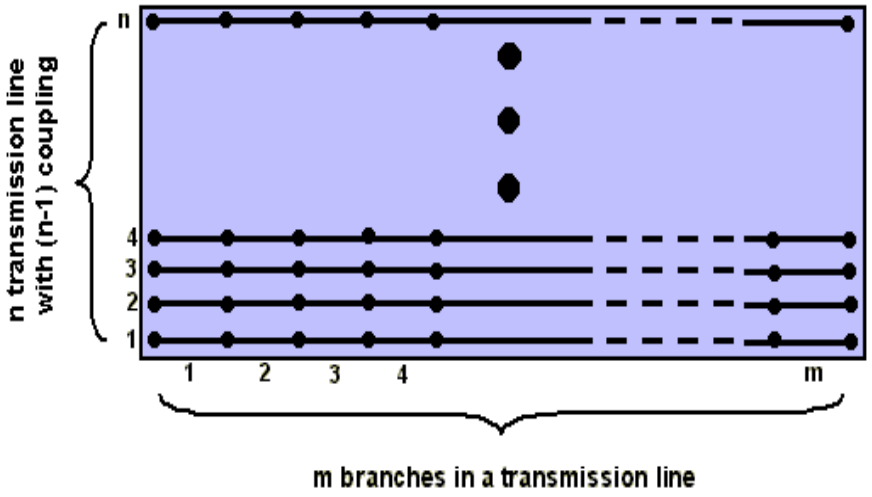


Figure 4.1(a) n transmission lines with (n-1) couplings over a ground plane

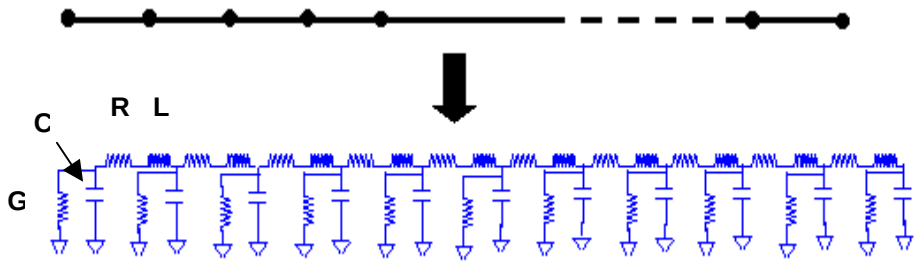


Figure 4.1 (b) Circuit representation of a transmission line with p model

Figure 4.1(a) shows n transmission lines with (n-1) inductive and capacitive coupling paths over a ground plane. The ground plane acts as a return current path for the transmission lines. Each transmission line with m branches in Figure 4.1(b) can be represented as cascaded p model with R, L, C and G parameters. There are n by (m+1) nodes and n by m branches in the n transmission line system in which node to node capacitive coupling and branch to branch inductive coupling in column are assumed. In order to obtain a voltage updating algorithm,

Kirchhoff's current law can be applied to the n transmission line system for the first column of the nodes and can be written as

$$\begin{pmatrix}
{}^1c_1\frac{d^1V_1}{dt} + {}^1mc_{1,2}\frac{d^1V_{12}}{dt} + {}^1mc_{1,3}\frac{d^1V_{13}}{dt} + \bullet\bullet {}^1mc_{1,n-1}\frac{d^1V_{1n}}{dt} + {}^1G_1V_1 - {}^1I_1 = 0 \\
-{}^1mc_{1,2}\frac{d^1V_{12}}{dt} + {}^1c_2\frac{d^1V_2}{dt} + {}^1mc_{2,3}\frac{d^1V_{23}}{dt} + \bullet\bullet {}^1mc_{2,n-1}\frac{d^1V_{2n}}{dt} + {}^1G_2V_2 - {}^1I_2 = 0 \\
-{}^1mc_{1,3}\frac{d^1V_{13}}{dt} - {}^1mc_{2,,3}\frac{d^1V_{13}}{dt} + {}^1c_3\frac{d^1V_3}{dt} + \bullet\bullet {}^1mc_{3,n-1}\frac{d^1V_{2n}}{dt} + {}^1G_3V_3 - {}^1I_3 = 0 \\
\bullet \quad \bullet \quad \bullet \quad \bullet \quad \bullet \quad \bullet\bullet\bullet \quad \bullet \quad \bullet \quad \bullet \quad \bullet = 0 \\
\bullet \quad \bullet \quad \bullet \quad \bullet \quad \bullet \quad \bullet\bullet\bullet \quad \bullet \quad \bullet \quad \bullet \quad \bullet = 0 \\
-{}^1mc_{1,n}\frac{d^1V_{1n}}{dt} - {}^1mc_{2,n}\frac{d^1V_{2n}}{dt} - {}^1mc_{3,n}\frac{d^1V_{3n}}{dt} \bullet\bullet\bullet + {}^1c_n\frac{d^1V_n}{dt} + {}^1G_nV_n - {}^1I_n = 0
\end{pmatrix} \tag{4.1}$$

where c_i is the node capacitance, $mc_{i,j}$ is the mutual capacitance between the i-th node and j-th node, ${}^1V_{i,j}$ is ${}^1V_i - {}^1V_j$ which is the differential voltage between the I-th and j-th nodes , ${}^1G_i$ is the shunt conductance at the i-th node and ${}^1I_i$ is the current in the i-th branch of the first column of the branch. Eq.(4.1) can be written in the form of a matrix equation as

$$MC\left|d^1V_i\right\rangle + G\left|{}^1V_i\right\rangle = \left|{}^1I_i\right\rangle \tag{4.2}$$

where

$$\text{MC} = \begin{pmatrix}
({}^1c_1 + \sum_{i=1}^{n-1} {}^1mc_{1,i+1})/dt & {}^1mc_{1,2}/dt & {}^1mc_{1,3}/dt & \bullet\bullet & {}^1mc_{1,n}/dt \\
-{}^1mc_{1,2}/dt & ({}^1c_2 + \sum_{i=1}^{n-1} {}^1mc_{2,i+1})/dt & {}^1mc_{2,3}/dt & \bullet\bullet & {}^1mc_{2,n}/dt \\
-{}^1mc_{1,3}/dt & -{}^1mc_{2,3}/dt & ({}^1c_3 + \sum_{i=1}^{n-1} {}^1mc_{3,i+1})/dt & \bullet\bullet & {}^1mc_{3,n}/dt \\
\bullet & \bullet & \bullet & \bullet\bullet & \bullet \\
\bullet & \bullet & \bullet & \bullet\bullet & \bullet \\
-{}^1mc_{1,n}/dt & -{}^1mc_{2,n}/dt & -{}^1mc_{3,n}/dt & \bullet\bullet & {}^1mc_{n,n}/dt
\end{pmatrix},$$

$$\text{G} = \begin{pmatrix}
G_1 & 0 & 0 & \bullet & \bullet & 0 \\
0 & G_2 & 0 & \bullet & \bullet & 0 \\
0 & 0 & G_3 & \bullet & \bullet & 0 \\
\bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\
\bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\
0 & 0 & 0 & \bullet & \bullet & G_n
\end{pmatrix}, \left|d^1V_i\right\rangle = \begin{pmatrix} d^1V_1 \\ d^1V_2 \\ d^1V_3 \\ \bullet \\ \bullet \\ d^1V_n \end{pmatrix}, \left|{}^1V_i\right\rangle = \begin{pmatrix} {}^1V_1 \\ {}^1V_2 \\ {}^1V_3 \\ \bullet \\ \bullet \\ {}^1V_n \end{pmatrix} \text{and } \left|{}^1I_i\right\rangle = \begin{pmatrix} {}^1I_1 \\ {}^1I_2 \\ {}^1I_3 \\ \bullet \\ \bullet \\ {}^1I_n \end{pmatrix}.$$

Using the central difference formula, Eq.(4.2) can be written as

$$\left|{}^{1}V^{n}{}_{i}\right\rangle = MCG^{-1}MC\left|{}^{1}V_{i}^{n-1}\right\rangle - MCG^{-1}\left|{}^{1}I_{i}^{n-1/2}\right\rangle \tag{4.3}$$

where

$$\text{MCG=MC + G, } \left|V_{i}^{n}\right\rangle = \begin{pmatrix} V_1^n \\ V_2^n \\ V_3^n \\ \bullet \\ \bullet \\ V_n^n \end{pmatrix}, \left|V_{i}^{n-1}\right\rangle = \begin{pmatrix} V_1^{n-1} \\ V_2^{n-1} \\ V_3^{n-1} \\ \bullet \\ \bullet \\ V_n^{n-1} \end{pmatrix} \text{ and } \left|{}^{1}I_{i}^{n-1/2}\right\rangle = \begin{pmatrix} {}^{1}I_1^{n-1/2} \\ {}^{1}I_2^{n-1/2} \\ {}^{1}I_3^{n-1/2} \\ \bullet \\ \bullet \\ {}^{1}I_n^{n-1/2} \end{pmatrix}.$$

Eq. (4.3) can be generalized as

$$\left|{}^{k}V^{n}{}_{i}\right\rangle = MCG^{-1}MC\left|{}^{k}V_{i}^{n-1}\right\rangle - MCG^{-1}\left|{}^{k}I_{i}(1-d_{km}) - {}^{k-1}I_{i}(1-d_{k1})\right\rangle \tag{4.4}$$

where d_{km} and d_{k1} shows the zero input current to I-th node of the k-th column and the zero output current from (m+1) th node of the k-th column, respectively. In order to obtain a current updating algorithm, Kirchhoff's voltage law can be applied to the n transmission line system for the first column of branches as in Eq(4.5) where ${}^{1}l_{i}$ is the self inductance at i-th branch of the first column, ${}^{1}ml_{i,i+1}$ is the mutual inductance between i-th and i+1th branch in the first column, ${}^{1}V_{12}$ is ${}^{1}V_{1} - {}^{1}V_{2}$ of the i-th row, ${}^{1}I_{i}$ is the current in i-th row of the first column, and ${}^{1}R_{i}$ is the resistance of the i-th row of the first column.

$$\begin{pmatrix}
{}^{1}V_{12} &= {}^{1}l_1\frac{d^1I_1}{dt} &+ {}^{1}ml_{12}\frac{d^1I_2}{dt} &+ {}^{1}ml_{13}\frac{d^1I_3}{dt} &+ \bullet\bullet &{}^{1}ml_{1n}\frac{d^1I_n}{dt} &+ {}^{1}R_1{}^{1}I_1 \\
{}^{2}V_{12} &= {}^{1}ml_{12}\frac{d^1I_1}{dt} &+ {}^{1}l_2\frac{d^1I_2}{dt} &+ {}^{1}ml_{23}\frac{d^1I_3}{dt} &+ \bullet\bullet &{}^{1}ml_{2n}\frac{d^1I_n}{dt} &+ {}^{1}R_2{}^{1}I_2 \\
{}^{3}V_{12} &= {}^{1}ml_{13}\frac{d^1I_1}{dt} &+ {}^{1}ml_{23}\frac{d^1I_2}{dt} &+ {}^{1}l_3\frac{d^1I_3}{dt} &+ \bullet\bullet &{}^{1}ml_{3n}\frac{d^1I_n}{dt} &+ {}^{1}R_3{}^{1}I_3 \\
\bullet &= \bullet &+ \bullet &+ \bullet &+ \bullet\bullet &\bullet &+ \bullet \\
\bullet &= \bullet &+ \bullet &+ \bullet &+ \bullet\bullet &\bullet &+ \bullet \\
{}^{n}V_{12} &= {}^{1}ml_{1n}\frac{d^1I_1}{dt} &+ {}^{1}ml_{2n}\frac{d^1I_2}{dt} &+ {}^{1}ml_{3n}\frac{d^1I_3}{dt} &+ \bullet\bullet &{}^{1}ml_{nn}\frac{d^1I_n}{dt} &+ {}^{1}R_n{}^{1}I_n
\end{pmatrix} \tag{4.5}$$

Eq. (4.5) can be written in the form of a matrix equation as

$$\left|{}^{i}V_{12}\right\rangle = ML\left|d^{1}I_{i}\right\rangle + R\left|{}^{1}I_{i}\right\rangle \tag{4.6}$$

where

$$\text{ML} = \begin{pmatrix} {}^{1}l_{1}/dt & {}^{1}ml_{12}/dt & {}^{1}ml_{13}/dt & \bullet & \bullet & {}^{1}ml_{1n}/dt \\ {}^{1}ml_{12}/dt & {}^{1}l_{2}/dt & {}^{1}ml_{23}/dt & \bullet & \bullet & {}^{1}ml_{2n}/dt \\ {}^{1}ml_{13}/dt & {}^{1}ml_{23}/dt & {}^{1}l_{3}/dt & \bullet & \bullet & {}^{1}ml_{3n}/dt \\ \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\ \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\ {}^{1}ml_{1n}/dt & {}^{1}ml_{2n}/dt & {}^{1}ml_{3n}/dt & \bullet & \bullet & {}^{1}ml_{nn}/dt \end{pmatrix}, \quad \left|{}^{i}V_{12}\right\rangle = \begin{pmatrix} {}^{1}V_{12} \\ {}^{2}V_{12} \\ {}^{3}V_{12} \\ \bullet \\ \bullet \\ {}^{n}V_{12} \end{pmatrix}, \quad \left|d^{1}I_{i}\right\rangle = \begin{pmatrix} d^{1}I_{1} \\ d^{1}I_{2} \\ d^{1}I_{3} \\ \bullet \\ \bullet \\ d^{1}I_{n} \end{pmatrix},$$

$$\left|{}^{1}I_{i}\right\rangle = \begin{pmatrix} {}^{1}I_{1} \\ {}^{1}I_{2} \\ {}^{1}I_{3} \\ \bullet \\ \bullet \\ {}^{1}I_{n} \end{pmatrix} \qquad \begin{pmatrix} {}^{1}R_{1} & 0 & 0 & \bullet & \bullet & 0 \\ 0 & {}^{1}R_{2} & 0 & \bullet & \bullet & 0 \\ 0 & 0 & {}^{1}R_{3} & \bullet & \bullet & 0 \\ \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\ \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\ 0 & 0 & 0 & \bullet & \bullet & {}^{1}R_{n} \end{pmatrix}.$$

Eq (4.6) can be rewritten using the central difference formula as

$$\left|{}^{1}I_{i}^{n+1/2}\right\rangle = \left|{}^{1}I_{i}^{n-1/2}\right\rangle + ML^{-1}\left|{}^{i}V^{n-1}{}_{12}\right\rangle - ML^{-1}R\left|{}^{1}I_{i}^{n-1/2}\right\rangle \tag{4.7}$$

where

$$\left|{}^{1}I_{i}^{n-1/2}\right\rangle = \begin{pmatrix} {}^{1}I_{1}^{n-1/2} \\ {}^{1}I_{2}^{n-1/2} \\ {}^{1}I_{3}^{n-1/2} \\ \bullet \\ \bullet \\ {}^{1}I_{n}^{n-1/2} \end{pmatrix}, \quad \left|{}^{1}I_{i}^{n-1/2}\right\rangle = \begin{pmatrix} {}^{1}I_{1}^{n-1/2} \\ {}^{1}I_{2}^{n-1/2} \\ {}^{1}I_{3}^{n-1/2} \\ \bullet \\ \bullet \\ {}^{1}I_{n}^{n-1/2} \end{pmatrix} \text{ and } \left|V_{i}^{n}\right\rangle = \begin{pmatrix} V_{1}^{n} \\ V_{2}^{n} \\ V_{3}^{n} \\ \bullet \\ \bullet \\ V_{n}^{n} \end{pmatrix}.$$

Eq. (4.7) can be generalized as

$$\left|{}^{k}I_{i}^{n+1/2}\right\rangle = \left|{}^{k}I_{i}^{n-1/2}\right\rangle + ML^{-1}\left|{}^{i}V_{k,k+1}^{n-1}\right\rangle - ML^{-1}R\left|{}^{k}I_{i}^{n-1/2}\right\rangle \tag{4.8}$$

where the upper left subscript, ‘k’, is the k-th column of branches, the upper right subscripts, ‘n+1/2’, ‘n-1/2’ and ‘n-1’ are the interlaced time steps, and the lower right subscript,’ i’, is the i-th row branch.

For a large coupled circuit network, SPICE analyze the network through Modified Nodal Analysis (MNA) that requires a large matrix inversion. In order to highlight the usefulness of the approach discussed in this section, let us consider a 100 transmission line system with all inductive and capacitive coupling in which each transmission line has 100 branches. The MNA matrix for the network requires 3.23 Gbytes of memory and, even though the sparse matrix solver can be used, it still requires about 64 Mbytes of memory. However, in the formulation discussed in this section, the solution requires just 158 Kbytes of memory resulting in the efficient memory usage and CPU time. Hence, on-chip buses containing many long interconnections can be analyzed using the FDTD formulation that has been presented.

IV.2 Verification with SPICE

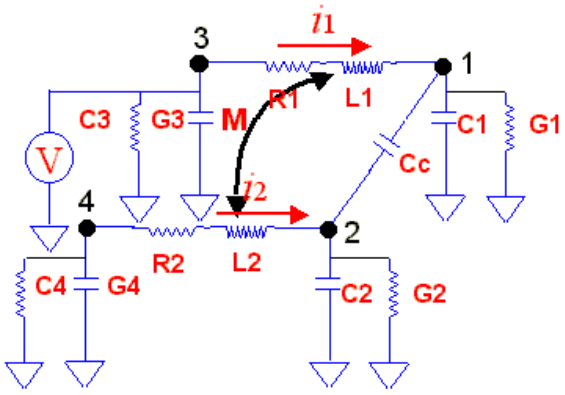


Figure 4.2 A simple coupled structure

For verification of the formulation in the previous section, a simple coupled structure was generated as in Figure 4.2. In the figure, the mutual capacitance, C_c, is 0.1 nF and the mutual coupling coefficient, M, is 0.1. The self-capacitance,

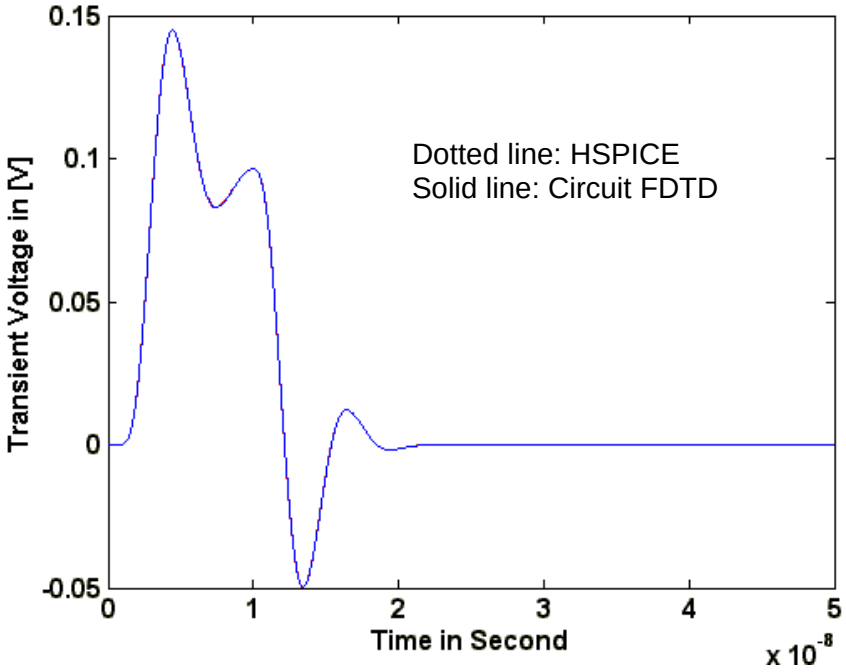


Figure 4.3(a) Voltage response at the node, 2

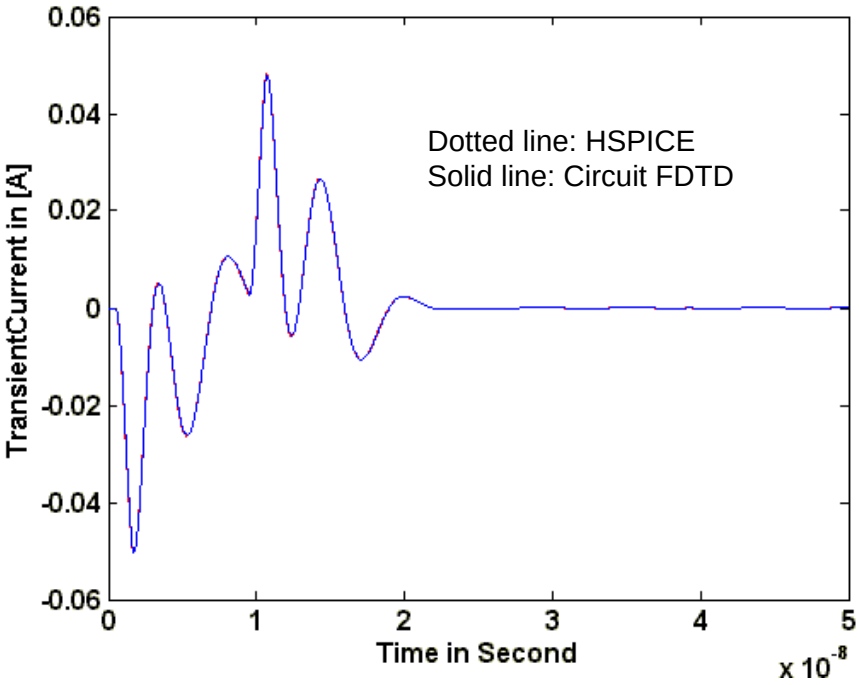


Figure 4.3(b) Current response in the branch with the inductor, L2

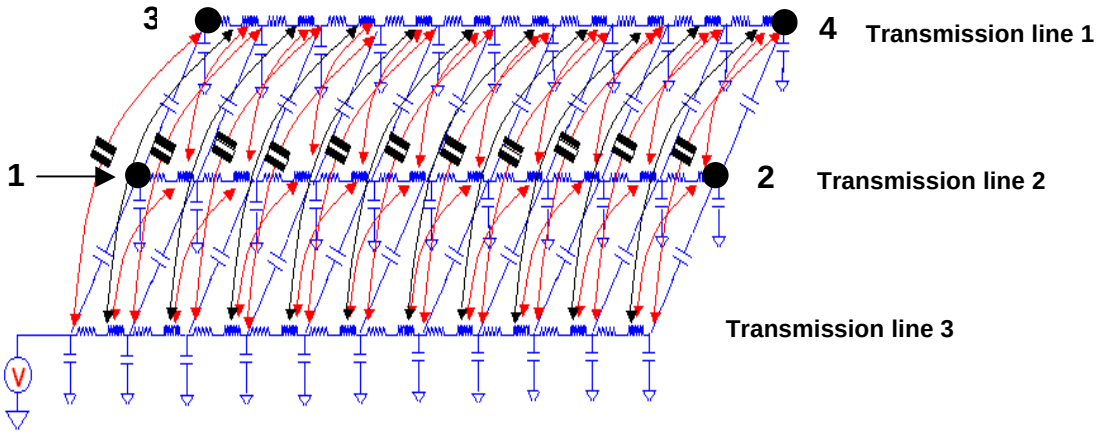


Figure 4.4 Coupled transmission lines with mutual inductance and capacitance

C1, C2, C3 and C4 are 1 nF, the branch inductors, L1 and L2 are 1nH, the branch resistors, R1 and R2 are 1 Ohm and the shunt conductance, G1, G2, G3 and G4 are 1e-6 S. The voltage source with rise time of 1ns, fall time of 1ns, pulse duration of 8ns and voltage variation from 0 to 2V was applied to node 3 and the transient response at node 2 and the branch current through the inductor L2 were observed for the time duration from 0 to 50 ns. Figure 4.3(a) shows the voltage response at node 2 using SPICE (dotted line) and the circuit FDTD (solid line) method. In Figure 4.3(b), the transient current through inductor L2 has been compared using the two methods. It can be seen that there is good correlation between SPICE and the circuit FDTD method, which verifies the formulation.

As an example for the coupled network, 3 coupled transmission lines with mutual inductance and capacitance are shown in Figure 4.4 in which a ground plane was assumed as a return current path. Each transmission line has 10 branches and 11 nodes. In Figure 4.4, the self-inductance is 47.3 pH, resistance is 0.345 ohm and self-capacitance is 3.36 fF. In addition, mutual capacitances,

mc_{12}, mc_{13} and mc_{23} are 0.336fF, 0.084fF and 0.336fF, where the lower subscripts, '12', '13' and '23' represent the coupling between the appropriate transmission lines. The mutual inductance coupling coefficients, ml_{12}, ml_{13} and ml_{23} are 0.1, 0.05 and 0.1. In Figure 4.4, a voltage source with rise time of 1ns, fall time of 1ns, pulse duration of 8ns and voltage variation from 0 to 2V was applied to the left most nodes of the first transmission line and the transient voltage response were observed at nodes 1, 2, 3 and 4. Figures 4.5(a) and (b) show the near-end noise at node 1 and 3 and the far-end noise at node 3 and 4, respectively. All transient responses in Figure 4.5(a)-(c) were overlapped with SPICE results showing good correlation, where the dotted line is from SPICE and the solid line is from the formulation discussed in the previous section.

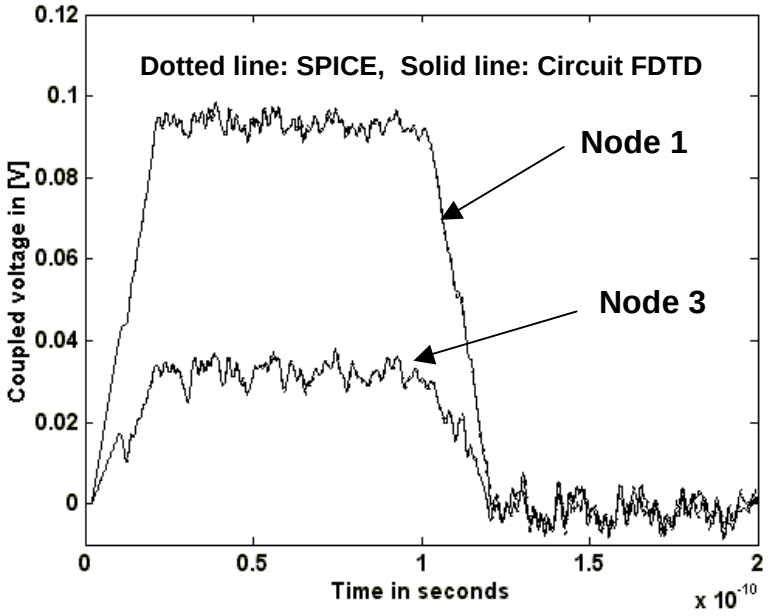


Figure 4.5(a) Near-end noise at nodes 1 and 3

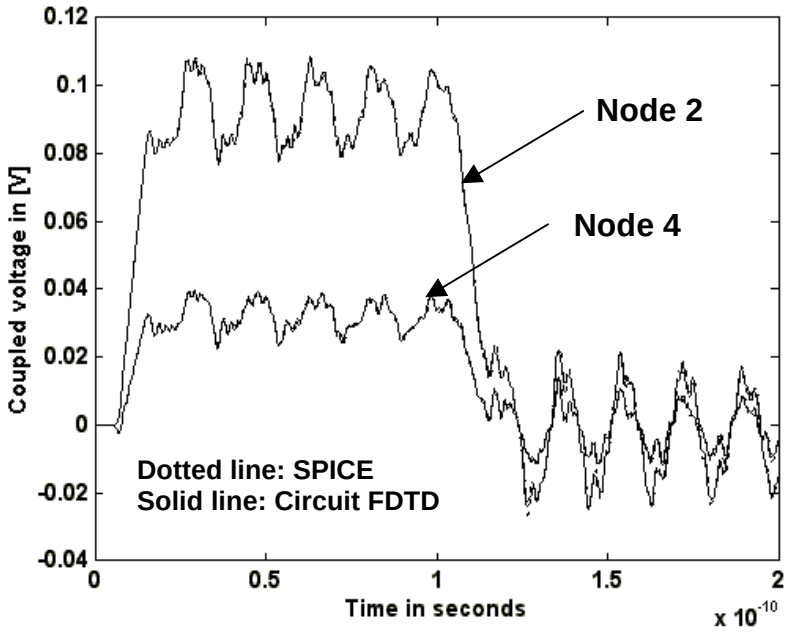


Figure 4.5(b) Far-end noise at nodes 2 and 4

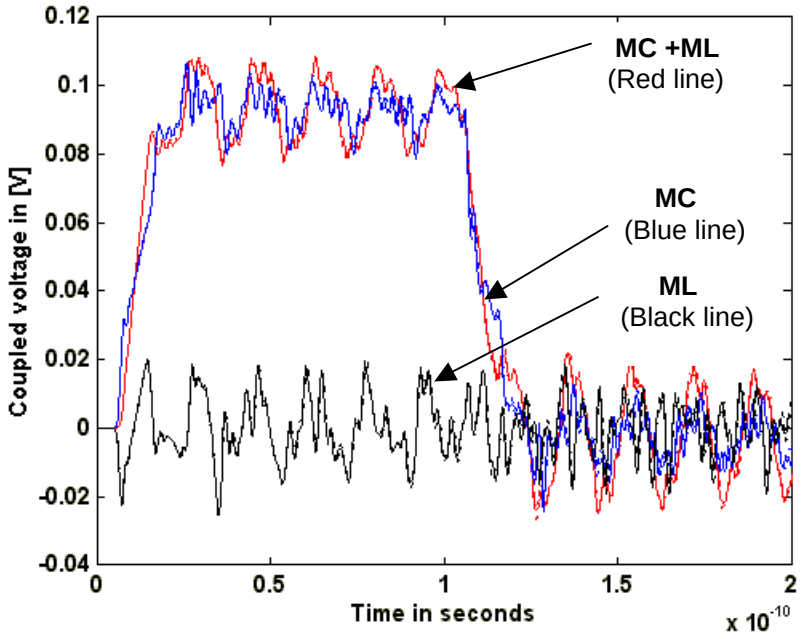


Figure 4.5(c) Far-end noise responses at node 3, with mutual capacitance only, mutual inductance only and mutual capacitance and inductance coupling

It can be seen that the coupled noise at node 3 and 4 in Figure 4.5(a) is less than the noise at node 1 and 2 due to less coupling from the source. Figure 4.5(c) shows the far-end noise at node 3, with mutual capacitance only, mutual inductance only and mutual capacitance and inductance coupling. The far-end noise with only mutual capacitance coupling is higher than the far-end noise with only mutual inductive coupling. This can be explained by the fact that, since the voltage source can be viewed as an electric energy source, the energy can be more easily transferred through the capacitor than the mutual inductor.

IV.3 Return currents

In the previous section, the coupled transmission line assumed an ideal return current path. In this section, the coupled interconnections have been combined with the on-chip power grid, resulting in a non-ideal return current path.

In order to study the return current effect, 3 test cases, a vertical Signal - Power - Ground (SPG) structure, a vertical Power-Ground-Signal (PGS) structure and a horizontal Power-Signal-Ground (PSG) structure were studied. In Test Case 1, signal, power and ground lines were stacked vertically, as shown in Figure 5.6(a). The signal line width was assumed to be 1um and power-ground line widths were assumed to be 3 um, with a line spacing of 12.5 um and line length of 1562.5 um. The circuit parameters for this structure were extracted from ANSOFT MAXWELL 2D, as shown in the left side of Figure 4.6(a). The extracted circuit parameters are summarized in Table IV.1 where the subscripts, P, S, G, GS, GP and SP represent the power line, the signal line, the ground line, the

ground line to signal line, the ground line to signal line and the signal line to power line coupling, in that order. Based on the circuit parameters, the well-known p -type equivalent circuits were used for the transmission lines in Figure 4.6(a)-(c).

Table IV.1 The extracted circuit parameters from ANSOFT MAXWELL 2D

Test structure	Extracted circuit parameters
SPG and SGP	Inductances: L_P=8.9426e-7H/m, L_G=8.9288e-7H/m, L_S=9.9985e-7H/m, L_{GS}=7.6761e-7H/m, L_{GP}=8.1998e-7H/m and L_{SP}=8.1998e-7H/m Capacitances: C_P=1.9412e-10F/m, C_G=1.4263e-10F/m, C_S=5.7129e-11F/m, C_{GS}=4.5133e-13F/m, C_{GP}=1.3812-10F/m and C_{SP}=5.4606-11F/m
PSG	Inductances: L_P=7.6674e-7H/m, L_G=7.6674e-7H/m, L_S=9.055e-7H/m, L_{GS}=3.1369-7H/m, L_{GP}=1.8444-7H/m and L_{SP}=3.1246e-7H/m Capacitances: C_P=3.9954e-11F/m, C_G=3.9496e-11F/m, C_S=2.1583e-11F/m, C_{GS}=2.1008e-13F/m, C_{GP}=8.0251e-12F/m and C_{SP}=2.109e-11F/m

A DC voltage source was placed at the far end from the driver. An inverter model discused in Chapter 3 mimics the driver shown in Figure 4.6. The input signal of the driver with 1.1V of DC voltage had a rise time of 20ps, fall time of 20ps, pulse duration of 80ps, and 200ps of period. Vdd and ground of the driver were connected to the right end of the power line and ground line, respectively. In addition, the output node of the driver was connected to the right end of the signal line named as Port 1. Test Case 2 is similar to Test Case 1 with power and ground lines interchanged. In Test Case 3, power, signal and ground lines are

the same width as in Test Case1 with a line spacing of 10um and line lengths of 937.5 um. Figure 4.7(a) and (b) show the output voltage of the driver at Port 1 and differential noise near the driver for Test case 1. The differential noise was measured between the right ends of the power and ground line.

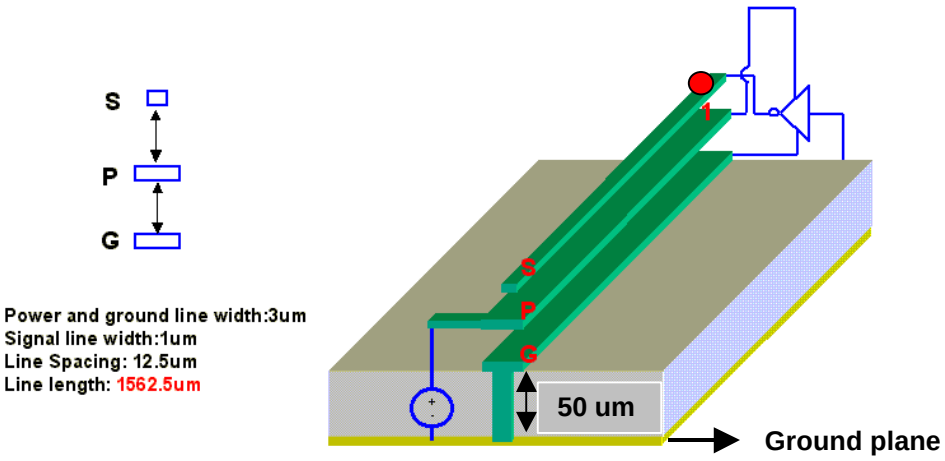


Figure 4.6(a)

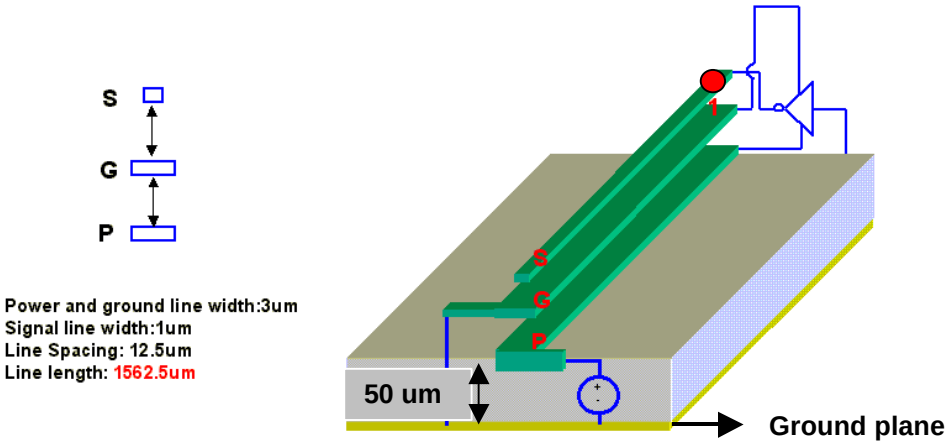


Figure 4.6(b)

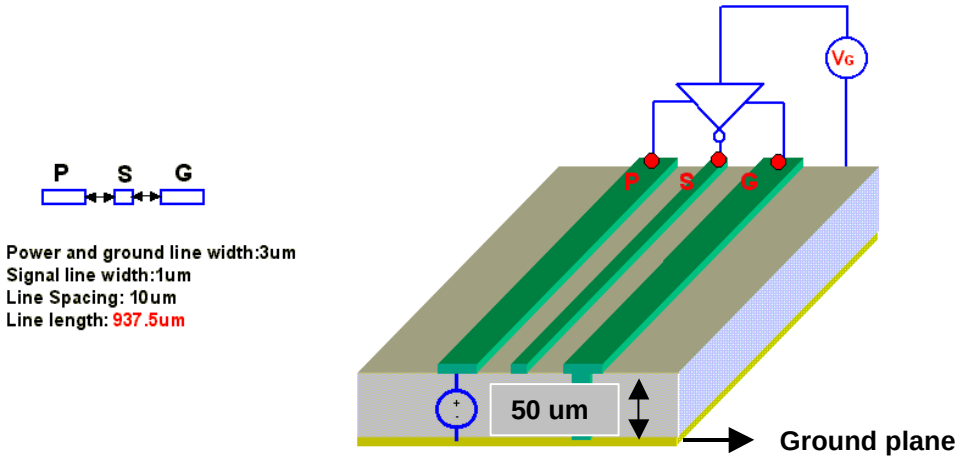


Figure 4.6(c)

Figure 4.6 (a) Vertical signal to power to ground (SPG) structure (Test Case 1)
(b) Vertical Power to Ground to Signal (PGS) structure (Test Case 2)
(c) Horizontal Power to Signal Ground (PSG) structure (Test Case 3)

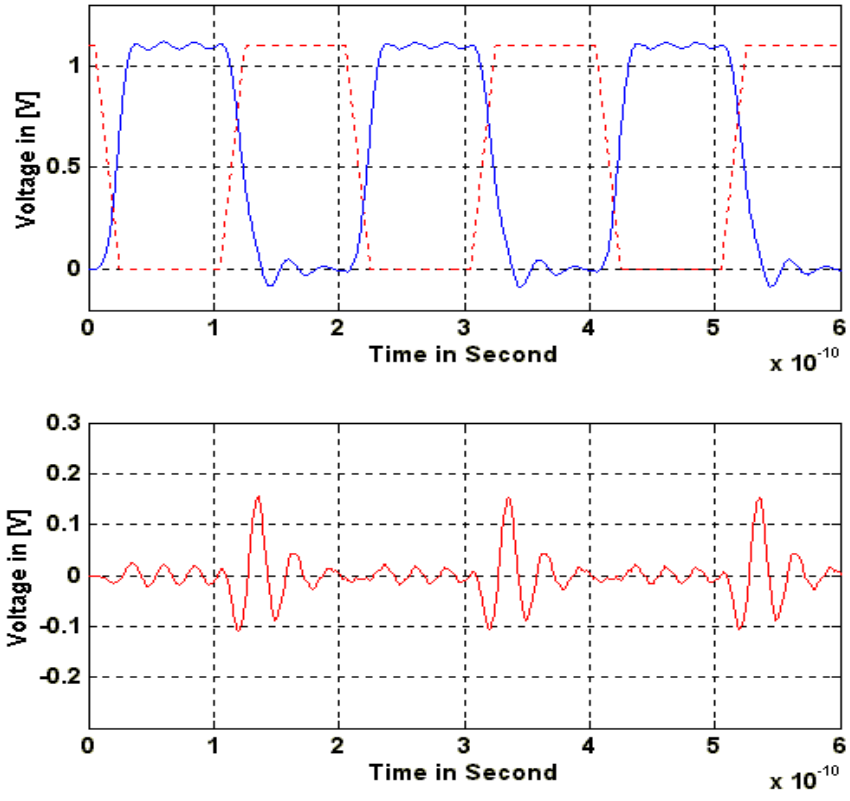


Figure 4.7 (a) Output voltage of the driver at Port 1
(b) Differential noise near the driver from Test Case 1

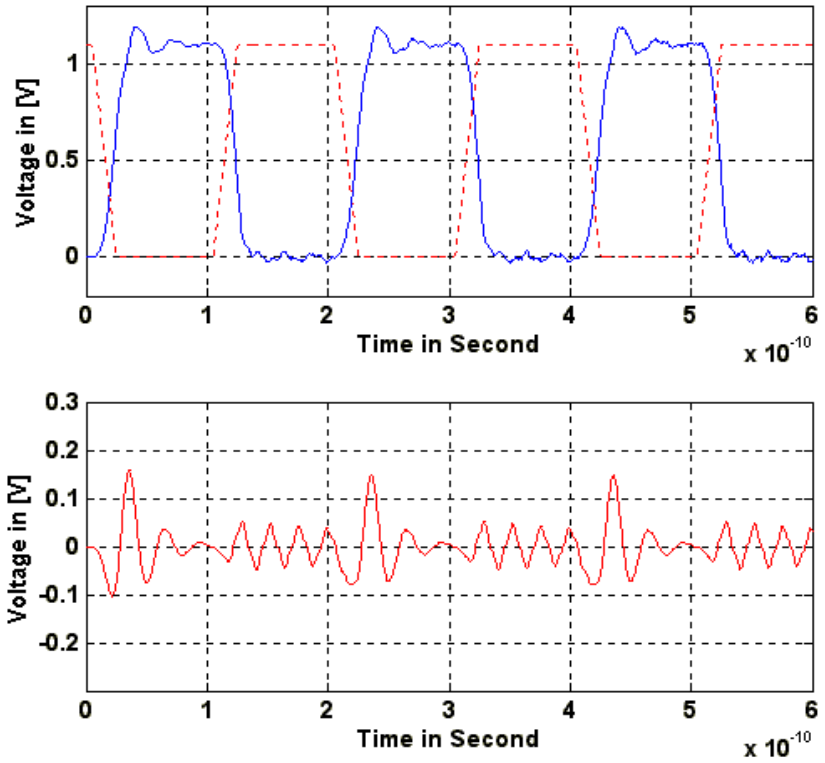


Figure 4.8 (a) Output voltage of the driver at Port 1
(b) Differential noise near the driver from Test Case 2

From Figure 4.7(b), most of the noise occurs during the high to low transition of the driver; very little noise occurs during the low to high transition. This can be explained based on the return currents. When the transition is from low to high, the driver connects the power line to the transmission line through the PMOS transistor. Current flows into the transmission line and the return current flows on the power line. The current loop is completed through the power line, the transmission line and the mutual capacitance between the transmission line and the power line. Since the ground line is not a part of the current loop, it does not excite any voltage disturbance between the power and ground line. However, when the transition is from high to low, the driver connects the transmission line

to the ground line through the NMOS transistor, thereby causing noise. Figure 4.8(a) and (b) show the output voltage of the driver at Port 1 and differential noise near the driver for Test Case 2. From Figure 4.8(b), the noise occurs during the low to high transition of the driver and little noise occurs during the high to low transition.

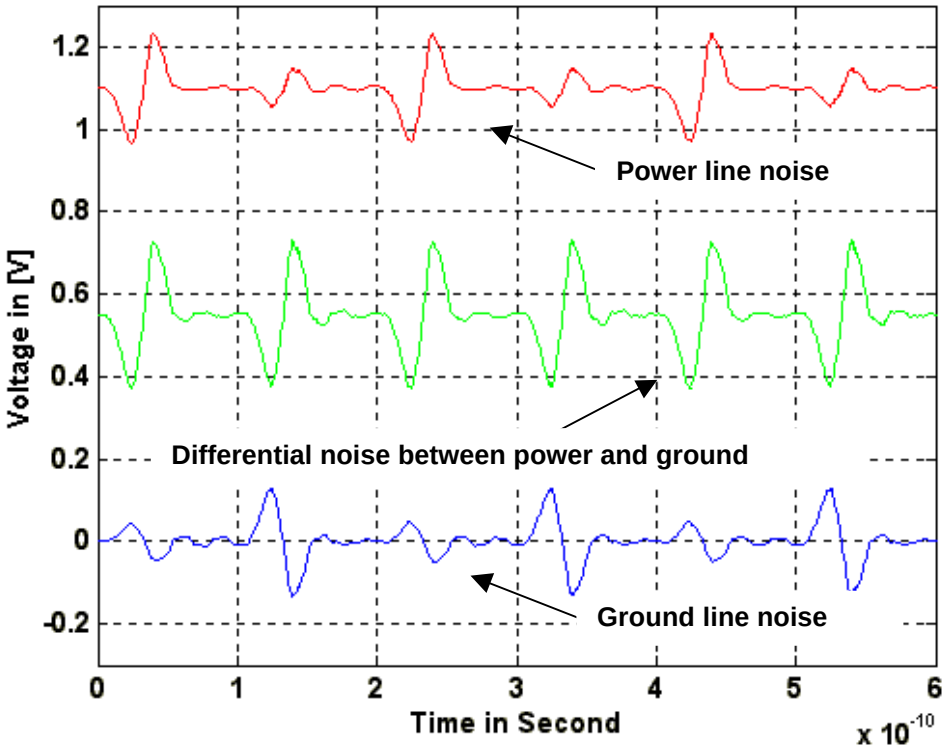


Figure 4.9 Power supply noise near the driver from Test Case 3

This behavior further substantiates the noise signature discussed earlier due to the return currents. Figure 4.9 shows power supply noise near the driver for Test Case 3. From Figure 4.9, the noise during the low to high transition of the driver is almost the same as the noise during the high to low transition. This is due to the symmetric structure whereby the signal line is sandwiched between the power and ground lines, causing equal return currents on the two lines.

IV.4 Simulation of long bus lines with an on-chip power grid

In order to study the noise due to return current, long bus lines were simulated along with an on-chip power grid structure consisting of 4 metal layers discussed in Chapter 2. Figure 4.10 shows the on-chip bus structure along with a power grid. The size of the power grid is 1500um by 1500um. Eight bus lines were inserted between power and ground lines at the top most metal layer. Each bus line has a thickness of 1um, width of 3um and length of 1500um. Four bus lines were activated with a driver (5 GHz clock signal) while 4 bus lines were held quiet in the low state.

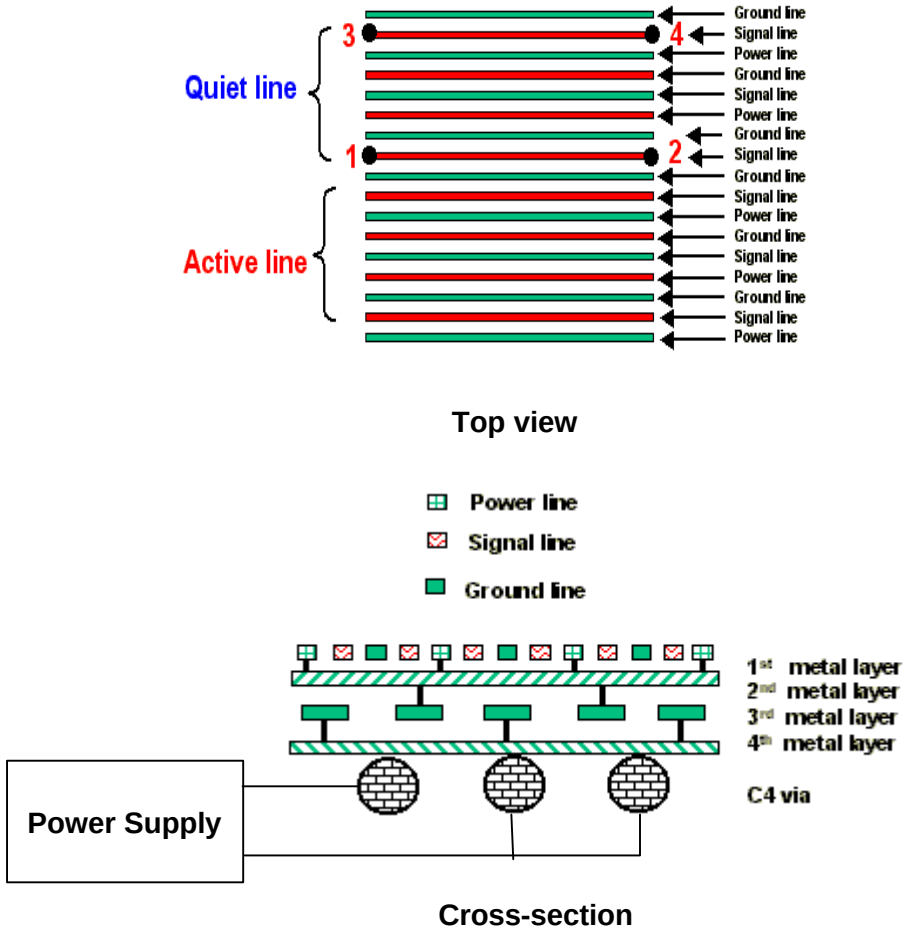


Figure 4.10 On-chip bus structure in power grid

The driver was connected to the left end of the power and ground line at the top most metal layer. In order to amplify the noise effect due to return current, bus line-to-line coupling was removed and bus line to power grid coupling was included. Figures 4.11(a) and (b) show the return current distribution at the top metal layer consisting of power line, ground line and signal line for Low to High and High to Low transition, respectively. In Figures 4.11(a) and (b), the striped red color and striped blue color show the positive and negative direction of the current, i.e., the right side and the left side, respectively. It can be seen that equal amount of return current flows on the power and ground line with the reference to the signal line due to the symmetric structure of the on-chip power grid, as mentioned earlier.

The noise due to return current was observed at the 4 ports (1,2,3 and 4) shown in Figure 4.12. Figure 4.12 (a)-(d) shows the noise response at the ports, 1,2,3 and 4 in order, which is the differential noise between the signal line and the nearest ground line. As can be expected, the highest noise occurred at port 1 next to the active drivers, as shown in Figure 4.12(a). The quiet signal line is affected by the near end switching drivers through mutual inductive and capacitive coupling between the power-ground lines and signal line which provide the return current path. For Figure 4.12(a)-(d), as can be seen, there is a delay of the noise propagation due to the proximity effect. Thus the noise response at port, 4, has the largest delay, as shown in Figure 4.11(d). Also, the noises at the ports, 2,3 and 4 are growing in amplitude due to the mutual inductive and capacitive coupling as time increases.

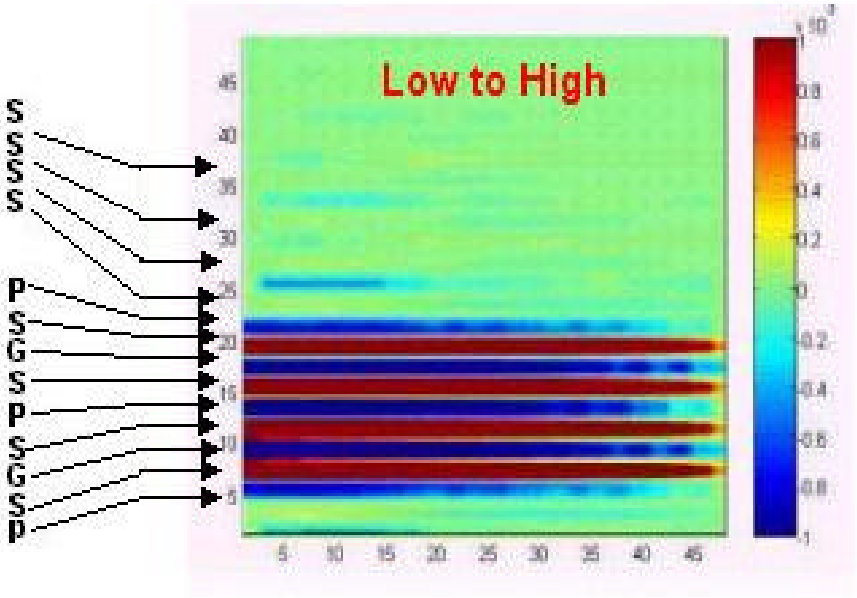


Figure 4.11(a) Return current at the top metal layer for Low to High transition

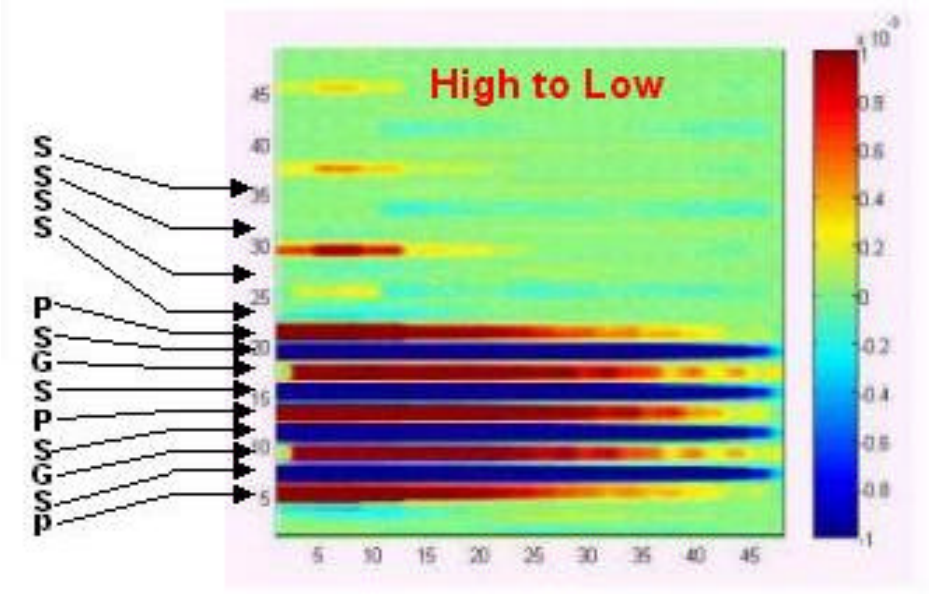


Figure 4.11(b) Return current at the top metal layer for High to Low transition

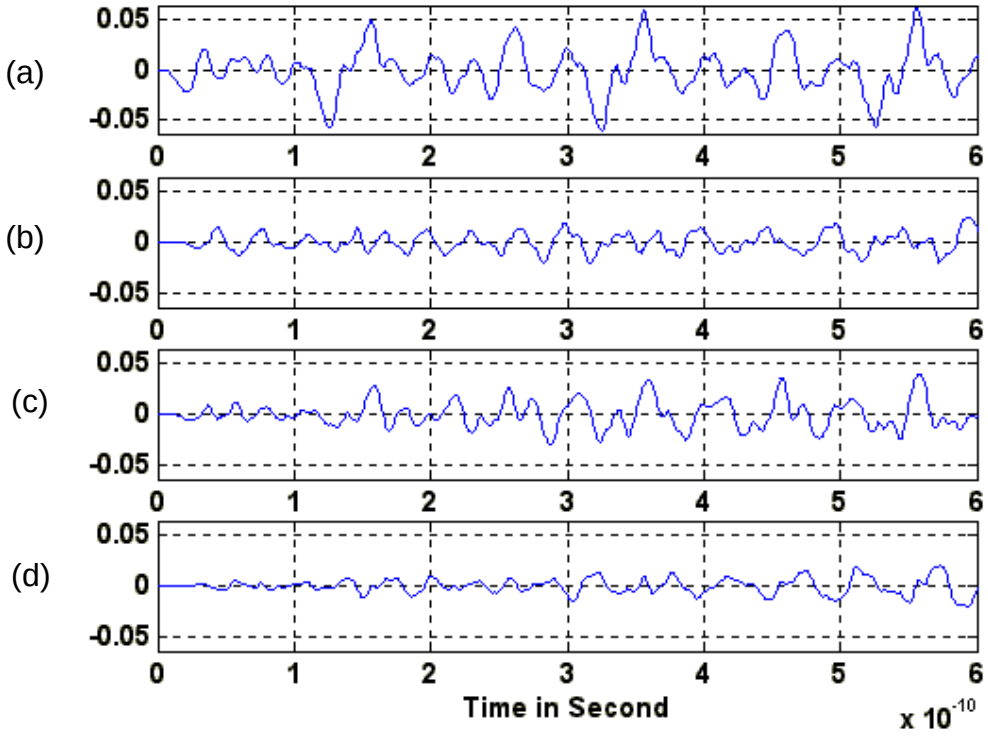


Figure 4.12 Noise response at ports 1,2,3 and 4

IV.5 Summary

In this chapter, the FDTD algorithm, which includes the mutual inductance and coupling capacitance, was discussed. This formulation was verified through a simple coupled structure using SPICE, showing good correlation between SPICE and circuit FDTD. It was noted that the circuit FDTD method can replace SPICE for the simulation of a large coupled system that includes the interaction between the on-chip interconnect and the on-chip power grid. Also the circuit FDTD method was used to simulate on-chip bus lines and the behavior of the transient noise was discussed, based on the return current path.

Chapter V

Package and Board Power Distribution

The International Technology Roadmap for Semiconductors (ITRS) projects integrated chips with feature size of 80nm, supply voltage of 0.9V, power dissipation of 170W and an on-chip clock frequency of 5.17 GHz in the year 2005. These requirements become even more stringent in the year 2016 where feature size of 25 nm, supply voltage of 0.4V, power dissipation of 288W and an on-chip clock frequency of 29 GHz is projected for high speed processors. This is shown in Table 1 for high performance applications in years 2001 - 2016.

Due to the fast switching speed of the circuits that result in sudden current demand, noise is generated in the system that can degrade performance. A major source of this noise can be attributed to the power delivery system (PDS) of the package and board, which if poorly designed can result in ground bounce, power supply compression and electromagnetic inference (EMI). The effect of these noise sources is amplified for small supply voltages and can lead to excessive increase in circuit delay, clock skew and PLL jitter. For future CMOS systems, one methodology to suppress noise is to design the PDS by identifying

a target impedance, which has to be met over a broad frequency range. This parameter can be computed from the ITRS by specifying a 10% allowed ripple on the voltage supply rails using Ohm's law as follows [39]:

$$Z_T = \frac{V_{dd} \times 0.05}{I} \tag{5.1}$$

where I is the current drawn by the microprocessor, which can be computed using the Power - Voltage relation, as shown in Table V.1. For example, in year 2005, a target impedance of $0.48\text{m}\Omega$ is required using Eq.(5.1). Based on the ITRS voltage and power projections, the target impedance is expected to reduce by a factor of 2 per computer generation, with a target impedance requirement of $0.06\text{m}\Omega$ in the year 2016. This is 16 times lower than the $0.93\text{m}\Omega$ required in 2001, which is alarming. Since current transients cause voltage fluctuations, a high speed computer system has to meet the target impedance over a large band width (at least DC-5GHz in year 2005) depending on the processor function, which includes data transfer to/from hard disk, data transfer to/from DRAM or on-chip processing. This makes the design process very complex. In addition to suppressing noise by maintaining a small self-impedance, a target transfer-impedance is also required between the processor and noise sensitive areas of the system.

Table V.1 2001 ITRS - High Performance

Year	Feature (nm)	Power (W)	Vdd (V)	Current (A)	Chip Freq. (MHz)	Target impedance (mOhm)
2001	150	130	1.1	118	1700	0.93
2003	107	150	1.0	150	3090	0.67
2005	80	170	0.9	189	5170	0.48
2007	65	190	0.7	271	6740	0.26
2010	50	218	0.6	363	12000	0.17
2013	35	251	0.5	502	19000	0.1
2016	25	288	0.4	720	29000	0.06

Since power is supplied to the integrated circuits through the package and board, the design of the power distribution network in the package and board is very important. An integral part of the power distribution network are decoupling capacitors which act as reservoirs of charge for the switching circuits. Based on the current demands, low-frequency, mid-frequency and high-frequency capacitors are required which need to be appropriately placed to ensure that the target impedance requirements are met. This requires the optimization of the PDS impedance in the presence of decoupling capacitors.

The focus of this chapter is the analysis of the PDS in the package and board. This has been combined with the on-chip power distribution impedance in later chapters.

This chapter is organized as follows. Section 1 discusses the power distribution network followed by distributed power planes in Section 2 and its equivalent circuit model in Section 3. Section 4 discusses the extension to multiple planes using the skin effect approximation. Section 5 discusses the effectiveness and placement of decoupling capacitors followed by a summary in Section 6.

V. 1 Power distribution network

The design of the power and ground planes arising in power distribution networks is an important area in high-speed digital systems. The power distribution network consists of a switching regulator, power and ground planes in the motherboard, power and ground planes in the package, and decoupling

capacitors, as shown in Figure 5.1 [61]. The network supplies voltage and current to the drivers and receivers that generate and receive the signals. A major challenge in the design of planes, which form an integral part of the power distribution system (PDS) for gigahertz (GHz) packages and boards, is the supply of clean power to the switching circuits. A major problem arising in power distribution networks is simultaneous switching noise (SSN) which is induced by the power and ground inductance. It has been recognized that power supply noise induced by a large number of simultaneously switching circuits in a printed wiring board (PWB) or multi-chip module (MCM) can limit the performance of the system [62].

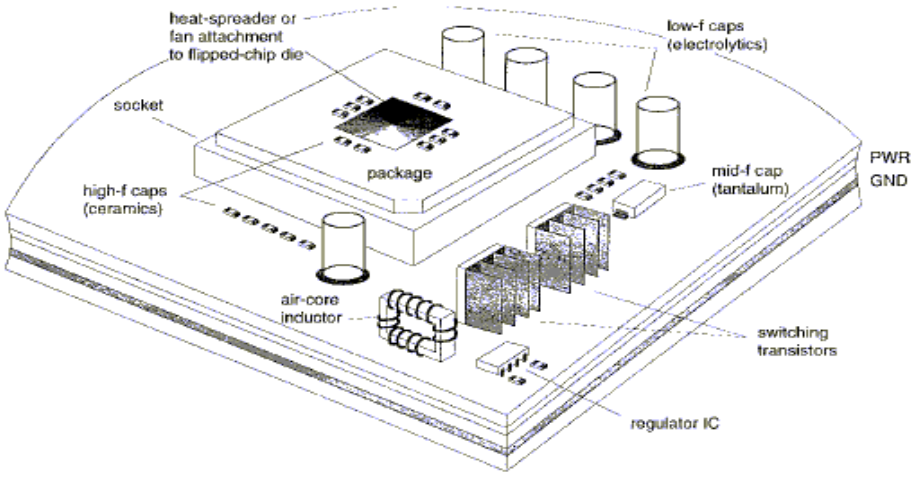


Figure 5.1 Power distribution network to a microprocessor

As clock speeds increase, and signal rise time and supply voltages decrease, the power supply noise, commonly known as delta-I noise or switching noise, appears as an undesired voltage fluctuation on the power/ground planes. This is caused by the fast transient currents that excite cavity modes between the

planes during the switching activity of the digital circuits [44]. Hence, the response of planes becomes very important at higher frequencies, especially beyond 100MHz. At these frequencies, power and ground planes behave as distributed networks that can support standing waves, which is the focus of this chapter.

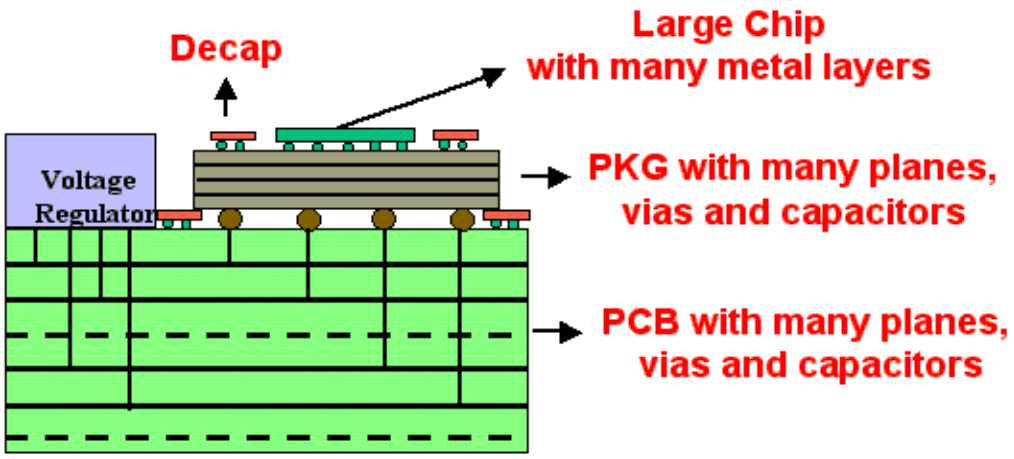


Figure 5.2 Chip, package and board

In [6] and [39], SPICE models have been used to analyze power/ground planes. However, as the size and frequency of the power distribution network increases, the use of SPICE is limited due to larger memory requirements and computational time. In a realistic package/board, since the PDS consists of numerous vias, decoupling capacitors, signal lines, and multiple plane layers, the number of transmission line segments required may become very large, as shown in Figure 5.2. As a result, large memory requirements and a considerable CPU run time are required for analysis. In [63], using the transmission matrix

method, a more efficient technique for solving power distribution network problems has been proposed.

In [44], an analytical solution consisting of a double infinite series has been used for calculating the impedance of plane pairs. The nonlinear solution has been converted to a linear solution for constructing spice models in [44]. This method is limited to rectangular planes. The method used in [44] is limited to a single plane pair. In this chapter, the method presented in [44] has been extended to multiple planes.

V. 2 Distributed Power Planes

An integral part of the power distribution network in gigahertz systems are planes in the package and board. Planes result in a small ohmic drop for DC

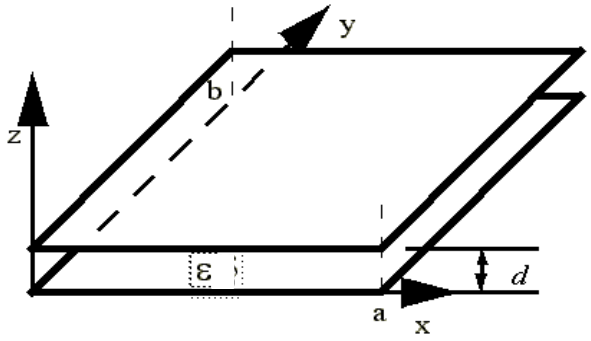


Figure 5.3 Plane structure

power distribution. At low frequencies, the planes behave as a capacitor with a low impedance. As the excitation frequency increases, the plane behaves as a parallel plate waveguide supporting radial waves. Since the structure is open ended (magnetic wall along the edge), it resonates at discrete frequencies.

This leads to an impedance variation with frequency of the plane structure, which needs to be computed. In this section, only two planes (one plane pair) are considered. The method presented in this section has been extended to multiple planes based on a skin effect approximation in the next section.

Consider the structure shown in Fig.5.3 which consists of two planes of dimensions axb, separated by a dielectric of thickness '*d*' and permittivity, 'e'. With the assumption that a,b >> *d* where *d* << l (the wavelength) which is true in all electronic packages including single chip and multi-chip modules, Maxwell's equations can be solved in terms of the impedance matrix Z at port locations on the plane using the Green's function [41-44], resulting in

$$Z_{ij}(w) = jwmd \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} \frac{e_n^2 e_m^2}{(k_{nm}^2 - k^2)} f(x_i, y_i) f(x_j, y_{ji}) \qquad (5.2)$$

where $f(x_i, y_i) = \cos\frac{2mpx_i}{2a} \sin c\frac{mpt_{xi}}{2a} \cos\frac{2npy_i}{2b} \sin c\frac{npt_{yi}}{2b}$, ($x_i$,$y_i$), ($x_j$,$y_j$) are the port locations, (t_{xi},t_{yi}), (t_{xj},t_{yj}) are the dimensions of the ports, $k = k' - jk''$ with $k' = w\sqrt{em}$ and $k'' = w\sqrt{em}(\tan d + r/d)/2$ for small losses, $k_{nm}^2 = (mp/a)^2 + (np/b)^2$ where *m*, *n* are the propagating modes on the planes, r is the skin depth, d is the dielectric loss angle and w is the angular frequency. Equation (5.2) is valid when t_x,t_y<< l, which in turn is valid in the frequency range of interest. The Z matrix generated from Eq.(5.2) captures both the self-impedance and the transfer-impedance and hence represents a complete analytical solution for the plane structure [41-44].

V. 3 Cavity resonator model

Based on [41],[44] and [45], the plane impedance can be represented using passive circuit elements whereby the equivalent circuit is formed using parallel resonant circuits and ideal transformers as

$$Z_{ij}(\omega) = \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} \frac{N_{mni} N_{mnj}}{1/\, j\omega L_{mn} + j\omega C_{mn} + G_{mn}} \tag{5.3}$$

where $L_{mn} = d/(\omega_{mn} ab\varepsilon)$,

$C_{mn} = ab\varepsilon/d$,

$G_{mn} = (ab\varepsilon/d)\omega_{mn}\left(\tan\delta + (\sqrt{2/\omega_{mn}\mu\sigma})/d\right)$,

and $N_{mni} = \varepsilon_n \varepsilon_m \cos\frac{m\pi x_i}{a} \sin c\frac{m\pi t_{xi}}{2a} \cos\frac{n\pi y_i}{b} \sin c\frac{n\pi t_{yi}}{2b}$.

G_{mn} can be approximated as $G_{mn} = \left(ab\varepsilon/d^2\right)\sqrt{2\omega_{mn}/\mu\sigma}$ for low dielectric loss ($\tan\delta << r/d$). For m=0 and n=0, ω_{mn} = 0 and so the only term remaining in the resonator model is due to the capacitance C_{00}, which represents the static mode. Fig. 5.3 shows the equivalent circuit diagram for *2* ports and '*mn*' modes. Since N_{00i} for the (0,0) mode is 1 for any port, the capacitor C_{00} is connected directly to the ports without transformers, as shown in Fig. 5.4. This model is based on waveguide theory for the planes where the circuit characteristics in the vicinity of a resonant frequency can be expressed in terms of G, L and C parameters. Since the planes act as cavity resonators, the capacitor 'C' is used for storage of electric energy and the inductor 'L' for storage of magnetic energy, whereby at the resonant frequency, there is an exchange of energy between the two elements. The conductance 'G' is used to account for the losses in the circuit.

Here, with m=n=0, the tank circuit is reduced to C_{00} which corresponds to the charging and discharging of the static capacitance of the planes. Also, since each resonator circuit contains mode-dependent component values around the mode resonance frequency, the whole circuit naturally reflects the frequency-dependent behavior that has been captured using lumped passive elements. The modeling approach for a single plane pair can be extended to multiple planes under the assumption that skin effect is prominent in high-speed systems, as discussed in [40,46].

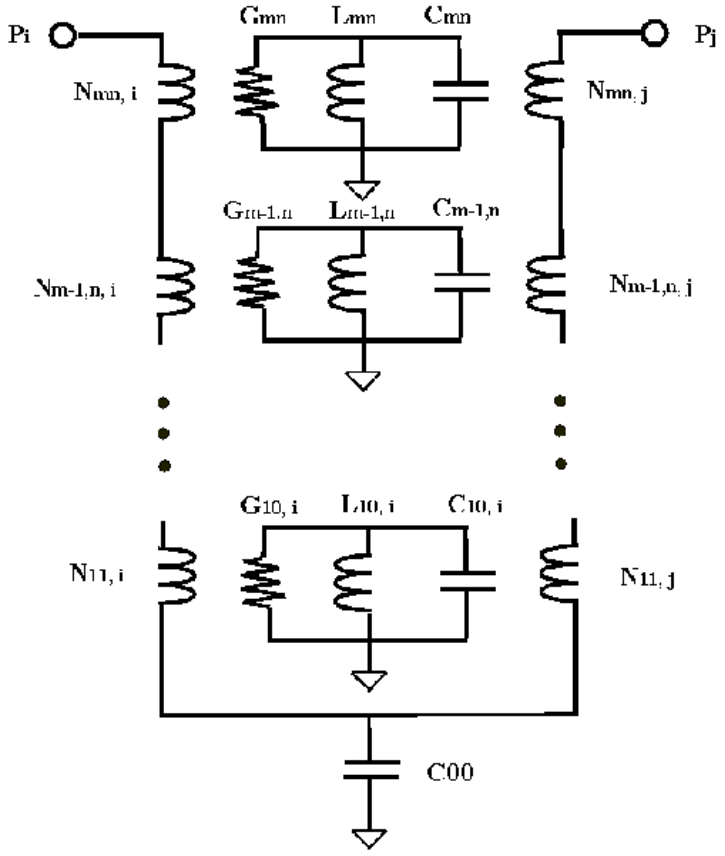


Figure 5.4 Equivalent circuit of the plane model for two arbitrary ports

V. 4 Extension to multiple planes

In [47], a method has been proposed for limiting the SSN noise by optimizing the impedance profile of the PDS. In [47], the frequency response of the PDS is computed by incorporating decoupling capacitors through the impedance matrix derived in [48]. However, the method is limited to two planes with multiple decoupling capacitors. In this section, a technique has been presented for extending the method discussed in [48] to multiple planes. This approximation is valid for high speed systems where the skin effect is prominent. The method lends itself to the rapid computation of the impedance matrix for multiple planes. Since analytical expressions are used for computing the impedance matrix, decoupling capacitors can be placed arbitrarily on a non-uniform grid. However, the method is currently limited to solid rectangular planes. This section also does not include the effect of vias on the frequency response of the planes. In [49], a discrete CTL model has been used to compute the S-parameters of multiple plane pairs. These results have been correlated with the results obtained using the method presented in this section.

Consider a three-plane stack-up, as shown in Fig 5.5, consisting of V1, V2, and V3 planes. The voltage values are arbitrary and could represent any logic voltage. Switching circuits draw current from the PDS, which are represented as current sources in Fig 5.4. For example, in a mixed signal module, V1 and V2 could represent digital and analog voltages, respectively, referenced to voltage V3 which is the global ground. The sources excite a cylindrical wave, which propagates outwards and bounces off the edge of the planes, causing standing

wave resonance. The magnetic field of the wave induces a current on the plane given by $\vec{J} = \hat{n} \times \vec{H}$ where $\hat{n}$ is the unit outward normal vector, $\vec{H}$ is the magnetic field and $\vec{J}$ is the induced current density flowing in the lateral direction. Due to the losses in the conductor, the induced currents $\vec{J}(z)$ in the cross section of the conductor is given by $\vec{J}(z) = J_o e^{-az} \hat{z}$ where 'a' is the attenuation constant. For frequencies at which the skin depth is less than the metal thickness 't', the current decays rapidly and the current density at the bottom of the plane V2 is zero. Hence the induced voltage between planes V2 and V3 is zero. Thus the planes are decoupled and the only coupling that is possible between plane pairs occurs at the port location, as will be discussed later. As an example, for copper, the skin depth is 9.3 um at 50 MHz. Thus the skin effect approximation is valid for frequencies above 50 MHz in most technologies such as FR4 and ceramics with metal thickness of 35 um and higher.

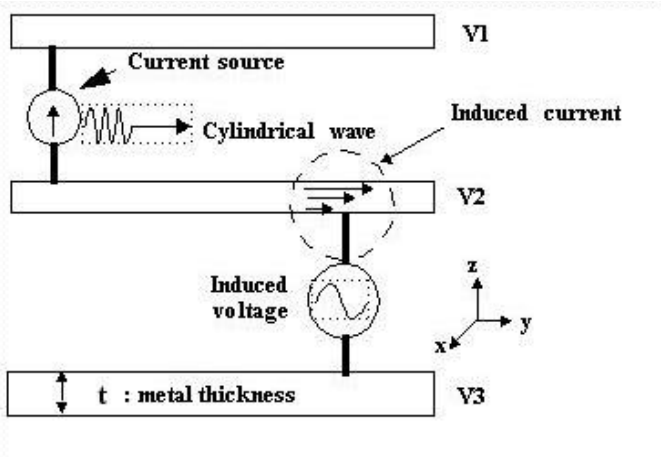


Figure 5.5 Skin effect approximation for plane-plane coupling

V. 4.1 Model to Hardware Correlation

Test case 1 : Test vehicle from Hewlett Packard

As mentioned earlier, though plane pairs can be decoupled, coupling between planes can occur at the port location. As an example, consider 3 planes with the bottom plane acting as the global ground, as shown in Fig. 5.6(a).

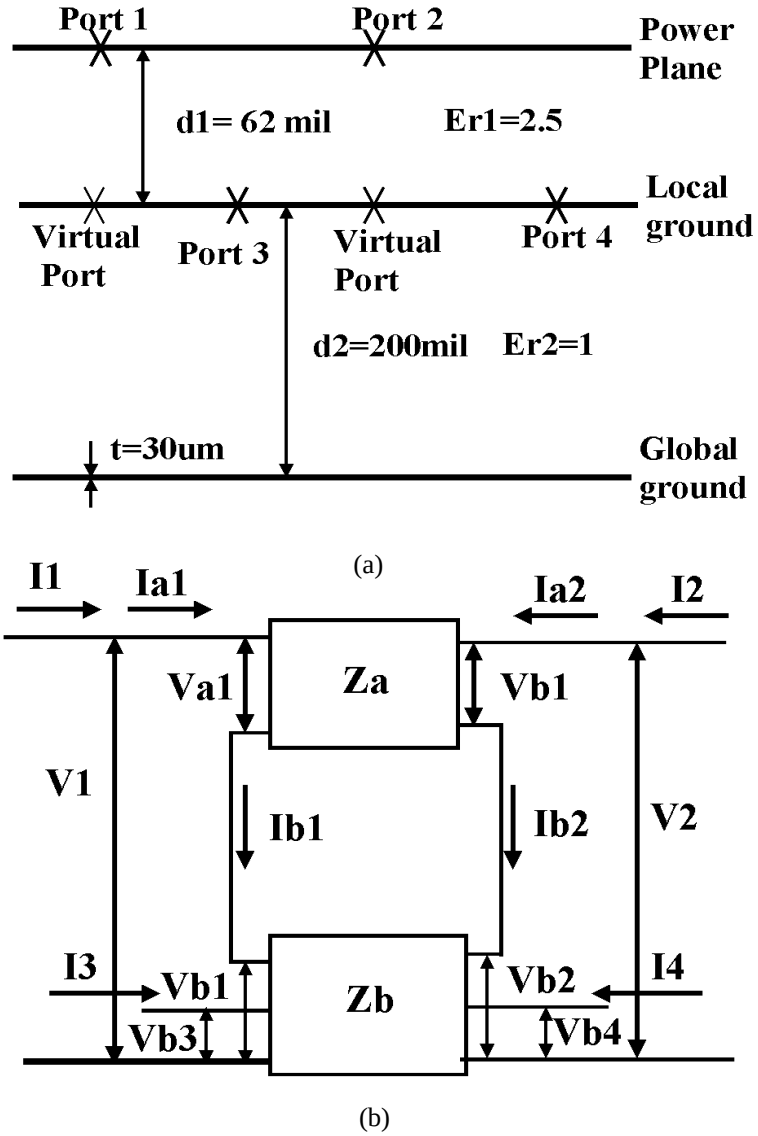


Figure 5.6 (a) Plane coupling through ports
(b) Equivalent network representation

As discussed in [49], the S-parameters were simulated at 4 ports with reference to the global ground with port locations and cross-section as shown in Fig 5.6(a). The plane response can be computed using the equivalent circuit shown in Fig 5.5(b) where the plane pairs are assumed to be decoupled. The PCB dimensions were 4 inches by 6 inches, 62 mils dielectric thickness, relative dielectric constant of 2.5 and copper conductivity of 5.7 $\mathrm{x}10^5$ Simens/cm with conductor thickness of 30 um. The distance between the local ground and the global ground was 0.2 inches. In the test vehicle, two test ports were located at Port 1(1 inch, 3 inch) and Port 2 (5 inch, 1 inch) on the power plane and the other two test ports were located at Port 3 (1 inch, 1 inch) and Port 4 (5inches, 3inches) on the local ground plane. The impedance matrix computed was for each plane pair by using Eq (5.4) and assuming virtual ports, as shown in Fig 5.6. Using the circuit representation in Fig. 5.6(b),

$$Z_{eq} = \begin{bmatrix} Z_{a11} + Z_{b11} & Z_{a12} + Z_{b12} & Z_{b13} & Z_{b14} \\ Z_{a21} + Z_{b21} & Z_{a22} + Z_{b22} & Z_{b23} & Z_{b24} \\ Z_{b31} & Z_{b32} & Z_{b33} & Z_{b34} \\ Z_{b41} & Z_{b42} & Z_{b43} & Z_{b44} \end{bmatrix} \tag{5.4}$$

where Z_{eq} is the equivalent impedance matrix for the structure. The equivalent impedance matrix, Z_{eq}, was computed, using the following network equation:

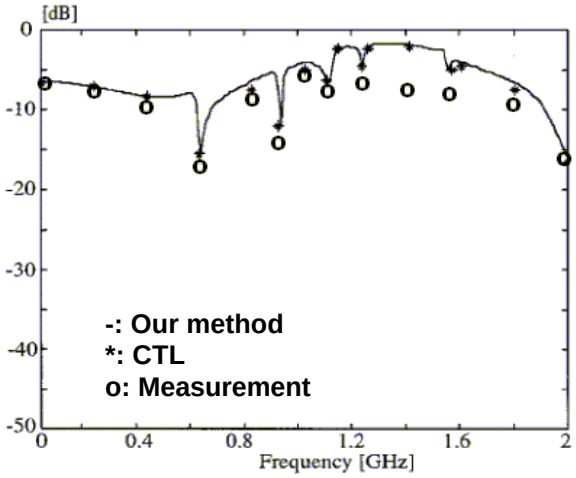
$$I1 = Ia1 = Ib1,\ I2 = Ib2 = Ia2,\ V1 = Va1 + Vb1,$$

$$V2 = Vb2 + Va2,\ I3 = Ib3\ ,\ \text{and}\ I4 = Ib4. \tag{5.5}$$

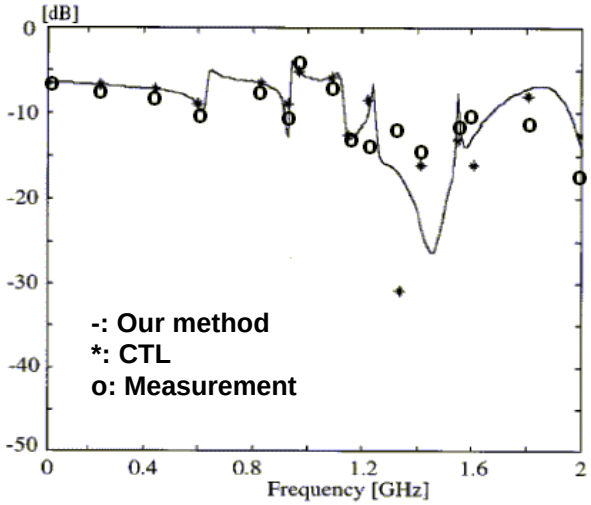
The Z_{eq} matrix in Eq.(5.4) was transformed to the S- matrix using the equation,

$$S = [Z_{eq} + Z_o]^{-1} \times [Z_{eq} - Z_o] \tag{5.6}$$

where Z_o is the port impedance. Figure 5.8(a) and (b) compares the computed result with the measurement from [49] where discrete coupled transmission lines (CTL's) were used for modeling power and ground planes. It shows good agreement from 50 MHz - 1 GHz. The discrepancy beyond 1 GHz can be attributed to via effects which have not been included in this section. Hence the error beyond 1 GHz is not due to the approximation used in this section.



(a)



(b)

Figure 5.7 Comparison of simulation results with [49]: (a) S13 and (b) S14

Test case 2 : Test vehicle from NTK

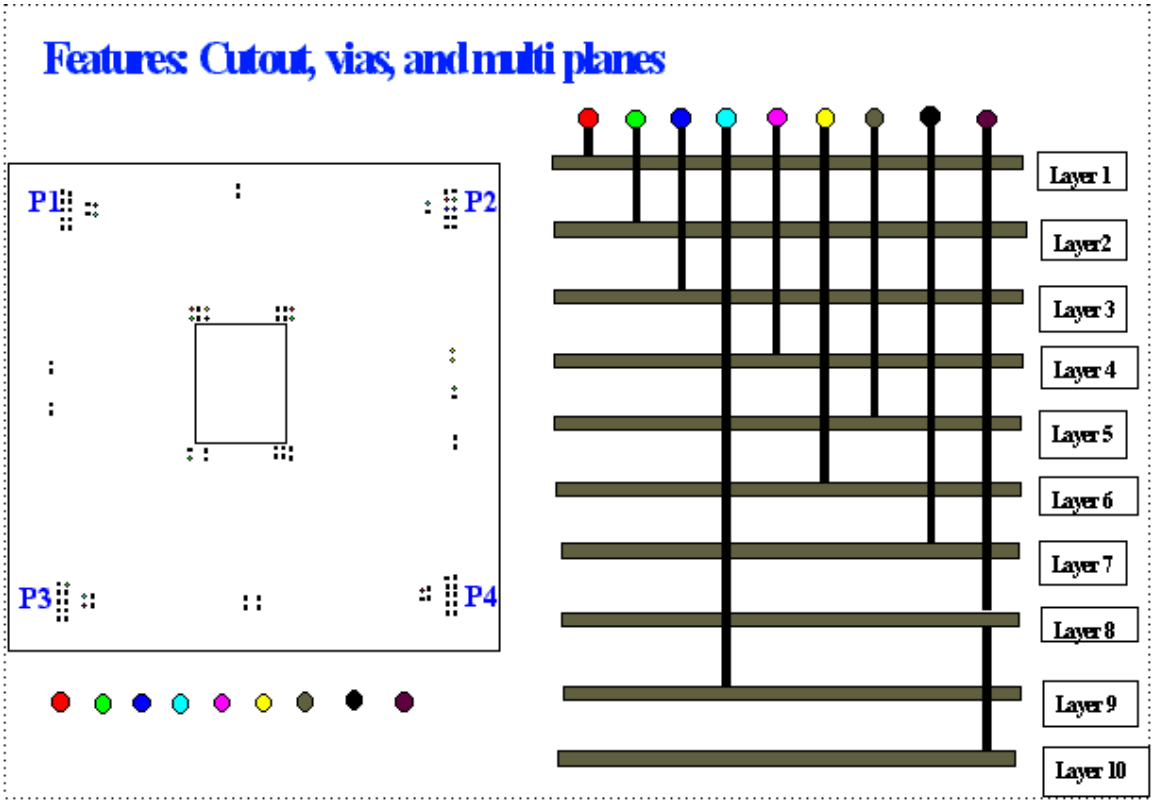


Figure 5.8 Top and side view of the ceramic test vehicle

The ceramic test vehicle, fabricated by NTK, consisted of 10 metal layers and 9 dielectric layers. The dimensions of the test vehicle were 4.753 cm by 4.753, 6 mils dielectric thickness, relative dielectric constant 9.8, and conductivity 0.67 $x10^5$ Siemens/cm with a conductor thickness of 10 um. Solid metal planes were stacked on each other with equal spacing of 6 mils between the layers. The first 3 layers out of the test vehicle were used for model verification. Four test ports were located at the coordinates (0.552 cm, 4.364 cm; P1), (4.241 cm, 4.364 cm; P2), (0.552cm, 0.424 cm; P3) and (4.241 cm, 0.424; P4) on the substrate.

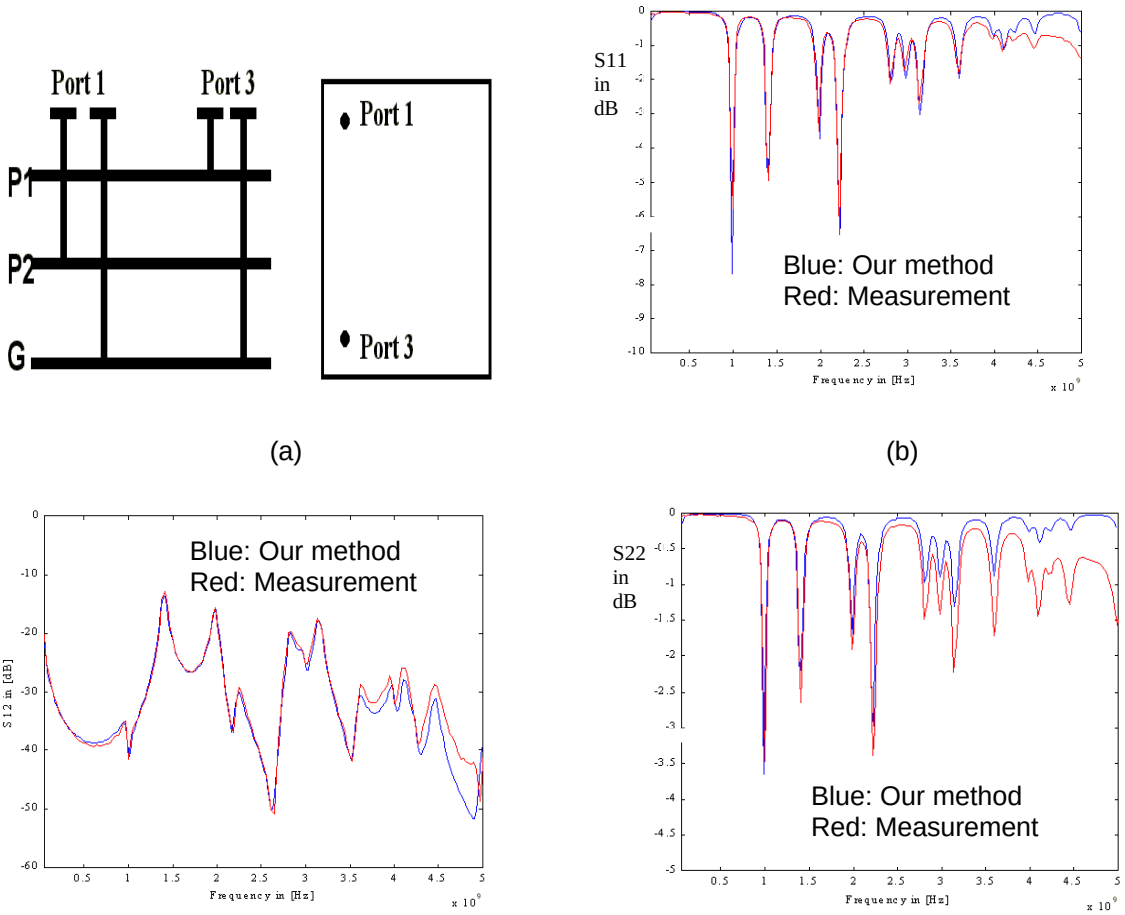


Figure 5.9 S-parameter measurement and simulation for the multi layered structure (a) Port configuration for measurement (b) S11 (c) S12 (d) S22

Figure 5.9(a) shows the top and side view of the ceramic test vehicle. The structure in Figure 5.9 was measured using a Vector Network Analyzer (VNA) and compared to simulations. Figure 5.9(b)-(d) shows the measured and simulated S-parameters between Port 1 and 3. The figure shows good agreement between measurement and simulation over the frequency band from 30 MHz to 3.5 GHz. A slight discrepancy is seen at higher frequencies. This deviation can be caused by the losses in the vias, which have not been included

in the model. Based on the results, the method presented in this section for multi-layered planes is valid over a frequency bandwidth of 3.5 GHz.

V. 5 Decoupling capacitors

Decoupling capacitors are required to provide enough current for the simultaneous switching circuit without disturbing the voltage level at the circuits when a large current surge occurs. Adding decoupling capacitors decreases the effective inductance in the power distribution network of packages and therefore reduces the simultaneous switching noise. A detailed understanding of the current path through the entire power distribution system is required prior to the placement of decoupling capacitors at the appropriate locations. The noise pulse width reflects the switching transition time of the circuits [50]. Typically simultaneous switching noise is generated by the fast transition of the on-chip or off-chip drivers, which causes high frequency noise [51]-[53]. However, when many circuits on a chip switch simultaneously and the current drawn is sustained for many cycles, low frequency noise is generated due to the resonance caused by interfaces. Therefore, a range of decoupling capacitors is required for supporting the switching circuits at the low frequency, mid frequency and high frequency range.

V. 5.1 Incorporation of decoupling capacitors

For an N-port plane system, the voltage at each port can be expressed as follows.

$$
\begin{aligned}
V_1 &= Z_{11}I_1 + Z_{12}I_2 + Z_{13}I_3 + \ldots\ldots + Z_{1N}I_N \\
V_2 &= Z_{21}I_1 + Z_{22}I_2 + Z_{23}I_3 + \ldots\ldots + Z_{2N}I_N \\
V_3 &= Z_{31}I_1 + Z_{32}I_2 + Z_{33}I_3 + \ldots\ldots + Z_{3N}I_N \\
&\bullet \\
&\bullet \\
&\bullet \\
V_N &= Z_{N1}I_1 + Z_{N2}I_2 + Z_{N3}I_3 + \ldots\ldots + Z_{NN}I_N
\end{aligned}
\qquad (5.7)
$$

In Eq (5.7), the voltage at the i-th port is given by

$$V_i = \sum_{j=1}^{N} Z_{ij} I_j \qquad (5.8)$$

where V and I are column vectors and Z is the N-port impedance matrix. Decoupling capacitors provide a compensation for the inductive part of the power distribution network. The decoupling capacitors can be represented as a one port system such that:

$$V_{cm}=Z_{cm}I_{cm} \quad \text{for m=N-M+1, ... N} \qquad (5.9)$$

where Z_{cm} and V_{cm} are the impedance and voltage for a single decoupling capacitor and ‘m’ represents the number of capacitors used. To ensure the continuity of current at the port location after attaching the decoupling capacitors,

$$I_k=I_l + I_c \qquad (5.10)$$

where I_k is the sum of the current in the l-th port and m-th decoupling capacitor, d_{lm} = 1 for m=l and otherwise d_{lm} = 0. Since ‘k’ and ‘l’ are dummy indices, from Eq. (5.7), (5.8) and (5.9),

$$V_i = \sum_{k=1}^{N} Z_{ik}[I_k - (V_{cm}d_{km})/Z_{cm}] \qquad (5.11)$$

Rearranging Eq (5.11),

$$V_i + \sum_{m=N-M+1}^{N} (Z_{im} / Z_{cm}) V_{cm} = \sum_{k}^{N} Z_{ik} I_k \qquad (5.12)$$

In matrix form, Eq (5.12) can be written as

$$[Zc][Vc]=[Z][Ic] \qquad (5.13)$$

where Zc is dimensionless, Z is the impedance matrix for the N port PDS, and Vc & Ic are modified column voltage and current vectors with decoupling capacitors, respectively. From Eq.(5.13),

$$[Vc]=[Zt][Ic] \qquad (5.14)$$

where $Z_t = Z_c^{-1} Z$ and Z_t is the N port impedance matrix with 'M' decoupling capacitors. The computation of the impedance matrix consists of two steps, namely, 1) computation of the N-port impedance matrix of the planes (Eq.5.2 and 5.3) and 2) modification of the impedance matrix to include the 'M' capacitors (Eq. 5.14).

The computational method discussed above has been implemented using a commercial software package, namely, MATLAB. The next section discusses the accuracy and salient features of the method.

V. 5.2 Test case : Validation with HSPICE

This section discusses several test cases that provide details on the accuracy, computation time and other features of the method that has been developed. The PDS consists of two planes that supply power to the chips with several decoupling capacitors attached to the power distribution network. Three types of decoupling capacitors have been used, as shown in Table 2. Since the

capacitors are surface mount components attached to the planes, the capacitors are non-ideal with ESR (equivalent series resistance) and ESL (equivalent series inductance) values, as shown in Table V.2.

Table V.2: Decoupling capacitor model

Type of Decap	ESR [Ohm]	ESL [H]	Capacitance[F]
Decap 1	0.3133	0.52E-9	100E-12
Decap 2	0.2084	0.52E-9	390E-12
Decap 3	0.1579	0.52E-9	1000E-12

Fig.5.10 shows the frequency response of the 3 kinds of decoupling capacitors, obtained using the impedance equation, $Z = R + jwL + 1/(jwC)$. In Table 2, each capacitor resonates with resonant frequencies of 6.979E08Hz, 3.534E08Hz, and 2.207E08Hz, respectively. Capacitor 1 has the highest resonant frequency and hence acts as a capacitor over the widest frequency band.

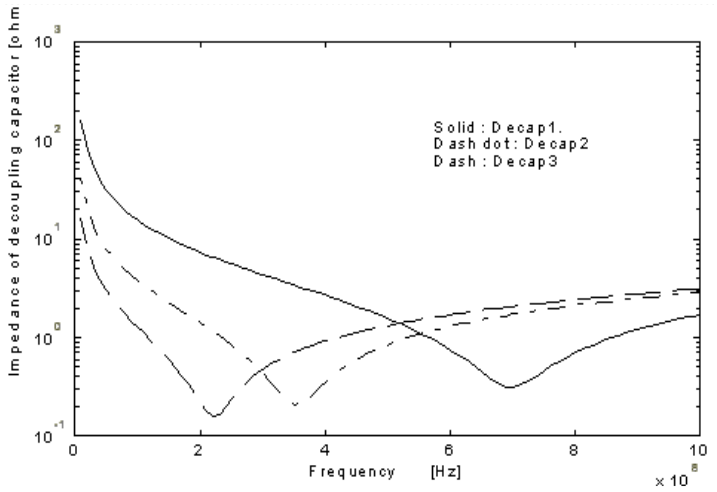


Figure 5.10 Frequency response of the decoupling capacitors

This enables the suppression of high frequency resonant peaks in the PDS. A test case was developed to check the accuracy of the method by comparing it to a model simulated using Hspice. The PDS was composed of two planes of size 4" by 6", dielectric thickness of 4 mil, ε_r=4, and copper thickness of 0.7 mil, as shown in Figure 5.11.

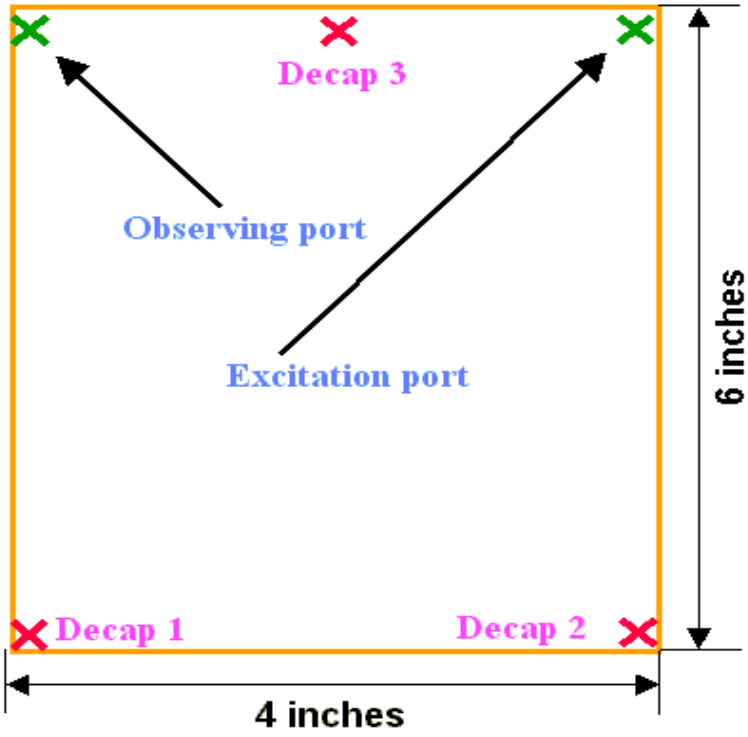
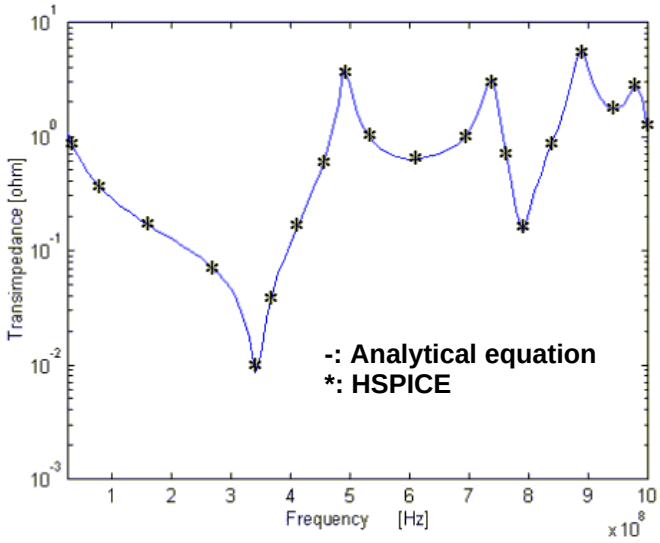


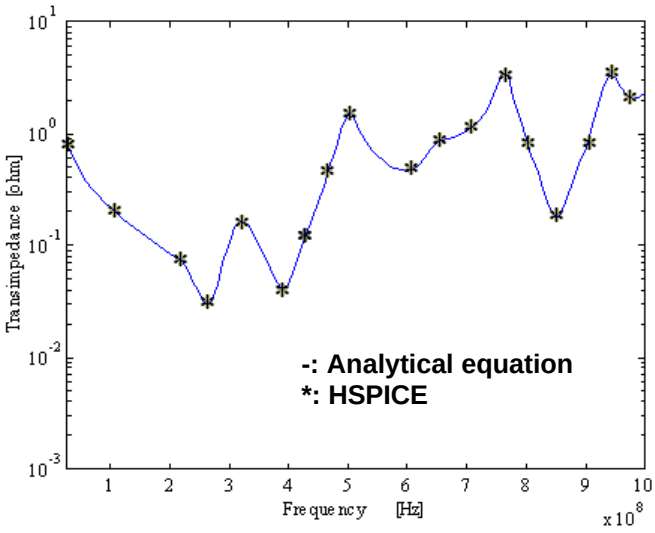
Figure 5.11 Plane structure with 3 decoupling capacitors

The Hspice deck consisted of an 8 by 8 array of uniform transmission lines using the method discussed in [54]. The array was excited at one corner and probed at an adjacent corner with the 3 capacitors populated at locations, (0.0",6") for Decoupling capacitor 1, (0.0", 0.0") for Decoupling capacitor 2 and (2",6") for Decoupling capacitor 3. The excitation point and observation point were (4",6") and (0", 6"). Fig.5.12(a) shows the results and the Hspice simulation results with

no decoupling capacitor and Fig.5.12(b) shows the results and the Hspice simulation results with decoupling capacitors. As can be seen, there is good agreement between the two results, which validates the approach discussed in this section.



(a) Transfer-impedance with no decoupling capacitor



(b) Transfer-impedance with 3 decoupling capacitors

Figure 5.12 Verification of the presented method

V. 5.3 Capacitor placement and decoupling capacitor effectiveness

The analysis of noise interaction in high speed, high frequency packaged systems is critical for maintaining signal integrity and for designing electronic systems that are compatible with the environment. Sensitive chips in close proximity to high speed digital blocks need to be protected from high frequency noise generated by the digital circuits, which can be coupled to the sensitive chip through the PDS [54]. In this section, the placement of capacitors on the board has been analyzed to gain a deeper understanding of the effectiveness of decoupling capacitors.

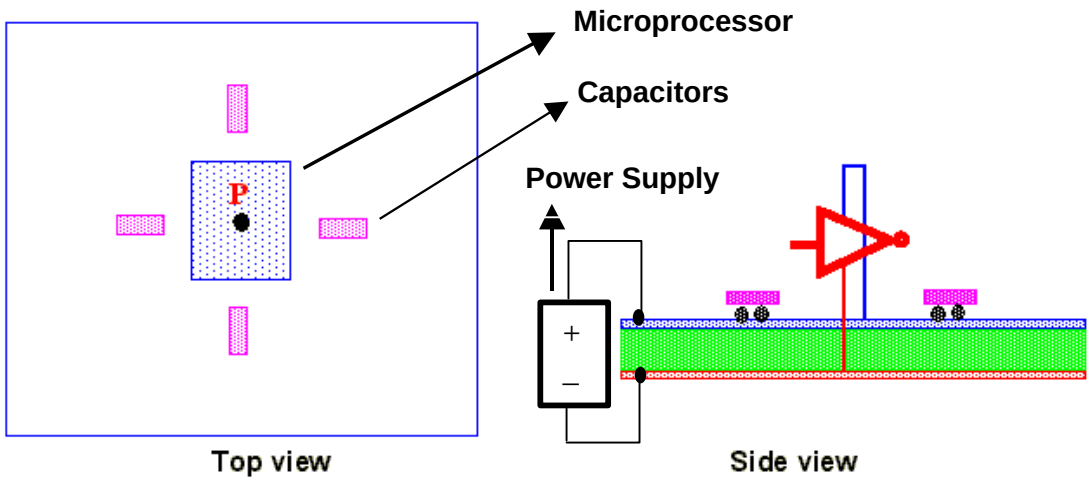


Figure 5.13 Layout of the package

Figure 5.13 shows the layout of the package which consists of a microprocessor and four decoupling capacitors with parasitics; ESL=0.1nH, ESR=50e-3 Ohm and C=300nF. The dimension of the test vehicle was 4.753 cm by 4.753 cm with 1.5 mils dielectric thickness, dielectric constant 9.8, conductivity 0.67 $x10^5$ Simens/cm and conductor thickness 10 um. One test port was defined at the center of the package to represent the microprocessor. Three test cases,

namely, with no capacitors (Test Case 1), module capacitors (Test Case 2), and on-chip capacitors (200nF) (Test Case 3), were used in the study. Figure 5.14 shows the self-impedance for Test Cases 1,2 and 3. From Fig. 5.14, on-package decoupling capacitor improves the impedance profile in the low frequency range, while an on-chip decoupling capacitor suppresses plane resonance and gives a good impedance profile over a broad frequency band. For the time domain simulation, a chip model that mimics a switching circuit was developed based on TSMC 0.25 um process technology. Figure 5.15(a) shows the transient current output based on the switching circuit model that was combined with the equivalent circuit of the plane model [46].

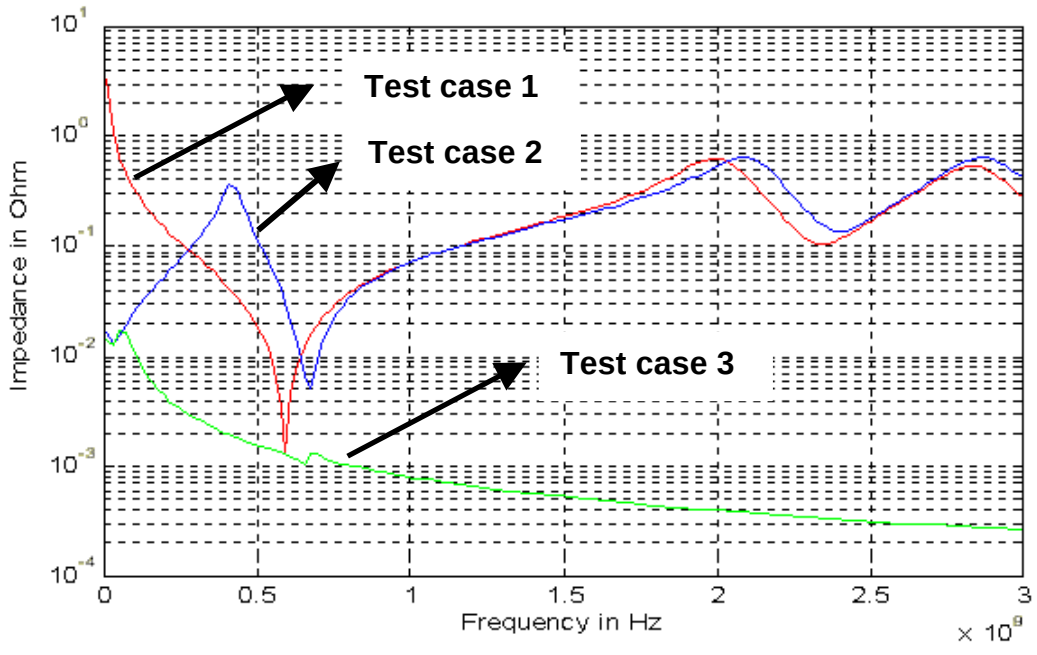
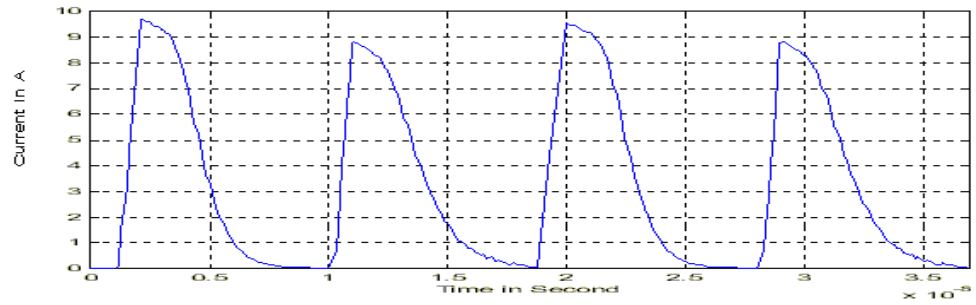


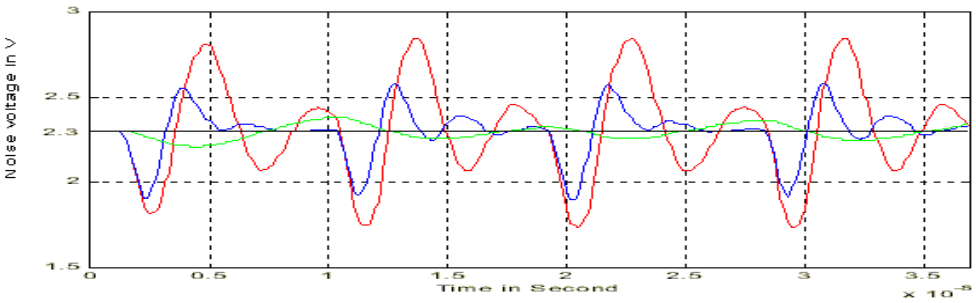
Figure 5.14 Impedance seen from the microprocessor
Red line: Test case 1, Blue line: Test case 2, Green line: Test case 3

Figure 5.15(b) shows the time response for Test Case 1, 2 and 3. The current transient had a slew rate of 9.6A/ns. From Fig. 5.15(b), it can be seen that the peak noise for Test Case 2 is reduced from 500 mV to 380mV and the noise voltage due to a slow current slew rate is significantly reduced, which translates to the usefulness of package decoupling capacitors in the low frequency region. When both the on-chip and package decoupling capacitors were used (Test Case 3), the peak noise was reduced to 100mV. It can be clearly seen that on-chip decoupling capacitors are required to lessen the high frequency noise, while the package decoupling capacitors are not very effective for high frequency decoupling. This is due to the finite ESR and ESL of the capacitors. An embedded decoupling capacitor is a good alternative for improving the decoupling capacitor effectiveness.

This section relied on SPICE for obtaining the transient and steady state response. The models included the planes and a simple current source model for the chip. This model therefore simplifies the interaction between the chip- and package. As part of this dissertation the SPICE models were translated into models that are compatible with the FDTD method. This integration enables a deeper understanding of the interaction between the chip and package which could enable the design of reliable systems in the future.



(a)



(b)

Figure 5.15(a) Current transient from the switching circuit model
(b) VDD-GND differential noise at the microprocessor
Red line: Test Case 1 (No package and on-chip capacitors)
Blue line: Test Case 2 (Package capacitors only)
Green line: Test Case 3 (Package capacitors and on-chip capacitors)

V.6 Summary

This chapter discussed the power distribution network followed by distributed power planes in the package and board, which represent an integral part of the power distribution network in gigahertz systems. Based on the physical phenomena observed in packages and boards, a technique for extending the single plane pair cavity resonator model for multiple plane pairs was developed. This model was verified through measurements. In addition, the effect of decoupling capacitors on package and boards was analyzed.

Chapter VI

Modeling Package and Board Planes using Circuit FDTD

Power planes are used to deliver power to both logic core and I/O circuits in modern computer systems. With each computer generation, the amount of power required is continuously increasing as depicted by ITRS [64]. As silicon technology advances, transistor scaling has required that the power supply voltage be reduced. Since the current delivery requirements on the power distribution network has gone up and the tolerance for noise has gone down, power planes need to have a low impedance at higher frequencies [57], as described in Chapter V.

In the previous chapter, the cavity resonator model for analyzing planes has been described in detail. Though the model is limited to solid rectangular planes, it provides an analytical solution which can be applied to planes in the package and board. As shown in the previous chapter, the model is extendable to multiple planes and can include decoupling capacitors. In this chapter, the cavity resonator model has been implemented using the FDTD method described in the earlier chapters.

VI.1 Resonator model using the Finite Difference Time Domain Method

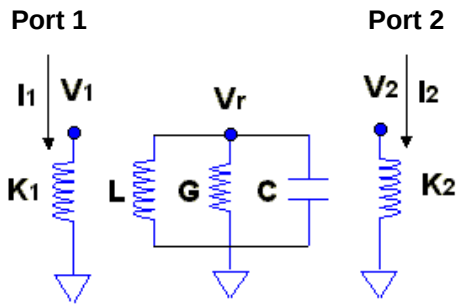


Figure 6. 1(a) A resonator circuit with two transformers

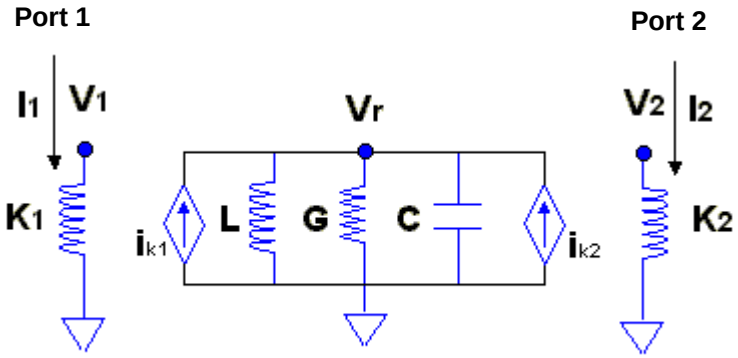


Figure 6.1 (b) Detailed circuit information of the resonator circuit

This section discusses the implementation of the resonator cavity model [44] based on the circuit FDTD method. Figure 6.1(a) shows a resonator with inductance L, conductance G, capacitance C and two transformers, which forms a sub-circuit of the model described in Chapter V. This circuit can be converted to Figure 6.1(b) where two dependent current sources are included to incorporate mutual coupling in Figure 6.1(b). The two transformers generate these two

dependent current sources. According to Kirchhoff's current law, the circuit in Figure 6.1(b) can be represented as

$$C\frac{dV_r}{dt} + GV_r + I_L - I_{k1} - I_{k2} = 0 \tag{6.1}$$

where V_r is the voltage at the node of the resonant circuit, G is the conductance of the resonant circuit, C is the capacitance of the resonant circuit, I_L is the current in the inductor L, I_{k1} is the current induced by the transformers with coupling coefficients k1 and I_{k2} is the current induced by the transformers with coupling coefficients k2. Using the central difference formula, Eq. (6.1) can be written as

$$V_r^n = CG^{-1}CTV_r^{n-1} - CG^{-1}(I_L^{n-1/2} - I_{k1}^{n-1/2} - I_{k2}^{n-1/2}) \tag{6.2}$$

where CG=(C/Δt + G) and CT=C/Δt. The current in the resonator inductor can be written as

$$I_L^{n+1/2} = I_L^{n-1/2} + (LT)^{-1}V_r^n \tag{6.3}$$

where LT is Δt/L.

Finally the voltage at the Ports 1 and 2 is calculated as

$$V_1^n = K_1 V_r^n \tag{6.4.a}$$

$$V_2^n = K_2 V_r^n \tag{6.4.b}$$

This simple voltage and current updating algorithm can be directly expanded to an N-port coupled system with M resonators, as shown in Figure 6.2. The generalized voltage and current updating algorithms can be written as

$$V_{r,i}^n = CG^{-1}(CTV_{r,i}^{n-1} - (I_{L,i}^{n-1/2} - \sum_{j=1}^{N} I_{k,j}^{n-1/2})) = 0 \tag{6.5.a}$$

where $V_{r,i}^n$ is the node voltage at i-th resonator and n-th time step, $I_{L,i}^{n-1/2}$ is the

branch current at i-th resonator and (n-1/2)-th time step, $\sum_{j=1}^{N} I_{k,j}^{n-1/2}$ is the summation of the dependent current sources caused by the N-port at I-th resonator, and

$$I_{k,j}^{n-1/2} = K_{j,i} I_i \text{ and}$$

$$I_{L,i}^{n+1/2} = I_{L,i}^{n-1/2} + LT_i^{-1} V_{r,i}^n \tag{6.5.b}$$

where $I_{L,i}^{n+1/2}$ is the branch current of the inductor at I-th resonator and $LT_i=\Delta t/L_i$. Finally the voltage for the N-port system is written as

$$V_j^n = \sum_{i=1}^{M} K_{ji} V_{r,i}^n \tag{6.6}$$

where V_k^n is the voltage at k-th port, K_{ki} is the coupling coefficient between k-th port and i-th resonator, and $V_{r,i}^n$ is the node voltage at i-th resonator.

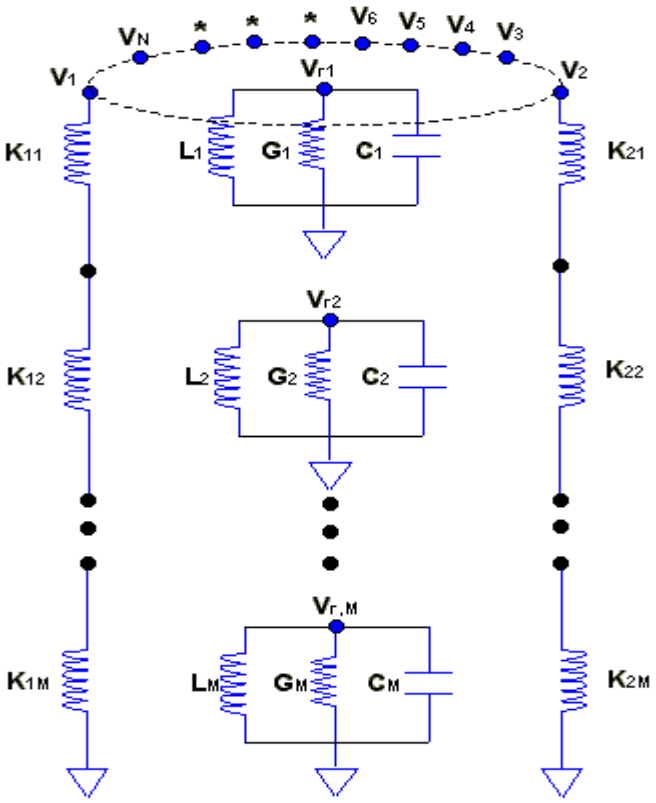


Figure 6.2. N-port coupled system with M resonators

VI.2 Verification of Resonator Model

A test circuit was constructed for the verification of the approach described in the previous section. The test circuit is shown in Figure 6.3 that consists of a current source, a shorted wire, 2 resonators and 4 transformers. The current source has a sawtooth waveform with rise time 10ns and fall time 20ns. The specification for the circuit is as follows:

K1, K2, K3 and K4=0.1, L1=10nH, C1=1nF, G1=1 S, L2=1nH, C2=10nF, G2=1 S, L=1nH and R=0.1 Ohm.

The current source was used to excite the resonant circuit and the transient response was observed from 0 to 205 ns, as shown in Figure 6.4. Figure 6.4(a) shows the voltage at Port 2, Figure 6.4(b) shows the voltages at the nodes of the resonators, 'r1' and 'r2', and Figure 6.4(c) shows the branch current in the wire. FDTD results at all ports were overlapped with the results from SPICE, showing good correlation.

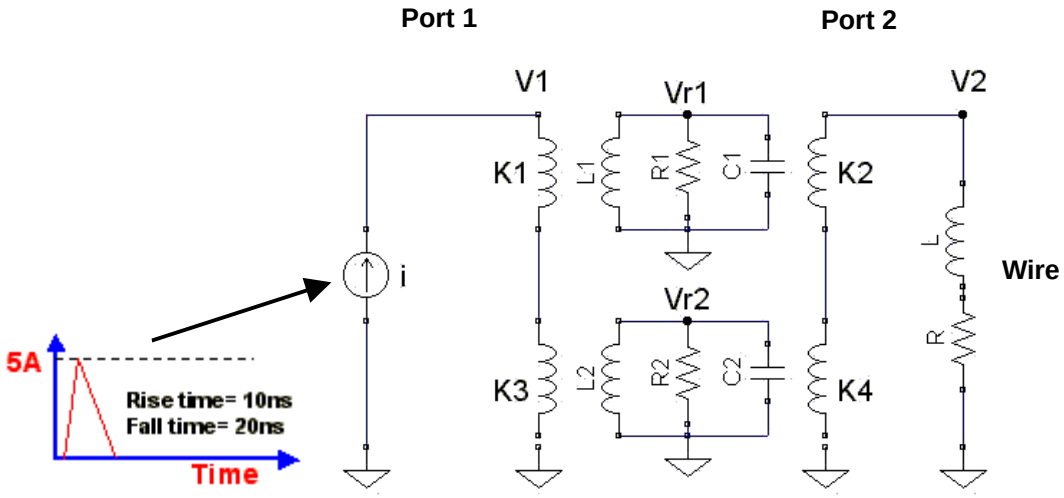


Figure 6.3 A test resonator circuit

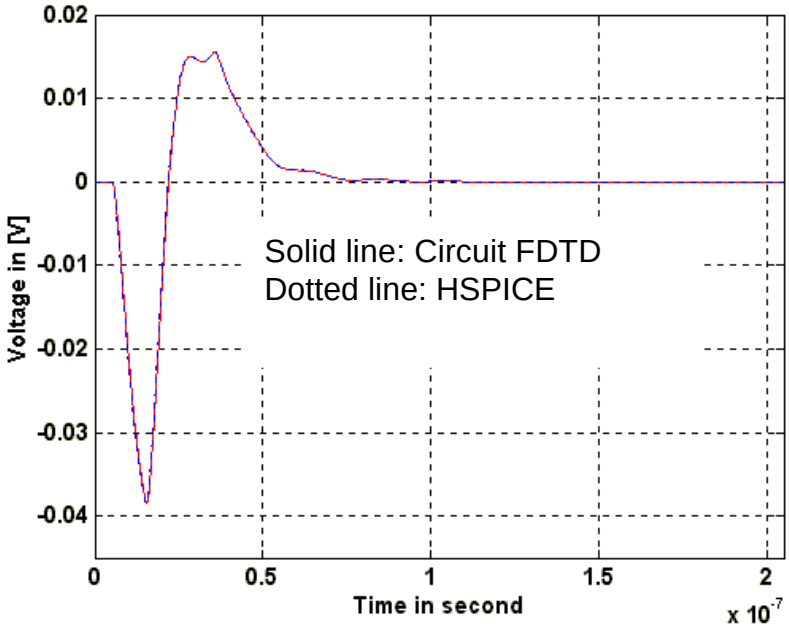


Figure 6.4(a)

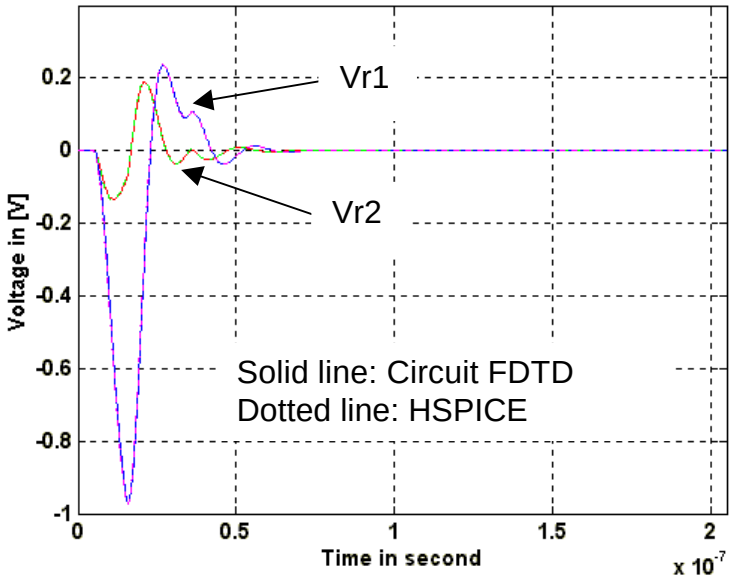


Figure 6.4(b)

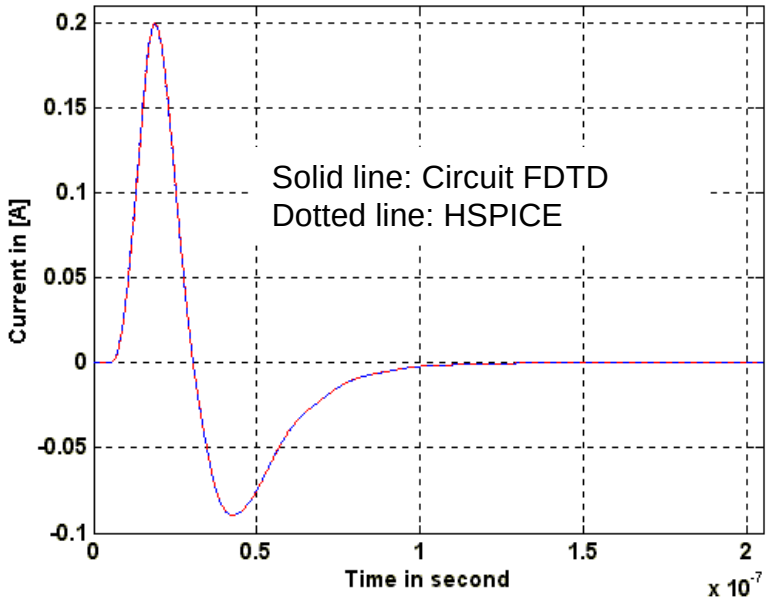


Figure 6.4(c)

Figure 6.4(a) Voltage at Port 2
(b) Voltages at the nodes of the resonators, 'Vr1' and 'Vr2'
(c) Branch current in the wire

VI.3 Simulation of Plane structure

This section discusses the simulation of two structures, namely, a shorted plane pair and an open plane pair. The plane pair is assumed to have a size of 10 by 10 cm^2, dielectric thickness 100 $x10^{-4}$cm, dielectric constant 4, and metal conductance of $5.8x10^5$ S/cm, as shown in Figure 6.5. Three ports were defined for the simulation of the short structure, as shown in Figure 6.5, where Port 1 at coordinate (0,0) is a shorted wire representing the voltage regulator module, Port 2 at coordinate (4,4) is a current source, and Port 3 is a observing port at coordinate (9,9).

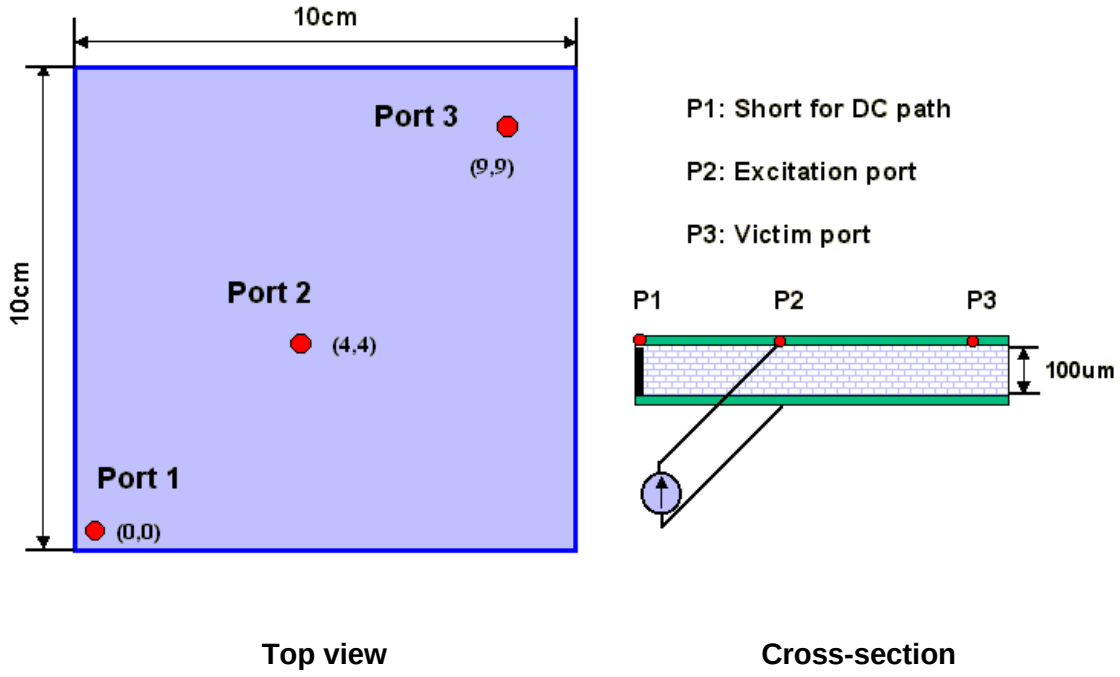


Figure 6.5 Shorted plane structure

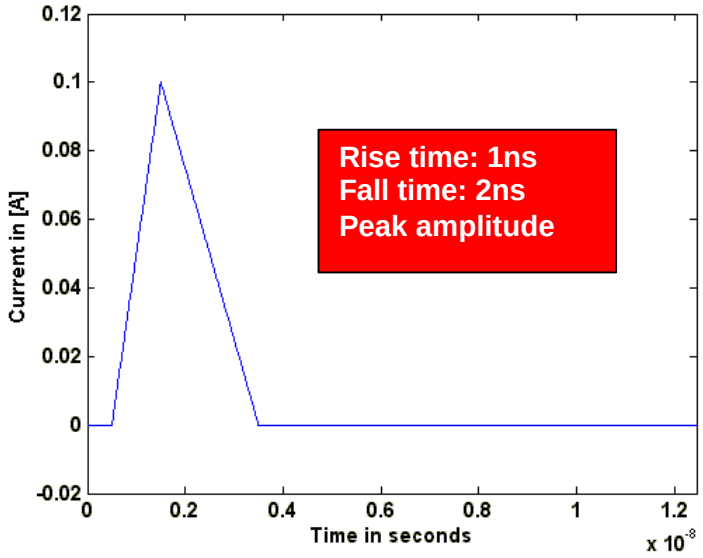


Figure 6.6(a) Wave form of the current source at Port 2

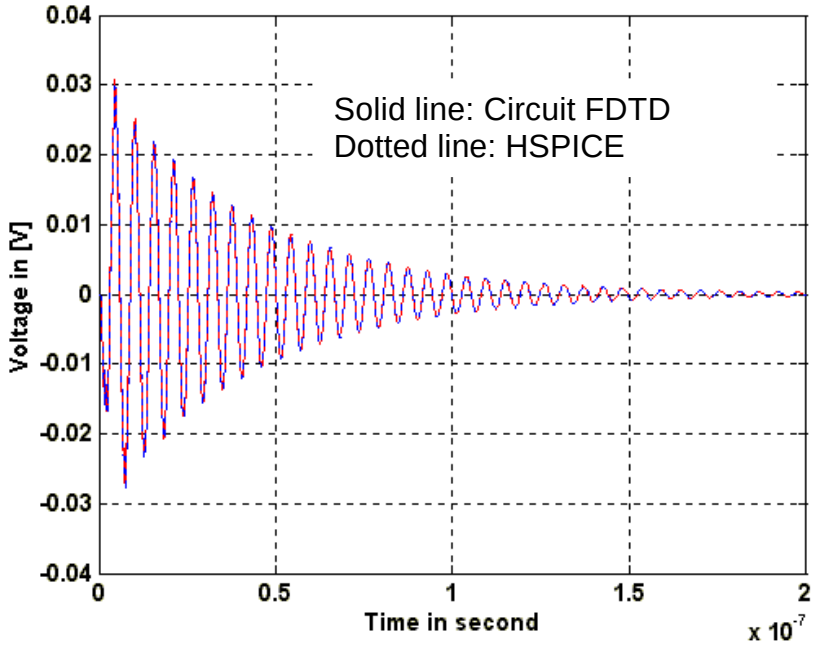


Figure 6.6(b) Noise caused by the current source at Port 2

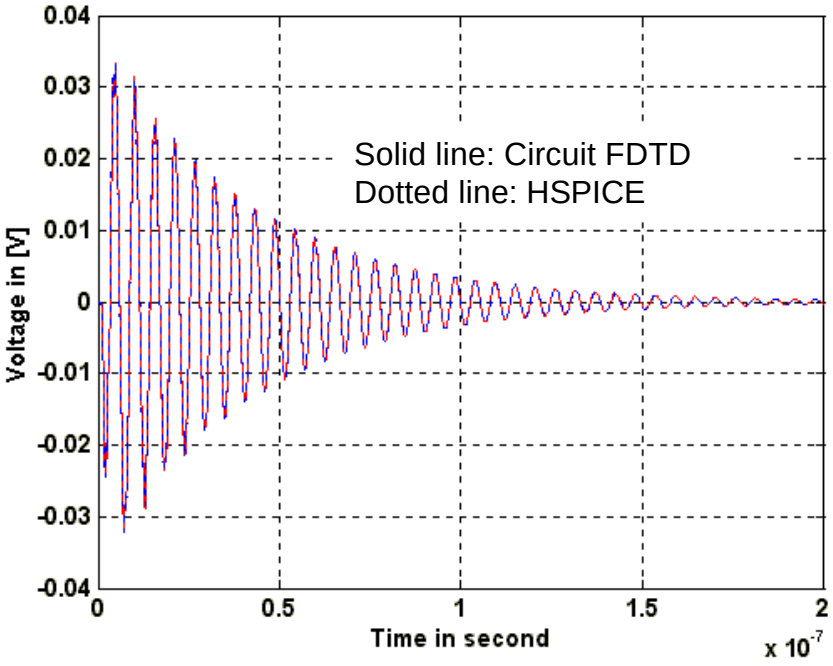


Figure 6.6(c) Coupled noise at Port 3 due to the current source at Port 2

The current source used for the simulation has a rise time of 1ns, fall time of 2ns, and peak magnitude of 0.1A, as shown in Figure 6.6(a). In addition, the plane resonator circuit was assumed to have 8 by 8 modes and the circuit parameters were extracted according to [45,46]. The transient response for the noise at Port 2 and Port 3 was observed for the time period from 0 to 200ns, as shown in Figures 6.6(b) and (c). Figure 6.6(b) shows the noise caused by the current source at Port 2 and Figure 6.6(c) shows the coupled noise at Port 3 due to the current source at Port 2. From both of the figures, it can be seen that the high frequency loss effect (skin effect) is included in the transient response, which cannot be handled using a conventional FDTD method [60].

For the response in the frequency domain, a Gaussian pulse and Fourier transform technique were used. The Gaussian pulse with time bandwidth of 2ns, and peak amplitude of 0.1A, was placed at Port 2, as shown in Figure 6.7(a).

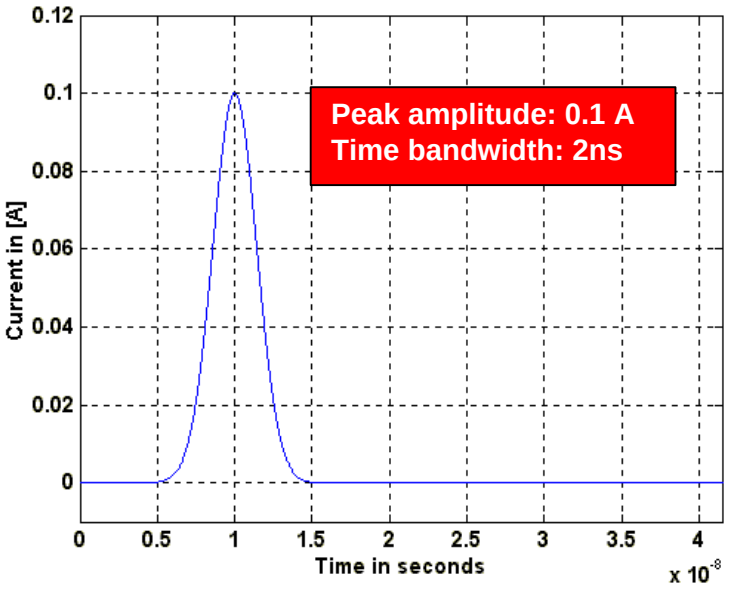


Figure 6.7(a) Gaussian pulse used for the frequency response

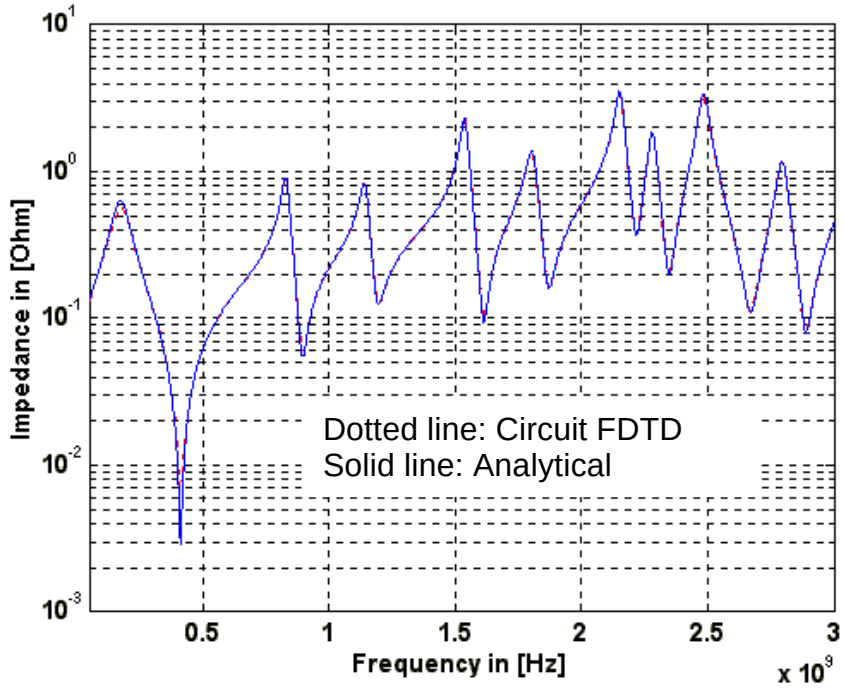


Figure 6.7(b) Self-impedance at Port 2 from the shorted structure

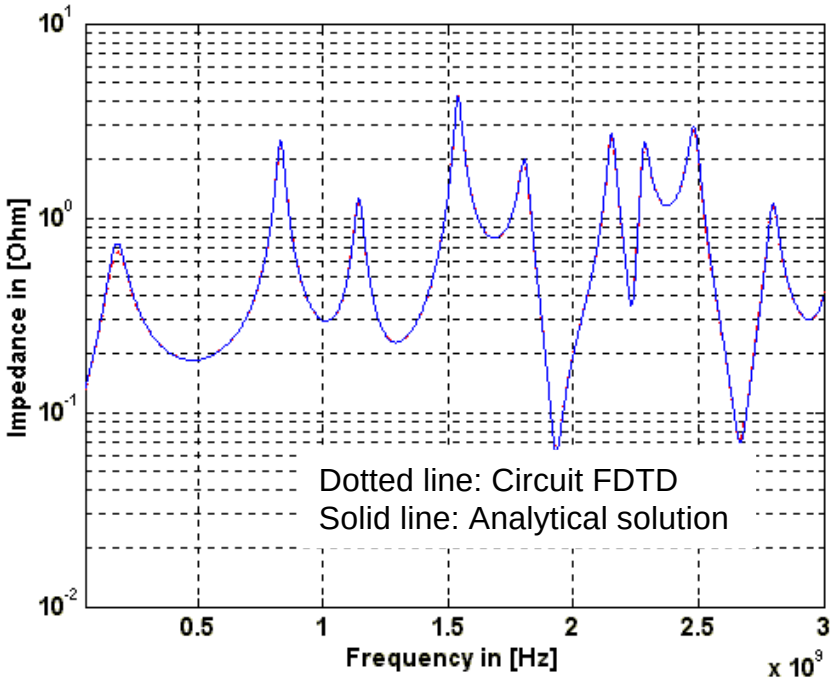


Figure 6.7 (c) Trans-impedance at Port 3 from the short structure

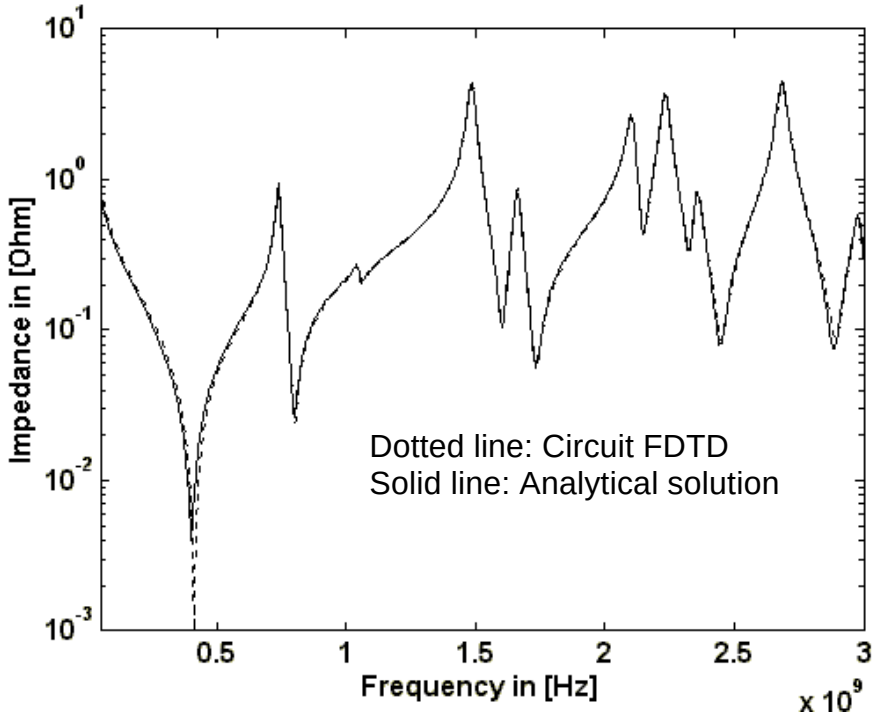


Figure 6.8 (a) Self-impedance at Port 2 from the open structure

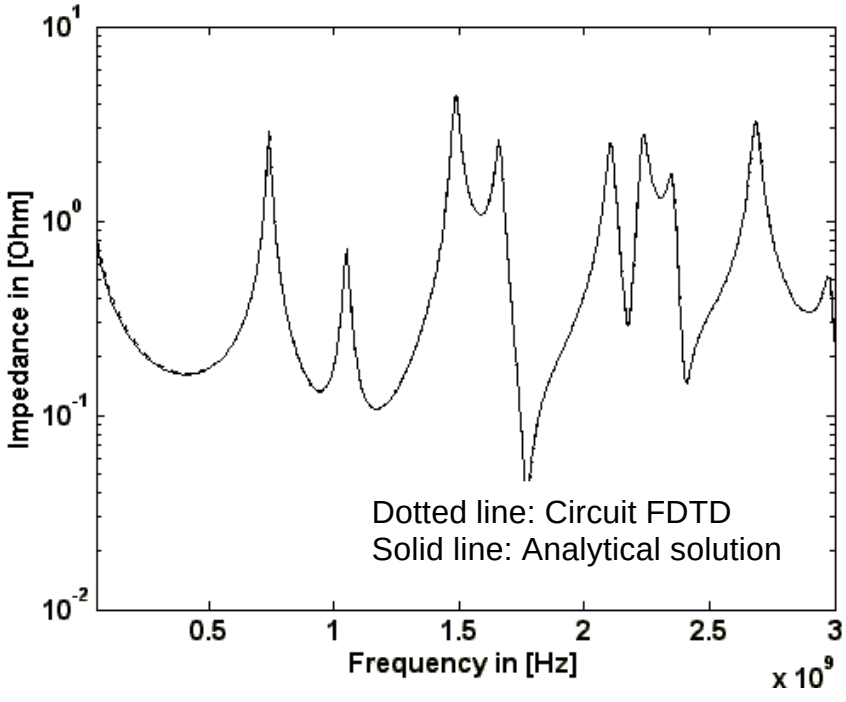


Figure 6.8 (b) Trans-impedance at Port 3 from the open structure

The transient noises at Port 2 and Port 3 were computed and, using Fourier-transformation, the frequency response was also calculated as a ratio of the noise voltage to the gaussian pulse amplitude in the frequency domain. The frequency domain self-impedance is shown in Figure 6.7(b) and is shown the transfer-impedance in Figure 6.7(c). These transformed results were overlapped with the result from the analytical solution in [44], showing good correlation. From Figure 6.7(b), the first resonant peak is due to the interaction between the shorted wire and plane. The interaction can be explained by the fact that the wire is in parallel to the plane pair. Therefore it can be seen that the first resonant peak moves to a lower frequency as the inductance of the structure increases. The rest of the resonant peaks come from the plane pair.

For the frequency response of the open structure, the shorted wire at Port 1 in Figure 6.6 was removed and a Gaussian pulse with time bandwidth of 2ns and peak amplitude of 1V was used at Port 2. The transient noise currents were computed at Port 2 and 3 followed by its Fourier transform. Figures 6.8(a) and (b) show the self-impedance at Port 2 and the trans-impedance at Port 3, which were overlapped with the results from the analytical solution, showing good correlation. The results in Figure 6.8 are due to the resonances in the plane structure [44]. As mentioned earlier, one advantage for implementing the cavity resonator model using the FDTD method is that it captures the high frequency loss effect. The other advantage is that it can be directly applied to plane structures containing many vias and decoupling capacitors.

When the frequency response is computed using Fourier transform, the time duration for simulation in the time domain needs to be specified to ensure accurate results in the frequency domain. The root mean square error between the frequency response using Fourier transform and plane impedance calculated by the analytical solution [44] is plotted as a function of the time duration in Figure 6.9(a). When the effective time duration is defined below 5 % of RMS error, it translates to a time duration of 120ns. The frequency response with 120ns of time duration was compared with the analytical solution, as shown in Figure 6.9(b). It is well known that the time response should reach a steady state before conversion to the frequency domain for obtaining an accurate frequency response using a Fourier transform. However, it is not well known in the literature as to how long the time response needs to last. The time duration required for a proper conversion to frequency domain is not unique and depends on the loss of a circuit network. Figure 6.9(c) shows the voltage response with the Gaussian pulse excitation on planes. From Figure 6.9(c), the maximum voltage is 0.217V and the voltage at t=120ns is 0.86nV. If the condition of the time duration for obtaining an accurate frequency response is defined as a ratio of the voltage at t=120ns to the maximum voltage, the ratio is ~4 $\mathrm{x10^{-9}}$. The value 4 $\mathrm{x10^{-9}}$ can be used as a measure to determine the time duration such that it guarantees a suitable conversion to the frequency domain with an RMS error of 5%. This criterion has been used in this dissertation.

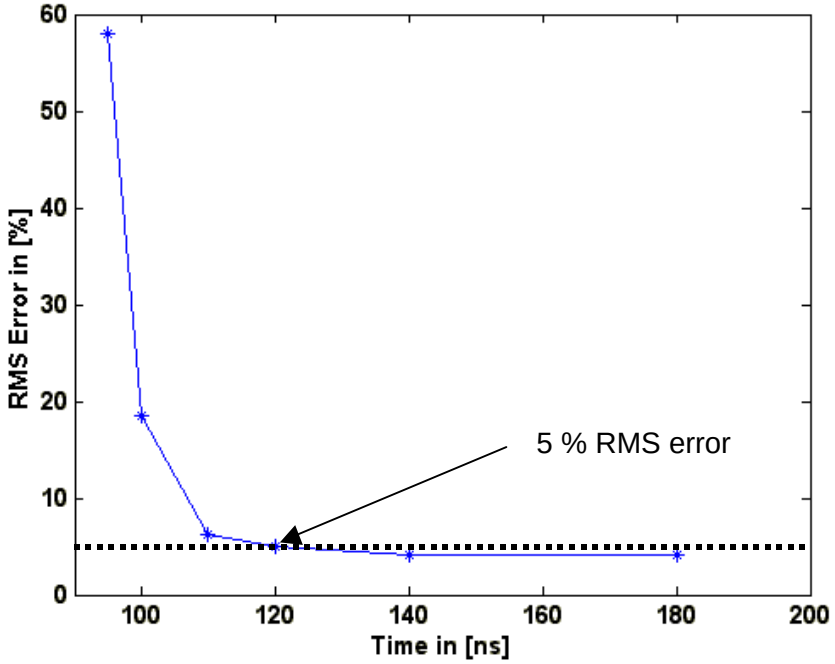


Figure 6.9(a) RMS error with the variation of the time duration

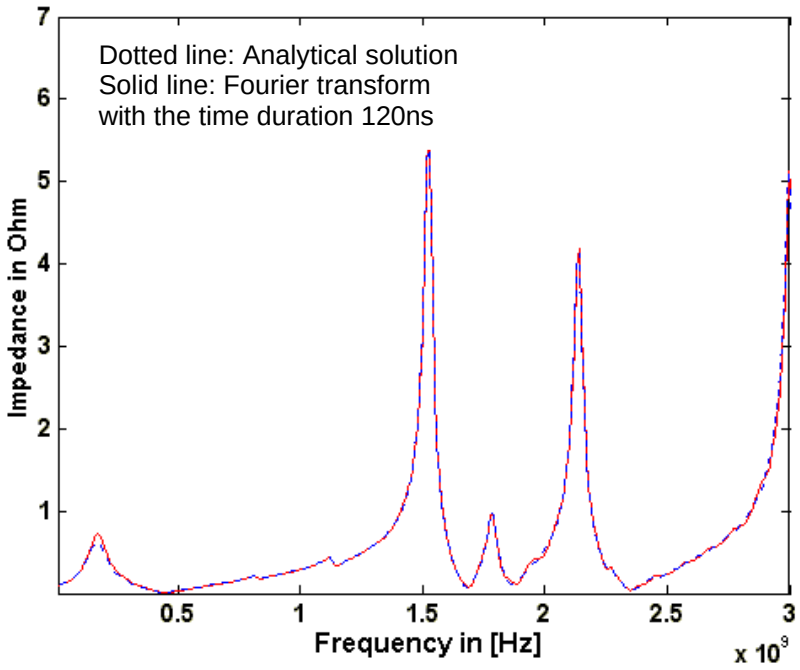


Figure 6.9(b) Comparison of the frequency response

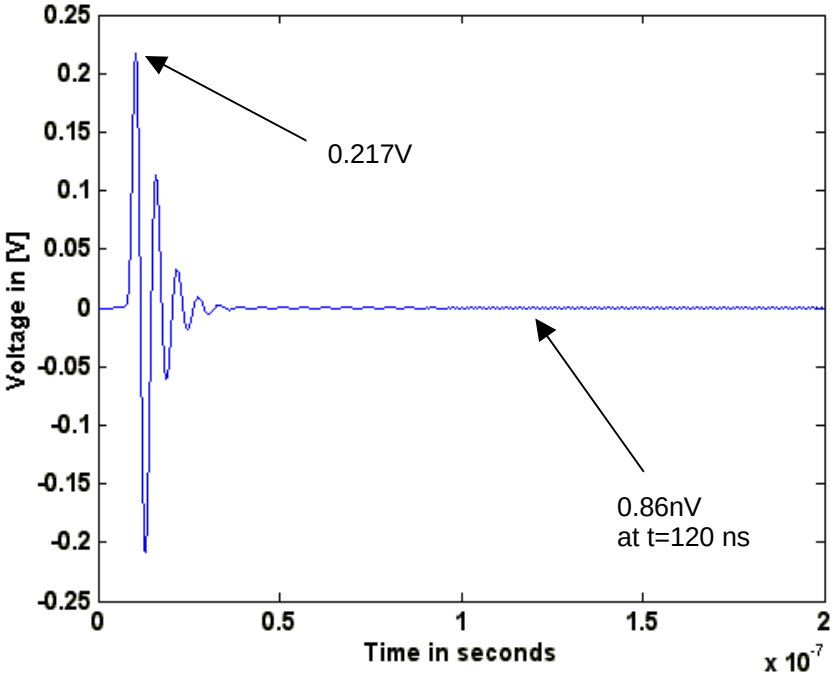


Figure 6.9(c) Time response of the voltage

VI.4 Radial wave propagation inside a plane pair

In order to visualize the radial wave propagation inside the plane pair, 1684 ports consisting of 1681 observation ports, 2 ports for the DC path and 1 port for the placement of a current source were defined on the plane pair shown in Figure 6.10. The plane pair is of size 10cm by 10cm with dielectric thickness 100um, relative dielectric constant 4, and metal conductance 5.8×10^5 S/cm. Positions, Port 1(0.5,4.5) and Port 2(0.5,5.5) were for DC path and Port 3 (5,5) was used for the location of the current source. The rest of the ports were assigned as the observation ports, which were uniformly distributed. A Gaussian pulse with time bandwidth, 0.2ns and peak amplitude of 1A was used as a current source for the simulation. The transient response was observed from 0 to 2 ns.

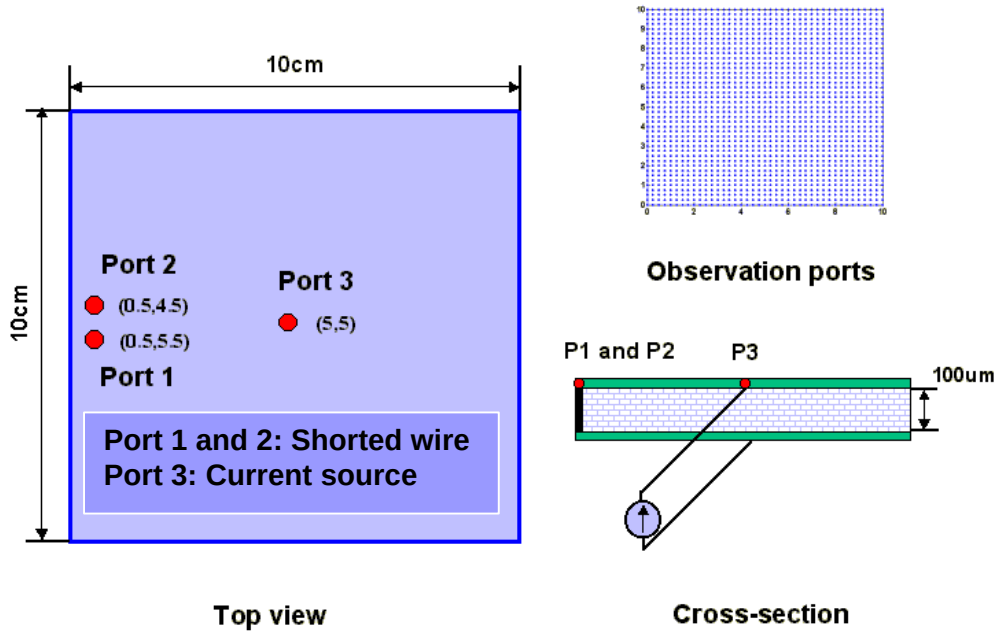


Figure 6.10 Plane pair for the radial wave propagation

The CPU time was 71 seconds for the simulation. Figure 6.11 (a)-(f) show the snapshots for the noise distribution on the plane pair at different times. Figures 6.11(a) and (b) show the radial wave propagation along the plane, reaching the plane boundary in Figure 6.11(c) and reflecting at the plane boundary in Figure 6.11(d). The reflecting waves move in the x and y direction, creating hot spots at the edges except at the location of the DC paths in Figure 6.11(e). The 4 corners are hotter due to the reflection in the x and y direction at the corners. From Figure 6.11(f), the energy stays in the cavity even at t=2ns even though the source is turned off at t=750 ps. This is the characteristic of a high Q cavity that can create problems. The simulation for the radial wave propagation shows the usefulness of the circuit FDTD method for simulating the plane structure with a large number

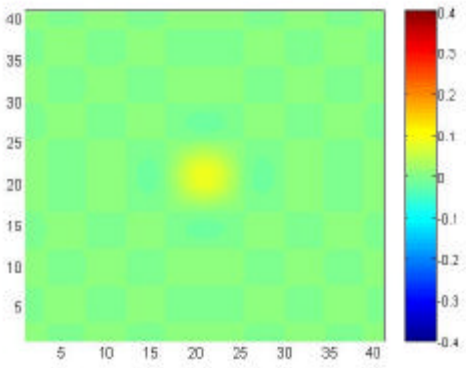


Figure 6.11 (a) At t=10ps

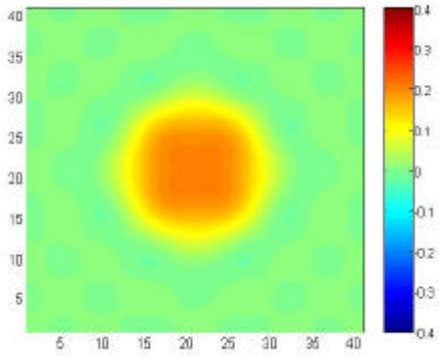


Figure 6.11 (b) At t=140ps

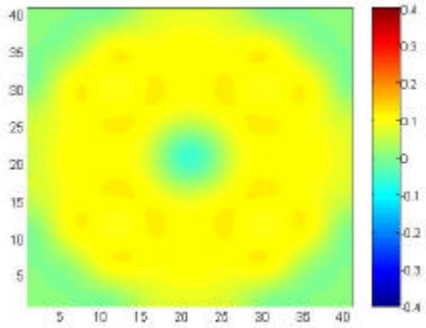


Figure 6.11 (c) At t=320ps

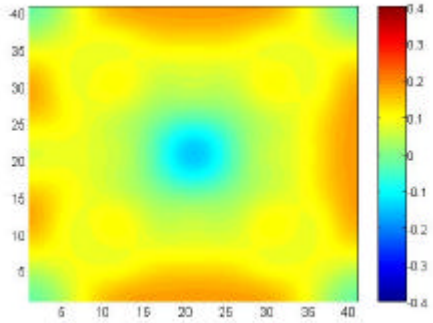


Figure 6.11 (d) At t=400ps

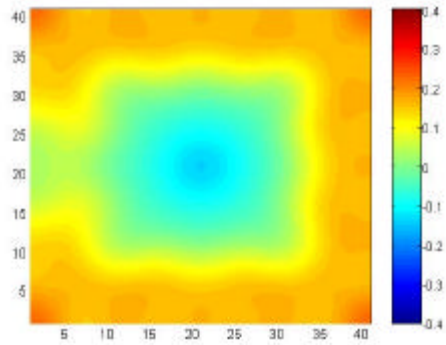


Figure 6.11 (e) At t=480ps

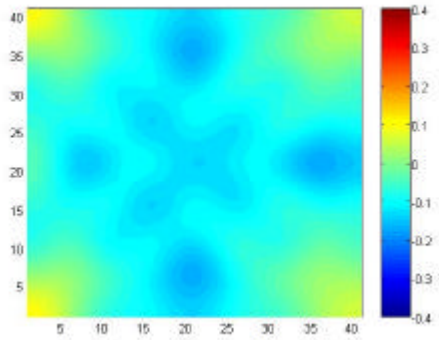


Figure 6.11 (f) At t=2ns

Figure 6.11 Snapshots for the noise voltage distribution on the plane pair at different times

of ports including many vias, decoupling capacitors and other circuit components. Table VI.1 shows the comparison of the CPU time of the circuit FDTD method with HSPICE for obtaining the time domain response using the resonator cavity model. In the comparison, the number of time steps was 1000 and the mode number was 10 by 10. It can be seen from the table that the speed-up of the circuit FDTD method over HSPICE is 100 – 100,000, showing a possibility of the circuit FDTD method being a good candidate for the simulation of a large electronic packaged system. Also, it should be noted that, if the structure with 1684 ports is simulated in SPICE, it may take ~15.3 days, based on the result from Table VI.1.

Table VI.1 Comparison of the CPU time of the circuit FDTD method with HSPICE

Port number	10	50	100	200	400	1000
HSPICE	15.2 s	300 s	1694 s	9114 s	4.54×10^4 s	2.86×10^6 s
Circuit FDTD	0.16 s	0.76 s	1.54 s	3.24 s	6.54 s	21.42 s

VI.5 Effectiveness of via location in a multi layer structure

In order to study the effectiveness of via location in a multi-layered plane structure, a Power-Ground-Power (PGP) plane structure was constructed. The connection via between the upper plane and the lower plane was located at the center of the plane structure, as shown in Figure 6.12. The physical dimension of the planes were the same as the details discussed in the previous section.

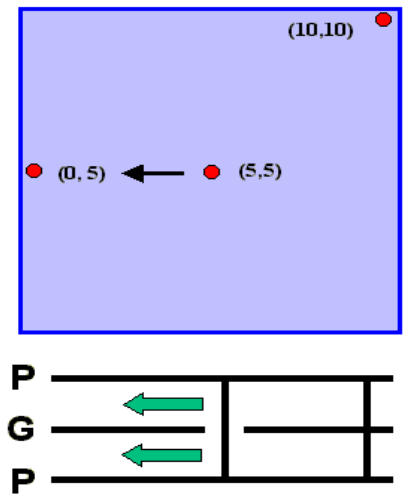


Figure 6.12 A multi-layered plane structure for the effectiveness of via location

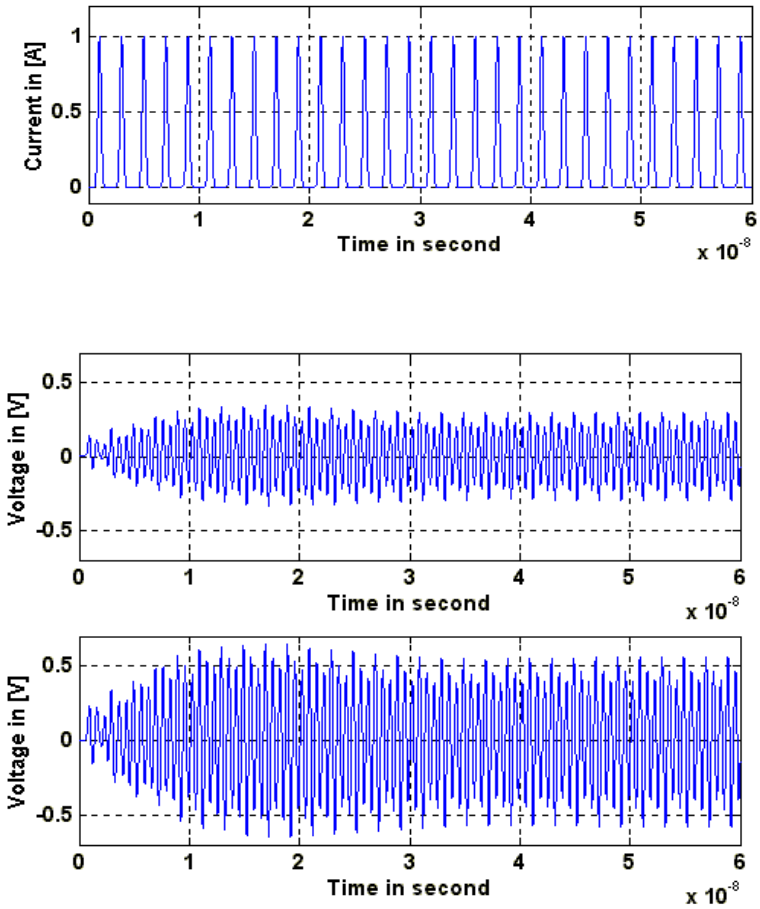


Figure 6.13(a) Current pulse used for the simulation
(b) Noise response for PGP structure
(c) Noise response for single plane pair

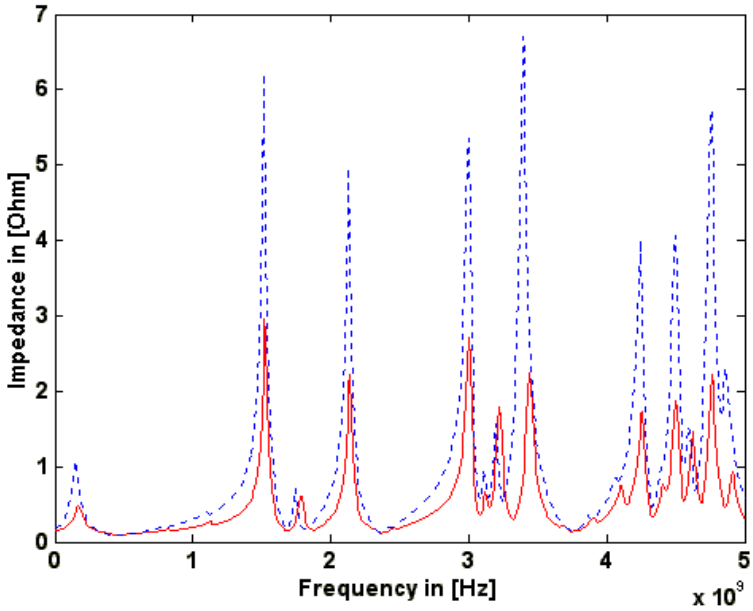


Figure 6.14 Frequency response of the plane structures
Dotted line: single plane pair
Solid line: Two plane pairs

The Gaussian current pulse with time bandwidth 0.2ns and period 2ns was used to excite the PGP structure for 30 cycles. Figure 6.13 (a) shows the current pulse used for the simulation, Figure 6.13 (b) shows the noise response for the PGP structure and Figure 6.13(c) shows the noise response for a plane pair, with details described in the previous section. As can be seen, the noise for the PGP structure is half as much as the one for the single plane pair and the connection via is fully effective. Also, in the frequency domain, the self-impedance of the PGP structure (solid line) is half of the self-impedance of the single plane pair (dotted line), as shown in Figure 6.14. The reason for the impedance difference in Figure 6.14 is that, when the PGP structure is compared to a single plane pair,

it has twice the capacitance and half the inductance, thereby resulting in 0.5 half of the plane impedance.

In order to define a distance for the effectiveness of a connecting via in the multi-layered structure, peak noises were calculated at the center of the PGP structure as the connection via location is moved from the center to the left side. The normalized effectiveness of the multi-layered structure with the variation of the connecting via location can be represented as

$$Effectiveness = \frac{V_{PG}(x_o, y_o) - V_{PGP}(x, y_o)}{V_{PG}(x_o, y_o) - V_{PGP}(x_o, y_o)} \tag{6.7}$$

where $V_{PG}(x_o, y_o)$ is the peak noise for a single plane pair at the location, $x=x_o$, and $y=y_o$, $V_{PGP}(x_o, y_o)$ is the peak noise for a multi-layered plane at the location, $x=x_o$, and $y=y_o$, and $V_{PGP}(x, y_o)$ is the peak noise for a multi-layered plane at the location, x=x, and $y=y_o$.

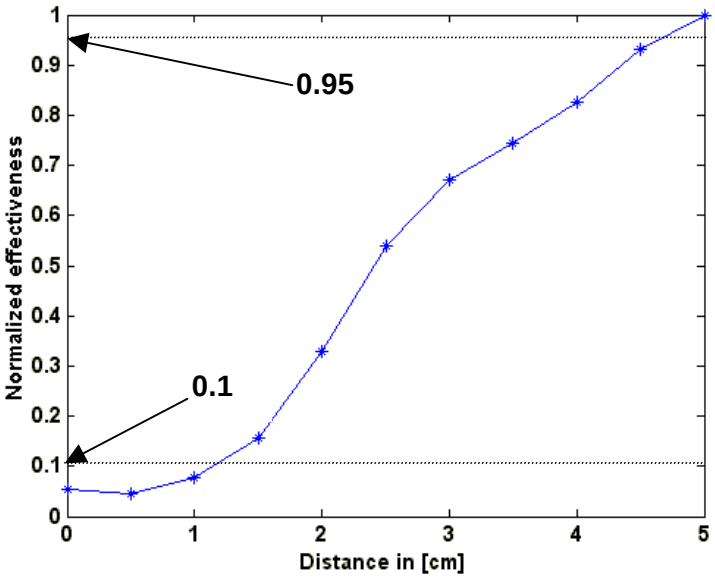


Figure 6.15 Normalized effectiveness

Using Eq (6.7), the normalized effectiveness is plotted in Figure 6.15 where the position of the connecting via was moved from the coordinate (5,5) to the coordinate (0,5), as shown in Figure 6.12. As can be seen, the effectiveness is less than 0.1 after a distance of 4cm from the center, which means that the multiplayer plane behaves as a single plane pair. When the effectiveness needs to be maintained within 5 % of the normalized effectiveness, the connection via should be located within the radius of 5mm with reference to the port at which a current surge occurs.

VI.5 Summary

As mentioned earlier, an integral part of the power distribution network in gigahertz systems are planes in the package and board. In this chapter, the resonator cavity model was implemented using the circuit FDTD method. It was verified in the frequency domain by comparing with the analytical solution, which showed good correlation. The result was also verified in the time domain with HSPICE. In addition, the radial wave propagation was visualized by defining 1684 ports on the plane pair. The results show the validity of the circuit FDTD method for analyzing realistic package and board power distribution networks. Also, the effectiveness of the connection via location in multi-layered structures was analyzed using a simple test case.

Chapter VII

Co-simulation of Chip and Package

Wafer level packages (WLP's) are defined as packages that are less than 1.2 times the size of the chip. WLP's offer a smaller footprint, lower parasitics and more inputs/outputs per unit area than a ball grid array, resulting in better electrical performance [58]. In this chapter the FDTD method has been applied to capture the interaction between the chip and package by analyzing the chip and package power distribution as a single network. In particular, the FDTD method has been applied to a wafer level chip scale package assembled on an integrated, high-density printed circuit board being developed at the Packaging Research Center, Georgia Tech. The results have been analyzed to understand the various interactions in the system hierarchy.

An important effect that is often neglected in the computation of power supply noise is the interaction between the chip-package and package-board. This interaction can cause additional resonances in the system [59]. If these resonances have sufficient magnitude and are triggered during system operation, excessive noise can be generated in the system. The purpose of the co-simulation is to capture resonances that are otherwise absent when each section of the system is analyzed separately.

VII.1 Simulation of the Wafer Level Package

To better understand the interactions between the chip and package, a standalone chip has been simulated in this section. The chip is in wafer level form which can be directly attached to the board. This is shown pictorially in Figure 7.1.

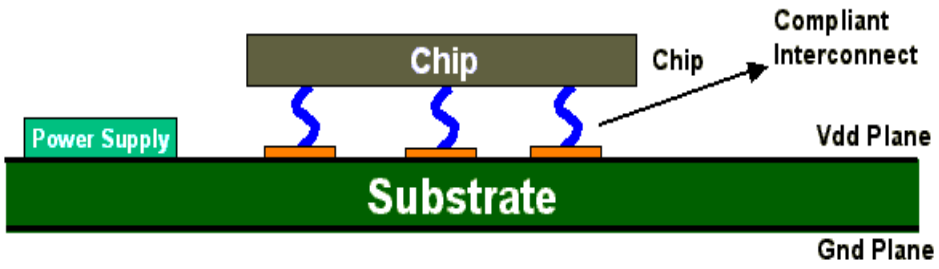


Figure 7.1 Wafer level package

In this section the power supply was assumed to be directly beneath the compliant interconnect with the board absent.

Based on ITRS, in the year 2005 the required power for a CPU is 160W, the DC voltage is 1.1V, the operating clock frequency is 5 GHz and the tolerance on the power supply is expected to be 55mV. The goal of the simulation in this section is to calculate a suitable inductance for the compliant interconnect that met the noise tolerance. For the simulation, it was assumed that the number of layers in silicon was 4, the size of the chip is 20.1mm by 27mm, the number of the compliant interconnects is 2464, number of CMOS inverters is 77616, the simultaneous switching power is 40% of the total power, and the on-chip decoupling capacitance was 400nF. In addition, the clock frequency is 5GHz, the

rise and fall times of the input signal are both 20 ps, and the period is 200ps. The line parameters for the on-chip power grid are summarized in Table VII.1.

Tabel VII.1 Line parameters of the on-chip power grid used for the simulation

	Resistance	Inductance	Capacitance
1st metal layer	0.345 Ohm	47.2 pH	3.36 fF
2nd metal layer	0.345 Ohm	47.2 pH	3.36 fF
3rd metal layer	0.172 Ohm	41.2 pH	4.8 fF
4th metal layer	0.345 mOhm	21.2 pH	45 fF

The compliant interconnect inductance was varied from 20pH to 2nH to find a suitable inductance that met the noise tolerance. The CPU time required for the simulation was ~3100s for one cycle.

Figure 7.2 shows the transient response for 20 pH of inductance for the compliant interconnect. Figures 7.2(a)-(d) show the input and output voltage, current signature at a CMOS inverter, current signature at the compliant interconnect and differential noise at a CMOS inverter. From Figure 7.2(c), it can be seen that the current transient at the interconnect shows the superposition of the current signatures with finite delay from the CMOS inverters at various locations. Figure 7.3 shows the differential noise from the power grid structure with the variation of interconnect inductance from 20pH to 2nH, as observed at a CMOS inverter for ten cycles. As can be seen, the differential noise increased due to the interaction between the inductance of the interconnect interaction

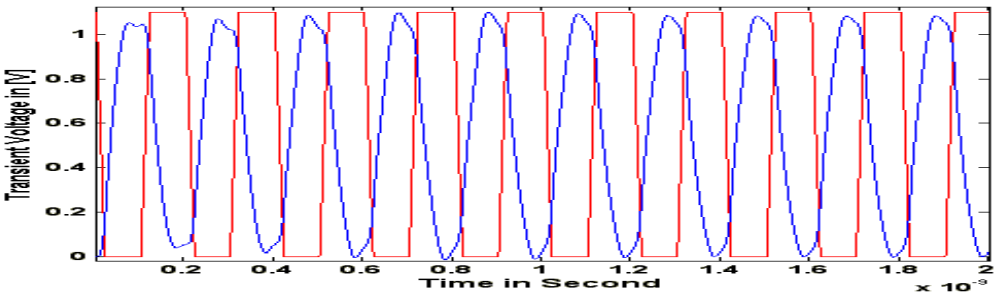


Figure 7.2(a) Input and output voltage of the driver

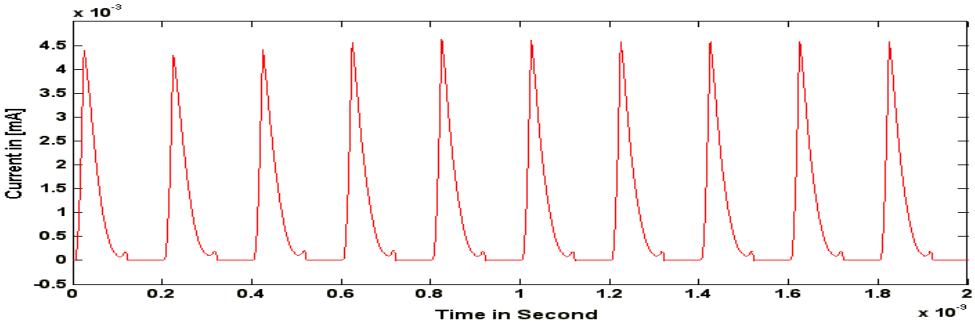


Figure 7.2(b) Current signature at a CMOS Inverter

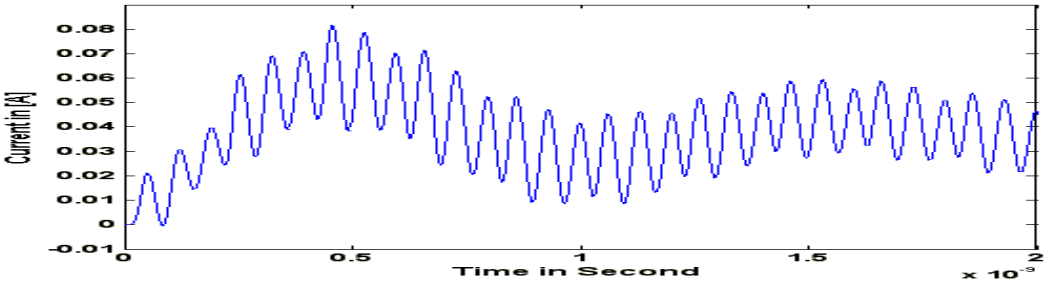


Figure 7.2(c) Current signature at C4 via

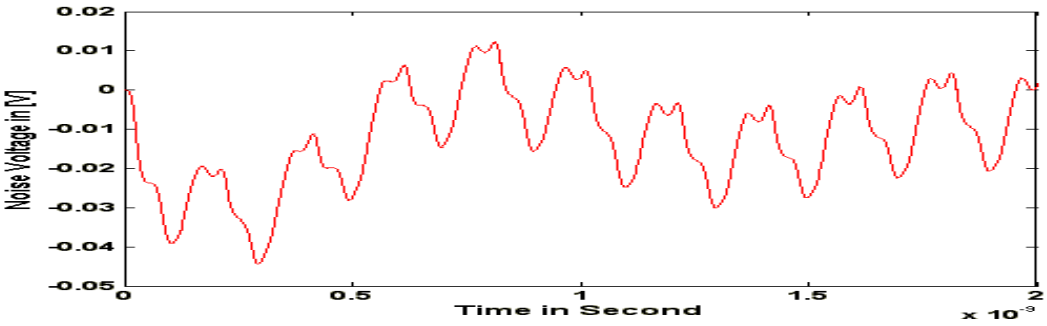


Figure 7.2(d) Differential noise at a CMOS inverter

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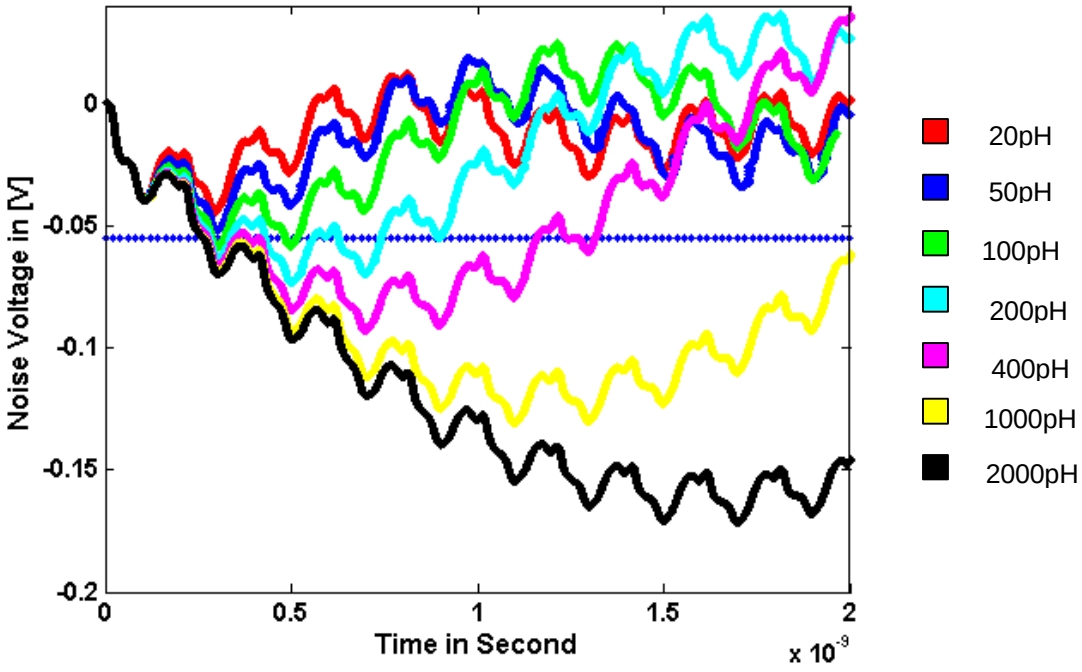

Figure 7.3 Differential noise from the power grid structure with the variation of compliant interconnect inductance from 20pH to 2nH

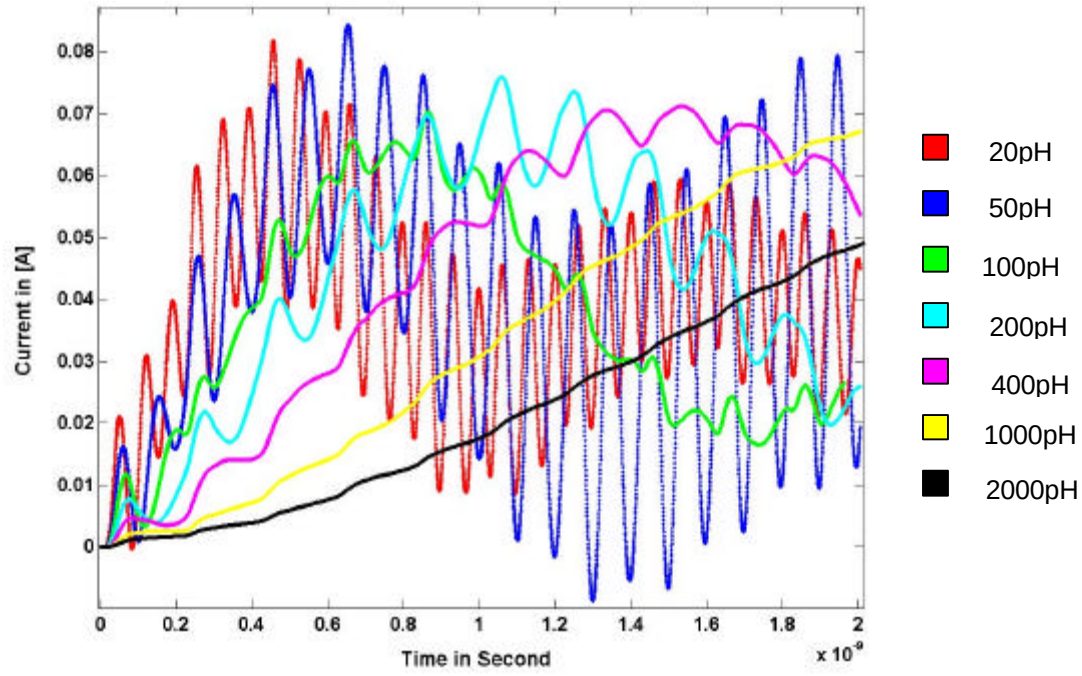

Figure 7.4 Current transient from the power grid structure with the variation of compliant interconnect inductance from 20pH to 2nH

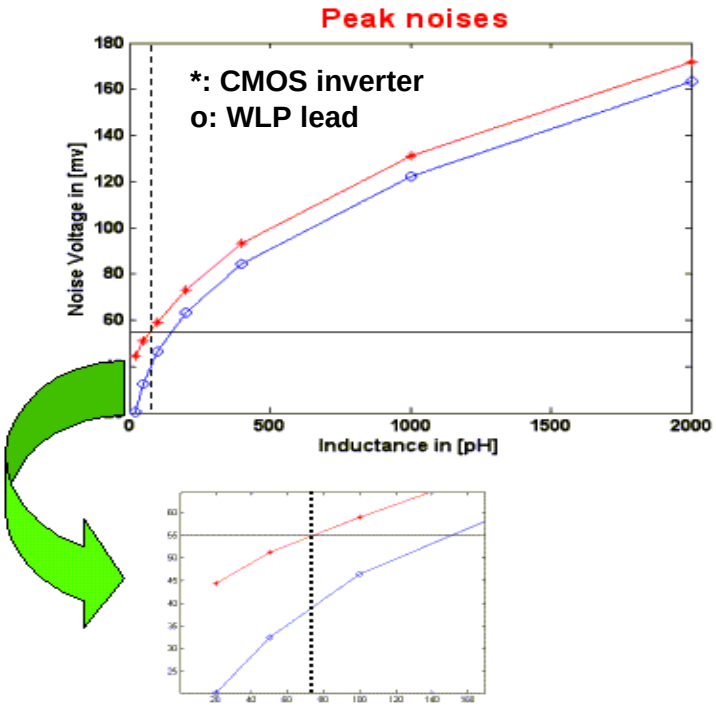

Figure 7.5 Peak noise at the location of CMOS inverters and compliant interconnect

includes the low frequency component in the noise response for 2nH of compliant interconnect inductance. Figure 7.4 shows the current transient from the power grid structure as the compliant interconnect inductance is varied from 20pH to 2nH, which was observed at the compliant interconnect for ten cycles. The current transient with 20pH of compliant interconnect inductance shows a faster supply of charge while the current transient for 2nH of compliant interconnect inductance shows slower supply of charge, causing power delay and an increased voltage droop on the power-ground rails. The peak noise at the locations of CMOS inverters and compliant interconnect are plotted in Figure 7.5. The star line is at the CMOS inverter and the circled line is at the compliant interconnect. It shows that 75pH of compliant interconnect inductance is required

to meet the noise margin specification. Since the effects of package and board parasitics were not included in the simulation, in reality, 75pH can mean an effective inductance for the compliant interconnect which includes package and board.

VII.2 Simulation of wafer level package on an integrated board

The silicon core circuits on a microprocessor or ASIC chip perform best when they are supplied with a constant power voltage with a small tolerance, usually 5 %. It is relatively easy to find a Voltage Regulator Module (VRM) that meets the 5 % tolerance at DC. By using feed back, the VRM holds the core power supply constant up to the bandwidth of the regulator, usually between 1kHz and 1MHz. At higher frequency, decoupling capacitors, usually located on the Printed Circuit Board (PCB), store charge and provide energy to the PCB as needed to hold the power supply voltage constant. With decoupling capacitors, it is possible to provide a low impedance power distribution system on the PCB that meets target impedance and is effective up to several hundred MHz [39].

As clock frequencies increase, the circuits on the silicon chip need a low power supply impedance and constant voltage up to several GHz. There is some amount of capacitance on chip that provides decoupling at the highest frequencies. But at lower frequency, current must come in through the electronic package, which is inductive in nature. The inductance of the package is in parallel with the capacitance of the chip and forms a parallel RLC resonant circuit, which resonates at some characteristic frequency. The circuit on the chip

sees a high impedance power supply at this frequency, which may cause problems [59]. The goal of this section is to analyze the chip-board resonance.

In order to study the interaction between the board and chip, it was assumed that the number of layers in silicon was 4, the size of the chip was 21mm by 21mm with 2.1 million passive elements, the number of the compliant interconnects was 9408, the inductance of each compliant lead is 50pH, the number of CMOS inverters was 56616, the simultaneous switching power was 40% of the total power, and the on-chip decoupling capacitance was 566nF. In addition, the clock frequency assumed was 5GHz, the DC voltage was 1.1V, the rise and fall times of the input signal were both 20 ps and the period was 200ps. The plane pair for the board was of size 5cm by 5cm with dielectric thickness 10um, relative dielectric constant 4, and metal conductance 5.8×10^5 S/cm. A total of 18uF board capacitance was used in the simulation. The details of the structure are shown in Figure 7.6.

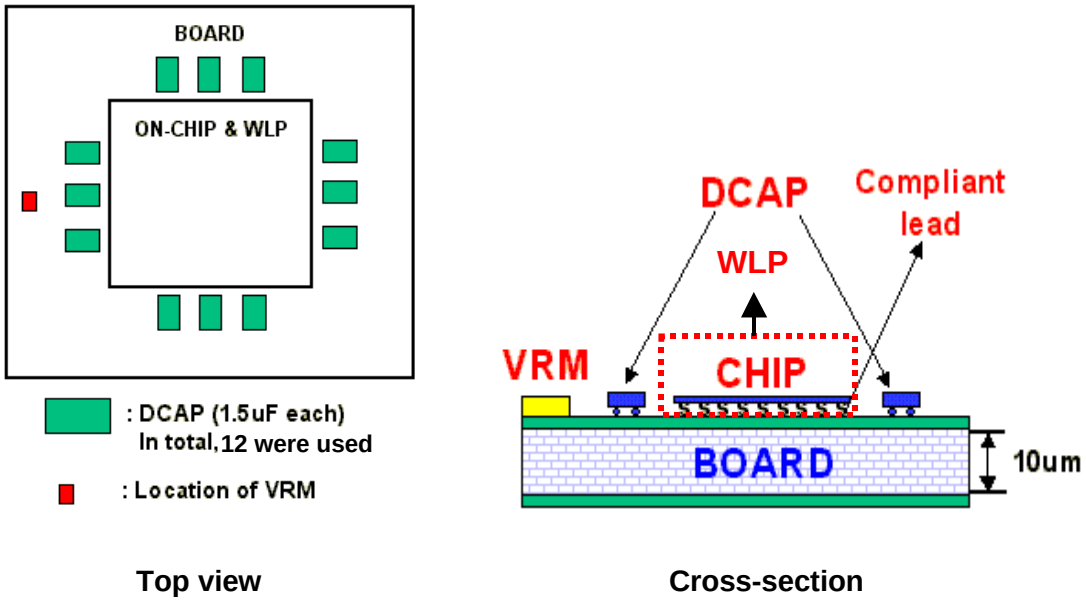

Figure 7.6 Board with 12 decoupling capacitors and a wafer level package

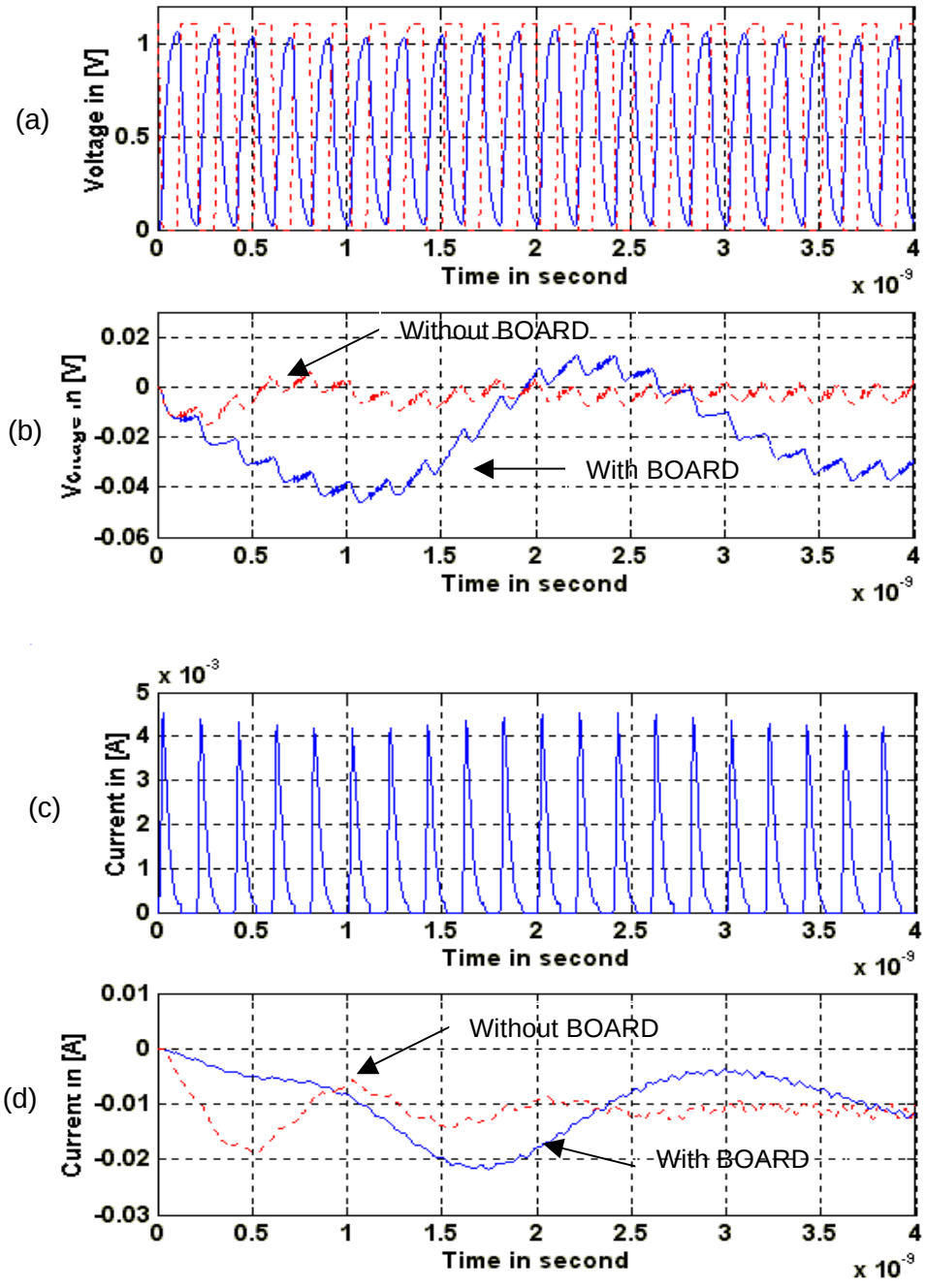

Figure 7.7 (a) Input and output voltage response at CMOS circuit
(b) Differential power supply noise
(c) Current signature of a CMOS circuit
(d) Current signature in WLP lead

Line parameters for the on-chip power grid in Table 6 were used for the simulation. The board shown in Figure 7.6 has 12 decoupling capacitors, chip size of 4.41 cm^2 and an ideal voltage regulator module. Figure 7.7 shows the transient response at a CMOS circuit and WLP lead. Figures 7.7 (a)-(d) show the input and output voltage response, power supply noise, CMOS current and current in WLP lead, respectively. In Figures 7.7(b) and (d), the dotted lines are from the response without the board. Figure 7.7(b) shows that the power supply noise with the board is larger than the noise without the board. This can be caused by the interaction between the on-chip capacitance and the lead inductance or the on-chip inductance and the board decoupling capacitance. The solid line in Figure 7.7(d) shows the delay in the supply of charge, causing more noise in the power–ground rails.

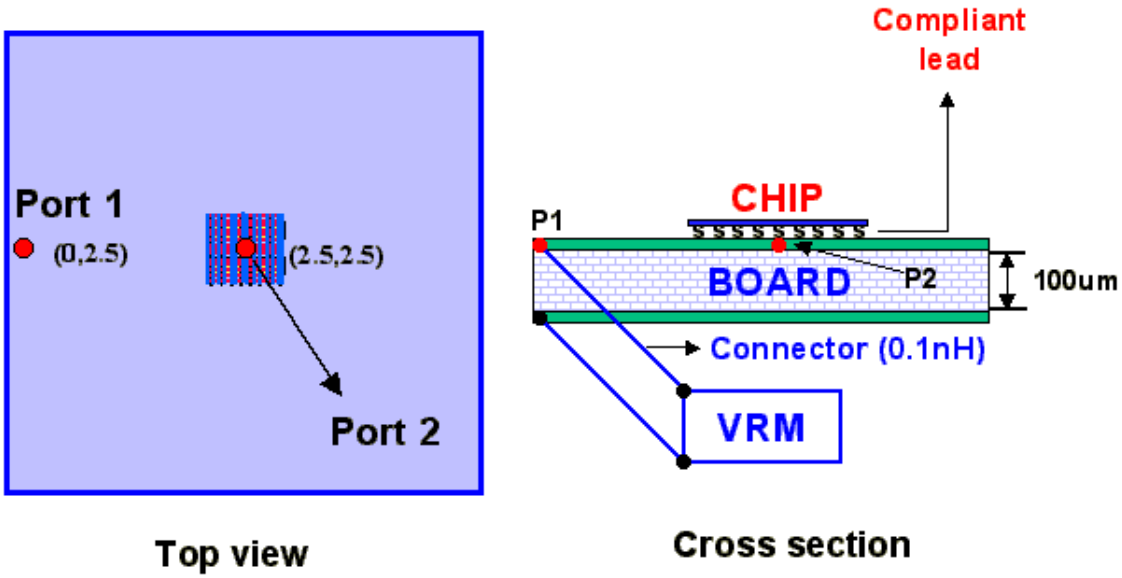

Figure 7.8 Plane pair with an on-chip power grid

In order to capture the chip-board interaction in the frequency domain, the structure in Figure 7.8 was simulated. The plane pair for the board was of size 5cm by 5cm with dielectric thickness 100um, relative dielectric constant 4, and metal conductance $5.8x10^5$ S/cm, as shown in Figure 7.8. It was assumed for the on-chip power grid that the number of layers in silicon was 4 and the size of the chip was 1.5 mm by 1.5 mm with the line parameters in Table Table VII.1.

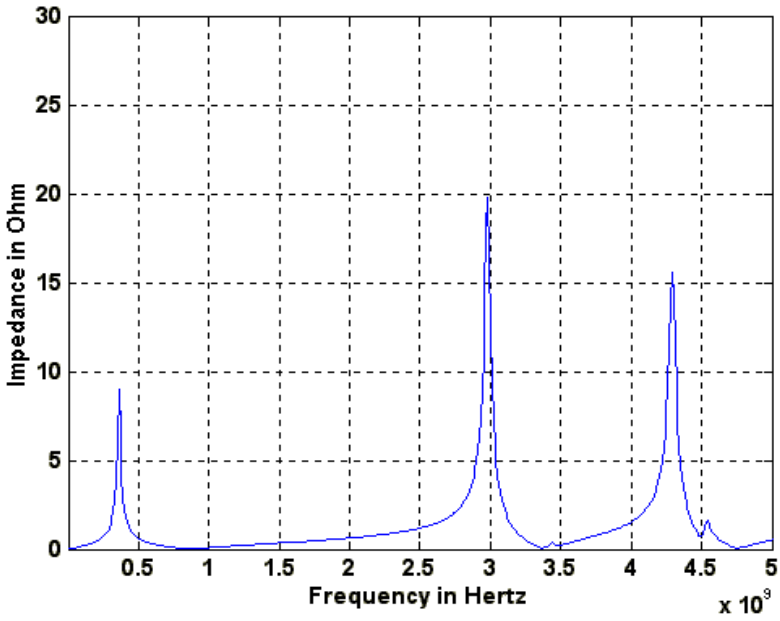

Figure 7.9 Self impedance seen from the port,2

Port 1 represents the location of the VRM connector with 0.1 nH of inductance and 10mOhm of resistance which was defined at x=0 cm and y=2.5cm. Port 2 represents the location of the Gaussian current source which was defined at x=2.5 cm and y=2.5 cm to measure the frequency response of the planes. The Gaussian current source has 0.1 ns of time bandwidth and 1A of peak amplitude. The assumed on-chip decoupling capacitance was 60nF. The

simulation for the plane response was done from 0 to 200ns. The time domain response was converted to the frequency domain using a Fourier transform. Figure 7.9 shows the self-impedance seen from Port 2. The first peak is caused by the interaction between the VRM connector and the plane capacitance. The rest of the resonant peaks are from the plane response.

Two simulations were conducted for capturing the chip-board interaction; namely, the simulation with only the chip and the simulation with chip and board. The impedance seen from the center of the chip was computed. Figure 7.10(a) shows the impedance with only the chip. Figure 7.10(b) shows the impedance from board and chip. From Figure 7.10(a), the resonant peaks occur at 220MHz, 1.9GHz and 3.2GHz, with the chip only. However, when the chip and board are combined, an additional resonance is generated around ~ 40MHz, as shown in Figure 7.10(b). This is the resonance due to the chip-board interactions, which can be calculated as

$$f_r = \frac{1}{2p\sqrt{LC}} \qquad (7.2)$$

When the resonant frequency with the chip attached to the board is known, the effective inductance of the board and chip can be calculated from Eq (7.2) with a first order approximation. With this procedure, the effective inductance is ~0.25nH assuming a chip capacitance of 60nF. As can be seen from Figure 7.10, the effective inductance of the board is in parallel with capacitance of the chip, which forms a parallel RLC resonant circuit that resonates at ~40MHz. The circuits on the chip see a high impedance power supply at this frequency, which can cause problems, if targeted during system operation.

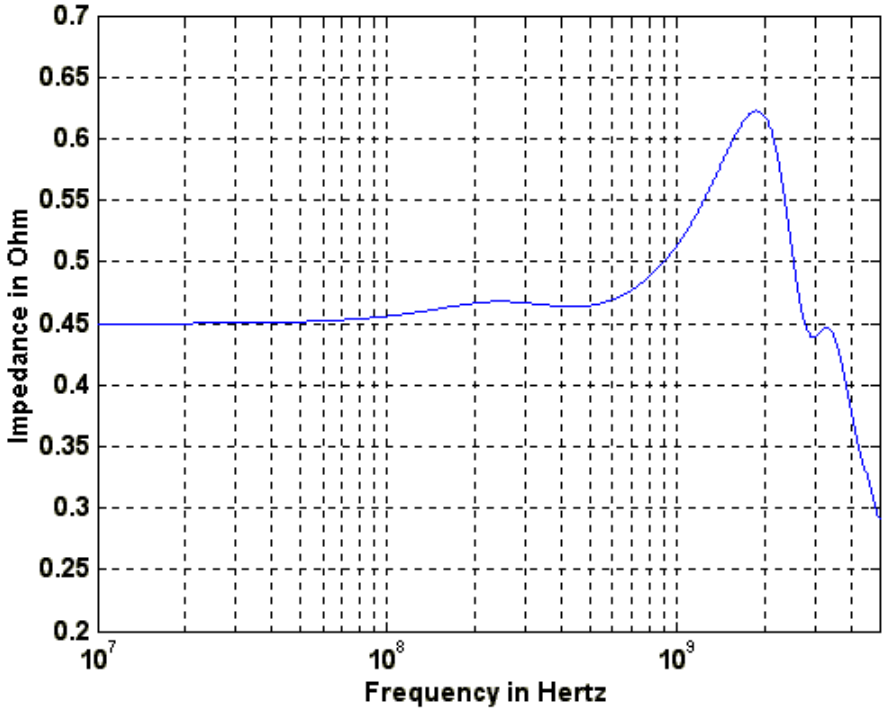

Figure 7.10(a) Self-impedance seen from the chip only

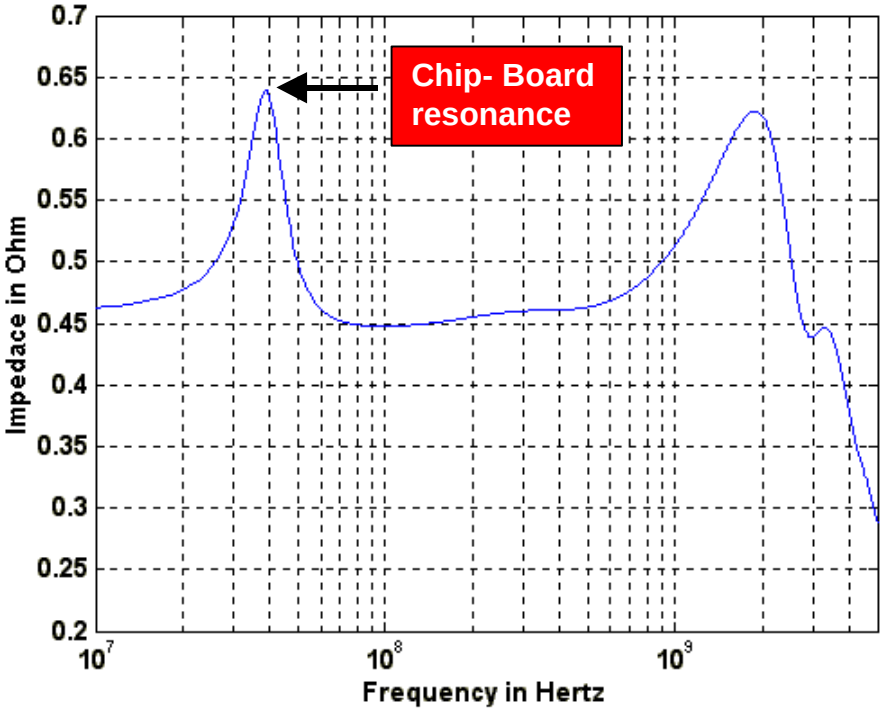

Figure 7.10(b) Self- impedance from the chip attached to board

VII.3 Summary

In this chapter, the circuit FDTD method was applied to a wafer level package. The results were analyzed to understand the various interactions in the system hierarchy. Also, the suitable inductance for the compliant interconnect that meets the noise tolerance for a large chip was calculated. For the simulation of wafer level package on an integrated board, the interactions between the chip and board were included for the computation of power supply noise. It was shown that the resonant peak at low frequency is caused by the inductance of the board and capacitace of the chip, which forms a parallel resonant circuit. This presents a high impedance to the chip power terminals which can disturb the chip supply voltage and impact the operation of the chip.

Chapter VIII

Summary and Future work

The goal of this dissertation was to demonstrate the feasibility of simulating power supply noise at the system level. This capability will enable the design of future nano-systems. In particular, the thesis is targeted towards CMOS based systems containing large chips in multi-layered packages and boards. This dissertation used the Finite Difference Time Domain (FDTD) method to solve the circuit equations extracted from the physical dimensions of the interconnections in the power distribution network.

The FDTD method has also been used to simulate the power supply noise for area array chips containing multiple levels of metalization. Effects such as peak noise distribution, noise propagation and on-chip decoupling have been quantified.

The FDTD method has been extended to include non-linear circuits, and verified with SPICE. Using the FDTD method, the effect of excessive power supply noise on the output of non-linear circuits has been quantified.

The planes that form an integral part of the package and board power distribution have been analyzed. Issues such as power supply impedance and radial wave propagation effects have been studied. Based on the physical

phenomena observed in packages and boards, a technique for extending the cavity resonator model for multiple planes has been proposed, which has been verified through measurements. In addition, the placement of decoupling capacitors on boards has been analyzed.

Devices driving long on-chip buses generate power supply noise based on the path of the return currents in the power distribution network. This is caused by the mutual inductance and coupling capacitance between the signal lines and the power distribution network. This problem is ideally suited for analysis using the FDTD method. The FDTD algorithm which includes the mutual inductance and coupling capacitance was developed and used to simulate long on-chip bus lines.

The cavity resonator model for multiple planes was implemented using the FDTD method. This was combined with the flip chip inductance, via inductance and solder ball inductance to capture the vertical and lateral parasitic inductance/capacitance in the package and board power distribution network.

Wafer level packages (WLP's) are defined as packages that are less than 1.2 times the size of the chip. WLP's offer a smaller footprint, lower parasitics and more inputs/outputs per unit area than ball grid array, resulting in better electrical performance. The FDTD method was applied to a wafer level chip scale package assembled on an integrated, high-density printed circuit board. The results have been analyzed to understand the various interactions in the system hierarchy.

An important effect that is often neglected in the computation of power supply noise is the interaction between the chip-package and package-board.

This interaction can cause additional resonances in the system. If these resonances have sufficient magnitude and are triggered during system operation, excessive noise can be generated in the system. The purpose of the co-simulation was to capture these resonances that are otherwise absent when each section of the system is analyzed.

As an extension to the methods described in this dissertation, the following items are proposed:

1. *Generation of a time domain macro model for non linear circuits.*

   This dissertation used the simple inverter circuits to mimic I/O driver or logic circuits. However, in reality, circuit blocks consist of complicated combinations of CMOS transistors, which can be computationally expensive for simulation at the system level. Hence, a compact form of non-linear circuit models can be developed, which can be simulated using the FDTD method.

2. *Generation of wavelet based macro-models for passive networks and their connection to the non-linear model described above.*

   The circuit FDTD method discussed in this dissertation is a time marching method. Therefore, when the time step is small, the time duration for the simulation can be long, making the method inefficient. Wavelet based techniques can be used to improve the efficiency.

3. *Efficient and realistic system level modeling of the power and signal integrity in "state of the art" microprocessors and packages.*

   Due to the advances in the process technology, today's electronic systems require an optimized design for maintaining signal and power integrity. The ability of the circuit FDTD method to solve a large network can be used to iteratively design the power distribution network.

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