NOISE SUPPRESSION AND ISOLATION IN MIXED-SIGNAL SYSTEMS USING ALTERNATING IMPEDANCE ELECTROMAGNETIC BANDGAP (AI-EBG) STRUCTURE

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NOISE SUPPRESSION AND ISOLATION IN MIXED-SIGNAL SYSTEMS USING ALTERNATING IMPEDANCE ELECTROMAGNETIC BANDGAP (AI-EBG) STRUCTURE

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Dedicated to
my parents
and
my brother and sister, and my aunt
for their support, encouragement, and love

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SUMMARY

With the evolution of technologies, mixed-signal system integration is becoming necessary for combining heterogeneous functions such as high-speed processors, radio frequency (RF) circuits, memory, microelectromechanical systems (MEMS), sensors, and optoelectronic devices. This kind of integration is required for convergent microsystems that support communication and computing capabilities in a tightly integrated module. A major bottleneck with such heterogeneous integration is the noise coupling between the dissimilar blocks constituting the system. The noise generated by the high-speed digital circuits can couple through the power distribution network (PDN) and this noise can transfer to sensitive RF circuits, completely destroying the functionality of noise-sensitive RF circuits.

One common method used for mixed-signal integration in the package is splitting the power and/or ground planes. The gap in the power and ground planes can partially block the propagation of electromagnetic waves. However, electromagnetic energy can still couple through the split, especially at frequencies greater than 1 GHz. The AI-EBG structure in this dissertation has been developed to suppress unwanted noise coupling in mixed-signal systems and this AI- EBG structure shows excellent isolation (-80 dB ~ -140 dB), which results in a noise coupling-free environment in mixed-signal systems. The AI-EBG structure would be part of the power distribution network (PDN) in systems and is expected to have a significant impact on noise suppression and isolation in mixed-signal systems in the future.

CHAPTER 1

INTRODUCTION

The integration of wireless technologies in handsets and mobile computers is forcing the integration of high-speed digital circuits with analog and radio frequency (RF) circuits. When the output drivers or internal logic circuits of a microprocessor switch simultaneously, the power supply noise generated from the noisy digital circuits can deteriorate the performance of sensitive RF/analog circuits. RF front-end circuits like low noise amplifiers (LNAs) need to detect low-power signals, and are extremely sensitive in nature. A large noise spike in or close to the operating frequency band of the device can de-sensitize the circuit, destroying its functionality. To prevent this, all radio architectures include filters and other narrow band circuits, which prevent the noise in the incoming spectrum from reaching the LNA. However, there are no systematic means for filtering noise from other sources – for example, noise can couple through the power rail and appear at the output of the LNA, where it can degrade the performance of the downstream circuits. Thus, an efficient noise suppression technique is required for isolating sensitive RF/analog circuits from noisy digital circuits.

The sensitivity of RF/analog circuits to power supply noise has resulted in difficulties for integration of digital and RF/analog subsystems. One common method used for mixed-signal integration in the package is splitting the power and/or ground planes [1]. The gap in the power and ground planes can partially block the propagation of electromagnetic waves. For this reason, split planes are usually used to isolate sensitive

RF/analog circuits from noisy digital circuits. However, electromagnetic energy can still couple through the split [10], especially at frequencies greater than 1 GHz. Hence, this method only provides marginal isolation (-20 dB ~ -60 dB) at frequencies above ~ 1 GHz and becomes ineffective as system operating frequency increases. Further, as systems become more and more compact, use of multiple power supplies becomes expensive. The use of ferrite beads across the split can result in a common power supply; however, since ferrite beads resonate above 200 MHz, the coupling between split islands increases at higher frequencies. The power segmentation method was proposed recently in [13], [14] but this method only provides good isolation at high frequencies over a narrow frequency band and since this narrow frequency band is fixed by the size of the structure, this frequency band is not tunable. Hence, the development of noise isolation methods is required for enabling integration of mixed-signal systems.

The focus of this dissertation is on noise suppression and isolation in mixed-signal systems using a novel electromagnetic bandgap (EBG) structure called alternating impedance EBG (AI-EBG) structure. The AI-EBG structure in this dissertation has been developed to suppress unwanted noise coupling in mixed-signal systems and this AI-EBG structure shows excellent isolation (-80 dB ~ -140 dB), which results in a noise coupling-free environment in mixed-signal systems. The AI-EBG structure would be part of the power distribution network (PDN) in systems and is expected to have a significant impact on noise suppression and isolation in future mixed-signal systems.

1.1 Power distribution network (PDN)

A power distribution network (PDN) is used to deliver power to core logic and I/O circuits in any semiconductor system. The PDN for the typical high-speed digital system is shown in Figure 1.1 and consists of power and ground planes in the board, power and ground planes in the package, a switching regulator, and decoupling capacitors. The PDN supplies drivers (switching circuits) that generate signals and receivers that receive the signals, with voltage and current to function. With advances in silicon technology, power supply voltage has reduced according to the scaling rules while the amount of power required has increased with every computer generation. As a result, the current delivery requirement for the power distribution network has increased greatly and the tolerance for the power supply noise has decreased. It has been recognized that the power supply noise induced by large numbers of simultaneously switching circuits in the power distribution network can limit their performance [1]-[5].

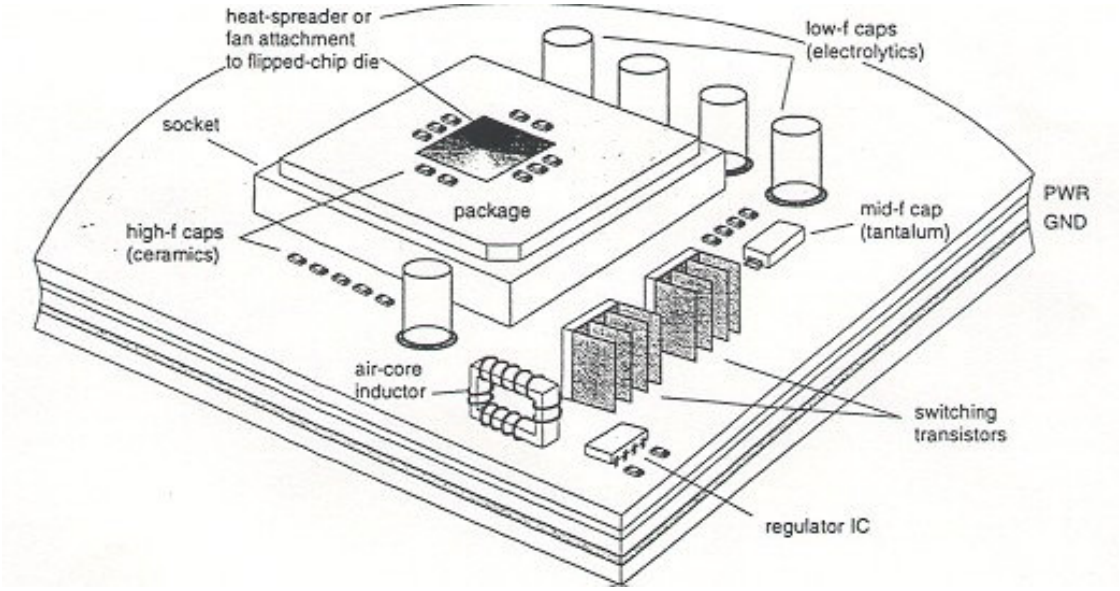


Figure 1.1 Power distribution network for the typical high-speed digital system [1].

Figure 1.2 shows the electrical equivalent circuit of the PDN, which can be mapped from the mechanical structure of the system in Figure 1.1 [1]. For a superior design of the power distribution network, the impedance of the power/ground planes should be designed to be as low as possible over the entire bandwidth of the signal [8]. As a result, the frequency-dependent driving point impedance (Z) of the PDN at the circuit terminals shown in Figure 1.2 should be kept very small compared to the impedance of the circuit load of each chip to avoid large voltage drops in the PDN.

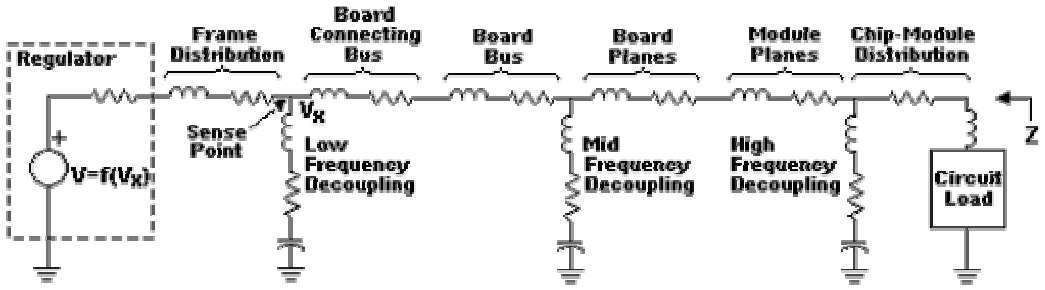


Figure 1.2 Equivalent circuit diagram for power distribution network [1].

A typical output impedance plot for the PDN looking back from the circuit loads is shown in Figure 1.3 [1]. At low frequencies, a power distribution network acts as a capacitor. In the mid-frequency range, a good network should behave as a transmission line with very low characteristic impedance, with the latter being orders of magnitude lower than the impedance of the circuit load. As the frequency increases beyond the mid-frequency range, the network has an inductive behavior with multiple resonant frequencies.

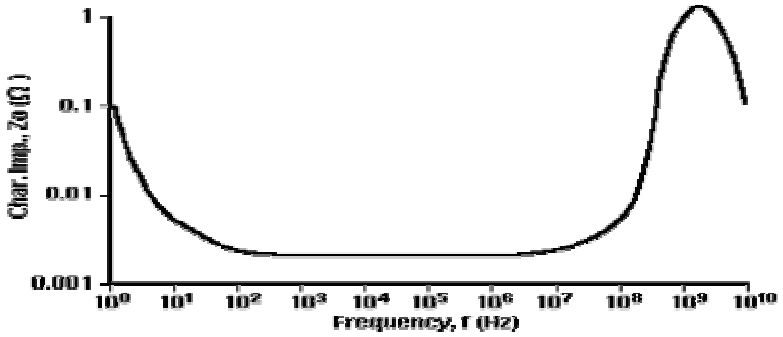


Figure 1.3 Output impedance for the typical power distribution network [1].

Since the fast switching speed of the digital circuits results in sudden current demand, noise generated can degrade system performance [1]-[6]. A major source of this noise can be attributed to the power distribution network (PDN) of the package and board. For future high-speed digital systems, one method to suppress noise is to design the PDN by identifying a target impedance [8], which has to be met over a broad frequency range. Based on the allowed ripple on the power supply rails, the target impedance for the PDN can be computed as

$$Z_{target} = \frac{V_{dd} \times 0.05}{I} \tag{1.1}$$

where V_{dd} is a power supply voltage, I is the current, 0.05 is the 5 % ripple voltage allowed. Using the above equation, the target impedance for various cases can be computed as in Table 1.1. For example, in 2005, a target impedance of 0.48 mΩ is required using (1.1). Based on the International Technology Roadmap for Semiconductors (ITRS) voltage and power projections, the target impedance is expected to reduce by a factor of 2 per computer generation, with a target impedance requirement of 0.06 mΩ in the year 2016. This is 16 times lower than the 0.93 mΩ required in 2001.

Since transient currents cause voltage fluctuations, a high-speed digital system has to meet the target impedance over a broad bandwidth (at least from DC to 5 GHz in 2005). In addition to suppressing noise by maintaining a small self-impedance, a small target transfer impedance is also required between the processor and noise-sensitive areas of the system.

Several major components are currently used to meet the target impedance over the wide frequency range. The voltage regulator module (VRM) is effective up to about 1 kHz. Bulk capacitors supply current and maintain a low PDN impedance from 1 kHz to 1 GHz. High frequency ceramic capacitors maintain the PDN impedance from 1 MHz to 1

Table 1.1 Target impedance tendency and projection based on ITRS 2001

Year	Power (W)	Vdd (V)	Current (A)	Frequency (MHz)	Z_{target} (mΩ)
1991	5	5	1	16	500
1996	25	2.6	10	300	27
2001	130	1.1	118	1700	0.93
2003	150	1.0	150	3090	0.67
2005	170	0.9	189	5170	0.48
2007	190	0.7	271	6740	0.26
2010	218	0.6	363	12000	0.17
2013	251	0.5	502	19000	0.1
2016	288	0.4	720	29000	0.06

GHz [74]. Electromagnetic bandgap (EBG) structures have been suggested to meet the target impedance goals over 1 GHz [26].

1.2 Simultaneous Switching Noise (SSN)

Simultaneous switching noise (SSN) refers to a noise fluctuation or voltage glitch generated in a digital system due to rapid changes in current caused by switching of many circuits in the system at the same time [32]. SSN is also referred to as "delta-I" noise because of its direct dependence on the rate of change of current or called "ground bounce" since the voltage glitch corresponds to an effective change of the power supply voltage and therefore can be seen as a shift in the internal ground reference voltage level. With recent advances in CMOS technology resulting in a faster device switching speed and higher package density, simultaneous switching noise (SSN) induced by a large number of internal and external switching circuits has become a critical issue in high-speed digital systems. SSN is mainly caused by inductance in the PDN associated with the board, package, and chip. Figure 1.4 shows an equivalent circuit for the system where the package and printed circuit board (PCB) metal layers add inductance to the power distribution network [2]. In this system, the voltage and current to the chip are supplied from a power supply on the motherboard through the metal layers on the package and PCB. The local supply on the chip acts as a non-ideal supply, primarily because the route taken by the power supply current through the board, package, and chip introduces a series inductance L into the system. There is a serious side effect of series inductance in the power supply circuitry. Whenever the power supply current changes in the presence of series inductance, the local V_{dd} level will drop since the current flowing through an

inductor cannot change instantaneously. Consequently, the transient supply currents flowing through these interconnections cause voltage fluctuations on the power supply rails of the chip. This voltage fluctuation, which is referred to as SSN, is given by:

$$\Delta V_{SSN} = NL_{eff} \frac{di}{dt} \tag{1.2}$$

where N is the number of simultaneously switching drivers, L_{eff} is the effective inductance of the power distribution network, and di/dt is the current slew rate of a single driver.

It is important to note that the effective inductance can be defined only for a loop of current. As shown in (1.2), the SSN is directly proportional to the current slew rate and

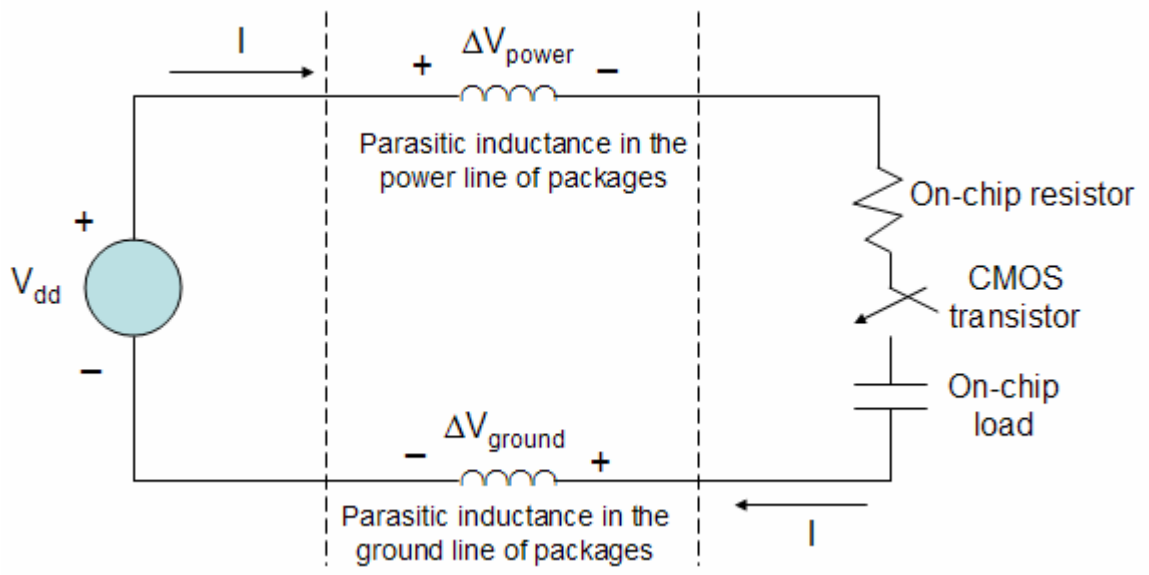


Figure 1.4 Equivalent circuit for the system where the package and printed circuit board (PCB) metal layers add inductance to the power distribution network [2].

the effective inductance. As a result, controlling the total allowed system noise requires controlling either the driver's slew rate or the effective inductance. However, the control

of the driver's slew rate requiring driver slowdown is not adequate because it adds delay to the driver output and can ultimately increase the machine cycle time. Hence, reducing the effective inductance is the proper solution. In the next section, traditional and advanced methods using decoupling capacitors to mitigate SSN are discussed.

1.3 Discrete and Embedded Decoupling Capacitors

A traditional method to suppress SSN is through decoupling capacitors on the board, package, and chip. Decoupling capacitors are connected between the power and the ground planes in order to lower the impedance of the power distribution network as well as supply current bursts for fast switching circuits [70]-[72].

To support the peak current needs of fast switching circuits, decoupling capacitors accumulate charge over the clock cycle, and then rapidly discharge during fast transitions. Power supplies cannot fulfill this role since voltage regulators respond too slowly and since the regulators are typically too far away. Decoupling capacitors provide fast switching drivers with extra current required to charge the load capacitor instead of the power supply. As a result, the power supply noise is reduced since the inductive effect in the loop current path is decreased by the decoupling capacitors.

The decoupling capacitors are expected to behave as a short circuit between the power/ground planes at high frequencies. However, it has been found that the parasitic inductance of the leads and mounting pads of the decoupling capacitors strongly limits their power supply noise mitigation ability [26]. In fact, the decoupling capacitor behaves as a series RLC resonant circuit, which becomes close to a short circuit only around its self-resonant frequency. As a result, the decoupling capacitor can be represented as a

series RLC circuit, as shown in Figure 1.5, and the impedance of the decoupling capacitor can be represented by the following equation:

$$Z_{real\_decap} = R_{ESR} + j\omega L_{ESL} + \frac{1}{j\omega C} \tag{1.3}$$

where Z_{real_decap} is the impedance of real decoupling capacitor, R_{ESR} is the equivalent series resistance (ESR), L_{ESL} is the equivalent series inductance (ESL), C is the capacitance, and $\omega = 2\pi f$ is the angular frequency.

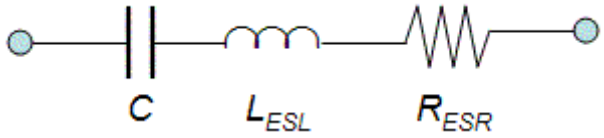


Figure 1.5 Model of the real decoupling capacitor.

The self-resonant frequency of the real decoupling capacitor is given by

$$f_{SRF} = \frac{1}{2\pi\sqrt{L_{ESL}C}} \tag{1.4}$$

at which the reactive impedances are cancelled and the impedance of the decoupling capacitor has a magnitude of R_{ESR}, which is the minimum magnitude of the impedance, as shown in Figure 1.6.

Due to this kind of characteristic of the decoupling capacitors, different kinds of decoupling capacitors should be used over the wide frequency range, depending on the package structure. Based on the resonant frequency, the decoupling capacitors can be

categorized into low-frequency, mid-frequency, and high-frequency capacitors, and incorporated at appropriate places throughout the system, as shown in Figure 1.1, for

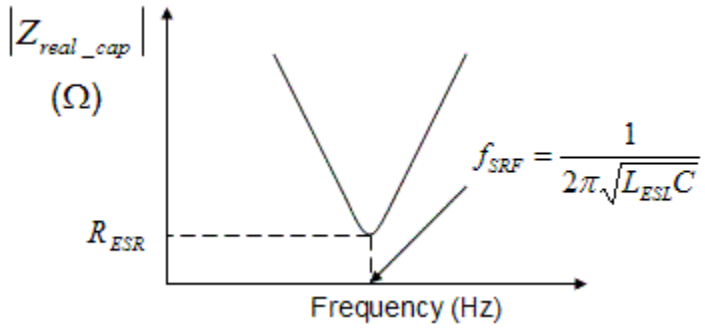


Figure 1.6 Typical response of a decoupling capacitor.

filtering the frequency components of current changes caused by circuit switching.

Typically, low-frequency and mid-frequency decoupling capacitors are mounted on the package and board, and high-frequency decoupling capacitors for $f > 1$GHz are buried in the chip as trench capacitors. However, it should be noted that it is almost impossible to lower the impedance of the PDN at frequencies greater than 1 GHz using decoupling capacitors since the parasitic inductance of the decoupling capacitor is dominant at high frequencies.

In general, the decoupling capacitors can be either discrete or embedded. The decoupling capacitors mentioned above are discrete decoupling capacitors. The embedded capacitors provide better high-frequency performance since they have less parasitic inductance but cannot suppress the intrinsic modes of the parallel-plate waveguide, which will be discussed in the next section. Another disadvantage of the embedded capacitors is that the process for the embedded capacitors is not standardized

and therefore the process can be a high-cost process. For example, Figure 1.7 shows the cross section of Barium Titanate ($BaTiO_3$) capacitor that was developed at the Packaging Research Center (PRC) at Georgia Tech. This embedded capacitor was fabricated using a hydrothermal process. In this process, nanograined ultra thin crystalline Barium Titanate thin films were synthesized on laminated copper foils using the low cost low temperature (< 100 °C) hydrothermal process. Hydrothermal synthesis of $BaTiO_3$ involves treating Ti-coated copper clad laminates with Ba2+ ions in highly alkaline solution at 95 °C. With this method high k thin films can be integrated into organic packages using standard printed wiring board processes such as lamination and lithography [73].

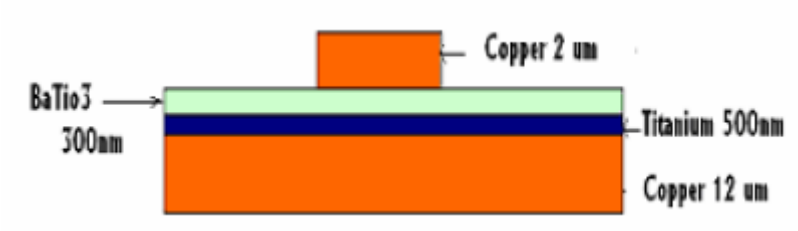


Figure 1.7 Cross section of $BaTiO_3$ capacitor [73].

1.4 Power/Ground Planes

The power/ground plane pair in a power distribution network behaves like a parallel-plate waveguide at high frequencies. A time-varying current flowing through vias in the PDN due to switching of the digital circuit causes the excitation of electromagnetic (EM) waves, which propagates between power and ground planes in the package and board. These waves reflect from the edges in the power distribution network

of the package and board and cause resonances over the frequency range, which increases the impedance magnitude of PDN at certain resonant frequencies. Hence, it is important to analyze the power/ground plane pair as a parallel-plate waveguide. The parallel-plate waveguide can support transverse electromagnetic (TEM), transverse magnetic (TM), and transverse electric (TE) waves, in addition to cavity resonator modes.

Consider a parallel-plate waveguide consisting of two perfectly conducting plates separated by a dielectric material as shown in Figure1.8. The dimensions in the x and z directions are assumed to be much larger than the dielectric thickness d, which makes fringing fields on the edges of the structure and any variation in the x direction neglected.

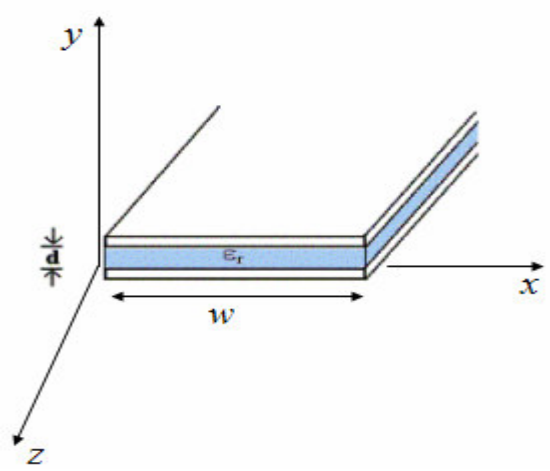


Figure 1.8 Parallel-plate waveguide.

1.4.1 Transverse Electromagnetic (TEM) Waves

Transverse electromagnetic (TEM) waves represent waves in which electric and magnetic fields are perpendicular to each other and both are transverse to the direction of wave propagation. For example, if propagation in the z direction, TEM waves are waves

that contain neither E_z nor H_z where E_z is the electric field component in the z direction and H_z is the magnetic field component in the z direction. The TEM wave solution can be obtained by solving Laplace's equation for the electrostatic potential $\Phi(x, y)$ between the two conducting plates:

$$\nabla^2 \Phi(x, y) = 0, \qquad \text{for } 0 \le x \le w \text{ and } 0 \le y \le d \tag{1.5}$$

Assuming that the upper conducting plate has a potential V_{dd} and lower conducting plate has a potential zero, we get

$$\Phi(x, d) = V_{dd}\,, \tag{1.6}$$

$$\Phi(x, 0) = 0. \tag{1.7}$$

Since we assume that there is no variation in x direction, the general solution to (1.5) for $\Phi(x, y)$ is

$$\Phi(x, y) = A_1 + A_2 y\,, \tag{1.8}$$

where A_1 and A_2 are unknown constants.

Using the boundary conditions in (1.6) and (1.7), we have

$$\Phi(x, y) = \frac{V_{dd}}{d} y\,. \tag{1.9}$$

The transverse electric field is then obtained as

$$\bar{E}(x, y, z) = -\nabla \Phi(x, y) e^{-jkz} = -\frac{V_{dd}}{d} e^{-jkz}\, \hat{y}, \tag{1.10}$$

where $k = \omega\sqrt{\mu\varepsilon}$ is the propagation constant of the TEM wave.

Then, magnetic field can be calculated as

$$\bar{H}(x, y, z) = \frac{1}{\eta} \hat{z} \times \bar{E}(x, y, z) = \frac{V_{dd}}{\eta d} e^{-jkz}\, \hat{x}, \tag{1.11}$$

where $\eta = \sqrt{\frac{\mu}{\varepsilon}}$ is intrinsic impedance of the dielectric material between two conducting plates.

The voltage V between the two conducting plates can be obtained as

$$V = -\int_{y=0}^{y=d} E_y dy = V_{dd} e^{-jkz}, \tag{1.12}$$

where $E_y = -\frac{V_{dd}}{d} e^{-jkz}$.

The total current flowing on the upper conducting plate can be calculated as

$$I = \int_{x=0}^{x=w} \bar{J}_S \cdot \hat{z} dx = \int_{x=0}^{x=w} (-\bar{y} \times \bar{H}) \cdot \hat{z} dx = \frac{w V_{dd}}{\eta d} e^{-jkz}, \tag{1.13}$$

where $\bar{J}_s = -\bar{y} \times \bar{H}$ is surface current density on the upper conducting plate.

Hence, the characteristic impedance of the parallel-plate waveguide is given by

$$Z_0 = \frac{V}{I} = \frac{\eta d}{w}. \tag{1.14}$$

It should be noted that the characteristic impedance of the parallel-plate waveguide depends only on the material parameters and the geometry of the waveguide.

1.4.2 Transverse Magnetic (TM) Waves

Transverse magnetic (TM) waves represent waves that do not have a component of the magnetic field in the direction of wave propagation. For example, for propagation along the z direction, TM waves are waves that contain nonzero E_z but $H_z = 0$.

The Helmholtz equation or wave equation for $\bar{E}$ is given as:

$$\nabla^2 \overline{E} + \omega^2 \mu \varepsilon \overline{E} = 0, \tag{1.15}$$

where μ is the permeability of the medium and ε is the permittivity of the medium.

For E_z, the Helmholtz equation can be written as

$$(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2} + k^2) E_z = 0, \tag{1.16}$$

where $k = \omega\sqrt{\mu\varepsilon}$ is the propagation constant of the medium.

Since $E_z(x, y, z) = e_z(x, y) e^{-j\beta z}$, equation (1.16) can be reduced to a two-dimensional wave equation for e_z as:

$$(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + k_c^2) e_z(x, y) = 0, \tag{1.17}$$

where $k_c^2 = k^2 - \beta^2$.

Since the dimension in the x direction is assumed to be much larger than the dielectric thickness d, making any variation in the x direction neglegible (i.e., $\frac{\partial}{\partial x} = 0$), equation (1.17) becomes

$$(\frac{\partial^2}{\partial y^2} + k_c^2) e_z(x, y) = 0. \tag{1.18}$$

The general solution to equation (1.18) is of the following form

$$e_z(x, y) = A_1 \sin k_c y + A_2 \cos k_c y. \tag{1.19}$$

Applying the boundary conditions that $e_z(x, y)$ should be zero at $y = 0$ and d, we obtain

$$A_2 = 0 \text{ and } k_c = \frac{n\pi}{d}, \text{ n = 0, 1, 2 …} \tag{1.20}$$

Hence, the electric field in the z direction can be written as

$$E_z(x, y, z) = A_n \sin \frac{n\pi y}{d} e^{-j\beta z}. \tag{1.21}$$

The transverse field components can be derived as follows:

$$H_x = \frac{j\omega\varepsilon}{k_c^2}\frac{\partial E_z}{\partial y} = \frac{j\omega\varepsilon A_n}{k_c}\cos\frac{n\pi y}{d} e^{-j\beta z}, \tag{1.22}$$

$$H_y = -\frac{j\omega\varepsilon}{k_c^2}\frac{\partial E_z}{\partial x} = 0, \tag{1.23}$$

$$E_x = -\frac{j\beta}{k_c^2}\frac{\partial E_z}{\partial x} = 0, \tag{1.24}$$

$$E_y = -\frac{j\beta}{k_c^2}\frac{\partial E_z}{\partial y} = -\frac{j\beta A_n}{k_c}\cos\frac{n\pi y}{d} e^{-j\beta z}. \tag{1.25}$$

For $n = 0$, $E_z = 0$ and $\beta = k = \omega\sqrt{\mu\varepsilon}$, which means that TM_0 mode is identical to the TEM mode for the parallel-plate waveguide. For $n \geq 1$, each n corresponds to a different TM_n mode with its propagation constant given by

$$\beta = \sqrt{k^2 - k_c^2} = \sqrt{k^2 - \left(\frac{n\pi}{d}\right)^2}. \tag{1.26}$$

For a TM wave to propagate, its propagation constant should be real, which requires that the wave number, k, be larger than the cut-off wave number, k_c. Thus, the cut-off frequency for the TM_n mode can be defined as

$$f_c = \frac{k_c}{2\pi\sqrt{\mu\varepsilon}} = \frac{n}{2d\sqrt{\mu\varepsilon}}. \tag{1.27}$$

Hence, the lowest TM mode is TM_1 mode with a cut-off frequency of $f_c = \frac{1}{2d\sqrt{\mu\varepsilon}}$. All higher order modes have cut-off frequencies equal to multiples of this cut-off frequency.

The wave impedance of the TM modes is given by

$$Z_{TM} = -\frac{E_y}{H_x} = \frac{\beta}{\omega\varepsilon} = \frac{\beta\eta}{k} = \eta\sqrt{1-\left(\frac{\omega_c}{\omega}\right)^2}. \qquad (1.28)$$

It is important to note that wave impedances are purely real for $f > f_c$ but purely imaginary for $f < f_c$. The phase velocity can be written as

$$v_p = \frac{\omega}{\beta} = \frac{c}{\sqrt{1-\left(\frac{\omega_c}{\omega}\right)^2}}. \qquad (1.29)$$

It should be noted that the phase velocity is a function of frequency. The group velocity is given by

$$v_g = \frac{d\omega}{d\beta} = c\sqrt{1-\left(\frac{\omega_c}{\omega}\right)^2}. \qquad (1.30)$$

1.4.3 Transverse Electric (TE) Waves

Transverse electric (TE) waves represent waves that do not have a component of the electric field in the direction of propagation. For example, for a wave propagating in the z direction, TE waves contain nonzero H_z but $E_z = 0$.

The Helmholtz equation or wave equation for $\bar{H}$ is given as:

$$\nabla^2 \bar{H} + \omega^2 \mu\varepsilon \bar{H} = 0. \qquad (1.31)$$

For H_z, the Helmholtz equation can be written as

$$\left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2} + k^2\right) H_z = 0, \qquad (1.32)$$

where $k = \omega\sqrt{\mu\varepsilon}$ is the propagation constant of the medium.

Since $H_z(x, y, z) = h_z(x, y)e^{-j\beta z}$, equation (1.16) can be reduced to a two-dimensional wave equation for h_z:

$$(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + k_c^2)h_z(x, y) = 0, \tag{1.33}$$

where $k_c^2 = k^2 - \beta^2$.

Since the dimension in the x direction is assumed to be much larger than the dielectric thickness d, making any variation in the x direction neglegible (i.e., $\frac{\partial}{\partial x} = 0$), equation (1.17) becomes

$$(\frac{\partial^2}{\partial y^2} + k_c^2)h_z(x, y) = 0. \tag{1.34}$$

The general solution to equation (1.18) is of the following form:

$$h_z(x, y) = A_1 \sin k_c y + A_2 \cos k_c y. \tag{1.35}$$

The electric field component, E_x, can be calculated as

$$E_x(x, y, z) = -\frac{j\omega\mu}{k_c^2}\frac{\partial H_z}{\partial y} = -\frac{j\omega\mu}{k_c}(A_1 \cos k_c y - A_2 \sin k_c y)e^{-j\beta z}. \tag{1.36}$$

Applying the boundary conditions that E_x should be zero at $y = 0$ and d, we obtain

$$A_2 = 0 \text{ and } k_c = \frac{n\pi}{d}, \text{ n = 1, 2 …} \tag{1.37}$$

Hence, the magnetic field in the z direction can be written as

$$H_z(x, y, z) = A_n \cos\frac{n\pi y}{d} e^{-j\beta z}. \tag{1.38}$$

The transverse field components can be derived as follows:

$$H_x = -\frac{j\beta}{k_c^2}\frac{\partial H_z}{\partial x} = 0, \tag{1.39}$$

$$H_y = -\frac{j\beta}{k_c^2}\frac{\partial H_z}{\partial y} = \frac{j\beta A_n}{k_c}\sin\frac{n\pi y}{d}e^{-j\beta z}, \tag{1.40}$$

$$E_x = -\frac{j\omega\mu}{k_c^2}\frac{\partial H_z}{\partial y} = \frac{j\omega\mu A_n}{k_c}\sin\frac{n\pi y}{d}e^{-j\beta z}, \tag{1.41}$$

$$E_y = -\frac{j\omega\mu}{k_c^2}\frac{\partial H_z}{\partial x} = 0. \tag{1.42}$$

The propagation constant of the TE_n mode is given by

$$\beta = \sqrt{k^2 - k_c^2} = \sqrt{k^2 - \left(\frac{n\pi}{d}\right)^2}. \tag{1.43}$$

It should be noted that the propagation constant of the TE_n mode is the same as that of the TM_n mode. The cut-off frequency for the TE_n mode can be defined as

$$f_c = \frac{k_c}{2\pi\sqrt{\mu\varepsilon}} = \frac{n}{2d\sqrt{\mu\varepsilon}}. \tag{1.44}$$

Hence, the lowest TE mode is the TE_1 mode with a cut-off frequency of $f_c = \frac{1}{2d\sqrt{\mu\varepsilon}}.$

All higher modes have cut-off frequencies equal to multiples of this cut-off frequency.

The wave impedance of the TE modes is given by

$$Z_{TE} = \frac{E_x}{H_y} = \frac{\omega\mu}{\beta} = \frac{k\eta}{\beta} = \frac{\eta}{\sqrt{1-\left(\frac{\omega_c}{\omega}\right)^2}}. \tag{1.45}$$

1.4.4 Cavity Resonator Modes

Power/ground planes represent large metal layers separated by a small dielectric distance, as shown in Figure 1.9. Due to the small dielectric distance, power/ground planes in the package and PCB are capacitive at low frequencies and are therefore ideal

for supplying power to the integrated circuits. However, with increaseing frequency, planes become inductive and resonate at discrete frequencies [1]. Conventional power

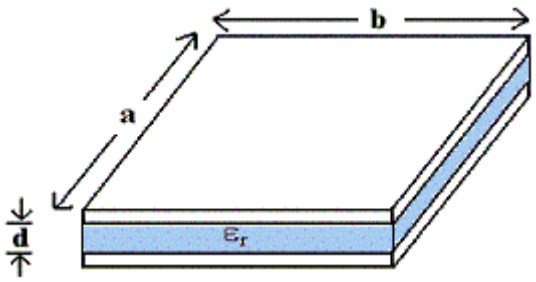


Figure 1.9 Schematic of power/ground planes in package and board.

and ground planes have a dielectric thickness of less than 100 mils and the dielectric thickness is becoming thinner with advances in technology. The lowest TM and TE modes for the parallel-plate waveguide have cut-off frequencies in the order of hundreds of gigahertz, which implies TM and TE modes of the parallel-plate waveguide are not a major concern for the systems operating at 10 GHz and below. For example, TM_1 and TE_1 modes for the power/ground planes with a dielectric thickness of 4.5 mils occur at 618 GHz by equations (1.27) and (1.44). Therefore, the only modes of concerns are the TEM modes of the parallel-plate waveguide and cavity resonator modes due to the finite size of the power/ground planes [77]. For the modes derived for the parallel-plate waveguide in previous sections, it was assumed that the conducting planes have infinite length in the x and z directions. However, real power and ground planes have finite size of width and length, which means that waves propagating to the edges of the power/ground planes have to be reflected back and forth. These reflections combine to

produce a cavity resonator mode at certain frequencies. The rectangular cavity resonator modes occur at the following frequencies [30]:

$$f_{cavity} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2 + \left(\frac{p\pi}{d}\right)^2}, \tag{1.46}$$

where μ is the permeability of a dielectric material, ε is the permittivity of a dielectric material, and m, n, and p are mode numbers equal to 0, 1, 2, … , except that at least one of the mode numbers must be nonzero. The parameters a, b, and d are the dimensions in Figure 1.9. In practical power/ground planes, the dielectric thickness d is much smaller than the width (a) and the length (b), which means the standing wave patterns along dimension d will be at frequencies that are ten to hundred of times larger than the resonant frequencies of waves along the width and length of power/ground planes. Hence, the cavity resonant frequencies in equation (1.46) for practical power/ground planes can be obtained with $p = 0$ and written as:

$$f_{cavity} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2}\ . \tag{1.47}$$

1.5 Noise Coupling in Mixed-Signal System

With the evolution of technologies, mixed-signal system integration is becoming necessary for combining heterogeneous functions such as high-speed processors, radio frequency (RF) circuits, memory, microelectromechanical systems (MEMS), sensors, and optoelectronic devices. This kind of integration is required for convergent microsystems that support communication and computing capabilities in a tightly integrated module. A

major bottleneck with such heterogeneous integration is the noise coupling between the dissimilar blocks constituting the system [9]. The noise generated by the high-speed digital circuits can couple through the power distribution network (PDN) and this noise can transfer to sensitive RF circuits, completely destroying the functionality of noise-sensitive RF circuits. Figure 1.10 shows the noise coupling mechanism due to electromagnetic (EM) waves in a mixed-signal system. The time-varying current flowing through a via due to switching of the digital circuits can cause the excitation of EM waves.

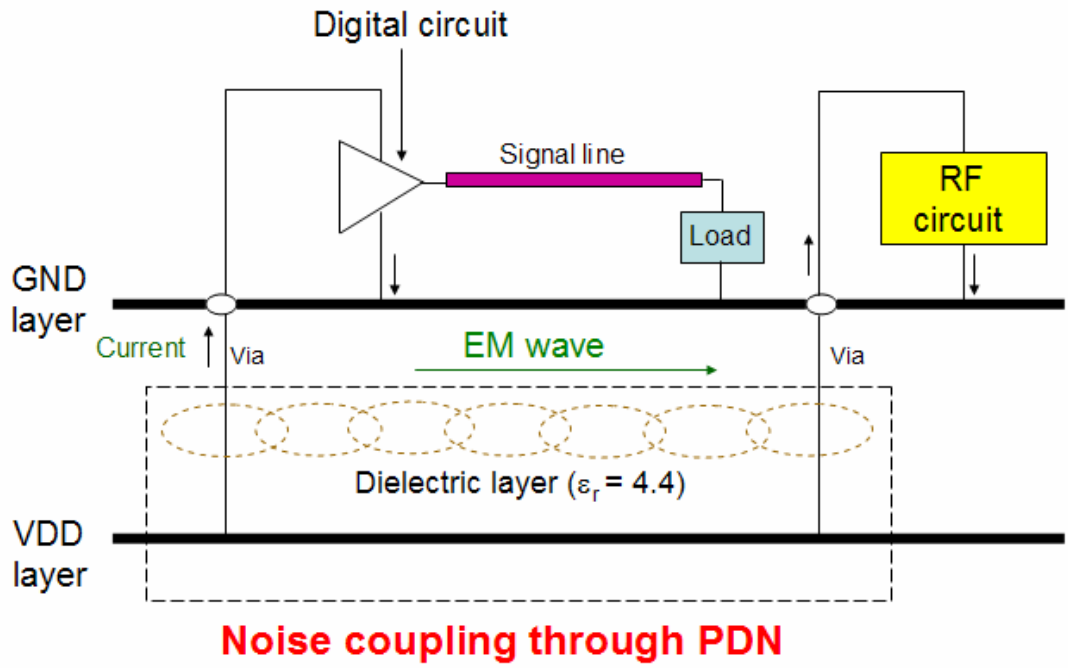


Figure 1.10 Noise coupling in a mixed-signal system.

Since a power/ground plane pair used to supply power to the switching circuits behaves like a parallel-plate waveguide at high frequencies [30], the EM wave propagates between the power/ground plane pair and couples to the RF circuit, causing failure of the

RF circuit. To prevent this noise coupling, traditional isolation techniques have used split planes with multiple power supplies [10], split planes and ferrite beads with a single power supply [12] and power-plane segmentation [13], [14]. All these methods have two fundamental problems namely, a) they provide poor isolation in the -20 dB to -60 dB range [10] above 1 GHz and b) they provide narrow band capability. Hence, the development of better noise isolation methods for the integration of digital and RF functions is necessary. One method for achieving high isolation over broad frequency range is through the use of electromagnetic band gap (EBG) structures. EBG structures are periodic structures that suppress wave propagation in certain frequency bands while allowing it in others. For power delivery networks, EBG structures can be constructed by patterning the ground plane. In this dissertation, a novel EBG structure based on the alternating impedance (AI-EBG) concept is discussed for use in power delivery networks.

1.6 Current Isolation Methods

Decoupling capacitors are usually used to suppress simultaneous switching noise in digital systems. However, the decoupling capacitors are not good enough for noise suppression and isolation in mixed-signal systems since noise-sensitive RF circuits exist in the systems. Currently, there are three methods for isolating sensitive RF circuits from noisy digital circuits in mixed-signal systems: split planes [10], split planes with ferrite beads [12], and power-plane segmentation [13], [14]. Each of these methods is described in detail.

1.6.1 Split Planes

One typical approach to isolate the sensitive RF/analog circuits from the noisy digital circuits is to split the power plane or both power and ground planes [10]. The gap in power plane or ground plane can partially block the propagation of electromagnetic waves. For this reason, split planes are usually used to isolate sensitive RF/analog circuits from noisy digital circuits. Although split planes can block the propagation of electromagnetic waves, part of the electromagnetic energy can still couple through the gap [10]. Hence, this method only provides a marginal isolation (-20 dB ~ -60 dB) at high frequencies (usually above ~ 1 GHz) and could create a serious problem as the sensitivity of RF circuits increases and the operating frequency of the system increases. Generally, split planes provide good isolation (-70 dB ~ -80 dB) at low frequencies (usually below ~ 1 GHz) but show poor isolation (-20 dB ~ -60 dB) at high frequencies because of electromagnetic coupling. In addition to this, split planes sometimes require separate power supplies to maintain the same DC level, which is not cost effective.

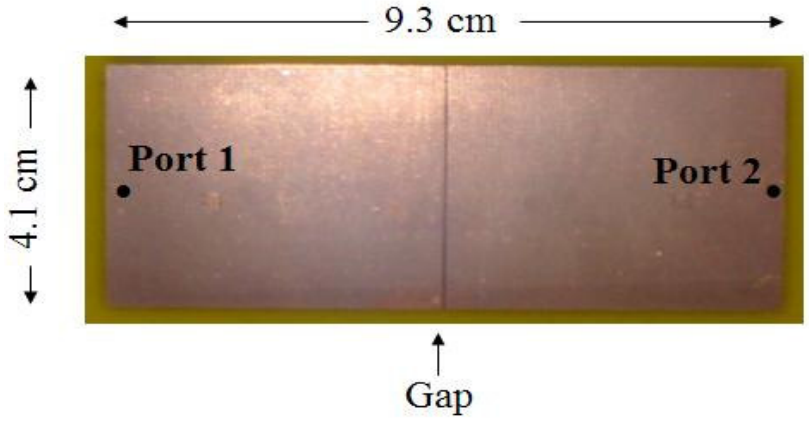


Figure 1.11 Photo of the fabricated split planes.

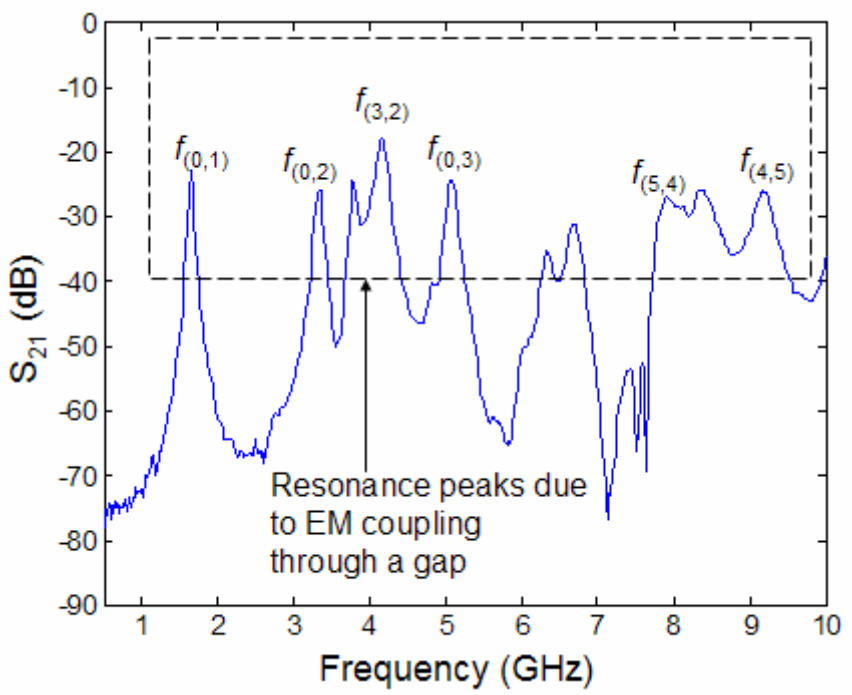
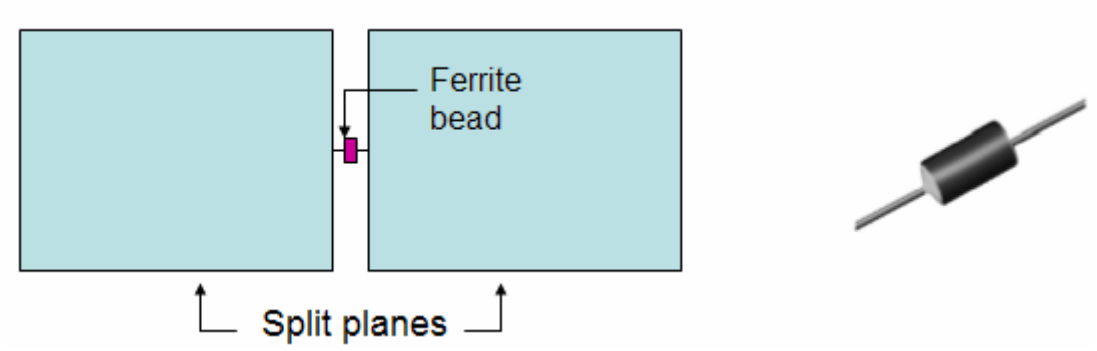


Figure 1.12 Measured transmission coefficient (S21) for the split planes in Figure 1. Some cavity resonator modes are shown by equation (1.10).

Figure1.11 shows a fabricated structure containing split planes. The size of the structure is 9.3 cm x 4.1 cm and port 1 and port 2 are located around at the edges. Figure 1.12 shows the measured transmission coefficient (S_{21}) between port 1 and port 2. It is clear that split planes show good isolation up to 1 GHz but show poor isolation at high frequencies (over 1 GHz). It is observed in Figure 1.12 that there are many resonance peaks above 1 GHz as a result of EM coupling through the gap. This measurement proves that electromagnetic energy can still couple through the split, especially at frequencies greater than 1 GHz. Hence, this method only provides marginal isolation (-20 dB ~ -60 dB) at frequencies above ~1.5 GHz, and becomes ineffective as system operating frequency increases. The resonance peaks in Figure 1.12 can be calculated using (1.47) and some cavity resonance modes are shown in Figure 1.12.

1.6.2 Split Planes with Ferrite Beads

Since split planes require multiple power supplies to maintain the same DC level, if that system requires the same DC level, the use of split planes is not cost effective. So, for a system that requires the same DC level, a ferrite bead is placed between the split planes, as shown in Figure 1.13 (a). A ferrite bead is a dowel-like device which has a center holes and is composed of ferromagnetic material. Figure 1.13 (b) shows a ferrite bead. When placed onto a current carrying conductor it acts as an RF choke. It offers a convenient, inexpensive, yet a very effective means of RF shielding, parasitic suppression and RF decoupling. The simple equivalent circuit for a ferrite bead is a single inductor. Since an inductor is a shorted circuit at the DC, a ferrite bead can provide a DC path



(a) (b)

Figure 1.13 (a) A ferrite bead between split planes and (b) Photo of a ferrite bead [75].

for the split planes. Hence, a single power supply can be used for the split planes with a ferrite bead. However, a real ferrite bead does not behave like an ideal inductor. Figure 14 shows typical impedance characteristic over a wide frequency range. The impedance

of the ferrite bead starts to drop around 200 MHz, which makes isolation worse after 200 MHz. Hence, this method also cannot provide good isolation at the high frequencies.

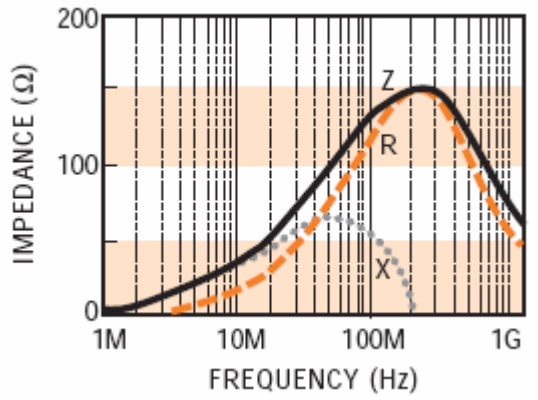


Figure 1.14 Typical impedance characteristics of a ferrite bead [75].

1.6.3 Power-plane segmentation method

A power-plane segmentation method was recently reported in [13], [14]. In this method, split planes are connected through a narrow conducting neck. Figure 1.15 shows the schematic of power-plane segmentation. This method provides good isolation (-50 dB ~ -80 dB) in a narrow high-frequency range (frequency range: 300 MHz ~ 700 MHz). But this narrow high-frequency range is not controllable since the size of the split planes determines this high-frequency range. For example, a structure with the power-plane segmentation in Figure 1.16 (a) was simulated. In this case, the size of the split power planes was 4.9 cm x 5.5 cm, the size of the ground plane was 10 cm x 5.5 cm, and the size of the narrow conducting neck was 0.2 cm x 0.5 cm. The transmission coefficient (S_{21}) between two ports in Figure 1.16 (a) is shown in Figure 1.16 (b). Hence, this

method is not appropriate for wide-band applications and is not good enough for mixed-signal system applications that require a higher isolation level.

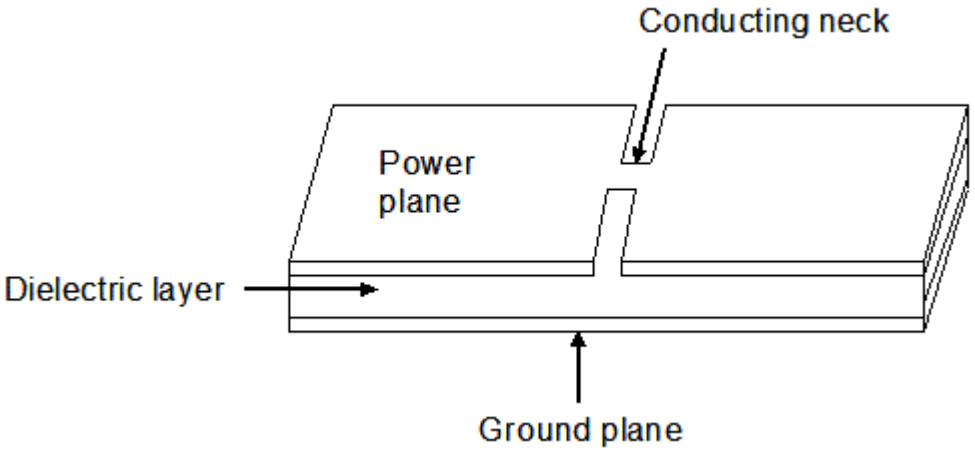
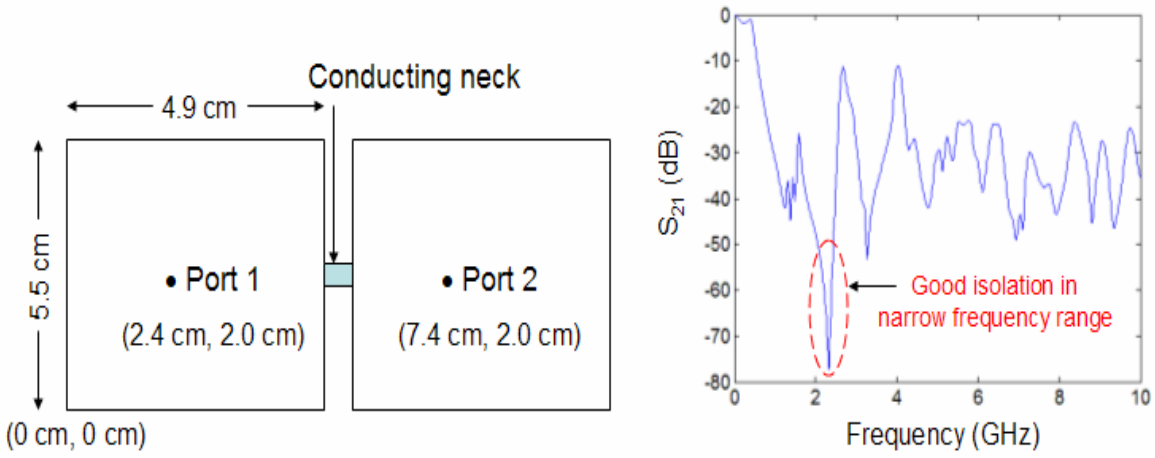


Figure 1.15 Schematic of power-plane segmentation.



(a) (b)

Figure 1.16 (a) Schematic of the structure for simulation and (b) Simulation results.

1.7 Electromagnetic Bandgap (EBG) Structure

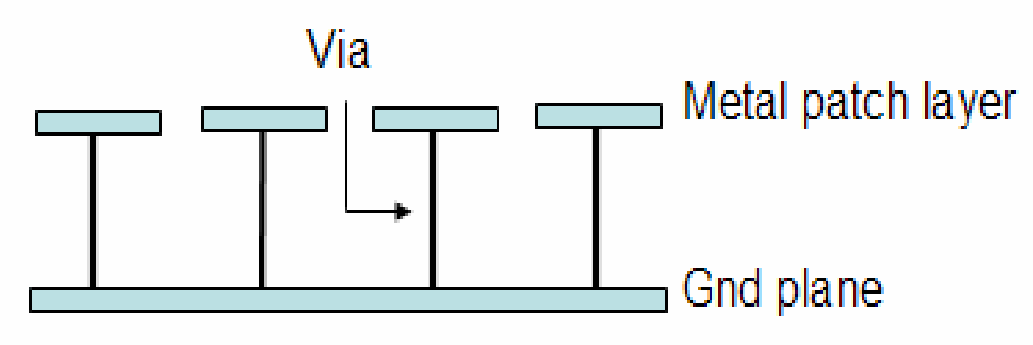
Electromagnetic bandgap (EBG) structures have become popular because of their ability for suppressing unwanted electromagnetic mode transmission and radiation in microwave and millimeter waves [15]-[17]. The EBG structures are periodic structures in which the propagation of electromagnetic waves is forbidden in certain frequency bands. In these EBG structures, the constructive and destructive interference of electromagnetic waves results in transmission and reflection bands [18]. The EBG structure has also been called a photonic bandgap (PBG) structure or a frequency selective surface (FSS). A common feature of periodic structures is the existence of frequency bands where electromagnetic waves are highly attenuated and do not propagate. Analogous to an electrical crystal where periodic atoms presents a bandgap prohibiting electron propagation, a photonic crystal is made of macroscopic dielectrics periodically placed (or embedded) within a surrounding medium. The periodic nature of the structure produces a photonic bandgap (PBG) within which photons (waves) are forbidden in a certain frequency range [18].

In 1987, a three-dimensional (3-D) periodic structure was realized by Yablonovitch [20] by mechanically drilling holes into a block of dielectric material. This structure prevents the propagation of microwave radiation in any three-dimensional (3-D) spatial direction, whereas the material is transparent in its solid form at these wavelengths. These artificially engineered structures are generically known as photonic bandgap (PBG) structures or photonic crystals. Although “photonic’ refers to light, the principle of “bandgap” applies to electromagnetic waves of all wavelengths. Consequently, there is controversy in the microwave community about the use of the

term “photonic” [21], and the term “electromagnetic bandgap (EBG) structure” or “electromagnetic crystal” is being proposed [22].

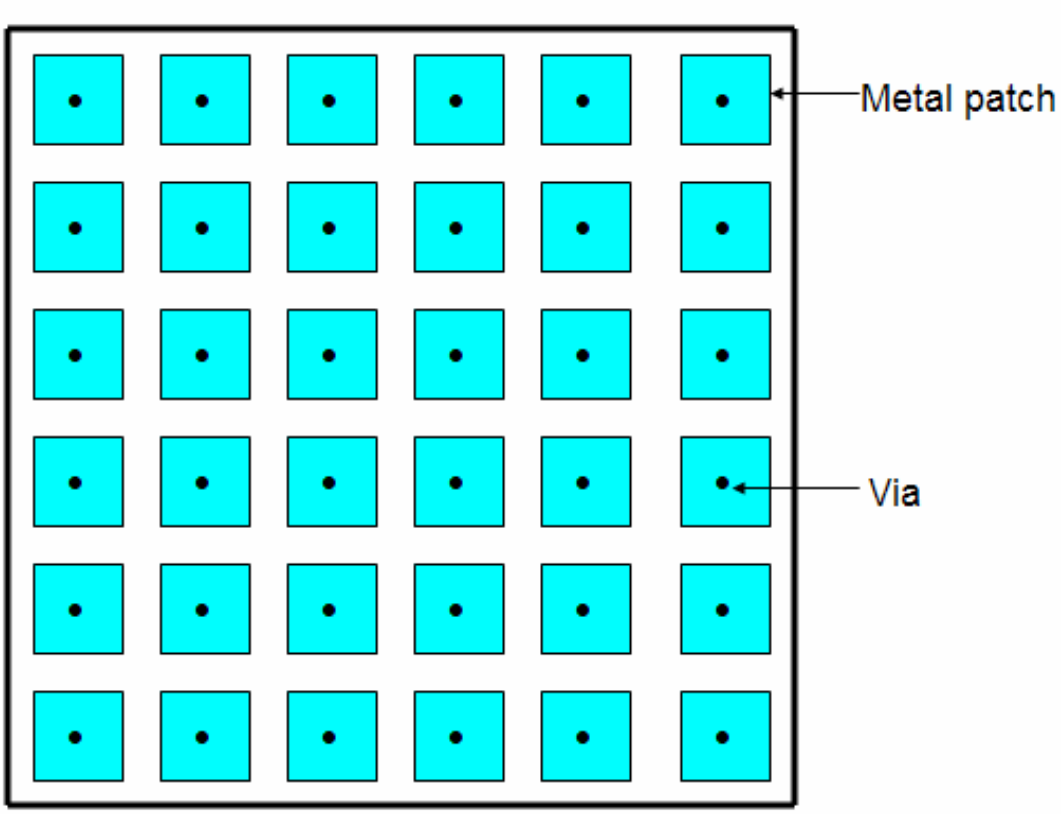
1.7.1 Mushroom-type EBG structure

The mushroom-type EBG structure was originally developed by D. Sievenpiper in 1999 for antenna applications [23]-[25]. Figure 1.17 shows the schematic of the mushroom-type EBG structure. By incorporating a special texture on a conducting surface, it is possible to alter its radio frequency electromagnetic properties [23], [24]. It has been proved that an antenna on a mushroom-type ground plane produces a smoother radiation profile than a similar antenna on a conventional metal ground plane, with less power wasted in the backward direction [23]. In this mushroom-type EBG structure, capacitance comes from the fringing electric field between adjacent metal patches and inductance comes from the currents in the ground plane and in the metal patch layer, as shown in Figure 1.18. Hence, the behavior of the structure can be described as a parallel resonant circuit in Figure 1.19.



(a)

Figure 1.17 (a) Cross-section of the mushroom-type EBG structure and (b) Top view of the mushroom-type EBG structure [29].



(b)

Figure 1.17 (a) Cross-section of the mushroom-type EBG structure and (b) Top view of the mushroom-type EBG structure [29].

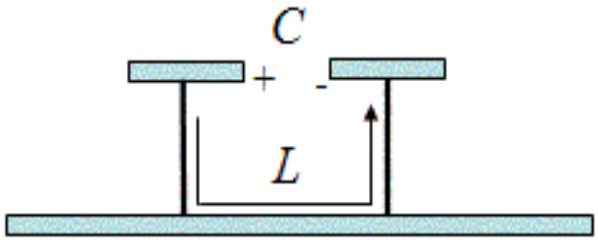


Figure 1.18 Origin of capacitance and inductance in mushroom-type EBG structure [29].

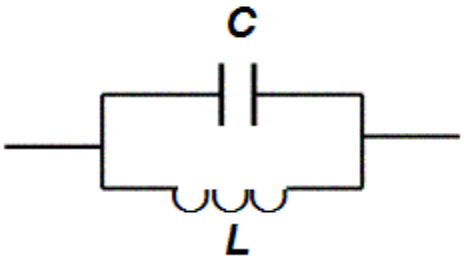


Figure 1.19 Parallel LC equivalent circuit for the structure in Figure 1.17 [29].

The fringing capacitance between adjacent metal patches can be derived using conformal mapping, a common method for solving two-dimensional electric field distributions [29]. The inductance in this structure can be derived easily from basic EM equations. Therefore, we have the following *C* and *L* equations for the structure in Figure 1.18.

$$C = \frac{w(\varepsilon_1 + \varepsilon_2)}{\pi} \cosh^{-1}\left(\frac{a}{g}\right) \tag{1.48}$$

$$L = \mu t \tag{1.49}$$

where w is the width of the metal patch, g is the gap distance, $a = 2w+g$, t is the via length, and μ is the permeability.

Figure 1.20 shows the above parameters with the mushroom-type EBG structure.

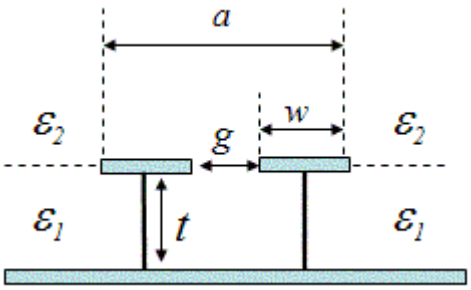


Figure 1.20 Geometrical parameters for the mushroom-type EBG structure [29].

For the mushroom-type EBG structure, the stopband center frequency, f_{center} [29], is given as

$$f_{center} = \frac{1}{2\pi\sqrt{LC}}, \tag{1.50}$$

where L is the sheet inductance of the mushroom-type EBG structure and C is the sheet capacitance of the mushroom-type EBG structure.

In the last few years, this mushroom-type EBG structure has been modified and applied for simultaneous switching noise (SSN) suppression in high-speed digital systems [26]-[28]. Figure 1.21 shows the cross-section of the modified mushroom-type EBG structure in high-speed digital systems. In this figure, the top metal layer is the Vdd plane and the bottom metal layer is the Gnd plane. In this modified mushroom-type EBG structure, blind vias are connected between the ground plane and metal patch layer, when applied to PDNs. The metal patch layer is placed in the dielectric layer that separates the power plane and ground plane. Since these modified mushroom-type EBG structures in [26]-[28] require an additional metal layer with blind via connections, it represents an expensive solution for printed circuit board (PCB) applications.

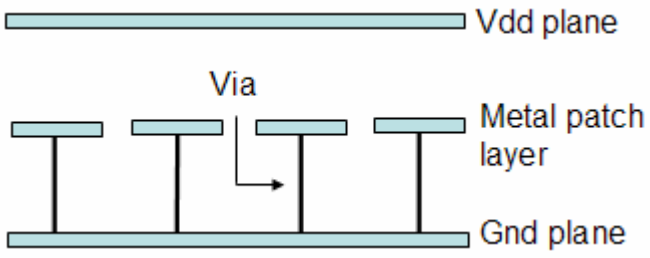


Figure 1.21 Cross-section of the modified mushroom-type EBG structure [26].

For the modified mushroom-type EBG structure in Figure 1.21, the stopband center frequency is given by [76]:

$$f_{center} = \frac{1}{2\pi\sqrt{L(C_1 + C_2)}}, \tag{1.51}$$

where L represents the inductance of the via, C_1 is the capacitance between the metal patch and the region of the top plate corresponding to such patch, and C_2 is the capacitance between the metal patch and the region of the bottom plate corresponding to

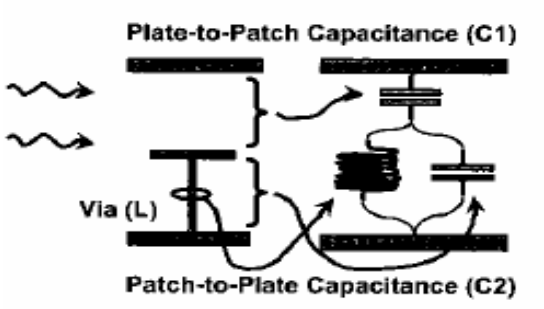


Figure 1.22 Model for the modified mushroom-type EBG structure [76].

the metal patch. These elements are shown in Figure 1.22. Figure 1.23 shows S-parameter simulation results for the modified mushroom-type EBG structure in Figure 1.21 when the via length (t) is varied from 1.54 mm to 4.62 mm [77]. In this structure, the total size of the structure was 10 cm x 10 cm and the size of the metal patch was 0.985 cm x 0.985 cm. The distance between the top metal plate and the metal patch layer was 1.54 mm and the gap between the metal patches was 0.15 mm. The dielectric constant was 4.4. In Figure 1.23, it is clear that isolation level in the stopband using the modified mushroom-type EBG structure ranges between -40 dB and -70 dB for all three cases. It is important to note that the stopband center frequency as well as the corner frequencies of

the stopband are shifted to lower frequencies when the via length (*t*) increases. This decrease of the stopband center frequency is associated with the increase in inductance, which is proportional to the via length [26].

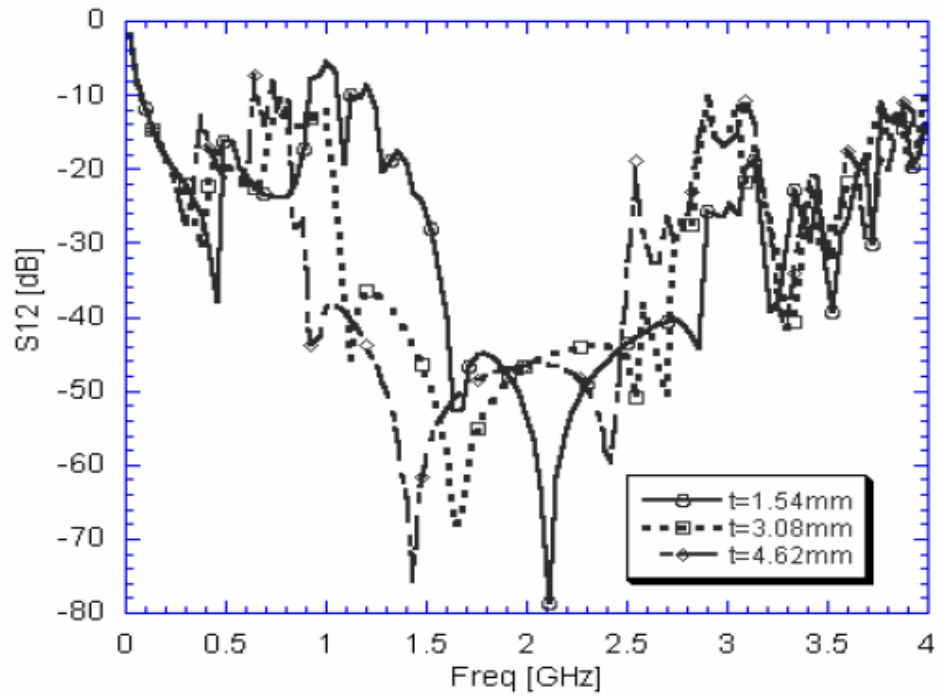
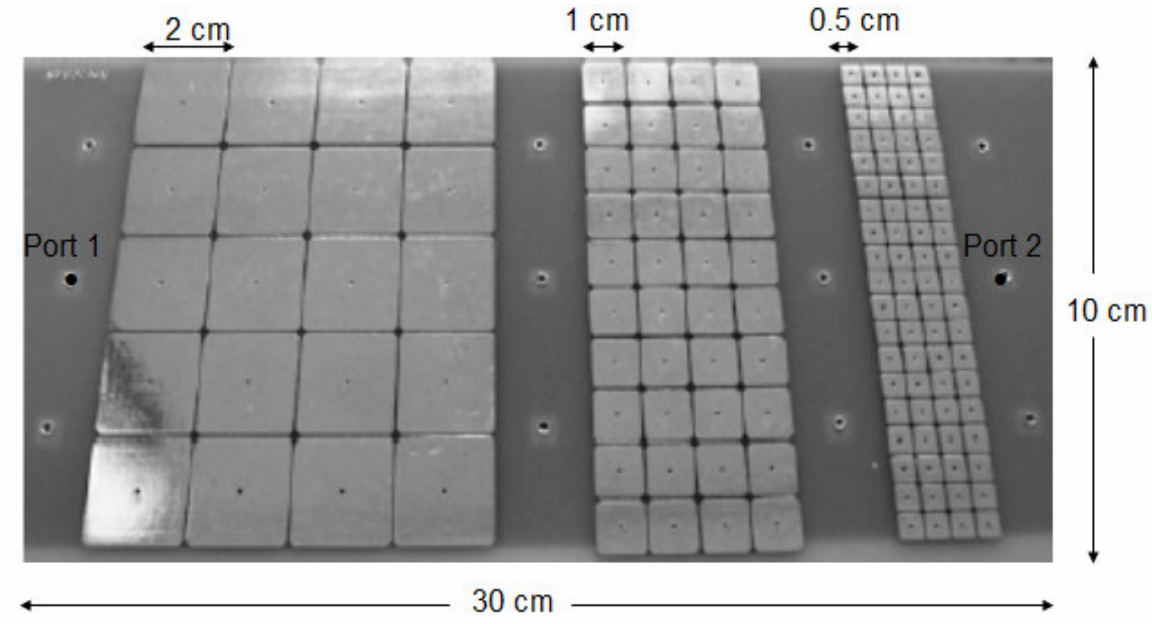


Figure 1.23 Effect of via length (t) on S-parameter for the modified mushroom-type EBG structure [77].

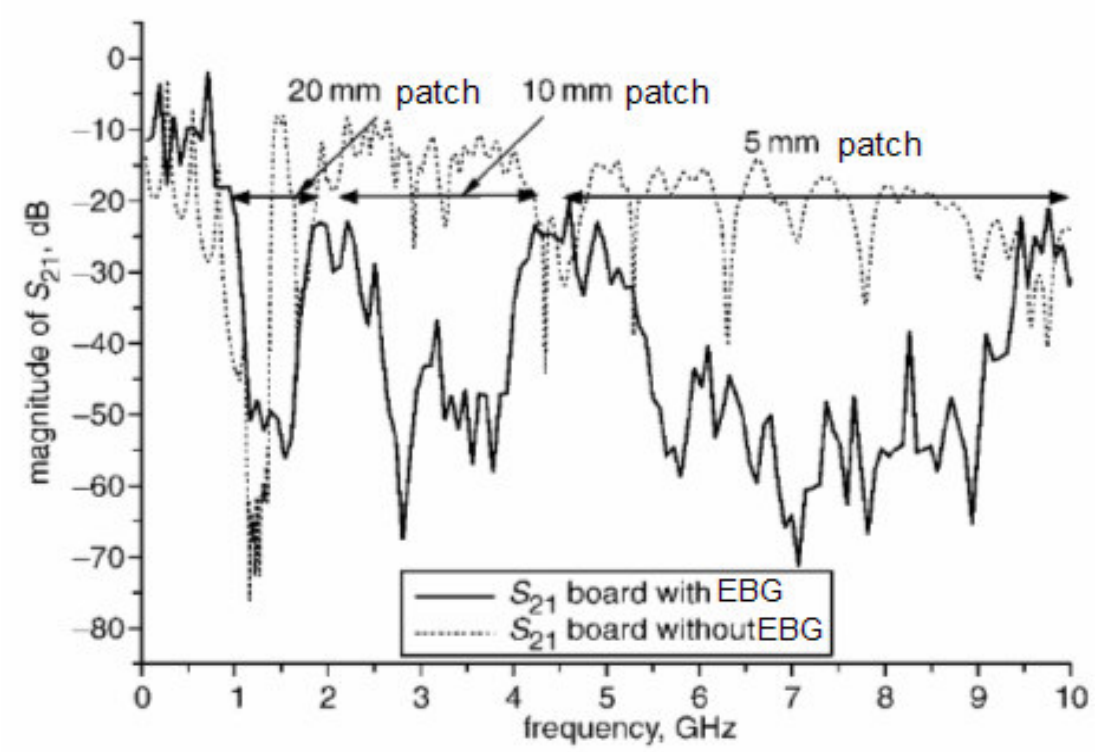
1.7.2 Mushroom-type EBG structure for Ultra Wide Band (UWB) applications

It is important to note the current status for ultra wide band (UWB) applications using the mushroom-type EBG structures. In this section, current status of the mushroom-type EBG structures for UWB applications is described.

In [57], a mushroom-type EBG structure was fabricated for UWB applications. The overall dimension of the PCB was 30 cm x 10 cm. The top view of the middle layer of the fabricated mushroom-type EBG structure is shown in Figure 1.24 (a). In this structure, sizes of metal patches were 2 cm x 2 cm, 1 cm x 1 cm, and 0.5 cm x 0.5 cm to obtain an ultra wide band stopband since different patch sizes produce different stopband frequency ranges. The dielectric material is FR4 with a relative permittivity $\varepsilon_r = 4.4$, and the conductor is copper with conductivity $\sigma_c = 5.8 \times 10^7$ S/m. Ports 1 and 2 are also shown in Figure 1.24 (a). Figure 1.24 (b) shows the measured transmission coefficient (S_{21}) for the structure in Figure 1.24 (a). The three stopbands are observed at 0.8 GHz-1.8 GHz, 2.2 GHz-4.2 GHz, and 4.5 GHz-10 GHz. It should be noted that isolation levels of the stopbands are between -50 dB and -60 dB and there are still resonance peaks in some frequency bands even though the total structure size is large. It is very difficult to make an ultra wide stopband using the mushroom-type EBG structure since the mushroom-type EBG behaves like a bandstop filter and therefore requires different patches for each 2 ~ 3 GHz stopband range. In Chapter 6, it will be shown that smaller hybrid AI-EBG structures produce a deeper and wider stopband than that of the mushroom-type EBG structures. In [58], isolation characteristics of the mushroom-type EBG structure were improved since two dielectric materials were used to disturb wave propagation. Figure 1.25 (a) shows the cross section of the fabricated mushroom-type EBG structure. A different material with high dielectric constant was employed for the space above the patches and the thickness of this material was made to be very thin. In Figure 1.25 (a), the following parameter values were used: $d = 5.4$ mm, $\nu = 0.8$ mm, h1 = 1540 μm, h2 = 16 μm. The dielectric constant of the dielectric material 1 was 4.5 and the dielectric constant

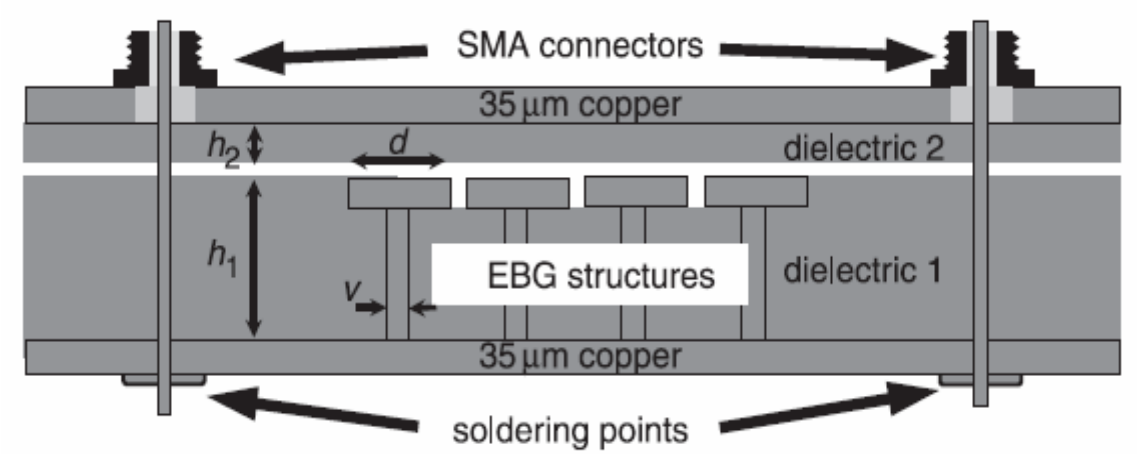


(a)

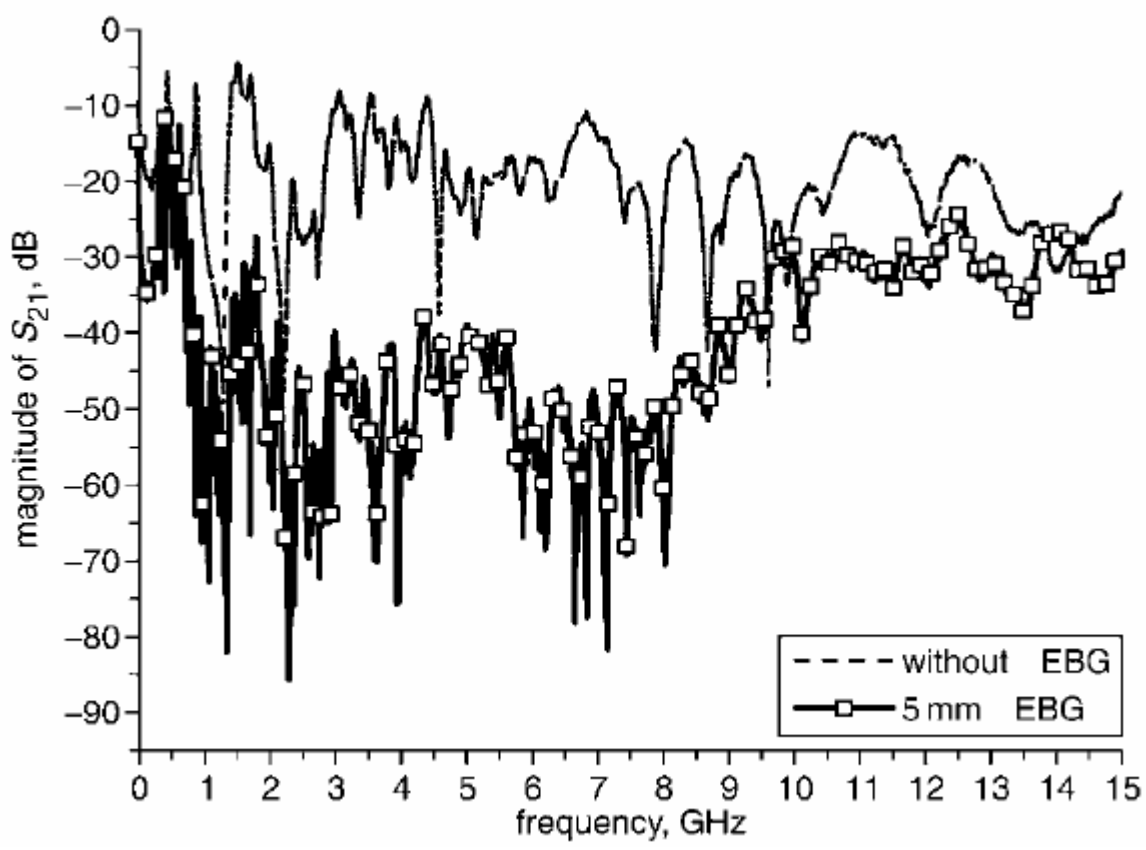


(b)

Figure 1.24 (a) Mushroom-type EBG structure for UWB applications and (b) Measured transmission coefficient (S_{21}) results [57].



(a)



(b)

Figure 1.25 (a) Cross section of the mushroom-type EBG structure with two dielectric materials and (b) Measured transmission coefficient (S_{21}) results [58].

of the dielectric material 2 was 30. This modification creates a non-symmetrical structure in which the patches are far closer to one of the parallel plates than the other. Figure 1.25 (b) shows the measured transmission coefficient (S_{21}) results for the mushroom-type EBG structure in Figure 1.25 (a). It is important that isolation levels of the stopbands are still between -50 dB and -60 dB and stopband range for -40 dB is around 6.5 GHz (i.e., from 2.2 GHz to 8.7 GHz). Moreover, this mushroom-type EBG structure requires two dielectric materials, which makes it more expensive than the previous mushroom-type EBG structure, which is not desired for printed circuit board (PCB) applications.

1.8 Proposed Research and Dissertation Outline

The objective of the proposed research is to develop an efficient method for noise suppression and isolation in mixed-signal systems that combine digital and RF electronics in a packaged module. This includes the design, modeling, analysis, fabrication, and characterization of a novel electromagnetic bandgap (EBG) structure called the alternating impedance EBG (AI-EBG) structure. The research also includes the integration of AI-EBG structures into power distribution networks (PDN) of mixed-signal systems for noise isolation and suppression.

The integration of wireless technologies in handsets and mobile computers is forcing the integration of high-speed digital circuits with analog and radio frequency (RF) circuits. When the output drivers or internal logic circuits of a microprocessor switch simultaneously, the power supply noise generated from the noisy digital circuits can deteriorate the performance of sensitive RF/analog circuits. Thus an efficient noise reduction scheme is required for isolating sensitive RF/analog circuits from noisy digital

circuits. Based on the issues in noise coupling in mixed-signal systems, the following research is proposed:

1. **Modeling and analysis of power distribution network in high-speed digital systems:** An efficient methodology has been developed for analyzing power distribution networks (PDN) in digital systems. This has been applied to a test vehicle from Rambus. This method has proved to be computationally efficient for computing power supply noise in high-speed digital systems. This work included the following:
    a. This methodology was applied to a test vehicle from Rambus consisting of a bidirectional 200 mV swing Differential Rambus Signaling Level (DRSL) with a data transfer rate of 3.2 Gbps/pair. First, the transmission matrix method (TMM) was applied to the PDN in the test vehicle to compute the frequency response. The results were correlated with measurement data using a vector network analyzer (VNA). Next, the macromodel representations of the plane pairs were generated at the desired ports using macromodeling.
    b. The coupling between split planes arising at high frequencies was studied in this work. This kind of coupling could result in detrimental effects to the system at high frequencies since split planes are supposed to serve as isolated islands.
    c. Power supply noise was computed efficiently in HSPICE. The macromodel of planes, differential driver model, and transmission lines

were co-simulated in HSPICE for computing power supply noise.

2. **Design and analysis of AI-EBG structure:** A novel electromagnetic bandgap (EBG) structure called the alternating impedance EBG (AI-EBG) structure was designed, modeled, and simulated for noise isolation/suppression in mixed-signal systems, which included the following:
    a. This EBG structure was optimized to produce excellent isolation level (-100 dB ~ -140 dB) using the transmission matrix method (TMM). The simulation results from TMM were verified using a full-wave solver (Sonnet^{TM}). This EBG structure produces the best isolation reported.
    b. The simulation methodology for the AI-EBG structure was proposed. Currently, full-wave solvers based on FEM or FDTD are used for simulating EBG structures. But these methods are computationally expensive and sometimes simulation is not possible due to large memory requirements. The AI-EBG structure was simulated to produce accurate results using TMM.
    c. The modeling and analysis of the novel EBG structure was discussed. Since this EBG structure consists of sections of high and low characteristic impedances, the EBG structure can be called as alternating impedance EBG (AI-EBG) structure. This EBG structure maximizes destructive wave interference in the stopband frequency range, which produces excellent isolation level in the bandgap frequency range.
3. **Model to hardware correlation of AI-EBG structure:** To verify the simulated results, AI-EBG structures were fabricated using standard PCB processes. The S-

parameter measurements were carried out using an Agilent 8720 ES vector network analyzer (VNA). The S-parameter measurement results showed excellent isolation for the EBG structure. The model to hardware correlation was also shown. Finally, the frequency tunability of the AI-EBG structure was shown through fabrication and measurement.

4. **Parametric analysis of AI-EBG structure:** The effect of critical parameters on bandgap frequency and isolation level in the AI-EBG structure were investigated by varying material and geometrical parameters through simulations. In addition to this, multi-layer effects of the AI-EBG structure were also studied. For this purpose, the liquid crystalline polymer (LCP) was chosen as a dielectric material. For comparison, three different cases were tested: a single plane pair, two plane pairs, and three plane pairs. The main purpose of this study was to see if it is possible to get better isolation from multi-layer structures with AI-EBG structure.
5. **Theoretical analysis of AI-EBG structure:** An efficient method to calculate the stopband center frequency of the AI-EBG structure was developed using the Brillouin zone concept. A dispersion analysis of the AI-EBG structure was computed by the transmission line network (TLN) method. In the TLN approach, a dispersion diagram was calculated using the unit cell in the AI-EBG structure. Due to the symmetry of the unit cell in the EBG structure, propagation through such a medium contains redundant propagation wave vectors. Hence, the unique vectors can be grouped in a region called the Brillouin Zone and the propagation characteristics of the AI-EBG structure can be obtained by analyzing the unit cell

(Brillouin Zone) in the AI-EBG structure. Finally, the cutoff frequency of the AI-EBG structure was investigated using the image parameter method.

6. **Noise suppression and isolation in mixed-signal systems containing the AI-EBG structure:** Mixed-signal systems were designed for supplying power to a Field Programmable Gate Array (FPGA) driving a 300 MHz bus with an integrated low noise amplifier (LNA) operating at 2.13 GHz. The mixed-signal system with and without the AI-EBG structure were designed, simulated, fabricated, and measured. The measured results were compared with simulation results, which included the following:
    a. The mixed-signal system simulations with and without the AI-EBG structure were performed in HP-ADS to see noise isolation levels available. The simulation results show that the proposed AI-EBG structure is a good candidate to suppress noise from digital circuits.
    b. The realistic mixed-signal system with and without the AI-EBG structure was designed and fabricated to see noise suppression effects due to AI-EBG structure. These mixed-signal test vehicles consist of an FPGA (driving a 300 MHz bus) and a Low Noise Amplifier (LNA) (operating at 2.13 GHz) which were fabricated on the FR4 based substrate. The board was a three metal layer PCB that measured 10.08 cm by 4.02 cm. The first metal layer was a signal layer, the second metal layer was a ground layer (Gnd), and the third metal layer is a power layer (Vdd). The AI-EBG structure was located in a ground layer in this test vehicle. The measurement results for the mixed-signal systems with and without the AI-

EBG structure proved that harmonic noise peaks due to digital circuits have been suppressed completely in the stopband frequency range using the AI-EBG structure.

7. **Signal integrity analysis:** The power delivery network needs to function along with the signal lines for high-speed transmission. Since the power and ground planes carry the return currents for the signal transmission lines, the impact of the EBG structures on signal transmission needs to be analyzed. Signal integrity analysis was performed by analyzing the characteristic impedance profile obtained from time domain reflectometry (TDR) measurements.
8. **Near and far field simulation and measurements:** The periodic gaps in the AI-EBG structure could create electromagnetic interference (EMI) problems if the AI-EBG plane is used as a reference plane. Hence, radiation analysis of the AI-EBG structure is important. For radiation analysis, three test vehicles were designed and fabricated for far field and near field measurements. Simulation results using a full wave solver (SONNET^{TM}) were compared with measurement results.
    a. Near field measurements were carried out using EMC Precision Scan (EPS-3000) equipment and NEC probe (CP-25) for the three test vehicles. The measurement results were compared with the simulation results using a full wave solver.
    b. Far field measurements were performed using an Anritsu MG3642A RF signal generator, an Agilent E4440A spectrum analyzer, and an antenna in an anechoic chamber. These measurement results were also compared with

the simulation results from a full wave solver.

9. **Design methodology in mixed-signal systems with the AI-EBG structure:** Through signal integrity, near and far field analyses, it is clear that design methodology is needed to avoid problems associated with signal integrity as well as EMI when the AI-EBG structure is employed in mixed-signal systems. Without a proper stack-up of planes in the mixed-signal system containing the AI-EBG structure, it is not possible to avoid problems associated with signal integrity as well as EMI. Hence, it is critical to develop the design methodology for avoiding these problems when the AI-EBG structure is used in a power distribution network. The best solution for avoiding the signal integrity and EMI problems is to use a solid plane as a reference plane, rather than the AI-EBG plane.
10. **Ultra wide band (UWB) applications of the AI-EBG structure:** Ultra wide band technology offers a solution for the bandwidth, cost, power consumption, and physical size requirements of next generation consumer electronic devices. In addition, UWB enables wireless connectivity with consistent high data rates across multiple devices and PCs within the digital home and office. UWB radios can use frequencies from 3.1 GHz to 10.6 GHz. In UWB technology, since the maximum signal power is limited to a very low level by Federal Communications Commission (FCC), any noise from digital circuits could destroy RF circuit performance. Hence, noise suppression is a major bottleneck for UWB technology. Various novel hybrid AI-EBG structures were designed, simulated, fabricated, and measured for UWB applications.

The remainder of this dissertation is organized as follows. Chapter 2 presents the modeling and analysis of power distribution network in high-speed digital system. In this chapter, an efficient methodology is suggested for analyzing power distribution networks (PDN) in digital systems. This methodology consists of the transmission matrix method (TMM) in the frequency domain and the macromodeling method in the time domain. It is shown that it is possible to compute power supply noise efficiently through this hybrid methodology. In addition, the coupling between two isolated planes, which is a detrimental effect to the system with a low voltage signaling in a high-speed digital system, is discussed. The design of the AI-EBG structure is discussed and a theoretical analysis of the AI-EBG structure is also shown in Chapter 3. In Chapter 4, the modeling, and analysis of a novel EBG structure called the alternating impedance electromagnetic bandgap (AI-EBG) structure are described. Chapter 5 shows noise suppression and isolation in the mixed-signal system with the AI-EBG structure as well as characterization of the AI-EBG structure. Novel hybrid AI-EBG structures for UWB applications are discussed in Chapter 6. The conclusions and future works are provided in Chapter 7.

CHAPTER 2

Modeling and Analysis of Power Distribution Network in High-Speed Digital Systems

Over the last decade, the scaling of the CMOS transistor has enabled the design of microprocessors operating at multi-gigahertz frequencies. This trend, based on the International Technology Roadmap for Semiconductors (ITRS), is expected to continue over many years for both desktop and mobile computers. Along with the scaling of the transistor, the number of transistors on a chip is doubling every 18 months, based on Moore's law. In addition, long-haul communication bandwidth is estimated to be doubling every nine months, much faster than Moore's law. This has resulted in the integration of short-range, low-power communication technologies such as IEEE 802.11, Bluetooth, and ultra wide band (UWB) into mobile computers. Integrating these technologies has increased the data processing requirements and computing capabilities in mobile devices.

A combination of voltage scaling and Moore's law is causing an alarming increase in the power consumed by microprocessors. Since computers are broadband systems, the current needs to be supplied to the switching circuits over a broad frequency range from DC to at least the fundamental clock frequency. This trend in microprocessors is causing a major challenge for distributing power in computer systems. With voltage

scaling and wireless integration in mobile computers, the tolerance to power supply noise is rapidly decreasing.

A major contribution to power supply noise is from the package and board level interconnections. Because of their distributed electrical characteristics, package and board interconnections can support electromagnetic waves in the power distribution network. These electromagnetic waves cause detrimental effects to the switching circuits, such as excessive power supply noise and coupling. To minimize such noise behavior, pre-layout analysis and post-layout verification of the power distribution network are necessary.

One of the most important areas in high-speed digital systems is the design and analysis of the power distribution network. The power distribution network supplies power to core logic and I/O circuits in any digital system. As clock speeds increase, and signal rise time and supply voltages decrease, the transient currents injected into the power distribution planes can induce voltage fluctuations on the power distribution network [1]. This undesired voltage fluctuation on the power/ground planes is commonly known as switching noise or delta-I noise. Power supply noise leads to unwanted effects on the power distribution network (PDN) such as ground bounce, false triggering in digital circuits, and waveform distortion in the time domain. It has been shown that power supply noise induced by a large number of simultaneously switching circuits in a printed circuit board (PCB) or multichip module (MCM) can limit the performance of the system [31]. Therefore, the power distribution network should be designed to have a low impedance over the entire bandwidth of the signal so that the transient currents do not cause excess voltage noise on the power distribution network [32]. However, the design

of the PDN to achieve this goal is difficult since modern CMOS microprocessors or application-specific integrated circuits (ASICs) have thousands of drivers that switch simultaneously within a clock cycle. With the trend toward low-voltage and low-power signaling in mobile computers, the power supply noise can be a major bottleneck for the reliable functioning of the system.

For meeting the high bandwidth demands and low-power requirements, digital technologies are quickly moving to gigabit data rate and subvoltage range signaling levels. To meet these requirements, Rambus has introduced the Yellowstone signaling technology utilizing a bidirectional 200 mV swing Differential Rambus Signaling Level (DRSL) with a data transfer rate starting at 3.2 Gbps/pair and scalable to 6.4 Gbps/pair [33]. These very high-operating frequencies and low-voltage swing place increasing demands on the quality of the power distribution network. Therefore, accurate analysis of the PDN has become critical for optimizing the performance of high-speed systems.

In the past, various numerical methods have been developed to analyze power distribution networks. Examples include Speed from Sigrity [34], [35], which is based on a finite difference time domain (FDTD) method, the transmission line method [36], [37], which uses a two-dimensional array of transmission lines or distributed RLCG elements in SPICE, the cavity resonator method [38], [39], the transmission matrix method (TMM) [40]-[42], and a circuit extraction approach based on the mixed-potential integral equation formulation (CEMPIE) method which is an extension of the partial-element equivalent circuit approach [43]. It has been shown in [40] that the transmission matrix method is efficient for analyzing electrically large power/ground planes of irregular shape. Though TMM computes the frequency response of power/ground planes, the

results have to be combined with transmission lines and nonlinear drivers for computing the power supply noise.

In this chapter, a hybrid method that combines the transmission matrix method (TMM) and macromodeling method has been applied to the Rambus board for computing power supply noise. The output of this analysis is a methodology that is useful for analyzing the PDN in digital systems such as mobile computers, which is the primary contribution of this chapter. Even though the method presented has been applied for post-layout verification, the method also lends itself to pre-layout analysis. Here, the methods can be used to estimate the layer stack-up, layer assignment, decoupling strategies, power islands, etc. for meeting the power supply noise budget.

2.1 Efficient hybrid methodology for analyzing PDN

The computation of power supply noise requires the simulation of nonlinear drivers in the presence of non-ideal supply voltages. The voltages to the nonlinear drivers are supplied through the PDN from the voltage regulator modules on the PCB. The PDN typically contains power/ground planes and decoupling capacitors attached together using numerous vias for high-frequency applications. The PDN is best analyzed and designed in the frequency domain [42]. However, the power supply noise is a transient phenomenon that needs to be computed in the time domain. The power supply noise is affected by the nonlinearity of the drivers. Hence, for understanding the impact of power supply noise on system performance, a hybrid method is required whereby nonlinear drivers can be simulated in the time domain with the frequency response of the PDNs.

Recently, a hybrid method for analyzing the PDN was proposed in [44]. This methodology preserves the accuracy of field simulators and concurrently improves the computational efficiency for the analysis of the entire system. First, the frequency response, such as impedance, is computed using the transmission matrix method. Then, a black box representation of the PDN is generated at the desired ports using macromodeling. The macromodel can be synthesized into SPICE net-lists and combined with drivers for enabling nonlinear circuit simulation. Finally, the macromodel of the PDN, nonlinear drivers, and transmission lines are simulated in conventional circuit simulators like SPICE. This methodology is shown in Figure 2.1. This section describes the details of this methodology for analyzing PDNs in complex systems.

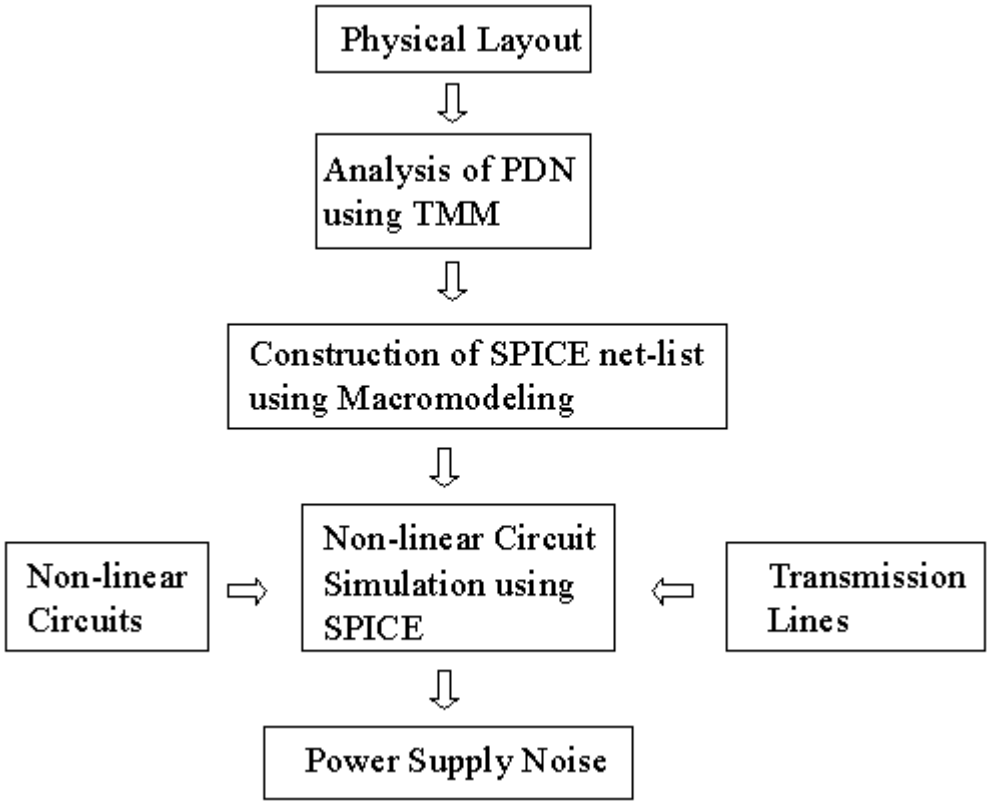


Figure 2.1 Modeling and simulation methodology for PDN.

The transmission matrix method offers an efficient technique for analyzing realistic power distribution networks [40]-[42]. Using the property that power distribution networks in the package and board can be represented as a cascade of unit cells consisting of distributed and repeated RLCG circuit elements, the multi-input/multi-output transmission matrix method can be used to simulate arbitrarily shaped, electrically large structures efficiently. Since the transmission matrix method is based on a multi-input/multi-output transfer function, the response of the PDN at specific ports can be computed by multiplying the individual square matrices. Once the matrix of the overall network is computed, it can be converted into a scattering matrix (S), an admittance matrix (Y), or an impedance matrix (Z) at specific points on the network. Therefore, while retaining the same size of the matrix for the overall network, the transmission matrix method provides the flexibility for analyzing large networks containing up to 20 power/ground plane pairs with relative ease. The salient features of the method are that it requires small memory and the CPU time scales linearly as the number of power/ground planes is increased. The transmission matrix method has been used in this section for computing the frequency response of the PDN.

The distributed behavior of interconnects at either the chip or package level can be extracted in the frequency domain from an electromagnetic simulation or from measurements. The response of the structure is available as frequency-dependent data that represents the scattering (S), admittance (Y), or impedance (Z) parameters. This information can be represented as a black box, which can be used to capture the behavior of the structure at the input/output ports. This black box representation of passive circuits can be modeled using macromodels based on rational functions. The macromodels can be

combined with a larger circuit by synthesizing SPICE net-lists for time domain simulation.

2.2 Transmission matrix method (TMM)

Power/ground planes represent large metal layers separated by a small dielectric distance, as shown in Figure 2.2. Because of the small dielectric distance, power/ground planes in the package and PCB are capacitive at low frequencies and are therefore ideal for supplying power to the integrated circuits. However, with an increase in frequency, planes become inductive and resonate at discrete frequencies [1]. Integrated circuits that trigger these resonances can result in large voltage variations on the PDNs. Hence, power/ground planes need to be carefully analyzed based on the frequency response. Since power/ground planes are electrically large structures, their analysis is nontrivial.

The transmission matrix method was first proposed by Dr. Joong-Ho Kim at Georgia Tech [67]. Power/ground planes can be divided into unit cells, as shown in Figure 2.2, and represented using a lumped element model for each cell, as described in [45]. The lumped element model parameters are computed from the physical structure. Each cell consists of an equivalent circuit with R, L, C, and G components, as shown in Figure 2.2 for a rectangular structure. Each unit cell can be represented using either a T or Π model [46], [47] as shown in the figure. Both models lead to similar results as discussed in [40]. The equivalent circuit parameters for a unit cell can be derived from quasi-static models, provided the dielectric separation (d) is much less than the metal dimensions (a, b) [48], which is true for power/ground plane pairs. From the lateral dimension of a unit cell (w), separation between planes (d), dielectric constant (ε), loss

tangent of dielectric ($tan(\delta)$),metal thickness (t), and metal conductivity (σ_c), the equivalent circuit parameters of a unit cell can be computed as:

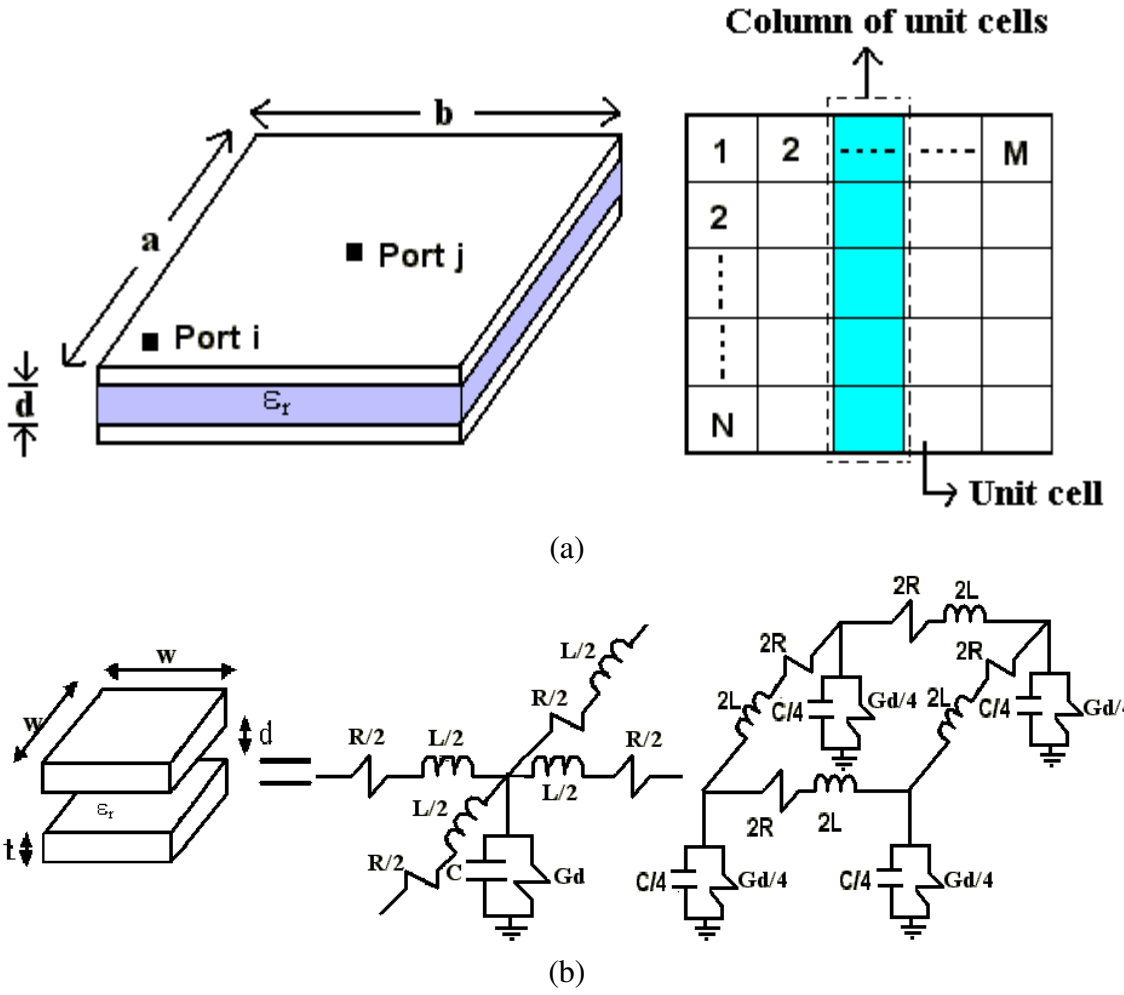


Figure 2.2 (a) Plane pair structure and (b) Unit cell and equivalent circuit (T and Π models).

$$C=\varepsilon_o\varepsilon_r\frac{w^2}{d},\quad L=\mu_o d,\quad R_{DC}=\frac{2}{\sigma_c t},\quad R_{AC}=2\sqrt{\frac{\pi f\mu_o}{\sigma_c}}(1+j),\quad G_d=\omega C\tan(\delta). \tag{2.1}$$

where ε_o is the permittivity of free space, μ_o is the permeability of free space, and ε_r is the relative permittivity of the dielectric. The parameter R_{DC} is the resistance of both the

power and ground planes for a steady DC current, where the planes are assumed to be of uniform cross-section. The AC resistance R_{AC} accounts for the skin effect on both conductors. The shunt conductance G_d represents the dielectric loss in the material between the planes.

By approximating the unit cell, a distributed network of RLCG elements can be generated for rectangular planes, as shown in Figure 2.2. Using a distributed network of RLCG elements, each rectangular plane pair can be divided into $(M-1)\times(N-1)$ unit cells. The $(M-1)\times(N-1)$ unit cells can be represented as a $2(M\times N)\times 2(M\times N)$ matrix formed by $(M\times N)$ input ports and $(M\times N)$ output ports. This is shown in Figure 2.3 for the Π equivalent circuit for the unit cells, which are cascaded to represent a pair of power/ground planes shown in Figure 2.2.

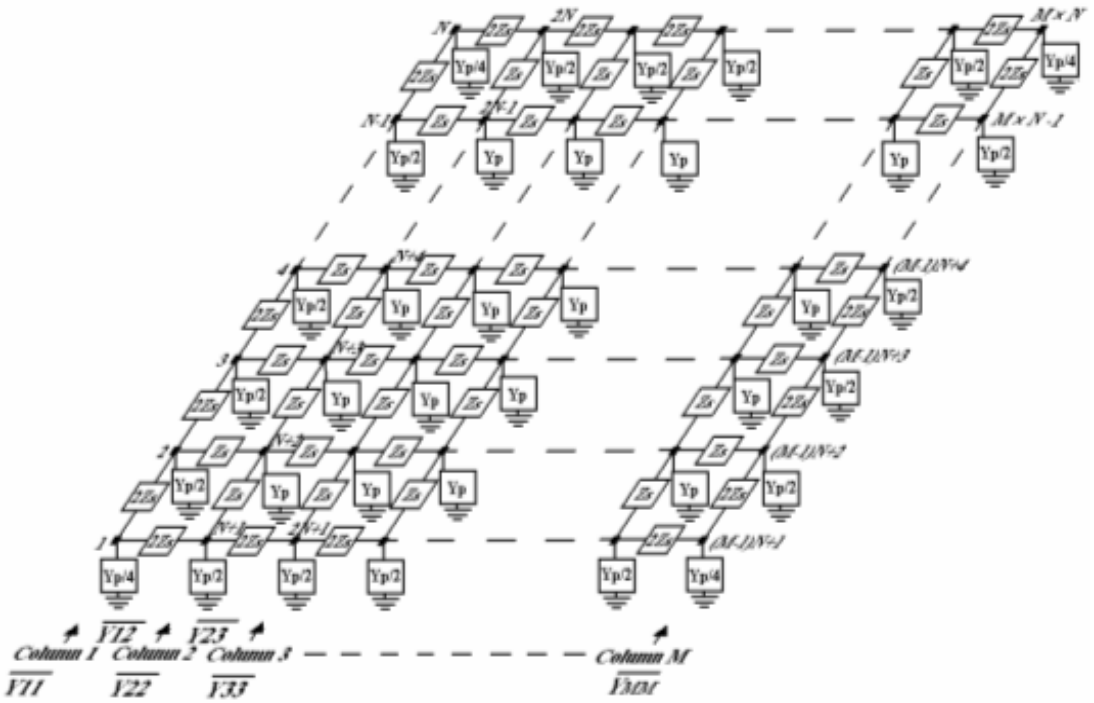


Figure 2.3 Equivalent circuit for a pair of power/ground planes.

From Figure 2.3, the input ports are indexed as 1 to $(M \times N)$, and the output ports are indexed as $(M \times N)+1$ to $2(M \times N)$. The transmission matrix for the $2(M \times N)$ port network can be derived in terms of the node voltages and port currents. Using the 2×2 block matrix representation, the transmission matrix can be represented to relate the voltages and currents as

$$\begin{aligned} \overline{V_{in}} &= [A_p]\overline{V_{out}} + [B_p]\overline{I_{out}} \\ \overline{I_{in}} &= [C_p]\overline{V_{out}} + [D_p]\overline{I_{out}} \end{aligned} \tag{2.2}$$

$$\text{where } \overline{V_{in}} = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_{M\times N} \end{bmatrix} \overline{I_{in}} = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{M\times N} \end{bmatrix} \overline{V_{out}} = \begin{bmatrix} V_{M\times N+1} \\ V_{M\times N+2} \\ \vdots \\ V_{2(M\times N)} \end{bmatrix} \overline{I_{out}} = \begin{bmatrix} I_{M\times N+1} \\ I_{M\times N+2} \\ \vdots \\ I_{2(M\times N)} \end{bmatrix}.$$

The above transmission matrix for a power/ground plane pair can be rewritten in the simpler form:

$$T_p = \begin{bmatrix} A_p & B_p \\ C_p & D_p \end{bmatrix} = \begin{bmatrix} I & 0 \\ C_p & I \end{bmatrix} \tag{2.3}$$

where $[I]$ is the identity matrix, $[0]$ is the null matrix, and $[C_p]$ represents $(M \times N)\times(M \times N)$ matrices. In equation (3.3), the matrix $[C_p]$ is of the form

$$[C_p] = \begin{bmatrix} \overline{Y}_{11} & -\overline{Y}_{12} & 0 & 0 & \cdots \\ -\overline{Y}_{12} & \overline{Y}_{22} & -\overline{Y}_{23} & 0 & \cdots \\ 0 & -\overline{Y}_{23} & \overline{Y}_{33} & -\overline{Y}_{34} & \cdots \\ \vdots & \vdots & \vdots & \vdots & \cdots \\ 0 & 0 & 0 & 0 & \cdots \; \overline{Y}_{MM} \end{bmatrix} \tag{2.4}$$

where $\overline{Y}_{11} = \overline{Y}_{MM} = 0.5\overline{Y}_{22} = 0.5\overline{Y}_{33} = \cdots\cdots = 0.5\overline{Y}_{(M-1)(M-1)} =$

$$\begin{bmatrix} \frac{Y_p}{4}+\frac{1}{Z_s} & -\frac{1}{2Z_s} & 0 & \cdots & 0 & 0 \\ -\frac{1}{2Z_s} & \frac{Y_p}{2}+\frac{2}{Z_s} & -\frac{1}{2Z_s} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \ddots & \vdots \\ 0 & 0 & \cdots & \ddots & \frac{Y_p}{2}+\frac{2}{Z_s} & -\frac{1}{2Z_s} \\ 0 & 0 & \cdots & & -\frac{1}{2Z_s} & \frac{Y_p}{4}+\frac{1}{Z_s} \end{bmatrix}$$

$$\overline{Y_{12}} = \overline{Y_{23}} = \cdots\cdots = \overline{Y_{(M-1)M}} =$$

$$\begin{bmatrix} \frac{1}{2Z_s} & & & & 0 \\ & \frac{1}{Z_s} & & & \\ & & \ddots & & \\ & & & \frac{1}{Z_s} & \\ 0 & & & & \frac{1}{2Z_s} \end{bmatrix}.$$

As can be seen in equation (2.4), the transmission matrix for a power/ground pair is tri-diagonal and sparse, which enables a reduction in memory usage and CPU run time when this method is applied to realistic structures [42].

The matrix computation in equations (2.2), (2.3), and (2.4) can be further reduced to compute the frequency response at specific ports in the network [42]. For irregular structures, the structure can be approximated using a rectangular array of unit cells where the nonmetallic areas are padded with zero matrix elements [40].

2.3 Rambus test vehicle

This section describes the test vehicle used for PDN analysis and for computing power supply noise. The Yellowstone test vehicle from Rambus consists of transmitter and receiver chips wirebonded onto plastic ball grid array (PBGA) packages on a PCB. The PBGA packages are directly attached to the board using solder balls or using sockets. This test vehicle is shown in Figure 2.4. The board is a six layer PCB that is 12.8 inches by 9.5 inches in size, as shown in Figure 2.5. In this figure, the PCB consists of two voltage planes, two ground planes, and two signal lines.

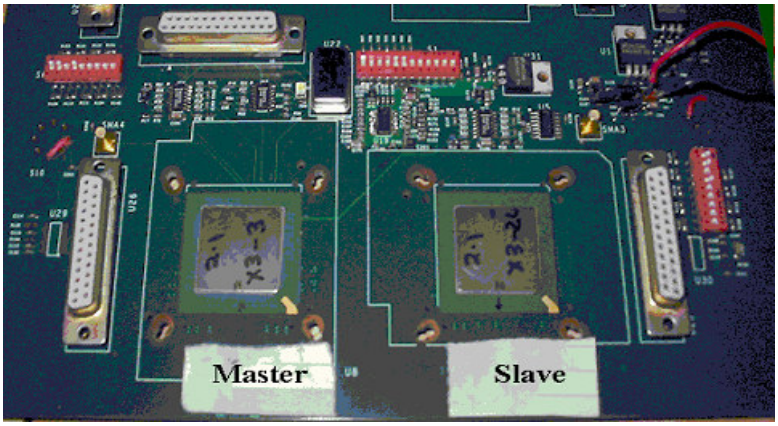


Figure 2.4 Test vehicle from Rambus.

Layer 3 is a voltage plane that provides 5 V to the peripherals on the board. It also has two irregular-shaped power islands of 1.2 V, master and slave sections, to supply voltage to the transmitter and receiver chips on the board, respectively, as shown in Figure 2.6. Layer 4 is a 1.2 V split plane, which serves the master and slave sections and includes a small island at the center with 3.3 V to supply voltage to the clock generation chip, as shown in Figure 2.6. The purpose of the split plane is to monitor

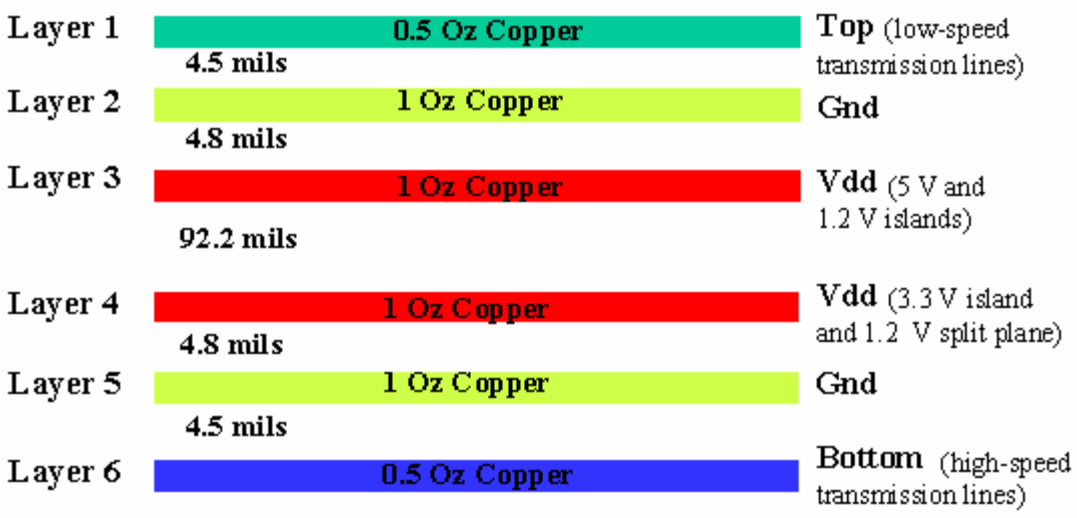


Figure 2.5 Cross-section of the PCB.

the power drawn by each subsystem. These two split planes are connected using a jumper. Layers 2 and 5 are solid ground planes. Layer 1 and layer 6 are signal layers for low- and high-speed interconnects, respectively, as shown in Figure 2.6. The low-speed signal transmission lines are single ended and their characteristic impedances are designed for 50 Ω using a trace width of 7 mils and 18 mil spacing. The high-speed signal nets are differential and are designed with a 6 mil width and 11.5 mil spacing. The differential traces have been designed to provide a 100 Ω differential impedance. The signal trace thickness on layer 1 and layer 6 is 0.7 mils. There are three ferrite beads on the board. All the ferrite beads are attached on the top surface next to the voltage regulators. One ferrite bead has been used for each supply voltage (i.e., 1.2 V, 3.3 V, and 5 V). The purpose of the ferrite bead is to isolate the power planes from any power supply noise. For example, the ferrite bead is placed on the 1.2 V external supply in layer 1 to ensure that the 1.2 V supply that is being fed to the two islands is clean and free of

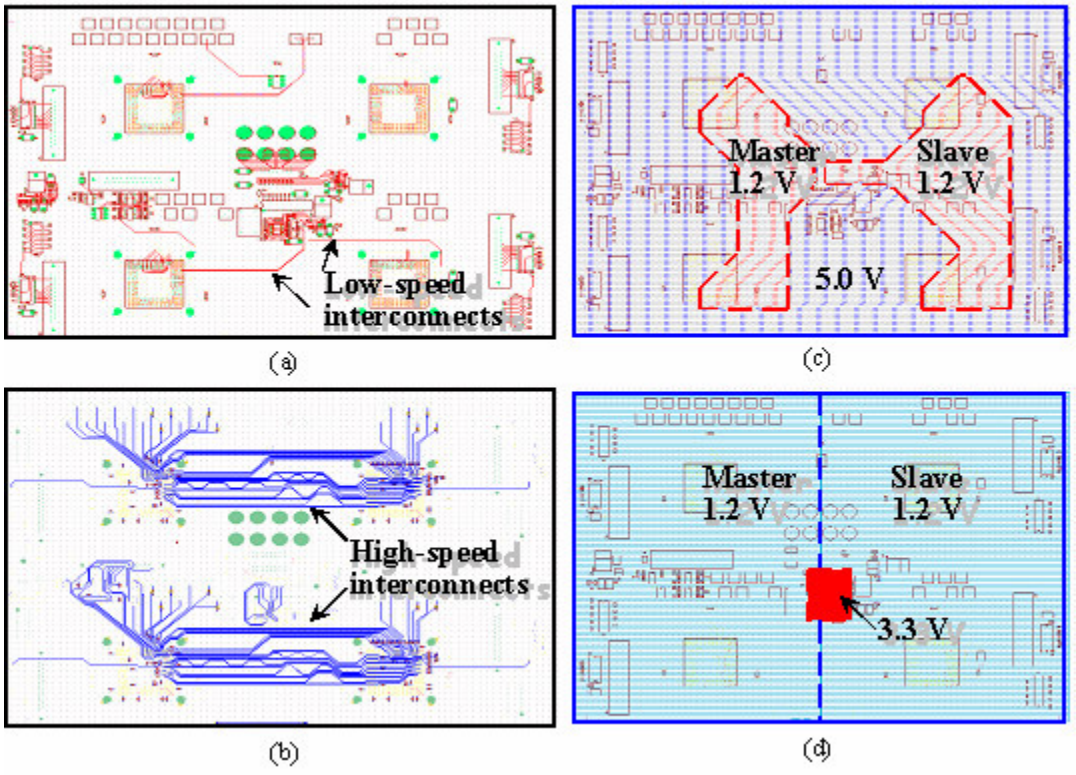


Figure 2.6 Power and signal plane layers of the PCB (a) Layer 1: signal layer for low-speed signal transmission lines, (b) Layer 6: signal layer for high-speed signal transmission lines, (c) Layer 3: power layer (5 V and 1.2 V master and slave islands), and (d) Layer 4: power layer (1.2 V split plane and 3.3 V island).

any power supply noise from other sources. After the ferrite bead, the 1.2 V is split into the master and slave supply in layer 3 through vias [49]. The dielectric material of the PCB is FR4 with a relative permittivity, ε_r = 4.5, the conductor is copper with conductivity, σ_c = 5.8 x 10^7 S/m, and dielectric loss tangent, $tan\,(\delta)$ = 0.02 at 1 GHz. The copper thickness for layer 1 and layer 6 is 0.75 mils and the copper thickness for other layers is 1.5 mils.

To check the accuracy of the transmission matrix method, the frequency response of the plane pair consisting of layers 4 and 5 was analyzed. The physical layout of layer 4 is shown in Figure 2.7, which consists of two planes separated around the mid-section. In

the test vehicle, layers 4 and 5 contained decoupling capacitors that could either be soldered or removed. Hence, the frequency response of the plane pair could be measured with and without decoupling capacitors. For all cases, the frequency response was measured at locations C238 (x = 2712.5 mils, y = 5687.5 mils) and C217 (x = 2712.5 mils, y = 687.5 mils) on the master section, as shown in Figure 2.7. These locations represented decoupling capacitor locations where pads were available for probing the power/ground plane.

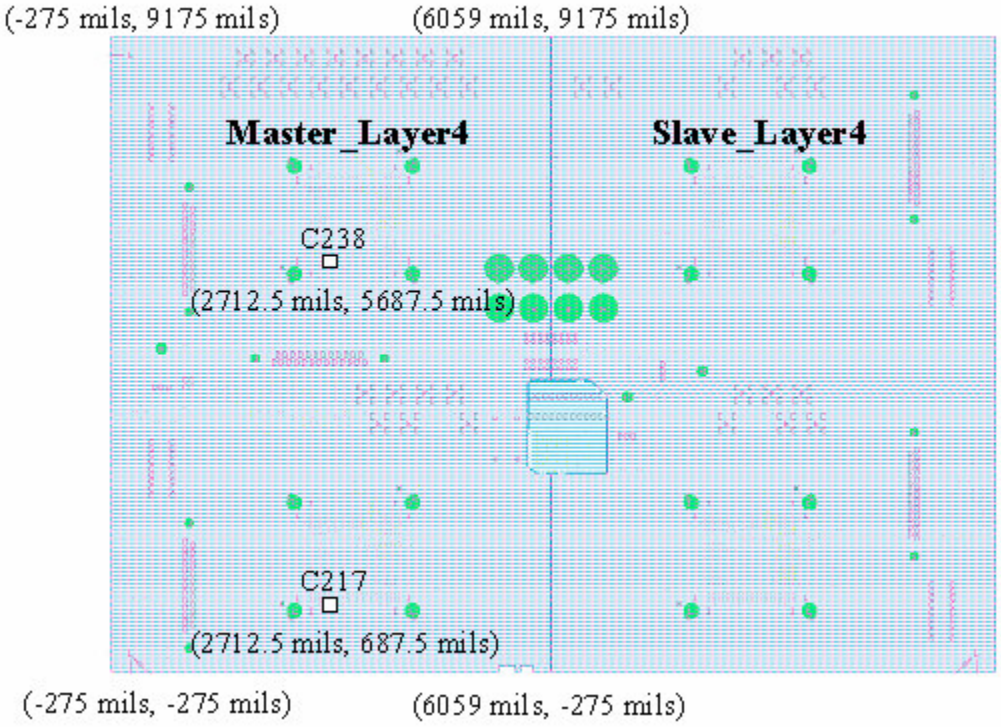
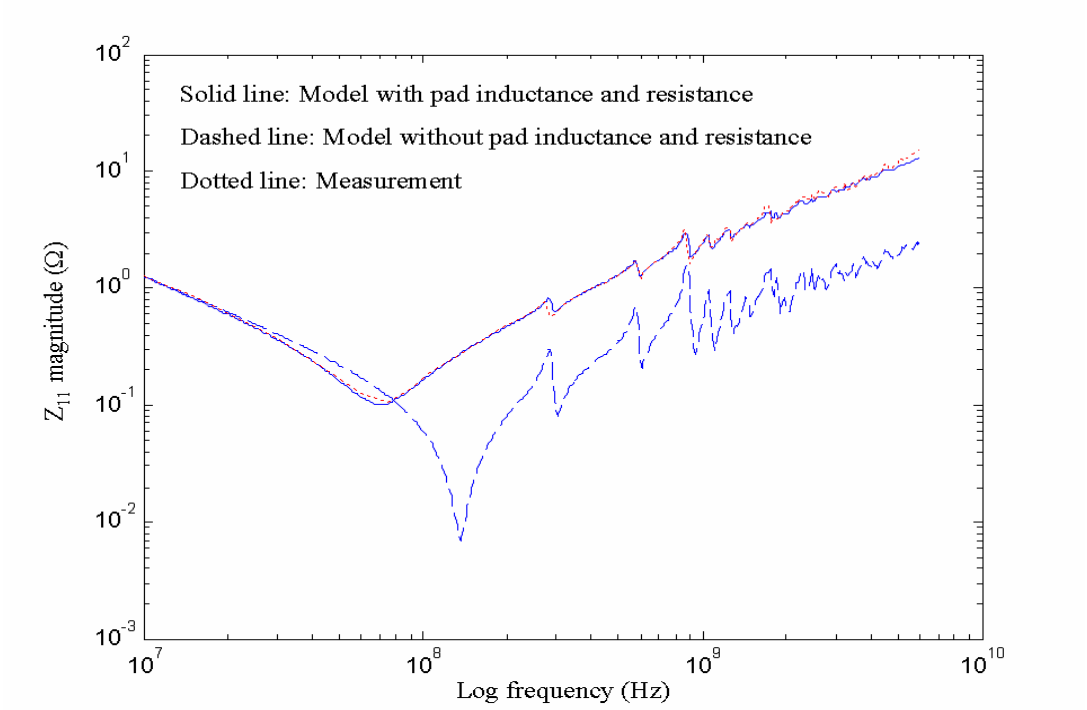
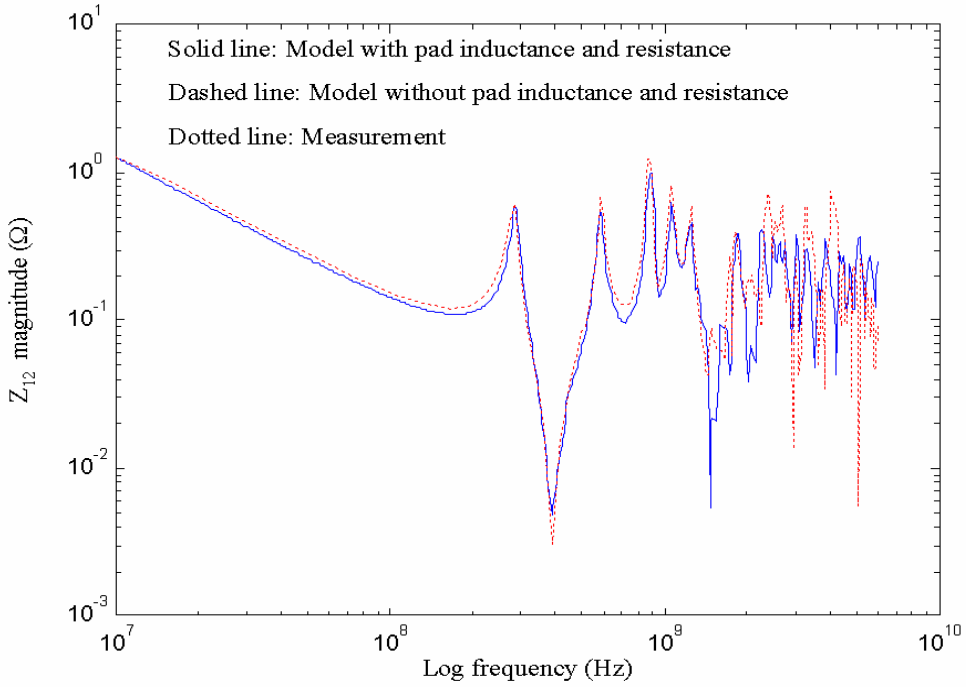


Figure 2.7 Locations of C217 and C238 sites on layer 4.

The transmission matrix method was used to calculate self-impedances at ports C238 and C217, and transfer impedance between ports C288 and C217. The planes were approximated as rectangular planes without any loss in accuracy. To verify the accuracy

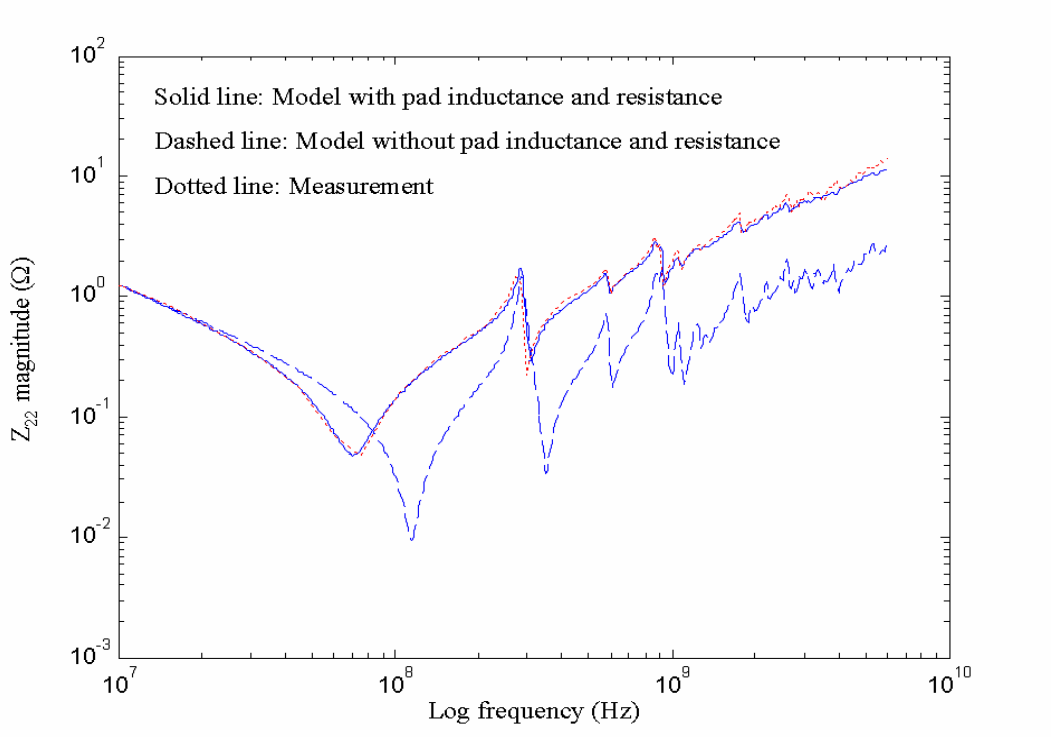


(a)



(b)

Figure 2.8 Model-to-hardware correlation with and without pad parasitics (a) Self-impedance at port C238, (b) Transfer impedance between port C238 and port C217, and (c) Self-impedance at port C217.



(c)

Figure 2.8 Model-to-hardware correlation with and without pad parasitics (a) Self-impedance at port C238, (b) Transfer impedance between port C238 and port C217, and (c) Self-impedance at port C217.

of the transmission matrix method, various measurements using a vector network analyzer (VNA) were performed. The model-to-hardware correlation results for the bare board (no decoupling capacitors) are shown in Figure 2.8 from 10 MHz to 6 GHz. From the figure, transfer impedance Z_{12} (dashed line) shows good model-to-hardware correlation. However, self-impedances Z_{11} (dashed line) and Z_{22} (dashed line) have a large discrepancy between modeling and measurement. This is due to the pad inductance and resistance, which were not included in the initial model.

The importance of the pad inductance and resistance on the frequency response of power/ground planes can be explained using Figure 2.9. In this figure, the frequency response of the plane pair is represented as a black box. The resistance and inductance at

the input and output ports are due to pads that are added in series to the power/ground planes. Hence, in Figure 2.9, the relationship between the measured voltages and currents can be written as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} + R_1 + j\omega L_1 & Z_{12} \\ Z_{21} & Z_{22} + R_2 + j\omega L_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \qquad (2.5)$$

In (2.5), the pad parasitics only affect the self-impedance, but not the transfer impedance of the power/ground planes. Hence, it is important to note that self-impedances are sensitive and require accurate calibration. Consequently, transfer impedance measurements are more reliable.

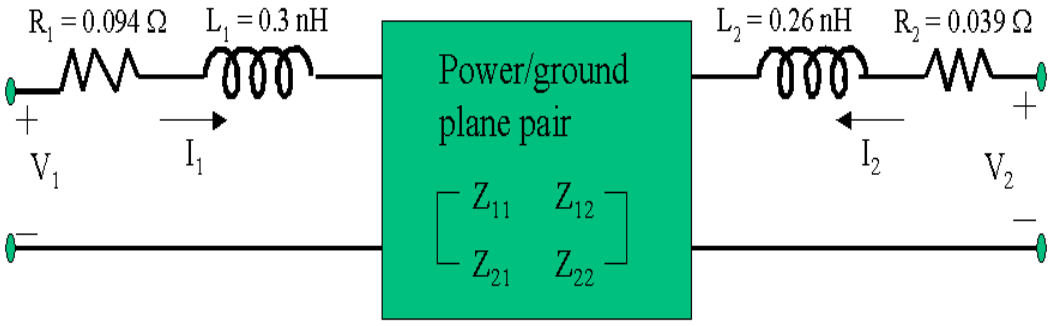


Figure 2.9 Modified equivalent network of the power/ground planes.

Since the transmission matrix method is a circuit-based formulation, the pad parasitics can be added to the model with ease. With the pad parasitics added, the modeling results for self-impedances (Z_{11}; solid line) at port C238 and port C217 and transfer impedance (Z_{12}; solid line) between port C238 and port C217 were compared with measurement results (dotted lines) between 10 MHz and 6 GHz in Figure 2.8. These results show very good correlation between modeling and measurement results.

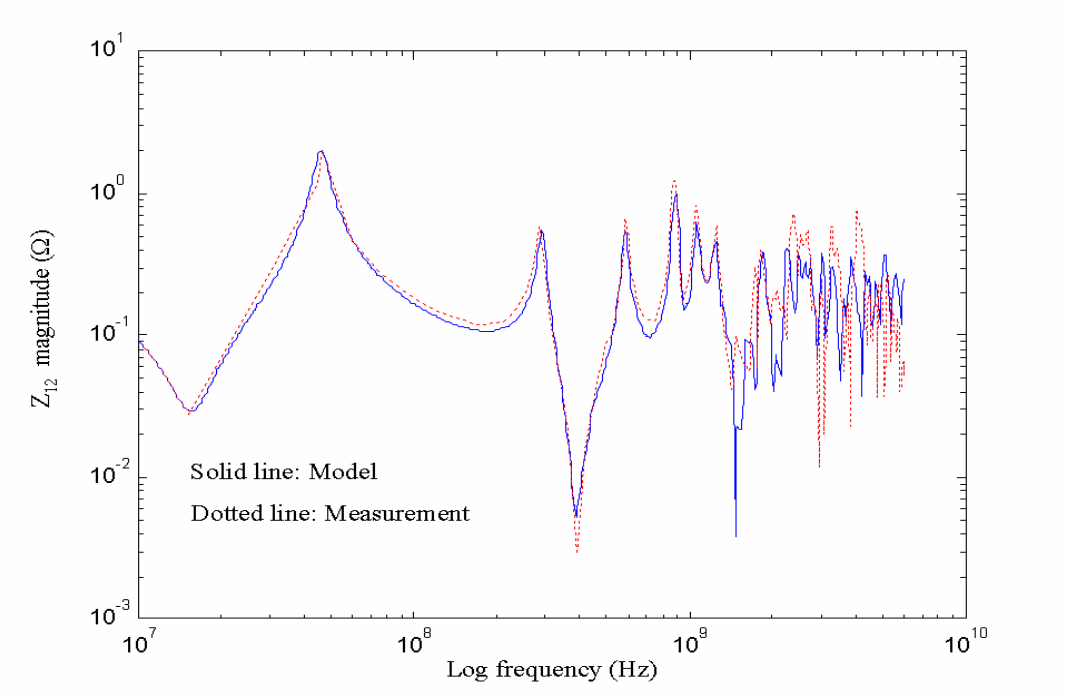
Next, the effects of decoupling capacitors on transfer impedance were investigated. The decoupling capacitors with value of 100 nF were placed at different locations on the board. The equivalent series inductance (ESL) and equivalent series resistance (ESR) of the decoupling capacitors were 0.55 nH and 0.02 Ω, respectively. The model-to-hardware correlations with decoupling capacitors are shown in Figure 2.10. The first null frequency and magnitude of transfer impedances are affected, as can be seen in Figure 2.10.

This can be explained using the schematic in Figure 2.11, which shows a capacitor represented as a series RLC circuit connected to the power/ground planes. The static capacitance of 12.5 nF between planes is shown in the figure. For a single decoupling capacitor, the self-resonant frequency (SRF) is given as

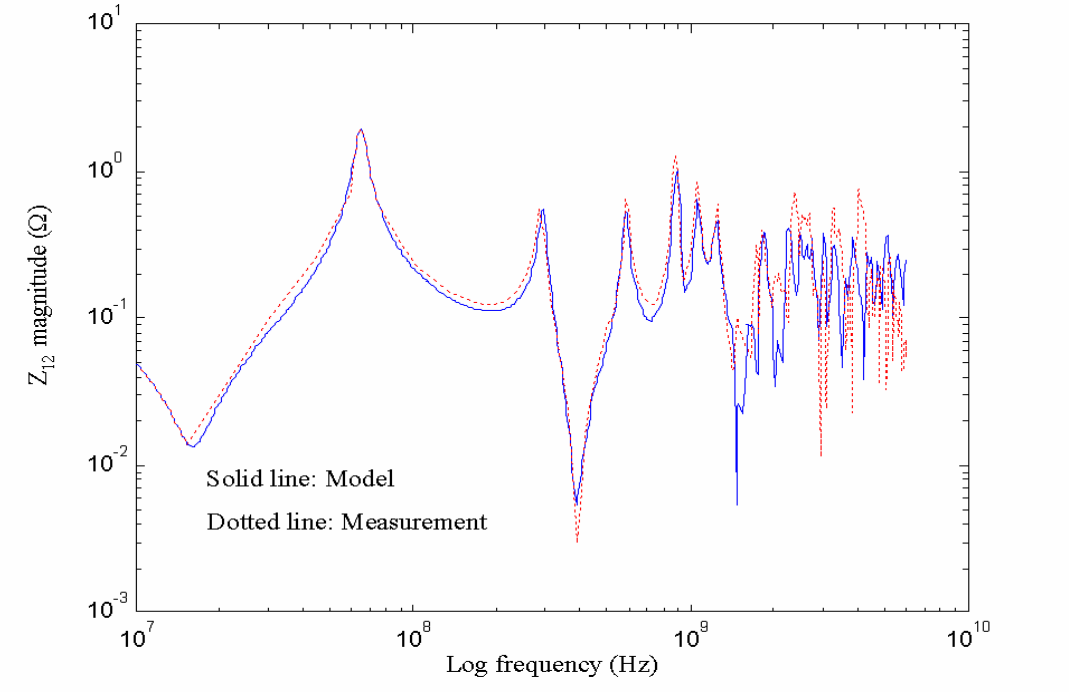
$$\text{SRF} = \frac{1}{2\pi\sqrt{L_{total}\,C_{cap}}} \cong 16.57 \text{ MHz}, \tag{2.6}$$

where L_{total} = 0.923 nH = (L_{cap}(ESL of decoupling capacitor) + L_{pad}(inductance of pad connected to decoupling capacitor)) and C_{cap}(capacitance of decoupling capacitor) = 100 nF. The impedance magnitude at the SRF represents the ESR of the decoupling capacitor. If the capacitance between power and ground layers is minimal and $C_{cap} >> C_{plane}$, where C_{plane}(plane capacitance) = 12.5 nF, the parallel resonant frequency (PRF) can be approximated as

$$\text{PRF} = \frac{1}{2\pi\sqrt{L_{total}\,C_{plane}}} \cong 46.86 \text{ MHz}. \tag{2.7}$$

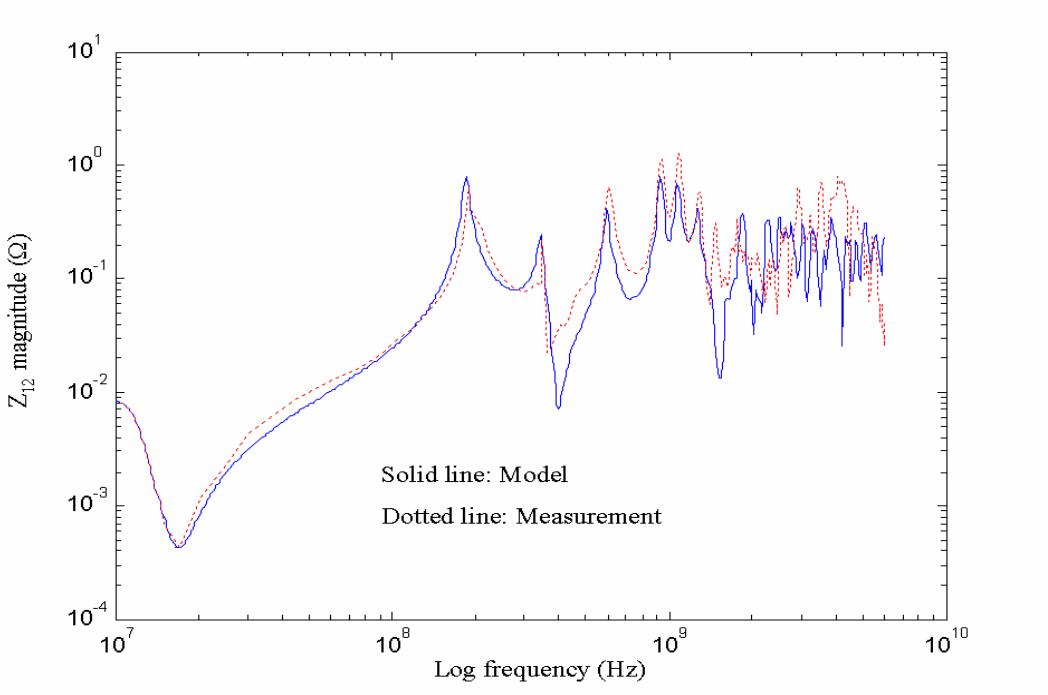


(a)



(b)

Figure 2.10 Model-to-hardware correlation of transfer impedances between port C238 and port C217 in layer 4 and layer 5 in the PCB (a) Transfer impedance between port C238 and port C217 with a decoupling capacitor, (b) Transfer impedance with two decoupling capacitors, and (c) Transfer impedance with 18 decoupling capacitors.



(c)

Figure 2.10 Model-to-hardware correlation of transfer impedances between port C238 and port C217 in layer 4 and layer 5 in the PCB (a) Transfer impedance between port C238 and port C217 with a decoupling capacitor, (b) Transfer impedance with two decoupling capacitors, and (c) Transfer impedance with 18 decoupling capacitors.

In Figure 2.10 (a), the addition of a decoupling capacitor results in a first null at 16.57 MHz, while the first peak occurs at 46.86 MHz. Figure 2.10 (b) shows the transfer impedance magnitude when two decoupling capacitors are attached. In this case, the first null remains at the same location, while the first peak moves to a higher frequency. This is due to the doubling in the capacitance and a reduction in the inductance to half its original value, which does not change the SRF but increases the PRF. Both Figure 2.10 (a) and (b) show good-model-to hardware correlation. In Figure 2.10 (c), all the decoupling capacitors (18) on the PCB were added and the results still show good model-to-hardware correlation, validating the accuracy of the transmission matrix method for modeling power/ground planes up to high frequencies. From Figure 2.10, the addition of

18 decoupling capacitors results in very low impedance up to 100 MHz. In Figure 2.10, the peaks in the frequency response are produced by standing wave resonances, which are undesirable [38].

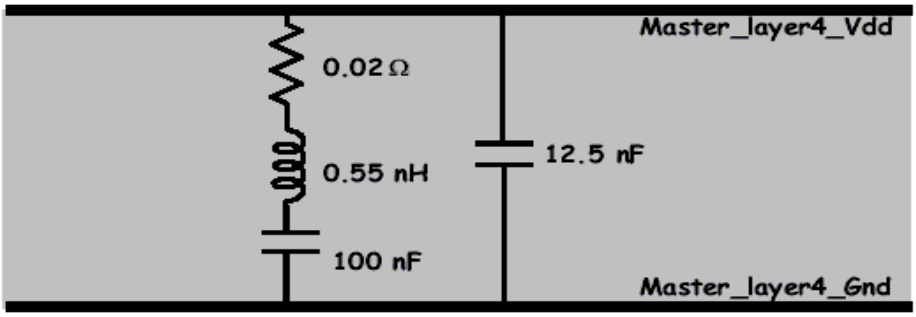


Figure 2.11 Model of power/ground plane pair with a decoupling capacitor.

It is important to note that the measured results in Figure 2.8 and Figure 2.10 are for loaded boards containing many nonidealities. Hence, the correlation between modeling and measurements in Figure 2.8 and Figure 2.10 is considered to be quite good, even though the results do not show exact correlation at higher frequencies.

2.4 Modeling of master-slave power distribution network

In the previous section, though layers 4 and 5 were modeled, these represented dummy layers that were used for checking the accuracy of the transmission matrix method. In reality, layers 2 and 3 were used to supply power to the master and slave chips, as shown in Figure 2.6. Layer 2 represented a continuous ground plane while a split plane structure was used in layer 3 for Vdd, as shown in Figure 2.12. The two islands on the master and slave sections were connected to a 1.2 V small narrow strip

power island and 1.2 V voltage regulator in layer 1 through 7 vias, as shown in Figure 2.12. A ferrite bead of inductance 120 nH was used to filter any power supply noise, as shown in Figure 2.12. There were 48 decoupling capacitors on the master and slave power islands in layer 3.

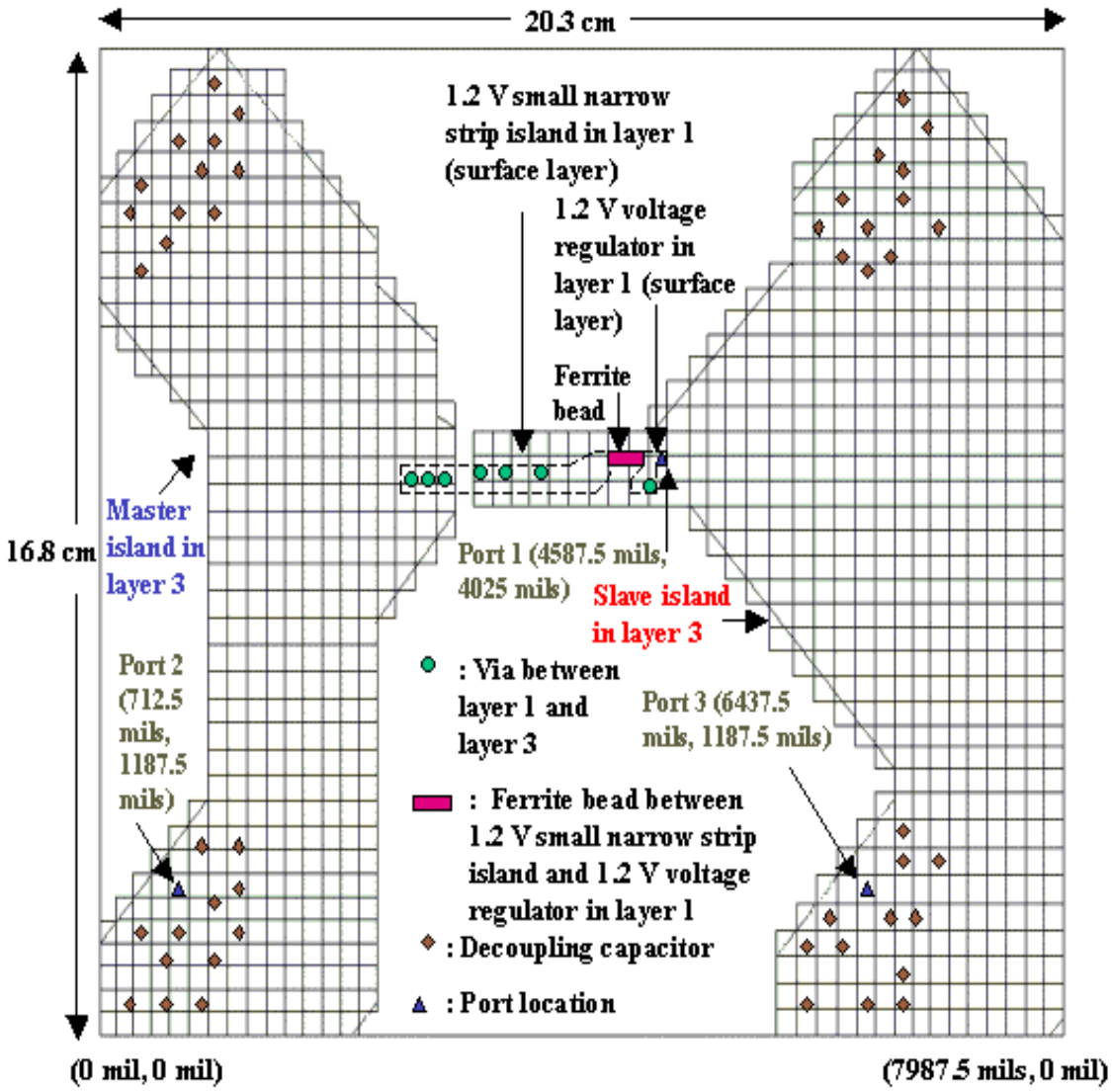
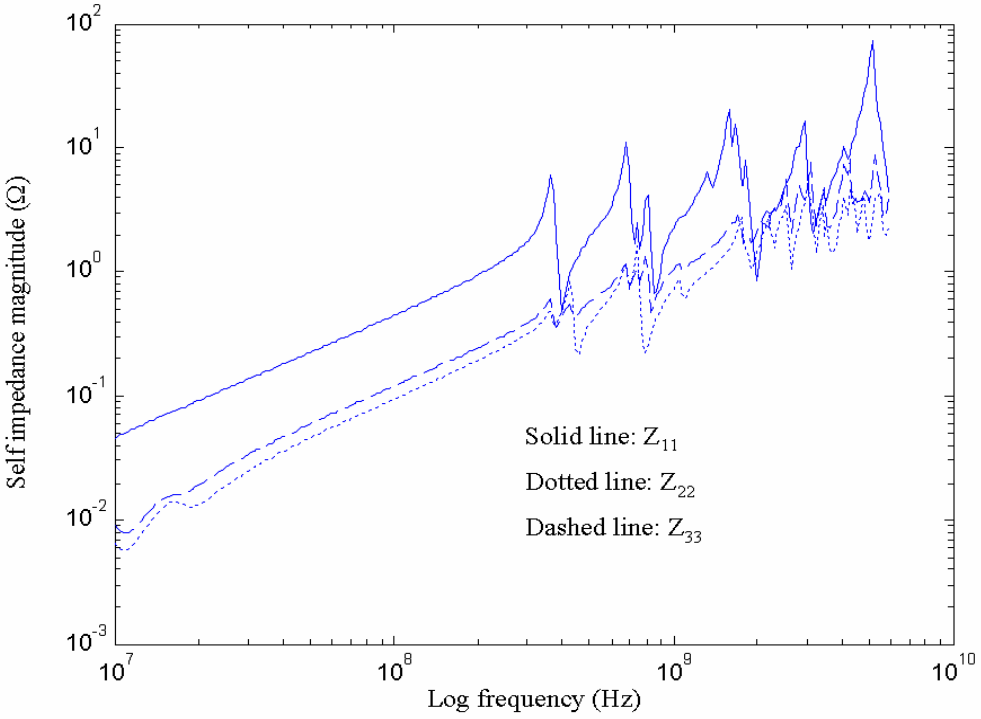


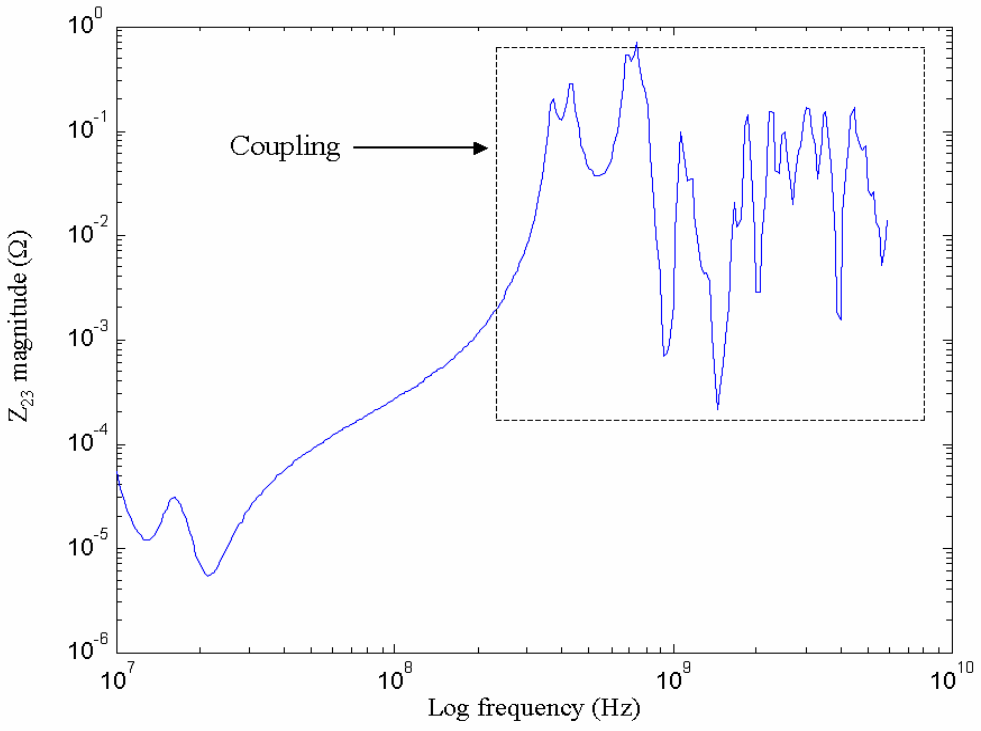
Figure 2.12 Modeling of master and slave islands.

Three ports were defined on the PDN, as shown in Figure 2.12, to represent the positions of the voltage regulator (port 1), master chip (port 2), and slave chip (port 3). Though additional ports could be used to represent the chip, no major change in the frequency response was observed with additional ports. All the voltages at the ports were defined between the voltage and ground planes, with coordinates as shown in Figure 2.12. The irregular structure shown in Figure 2.12 was modeled using the transmission matrix method. A rectangular grid was used, as shown in Figure 2.12, with a unit cell size of 0.385 cm x 0.385 cm, which corresponds to an electrical size of $\lambda/6.2$ at 6 GHz. This resulted in 1,087 unit cells for approximating the structure, which included the narrow rectangular strip on layer 1, voltage regulator on layer 1, the continuous ground plane on layer 2, and the split plane in layer 3, as shown in Figure 2.12. The seven vias connecting layers 1 and 3 were represented as short circuits and modeled in TMM by enforcing the continuity of the currents and voltages at these sections. TMM was used to compute the 3 x 3 impedance matrix, which provides the self- and transfer impedance at the three port locations. The transfer impedance of the master and slave sections in layer 3 was simulated across the master and slave split sections from 10 MHz to 6 GHz. In addition, the self-impedances of the master and slave sections were computed. The self-impedance within the master and within the slave sections remains almost identical, as shown in Figure 2.13 (a).

The self-impedance (Z_{11}) seen from the voltage regulator shows higher impedance than either Z_{22} or Z_{33}. This is because a narrow strip was used to supply the charge to the switching circuits in layer 1. The narrow strip has smaller capacitance, larger inductance, and therefore larger impedance. In Figure 2.13 (b), the transfer impedance between the



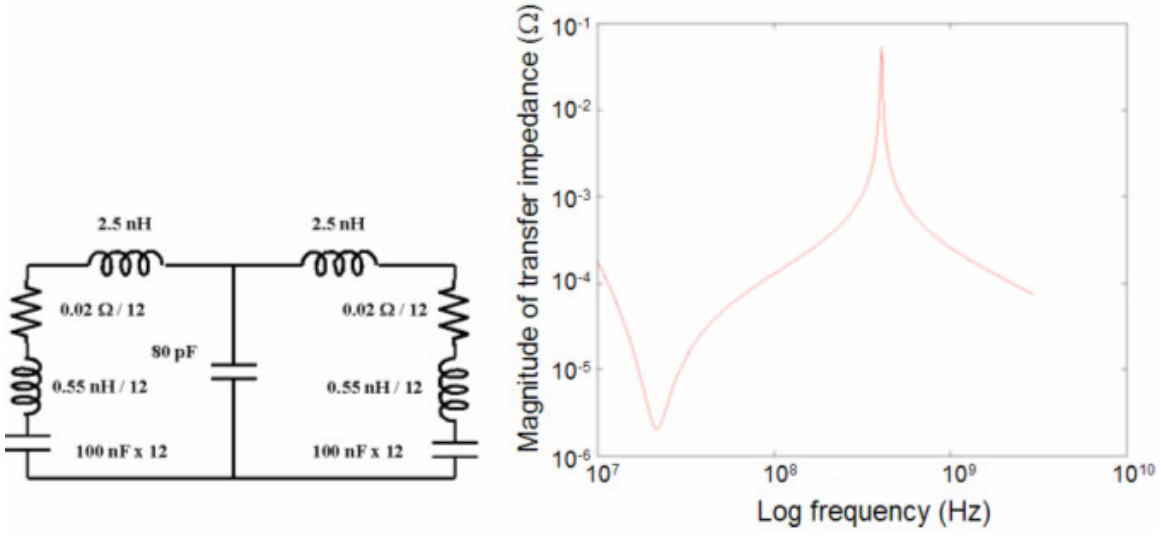
(a)



(b)

Figure 2.13 Impedances of master and slave islands (a) Self-impedances at port 1, 2, and 3 and (b) Transfer impedance between port 2 in master island and port 3 in slave island.

master and slave split sections show little coupling at low frequencies since separate islands were used to supply power to the master and slave sections. However, substantial coupling between the master and slave sections was observed at high frequencies even though these sections were separated. This is because the narrow strip from the voltage regulator was used to maintain the same potential on the two islands using vias. This induces capacitive coupling between the two islands. When the strip from the voltage regulator used to maintain the same potential on the two islands creates a resonance, energy is coupled through the coupling capacitance. This kind of behavior can be explained using a simple equivalent circuit, as shown in Figure 2.14. In this figure, 2.5 nH of inductance is the spreading inductance from the decoupling capacitor to the master and slave chips. Each chip has 12 capacitors in parallel, which results in a small



(a) (b)

Figure 2.14 (a) Equivalent circuit for coupling between master and slave islands (b) its transfer impedance response between port 2 and port 3.

impedance at low frequencies. The circuit in Figure 2.14 generates a null at 21.47 MHz and a peak at 512.15 MHz, similar to the coupling shown in Figure 2.13 (b). Hence, isolated islands can couple energy at high frequencies, which is a detrimental effect for low-voltage signaling methods.

2.5 Modeling and analysis of power supply noise

Three-port impedance parameters from 10 kHz to 6 GHz, as shown in Figure 2.13 were generated using the transmission matrix method. These were converted to admittance parameters that were used as inputs to the macromodeling program. Using the macromodeling method in [78], the frequency response was divided into irregular subbands. This was because the admittance parameters had highly unbalanced amplitudes that varied from 7.4498×10^{-9} to 227.6 [mho] from DC to 6 GHz. The comparison between the input y-parameters and the macromodels is shown in Figure 2.15 for Y_{22} and Y_{23}, which shows good agreement between the input y-parameter data and the macromodels.

The time domain simulation was performed in HSPICE using a macromodel of the power/ground planes, differential drivers, and transmission lines for computing power supply noise. The schematic for simulating power supply noise is shown in Figure 2.16. The driver model used was a time-dependent resistive switch representing four differential drivers. The drivers were connected to four differential transmission lines. The differential drivers with 0.05 ns rise time and 0.05 ns fall time were powered from port 2. The differential transmission lines with 100 Ω characteristic impedance (50 Ω characteristic impedance to ground) and 1 ns delay was connected to the output of the

driver. A standard transmission line model available in HSPICE was used to represent the transmission lines. The far end of the transmission lines was terminated in a 50 Ω for matching and connected to 0.3 V supply voltage. Port 3, representing 1.2 V power supply for the slave chip, was left unterminated. Hence, the differential transmission lines provide the communication path between the master and slave chips. The voltage regulator module with 0.6 V supply voltage is connected between port 1 and ground in Figure 2.16.

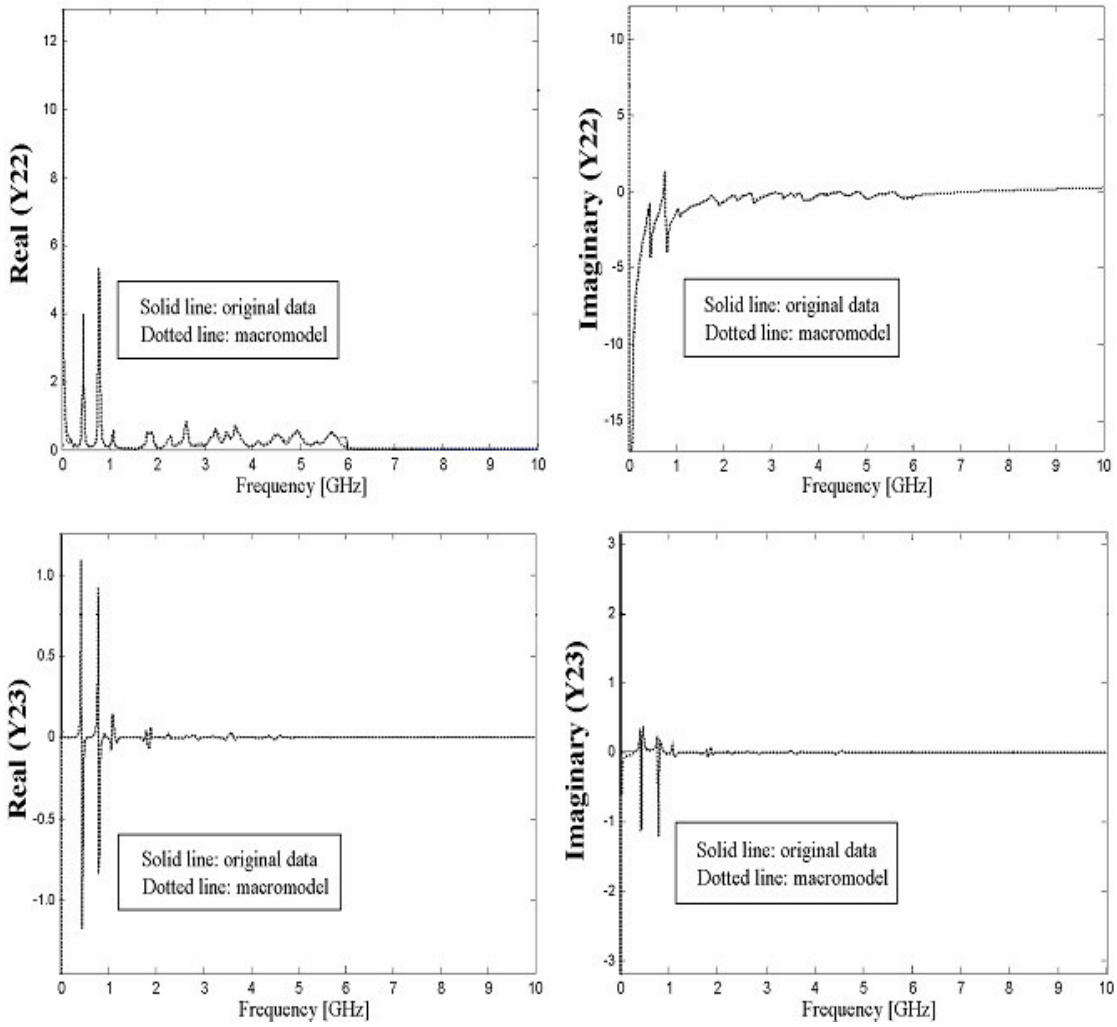


Figure 2.15 Comparison between the input Y-parameters and macromodels.

In Figure 2.5, the two ground planes are connected to each other using numerous vias. Hence, the potential of the two ground planes is maintained constant at the same potential. In Figure 2.16, the differential transmission lines are referenced to the ground plane, which is consistent with the cross-section in Figure 2.5. When drivers switch from high to low or low to high, they deposit time-varying charges on the power/ground planes. These time-varying charges result in a current source that excites electromagnetic waves between the power/ground planes, causing them to bounce [50], [51]. The time-varying charges are a direct result of the return current on the planes. Hence, appropriate referencing for the transmission lines in Figure 2.16 is important for simulating power

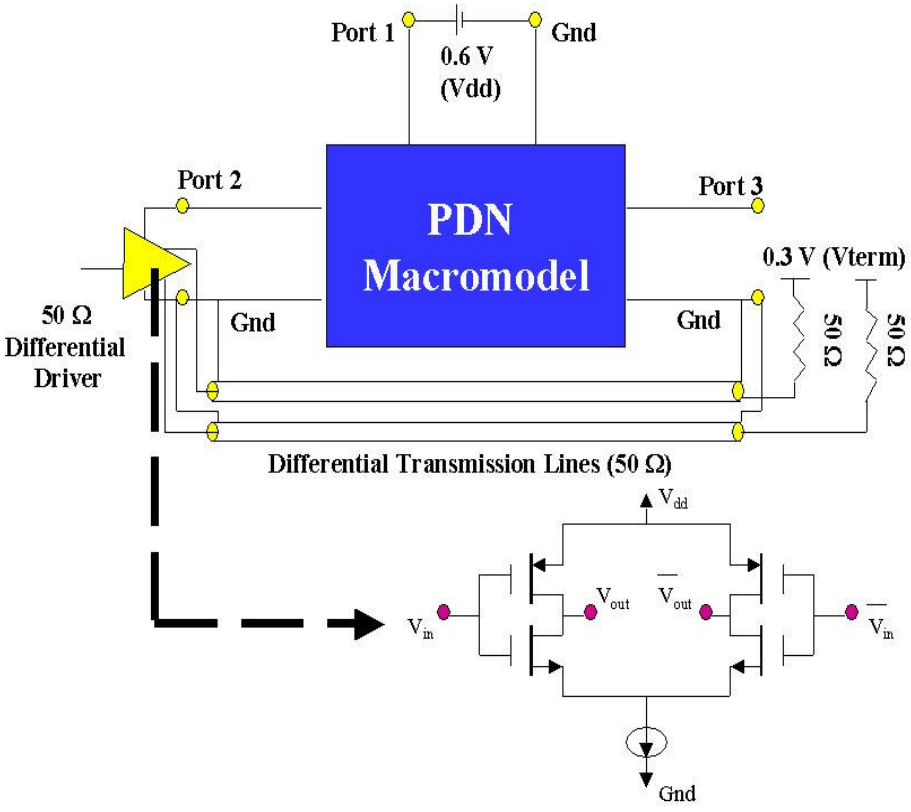


Figure 2.16 Modeling of power supply noise with differential drivers, transmission lines and PDN macromodel.

supply noise.

The time domain waveform of power supply noise between port 2 and ground is shown in Figure 2.17. In this figure, the maximum power supply noise occurs when the driver output changes from low to high or from high to low. This is because the return current from the transmission lines on the power/ground planes excites electromagnetic waves, causing plane bounce. In packages containing planes, the return current is on a reference plane that is in close proximity to the transmission line. This is because, at high speed, the return current follows the path of least inductance, not the path of least resistance. The lowest inductance return path lies directly under a signal conductor, minimizing the total loop area between outgoing and returning current paths [52].

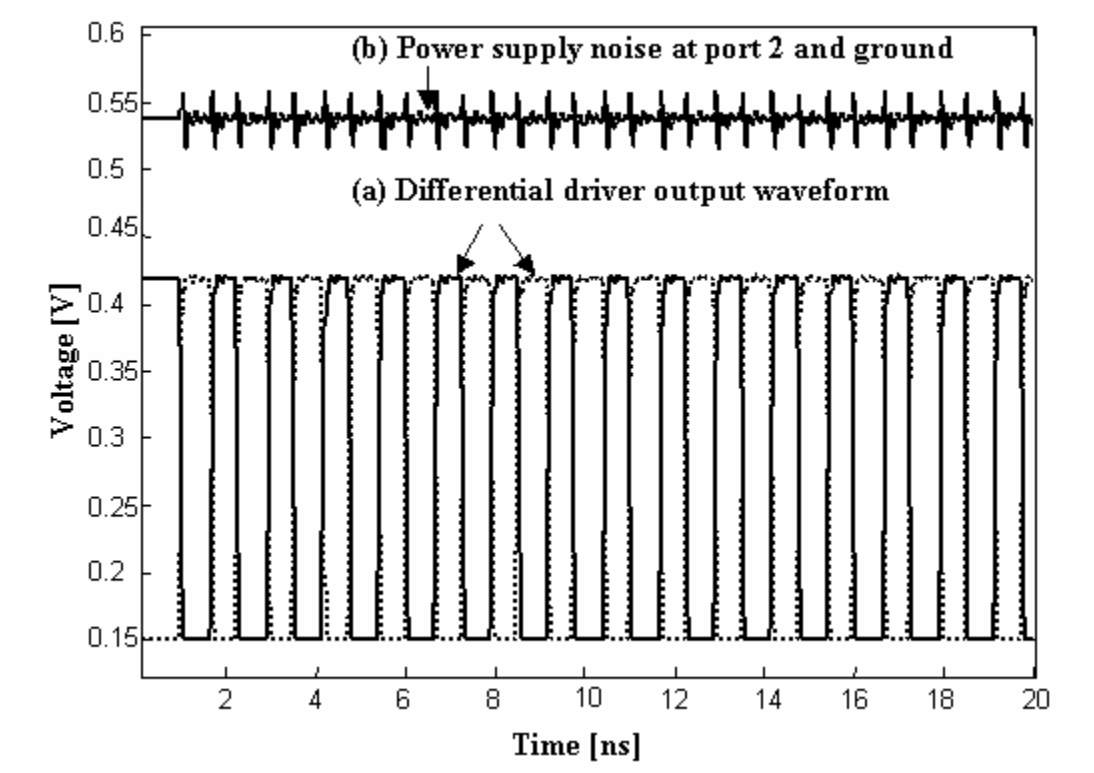


Figure 2.17 Power supply noise simulation results (a) Differential driver output waveform and (b) Power supply noise between port 2 and ground.

This effect is captured in Figure 2.17. In this figure, even though the peak noise occurs during the transition, the power supply continues to bounce even between transitions. This is due to the Q-factor of the power/ground planes. Perfectly balanced differential drivers cannot generate power supply noise. This is because the current drawn from V_{dd} is perfectly balanced by the current into ground. However, process variations cause an imbalance in the driver output current. This condition has been simulated by injecting a 10 ps delay between the differential inputs. The switching of four differential drivers result in a power supply noise of 40 mV, as shown in Figure 2.17. To provide a measure of the efficiency of the methodology proposed, the CPU time for computing power supply noise on a Sun workstation was 36.8 secs.

2.6 Summary

In this chapter, an efficient modeling and analysis methodology for a PDN in a high-speed system has been described. This methodology is based on a hybrid method that combines the TMM in frequency domain and the macromodeling method in time domain. First, TMM was applied to the PDN in the test vehicle to compute the frequency response. The results were correlated with measurement data using vector network analyzer measurements. Next, the macromodel representation of the plane pairs was generated at the desired ports using macromodeling. Finally, the macromodel of the planes, the differential driver model, and transmission lines were co-simulated in HSPICE for computing power supply noise. The methodology for modeling and analyzing power distribution networks, as presented in this chapter, can be applied to complex systems containing numerous chips on multi-layered packages and boards.

The important discovery in this chapter through analysis was that substantial coupling between the master and slave islands was observed at high frequencies even though these islands were separated. This kind of coupling could result in detrimental effects to the system at high frequencies since split planes are supposed to serve as isolated islands. Hence, isolated islands can couple energy at high frequencies, which is a detrimental effect for low-voltage signaling methods. This kind of coupling between split planes creates a major problem in mixed-signal systems since RF circuits are very sensitive to any noise through this kind of coupling.

CHAPTER 3

Alternating Impedance Electromagnetic Bandgap (AI-EBG) Structure

In this chapter, a novel two layer EBG structure is discussed. Along with reducing the layer count, this structure does not require any blind vias. Moreover, this structure provides better isolation level as compared to other EBG structures that have been proposed so far.

A theoretical analysis of the alternating impedance electromagnetic bandgap (AI-EBG) structure is discussed using the Brillouin zone concept. It is important to understand the importance of the reciprocal lattice and Brillouin zone when periodic structures such as EBG structures are analyzed. Due to the symmetry of the unit cell in the AI-EBG structure, propagation through such a medium contains redundant propagation wave vectors. Hence, the unique vectors can be grouped in a region called the irreducible Brillouin zone. To this end, the following steps have been taken. First, the reciprocal space has been introduced, compared with the real space, to understand the Brillouin zone in the reciprocal space. Second, it has been shown how the Brillouin zone can be constructed in the reciprocal lattice. Third, the design of the AI-EBG structure has been shown. Fourth, the equation to estimate the stopband center frequency in the first stopband of the AI-EBG structure has been developed using the Brillouin zone concept. Fifth, the propagation characteristics of the AI-EBG structure has been analyzed using

the transmission line network method. Finally, the cutoff frequency of the AI-EBG structure has been studied using the image parameter method.

3.1 Periodic Structures

Periodic structures have become popular because of their ability for suppressing unwanted electromagnetic mode transmission and radiation in microwave and millimeter waves [15]-[17]. The EBG structures are periodic structures in which the propagation of electromagnetic waves is forbidden in certain frequency bands. In these EBG structures, the constructive and destructive interference of electromagnetic waves results in transmission and reflection bands [18]. The EBG structure has also been called a photonic bandgap (PBG) structure or a frequency selective surface (FSS). A common feature of periodic structures is the existence of frequency bands where electromagnetic waves are highly attenuating and do not propagate. Analogous to an electrical crystal where periodic atoms presents a bandgap prohibiting electron propagation, a photonic crystal is made of macroscopic dielectrics periodically placed (or embedded) within a surrounding medium. The periodic nature of the structure produces a photonic bandgap (PBG) within which photons (waves) are forbidden in a certain frequency range [18].

Periodic structures support slow wave propagation (slower than the phase velocity of the unloaded line) and have passband and stopband characteristics similar to those of filters. Therefore, periodic structures are good for applications in antennas, traveling-wave tubes, and phase shifters [48].

3.2 Bloch Theorem

An electron in a periodic structure can be characterized by its wave function, $\Psi(\vec{r})$. Bloch discovered that such electrons have wave functions in the form of a plane wave multiplied by a function that has the periodicity of the direct lattice [68], [69]. That is,

$$\Psi_k(\vec{r}) = \exp(i\vec{k}\cdot\vec{r})u_k(\vec{r}) \tag{3.1}$$

where $\vec{k}$ is wave vector and

$$u_k(\vec{r}) = u_k(\vec{r}+\vec{R}) \tag{3.2}$$

for all direct lattice vectors $\vec{R}$. This result is known as Bloch's theorem. From equation (3.1), we have

$$\psi_k(\vec{r}+\vec{R}) = \exp[i\vec{k}\cdot(\vec{r}+\vec{R})]u_k(\vec{r}+\vec{R}) = \exp(i\vec{k}\cdot\vec{R})\psi_k(\vec{r}) \tag{3.3}$$

for any value of $\vec{k}$ and every $\vec{R}$ in the direct lattice.

Equation (3.3) is an alternative form of Bloch's theorem. It tells us that the electron wave function in any primitive unit cell of the direct lattice differs from that in any other cell only by the factor $\exp(i\vec{k}\cdot\vec{R})$. For real $\vec{k}$, this represents a difference in phase. The wave vector, $\vec{k}$, has dimensions of reciprocal length and belongs in reciprocal space with the vector $\vec{K}$. Let us assume that the electron wave function also has a wave vector that is equal to a reciprocal lattice vector. From equation (3.3),

$$\psi_K(\vec{r}+\vec{R}) = \exp(i\vec{K}\cdot\vec{R})\psi_K(\vec{r}) = \psi_K(\vec{r}) \tag{3.4}$$

for all $\vec{R}$. That is, the electron wave functions ψ_κ are periodic in $\vec{R}$.

Let's assume that an electron has a wave vector $\vec{k}$ given by

$$\vec{k} = \vec{K} + \vec{k}' \tag{3.5}$$

where $\vec{k}'$ is some other vector in reciprocal space. From equations (3.3) and using $\exp(i\vec{K}\cdot\vec{R}) = 1$, we find that

$$\psi_k(\vec{r}+\vec{R}) = \exp\{i[(\vec{K}+\vec{k}')\cdot\vec{R}]\}\psi_K(\vec{r}) = \exp(i\vec{k}'\cdot\vec{R})\psi_k(\vec{r}) \tag{3.6}$$

or the wave functions ψ_K obey Bloch's theorem as if they had wave vector $\vec{k}'$. Thus the wave function does not have a unique wave vector $\vec{k}$ but a set of wave vectors that differ from each other by the set of reciprocal lattice vectors.

One important fact that Bloch's theorem states is that different values of $\vec{k}$ do not necessarily lead to different modes. Specifically, a mode with wave vector $\vec{k}$ and a mode with wave vector $\vec{k}+\vec{K}$ are the same mode, if $\vec{K}$ is a reciprocal lattice vector. The region of important and nonredundant values of $\vec{k}$ is called the Brillouin zone.

Brillouin zone can be constructed in the reciprocal lattice as follows. First, convert real lattice to reciprocal lattice. Second, select a lattice point and draw construction lines to the nearest neighboring points.Third, draw lines that perpendicularly

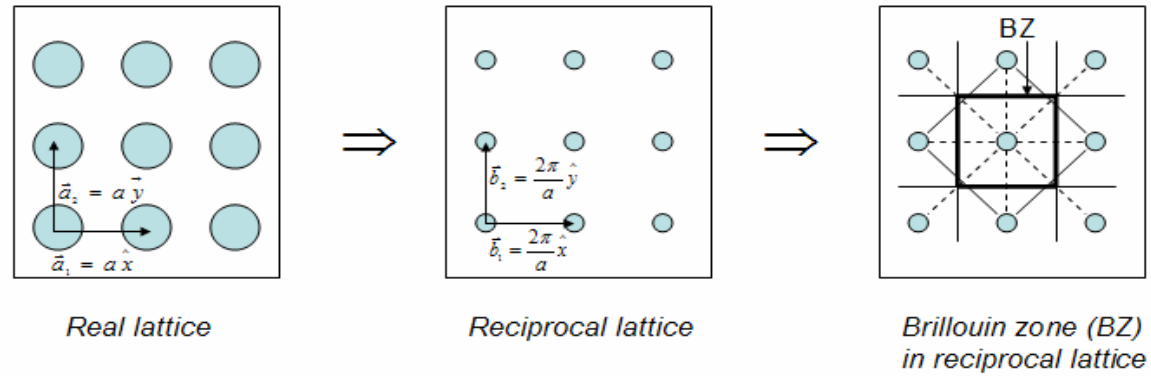


Figure 3.1 Construction procedures for Brillouin zone (BZ) in reciprocal lattice.

bisect the construction lines. Finally, the smallest enclosed area represents the Brillouin zone. Therefore, the Brillouin zone is a primitive cell in the reciprocal lattice.

3.3 Design of AI-EBG Structure

The alternating impedance electromagnetic bandgap (AI-EBG) structure is a metallo-dielectric EBG structure that consists of two metal layers separated by a thin dielectric material, as shown in Figure 3.2. In the AI-EBG structure, only one metal layer has a periodic pattern which is a two-dimensional (2-D) rectangular lattice with each element consisting of a metal patch with four connecting metal branches, as shown in Figure 3.3 (a).

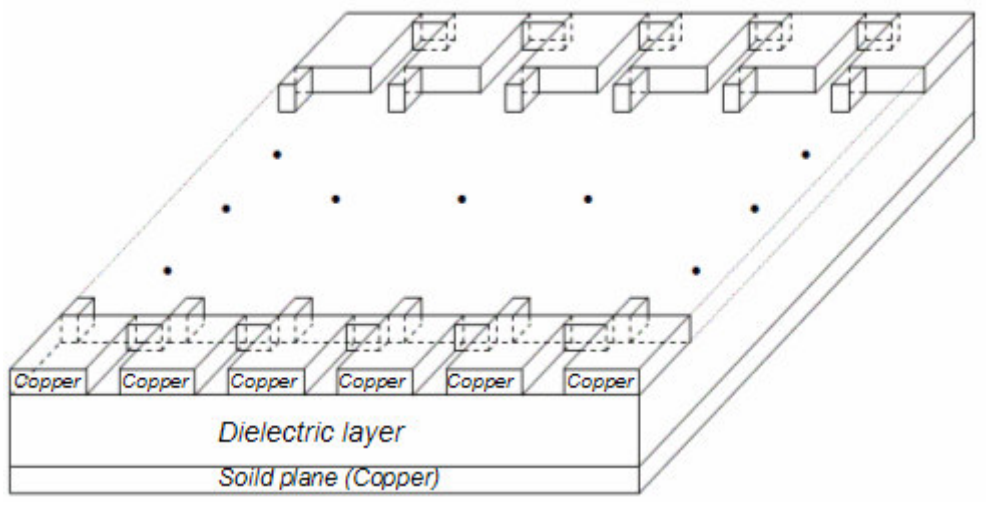
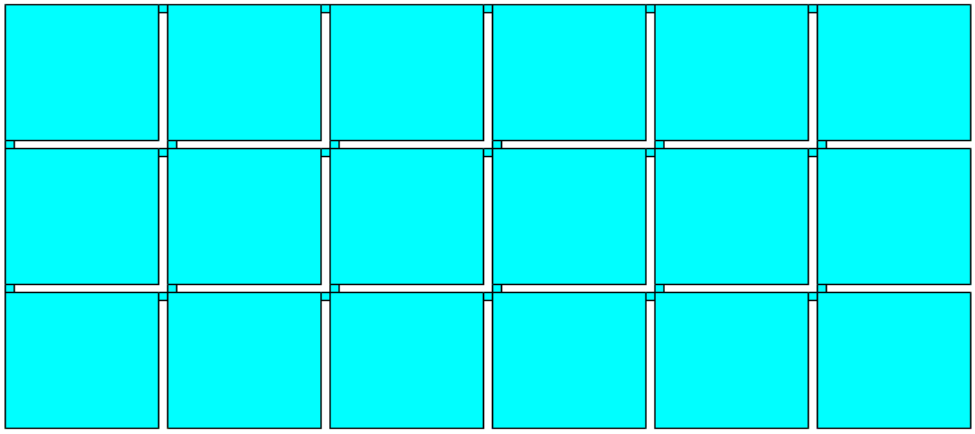


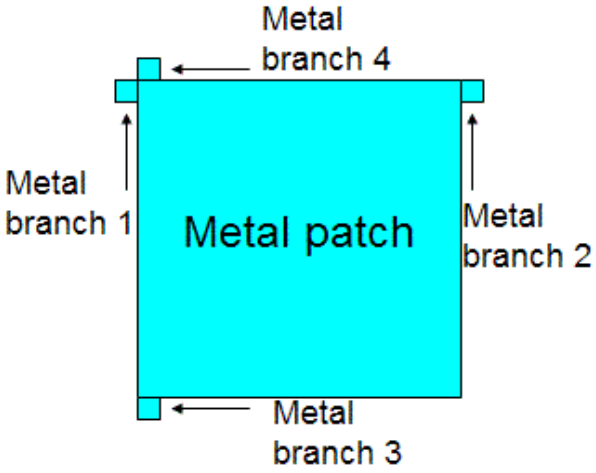
Figure 3.2 Schematic of three-dimensional (3-D) alternating impedance electromagnetic bandgap (AI-EBG) structure.

This EBG structure can be realized with metal patches etched in the power plane (or in the ground plane depending on design) connected by metal branches to form a

distributed *LC* network (where *L* is inductance and *C* is capacitance). In this structure, a metal branch introduces additional inductance while the metal patch and the corresponding solid plane form the capacitance. The unit cell of this EBG structure is shown in Figure 3.3 (b). The location of metal branches on edges of metal patch was optimized to ensure maximum wave destructive interference, which results in excellent



(a)



(b)

Figure 3.3 (a) Schematic of periodic pattern in one of power and ground planes and (b) Unit cell.

isolation characteristics in stopband range. It is important to note that the shape of the metal patch and branch can be a square, or a rectangle. Figure 3.3 (a) represents one layer of the plane pair where the other layer (not shown) is a solid plane.

The structure formed in Figure 3.2 does not require blind vias and the dielectric thickness can be very thin (1 mil ~ 4 mils), which results in a low-cost process. Hence, the AI-EBG structure has the advantage of being simple and can be easily designed and fabricated using a standard printed circuit board (PCB) process without the need for blind vias and using only two metal layers, compared to the mushroom-type EBG structure in [26]-[28], which require three metal layers and blind vias.

3.4 Equivalent circuit representation of AI-EBG structure

The EBG structure presented in the previous section can be called the alternating impedance electromagnetic bandgap (AI-EBG) structure since it consists of alternating sections of high and low characteristic impedances, as shown in Figure 3.4. The EBG structure in Figure 3.2 is a two-dimensional (2-D) parallel-plate waveguide (or 2-D transmission line) with alternating perturbation of its characteristic impedance. The metal patch on the top layer and corresponding solid plane on the bottom layer can be represented as a parallel-plate waveguide having low characteristic impedance, while the metal branch and the corresponding solid plane pair can be treated as a parallel-plate waveguide having high characteristic impedance [53]. This is because the characteristic impedance in a parallel-plate waveguide for a TEM mode (dominant mode in plane pairs with thin dielectrics), is given by

$$Z_o = \frac{\eta d}{w} = \sqrt{\frac{L}{C}} \tag{3.7}$$

where η is intrinsic impedance of the dielectric, d is the dielectric thickness, w is the width of the metal, L and C are inductance and capacitance per unit length. Since $w_{patch} > w_{branch}$ and characteristic impedances are inversely proportional to w, Z_0 of the metal patch is lower than Z_0 of the metal branch. Due to this impedance perturbation, wave propagation can be suppressed in certain frequency bands.

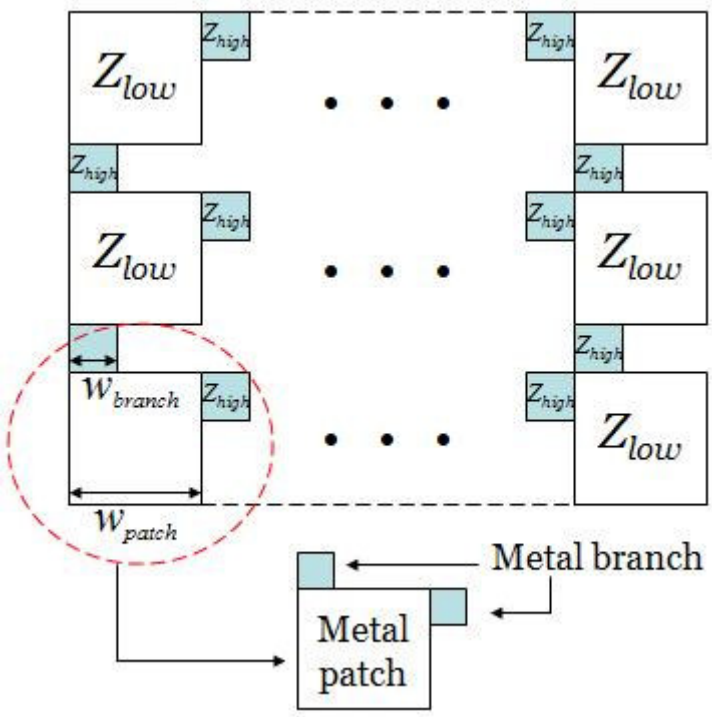


Figure 3.4 EBG structure with alternating impedance.

The AI-EBG dispersion characteristics can also be explained using filter theory. Figure 3.4 shows the three-dimensional (3-D) schematic of the EBG structure with 3 equivalent circuits described. Figure 3.5 (a) shows the one-dimensional (1-D) T-type

equivalent circuit of the metal patch including the dielectric and the corresponding solid plane. Figure 3.5 (b) shows the 1-D equivalent circuit of the metal branch including the dielectric and the corresponding solid plane. In these figures, C_{branch} is very small and can be neglected due to the size of the metal branch. In addition to the *LC* elements, small parasitic reactances at the interface between the metal patch and branch exist, as shown in Figure 3.5 (c) due to discontinuities caused by the change in width [48]. From Figure 3.5, it is clear that the resulting two-dimensional *LC* network representing AI-EBG

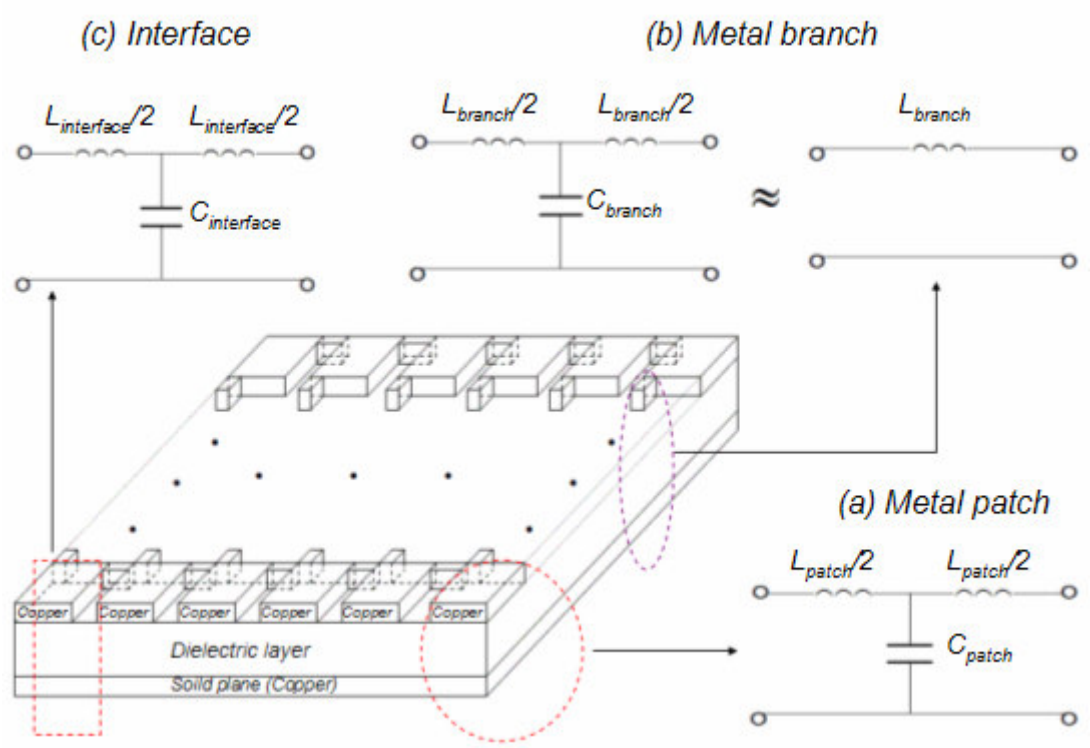


Figure 3.5 One-dimensional (1-D) equivalent circuits for 3 parts of AI-EBG structure (a) 1-D equivalent circuit for the metal patch including FR4 and the corresponding metal part of the other solid plane, (b) 1-D equivalent circuit for the metal branch part including FR4 and the corresponding metal part of the other solid plane, and (c) 1-D equivalent circuit for the interface between a metal patch and a metal branch.

structure is a low-pass filter (LPF), which has been verified through simulations and measurements in Chapter 4.

3.5 Stopband Center Frequency of AI-EBG Structure

It is possible to obtain the stopband center frequency of the AI-EBG structure using the Brillouin zone concept. Figure 3.6 shows the Brillouin zone of the AI-EBG structure. The smallest region within the Brillouin zone is called the irreducible Brillouin zone, which is shown as a triangle in Figure 3.6. The rest of the Brillouin zone contains redundant copies of the irreducible zone. The special points at the corners on the Brillouin zone are conventionally known as Γ, X, and M. From the right and top ends of the Brillouin zone in Figure 3.6, we have

$$k_x = \frac{\pi}{a_x} \text{ and } k_y = \frac{\pi}{a_y}, \tag{3.8}$$

where k_x is the wave vector in the x direction, a_x is the length in the x direction in real space (corresponding to the length in the x direction in Brillouin zone in the reciprocal space), k_y is the wave vector in the y direction, a_y is the length in the y direction in real space (corresponding to the length in the y direction in Brillouin zone in the reciprocal space).

Using $k = 2\pi f\sqrt{\mu\varepsilon}$ and assuming that $a = a_x = a_y$, the stopband center frequency, f_{center}, is obtained as

$$f_{center} = \frac{1}{2a\sqrt{\mu\varepsilon}} = \frac{v_p}{2a}, \tag{3.9}$$

where $v_p = \frac{1}{\sqrt{\mu\varepsilon}}$ is the phase velocity of the light in the medium. Since waves can travel in the x direction (from point Γ to point X in Figure 3.6), in the y direction (from point X to point M in Figure 3.6) and in a diagonal direction (from point M to point Γ in Figure

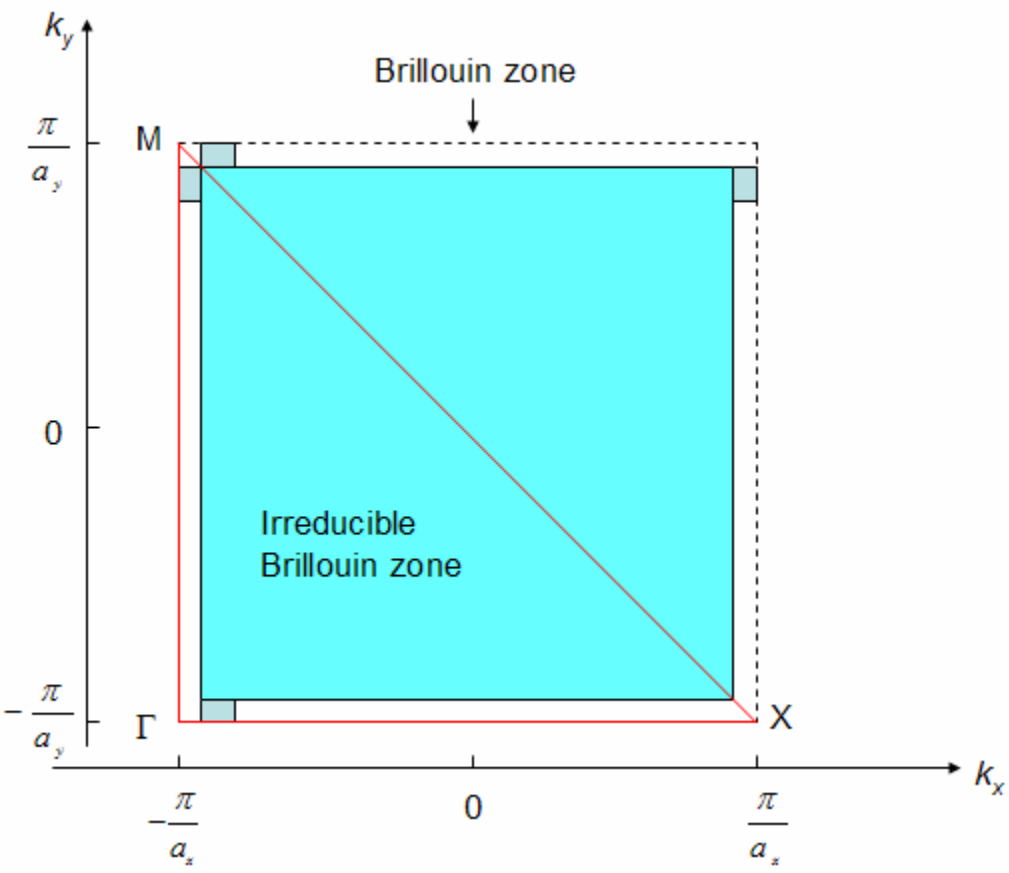


Figure 3.6 Brillouin zone of the AI-EBG structure in Figure 3.3 (a).

3.6), the stopband center frequency should be averaged as

$$f_{center} = \frac{f_{center(\Gamma X)} + f_{center(XM)} + f_{center(M\Gamma)}}{Number\_of\_paths\_in\_BZ}, \tag{3.10}$$

where $f_{center(\Gamma X)}$ is the stopband center frequency in the x direction (from point Γ to point X in Figure 3.6), $f_{center(XM)}$ is the stopband center frequency in a diagonal direction (from X point to M point in Figure 3.6), and $f_{center(M\Gamma)}$ is the stopband center frequency in the y direction (from point M to point Γ in Figure 3.6).For example, for the AI-EBG structure in Figure 4.2 (a), the stopband center frequency is calculated as 4.03 GHz, which is close to the stopband center frequency of the first stopband in Figure 4.2 (b) and therefore is well correlated with the simulation results in Figure 4.2 (b). The method developed using the Brillouin zone concept in this section can be used to estimate the stopband center frequency in the AI-EBG structure for fast design process.

3.6 Propagation Characteristics of AI-EBG Structure

To understand the dispersion characteristics of the AI-EBG structure, the transmission line network (TLN) method has been used in this section. The TLN approach is based on standard periodic analysis for one dimensional symmetric unit cells [48], [62]. Figure 3.7 shows the unit cell for the two-dimensional AI-EBG structure. It consists of two metal layers with a metal patch on the top layer, four metal branches on top layer, and a ground plane on the bottom layer.

For clarity, the structure is assumed periodic along the y direction with perfect magnetic walls along the x directed boundaries. This represents a 1-dimensional structure with periodicity along the y-direction. The structure is assumed infinite along the y direction with wave propagation along the y axis. This enables the modeling and visualization

using TLN analysis, while retaining sufficient generality to describe the unique dispersion characteristics of the AI-EBG structure.

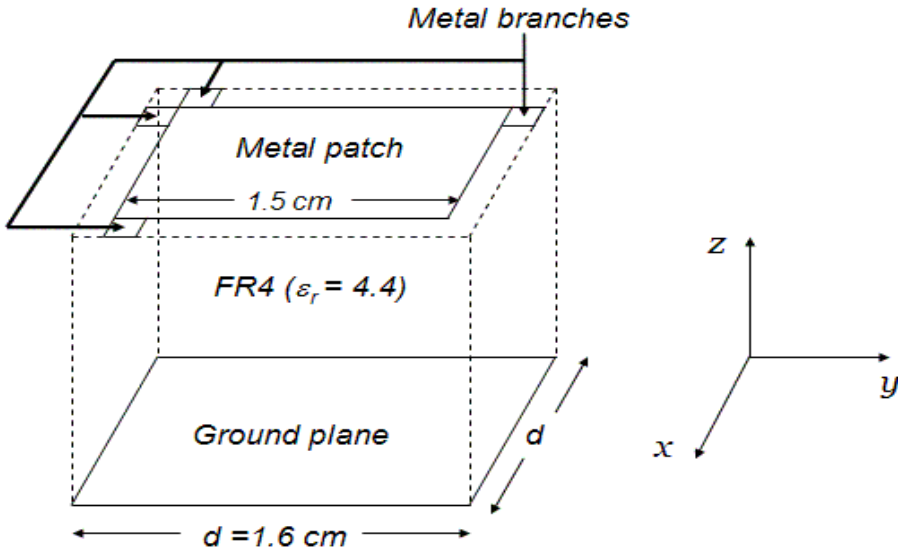


Figure 3.7 Two-dimensional (2-D) unit cell of the AI-EBG structure.

Using the equivalent transmission line circuit in Figure 3.8, the transfer matrix for the unit cell can be written as:

$$T_{Unit\ \_\ Cell\ (BZ)} = T_{L/2} T_{TL} T_C T_{TL} T_{L/2} \tag{3.11}$$

The first and fifth matrix in (3.11), $T_{L/2}$, represents the equivalent series inductance due to the metal branch on the edge of the metal patch. The value of the series inductance is halved ($L/2$) to account for symmetry of the structure. The second and fourth matrix, T_{TL}, represents the transfer matrix for a uniform section of transmission line of length $d/2$. The

third matrix, T_C, represents the equivalent shunt capacitance between the metal patch and the ground plane.

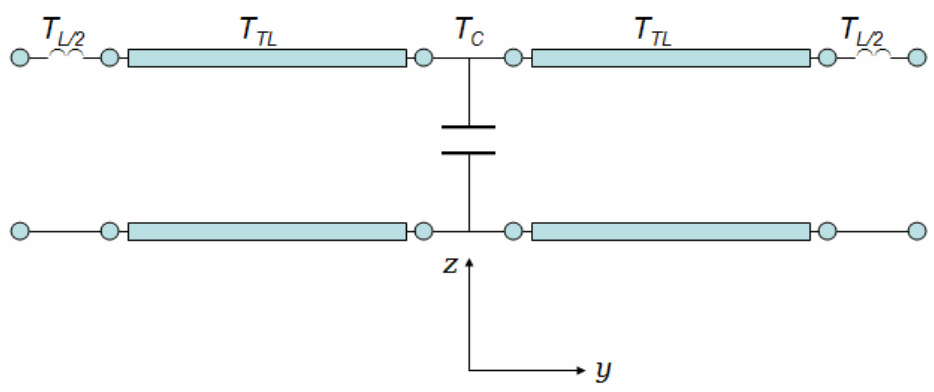


Figure 3.8 Equivalent TL circuit for the unit cell in Figure 3.7 on y-direction.

Using ABCD matrix, $T_{Unit\_Cell(BZ)}$ can be expressed as

$$T_{Unit\_Cell(BZ)} = \begin{bmatrix} 1 & \frac{Z_{branch}}{2} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cos\frac{kd}{2} & jZ_0 \sin\frac{kd}{2} \\ jY_0 \sin\frac{kd}{2} & \cos\frac{kd}{2} \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_{patch} & 1 \end{bmatrix}$$

$$\begin{bmatrix} \cos\frac{kd}{2} & jZ_0 \sin\frac{kd}{2} \\ jY_0 \sin\frac{kd}{2} & \cos\frac{kd}{2} \end{bmatrix} \begin{bmatrix} 1 & \frac{Z_{branch}}{2} \\ 0 & 1 \end{bmatrix} \tag{3.12}$$

where $Z_{branch} = j\omega L_{branch}$, kd = the phase delay of the transmission line segment, $k = 2\pi f\sqrt{\mu\varepsilon}$, d is the length of a unit cell, $Y_{patch} = j\omega C_{patch}$, Z_0 is the characteristic impedance of the transmission line segment, Y_0 is the characteristic admittance of the transmission line segment, ω is the angular frequency given by $\omega = 2\pi f$, f is the frequency and μ and ε are the permeability and permittivity of the dielectric material.

After some calculations, (3.12) becomes:

$$T_{Unit\_Cell(BZ)} = \begin{bmatrix} A_{BZ} & B_{BZ} \\ C_{BZ} & D_{BZ} \end{bmatrix} \tag{3.13}$$

where

$$A_{BZ} = \cos^2\frac{kd}{2}(1+\frac{ZY}{2}) - Z_0Y_0\sin^2\frac{kd}{2} + j\sin\frac{kd}{2}\cos\frac{kd}{2}(ZY_0 + Z_0Y),$$

$$B_{BZ} = \cos^2\frac{kd}{2}(1+\frac{Z^2Y}{4}) - \sin^2\frac{kd}{2}(ZZ_0Y_0 + Z_0^2Y) + j\sin\frac{kd}{2}\cos\frac{kd}{2}(\frac{Z^2Y}{2} + Z_0ZY + 2Z_0),$$

$$C_{BZ} = Y\cos^2\frac{kd}{2} + j2Y_0\sin\frac{kd}{2}\cos\frac{kd}{2},$$

$$D_{BZ} = \cos^2\frac{kd}{2}(1+\frac{ZY}{2}) - Z_0Y_0\sin^2\frac{kd}{2} + j\sin\frac{kd}{2}\cos\frac{kd}{2}(ZY_0 + Z_0Y),$$

$Z = Z_{branch}$ *and* $Y = Y_{patch}$.

By combining the ABCD matrix of the Brillouin zone unit cell, $T_{Unit\_Cell(BZ)}$, with Floquet's theorem, which relates the voltage and current between the *n*th terminal (input of the unit cell) and *n+1*th terminal (output of the unit cell) through $e^{-\gamma d}$, we obtain [18]:

$$\begin{bmatrix} V_n \\ I_n \end{bmatrix} = T_{Unit\_Cell(BZ)}\begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} = \begin{bmatrix} A_{BZ} & B_{BZ} \\ C_{BZ} & D_{BZ} \end{bmatrix}\begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} = e^{\gamma d}\begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} \tag{3.14}$$

where $\gamma = \alpha + j\beta$ is the complex propagation constant, α is the attenuation constant, and β is the phase constant.

Based on a nontrivial solution for (3.14), the following analytic dispersion equation for the AI-EBG structure can be obtained as:

$$\cos\beta d = \frac{Z_{branch}Y_{patch}}{2}\cos^2\frac{kd}{2} + \cos kd + j\frac{\sin kd}{2}(\frac{Z_{branch}Y_0 + Z_0Y_{patch}}{Z_0Y_0}) \tag{3.15}$$

It should be noted that α is zero for a nonattenuating, propagating wave in a periodic structure.

Figure 3.9 shows the dispersion diagram using equation (3.15) for the unit cell of the AI-EBG structure in Figure 3.7. As shown in Figure 3.9, the dispersion diagram consists of alternating passbands and stopbands. In this dispersion diagram, the first mode is a slow-wave TM mode that is tightly bound to the surface [28]. It starts as a forward propagating TEM mode at very low frequency, and transits to a forward propagating TM surface wave. The group velocity ($d\omega/d\beta$) of this mode is positive and its phase velocity (ω/β) is much less than the speed of light, which indicates that this mode is forward propagating as a slow-wave. The second mode is a backward mode since it has a negative group velocity. The third mode is a forward propagating wave. In the dispersion diagram, the AI-EBG structure like other periodic structures supports slow-wave propagation and has passband and stopband characteristics similar to those of filters.

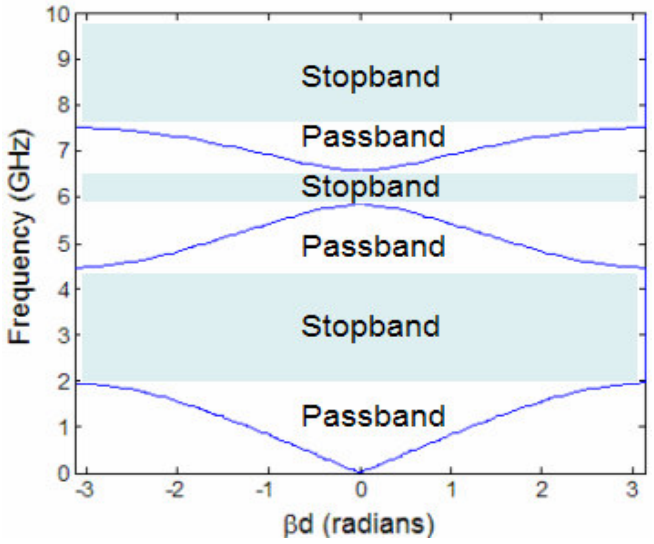


Figure 3.9 Dispersion diagram of the AI-EBG structure using transmission line network (TLN) method.

3.7 Cutoff Frequency of AI-EBG Structure

Since the AI-EBG structure is a low pass filter, it is more important to know cutoff frequency rather than the stopband center frequency in practical applications. The cutoff frequency is defined as the frequency at which the stopband starts. In this section, the AI-EBG structure was studied to obtain the cutoff frequency using the image parameter method. The image parameter method involves the specification of passband and stopband characteristics for a cascade of two port networks [48].

Figure 3.10 shows an arbitrary two port network specified by its ABCD parameters. The image impedance Z_{i1} is defined as the input impedance at port 1 when port 2 is terminated with Z_{i2} and the image impedance Z_{i2} is defined as the input impedance at port 2 when port 1 is terminated with Z_{i1}.

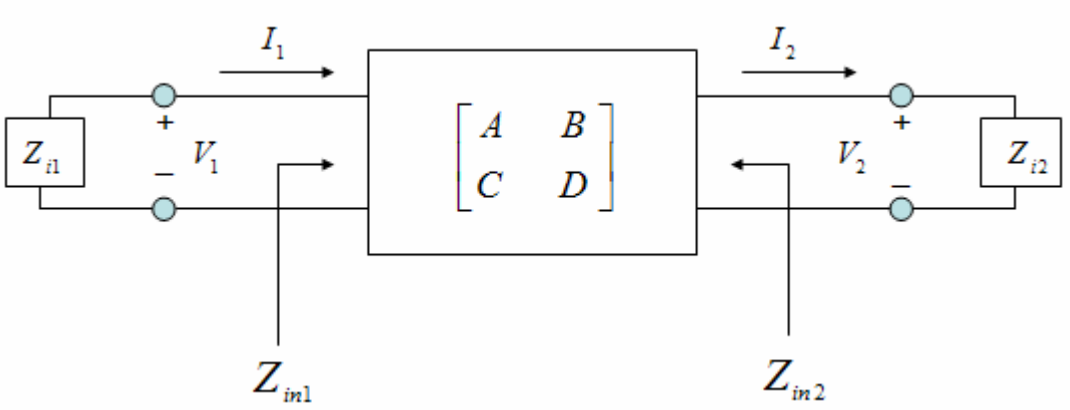


Figure 3.10 Arbitrary two port network with its image impedances.

The port voltages and currents in Figure 3.10 are related as

$$\begin{aligned} V_1 &= AV_2 + BI_2, \\ I_1 &= CV_2 + DI_2. \end{aligned} \tag{3.16}$$

The input impedance at port 1, with port 2 terminated with Z_{i2}, is given by

$$Z_{in1} = \frac{V_1}{I_1} = \frac{AV_2 + BI_2}{CV_2 + DI_2} = \frac{AZ_{i2} + B}{CZ_{i2} + D} \tag{3.17}$$

Using $AD - BC = 1$ for a reciprocal network, we get

$$\begin{aligned} V_2 &= DV_1 - BI_1, \\ I_2 &= -CV_1 + AI_1. \end{aligned} \tag{3.18}$$

The input impedance at port 2, with port 1 terminated with Z_{i1}, can be obtained as

$$Z_{in2} = -\frac{V_2}{I_2} = -\frac{DV_1 - BI_1}{-CV_1 + AI_1} = \frac{B + DZ_{i1}}{A + CZ_{i1}} \tag{3.19}$$

In this case, $Z_{in1} = Z_{i1}$ and $Z_{in2} = Z_{i2}$ are desired. From equations (3.17) and (3.19), we have the following equations:

$$\begin{aligned} Z_{i1}(CZ_{i2} + D) &= AZ_{i2} + B, \\ Z_{i1}D - B &= Z_{i2}(A - CZ_{i1}). \end{aligned} \tag{3.20}$$

Solving for image impedances, we have

$$\begin{aligned} Z_{i1} &= \sqrt{\frac{AB}{CD}}, \\ Z_{i2} &= \sqrt{\frac{BD}{AC}}. \end{aligned} \tag{3.21}$$

If the network is symmetric, then $A = D$. In this case, equation (3.21) becomes

$$Z_{i1} = Z_{i2} = \sqrt{\frac{B}{C}}. \tag{3.22}$$

The equivalent T-type circuit of the one dimensional (1-D) AI-EBG structure is shown in Figure 3.11. This circuit is a low pass filter network since the series inductors and shunt capacitor tend to block high frequency signals while passing low frequency

signals. If we let $Z_1 = j\omega L_{branch}$ and $Z_2 = \frac{1}{j\omega C_{patch}}$, then we have the following *ABCD* parameters for the equivalent T-type circuit of the one dimensional (1-D) AI-EBG structure in Figure 3.11:

$$\begin{aligned} A &= 1 + \frac{Z_1}{2Z_2}, \\ B &= Z_1 + \frac{Z_1^2}{4Z_2}, \\ C &= \frac{1}{Z_2}, \\ D &= 1 + \frac{Z_1}{2Z_2}. \end{aligned} \tag{3.23}$$

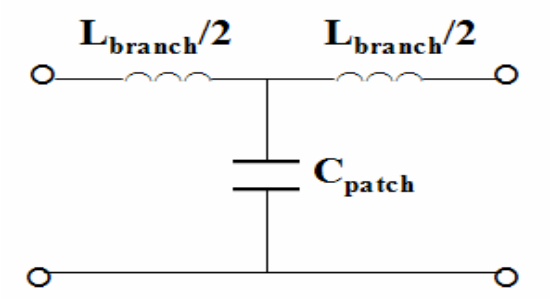


Figure 3.11 Equivalent circuit of 1-D AI-EBG Structure.

The image impedance of the equivalent T-type circuit of the one dimensional (1-D) AI-EBG structure is given by

$$Z_i = \sqrt{\frac{AB}{CD}} = \sqrt{\frac{B}{C}} = \sqrt{Z_1 Z_2}\sqrt{1+\frac{Z_1}{4Z_2}} = \sqrt{\frac{L_{branch}}{C_{patch}}}\sqrt{1-\frac{\omega^2 L_{branch} C_{patch}}{4}} \tag{3.24}$$

The cutoff frequency of the AI-EBG structure in Figure 3.11 is defined as

$$f_{cutoff} = \frac{1}{\pi\sqrt{L_{branch}C_{patch}}} \tag{3.25}$$

In the above equation, $L_{branch}(nH) \cong 2\cdot 10^{-4}\cdot l_s \cdot \left[\ln(\frac{l_s}{w_s+t}) + 1.193 + 0.2235\cdot(\frac{w_s+t}{l_s})\right]\cdot K_g$ is the inductance of the metal branch in the AI-EBG structure [66], l_s, w, and t represent the length, width, and thickness in μm of the metal branch. K_g is a correction factor taking the effect of a ground plane with a distance h away from the metal branch. K_g is given by the following equation.

$$K_g = 0.57 - 0.145\ln\frac{w_s}{h}, \qquad \frac{w_s}{h} \rangle 0.05 \tag{3.26}$$

$C_{patch} = \varepsilon_0\varepsilon_r\frac{A}{h}$ is the capacitance by the metal patch on the top metal layer and

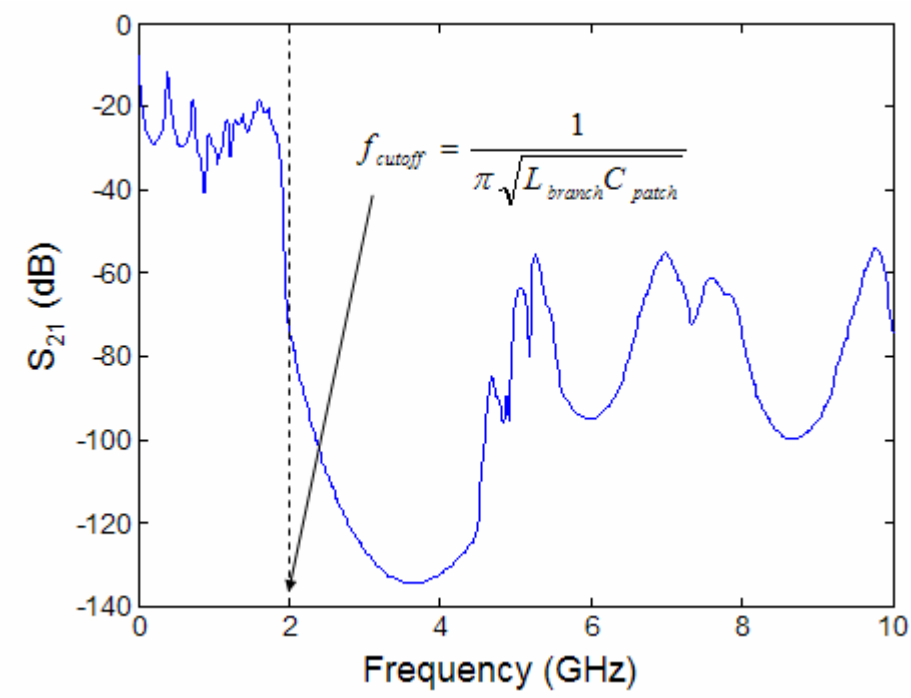


Figure 3.12 Cutoff frequency of the AI-EBG structure in Figure 4.2 (a) with S_{21} simulation result in Figure 4.2 (b).

corresponding solid plane on the bottom metal layer. ε_o is the permittivity of free space, ε_r is the relative permittivity of the dielectric, *A* is the area of the metal patch, and *h* is the dielectric thickness.

Using equation (3.25) for the AI-EBG structure in Figure 4.2 (a), f_{cutoff} is calculated as 2.03 GHz, which is quite well correlated with the simulation results in Figure 4.2 (b). In Figure 3.12, f_{cutoff} is shown in S_{21} simulation result for the AI-EBG structure in Figure 4.2 (b). In Table 3.1, the cutoff frequencies of the AI-EBG structures in Figure 4.7 are shown using equation (3.25). These cutoff frequencies using equation (3.25) are well correlated with the measurement results in Figure 4.7. The equation (3.25) will be used to explain the behavior of the AI-EBG structure when some parameters of the AI-EBG structure are changed in Chapter 4.

Table 3.1 Cutoff frequencies of the AI-EBG structures in Figure 4.7

AI-EBG Structures	Cutoff frequency
Metal patch size (1.5 cm x 1.5 cm) and metal branch size (0.1 cm x 0.1 cm)	2.03 GHz
Metal patch size (1..0 cm x 1.0 cm) and metal branch size (0.1 cm x 0.1 cm)	3.31 GHz
Metal patch size (0.7 cm x 0.7 cm) and metal branch size (0.1 cm x 0.1 cm)	5.18 GHz

3.8 Summary

In this chapter, theoretical analysis of the AI-EBG structure was shown using the Brillouin zone concept. First, the reciprocal space concept was introduced to understand the Brillouin zone. Second, it was shown how the Brillouin zone was constructed in the reciprocal lattice. Third, the equation to estimate the stopband center frequency of the AI-EBG structure was driven using the Brillouin zone concept. Fourth, the propagation characteristics of the AI-EBG structure was analyzed using the transmission line network method. Finally, the cutoff frequency of the AI-EBG structure was obtained using image parameter method. The cutoff frequency formula of the AI-EBG structure was obtained using the image parameter method and can be used for fast design process.

CHAPTER 4

Modeling and Analysis of AI-EBG Structure

This chapter describes the modeling, simulation, measurement and analysis of a novel electromagnetic bandgap (EBG) structure called the alternating impedance EBG (AI-EBG) structure for noise isolation and suppression in mixed-signal systems.

The AI-EBG structure was introduced in Chapter 3 and theoretical analysis of the AI-EBG structure was demonstrated in Chapter 3. In this chapter, the modeling, simulation, and measurement of the AI-EBG structure are shown to prove the excellent isolation property of the AI-EBG structure. First, the AI-EBG structure showed excellent isolation (-80 dB ~ -140 dB) through simulations and measurements. This was possible since the AI-EBG structure was optimized to ensure maximum wave destructive interference, which results in excellent isolation in the stopband frequency range. Second, the modeling and simulation methodology for the AI-EBG structure were proposed for efficient simulation using TMM. It is necessary to extend the basic model described in section 2.2 with circuit models for edge and gap effects. It is critical to model these effects to obtain accurate bandwidth and isolation levels in S parameter simulation. The equivalent circuit for the AI-EBG structure with these effects is also shown. Various AI-EBG structures have been designed, fabricated, and model-to-hardware correlation is demonstrated in this chapter. Finally, various simulations are performed to see the change of isolation level and the change of stopband frequency range by varying various parameters such as dielectric constant and metal patch size. The information through these simulations can be used for various applications that require the AI-EBG structure.

4.1 Modeling and simulation of AI-EBG Structure

This section describes the modeling of the EBG structure for extracting the S-parameters and computing voltage distributions. Full-wave EM solvers can be used to analyze EBG structures, but they are computationally expensive due to the grid size required. So, there is a need for efficient methods for modeling EBG structures with reasonable simulation time and good accuracy. The transmission matrix method (TMM) is a good candidate for analyzing the AI-EBG structure since it has been successfully applied to complex power delivery network [40]-[42]. The good model to hardware correlation for a realistic PDN in packages and boards was verified in [12].

In order to increase accuracy of the simulation, it is necessary to extend the basic model described in section 2.2 with circuit models for edge and gap effects. It is critical to model these effects to obtain accurate bandwidth and isolation levels in S parameter simulation. Edge effects can be modeled by adding an *LC* network to all the edges of the AI-EBG structure to model the fringing fields. The total capacitance (C_T) including fringing capacitance (C_f) for the edge cells of the AI-EBG structure can be calculated by employing the empirical formula for the per unit length capacitance of a microstrip line described in [66] given by:

$$C_T = \varepsilon_{eff}\left[\left(\frac{W}{d}\right)+0.77+1.06\left(\frac{W}{d}\right)^{0.25}+1.06\left(\frac{t}{h}\right)^{0.5}\right], \tag{4.1}$$

where $\varepsilon_{eff} = \frac{\varepsilon_r+1}{2}+\frac{\varepsilon_r-1}{2}\frac{1}{\sqrt{1+\frac{12d}{W}}}$ is the effective dielectric constant in [18], W is the metal line width, d is the dielectric thickness and t is the metal thickness. In (4.1), the first

term is for the parallel-plate capacitance, and the other three terms in (4.1) account for fringing capacitance. In order to maintain a physical phase velocity, the per unit length inductance must be reduced from the parallel-plate inductance in accordance with

$$\sqrt{LC} = \sqrt{\mu\varepsilon} \ . \qquad (4.2)$$

This reduction is accomplished by adding an inductance between two adjacent nodes on the edge of the AI-EBG structure. Gap coupling can be modeled by including a gap capacitance, C_g, between nodes across a gap in two metal patches in the AI-EBG structure. The gap capacitance was extracted from a 2-D solver such as Ansoft Maxwell™. For example, the gap capacitance per unit length extracted from Ansoft Maxwell™ for the AI-EBG structure in Figure 4.2 (a) was 5.5 pF/m. Figure 3.5 shows the updated equivalent ∏ circuit for the unit cell including fringing and gap capacitances. It is important to note that the locations of the fringing and gap capacitances in the unit cell depend on the location of the unit cell in the AI-EBG structure. Once the unit cell

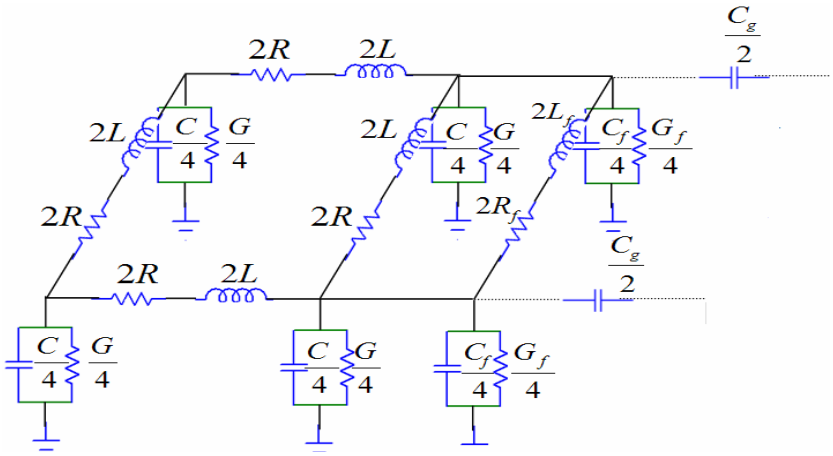
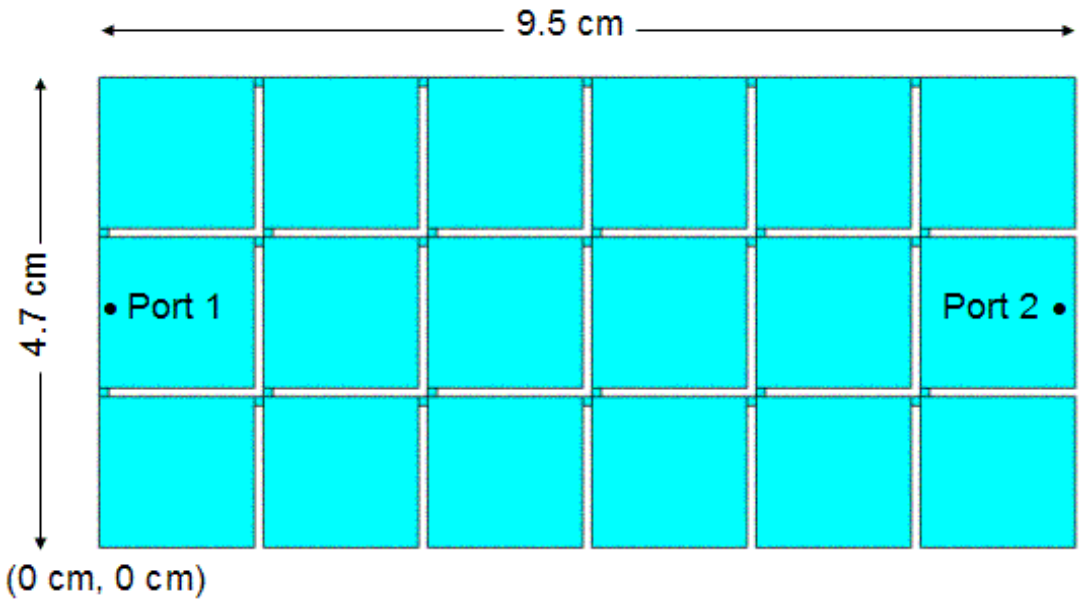


Figure 4.1 Equivalent ∏ circuit model for the unit cell including fringing and gap effects.

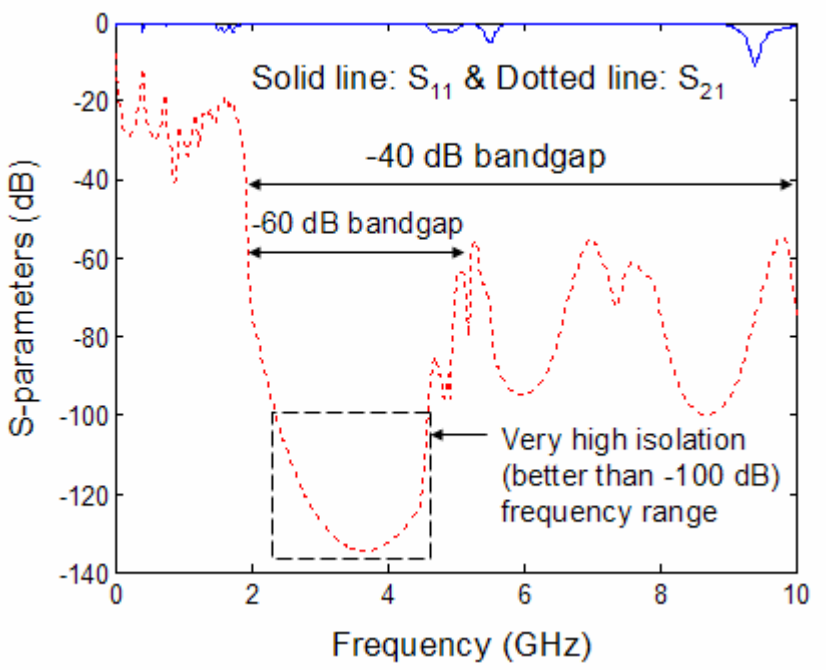
equivalent circuits are available, these are converted to ABCD matrices and efficiently solved using TMM [40]-[42]. This formulation was developed by Krishna Bharath and Dr. Ege Engin who are part of the EPSILON group at Georgia Tech [79].

The test structure used to verify the model was a two metal layer board with size 9.5 cm by 4.7 cm. In this example, the size of the metal patch was 1.5 cm x 1.5 cm and the size of the metal branch was 0.1 cm x 0.1 cm. The dielectric material of the board was FR4 with a relative permittivity, ε_r = 4.4, the conductor was copper with conductivity σ_c = 5.8 x 10^7 S/m, and dielectric loss tangent was *tan* (δ) = 0.02. The copper thickness for the power plane and the ground plane was 35 μm and the dielectric thickness was 2 mils. A unit cell size of 0.1 cm x 0.1 cm, which corresponds to an electrical size of λ/14.3 at 10 GHz, was used for approximating the structure. Port 1 was placed at (0.1 cm, 2.4 cm) and port 2 was located at (9.4 cm, 2.4 cm) with the origin (0 cm, 0 cm) lying at the bottom left corner of the structure, as shown in Figure 4.2 (a). The transmission coefficient between two ports, S_{21}, was computed by TMM and is shown in Figure 3.6 (b). This result shows an excellent stopband floor (-120 dB) and broad stopband (over 8 GHz for -40 dB bandgap).

It is important to visualize the voltage distribution within the AI-EBG structure in a mixed-signal system where sensitive RF circuits and noisy digital circuits exist together. The main purpose of this analysis is to see that noise generated by digital circuits cannot propagate to RF circuits at stopband frequencies. In this analysis, assume that noisy digital circuits are located at port 1 and sensitive RF circuits are located at port 2. TMM was also used to obtain the voltage variation on the AI-EBG structure in Figure



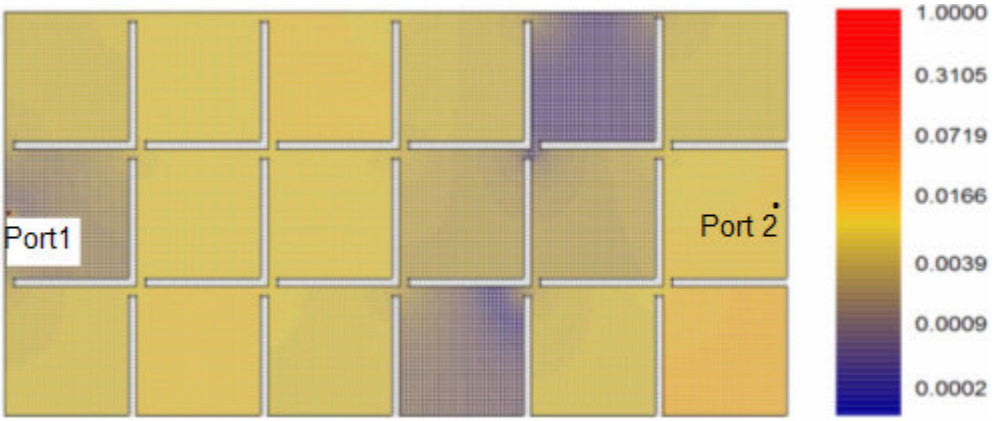
(a)



(b)

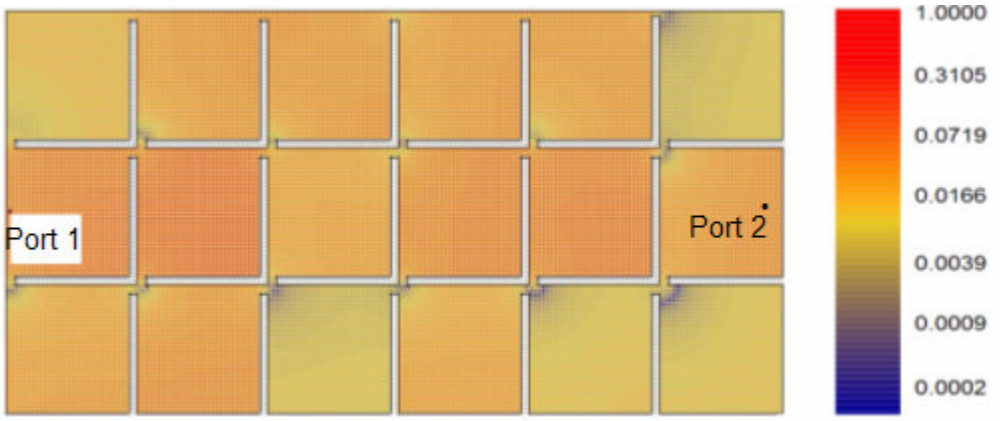
Figure 4.2 (a) Schematic of the simulated AI-EBG structure and (b) Simulated results of S-parameters for the AI-EBG structure in (a).

4.2 (a). First, the transfer impedances from the input port to all locations on the power/ground planes were computed using TMM. Then, a 10 mA current source was applied between the power and ground planes on the input port that is a port 1 in Figure 4.2 (a) to get the voltage distribution across the AI-EBG structure. Figure 4.3 (a) ~ (d) are the simulated color scale voltage magnitude distributions on the AI-EBG structure at 500 MHz, 1.5 GHz, 4 GHz and 7 GHz. The voltage variation is represented by a color contrast in these figures. The unit in the color bars in Figure 4.3 is [V]. Figure 4.3 (a) shows that the AI-EBG structure does not provide good isolation at 500 MHz since 500 MHz is a frequency in passband. Figure 4.3 (b) shows the voltage distribution on the AI-EBG structure at 1.5 GHz, which is a frequency in the passband. In contrast, a voltage distribution in Figure 4.3 (c) shows good isolation since voltage variation is observed only in few metal patches around the metal patch containing port 1. This frequency, 4 GHz, corresponds to the stopband frequency in the first stopband of the AI-EBG structure



(a)

Figure 4.3 Simulated voltage magnitude distributions on the AI-EBG structure at different frequencies (a) At 500 MHz, (b) At 1.5 GHz, (c) At 4 GHz, and (d) At 7 GHz.



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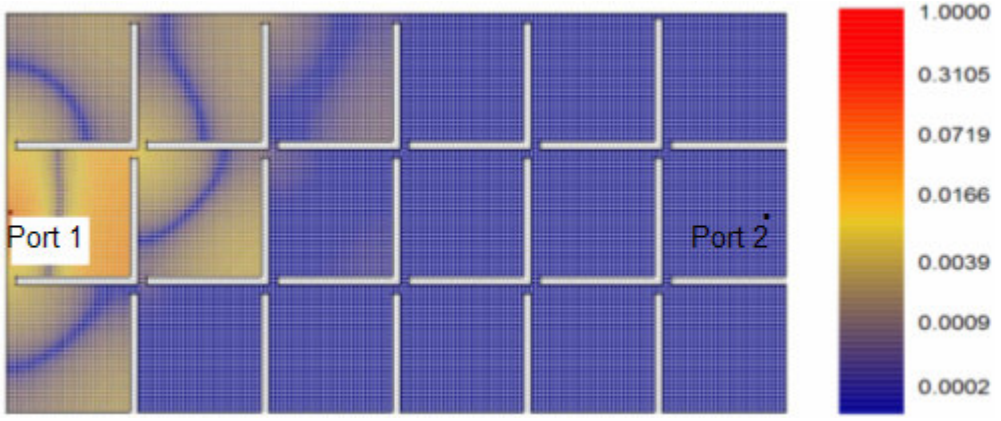
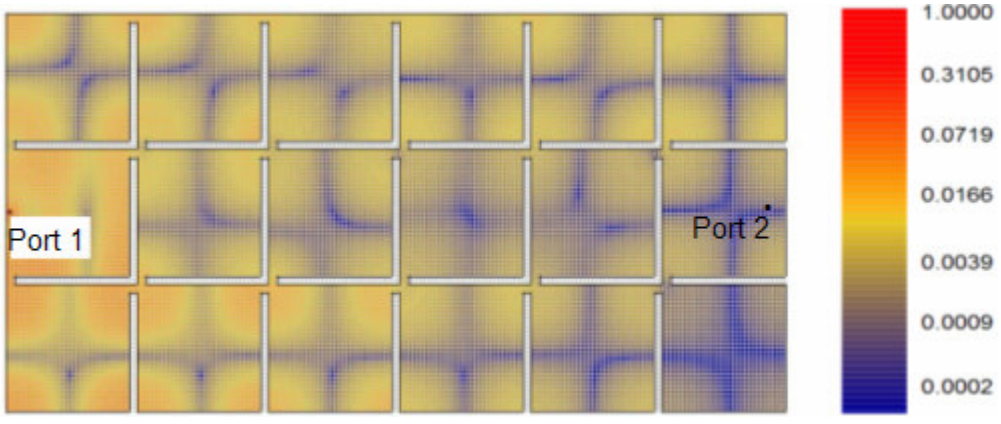


(c)



(d)

Figure 4.3 Simulated voltage magnitude distributions on the AI-EBG structure at different frequencies (a) At 500 MHz, (b) At 1.5 GHz, (c) At 4 GHz, and (d) At 7 GHz.

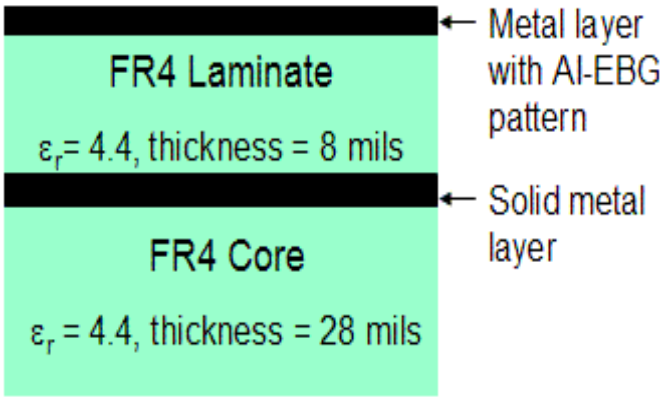
in Figure 4.2 (b). It is important to note that noise generated by the current source on the input port can not propagate to the metal patches in the fourth, fifth, sixth columns in the AI-EBG structure at 4 GHz, which means that noise generated by digital circuits cannot propagate to the RF circuits located at port 2 in Figure 4.2 (a). Finally, voltage variation across the whole AI-EBG structure is again observed at 7 GHz as can be seen in Figure 4.3 (d), which represents the passband.

4.2 Model-to-hardware correlation

To verify the simulated results, the EBG structures discussed in the previous section were fabricated using standard PCB processes. Figure 4.4 (a) shows the cross section of the fabricated structure. The top layer is a metal layer with AI-EBG pattern and second metal layer is a continuous solid plane. The dielectric material between these two metal layers is FR4 with a relative permittivity $\varepsilon_r = 4.4$. The conductor is copper with conductivity $\sigma_c = 5.8 \times 10^7$ S/m, and a dielectric loss tangent is $tan(\delta) = 0.02$. The bottom layer is an FR4 core layer for mechanical support.

The S-parameter measurements were carried out using an Agilent 8720 ES vector network analyzer (VNA). Figure 4.5 shows S-parameter results for one of the fabricated AI-EBG structures. In this case, the size of the metal patch was 1.5 cm x 1.5 cm and the size of the metal branches was 0.3 mm x 0.3 mm. The entire structure size was 9.15 cm x 4.56 cm. The return loss, S_{11}, is almost 0 dB in the stopband, in Figure 4.5, which shows the excellent isolation property of the AI-EBG structure. The measured S_{21} shows a very deep and wide bandgap (over 8 GHz for -40 dB bandgap) and S_{21} reached the sensitivity

limit (-80 dB ~ -100 dB) of the VNA used in the frequency range from 2.2 GHz to 4.5 GHz. The modeling results were compared with measurement result in Figure 4.6, which shows reasonable agreement. The discrepancy between modeling and measurement is due to the sensitivity limit of the VNA in the stopband. The other reason for this



(a)

(b)

Figure 4.4 Fabrication of AI-EBG structure (a) Cross section of fabricated AI-EBG structure and (b) Photo of fabricated AI-EBG structure.

discrepancy is due to fabrication process error. This is because the fabrication process error can change the width of the metal branch in the AI-EBG structure and this change can cause a shift of S_{21} curve.

To see frequency tunability of the AI-EBG structure, the EBG structures having different metal patch sizes were designed and fabricated using a standard PCB process. However, a metal branch size of 0.1 cm x 0.1 cm was used for all cases. Figure 4.7 shows the photographs of fabricated EBG structures and corresponding S-parameter measurement results. The dashed area in Figure 4.7 represents the frequency range of the first stopband in the AI-EBG structure. Port 1 and port 2 locations are also shown in Figure 4.7. In Figure 4.7, the dispersion diagrams of the AI-EBG structures using transmission line network (TLN) method are also shown. It is important to note that as the size of the metal patch decreases, the stopband occurs at higher frequency range since the cutoff frequency is inversely proportional to the capacitance of the metal patch by equation (3.25). This will be discussed in the next section in detail.

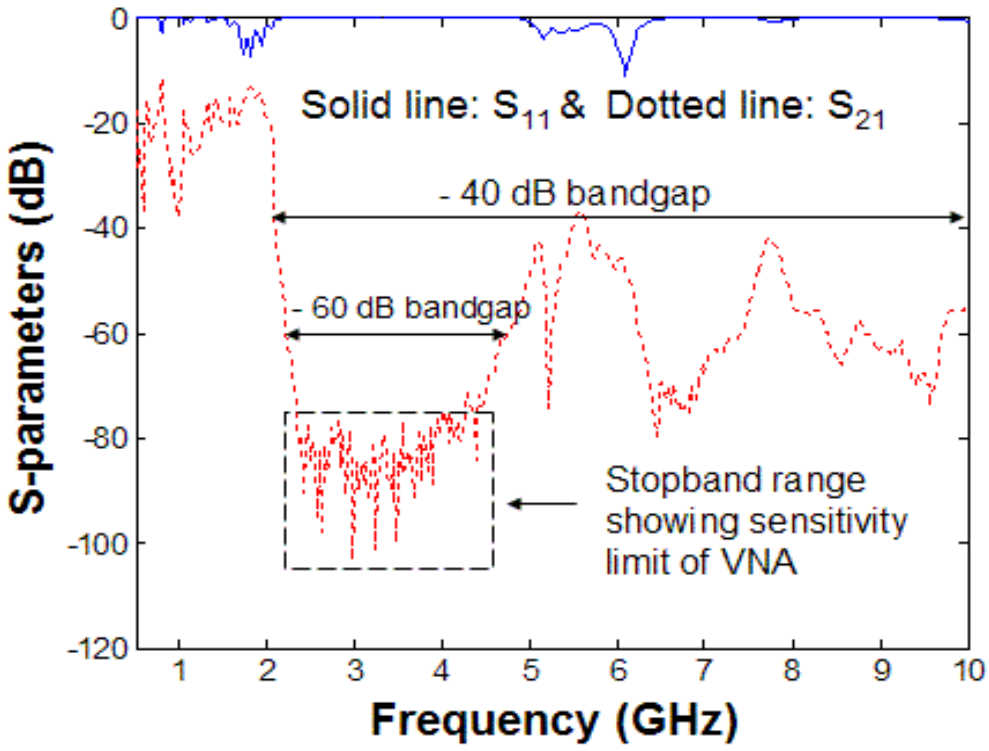


Figure 4.5 Measured S-parameters of the AI-EBG structure.

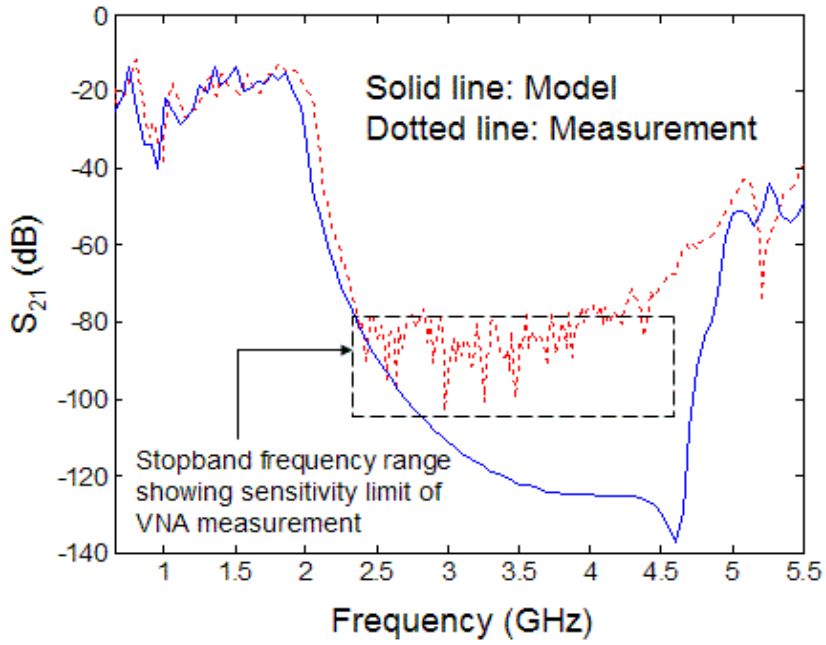
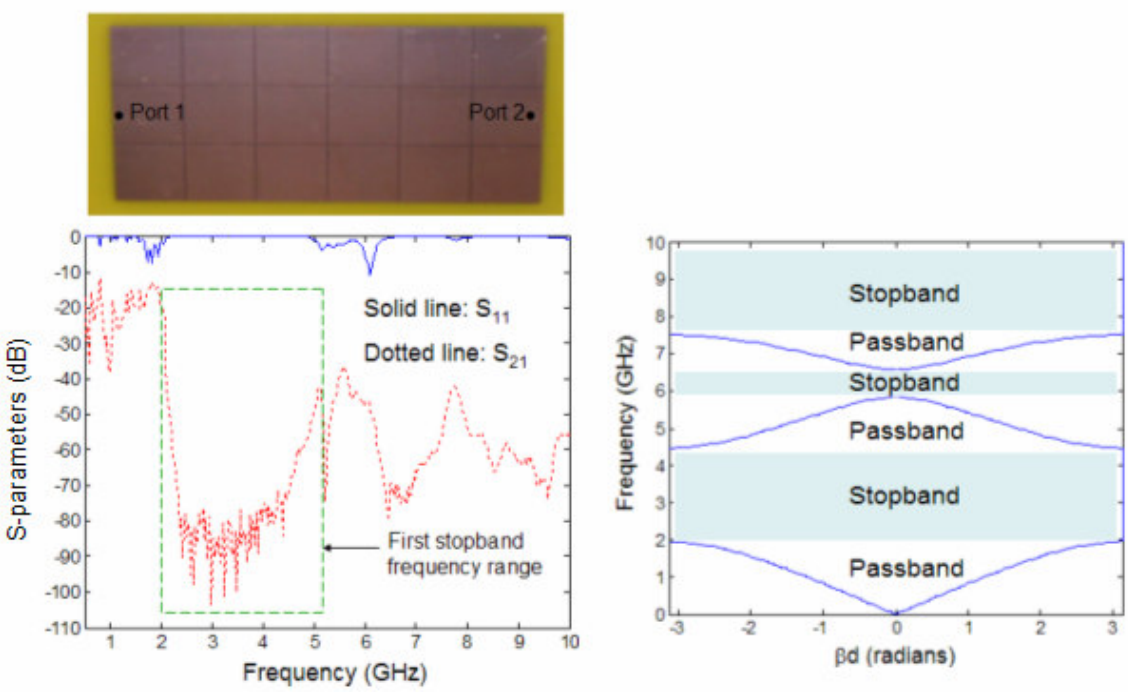
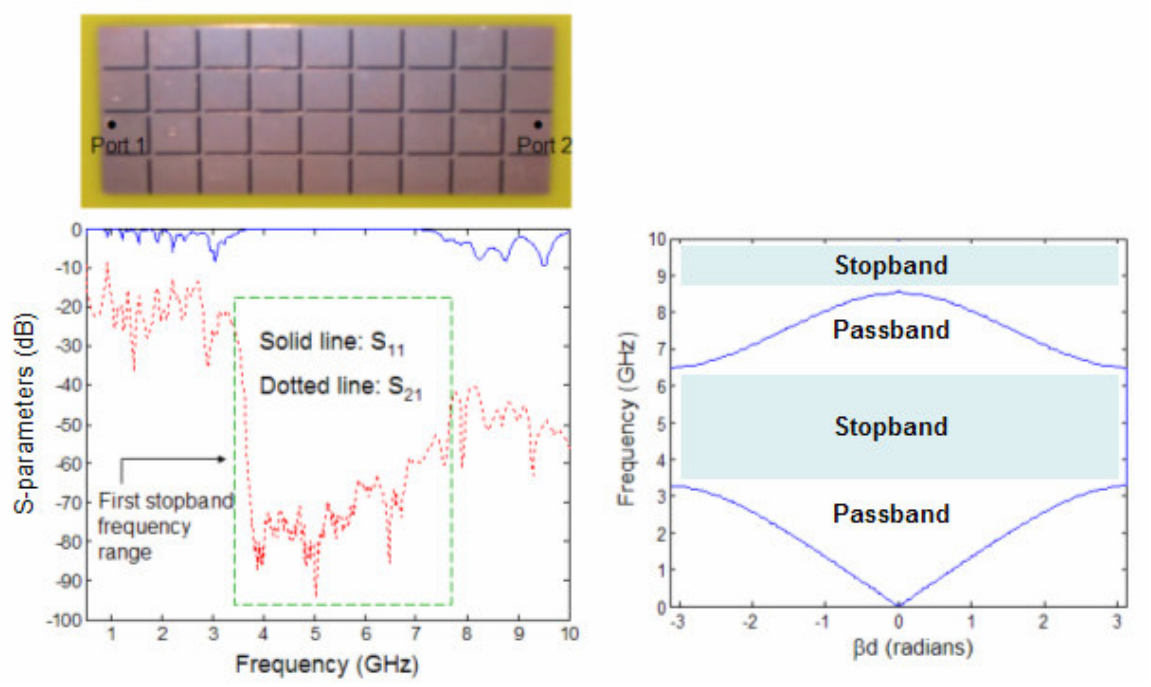


Figure 4.6 Model-to-hardware correlation for the AI-EBG structure.



(a)

Figure 4.7 S-parameter measurements: frequency tunability (a) AI-EBG structure with the metal patch size of 1.5 cm x 1.5 cm, (b) AI-EBG structure with the metal patch size of 1.0 cm x 1.0 cm, and (c) AI-EBG structure with the metal patch size of 0.7 cm x 0.7 cm.



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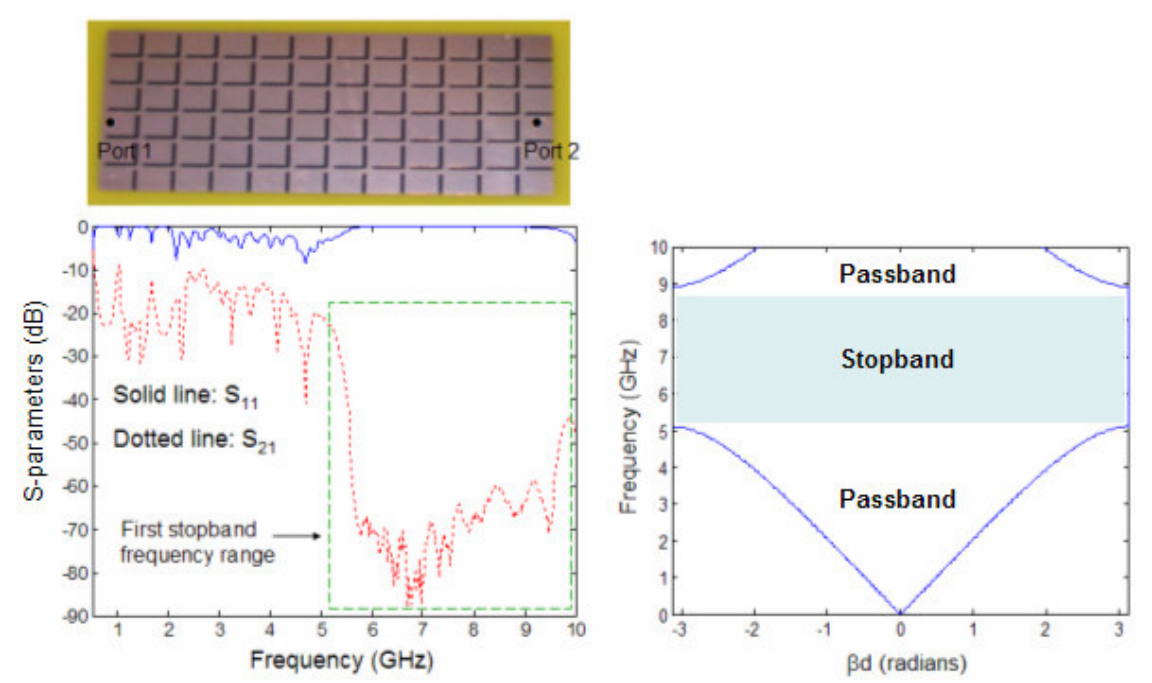


(c)

Figure 4.7 S-parameter measurements: frequency tunability (a) AI-EBG structure with the metal patch size of 1.5 cm x 1.5 cm, (b) AI-EBG structure with the metal patch size of 1.0 cm x 1.0 cm, and (c) AI-EBG structure with the metal patch size of 0.7 cm x 0.7 cm.

4.3 Parametric analysis of AI-EBG structure

This section describes the effect of critical parameters on stopband frequency and isolation levels in achievable AI-EBG structure using simulations. It is important to note that certain geometrical and material parameters can change the characteristics of the AI-EBG structure significantly.

4.3.1 Effect of metal patch size

The first parameter to be studied is the metal patch size of the AI-EBG structure. The metal patch size was changed to see the effect on the transmission coefficient (S_{21}). Figure 4.8 shows the S_{21} results for the different stopband ranges, which demonstrates the frequency tunability of the AI-EBG structure. For the first AI-EBG structure (AI-EBG 1) in Figure 4.8, the size of the metal patch was 1.0 cm x 1.0 cm and the size of the metal branch was 0.1 cm x 0.1 cm. The entire size of the AI-EBG 1 structure was 10.9 cm x 5.4 cm. For the second AI-EBG structure (AI-EBG 2) in Figure 4.8, the size of the metal patch was 0.7 cm x 0.7 cm and the size of the metal branch was 0.1 cm x 0.1 cm. The entire AI-EBG 2 structure size was 9.5 cm x 4.7 cm.

It is important to note that as the size of the metal patch decreases, the stopband occurs at higher frequency range since the cutoff frequency, which is a frequency at which stopband begins, is inversely proportional to the capacitance of the metal patch by the following equation.

$$f_{cutoff} \sim \frac{1}{\sqrt{L_{branch}\ C_{patch}}} \tag{4.3}$$

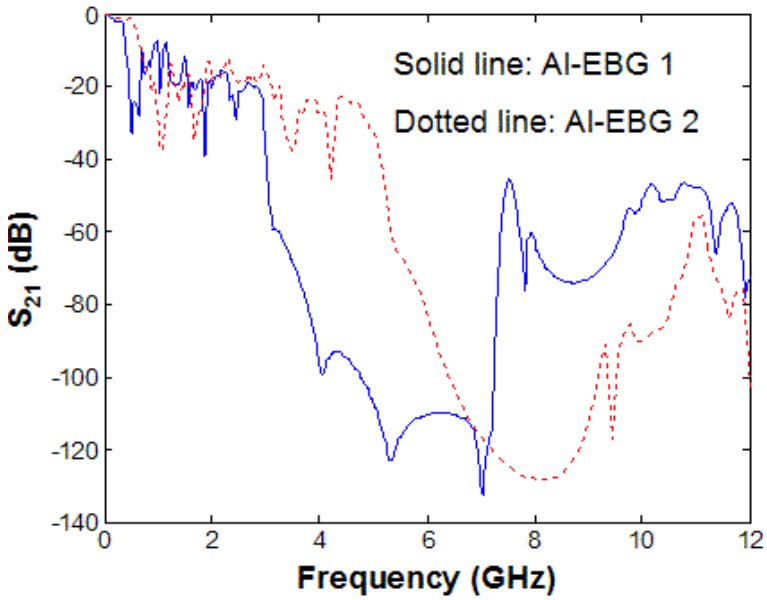


Figure 4.8 Effect of metal patch size in AI-EBG structure.

4.3.2 Effect of dielectric constant

The second parameter to be studied is the dielectric constant. The test structure used was a two metal layer board that is 9.5 cm by 4.7 cm in size. In this case, the size of the metal patch was 1.5 cm x 1.5 cm and the size of the metal branch was 0.1 cm x 0.1 cm. The dielectric material of the board was FR4 with a relative permittivity, $\varepsilon_r = 4.4$, the conductor was copper with conductivity, $\sigma_c = 5.8 \times 10^7$ S/m, and the dielectric loss tangent was $tan(\delta) = 0.02$. The copper thickness for the power plane and ground plane was 35 μm and the dielectric thickness was 4.5 mils. A unit cell size of 0.1 cm x 0.1 cm was chosen, which corresponds to an electrical size of $\lambda/14.3$ at 10 GHz.

Figure 4.9 shows the transmission coefficient when the dielectric constant is varied from 4.4 to 10 and from 4.4 to 2.2. All other geometrical parameters are fixed in this

simulation. When the dielectric constant increases, the cutoff frequency is shifted towards lower frequency. This decrease of the cutoff frequency is associated with the

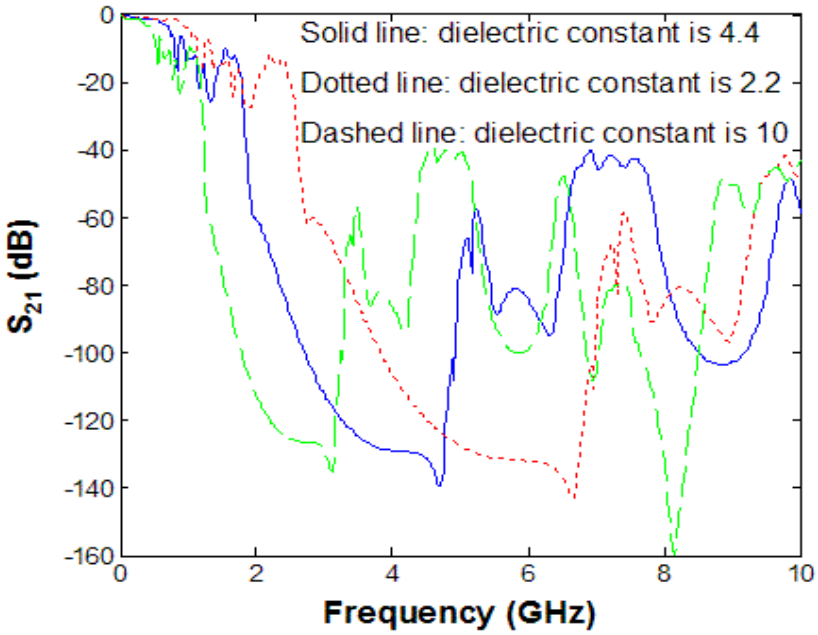


Figure 4.9 Effect of dielectric constant in AI-EBG structure.

increase in capacitance of the metal patch and branch since capacitance is proportional to the dielectric constant. The cutoff frequency is inversely proportional to capacitance. The bandwidth of the stopband decreases as the dielectric constant increases. This is because bandwidth of the stopband is inversely proportional to capacitance. The bandwidth (BW) of stopband is related to capacitance and inductance by the following equation [29].

$$BW \sim \sqrt{\frac{L}{C}} \tag{4.4}$$

Next, the dielectric constant was varied from 4.4 to 2.2. Figure 4.9 shows the simulated transmission coefficient when the dielectric constant is varied from 4.4 to 2.2. All other

geometrical parameters were fixed. When the dielectric constant decreases, the cutoff frequency is shifted towards higher frequency. This increase of the cutoff frequency is associated with the decrease of capacitance of the metal patch and branch since capacitance is proportional to dielectric constant and cutoff frequency is inversely proportional to capacitance. The bandwidth of the stopband increases as the dielectric constant decreases. This is because the bandwidth of the stopband is inversely proportional to capacitance through equation (4.3).

4.3.3 Effect of metal branch

The metal branch size was varied from 0.2 mm x 0.2 mm to 1 mm x 0.2 mm to see if there is any change in the frequency response. In this case, the test structure was a two metal layer board that was 10.08 cm by 4.02 cm in size and the size of the metal patch was 2 cm x 2 cm. The dielectric material of the board was FR4 with a relative permittivity $\varepsilon_r = 4.4$ and the dielectric loss tangent was $tan(\delta) = 0.02$. The conductor was copper with conductivity, $\sigma_c = 5.8 \times 10^7$ S/m. The copper thickness for the power plane and ground plane was 35 μm, and the dielectric thickness was 4.5 mils. A unit cell size of 0.2 mm x 0.2 mm was used in these simulations. The metal branch size was varied from 0.2 mm x 0.2 mm to 1 mm x 0.2 mm to see if there was any change in the frequency response. Figure 4.10 shows the simulated S_{21} for both cases.

When the metal branch size increases, the cutoff frequency is shifted towards lower frequency. This decrease of the cutoff frequency is associated with the increase of inductance of the metal branch since the cutoff frequency is inversely proportional to inductance. The bandwidth of the stopband increases as the metal branch size increases.

This is because the bandwidth of the stopband is proportional to inductance through equation (4.4).

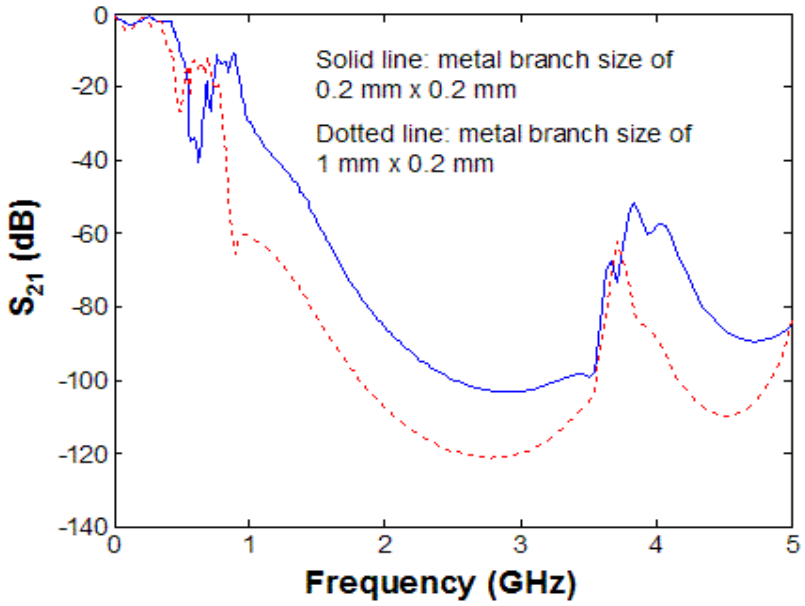


Figure 4.10 Effect of metal branch size in AI-EBG structure.

4.3.4 Effect of dielectric material

Three different dielectric materials were simulated to see the effect of dielectric material. Three different dielectric materials evaluated were FR4, liquid crystalline polymer (LCP), and high k material. The reason why these three dielectric materials were chosen is that FR4 is most common dielectric material for package and board, LCP has advantage of being stable and easy to fabricate in thin films, and high k material is a promising dielectric material for a compact high performance capacitor. The material characteristics of these three materials are summarized in Table 4.1.

Figure 4.11 shows the simulated transmission coefficient (S_{21}) for these three materials. The stopband for the high k material occurs at lower frequencies than the

stopbands of FR4 and LCP. This is because the dielectric constant of high k material is higher than that of FR4 and LCP and the cutoff frequency is inversely proportional to capacitance by equation (4.3).

Table 4.1 Material characteristics of three different dielectric materials

	FR4	LCP	High k material
Dielectric constant (ε_r)	4.4	2.9	16
Loss tangent (*tan d*)	0.02	0.002	0.006
Dielectric thickness (μm)	101.6	25.4	16

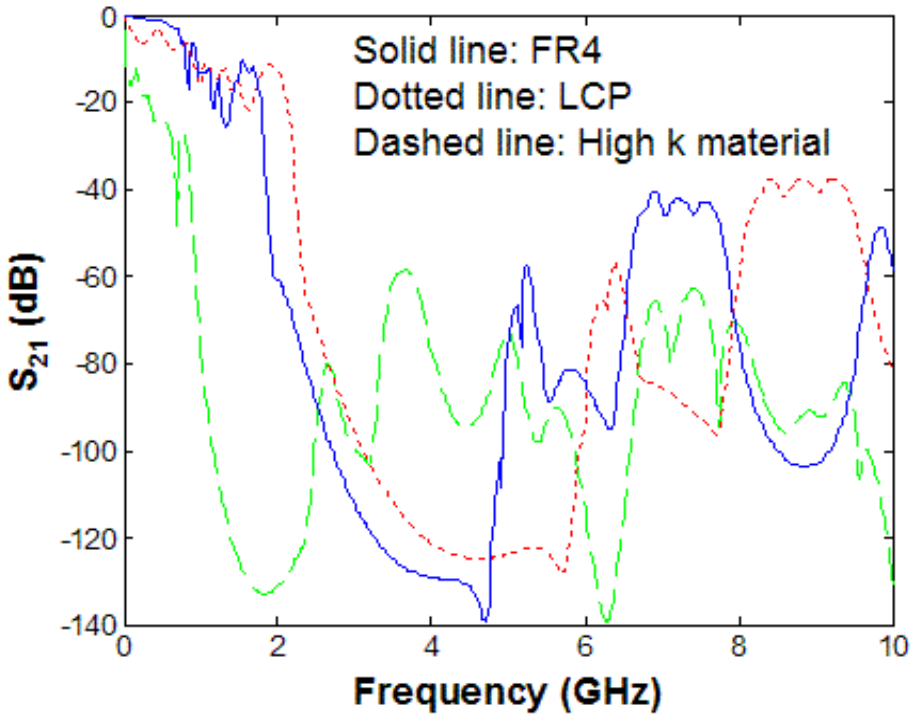


Figure 4.11 Effect of dielectric material in AI-EBG structure.

The bandwidth of stopband of high k material is smaller than that of FR4 and LCP since stopband bandwidth is inversely proportional to capacitance by equation (4.4). Hence, compared with FR4, high k material is proper for low and narrow frequency applications and LCP is better for ultra wide band (UWB) applications.

4.3.5 Effect of multiple-layers

To see the effects of multi-layers, LCP was chosen as the dielectric material. For comparison, three different cases were tested; a single plane pair, two plane pairs, and three plane pairs. The main purpose of this comparison was to investigate the possibility of getting better isolation from multiple-layer AI-EBG structures than a single plane pair AI-EBG structure. For a single plane pair, the size of the structure was 4.7 cm x 4.7 cm, the metal patch size was 1.5 cm x 1.5 cm and the metal branch size was 0.05 cm x 0.1 cm. Port 1 was located at (0.75 cm, 0.75 cm) and port 2 was located at (3.95 cm. 3.95 cm). For two plane pairs, the stack-up of planes is shown in Figure 4.12. The size of the structure, metal patch size and the metal branch size are the same as those of a single plane pair. Port 1 was located at (0.75 cm, 0.75 cm) on the top plane pair and port 2 was

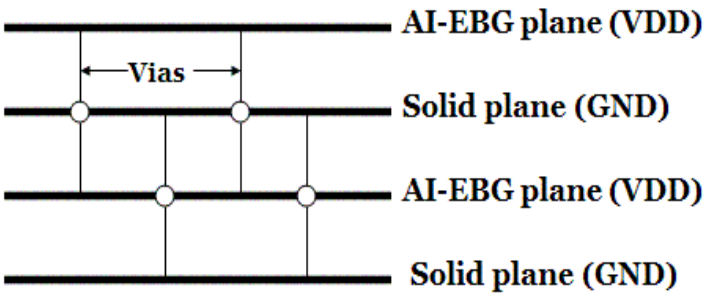


Figure 4.12 Cross-section of the two plane pairs.

located at (3.95 cm. 3.95 cm) on the bottom plane pair. Vias were vertically connected from voltage (VDD) plane to voltage plane and from ground (GND) plane to ground plane. This ensures that voltage planes and ground planes are at the same potential. For three plane pairs, the stack-up of planes is shown in Figure 4.13. The size of the structure, metal patch size and the metal branch size are the same as those of a single plane pair. Port 1 was located at (0.75 cm, 0.75 cm) on the top plane pair and port 2 was located at (3.95 cm. 3.95 cm) on the bottom plane pair. Figure 4.14 shows the transmission coefficient (S_{21}) for the three cases. As can be observed, there is an improvement in S_{21} as the stack-up of planes increases. However, the improvement in S_{21} is not significant. This is because destructive wave interference can be maximized in horizontal direction in the AI-EBG structures rather than in vertical direction since waves travel in power/ground planes horizontally and experience destructive interference.

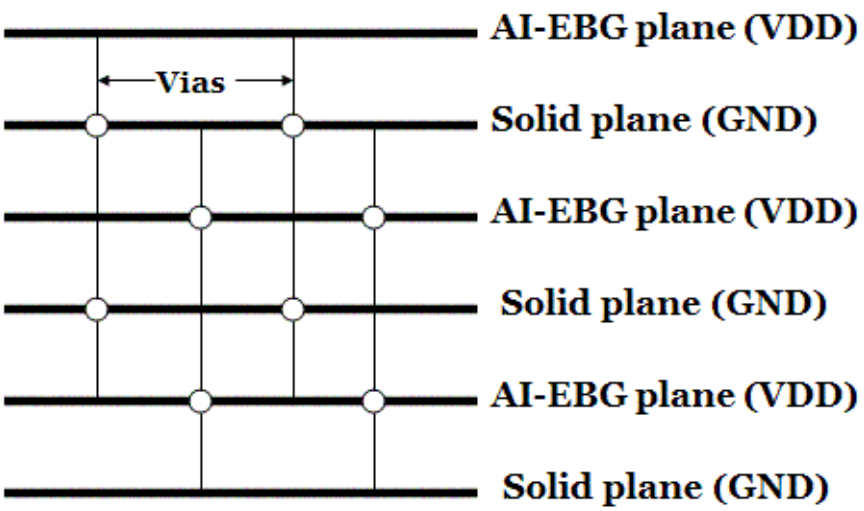


Figure 4.13 Cross-section of three plane pairs.

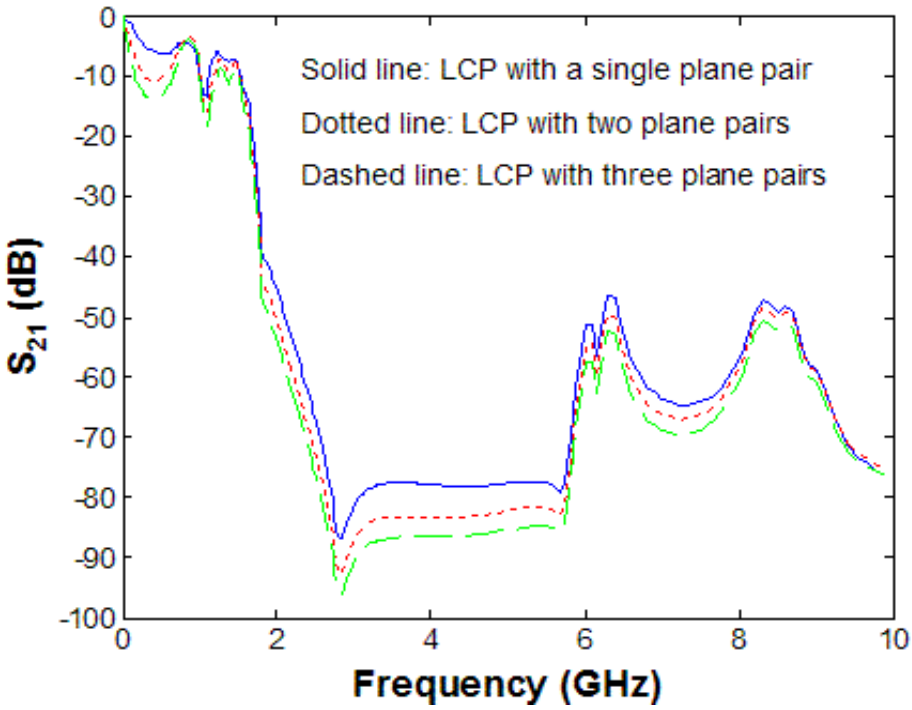


Figure 4.14 Effect of multi-layers in AI-EBG structure.

4.4 Summary

In this chapter, the modeling and analysis of the AI-EBG structure has been described. The AI-EBG structure showed excellent isolation (-80 dB ~ -140 dB) through simulations and measurements. This was possible since the AI-EBG structure was optimized to ensure maximum wave destructive interference, which results in excellent isolation in the stopband frequency range. The equivalent circuit for the AI-EBG structure is also shown. The modeling and simulation methodology for the AI-EBG structure were proposed for efficient simulation using TMM. Various AI-EBG structures were designed, fabricated, and model-to-hardware correlation was demonstrated in this chapter. Finally, various simulations were performed to see the change of isolation level

and the change of stopband frequency range by varying various parameters such as dielectric constant and metal patch size. The information through these simulations can be used for various applications that require the AI-EBG structure.

CHAPTER 5

Noise Suppression in Mixed-Signal Systems using AI-EBG Structure and Characterization of AI-EBG Structure

In this chapter, simulation, design, fabrication, and measurement of a mixed-signal test vehicle containing the AI-EBG structure in the power delivery network are presented. The results have been compared to a similar test vehicle with solid planes. First, the mixed-signal system simulations with and without the AI-EBG structure were performed in HP-ADS to see noise isolation levels available. The simulation results show that the proposed AI-EBG structure is a good candidate to suppress noise from digital circuits. Second, the AI-EBG structure has been integrated into a mixed-signal test vehicle to demonstrate the isolation levels achievable. The ability of the AI-EBG structure to suppress switching noise has been quantified in this chapter. The measurement results for the mixed-signal test vehicle with and without AI-EBG structure have shown that harmonic noise peaks due to digital circuits can be suppressed in the stopband frequency range using the AI-EBG structure.

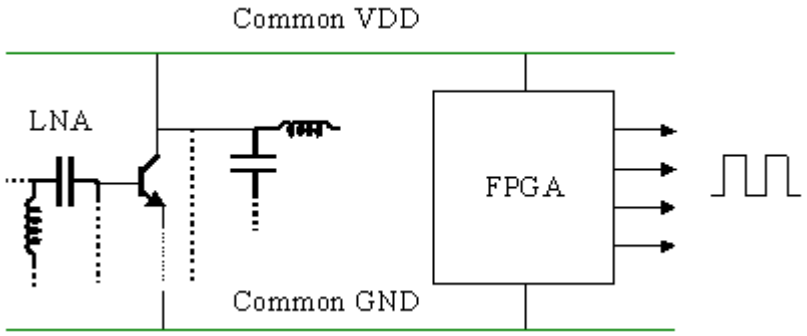
The power delivery network needs to function along with the signal lines for high-speed transmission. Since the power and ground planes carry the return currents for the signal transmission lines, the impact of AI-EBG structure on signal transmission

needs to be analyzed. First, time domain waveform measurements at the output of the FPGA and far end of the transmission line have been measured. Second, time domain reflectrometry (TDR) measurements have been measured and discussed to understand the discontinuities in the characteristic impedance profile due to the gaps in the AI-EBG plane. Third, near field and far field simulations and measurements have been discussed to understand possible electromagnetic interference (EMI). Finally, design methodology has been suggested to avoid any possible signal integrity and EMI problems when the AI-EBG structure is used as a part of the power distribution network in mixed-signal systems.

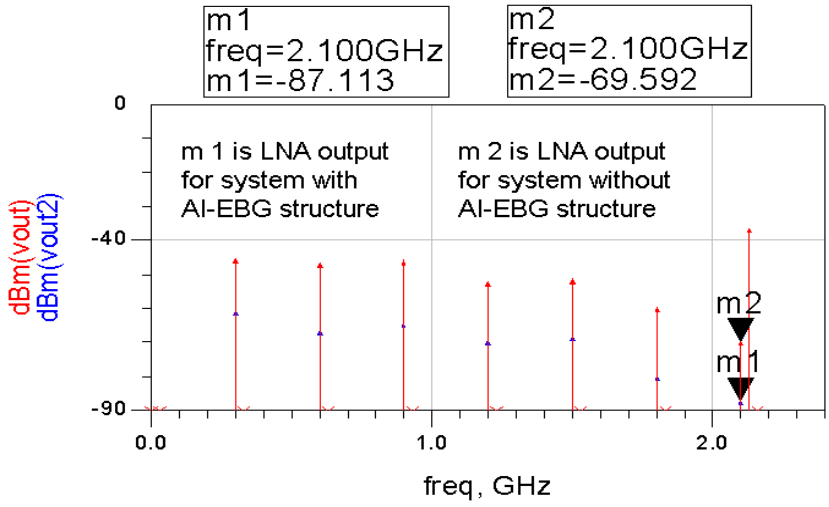
5.1 Mixed-Signal System Simulation

To study the actual reduction in noise obtained through the use of the AI-EBG based power supply scheme, power distribution networks consisting of a plane pair with and without the AI-EBG structure were modeled using TMM and used for system simulation in HP-ADS™. Figure 5.1 (a) shows the schematic of a test vehicle to study noise coupling in SOP-based mixed-signal systems. A common power distribution system is used for supplying power to a Field Programmable Gate Array (FPGA) driving a 300 MHz bus and a low noise amplifier (LNA) operating at 2.13 GHz. Noise generated in the digital subsystem couples to the LNA through the power rails. Sensitive devices such as a LNA are particularly susceptible to external noise since RF signals at the input of these devices have very low power and large signals appearing in band can make the active device to saturation, reducing its sensitivity. The use of the AI-EBG structure in the implementation of the power distribution system provides a cost-effective and

compact means for noise suppression, as compared to the use of split planes with multiple power supplies. Figure 5.1 (b) shows simulated LNA output spectrum (using



(a)



(b)

Figure 5.1. Mixed-signal system simulation. (a) Schematic of simulated mixed-signal system. (b) Simulation results for mixed-signal systems with and without the AI-EBG structure.

HP-ADS^{TM}), where the power distribution system has been implemented with and without the AI-EBG structure. It can be observed that the harmonics of the digital noise couple into the LNA circuitry and appear at its output in both cases. However, for the system with the AI-EBG based power scheme, there is significant reduction of the noise amplitudes. In particular, the 7th harmonic of the 300 MHz FPGA clock (at 2.1 GHz) lies close to the frequency of operation of the LNA. For the system without the AI-EBG based power scheme, the amplitude of this noise spike is -69.592 dBm. However, for the system with the AI-EBG structure, this harmonic noise peak has been suppressed to -87.113 dBm [53].

5.2 Design and Fabrication of Mixed-Signal Systems

To verify the use of the AI-EBG based scheme for mixed-signal noise suppression, a test vehicle containing an FPGA driving a 300 MHz bus with an integrated low noise amplifier (LNA) operating at 2.13 GHz was designed and fabricated on an FR4 based substrate. The LNA design was done by Dr.Vinu Govind [54], [55] in this mixed-signal system. Figure 5.2 shows the cross section of the fabricated mixed-signal test vehicle. The board is a three metal layer PCB that is 10.8 cm by 4.02 cm. The first metal layer is a signal layer, the second metal layer is a ground layer (Gnd), and the third metal layer is a power layer (Vdd). The AI-EBG structure was located on the ground layer in the test vehicle. The dielectric material in the PCB was FR4 with a relative permittivity, $\varepsilon_r = 4.4$ and dielectric loss tangent $tan(\delta) = 0.02$. The metallization used was copper with conductivity, $\sigma_c = 5.8 \times 10^7$ S/m. The dielectric thickness between metal layers was 5 mils with a bottom dielectric layer thickness of 28 mils. The bottom dielectric layer

was used for mechanical support. Figure 5.3 shows the photograph of the fabricated mixed-signal system containing the AI-EBG structure. The LNA was used as the noise sensor since it is the most sensitive device in an RF receiver. Noise generated in the FPGA couples to the LNA through the power distribution network. In the fabricated test vehicle, size of the metal patch and metal branch used in the EBG

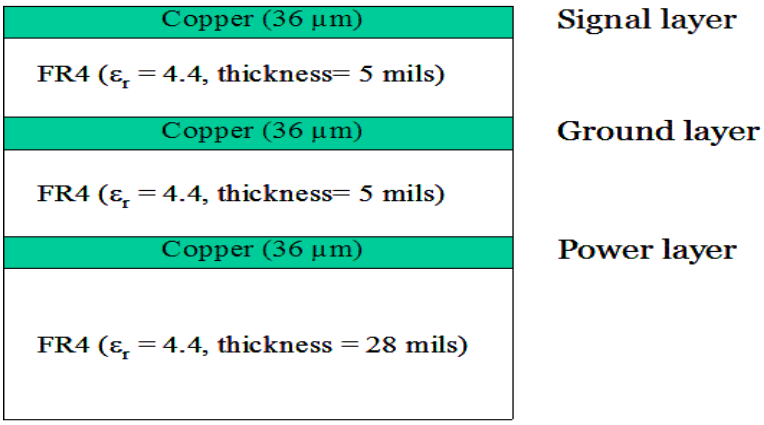


Figure 5.2 Cross-section of the fabricated mixed-signal systems.

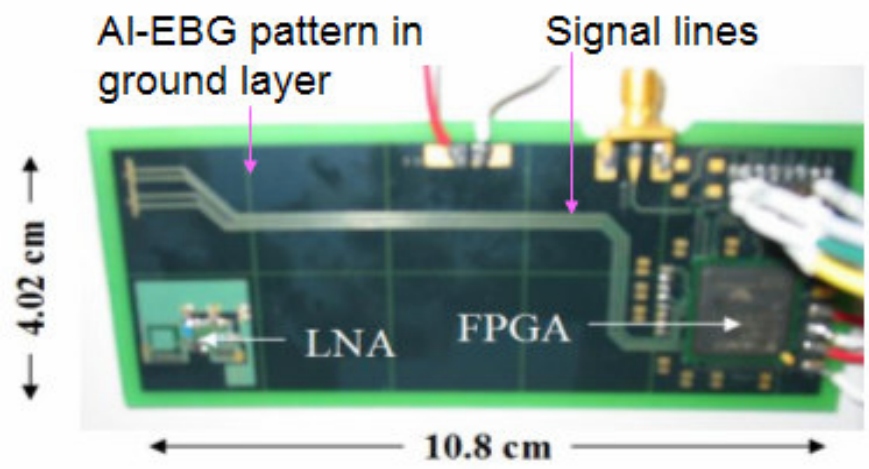


Figure 5.3 Photograph of the mixed-signal system containing the AI-EBG structure.

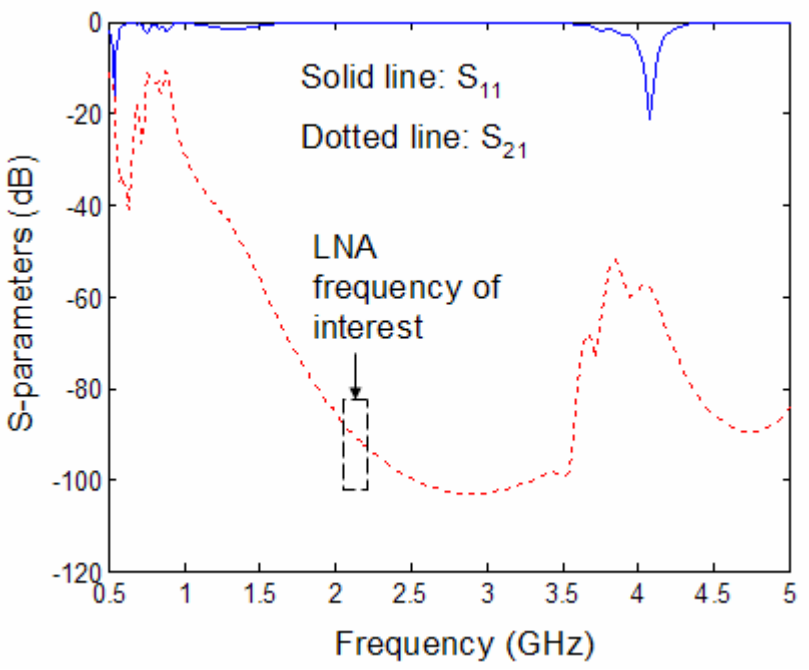


Figure 5.4 Simulated S-parameters for the AI-EBG based PDN.

Structure was 2 cm x 2 cm and 0.2 mm x 0.2 mm, respectively. Figure 5.4 shows the transmission coefficient (S_{21}) between FPGA and LNA, which was simulated using transmission matrix method (TMM). In Figure 5.4, S_{21} shows a very deep stopband (~-100 dB), which can be required to suppress harmonic noise peaks generated by the digital circuits in the FPGA.

5.3 Noise Measurements

Figure 5.5 shows the measurement set-up for noise measurements. The AI-EBG-based common power distribution system was used for supplying power (3.3 V) to the RF and FPGA ICs. For comparison, a test vehicle similar to Figure 5.3 was also fabricated without the AI-EBG structure. In the measurements, the FPGA was

programmed as four switching drivers using Xilinx software. The input terminal of the LNA was grounded to detect only noise from the FPGA through the PDN. The output terminal of the LNA was connected to a HP E4407B spectrum analyzer to observe noise from the FPGA. Sunanda Janagama worked together for this noise measurement.

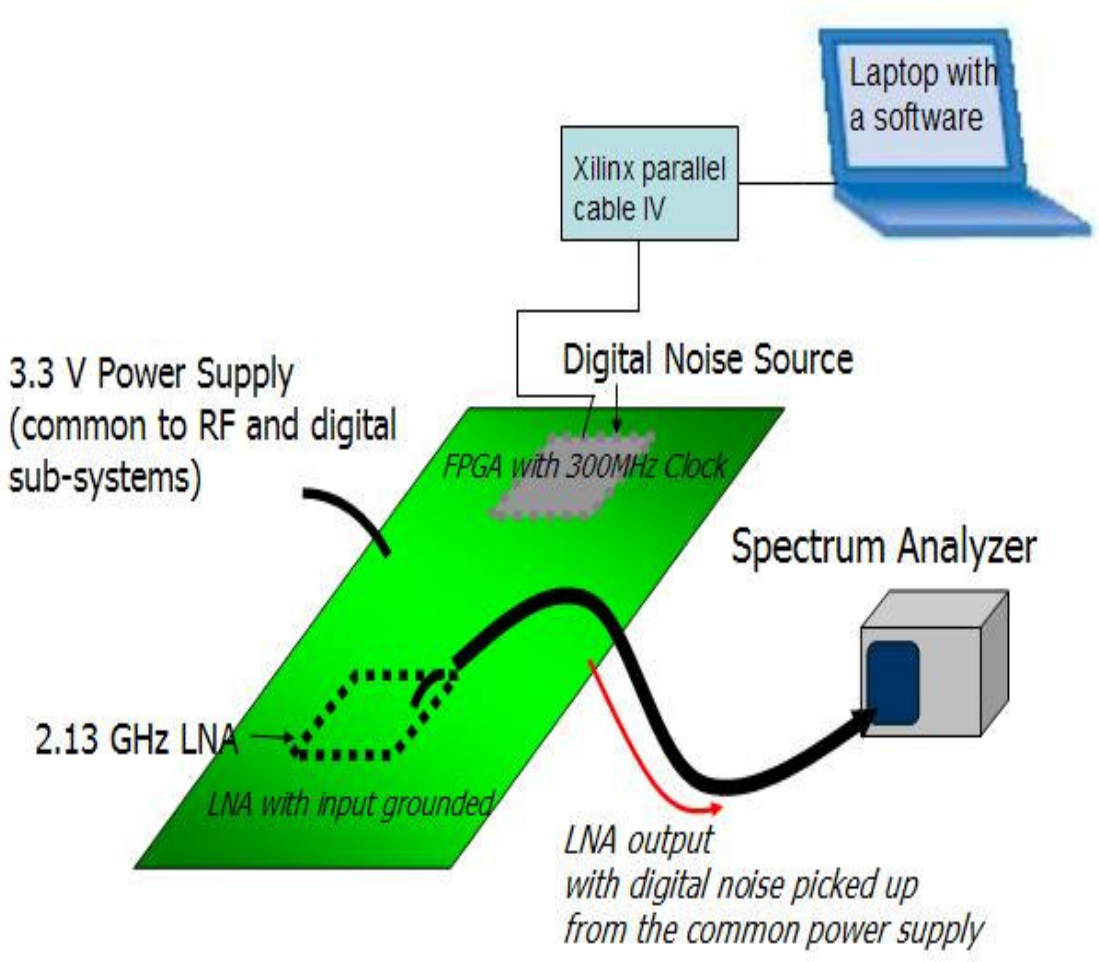
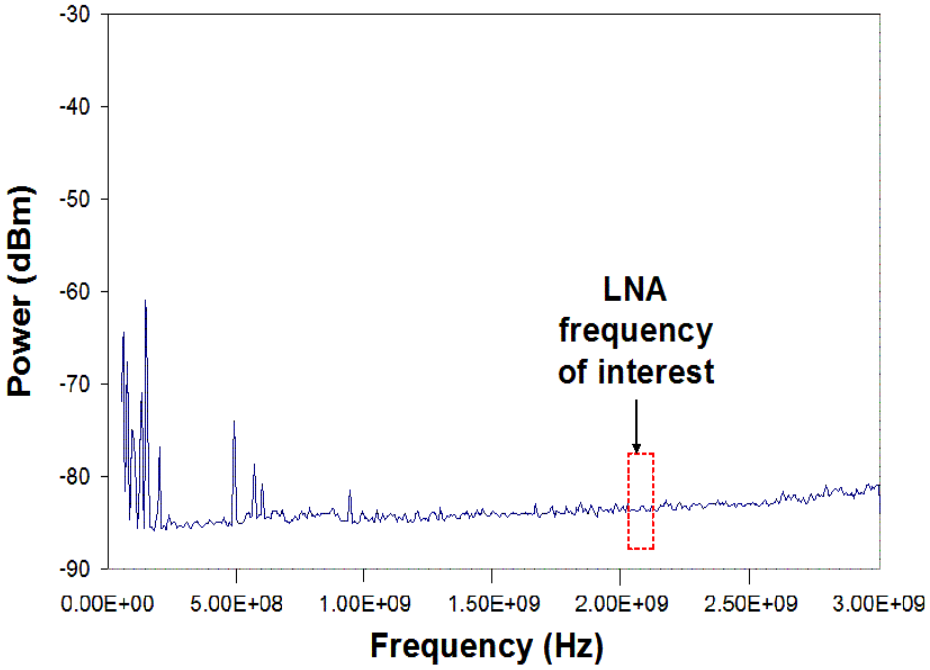
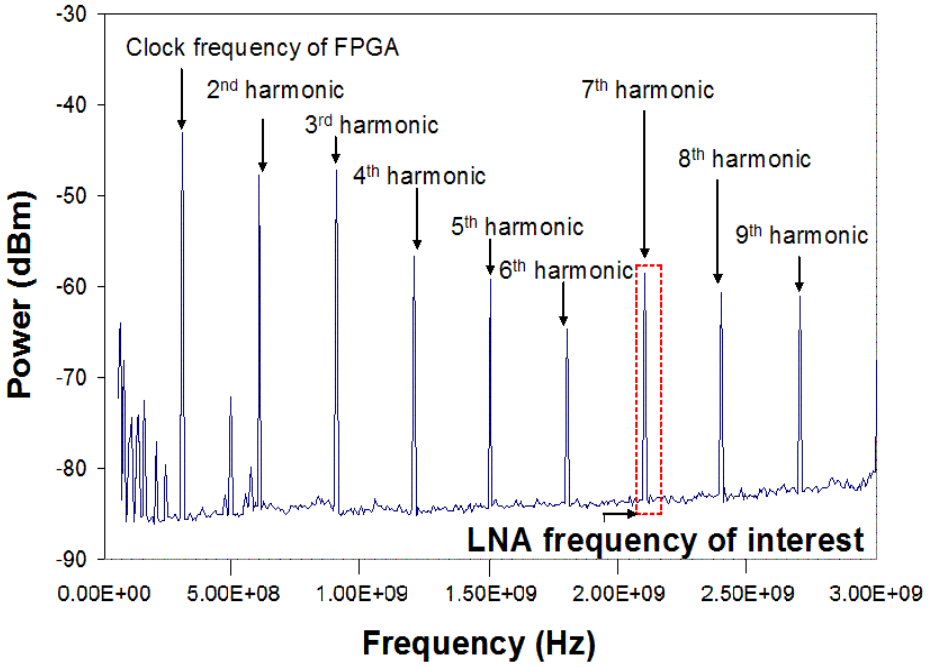


Figure 5.5 Measurement set-up for noise measurements.



(a)



(b)

Figure 5.6 Measured output spectrum of the LNA (a) When the FPGA is completely switched off and (b) When the FPGA is switched on.

Figure 5.6 shows the measured output spectrum of the LNA for the test vehicle without the AI-EBG structure. With the FPGA completely switched off, the output spectrum is clean and contains only low frequency noise, as shown in Figure 5.6 (a). However, when the FPGA is switched on with four switching drivers, the output spectrum exhibits a large number of noise components, as shown in Figure 5.6 (b), at the output of the LNA. As can be seen in Figure 5.6 (b), the noise components are harmonics of the FPGA clock frequency, which is at 300 MHz. In this diagram, the 7th harmonic of the 300 MHz FPGA clock (at 2.1 GHz) lies close to the frequency of operation of the LNA, potentially degrading its performance. Hence, the 7th harmonic noise peak should be suppressed for good LNA functionality. With the AI-EBG structure integrated into the ground plane, it is possible to suppress this harmonic noise peak. Figure 5.7 shows the measured the LNA output spectrum around 2.1 GHz for the test vehicles with and without AI-EBG structure.

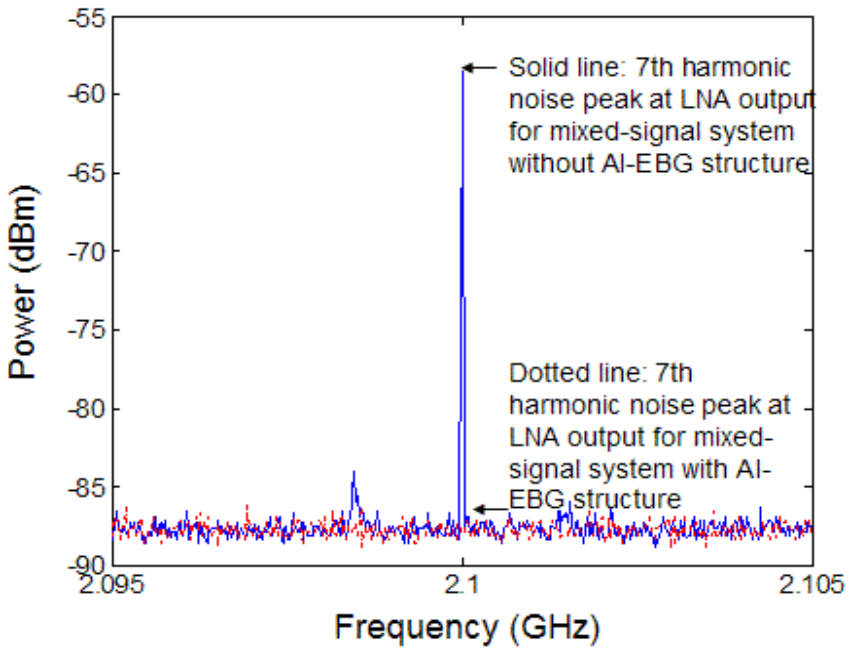


Figure 5.7 Measured 7th harmonic noise peaks at 2.1 GHz for the test vehicle with and without the AI-EBG structure.

The 7th harmonic noise peak at 2.1 GHz has been suppressed from -58 dBm to -88 dBm using the AI-EBG structure, which shows the ability of the AI-EBG structure for excellent noise suppression. It should be noted that -88 dBm is the noise floor in this measurement, which means that the 7th harmonic noise peak due to FPGA has been suppressed completely. Figure 5.8 shows the measured the LNA output spectrum from 50 MHz to 3 GHz for the test vehicles with and without the AI-EBG structure. The harmonic noise peaks from 2 GHz to 3 GHz have been suppressed completely using the AI-EBG structure. This frequency range (from 2 GHz to 3 GHz) corresponds to a stopband with -100 dB isolation level, as shown earlier in Figure 5.4. As can be observed, the AI-EBG based scheme shows very efficient suppression of noise propagation from the digital circuits into RF circuits in integrated mixed-signal systems.

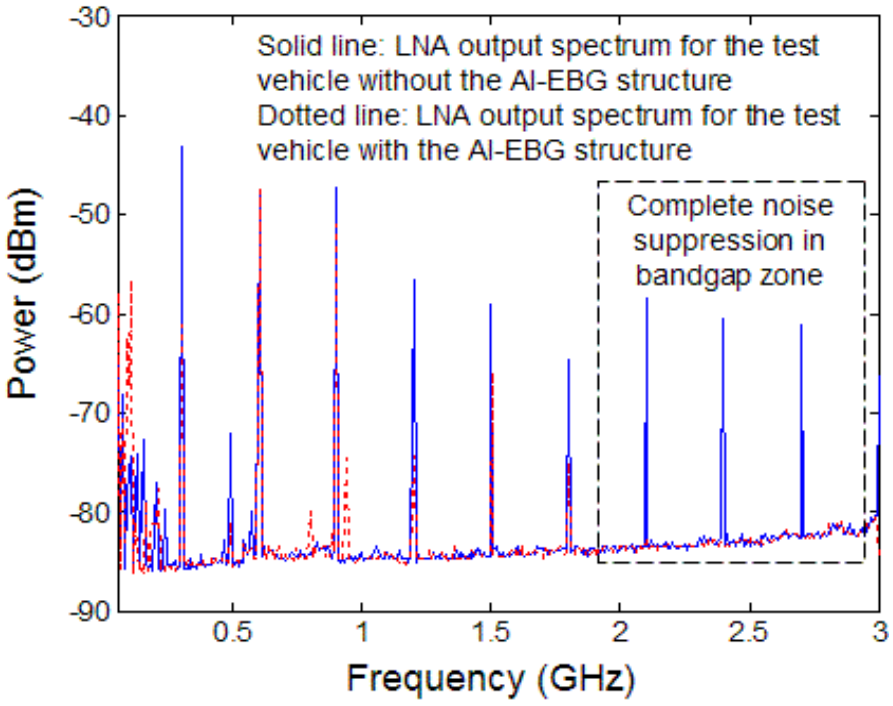


Figure 5.8 Measured LNA output spectrum for the test vehicles with and without the AI-EBG structure.

5.4 Signal Integrity Analysis

The power delivery network needs to function along with the signal lines for high-speed transmission. Since the power and ground planes carry the return currents for the signal transmission lines, the impact of AI-EBG structure on signal transmission needs to be analyzed. First, time domain waveform measurements at the output of the FPGA and far end of the transmission line have been measured. Second, time domain reflectrometry (TDR) measurements have been measured and discussed to understand the discontinuities in the characteristic impedance profile due to the gaps in the AI-EBG plane.

5.4.1 Time Domain Waveforms

Since the AI-EBG plane (i.e., the plane with AI-EBG pattern) is used as a reference plane for signal lines in the stack-up shown in Figure 5.2 in the previous section, the gaps in the AI- EBG structure function as discontinuities, causing degradation in the waveform. In a solid plane, return currents for high speed transmission follow the path of least inductance. The lowest inductance return path lies directly under a signal line, which minimizes the loop area between the outgoing and returning current path [52].

To better understand signal quality, signal waveforms at the output of the FPGA and far end of the transmission line were measured. These two locations are shown in Figure 5.9. The signal from the FPGA propagates along a transmission line. Figure 5.10 shows the measurement results at both locations at 100 MHz. In this figure, two signal waveforms were overlapped to compare difference between them. In this case, there is no

serious signal integrity problem since slopes of signal waveforms are almost the same. But the signal waveform at the far end of transmission line has larger amplitude as compared to the output of the FPGA.

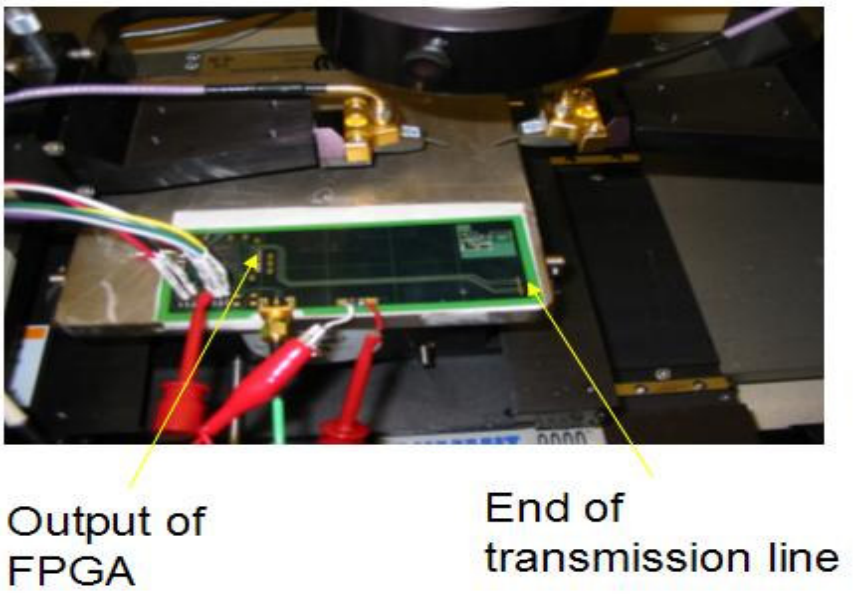


Figure 5.9 Waveform measurement at two locations on the mixed-signal board.

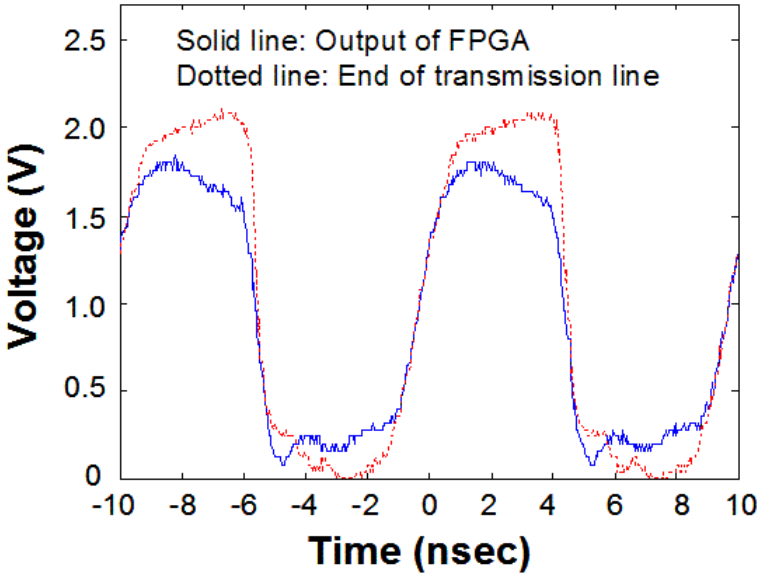
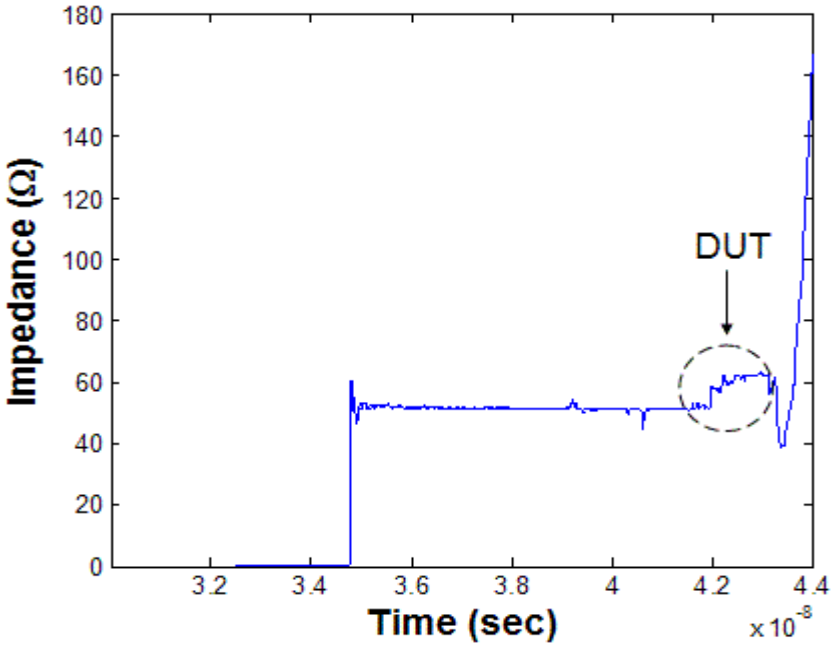


Figure 5.10 Measured waveforms at two different locations.

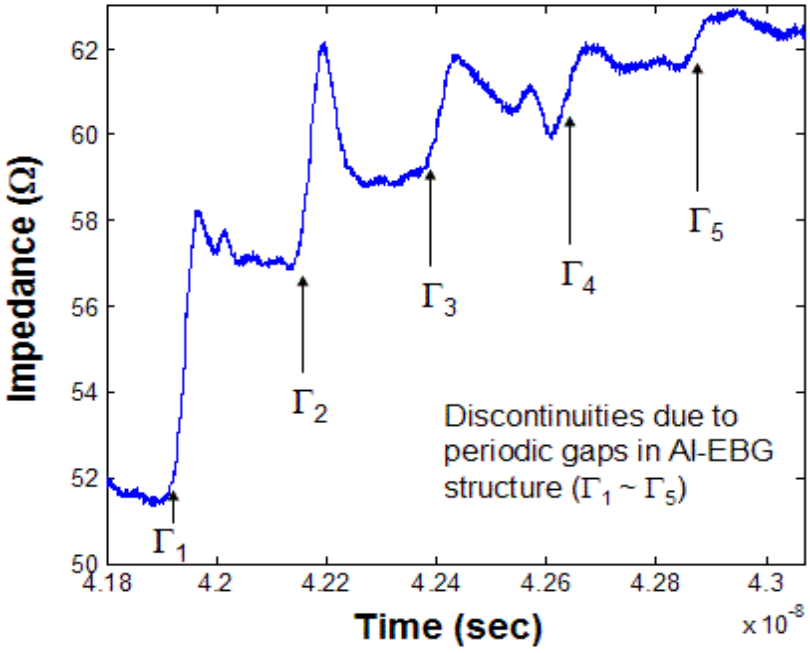
5.4.2 Time Domain Reflectometry (TDR) Measurements

To investigate the phenomena identified in the previous section, time domain reflectometry (TDR) measurements were performed to measure the characteristic impedance of the transmission line. In a TDR measurement, an injected voltage pulse propagates down the signal line, reflects off the discontinuity, and then returns to form a pulse on the oscilloscope [32]. Figure 5.11 (a) shows the measured characteristic impedance profile for one of four transmission lines used in the test vehicle. For this measurement, Cascade microprobes were used for probing the pad at the end of the first transmission line. Figure 5.11 (b) shows the magnified impedance profile for the device under test (DUT). In this figure, discontinuities in the impedance profile were observed. Each change in characteristic impedance causes the TDR trace to bump up or down to a new impedance level. Increasing impedance implies increased inductance, reduced capacitance, or both. Conversely, decreasing impedance implies increased capacitance, reduced inductance, or both [32]. In Figure 5.11 (b), the first discontinuity is caused by the first gap in the AI-EBG structure, which is an inductive discontinuity, as can be seen in Figure 5.9. The inductive discontinuity is followed by a lower impedance transmission line due to the extra capacitance caused by the transmission line traversing a metal patch. Since an injected signal passes over five gaps before it arrives at the FPGA, there are five discontinuities along the signal path, as shown in Figure 5.11 (b).

Next, it can be explained why the signal amplitude at far end of transmission line is bigger than that at output of the FPGA. In case, a signal propagates from the FPGA to the end of transmission line. When a signal passes over a metal branch, the TDR trace bumps up. So, a signal propagates down a transmission line with characteristic



(a)



(b)

Figure 5.11 Measured characteristic impedance profile of the first transmission line over AI-EBG structure in the mixed-signal system (a) Characteristic impedance profile of the first transmission line over AI-EBG structure and (b) Magnified characteristic impedance profile of the first transmission line over AI-EBG structure.

impedance Z_1 and meets a discontinuity due to a gap where the characteristic impedance of the transmission line changes to Z_2. The reflection coefficient formula for this case is given as [32]

$$\Gamma = \frac{v_n^-}{v_n^+} = \frac{Z_{o,n+1} - Z_{o,n}}{Z_{o,n+1} + Z_{o,n}} \tag{5.1}$$

where Γ is a reflection coefficient, v_n^+ is a voltage traveling in positive direction at *n*th transmission line, v_n^- is a voltage traveling in negative direction at *n*th transmission line, $Z_{o,n}$ is a characteristic impedance at *n*th transmission line, $Z_{o,n+1}$ is a characteristic impedance at *(n+1)*th transmission line. Since $Z_2 > Z_1$ in this case, the reflected wave is a positive copy of the incident wave. The incident and reflected waves superimpose. The voltage should be continuous at the discontinuity, so the signal continues onto the second transmission line with peak amplitude based on the total voltage on the first line. When the incident and reflected waves have the same sign, they add, and the voltage signal on the second transmission is large. This situation continues when an injected signal passes over a metal branch in a gap. This is because periodic gaps in AI-EBG structure make discontinuities in impedance profile and these discontinuities make reflection coefficient positive.

5.5 Field Analysis of AI-EBG Structure

In this section, near field and far field simulations and measurements were discussed to understand possible electromagnetic interference (EMI) due to a periodic gap in the AI-EBG plane when the AI-EBG structure is used as a reference plane for a signal line.

5.5.1 Near Field (NF) Simulation and Measurement

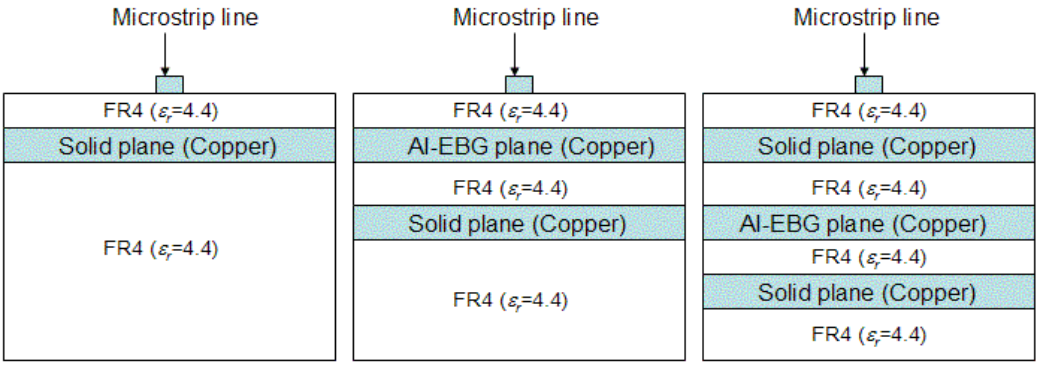
The return current on the reference plane of a signal line plays an important role in near field electromagnetic coupling, and therefore, the return current effect should be taken into consideration in mixed-signal system design. Return current on the reference plane flows mostly in the area below the signal line and tapers off as one traverses from the center towards the edge. In this section, current flowing on the signal line and the area on the reference plane below the signal line will be referred to as "differential mode current" and the current on the reference plane away from the signal line will be referred to as "common mode current". The magnetic field produced by the differential mode is zero since current flows in opposite directions. In this case, the magnetic field due to the current on a microstrip line is given by equation (5.2). In this equation, I is current flowing on the microstrip line and r is the radial distance from the microstrip line.

$$H = \frac{I}{2\pi r}\hat{\phi} \tag{5.2}$$

However, this is not the case for the common mode current. The effect of the common mode current is often ignored due to its small magnitude [64]. The purpose of this work is to understand the near field behavior from a simple signal line such as a microstrip line for the test vehicles with and without various AI-EBG structures.

Three test vehicles have been designed and fabricated for radiation analysis [59]. The first test vehicle is a microstrip line on a solid plane, the second test vehicle is a microstrip line on an AI-EBG structure, and the third test vehicle is a microstrip line on an embedded AI-EBG structure. The third test vehicle was designed to suppress noise in mixed-signal systems without any EMI problems. This is possible since the solid plane was used as a reference plane for the microstrip line in this embedded AI-EBG structure.

In Figure 5.12, the cross section of these three test vehicles are shown. The top view of these three test vehicles is also shown in Figure 5.13. The dielectric material of the test vehicles is FR4 with a relative permittivity, ε_r = 4.4, the conductor is copper with conductivity, σ_c = 5.8 x 10^7 S/m, and a dielectric loss tangent is tan (δ) = 0.02. The copper thickness for the microstrip line, solid plane and AI-EBG plane in the test vehicles is 35 μm, the dielectric thickness between two conductors is 5 mils and the dielectric thickness of the most bottom layer is 28 mils. For the AI-EBG structures in the second and third test vehicles, the size of the metal patch is 1.5 cm x 1.5 cm and the size of metal branch is 0.1 cm x 0.1 cm. It should be noted that the size of the metal patches in the first column near SMA connector is 1.3 cm x 1.5 cm.



(a) (b) (c)

Figure 5.12 Cross section of the three test vehicle (a) Test vehicle 1 is a microstrip line on a solid plane, (b) Test vehicle 2 is a microstrip line on an AI-EBG structure, and (c) Test vehicle 3 is a microstrip line on an embedded AI-EBG structure.

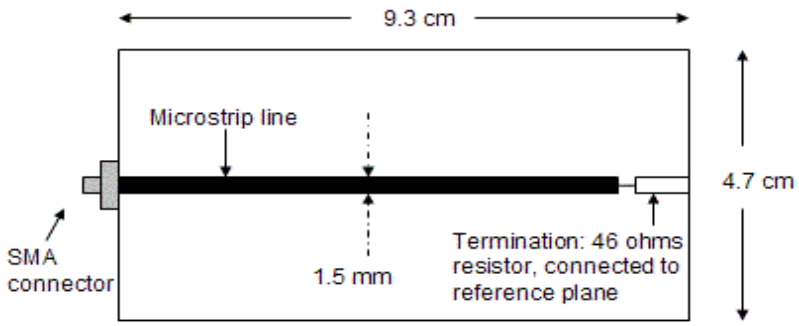


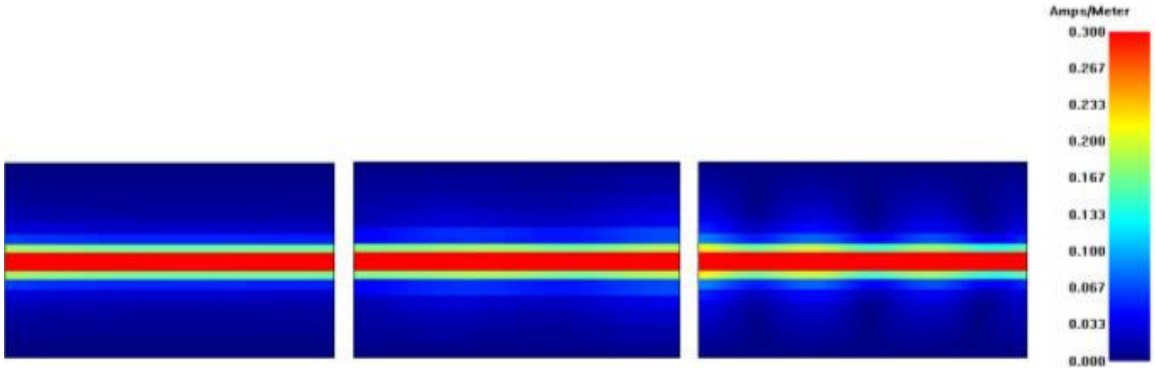
Figure 5.13 Top view of the test vehicles.

The return current on the reference plane of a microstrip line plays an important role in near-field electromagnetic coupling. Hence, the return current effects should be considered in package and board design [64]. The full wave solver (SONNET^{TM}) was used for current density simulation of the three test vehicles. This simulation was contributed by Daehyun Chung. To ensure that simulation results are correct, the standing wave patterns on the reference plane for the test vehicle 1 were captured and these patterns are shown in Figure 5.14. Standing waves are formed at 800 MHz, 1.6 GHz, and 2.4 GHz for the test vehicle 1 and these frequencies correspond to the nulls in the S_{11} simulation, which is shown in Figure 5.15. For S-parameter simulation, port 1 was located at the SMA connector and port 2 was at far end of the microstrip line. The wavelength of the return current can be calculated using the following equation.

$$\lambda = \frac{c}{\sqrt{\varepsilon_{eff}}\, f} \tag{5.3}$$

where $\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2\sqrt{1 + 12\,\frac{h}{w}}}$ is the effective permittivity, ε_r is the relative permittivity of the substrate, w is the width of the microstrip line and h is the height between the microstrip line and the reference plane. The relative permittivity for the test

vehicle 1 is approximately 4.2 for the given microstrip line dimensions.



(a) (b) (c)

Figure 5.14 Standing wave patterns on reference plane of the test vehicle 1 (a) 1st resonance pattern at 800 MHz, (b) 2nd resonance pattern at 1.6 GHz, and (c) 3rd resonance pattern at 2.4 GHz.

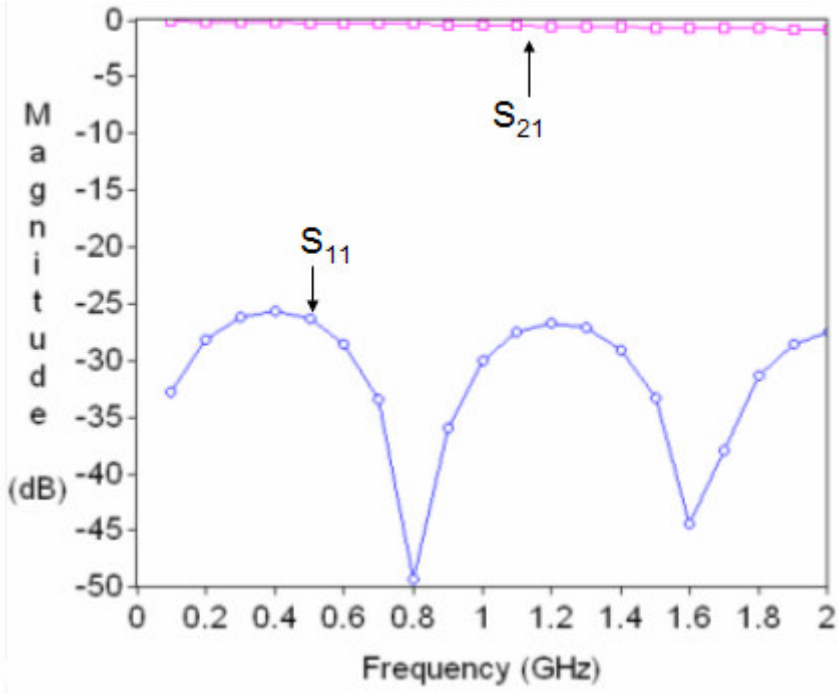


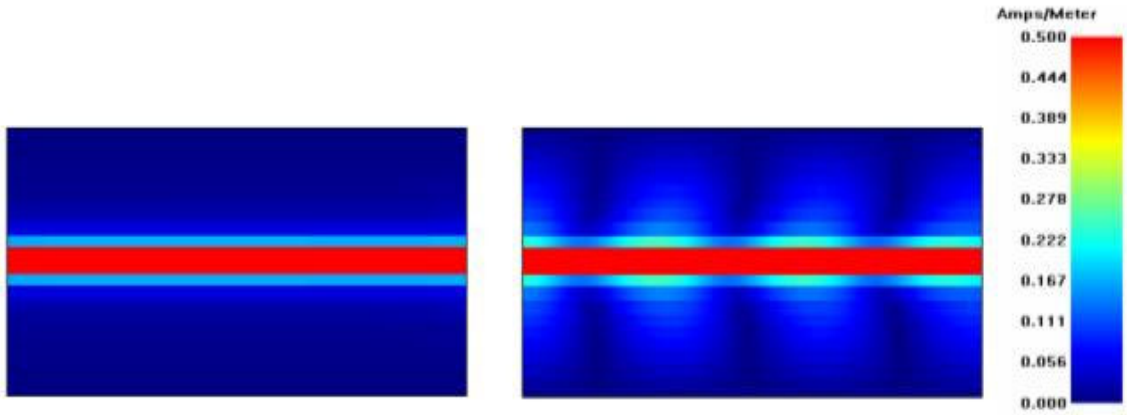
Figure 5.15 S-parameter simulation results of the microstrip line on the test vehicle 1.

Using equation (5.3), the standing waves have wavelengths at frequencies of 800 MHz, 1.6 GHz, and 2.4 GHz, as given in Table 5.1.

Table 5.1 Wavelengths for the standing waves using equation (5.3)

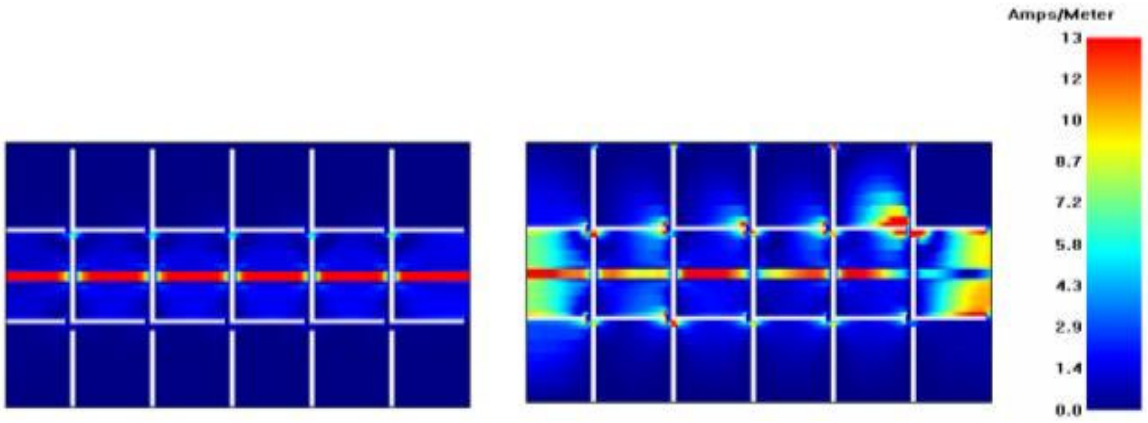
Frequency	Wavelength
800 MHz	18.298 cm
1.6 GHz	9.149 cm
2.4 GHz	6.099 cm

Two frequencies at 300 MHz and 2.7 GHz were chosen for the near field analysis. Figure 5.16 shows current density for the solid reference plane in the test vehicle 1 at 300 MHz and 2.7 GHz and Figure 5.17 shows current density for the AI-EBG plane in the test vehicle 2. The current densities for the solid reference plane in test vehicle 3 (an embedded AI-EBG structure), which is shown in Figure 5.18, showed almost same results as those for the test vehicle 1 since a solid plane was used for both test vehicles. It should be noted that current densities at 300 MHz for the test vehicles 1 and 2 showed the



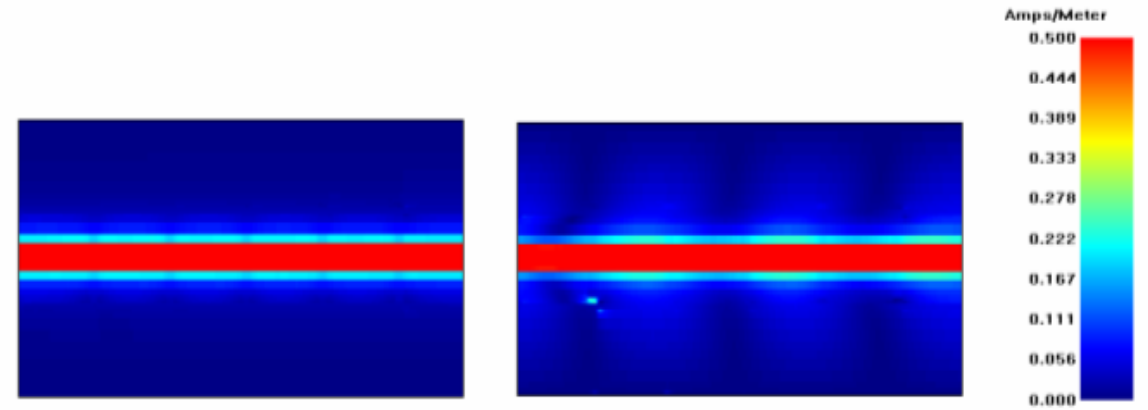
(a) (b)

Figure 5.16 Current density simulation results for the test vehicle 1 (a) Current density at 300 MHz and (b) Current density at 2.7 GHz.



(a) (b)

Figure 5.17 Current density simulation results for the test vehicle 2 (a) Current density at 300 MHz and (b) Current density at 2.7 GHz.



(a) (b)

Figure 5.18 Current density simulation results for the test vehicle 3 (a) Current density at 300 MHz and (b) Current density at 2.7 GHz.

same tendency but, at 2.7 GHz, the current density for the AI-EBG plane in the test vehicle 2 showed a non-ideal current flow, which can cause higher radiation. A non-ideal return path occurs when the return current associated with a signal trace is forced to diverge away from the path of least inductance. This deviation in the ideal return path of the current results in far field radiation, which can cause EMI problem [65]. The periodic gaps in the AI-EBG structure gives rise to the problems listed above at high frequencies.

The near field measurement was carried out using EMC Precision Scan (EPS-3000) equipment and NEC probe (CP-25). This measurement was carried out with Krishna Srinivasan in Epsilon group together. Generally, near field measurement in the GHz range is very difficult since almost all of the commercially available probes are not sensitive for near field measurement in GHz range. However, the NEC probe in this measurement covers a bandwidth of 3 GHz. In these near field measurements, the y component of magnetic field (H_y) was recorded and the unit of the magnetic field intensity is [dBμV]. It should be noted that the near field results can be related to the current density simulation results since the maximum magnetic field intensity represents the maximum current density in this case. The values have been obtained for the magnetic field 12 mm above the microstrip line and normalized with respect to the maximum value of the y component of the magnetic field, which occurs at 2.35 cm, as shown in Figure 5.19.

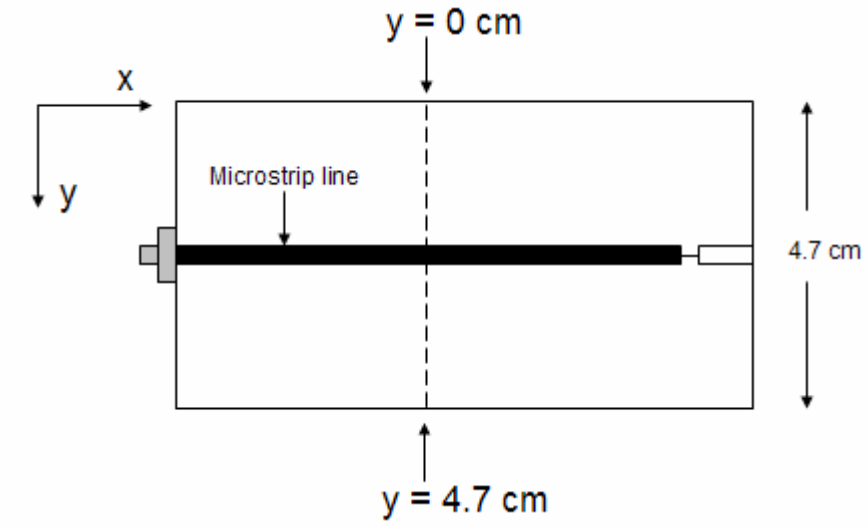
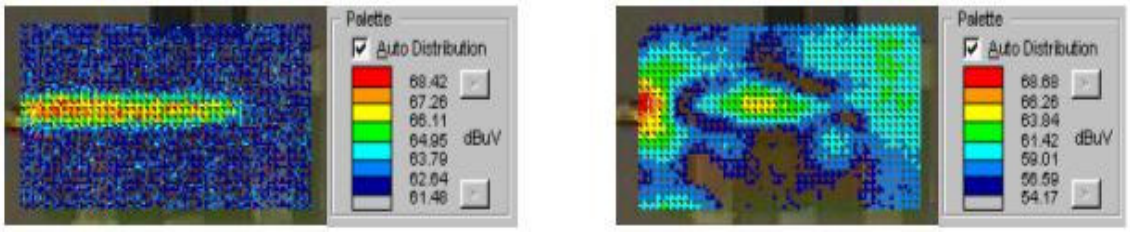


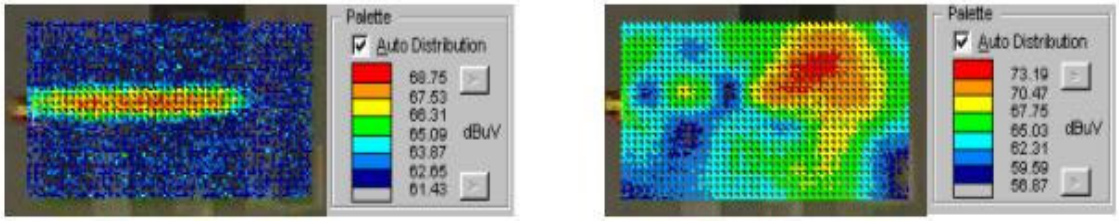
Figure 5.19 Schematic of y component of the magnetic field at 12 mm above the microstrip line.

Figure 5.20 shows near field measurement results for test vehicle 1 at 300 MHz and 2.7 GHz while Figure 5.21 shows near field measurement results for test vehicle 2 at 300 MHz and 2.7 GHz. The near field measurement results for the vehicle 3 are shown in Figure 5.22. Test vehicle 1 and 3 showed the same results since a solid plane was used as a reference plane for both cases. For test vehicle 2, near field results at 300 MHz showed the same results as those for test vehicles 1 and 3 at 300 MHz but near field results at 2.7 GHz showed totally different results from those for test vehicles 1 and 3 since an AI-EBG plane was used as a reference plane for the test vehicle 2, which causes a non-ideal return current flow due to periodic gaps in the AI-EBG plane, and which makes magnetic field distribution in an AI-EBG plane different from that in a solid plane.



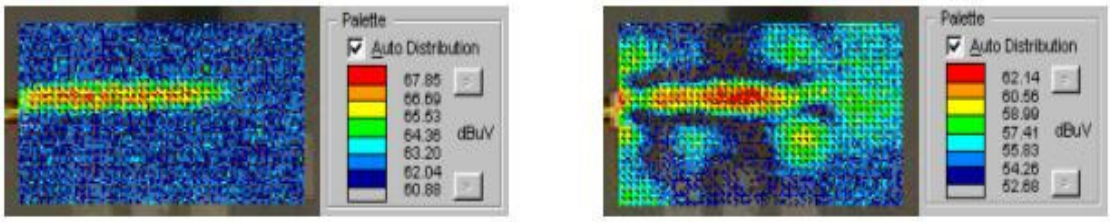
(a) (b)

Figure 5.20 Near field measurement results for test vehicle 1 (a) Magnetic field intensity at 300 MHz and (b) Magnetic field intensity at 2.7 GHz.



(a) (b)

Figure 5.21 Near field measurement results for test vehicle 2 (a) Magnetic field intensity at 300 MHz and (b) Magnetic field intensity at 2.7 GHz.



(a) (b)

Figure 5.22 Near field measurement results for test vehicle 3 (a) Magnetic field intensity at 300 MHz and (b) Magnetic field intensity at 2.7 GHz.

It should be noted that there are similarities between current density simulation results and near field measurement results. This is because the current distribution on the reference plane for the microstrip line creates the magnetic field and both have the similar signature.

5.5.2 Far Field (FF) Simulation and Measurement

The far field simulation was also performed using SONNET^{TM} for the three test vehicles in Figure 5.12. This simulation was mainly contributed by Daehyun Chung. In this simulation, surface radiation from the surface of the test vehicles was investigated by changing the degrees (ϕ = 0°~180° at every 10° and θ = -90°~90° at every 10°), which is shown in Figure 5.23. Figure 5.24 shows far field simulation results for the three test vehicles. It should be noted that test vehicle 2 showed the maximum radiation intensity (after 2 GHz) among three test vehicles since the AI-EBG plane was used as a reference plane for the microstrip line in the test vehicle 2 and the periodic gap in the AI-EBG plane makes the return current non-ideal, which causes a far field radiation at high frequencies.

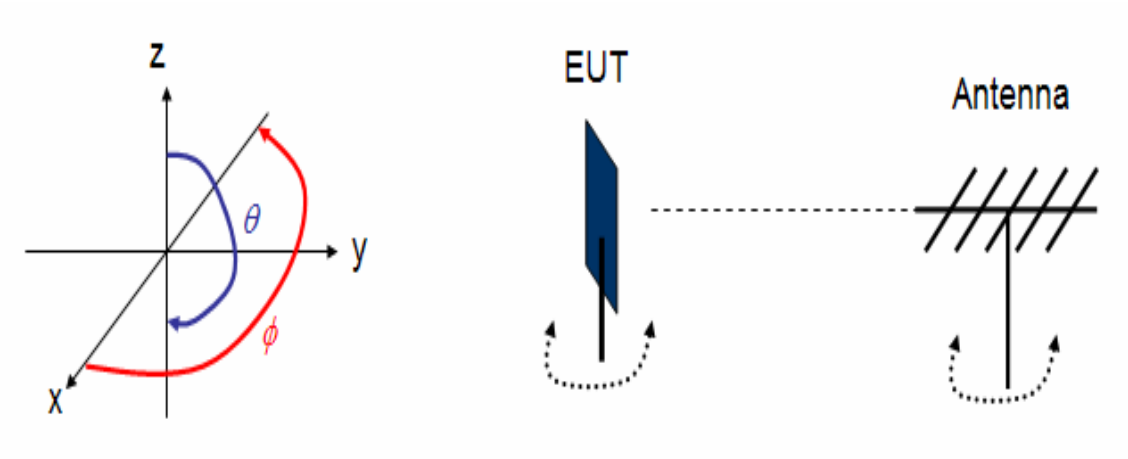
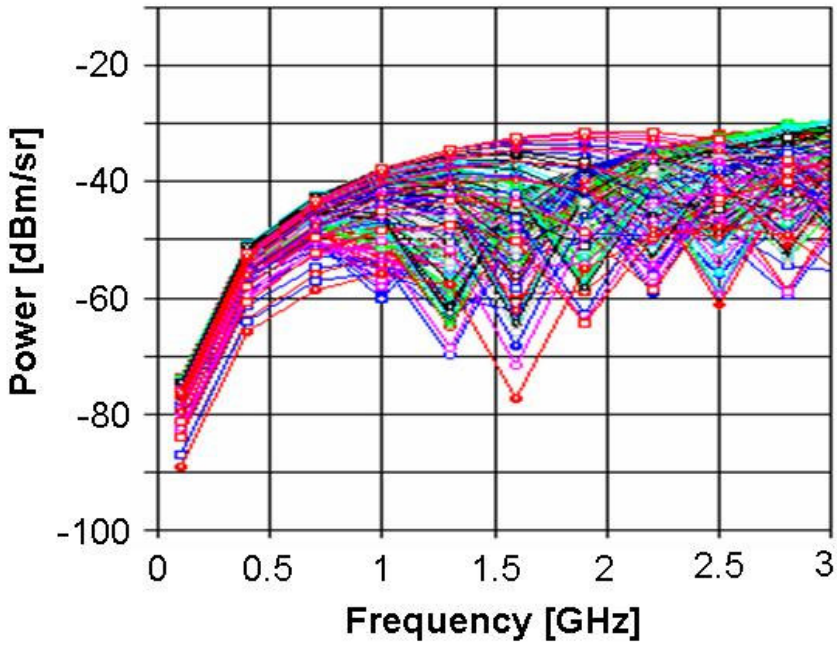
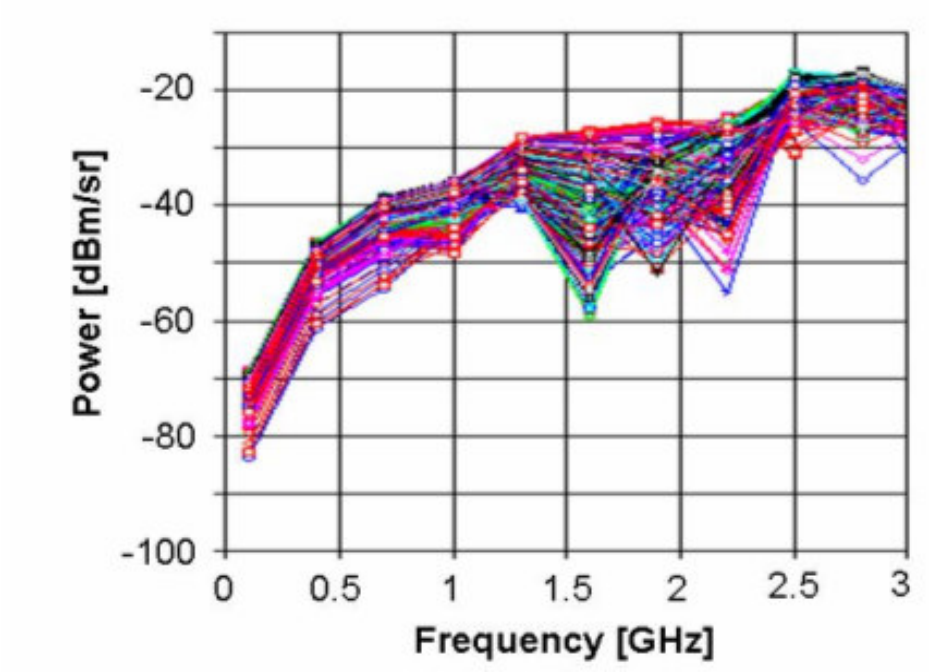


Figure 5.23 Far field (FF) simulation set-up.



(a)

Figure 5.24 Far field simulation results (a) Test vehicle 1 (a solid plane as a reference plane), (b) Test vehicle 2 (an AI-EBG plane as a reference plane), and (c) Test vehicle 3 (a solid plane in an embedded AI-EBG structure as a reference plane).



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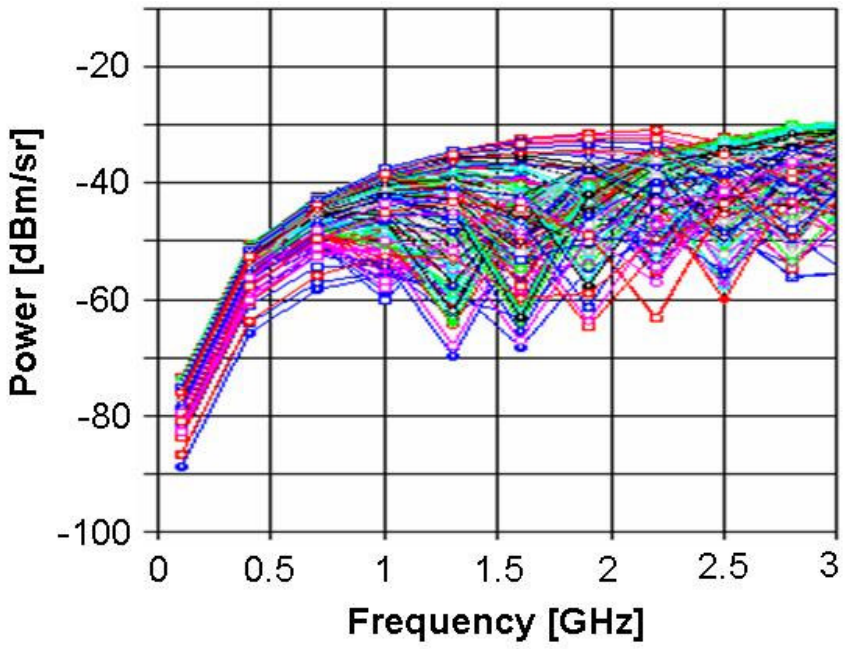
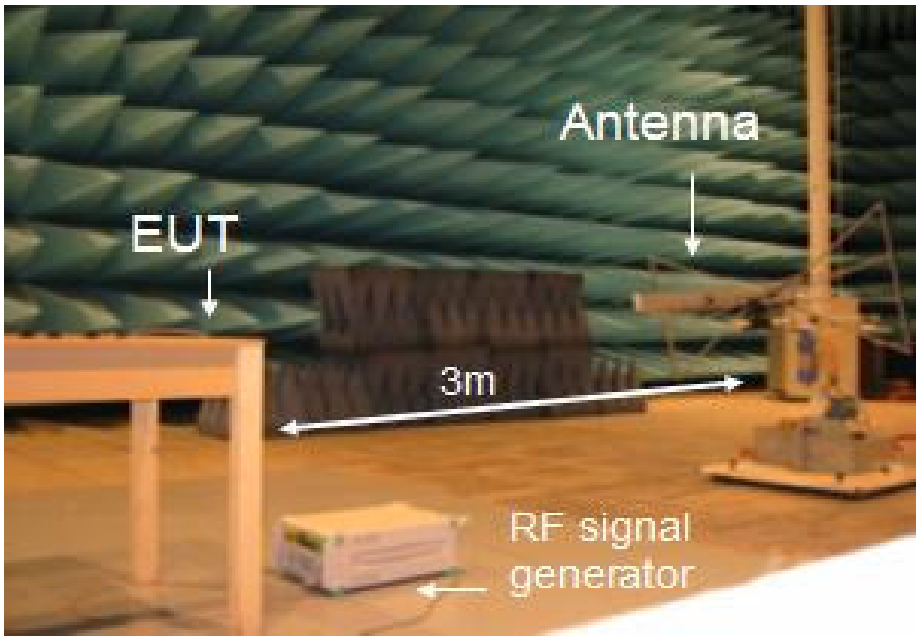


(c)

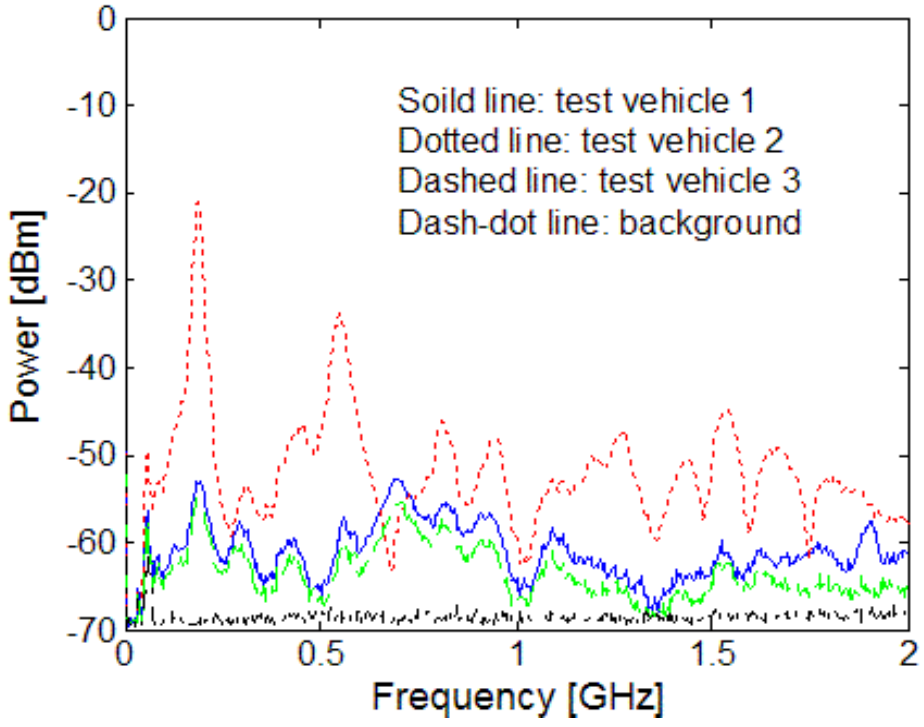
Figure 5.24 Far field simulation results (a) Test vehicle 1 (a solid plane as a reference plane), (b) Test vehicle 2 (an AI-EBG plane as a reference plane), and (c) Test vehicle 3 (a solid plane in an embedded AI-EBG structure as a reference plane).

To verify the above simulation results, far field measurements were done for the test vehicles. These measurements were carried out by Dong Gun Kam who is a graduate student in Professor Joungho Kim at KAIST in Republic of Korea. The far field measurements were done using an Anritsu MG3642A RF signal generator (BW: 125 kHz ~ 2,080 MHz), an Agilent E4440A spectrum analyzer (BW: 3 kHz ~ 26.5 GHz, Res. BW = Video BW = 3 MHz), and an antenna in anechoic chamber. Figure 5.25 (a) shows the measurement set-up for the far field measurements. Since the RF signal generator works properly up to 2 GHz (i.e., 2 GHz is the highest frequency limitation of our signal generator), the far field measurement was also done up to 2 GHz. The distance between EUT and antenna was 3 m in this case. The RF signal generator was connected to EUT as a source and the spectrum analyzer, which was connected to the antenna, recorded the field intensity from the surface of the test vehicle. In this measurement, surface radiation from the surface of the test vehicles was investigated by changing the location of the EUT and antenna for the degrees ($\phi = 0°$, 90°, 180° and $\theta = 0°$ and 90°) and measured the maximum field intensity among the field intensities from the above degrees. In this measurement, the radiation intensity from test vehicle 2 is the maximum among the three test vehicles, as shown in Figure 5.25 (b), and test vehicles 1 and 3 showed almost the same radiation intensity because a solid plane was used as a reference plane for these two test vehicles. It should be noted that the radiated power intensities of the far field measurements in Figure 5.25 (b) are in the range of the simulated power intensities in Figure 5.24, except for the peaks at 190 MHz and 550 MHz for test vehicle 2.

To minimize possible EMI problem, the test vehicle with an embedded AI-EBG structure (test vehicle 3) was designed and showed almost the same (or a little better) radiation characteristics as that of test vehicle 1 (reference test vehicle). This test vehicle (test vehicle 3) showed that an embedded AI-EBG structure can be used to suppress noise in mixed-signal systems without causing EMI problems.



(a)



(b)

Figure 5.25 Far field measurement set-up and results (a) Measurement set-up for far field measurement and (b) Far field measurement results.

5.6 Design Methodology

Since the AI-EBG plane is used as a reference plane for signal lines, it can cause signal integrity problems. The best solution for avoiding this signal integrity problem is to use a solid plane as a reference plane, rather than the AI-EBG plane. For example, in Figure 5.2, the AI-EBG plane should be located on power layer (3rd metal layer) rather than on ground layer (2nd metal layer), which eliminates the signal degradation due to the EBG structure.

To prevent possible signal integrity as well as EMI problems, the plane stack-up in Figure 5.26 is recommended. In Figure 5.26, the first plane is the solid reference

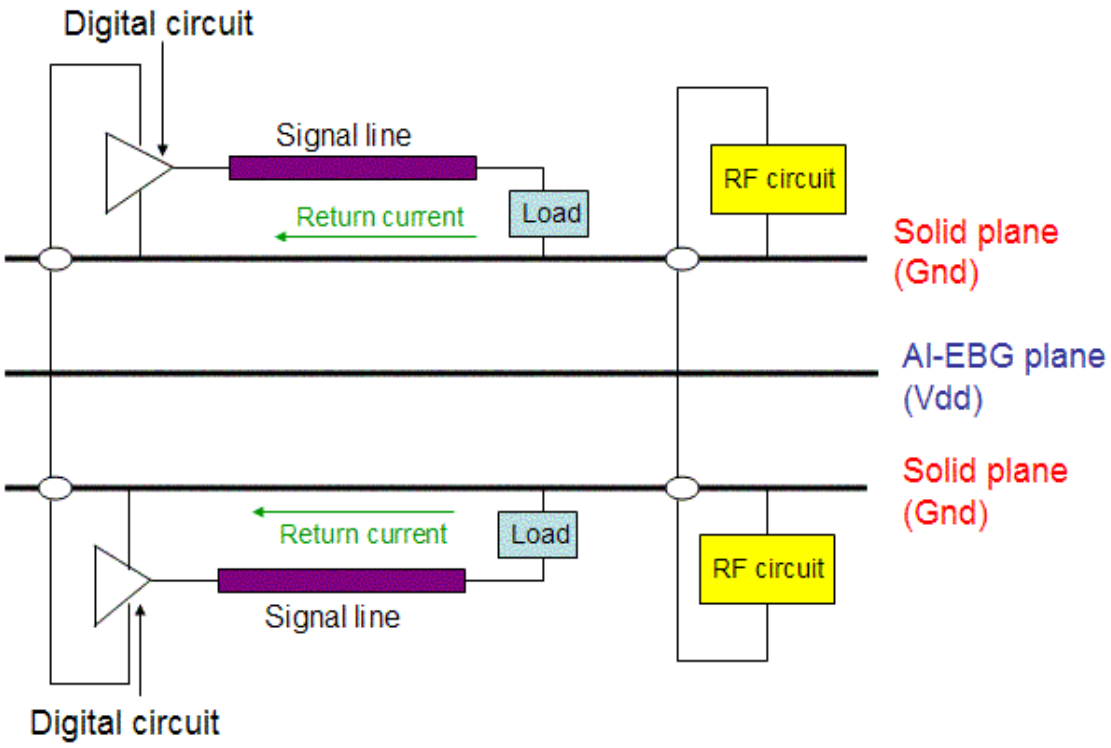


Figure 5.26 Plane stack-up for avoiding possible problems related to signal integrity and EMI.

ground plane for the signal lines on the top, the second plane is the AI-EBG plane, and the third plane is the solid reference ground plane for the signal lines on the bottom. In this stack-up, the AI-EBG plane is located between solid planes, which avoids possible problems associated with signal integrity because solid planes are used as reference planes for signal transmission lines. Since gaps in reference planes cause common mode currents of the transmission lines, the stack-up shown in Figure 5.26 also avoids radiation from the AI-EBG structure. This has been confirmed through a combination of modeling and measurements in the previous section. Figure 5.27 shows the plane stack-up for multilayer applications.

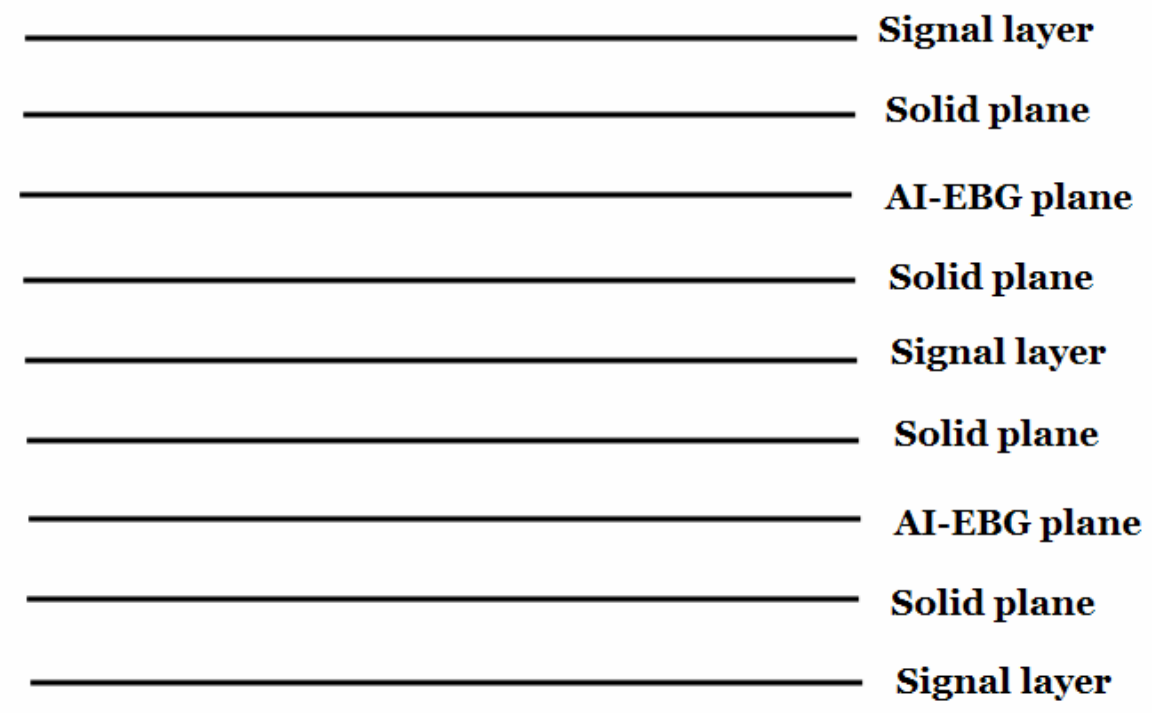


Figure 5.27 Plane stack-up for multilayer structure for avoiding possible problems related to signal integrity and EMI.

5.7 Summary

In this chapter, the realistic mixed-signal system with and without AI-EBG structure have been designed and fabricated to see noise suppression effects due to AI-EBG structure. These mixed-signal test vehicles consist of an FPGA (driving a 300 MHz bus) and a Low Noise Amplifier (LNA) (operating at 2.13 GHz) which were fabricated on the FR4 based substrate. The board was a three metal layer PCB that is 10.08 cm by 4.02 cm. The first metal layer was a signal layer, the second metal layer was a ground layer (Gnd), and the third metal layer is a power layer (Vdd). The AI-EBG structure was located in a ground layer in this test vehicle. The measurement results for the mixed-signal systems with and without AI-EBG structure proved that harmonic noise peaks due to digital circuits have been suppressed completely in stopband frequency range using the AI-EBG structure.

In this chapter, various characterizations were performed to understand the effect of the gap in the AI-EBG structure. First, time domain waveform measurements at the output of the FPGA and far end of the transmission line were shown. Second, time domain reflectrometry (TDR) measurements were also shown and discussed to understand the discontinuities in the characteristic impedance profile due to the gaps in the AI-EBG plane. Third, near field and far field simulations and measurements were analyzed to understand possible electromagnetic interference (EMI). Finally, design methodology was suggested to avoid any possible signal integrity and EMI problems when the AI-EBG structure is used as a part of the power distribution network in mixed-signal systems.

CHAPTER 6

Ultra Wide Band (UWB) Applications of AI-EBG Structures

In this chapter, various novel hybrid alternating impedance electromagnetic bandgap (AI-EBG) structures have been discussed for noise suppression and isolation in ultra wide band (UWB) applications (from 3.1 GHz to 10.6 GHz). In UWB technology, since the maximum signal power is limited to a very low level (-41.3 dBm) by the Federal Communications Commission (FCC), any noise from digital circuits could destroy the functionality of RF circuits and cause system failure. Hence, noise suppression is a major bottleneck for UWB technology since very high isolation is required over the UWB frequency range. In the previous chapters, the AI-EBG structure showed excellent isolation but the stopband range for -80 dB isolation was between 3 GHz and 4 GHz even though the stopband range for -40 dB isolation was over 8 GHz. Hence, it is critical to design hybrid AI-EBG structures for UWB frequency range. Various novel hybrid AI-EBG structures have been designed, simulated, fabricated, and measured for UWB isolation requirement. These hybrid AI-EBG structures have shown excellent isolation over UWB frequency range.

6.1 Introduction

Ultra wide band (UWB) technology offers a solution for supporting the bandwidth, cost, power consumption, and physical size requirements of next generation

consumer electronic devices. UWB enables wireless connectivity with consistent high data rates across multiple devices and PCs within the digital home and the office. UWB radios can use frequencies from 3.1 GHz to 10.6 GHz. To allow for such a large signal bandwidth, the Federal Communications Commission (FCC) put in place severe broadcast power restrictions. Since the maximum signal power is limited to a very low level (-41.3 dBm ≅ 74 nW), any in-band noise reaching the receiver from digital circuits could corrupt the signal of RF circuits, which could lead to failure of the system. For example, a UWB transceiver, as shown in Figure 6.1, exists in a module or a chip on the same board with noisy digital circuits. Since the low noise amplifier (LNA) in the UWB transceiver is extremely sensitive, a noise spike from digital circuits in or close to the operating frequency band of the device can de-sensitize the circuit, destroying its functionality. Therefore, noise suppression in UWB frequency range is a major bottleneck in UWB technology because very high isolation is required to ensure noise free environment in UWB system.

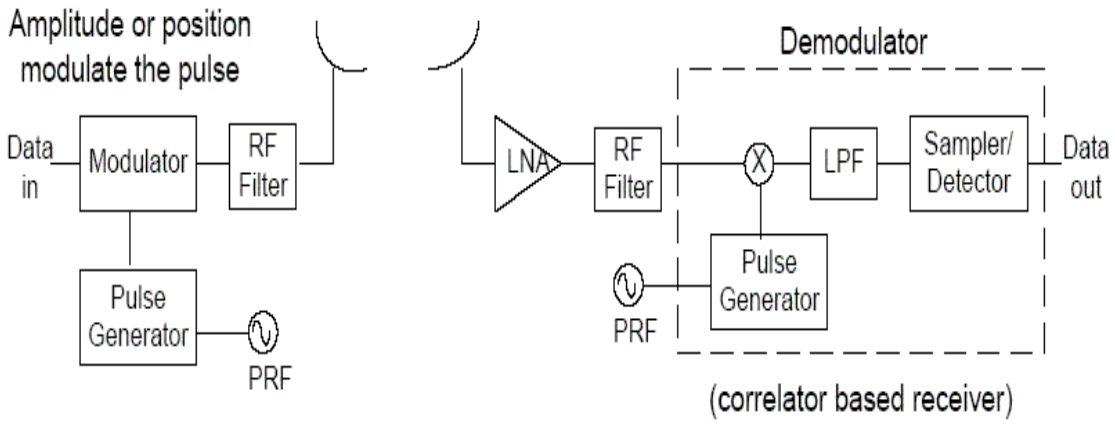


Figure 6.1 Ultra wide band (UWB) transceiver architecture.

6.2 Design of Hybrid AI-EBG Structures for UWB

In filter theory, the overall effect of cascaded filters is a superposition of effect of the individual filters. Similarly, since AI-EBG structure behaves like a low pass filter, which has been shown through simulations and measurements, and metal patch size mainly determines the stopband center frequency in AI-EBG structure, it is possible to design a hybrid AI-EBG structure for ultra wide band (UWB) frequency range (from 3.1 GHz to 10.6 GHz). In addition to UWB frequency range, a very high isolation level (~ better than -70 dB) is required over the whole UWB frequency range. It is almost impossible to satisfy these requirements using conventionally known EBG structures.

These requirements can be achieved using hybrid AI-EBG structures [60]. In this case, two different metal patches were used to obtain an ultra wide stopband. A metal patch has size 1.5 cm x 1.5 cm and the other has size 0.7 cm x 0.7 cm. The metal branch of 0.1 cm x 0.05 cm was used in the structure. The port 1 is placed at (0.3 cm, 1.95 cm) and port 2 is located at (9.2 cm, 1.95 cm) with the origin (0, 0) lying at the bottom left corner of the structure, as shown in Figure 6.2. The first metal patch (1.5 cm x 1.5 cm) and branch make a stopband that ranges from 2 GHz to 5 GHz and the second metal patch (0.7 cm x 0.7 cm) and branch make a stopband that ranges from 5 GHz to 11 GHz. This bandgap range covers a frequency range for an UWB wireless LAN card. The size of the board is 9.5 cm x 4.7 cm for this case, which is the same size of WLAN card. The dielectric material of the board is FR4 with a relative permittivity, $\varepsilon_r = 4.4$. The conductor is copper with conductivity, $\sigma_c = 5.8 \times 10^7$ S/m, and dielectric loss tangent, $\tan(\delta) = 0.02$. The transmission matrix method (TMM) in [40]-[42] was used to model and simulate this structure. In TMM, a unit cell size of 0.05 cm x 0.05 cm, which corresponds to an

electrical size of λ/26 at 11 GHz, was used for accurate results. The simulated S_{21} result in Figure 6.2 shows an excellent stopband floor (below -80 dB) for ultra wide band frequency range.

In some applications, compact size is required. For this purpose, a smaller hybrid AI-EBG structure was also designed. One metal patch has size 1.5 cm x 1.5 cm and the other has size 0.7 cm x 0.7 cm. The metal branch of 1 mm x 0.2 mm was used in the structure. Port 1 is placed at (0.3 cm, 1.95 cm) and port 2 is located at (5.2 cm, 2.35 cm)

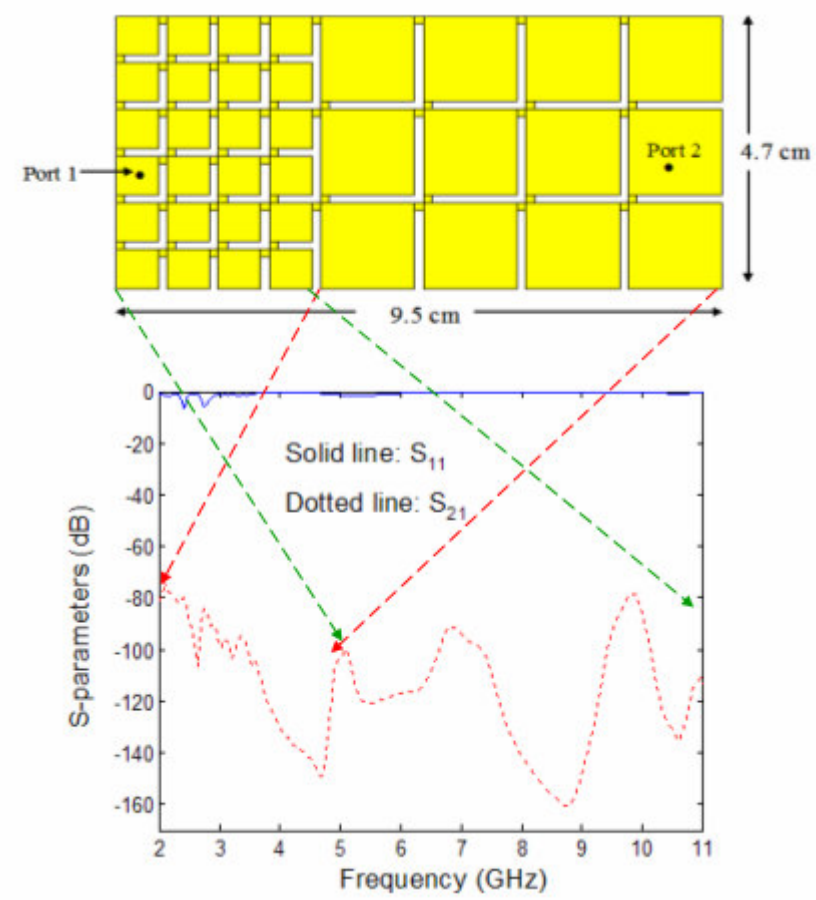


Figure 6.2 Schematic of simulated novel hybrid AI-EBG structure and simulated results of S-parameters for the novel hybrid AI-EBG structure.

with the origin (0, 0) lying at the bottom left corner of the structure, as shown in Figure 6.3. The first metal patches (1.5 cm x 1.5 cm) and branches make a stopband that ranges from 2 GHz to 5 GHz and the second metal patches (0.7 cm x 0.7 cm) and branches make a stopband that ranges from 5 GHz to 12 GHz, as shown in Figure 6.4. This bandgap range covers a frequency range for UWB applications. The size of the board is 5.5 cm x 4.7 cm for this case, which is mini PCI card size. The dielectric material of the board is FR4 with a relative permittivity, $\varepsilon_r = 4.4$. The conductor is copper with conductivity, $\sigma_c = 5.8 \times 10^7$ S/m, and dielectric loss tangent, $\tan(\delta) = 0.02$. The transmission matrix method (TMM) in [8]-[9] was used to model and simulate this structure. In TMM, a unit cell size of 0.2 mm x 0.2 mm, which corresponds to an electrical size of $\lambda/65$ at 11 GHz, was used for accurate results. The simulated result in Figure 6.4 shows an excellent stopband floor (better than -80 dB) for UWB frequency range.

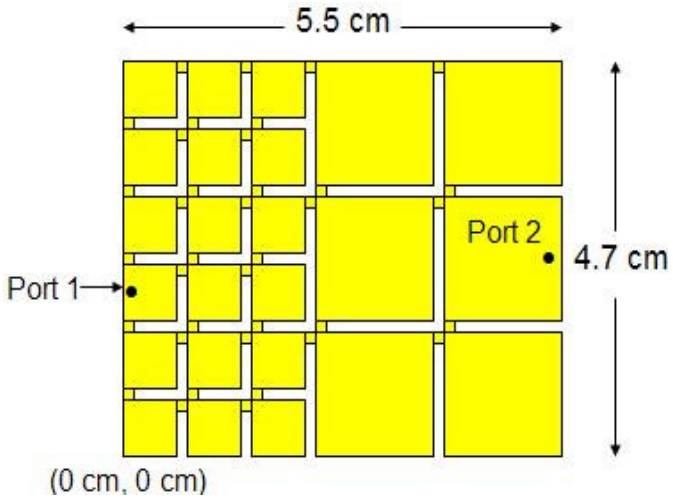
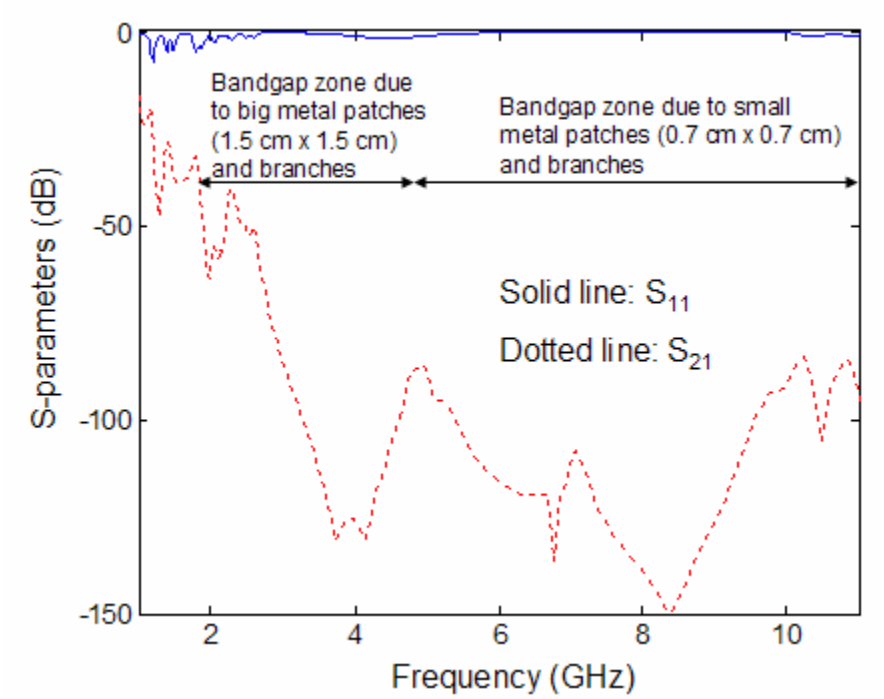
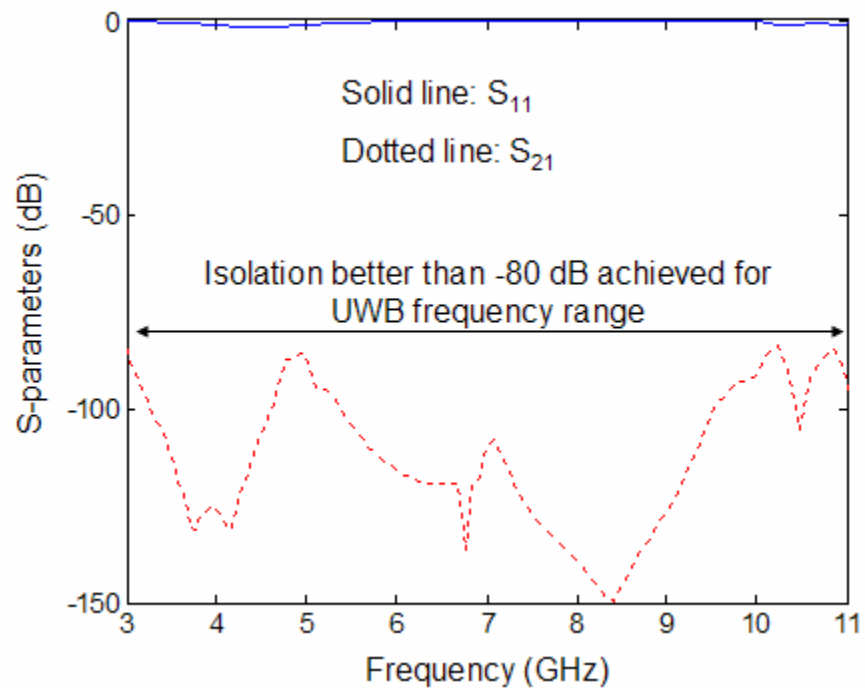


Figure 6.3 Compact hybrid AI-EBG structure for UWB applications.



(a)

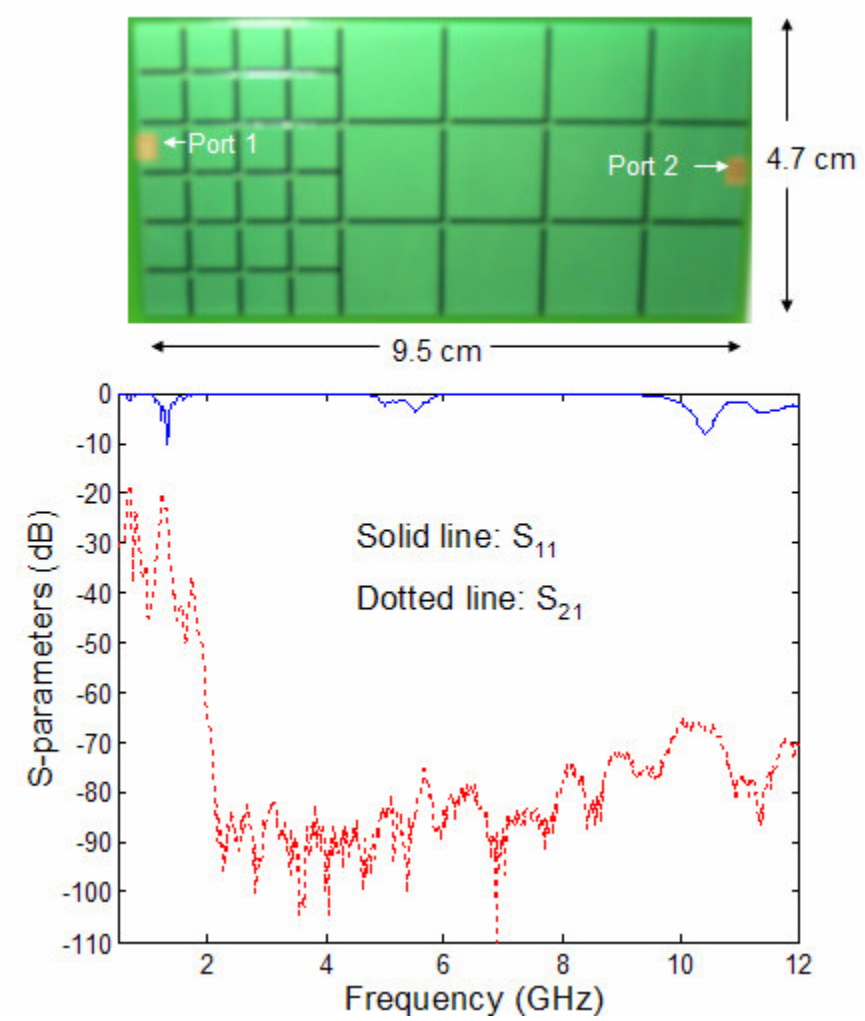


(b)

Figure 6.4 Simulated results of S-parameters for the hybrid AI-EBG structure (a) S-parameters from 1 GHz to 11 GHz and (b) S-parameters from 3 GHz to 11 GHz.

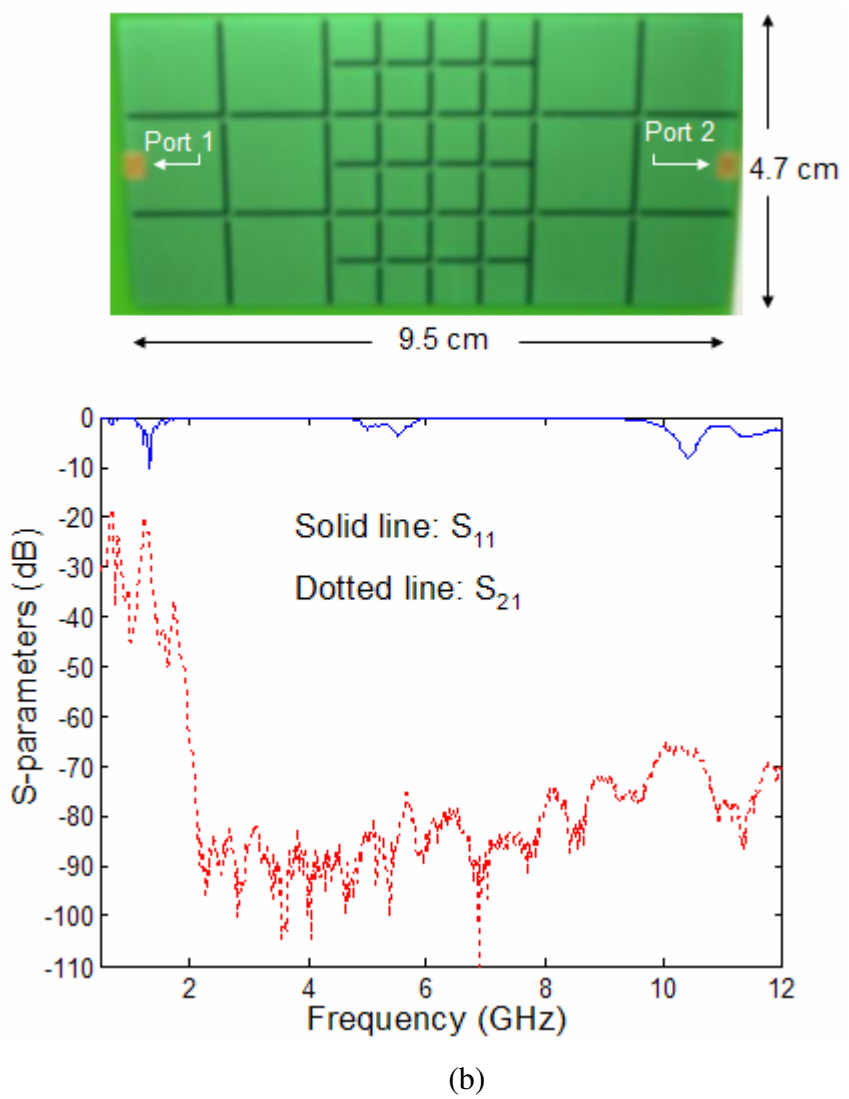
6.3 Fabrication and Measurement of Novel Hybrid AI-EBG Structures

To verify the simulated results in the previous section, these hybrid AI-EBG structures were fabricated using standard FR4 process. Figure 6.5 shows the photographs of fabricated hybrid AI-EBG structures and corresponding S-parameter measurement results. As can be observed, these hybrid AI-EBG structures show excellent isolation over ultra wide band frequency range (from 2 GHz to 12 GHz). In fact, S_{21} reached the sensitivity limit (-80 dB ~ -100 dB) of the VNA used in the frequency range from 2 GHz to 8 GHz. The measured S21 results in Figure 6.5 (a) and (b) show almost the same results even though the locations of the metal patches are different in the structures. These results are much better than those from the mushroom-type EBG structures in terms of isolation level and bandwidth of the stopband. The reason why the AI-EBG structure produces a better isolation level is because the AI-EBG structure is more optimized to make maximum wave interference and the reason why the AI-EBG structure produces wider stopband is because the AI-EBG structure is a low-pass filter (while the mushroom-type EBG structure is a bandstop filter). Moreover, these hybrid AI-EBG structures do not need an additional metal layer and blind vias, making them desirable for PCB applications.



(a)

Figure 6.5 Photographs of the fabricated hybrid AI-EBG structures and their measured S-parameter results.



(b)

Figure 6.5 Photographs of the fabricated hybrid AI-EBG structures and their measured S-parameter results.

Figure 6.6 shows the photograph of the fabricated compact hybrid AI-EBG structure and its S-parameter measurement results. The measured S_{21} results of the compact hybrid AI-EBG structure also show very good isolation even though the measured S-parameter results of the compact hybrid AI-EBG structure are not as good as those of the hybrid AI-EBG structure in Figure 6.5. The decrease of the isolation level of the compact hybrid AI-EBG

structure is due to a decrease of the number of the metal branches and patches in the structure.

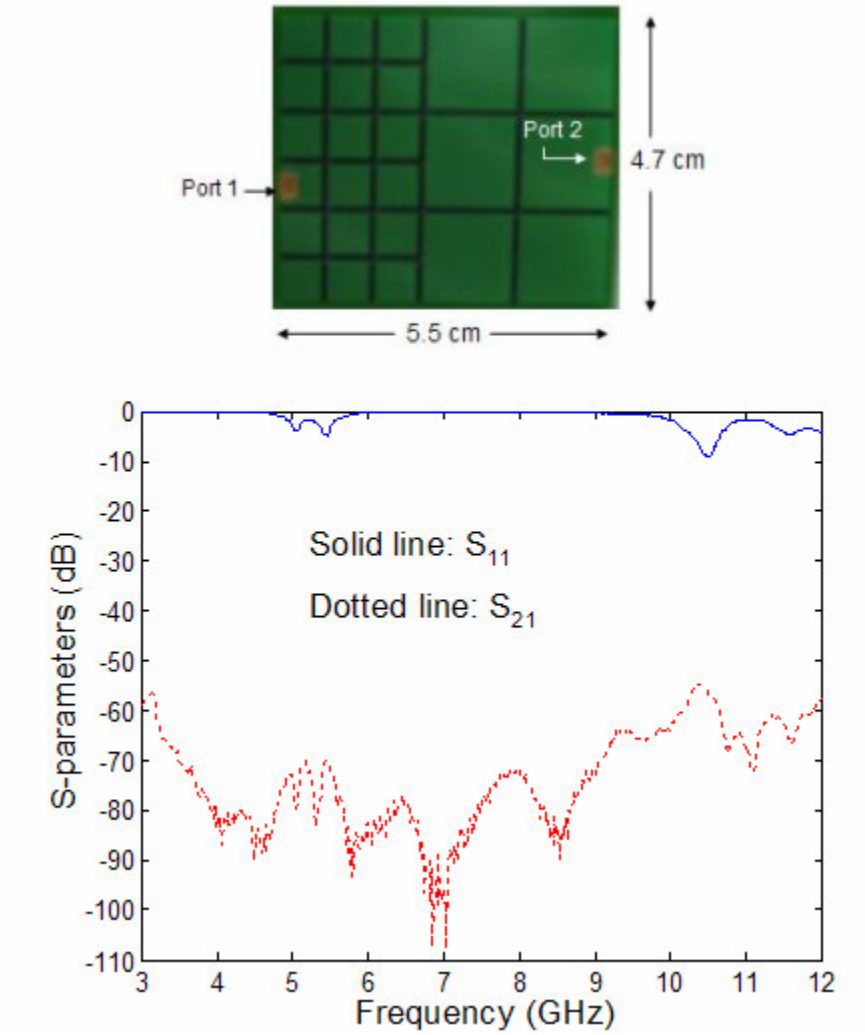


Figure 6.6 Photograph of the compact hybrid AI-EBG structure and its measured S-parameters.

6.4 Mixed-Signal System Simulation for UWB

As an example of the use of the hybrid AI-EBG structure for mixed-signal integration, consider the mixed-signal system in which there is a low noise amplifier

(LNA) and a digital processor powered using a common power supply. The processor drives an 800 MHz bus. Noise generated in the digital sub-system couples into the LNA through the common power supply. Use of the AI-EBG structure in the implementation of the power distribution system provides a cost-effective and compact means for noise suppression, as compared to the use of split planes with multiple power supplies. Fig. 6.7 shows simulated LNA output spectrum (using HP-ADS™) where the power distribution system has been implemented with and without the hybrid AI-EBG structure. The dotted line represents the noise power appearing at the output of the LNA using an ordinary

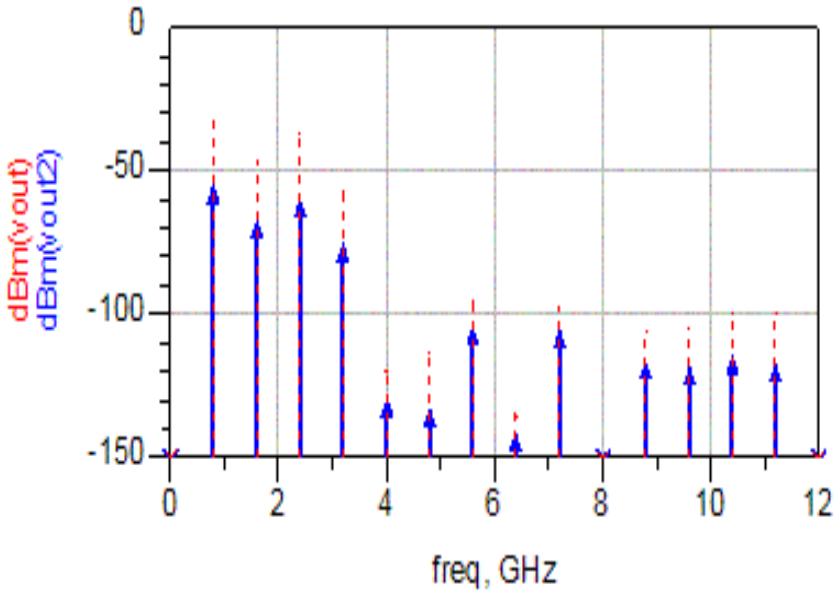


Figure 6.7 Mixed-signal system simulation results for UWB application.

solid plane-pair for power distribution. The solid line represents noise power when the AI-EBG based power distribution scheme is used in the system. Although the harmonics of the digital noise does couple into the LNA circuitry in both cases, there is significant

reduction of the noise amplitudes for the system with the hybrid AI-EBG based power scheme.

6.5 Ultimate Isolation from DC to Infinite Frequency

The development of the structure that can provide excellent isolation from DC to infinite frequency is critical since some noises occur at low frequency due to nonlinearity of active devices. Therefore it's difficult to suppress this noise by the AI-EBG structure since the metal patch size should be large enough to move the stopband to a low frequency like 10 MHz. It is possible to achieve excellent isolation from DC to infinite frequency. This can be achieved using the following concept: "power island in sea of hybrid alternating impedance electromagnetic bandgap (AI-EBG) structure." In this structure, the gap around the power island provides excellent isolation from DC to around 1.5 GHz, one AI-EBG structure provides excellent isolation from 1.5 GHz to 5 GHz, the other AI-EBG structure provides excellent isolation from 5 GHz to 10 GHz, and combination effect of the hybrid AI-EBG structure provides excellent isolation from 10 GHz to infinite frequency.

To ensure that this is possible, this novel structure was fabricated using a standard FR4 process. Figure 7.7 shows the photograph of the fabricated novel structure and corresponding S-parameter measurement results. As can be observed, this structure shows excellent isolation from DC to 12 GHz. In fact, S_{21} reached the sensitivity limit (-80 dB ~ -100 dB) of the VNA used in the frequency range from DC to 5 GHz. Some peaks around 5 GHz and 10 GHz can be suppressed by optimizing the metal branch in the structure.

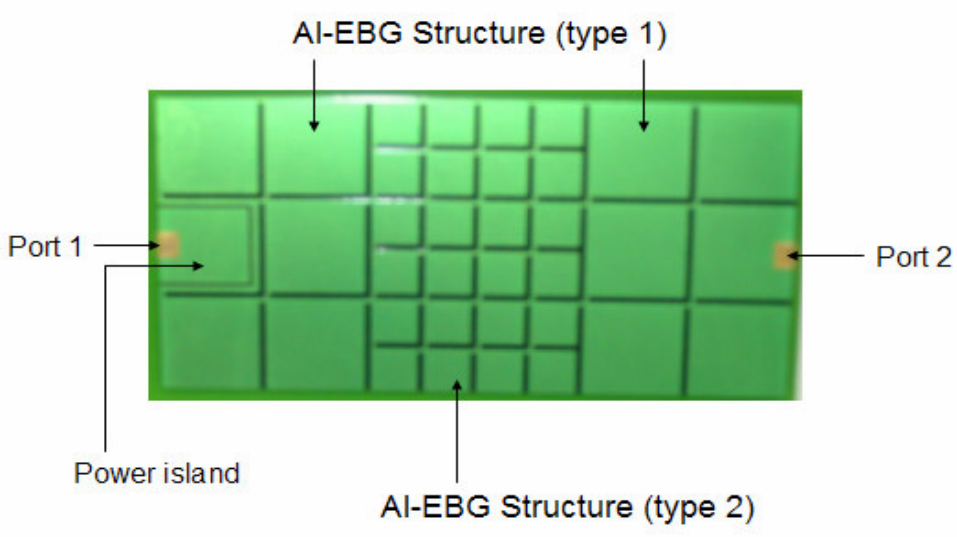


Figure 6.8 Photography of a novel structure for ultimate isolation.

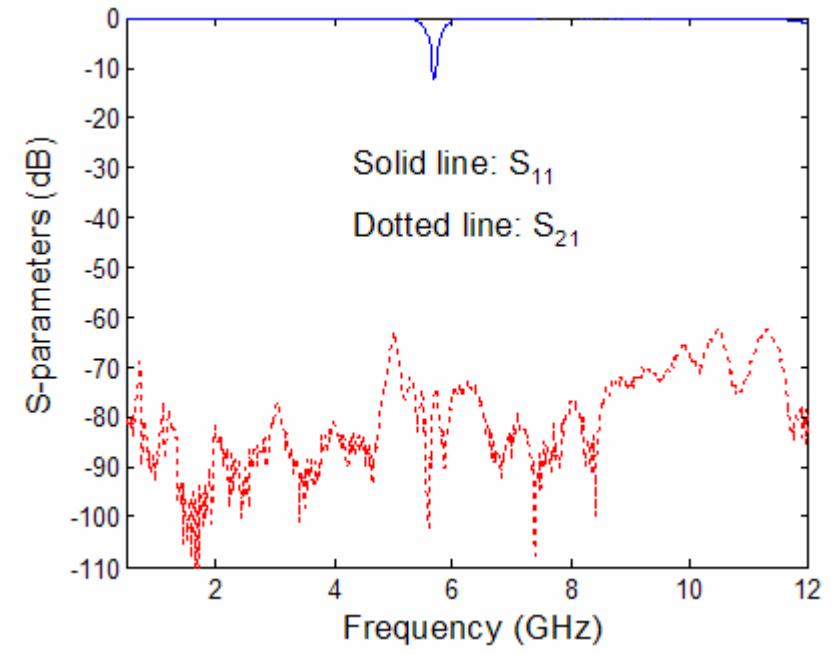


Figure 6.9 Measured S-parameter results for the structure in Figure 6.8.

6.6 Summary

In this chapter, novel hybrid AI-EBG structures were designed, simulated, fabricated, and measured. The measured transmission coefficients of the hybrid AI-EBG structures showed excellent isolation over ultra wide band (UWB) frequency range. It was also shown that the hybrid AI-EBG structure produced much better isolation than that of the mushroom-type EBG structure for UWB applications. The reason why the AI-EBG structure produces better isolation is because the AI-EBG structure is more optimized to make maximum wave interference in the structure and the reason why the AI-EBG structure produces a wider stopband is because the AI-EBG structure is naturally a low-pass filter, while the mushroom-type EBG structure is a bandstop filter. Moreover, these hybrid AI-EBG structures do not need additional metal layer and blind vias, which is proper for PCB applications.

CHAPTER 7

Conclusions and Future Works

In this dissertation, an efficient method has been developed using a novel electromagnetic bandgap (EBG) structure called the alternating impedance electromagnetic bandgap (AI-EBG) structure for noise suppression and isolation in mixed-signal systems. The integration of wireless technologies in handsets and mobile computers is forcing the integration of high-speed digital circuits with analog and radio frequency (RF) circuits. When the output drivers or internal logic circuits of a microprocessor switch simultaneously, the power supply noise generated from the noisy digital circuits can deteriorate the performance of sensitive RF/analog circuits. RF front-end circuits like low noise amplifiers (LNAs) need to detect low-power signals, and are extremely sensitive in nature. A large noise spike in or close to the operating frequency band of the device can de-sensitize the circuit, destroying its functionality. To prevent this, all radio architectures include filters and other narrow band circuits, which prevent the noise in the incoming spectrum from reaching the LNA. However, there are no systematic means for filtering noise from other sources – for example, noise can couple through the power rail and appear at the output of the LNA, where it can degrade the performance of the downstream circuits. Thus, an efficient noise suppression technique is required for isolating sensitive RF/analog circuits from noisy digital circuits.

The sensitivity of RF/analog circuits to power supply noise has resulted in difficulties for integration of digital and RF/analog subsystems. One common method used for mixed-signal integration in the package is splitting the power and/or ground

planes. The gap in the power and ground planes can partially block the propagation of electromagnetic waves. For this reason, split planes are usually used to isolate sensitive RF/analog circuits from noisy digital circuits. However, electromagnetic energy can still couple through the split, especially at frequencies greater than 1 GHz. Hence, this method only provides marginal isolation (-20 dB ~ -60 dB) at frequencies above ~ 1 GHz and becomes ineffective as system operating frequency increases. Further, as systems become more and more compact, use of multiple power supplies becomes expensive. The use of ferrite beads across the split can result in a common power supply; however, since ferrite beads resonate above 200 MHz, the coupling between split islands increases at higher frequencies. The power segmentation method was proposed recently, but this method only provides good isolation at high frequencies over a narrow frequency band and since this narrow frequency band is fixed by the size of the structure, this frequency band is not tunable. Hence, the development of noise isolation methods is required for enabling integration of mixed-signal systems.

The AI-EBG structure in this dissertation has been developed to suppress unwanted noise coupling in mixed-signal systems and this AI- EBG structure shows excellent isolation (-80 dB ~ -140 dB), which results in a noise coupling-free environment in mixed-signal systems. Moreover, the AI-EBG structure has the advantage of being simple and can be designed and fabricated using standard printed circuit board (PCB) processes without the need for additional metal layer and blind vias. The excellent noise suppression in mixed-signal systems with the AI-EBG structure has been demonstrated through measurements, which make the AI-EBG structure a promising candidate for noise suppression and isolation in mixed-signal systems. Signal

integrity analysis for the mixed-signal system with the AI-EBG structure has been described and a design methodology has been suggested for avoiding signal integrity and EMI problems. In addition to these, near field and far field simulation and measurements of the three test vehicles have shown that an embedded AI-EBG structure could be used for avoiding possible EMI problem. Finally, novel hybrid AI-EBG structures have been designed, simulated, fabricated, and measured and measured transmission coefficients of the hybrid AI-EBG structures showed excellent isolation over ultra wide band (UWB) frequency range.

The AI-EBG structure can be part of the power distribution network (PDN) in systems and is expected to have a significant impact on noise suppression and isolation in mixed-signal systems in the future.

As an extension to the work described in this dissertation, the following areas of research could be interest:

1. **Investigation of stopband control of any active device:** Without changing the size of the metal patch, it is interesting to change the stopband with any active device. Especially, it is useful if it is possible to move the stopband to low frequency range (for example, below 10 MHz) with any active device for a compact power/ground plane pair since a large metal patch size is required to move the stopband to the low frequency range and it is impossible to use a larger metal patch size than the size of a compact power/ground pair. This kind of stopband control by an active device could be possible if this active device can vary the capacitance of the device and therefore, vary the stopband range.
2. **Miniaturization of AI-EBG Structure:** This is important since available space

in PDN for AI-EBG structure could be limited in some applications. For miniaturization of AI-EBG structure, many approaches can be investigated. For example, if we use a material having a high dielectric constant as a dielectric material, capacitance of a metal patch increases and cutoff frequency moves to lower frequency since the cutoff frequency is inversely proportional to capacitance of a metal patch. Hence, for a given frequency range, it is possible to reduce the size of a metal patch and the area of the total AI-EBG structure to obtain the same isolation level.

APPENDIX A

PUBLICATIONS

[1] **J. Choi**, V. Govind, M. Swaminathan, K. Bharath, D. Chung, D. Kam, J. Kim, "Noise suppression and isolation in mixed-signal systems using alternating impedance electromagnetic bandgap (AI-EBG)," submitted to *IEEE Transactions on Electromagnetic Compatibility*, September 2005.

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[4] **J. Choi**, D. Kam, D. Chung, K. Srinivasan, V. Govind, J. Kim, and M. Swaminathan, "Near field and far field analysis of alternating impedance electromagnetic bandgap (AI-EBG) structure for mixed-signal applications," has been selected to be included in a special issue of *IEEE Transactions on Advanced Packaging* as one of an

excellent paper in 14th EPEP conference and will be submitted to *IEEE Transactions on Advanced Packaging*, March 2006.

[5] **J. Choi**, V. Govind, and M. Swaminathan, "Alternating impedance electromagnetic bandgap (AI-EBG) structure for noise suppression in ultra wide band (UWB)," will be submitted to *IEEE Microwave and Guided Wave Letters,* December 2005.

[6] **J. Choi,** V. Govind, and M. Swaminathan, "Ultimate isolation using novel hybrid alternating impedance electromagnetic bandgap (AI-EBG) structure," will be submitted to *Electronics Letters*, December 2005.

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[10] **J. Choi**, V. Govind, and M. Swaminathan, "Noise suppression and signal integrity analysis in mixed-signal systems with alternating impedance electromagnetic bandgap (AI-EBG) structures," *SRC TECHCON05 Conference*, Portland, Oregon, October 2005.

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APPENDIX B

Awards / Patents

1. **Semiconductor Research Corporation (SRC) Inventor Recognition Award** from SRC for his invention of a novel electromagnetic bandgap structure called alternating impedance electromagnetic bandgap (AI-EBG) structure for noise suppression and isolation in mixed-signal systems, SRC TECHCON05 Conference, October 2005.

2. **Certificate of Recognition** for the paper presented at *IEEE 7th Asia and South Pacific Design Automation Conference (DAC) & 15th International Conference on VLSI Design*, Bangalore, India, January 2002.

3. U.S. Utility Patent Application

   Title: An Electromagnetic Bandgap Structure for Isolation in Mixed-Signal Systems

   Serial No.: 10/936,774; Filing Date: September 8, 2004

   Inventors: **Jinwoo Choi**, Vinu Govind, and Madhavan Swaminathan

   Attorney Docket No.: 62020-1710; GT ID No.: 3142

4. U.S. Utility Patent Application

   Title: Design Methodology with Alternating Impedance Electromagnetic Bandgap (AI-EBG) Structures in Mixed-Signal Systems

   Filed as a provisional U.S. patent in April, 2005

Inventors: **Jinwoo Choi**, Vinu Govind, and Madhavan Swaminathan

GT ID No.: 3418

5. U.S. Utility Patent Application

Title: Mixed-Signal Systems with Alternating Impedance Electromagnetic Bandgap (AI-EBG) Structures for Noise Suppression/Isolation

Filing Date: October 17, 2005

Inventors: **Jinwoo Choi**, Vinu Govind, and Madhavan Swaminathan

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