

**DESIGN EXCHANGE FORMATS FOR ASSESSING OHMIC DROPS
AND THERMAL PROFILES IN THREE DIMENSIONAL
INTEGRATED CIRCUITS**

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The Academic Faculty

By

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INTEGRATED CIRCUITS**

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To my Grandparents

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SUMMARY

Three dimensional integrated circuits (3D ICs) fabricated with through-silicon vias (TSVs) have smaller planar dimensions, shorter wire length, and better performance than 2D ICs. Heat dissipation causing temperature increase has posed new challenges for design of 3D integrated circuits (IC). In addition to the thermal problem, 3D ICs also require careful design of power grids/network because many inter-tier resistive through-silicon vias in 3D IC can cause larger voltage drop than 2D ICs. The performance optimization of a 3D stack requires validation of thermal and electrical integrity during the co-design.

Many 3D stacks will combine digital and analog circuitry, requiring a strong mixed-signal design approach. This will require close collaboration between different domains of circuit fabrication which traditionally have been working separately. Hence there must be some standards to facilitate smooth and effective design of 3D ICs.

In this thesis, we perform steady-state electrical and thermal simulations to analyze the properties of a 3D stack. We optimize electrical and thermal performance using genetic algorithm to achieve optimized power map profile for minimizing voltage drop and temperature, which can benefit both thermal and power integrity management.

This thesis presents initial efforts in designing such standards. Steady state electrical and thermal simulations are performed to demonstrate the necessary information that needs to be exchanged between the dies to ensure adequate co-design. The main purpose of a Design Exchange Format (DEF) between dies is to permit sharing of information necessary for design by external parties without disclosing their intellectual property (IP). The requirements of the standards should be the minimum necessary to produce satisfactory answers. Producing such models is just a customer support function. The role of the standards is to facilitate the transfer of information through a compact model, not necessarily to build one.

CHAPTER 1

INTRODUCTION

The increasing demands of multifunctional portable devices have made engineers think beyond the traditional chip fabrication technology. Moore's law has been the guiding principle for electronics industry for many decades. Figure 1.1 shows the Moore's law which states that the number of transistors on a chip will double approximately every two years.

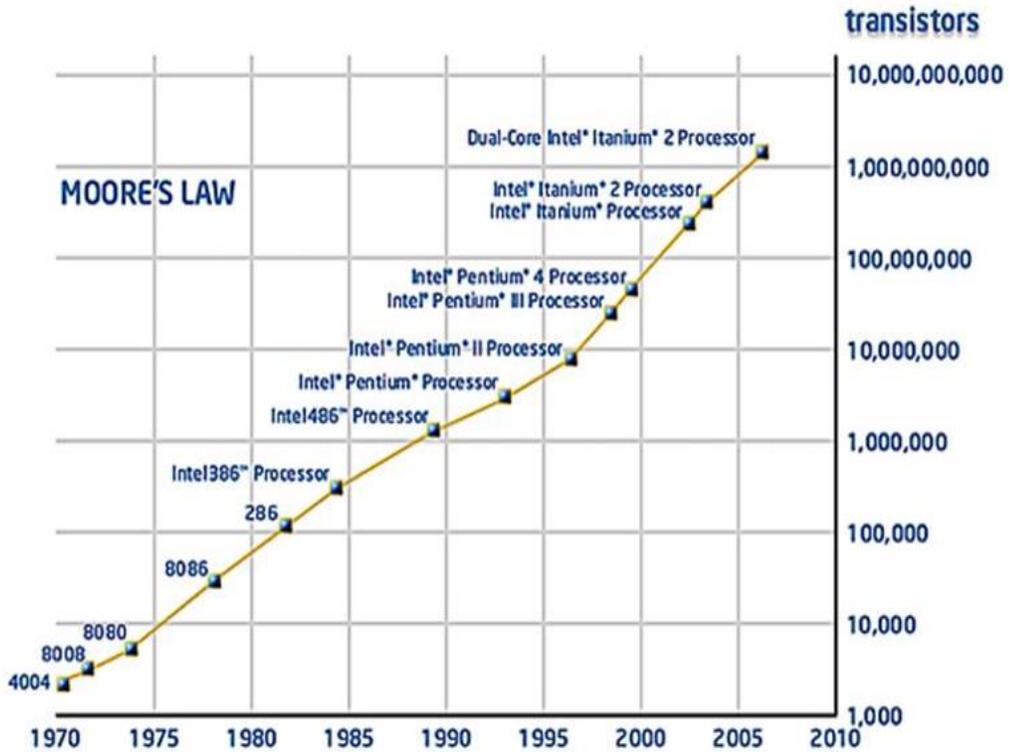


Figure 1.1: Moore's Law [1].

With transistors reaching upto atomic scale Moore's law may soon be hitting a wall. With silicon chips hitting the thermodynamic and quantum limits, Moore's law is on the verge of saturation in next decade or so [32].

However history has proven time and again that realization of Moore's law drives us to new levels of innovation. So, following the trend of the semiconductor industry the successor to present System on chip (SOC) technology could very well be Stacked ICs and Packages (SiP). SiP which means stacking of either bare chips or packages in three dimensions enables system miniaturization. Its applications are similar to those of IC integration namely high volume integration and multifunctional manufacturing of portable devices. If integration along two dimensions seems to have reached saturation, then why not start cramming more components along the third dimension using SiP technology. The International Technology Roadmap for Semiconductors (ITRS) has identified SiP as a way of improving the performance without further shrinking the transistor dimensions.

1.1 System in Package/Stacked ICs and Packages (SiP)

In contrast to SoC, system-in-package (SiP) is characterized by any combination of more than one active electronic component (package or die) of different functionality, plus optional passive devices and other devices such as MEMS or optical components. All components are assembled into a single package and provide the multiple functions associated with a system or subsystem. Figure 1.2 shows integration of a processor and a Near Field Communication (NFC) chip using wire bonds from Samsung using a Fine Pitch Ball Grid Array package (FBGA) [33].

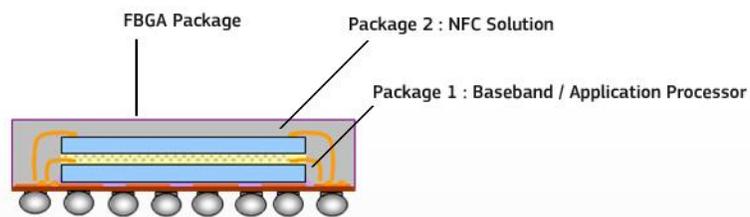


Figure 1.2: Example of SiP, security solution from Samsung [33].

Key areas of application for SiP designs include wireless products (GPS modules, Bluetooth solutions, 802.11 modems) and portable products where there is a need for a combination of large memory (SDRAM, flash, SRAM), and digital-logic or mixed-signal designs that require very sophisticated analog design. The future of SiP also includes electronic market sectors such as smartphones, flat panel LED TVs, automobiles, high end computers to name a few. Nano scale biosensors, personal healthcare and environment sensing modules are emerging SiP markets. All the above technologies involve density of thousands of functions per cubic centimeter.

SiP is mainly divided into two broad categories. Non-TSV (Through Silicon Via) and TSV based solution. Concept of SIP originated from Bell Labs 40 years ago. However, first functional SIP came in 1992 from Irvine Sensors. Non-TSV SiP has grown in parallel with IC chip packing from DIP (Dual Inline Package) to JLCC (J-leaded chip carriers). Non-TSV based SiP is further discretized into chip and package stacking. Advancement in chip stacking is has come from the ability to stack more and more dies in a given height. Wafer thinning by grinding or chemical polishing, wafer handling and thin wafer dicing are the key technologies that help us achieve the above goals. Non-TSV integration can be achieved in four different ways.

- **Wire bonding** includes traditional wired connections between multilevel chips. Several key features like spacer technology, die adhesives, molding and type of bonding (forward/reverse) have to be taken into considerations for application specific requirements.

- **Flip chips** came as an alternative to wire bonding allowing higher connection density. They can be used with wire bonding for faster communication or independently as in case of Chip on Chip (CoC).
- **Side Termination** requires metal routing on chip edge. Its three variations depends on interconnections namely metallization, polymer or a solder bump. In embedded ICs, the IC is embedded into the silicon substrate for further miniaturization.
- **Tape Automated Bonding (TAB)** is common for chip to substrate bonding. It uses metallized flexible polymer for bonding.

Each of the above mentioned variation has its own pros and cons. Wire bonding has wiring density issues when chips increase in number. Flip chips are faster but, they are costly. Embedded ICs can incorporate thin film passives like capacitors and inductors. Yield is an issue with them. TAB increases package size and the number of fabrication processes. Package Stacking has three variations namely,

- **Package on Package (PoP)**, in which individual packages are stacked on top of each other. At sidewalls conductive epoxy is applied.
- **Package in Package (PiP)** involves flipping of the top die (tested package) with internal interconnections via wire bonding.
- **Folded Scale Chip Stacked Package (FSCSP)** use thin flexible flpsubstrate. A chip is mounted on one half of the substrate and the remaining of the flex is folded over the chip.

However all the aforementioned packaging techniques have some manufacturing issues. PoP is simple and best among the three, but it adds to package size. PiP is limited to expansion to additional package once the final die has been fabricated. FSCSP is

limited by the cost and availability of double sided substrates. Figure 1.3 shows various forms of SiP integration techniques.

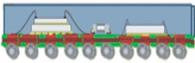
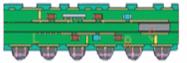
Chip/component configuration	Technology
Side-by-side placement	<p>Substrate: organic laminate, ceramic, glass, silicon, lead frame </p> <hr/> <p>Chip interconnection: wire bond and/or flip chip</p> <p>Plus passive components → integrated into the substrate discrete (chip-scale package, surface-mount device) </p>
	<p>Package-on-package Package-in-package </p> <p>Stacked die → wire bond, wire bond plus flip chip  </p> <hr/> <p>Chip-to-chip/wafer → flip chip, face to face through silicon wafer-level 3-D stack wafer to wafer </p>
Embedded structure	<p>Chip in pcb/polymer → single layer multilayer 3-D stack </p> <hr/> <p>Wafer-level thin-chip integration → single layer stacked functional layers </p>

Figure 1.3: Different types of System in package design. [2]

A vital problem for SoC development is the integration of increasingly sophisticated IP into the design. Even if integration is achieved, a lot of effort must be given to verification, which takes major portion of the design cycle and requires costly and sophisticated EDA tools. In addition, as chips become more complex, there's an immediate requirement for advanced silicon processes to attain smaller die size and lower power. These cutting- edge processes entail significant research and production costs, and even more costly EDA tools. SoC often requires long development time required for front-end design and verification as well as backend placement and routing.

SiP development is shorter since the components don't require as much design verification (at the functional level). But many of the EDA tools for high-speed mixed

signal system designs compatible with SiP aren't commercially available. Thus, they require in-house development. Moreover, EDA tools covering mechanical aspects of SiP are still in an embryonic stage [39]. There are no simple answers for choosing between a SIP or SOC solution. The key to making the best choice is to impartially understand the pros and cons of each option. One can use the SiP approach when complex semiconductor components are to be integrated in a single system and a short time to market is critical. While, the use of SoC can be favored for high-volume production and long-life applications in which high performance is essential [38].

Table 1.1 shows the comparison between currently prevailing SoC technology and the future SiP technology.

Table 1.1: Comparison between SoC and SiP [2]

	SoC	SiP
Power	Low	Medium
Performance (Clock Speed)	High	Medium
System Design Flexibility	Low	High
IP availability		High
Unit Cost	Low	Medium
Development Cost/Time	High	Low-Medium
EDA Tools	Mature	Limited
Available Design Services	High	Limited

One of the most important advantages of 3D ICs is that it allows the integration of different IC technologies like analog, digital, radio frequency (RF) and memory into one package, resulting in more functionality in a given volume. Traditionally these different chips are interconnected using common chip assembly technologies like wire bonds, tape automated bonding (TAB) or flip chip technology.

Through Silicon Vias (TSVs) have been recognized as one of the major technologies to achieve 3D integration of heterogeneous ICs for next generation devices. A through-silicon via is a vertical electrical connection passing completely through a silicon wafer or die. TSVs are a high performance technique used to create 3D packages and 3D integrated circuits, compared to alternatives such as package-on-package, because the density of the vias is substantially higher, and because the length of the connections is shorter. TSVs enabled chips can be stacked vertically, thus reducing the interconnection length due to the thickness of die. Memory can be stacked directly over processor to provide high speed and low loss memory-logic interface.

Current technology uses an intermediate level between traditional 2D and 3D assembly, known as 2.5D integration. It is a stepping stone towards the ultimate goal of ‘true 3D’ integration. The main difference between a conventional 2D IC and a 2.5D IC as shown in Figure 1.4 below is that, in the case of the 2.5D IC, a passive silicon interposer is placed between the substrate and the active dies, where this silicon interposer has through-silicon vias connecting the metallization layers on its upper and lower surfaces. This approach enables much denser interconnections between dies than would be possible with packaged parts, as well as cutting signal latency and power consumption [34]. In 2011 Xilinx announced a single layer, multi-chip silicon interposer for its 28nm 7 series FPGAs. It uses a 100 μ m thick, silicon interposer with 45 μ m pitch micro bumps and 10 μ m TSV. The FPGA slices are connected by ~10,000 connections created on the silicon interposer. Compared to connections on a PWB, the interposer interconnect technology provides over 100 angstrom the die-to-die connectivity bandwidth per watt, at one-fifth the latency [35].

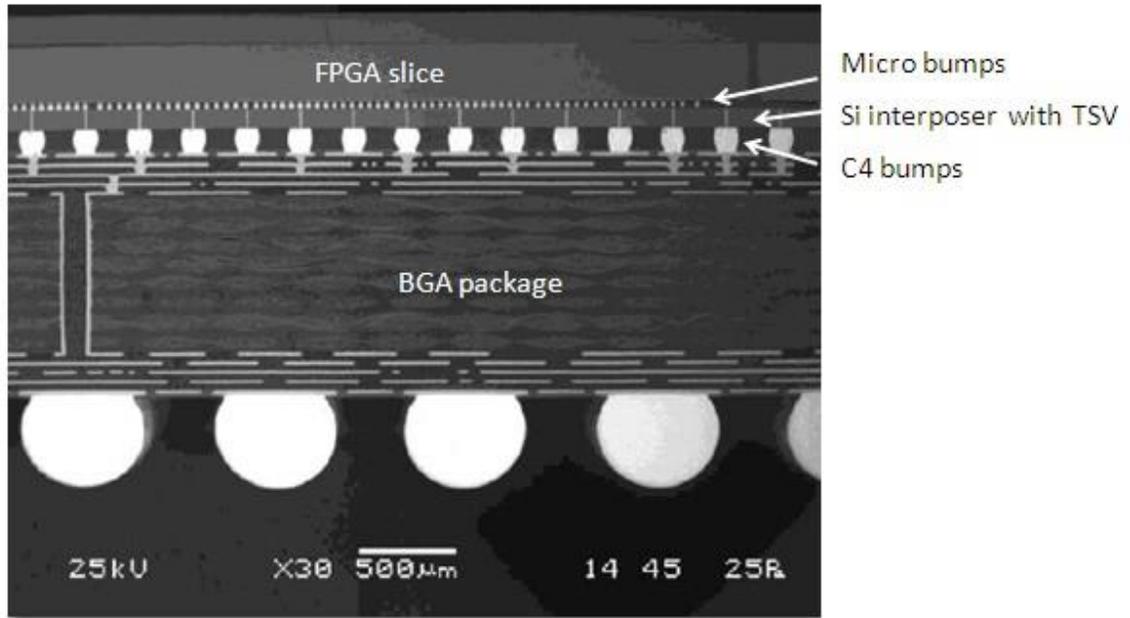


Figure 1.4: Xilinx Virtex 7 FPGA using 2.5D integration. [35]

1.2 Challenges with 3D Integration

2.5D/3D ICs with TSVs do not require radical new changes. The silicon interposer can be fabricated with the current process technology and the memory/processor cores can continue using the traditional CMOS process. But 3D integration does require some new capabilities that need to be added for analog/custom design and IC/package co-design. The end goal is similar to current SoC technology, i.e. to optimize system cost with the shortest possible turnaround time. If 3D ICs cannot be both cost and time effective, they will suffer from premature extinction.

In comparison to conventional 2D circuits, 3D ICs provide the possibility for extremely increased levels of integration in the given circuit area. This creates stern design bottlenecks in the areas of thermal and power delivery management. First, due to highly dense integration, the amount of heat per unit area or the heat density increases, resulting in higher on-chip temperatures. Second, the power to be delivered to a 3D chip

is tremendously increased due to vertical alignment of ICs, leading to significant complications in the task of reliable power delivery. An n -tier stack will consume n times the power as compared to its 2D counterpart for the same footprint area. Moreover, through-silicon vias contribute additional resistance to the supply network. Increased current density due to small TSV cross section and difference in interconnect dimension mismatch in a 3D stack can lead to electro migration failures [36].

Many 3D stacks will combine digital and analog/RF circuitry, requiring a strong analog/mixed-signal capability. Because of the unique packaging requirements of stacked die, an IC/package co-design capability is a must. Thus, anyone who presents a complete “solution” must provide proficiency in digital, analog IC, package, and PCB design [3]. 3D IC design is a shared effort. The logic IC designer knows where to place pins, but knows little about the design of the memory IC. The memory IC designer can put TSVs inside the die, but has limited knowledge of the logic IC. 3D ICs will require close collaboration and co-design among groups that have historically worked separately. TSVs have some special tooling requirements. TSVs in active layers must be designed by IC design tools. However, TSVs in active layers may be planned with packaging or SiP tools. TSVs in passive layers may be both planned and designed with packaging or SiP tools. Figure 1.5 shows a general TSV based 3D IC.

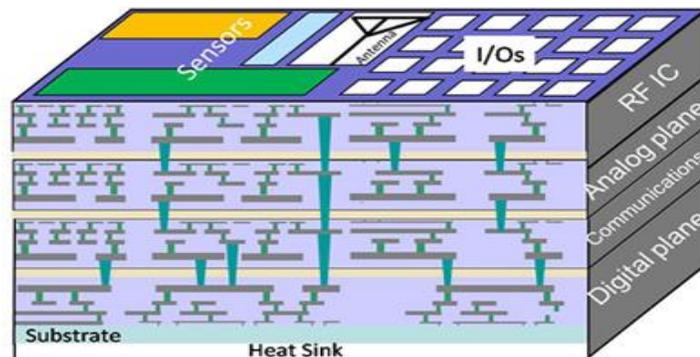


Figure 1.5 Schematic of a heterogeneous 3D IC stack. [4]

This thesis deals with two major issues which are required to effectively design the next generation 2.5D/3D ICs namely,

- Pathfinding and Optimization.
- Heterogeneous IC co-design.

1.3 Pathfinding (Exploration) and Optimization

3D stacked chips are becoming a promising system integration technology for modern systems. The use of multi-processor systems has increased the communication delays between processor cores, and an effective way to reduce this impact is 3D integration technology and the use of through-silicon vias for inter-layer communication. However, 3D chips present important thermal issues due to the presence of processing units with a high power density, which are not homogeneously distributed in the stack. Also, the presence of hot-spots creates thermal gradients that impact negatively on system reliability and lead to increased leakage power consumption. The location of power cells in each chip impacts the distribution of the temperature profile of the complete stack, and the arbitrary distribution will lead to a large temperature gradient, thus degrading its performance and reliability.

3-D ICs also pose challenges for power delivery network design due to larger supply currents and longer power delivery paths compared to 2-D ICs. Power delivery must provide sufficient current to each module and reduce IR-drop, i.e., the DC voltage drop during normal operation. This drop is one of the dominant causes of power-noise issues in 3D ICs. Pathfinding can help in determining where functionality goes in a die. It can help designers to find a sweet spot in their design technology and choose the best die

order in the stack. Pathfinding can aid in optimizing connectivity between chips by carefully placing the TSVs between the dies.

1.4 The Co-Design Problem

Three dimensional integrated circuits (3D ICs) built with through-silicon vias (TSVs) have smaller planar dimensions, shorter wire length, and better performance than 2D ICs. Many 3D stacks will combine digital and analog/RF circuitry, requiring a strong analog/mixed-signal capability. Because of the unique packaging requirements of stacked die, an IC/package co-design capability is required. Hence there must be some standards to facilitate smooth and effective design of 3D ICs.

Developers of 3D ICs need to remember that a 3D IC will include ICs with different functionality. Designing one of the chips first and throwing it “over the wall” to other chip designers will not result in design convergence or an optimal, cost-effective solution. If the different chips are not designed co-operatively, the interconnect will not be optimized, and extra vias will be needed to handle signals that cross from one point to another. Without co-design, timing, power, and signal integrity will not be optimized. IC/package co-design is important for 3D ICs because there are a large number of I/Os, and because the cost of packaging goes higher with multiple die in one package. Without co-optimization, the package could end up costing more than the silicon die. Important capabilities include I/O feasibility planning, connectivity management, 3D visualization, SiP layout, and support for multi-fabric analog and RF circuitry [3].

The board must be considered as well. 3D die stacks result in additional interconnect that will have to find its way down to the board. As more connectivity is handled inside the package, there’s less complexity on the board. The board designer needs to know

what's going to be positioned near the 3D package. By positioning and rotating components properly, the designer can reduce the number of layers required for the board.

This thesis provides evaluation of voltage drops and temperature gradients for the proposed Design Exchange Format (DEF). DEF can act as a standard for exchange of information between different die vendors for efficient design of a 3D stack without disclosing their sensitive Intellectual Property (IP). Standards will become an important part of the 3D IC ecosystem. An initial effort may focus on defining nomenclature of data that need to be exchanged between different vendors. Such information can include the voltage/current profiles, voltage drop and thermal gradient limits. Down the road, detailed I/O standardization between interfaces such as memory, logic, and interposer layers can be established for better and much deeper level of information exchange.

Meanwhile, the 3D-IC Alliance³ is focusing on the manufacturing side, and has released the Intimate Memory Interconnect Standard (IMIS) [37] to standardize vertical interconnect requirements.

1.5 Thesis Outline

The thesis outline is as follows: Chapter 2 discusses optimization of power and TSV maps for thermal and power integrity. In this chapter, the power map optimization is achieved by using genetic algorithm. TSV optimization is done using iterative removal of residual TSVs. Key results for early pathfinding and , importance of electrical and thermal co-optimization are summarized in this chapter.

Chapter 3 demonstrates a scheme to define the proposed exchange formats for three dimensional ICs. Steady state DC IR and thermal simulations are performed to estimate the ohmic drop and temperature gradient for validation of the design exchange format.

Chapter 4 summarizes the research that has been done. It also discusses the future work and improvements that can be done based on the present work.

CHAPTER 2

OPTIMIZATION FOR THERMAL AND POWER INTEGRITY

2.1 Introduction

In the past, a considerable amount of thermal placement/optimization methods have been proposed for minimization of 2D/3D on-chip temperature gradients [9-17]. These proposed methods include the force-directed method [10], transformation-based 3D placement [11], partitioning-based 3D placement [12], and placement algorithm based on fuzzy set theory [10]. With regard to IR drop analysis, the work in [18] investigates the effect of number of power/ground bumps and power TSVs on IR drop. The work proposed in [19] considers deadspace redistribution of thermal TSVs. Insertion of dead space insertion and distribution of signal and thermal TSV during floor planning is proposed for voltage drop optimization [20]. The study in [19] considers buffer and signal-TSV insertion.

In this chapter, optimization on temperature and voltage drop for a 3D stack using genetic algorithm (GA)-based optimization method is performed. Most of the aforementioned proposed methods try to improve the temperature profile by altering the whole stack, such as placing the high power blocks on dies closer to the heat sink. Moreover, some of the techniques reported earlier do not take the effect of TSVs into account while others model them with effective thermal conductivities. None of the methods deals with the scenario when both dies have nearly equal power or the total power consumed by a die should remain constant. In addition, the constraint on the TSV positions between die to die can exist when dies are manufactured by different chip

vendors. The vendors can move around devices in their dies, but devices cannot be moved across dies that are designed by different vendors. Hence, the power map on individual die can change with constant total power consumption. This chapter presents optimization on a 3D stack comprising of a PCB, an interposer, and redistribution layers (RDL), two dies, and TSVs in interposer and in dies. To aid pathfinding, optimization for power map is performed on the bottom dies to obtain the minimum possible voltage drop on the die. Similar investigation and optimization is performed for steady-state thermal analysis.

2.2 Need for Optimization

3D stacked ICs utilizing short TSV interconnections provides reduced communication delays between dies and improved system performance, compared to 2D ICs [5]. 3D stacked ICs comprising of many stacked dies, TSVs, and bonding layers using micro bumps is shown in Figure 2.1. Because of vertical stacked active transistor layers, heat density of a 3D stack can increase dramatically causing rapid temperature increase [6, 7], particularly for high power-density applications. In addition, the low thermal conductivities of under fill/glue layers and back-end-of-line (BEOL) layers can make the thermal problem even worse [8]. On the other hand, the continuous increasing power density demands sufficient amount of current to be supplied to ICs. In a 3D stack, the power delivery requires current to be supplied to all transistor layers by routing through multiple inter-tier TSVs. These multi-tier resistive TSVs can cause increased voltage drop, compared to 2D ICs. In addition to DC voltage drop, the current carrying capability of TSVs also requires limiting current when designing and optimizing the power delivery networks for a 3D stack. The current needs to be limited to avoid electromigration

failures. Electromigration is the gradual transfer of metal when high direct current density is used. This can result in the eventual loss of connections or failure of a circuit

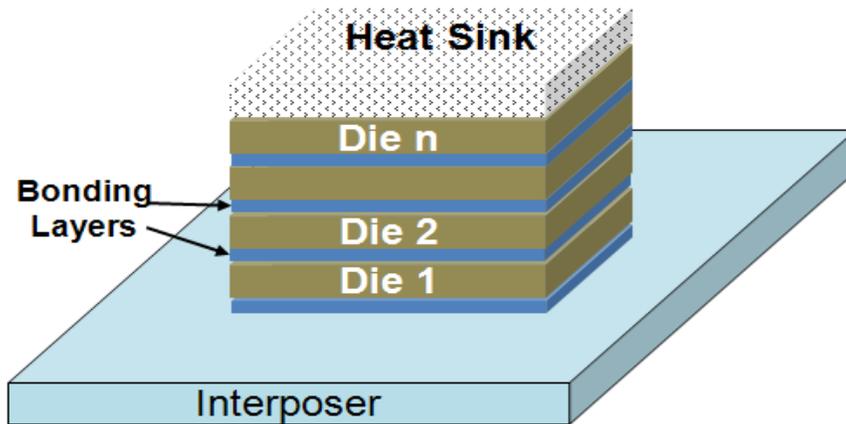


Figure 2.1: 3D stacked dies using TSVs and micro-bump/bonding layers.

2.3 Structure Setup

The structural configurations for thermal and electrical simulations are shown in Figure 2.2 and Figure 2.3, respectively. As shown in Figure 2.2, in the 3D stack, dies are connected in face-to-back configuration using TSVs and micro bumps [22].

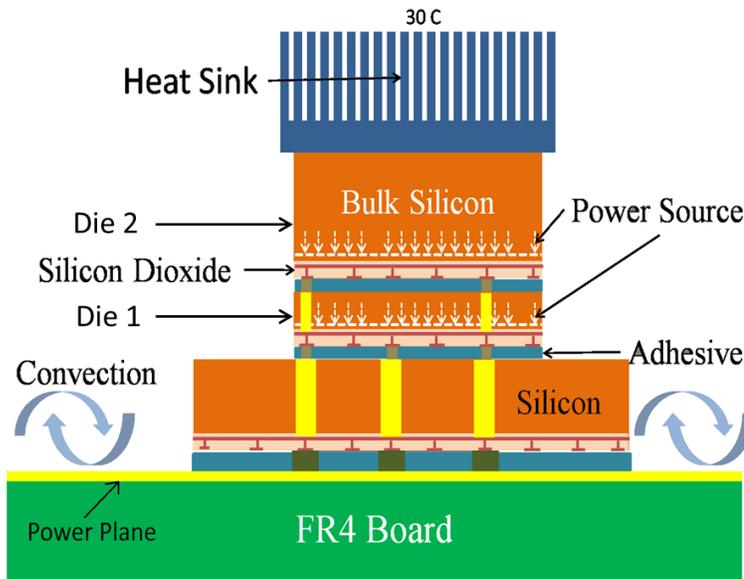


Figure 2.2: Structural configuration for thermal simulation

Each die contains one set of redistribution layers and TSVs. For the top die, no TSVs are required. In addition to metal RDL, each die consists of two layers: silicon dioxide insulator and a silicon substrate. The interposer and the two dies are bonded together using micro bumps with underfill. Block-wise power densities are defined for each die to represent the power consumption of active devices. The interposer is connected to the PCB power plane through bumps. Table 2.1 provides the details of geometrical information and material properties used in thermal simulation. Constant temperature boundary condition is used at the top surface of the top die to represent the ideal heat sink with a constant temperature of 30 Celsius. Convection boundary condition with a heat transfer coefficient of $10 \text{ Wm}^{-2}\text{K}^{-1}$ is used on top surface of the PCB, as shown in Figure 2.2.

Table 2.1: Geometrical information and material properties for thermal simulation.

	Size (mm ²)	Material Thickness (μm)	Thermal Conductivity (W/(mK))
Silicon die	1.1x 1.1	100	110
Bulk Silicon	1.1x 1.1	500	110
Adhesive	1.1x 1.1	50/20	0.3
PCB	10 x 10	800	4.3
Silicon Dioxide	1.1x 1.1	10	1.3
Copper Power Plane	10 x 10	30	400

In the electrical simulation configuration shown in Figure 2.3, the RDL comprises of two layers of metal grids placed orthogonally on top of each other. Power and ground traces alternate in each layer. The corresponding power/ground grids in each layer are connected to each other through metal connectors, which are referred to as micro-interconnects.

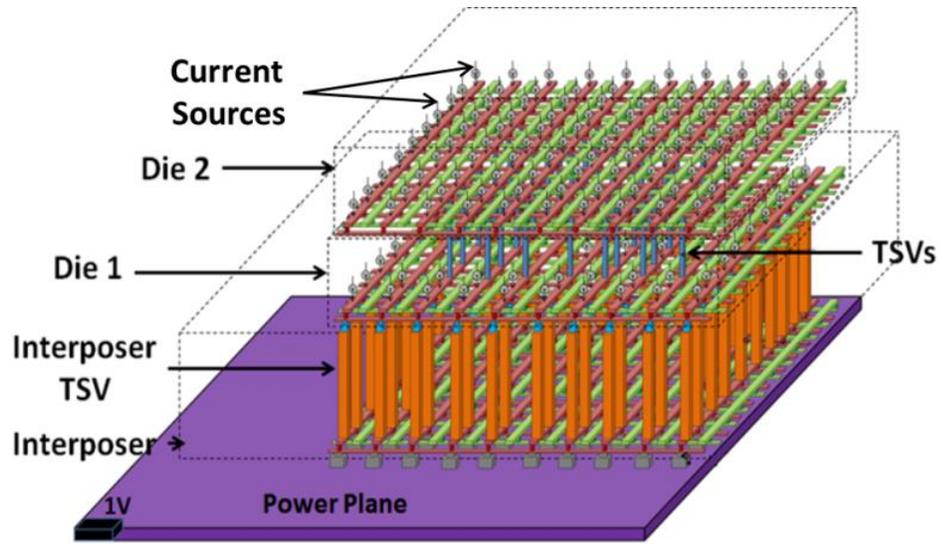


Figure 2.3: Structural configuration for DC voltage drop simulation.

A voltage source is placed at the bottom corner of the PCB power plane. Current sources at specific positions (Figure 2.3) in RDL are used to represent active devices. For a given amount of power density P , die area A , and input voltage V , the current value I for each block can be calculated as

$$I = \frac{P \cdot A}{V} \quad (2.1)$$

Table 2.1 provides details about the structures used in the IR drop stimulation.

Table 2.2: Component details for voltage drop simulation.

Components	Connection	Area	Height (μm)
Bumps	Power plane to interposer	50 x 50 μm^2	50
Interposer TSVs	Interposer to micro-bump	30 x 30 μm^2	200
Die TSVs	Die1 to Die 2	10 x 10 μm^2	100
Micro-Bumps	Interposer to Die 1	20 x 20 μm^2	20
Die 1, Die 2	-	1.1x1.1 mm^2	100
Power Plane	-	10 x 10 mm^2	30
Interposer	-	3 X 3 mm^2	200

For both the configurations for electrical and thermal analysis, all components including bumps, micro-bumps, and TSVs have rectangular cross-section. The RDL layer has a length L of 3 mm in interposer and 1.1 mm in stacked dies. The thickness T of the power/ground grid conductor is $1 \mu\text{m}$. The width W is $10 \mu\text{m}$, and the pitch P , the gap between power and ground conductors, is set to $50 \mu\text{m}$. The pitch between TSVs is $100 \mu\text{m}$. Figure 2.4 shows the modeled RDL structure.

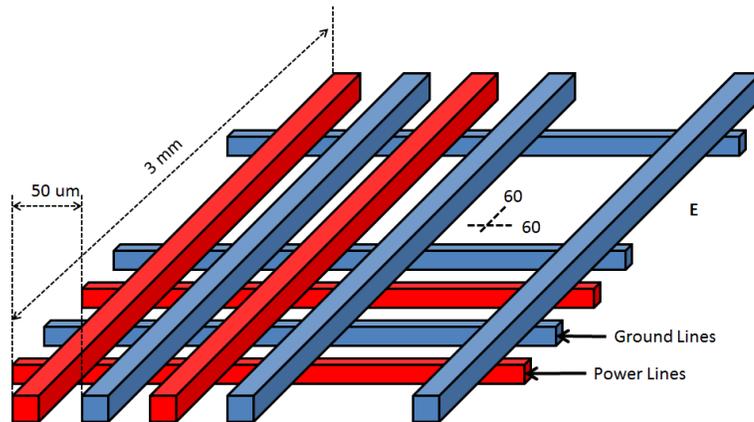


Figure 2.4: Structural configuration RDL layer.

In voltage drop simulation, the PCB, substrate, and TSV dimensions are the same as that used for thermal simulation. A finite volume-based solver [22-24] is used for both DC voltage and thermal simulations in this thesis.

2.4 Algorithm for Steady State DC and Thermal Optimization.

It is well known that the location of dies in a 3D stack can play a vital role in heat dissipation if dies consume different powers. However, if two dies in a 3D stack consume nearly the same power, the positioning/placement of blocks with non-uniform power maps on dies can have a substantial impact on temperature, which can affect the delay and leakage power. In addition to temperature increase, heat generation can cause mechanical issues such as thermal-induced stress, which can lead to mechanical fractures

in the stack [25]. Minimizing IR drop in a 3D stack plays a vital role in proper functioning of a system. Because of the shrinking of device and interconnect size, interconnect resistance increases by a large amount. While keeping the interconnect dimensions small, maintaining required voltage drop margin has become one of the key factors in the proper functioning of a 3D stack [18].

A genetic algorithm based optimization technique has been used here for optimization of both thermal and electrical response. Genetic algorithm (GA) [26] is preferred over other optimization algorithms such as calculus-based algorithms, for GA is a global optimization algorithm that does not depend upon initial conditions. GA does not collapse even if inputs change slightly [26]. Figure 2.3 shows a general flowchart of genetic algorithm-based optimization.

For thermal optimization, the power map consists of a 5×5 array, a total of 25 blocks of equal area. An initial population is generated by keeping the total power consumed by all members of the initial population constant. After temperature distribution is generated using the finite- volume solver from the initial population, the two best power maps that yield the lowest temperatures are selected as parents for the next generation. The power blocks are randomly selected from each parent to form a next generation. This process is referred to as crossover. There is a strong chance that the power consumed may change after each crossover. Therefore, after each crossover, the power map is re-normalized to keep the total power consumption constant. Mutation is performed by swapping some power blocks in each offspring. The next generation is again fed to the simulator to obtain the thermal profile of the next generation. The above process is repeated till a steady value of die temperature is reached.

Similar procedure is used for DC IR drop optimization. IR drop analysis with current sources is simulated in a 10×10 mesh array. Table 2.3 briefly describes the setup for the optimization engine

Table 2.3: Optimization engine setup for simulation.

	Power map (Thermal)	Power map (IR drop)
Population Mesh	25 blocks (5x5 mesh)	100 current sources (10x10 mesh) placed on RDL
Constant Parameters	TSV distribution, total power consumed by each die	TSV distribution, total power consumed by each die
Optimization Goal	Minimizing the maximum temperature on the bottom die.	Minimizing the voltage drop on the bottom die.

- **Genetic Algorithm (GA) Topology [26]**

1. *Chromosomes*: A chromosome represents one of the many possible solutions to the problem being solved. Chromosomes are various power maps that are used as initial inputs to the solver. Figure 2.5 shows one of the power maps for thermal profile. Each of the A_i s represents power densities in a particular area.

A_1	A_2	A_3	A_4	A_5
A_6	A_7	A_8	A_9	A_{10}
A_{11}	A_{12}	A_{13}	A_{14}	A_{15}
A_{16}	A_{17}	A_{18}	A_{19}	A_{20}
A_{21}	A_{22}	A_{23}	A_{24}	A_{25}

Figure 2.5: Power map for thermal simulation (in W).

2. *Population*: Population represents the set of possible solutions used in GA. It is equal to the number of chromosomes Figure 2.6 illustrates the initial population for the engine. GA works on to evolve the given solutions to better and more optimal solutions.

3. *Cross over*: Cross over is one of the steps in GA where the two best chromosomes interact to give rise to a third chromosome. The two chromosomes involved in cross over are called parent chromosomes, while the new chromosome produced is called

the child/daughter. The percentage of inheritance from each parent is determined by the cross over location which is random. The probability of cross-over happening is called cross over rate. In Figure 2.7 the daughter contains cells from both parent A and B.

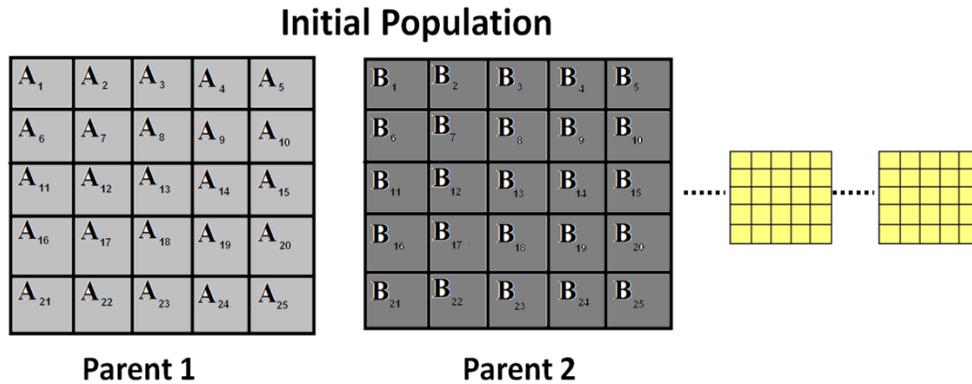


Figure 2.6: Initial population.

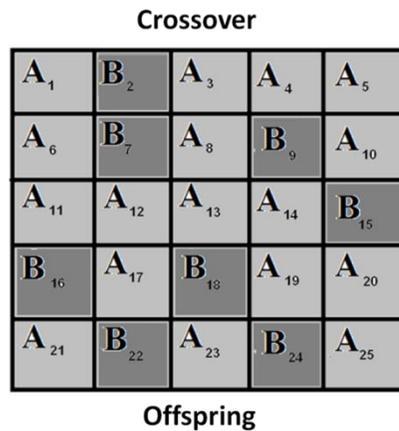
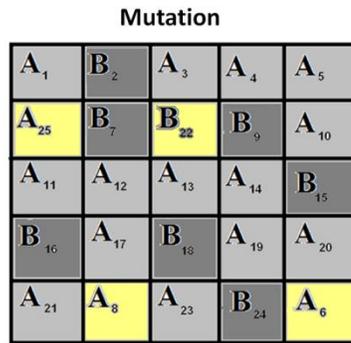


Figure 2.7: Depiction of cross over.

4. *Mutation:* To avoid convergence to local optima at the expense of global optima, random changes are introduced in the off springs produced after crossover [27]. These random changes are called mutation. Mutation causes a random change in chromosome causing a modification in the solution. Small changes increase the probability of solution converging but the convergence is more likely towards local optima. On the other hand, large changes increase the probability of solution converging to global optima, at the expense of rate of convergence. The probability of mutation happening called the mutation rate can be also be controlled to alleviate the

problem of solution converging to local optima. Figure 2.8 shows the mutation process, where A_{25} is swapped with A_6 and B_{22} is swapped with A_8 .



Mutated Offspring

Figure 2.8: Depiction of mutation.

The flow chart of GA applied to power block problem is shown in Figure 2.9. The various steps of GA are explained below the flowchart.

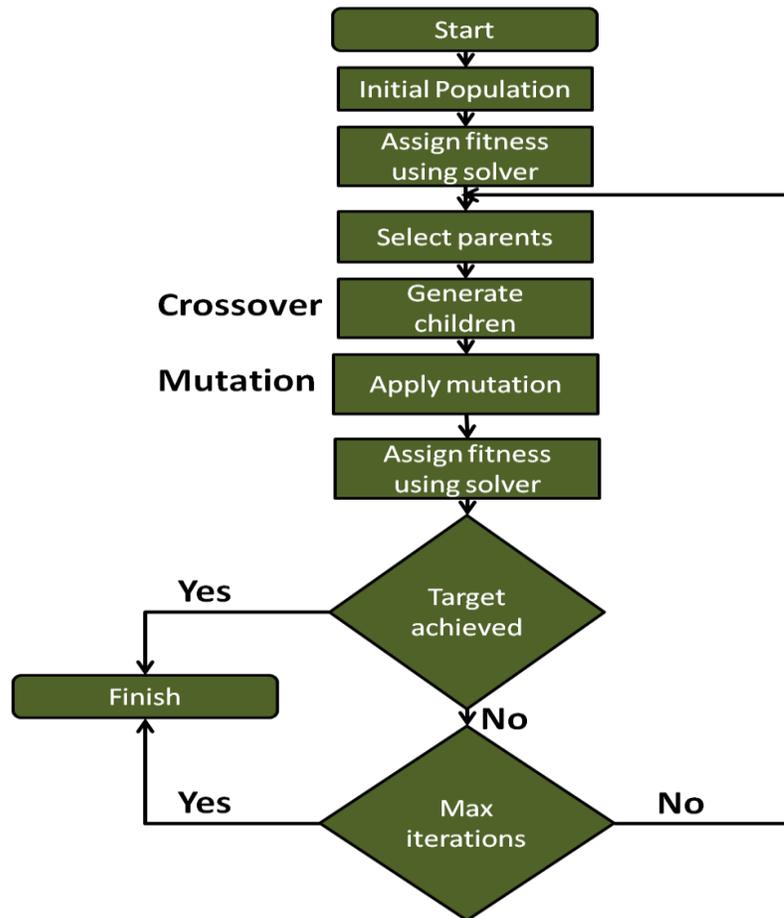


Figure 2.9: Flow chart of genetic algorithm.

1. The inputs to GA include:
 - The Structure file containing material properties, RDL layers and TSV locations, maximum iterations.
 - *GA population*: GA populations controls the number of solutions GA has to work to evolve them into better solutions. A high value of population requires larger run time, but might lead to faster convergence.
 - *Cross over rate*: The probability of cross over can be specified using the cross over rate.
 - *Mutation rate*: The probability of mutation can be specified by specifying the mutation rate.

For thermal optimization, the power map consists of a 5x5 array, a total of 25 blocks of equal area.

2. Initial Population: An initial population is generated by keeping the total power consumed by all members of the initial population constant.
3. Checking if specifications are met: If the solution with highest fitness meets the specification or if number of iterations equal the maximum allowed iterations, the algorithm terminates with output as the solution with highest fitness. If the specifications are not met and more iterations are allowed, the algorithm goes to the next step - Pruning.
4. Crossover: The power blocks are randomly selected from each parent to form a next generation. This process is referred as crossover. There is a strong chance that the power consumed may change after crossover. Therefore, after each crossover, the power map is re-normalized to keep the total power consumption constant.
5. Mutation: It is performed by swapping some power blocks in each offspring. The next generation is again fed to the simulator to obtain the thermal profile of the next generation. The above process is repeated till a steady value of die temperature is reached.

2.4 Simulation Setup

In the analysis, the power map of die1 in Figure 2.2 is to be optimized while the power map of die 2 (top die) is kept constant. Figure 2.10 shows the power map for die 2. Two TSV maps in which TSVs going from die 1 (bottom die) to die 2 are used in the simulation. The two different TSV maps are shown in Figure 2.11

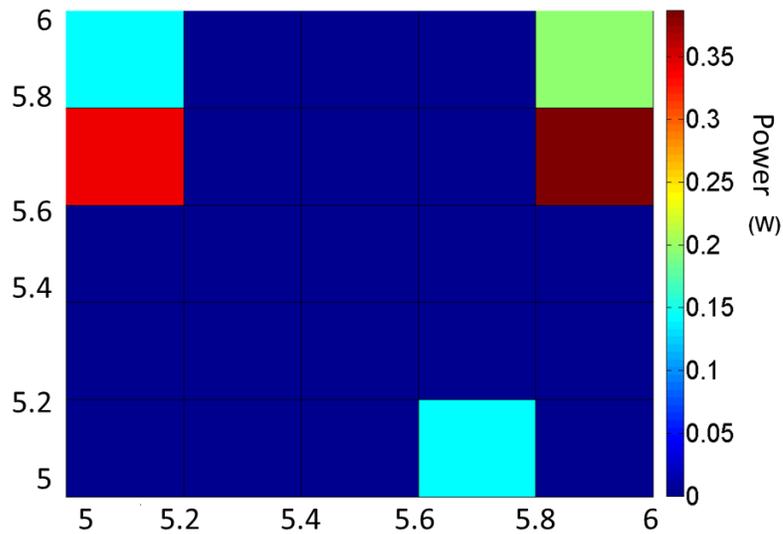


Figure 2.10: Power map used for die 2.

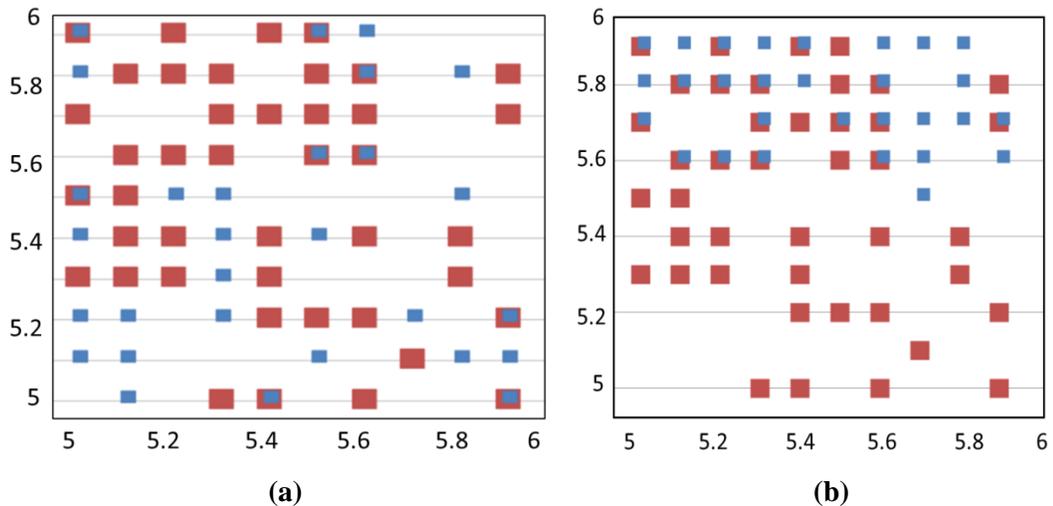


Figure 2.11: (a) TSV map-1, (b) TSV map-2. (Red dot: TSV from interposer to die 1, blue dot: TSV from die 1 to die 2) (dimension in mm).

We consider two scenarios for both thermal and DC voltage drop optimizations. Scenario I utilizes TSV map-1 while Scenario II uses TSV map-2. Both scenarios use same number of TSVs and the power map for die 2 (Figure 2.10). As shown in Figure 2.11, the difference between the two TSV maps is that TSV map-2 has more number of 1:1 corresponding TSVs from interposer to die 1 and die 1 to die 2, which means that there are more blue squares covering the red squares in Figure 2.11b than Figure 2.11a.

2.5 Simulation Results

The dimensions of the RDL is taken to be $1.1 \times 1.1 \text{ mm}^2$ as shown in Figure 2.4. Hence the total power consumption for both dies is fixed as 1.21 W, which is equivalent to power density of 100 W/cm^2 . Since we are considering the fact that the two dies are supplied by different vendors, hence one cannot alter the power distribution profile of the other die. Therefore in the optimization performed, the power map of the top die is kept constant while the power map of the bottom die is to be optimized.

2.5.1 Thermal Optimization

The lower die (die1) will be hotter in a two die case since it is far from the heat sink. Heat travelling from die 1 has to follow a higher resistance path in order to reach the heat sink, thus resulting in a considerably higher temperature than the upper die (die 2). It is important to note that the goal of optimization is to minimize the temperature of the hottest die, which is the bottom die in the stack. Thus, the goal (fitness function) for GA is to minimize the maximum die temperature within a feasible working temperature range. The power map of die 1 is same as die 2 before optimization.

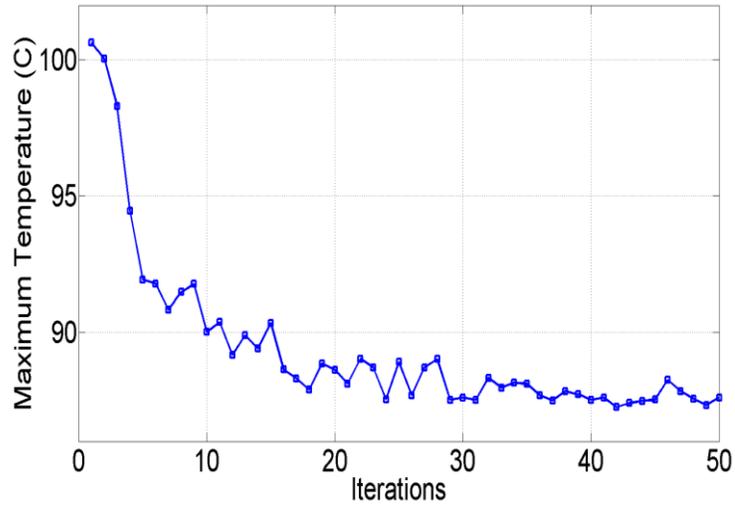


Figure 2.12: Maximum temperature of the bottom die with iterations.

Scenario I

Figure 2.12 shows the maximum die temperature with iterations. It shows the maximum temperature converges after 35 iterations. Figure 2.13 shows the initial power map and the power map of the bottom die after 50 iterations. Compared to the initial power map, the final power map has more evenly distributed power blocks. As temperature distribution can provide better insight regarding the optimization, Figure 2.14 shows the comparison between the initial and converged thermal profile after optimization.

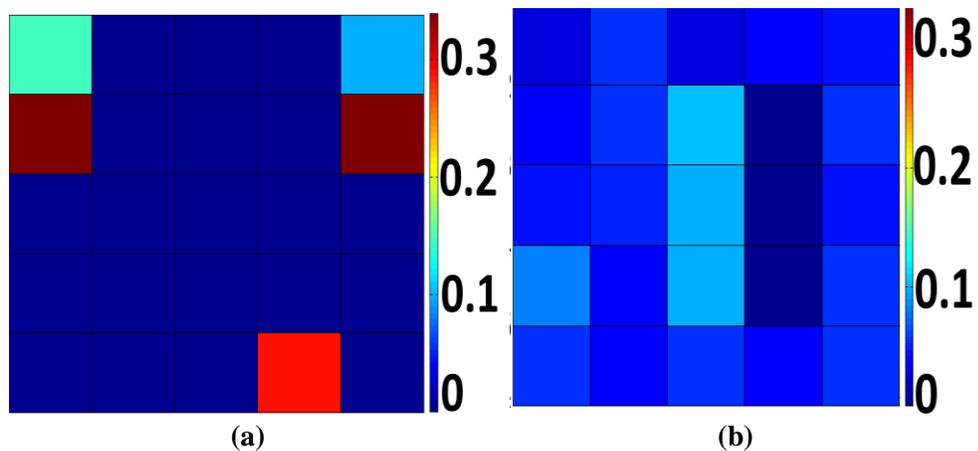


Figure 2.13: (a) Initial power map, (b) optimized power map after 50 iterations (Unit: W).

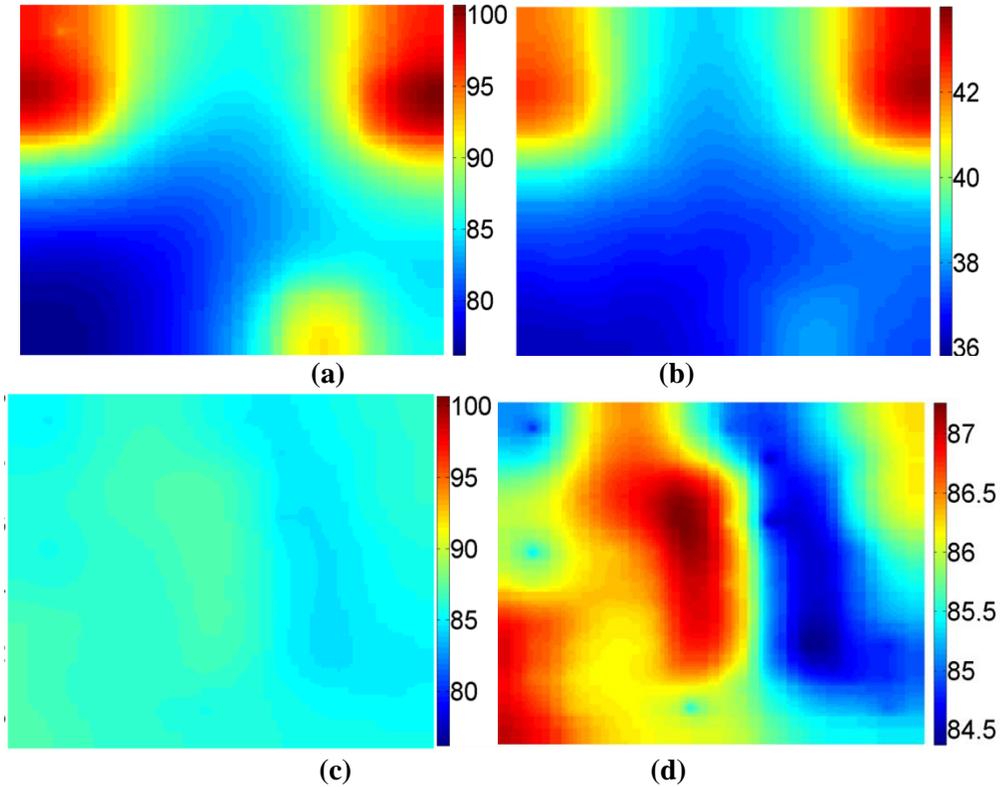


Figure 2.14: Temperature of (a) bottom die before optimization, (b) top die after optimization, (c) bottom die after optimization, (d) bottom die after optimization with normalized scale (Unit : °C).

Figure 2.15 shows the histogram of temperatures on the bottom die (die 1). As seen in Figure 2.14, the optimization results in a much lower peak temperature. The maximum temperature in the die has reduced from 100 °C to 88 °C, around 12% decrease in the maximum die temperature. In addition, the difference between minimum and maximum temperatures after optimization has reduced from 26 °C to 5 °C, which shows uniformity in temperature distribution.

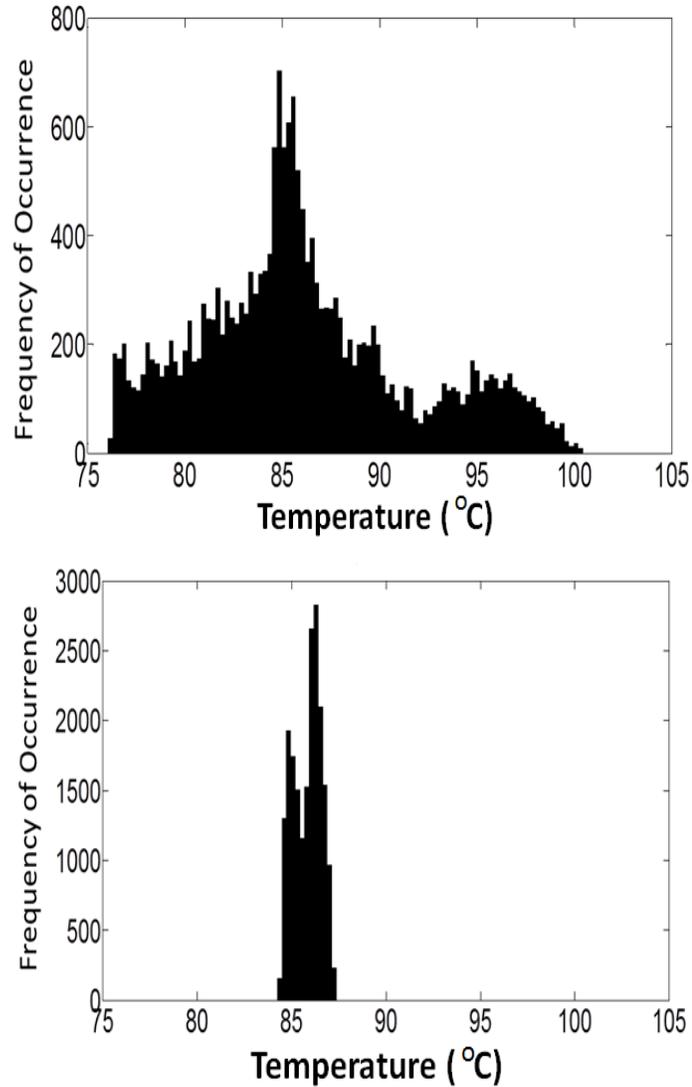


Figure 2.15. Temperature distribution histogram, (top) before optimization, (bottom) after optimization.

Scenario II

In this scenario, TSV map-2 (Figure 2.11b) is used. The optimized temperature maps of the bottom die for scenario II are shown in Figure 2.16. Figure 2.16a shows localized hot spots, the red regions at top corner of the die, which result in a maximum temperature of 98 °C before optimization. After optimization, Figure 16b shows there are no obvious hotspots on die 1 because of the absence of red regions in Figure 2.16b. Figure 2.16c

illustrates the renormalized temperature profile of die 1 with a different scale. Because of the many overlapping TSVs (Figure 2.11b), the cold spots, (the deep blue regions), appear. Figure 2.17 shows frequency of occurrence of different temperature in die1. Similar to Scenario I, the temperature gradient has reduced from 24 °C to 4 °C, indicating of importance of optimization.

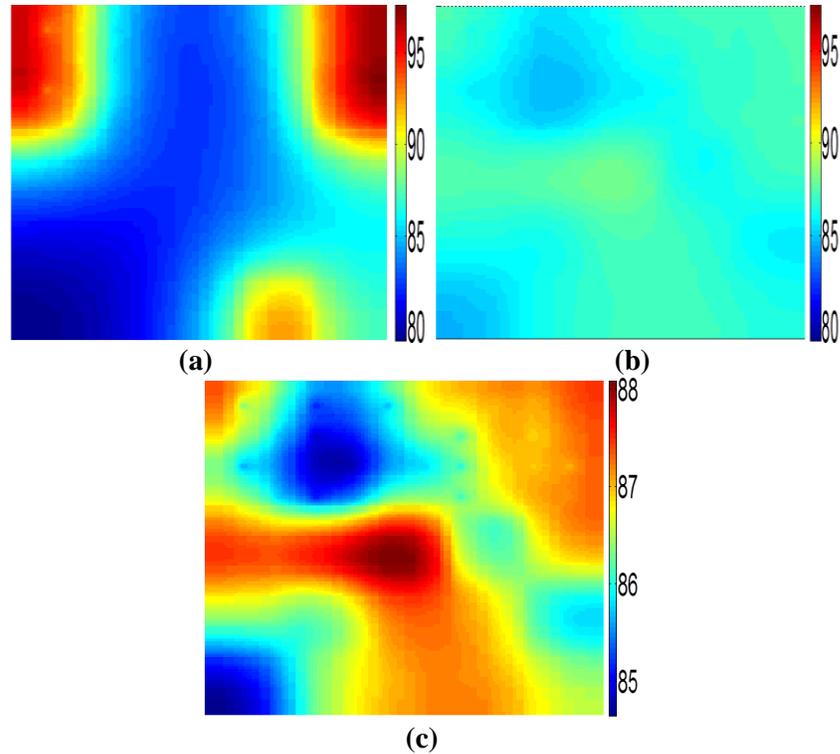


Figure 2.16: Temperature of (a) bottom die before optimization, (b) bottom die after optimization, (c) bottom die after optimization with normalized scale (Unit : °C).

The comparison of temperatures in Figure 2.14b and Figure 2.14d shows that the hotspots (high temperature areas) on the top and the bottom dies are misaligned after the optimization, which results in the reduction in maximum die temperature. Similar results are observed in Figure 2.16b and Figure 2.16c for Scenario II. With a constant TSV map, the best response to a particular power map of one die is to place the hotspots, which is produced by high power density block in the die, such that the hotspots are not vertically aligned.

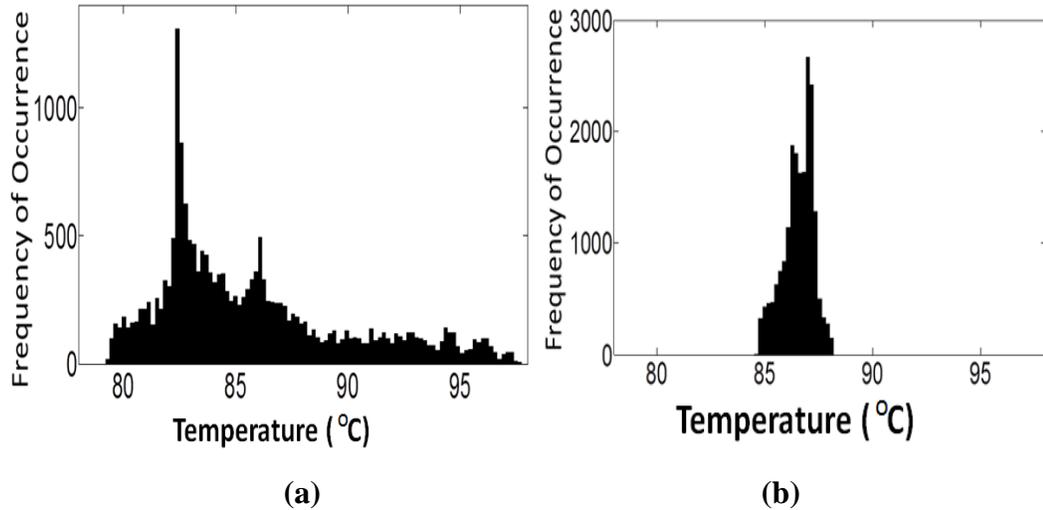


Figure 2.17: Frequency of occurrence on die 1, (a) before optimization, (b) after optimization.

2.5.2 DC IR drop optimization

The power map of the bottom die before optimization comprises of a randomly chosen power map with total power of 1.21 W. The goal of optimization is to minimize the voltage drop on die 1 (bottom die).

Scenario I

Figure 2.18 shows the power maps of the bottom die before and after optimization for Scenario I. The optimized power map depends on the TSVs going from interposer to die 1, as these TSVs carry the current from PCB to die 1.

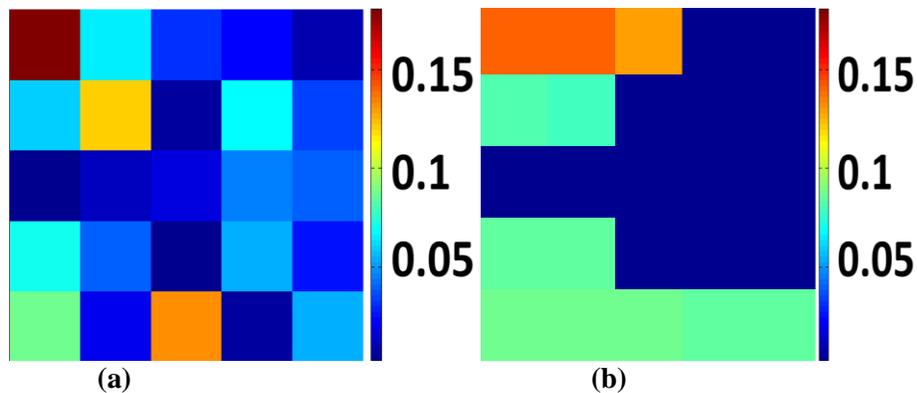


Figure 2.18: Bottom die power map, (a) before optimization, (b) after optimization. (unit: W)

Figure 2.19 shows the voltage drop at the bottom die versus the number of iterations. It shows that the voltage drop converges after 61 iterations. The maximum voltage drop reduces from 45 mV to 39 mV, about 13% reduction.

Figure 2.20 shows the voltage profile on the RDL of die 1. Compared to the initial voltage profile, the optimized voltage profile has fewer number of nodes with large voltage drop, which is indicated by the blue spots in Figure 2.19.

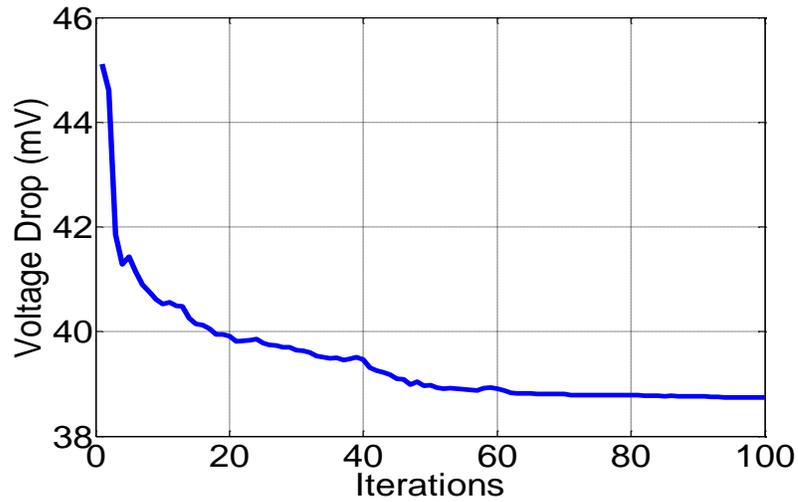


Figure 2.19: Minimum voltage on the bottom die vs iterations.

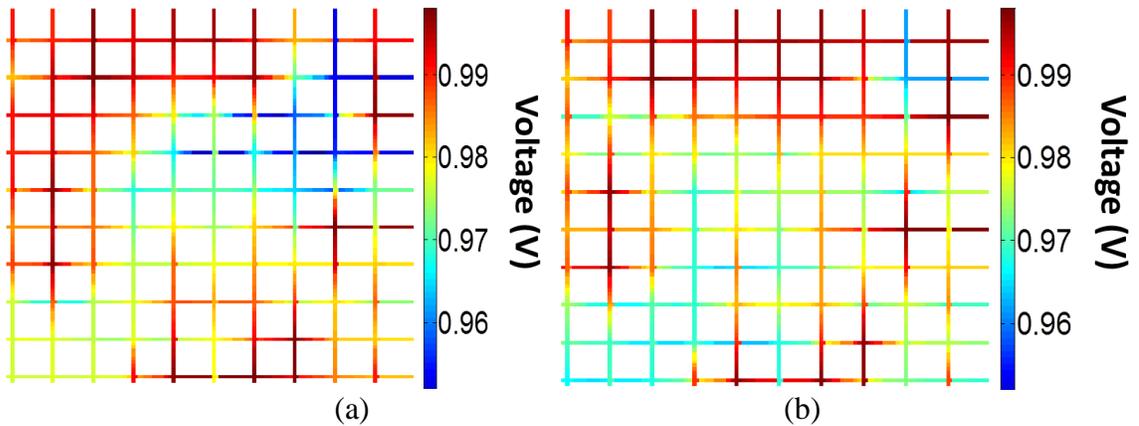


Figure 2.20: Voltage drop (a) before and (b) after optimization.

The area marked by the dash frame in Figure 2.21 denotes the voltage for bottom die. As we can see from Figure 2.20, the voltage drop gradient is also improved by at least 20%.

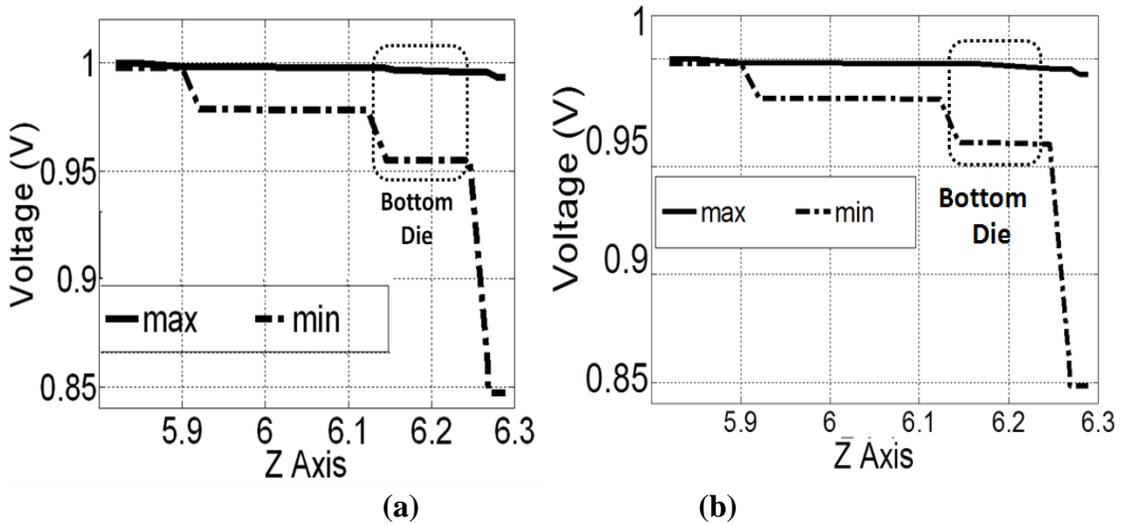


Figure 2.21: Voltage across z axis (a) before and (b) after optimization.

Scenario II

For scenario II, Figure 2.22 shows the voltage drop at the bottom die versus iterations. It shows that the voltage drop converges after 41 iterations. The maximum voltage drop reduces from 50 mV to 29 mV, about 42% reduction.

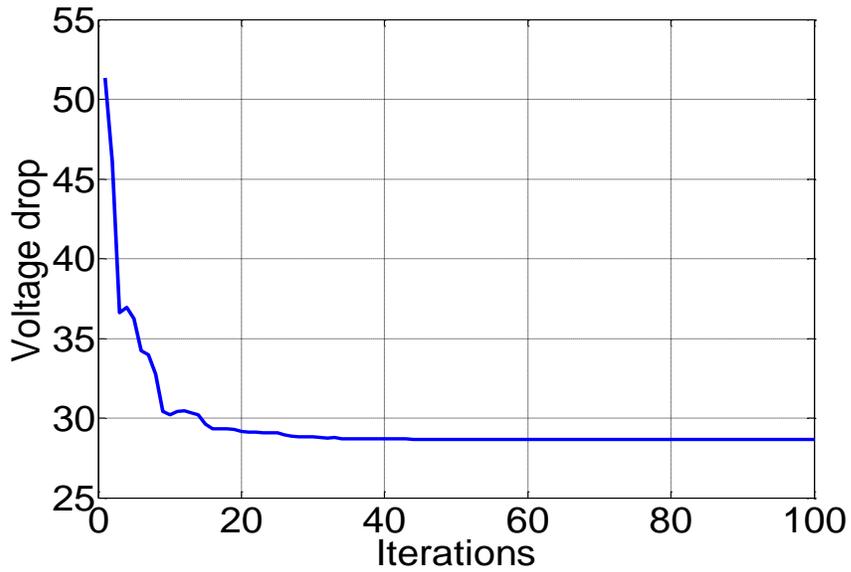


Figure 2.22: Minimum voltage on the bottom die with iterations.

Figure 2.23 shows the power maps of the bottom die before and after optimization for scenario II. As seen in Figure 2.23, since the TSV map has more overlapping TSVs (Figure 2.11b), most of the power in the bottom die is concentrated in the top region irrespective of the power map of the top die.

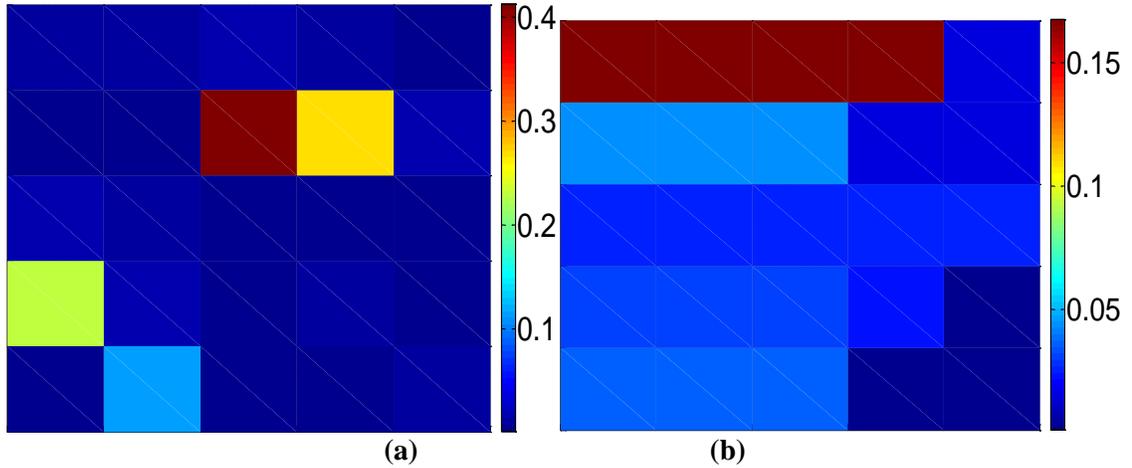


Figure 2.23: Bottom die power map (a) before optimization (b) after optimization. (unit: W)

Figure 2.24 shows the voltage profile on the RDL of die 1. Compared to the voltage profile before optimization, the optimized voltage profile has less blue region with large voltage drop. As can be seen from Figure 2.25, the voltage drop gradient has been improved.

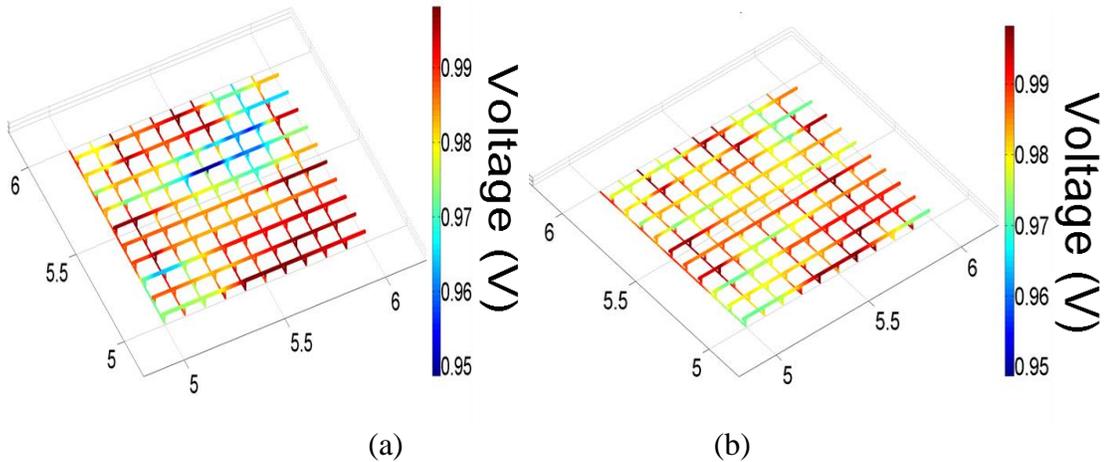


Figure 2.24: Voltage profile (a) before and (b) after optimization.

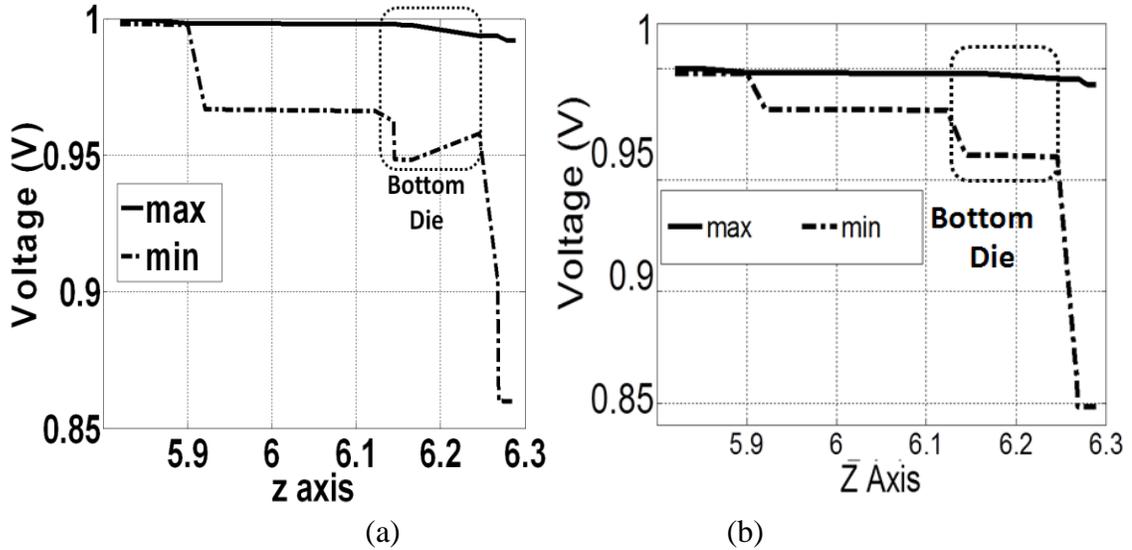


Figure 2.25: Voltage gradient along z axis (a) before and (b) after optimization.

2.5.3 Importance of co-optimization

In Section 2.5.1 and 2.5.2, the optimization is performed for thermal and voltage drop without considering their interaction. To cross-validate the optimized results, we perform another set of simulations. In the simulation, the optimized power map for thermal optimization is used as the input to simulate the voltage drop and vice versa. Figure 2.26 shows the results for all scenarios when they were simulated with optimized power maps for both IR drop and thermal analysis.

The horizontal axis shows the maximum temperature on die 1, and the y axis shows the maximum voltage drop on die 1. Figure 2.26 shows that optimized power map for thermal analysis can result in larger IR drop than the optimized voltage drop. It also shows that optimized power map for IR drop analysis can result in larger temperature, indicating the importance of co-optimization.

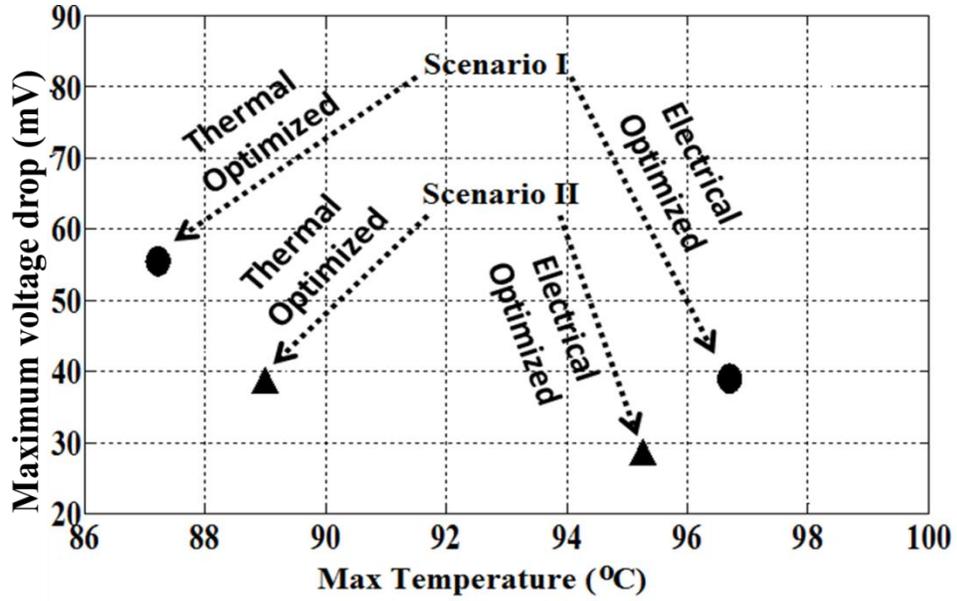


Figure 2.26: Cross-validation results.

2.6 Matrix Synthesis Process (MSP)

Matrix Synthesis Process (MSP) is to synthesize a matrix out of a given list of numbers such that no submatrix of a particular size has a large sum. MSP can be used to model the thermal placement problem of minimizing the temperature and thermal gradient on a die [31]. The amount of heat generated by the die area can be represented by a nonnegative real number. A submatrix $S_s(M)$ in corresponds to a region of size $s \times s$ on the chip. The submatrix with the largest sum corresponds to the hottest region on the chip. So MSP is equivalent to finding a placement of the power consuming blocks such that the temperature of the hottest region is the lowest among all possible placements [31].

From now on, we assume for simplicity that for a matrix of size $n \times m$, $n=m=sr$ for some integer r . In other words, we are placing $s^2 r^2$ numbers into a $sr \times sr$ matrix. We assume $n=m$ and let $x_1 > x_2 > x_3 \dots > x_{n \times n}$, where x_i are entries in the matrix which represent power densities.

The basic idea of the algorithm is to distribute the numbers evenly in the matrix. We divide the numbers into $s \times s$ groups according to their magnitudes. We observe that it is possible to have a placement with the property that every $s \times s$ submatrix contains exactly one number from each group. Figure 2.27 shows how we group elements.

G_1	G_2	G_1	G_2
G_3	G_4	G_3	G_4
G_1	G_2	G_1	G_2
G_3	G_4	G_3	G_4

Figure 2.27: Group formation for MSP.

For example, let $t=2$, $m=n=4$, $x_i = i$ for $1 \leq i \leq 16$. In other words, we want to place numbers 16, 15... 1 into 4×4 matrix. Then G_0 contains 1-4, G_1 contains 5-8, G_3 contains 9-12 and G_4 contains 13-16. Figure 2.28 shows one of the possible implementations of MSP

1	7	3	6
10	14	9	13
4	8	2	5
11	15	12	16

Figure 2.28: One of the possible implementations.

The MSP approach for 3D ICs is as follows.

- Randomly assign power densities to dies at all levels, keeping the total power density constant in the stack.
- Apply MSP on individual dies. Store maximum sum submatrices $max(S_s(M))$ and their location.
- Places the submatrices such that one with largest sum is closest to heat sink. Two cases will arise. If the larger sum submatrix replaces the lower sum submatrix. A lower sum submatrix replaces the larger sum submatrix. In the latter case MSP has to be applied again locally on the corresponding die.
- Sort the dies based on total power consumption. Matrix with the largest sum $max(S(M))$ is placed closer to the heat sink.
- Check whether $max(S_s(M))$ and matrix sum $(S(M))$ are in sorted order.
- If yes then terminate algorithm, else go to Step 2.
- The elements are grouped according to $s \times s$ submatrix.

Tables 2.4-2.9 show the results for various input parameters for the algorithm. The improvement tabulated is based on the maximum sum submatrix $max(S_s(M))$ before and after applying MSP.

Table 2.4: Summary of different die layers for a 10 X 10 matrix.

Layer number	before	after	Impr. (%)	before	after	Impr. (%)	before	after	Impr. (%)	before	after	Impr. (%)
1	1143611	929100	18.75734	1496670	1071100	28.43446	1079791	865700	19.82708	1156869	869400	24.84888
2	1101728	960670	12.80334	1243535	1081700	13.01411	1426499	867700	39.17276	1291792	875900	32.19497
3				1238081	1092400	11.76668	1190415	867800	27.10105	1503410	888200	40.92097
4							1087442	1025500	5.69612	1368421	894600	34.62538
5										1390792	1015100	27.01281
6										1192642	1017300	14.70198

Table 2.5: Improvement data for different matrix sizes for a 2 X 2 submatrix.

size	6			8			10			16		
layer	Initial	After	Impr.(%)									
1	3289611	2341583	28.81885	1773692	2004883	-13.0345	1079791	865700	19.82708	492732	448889.8	8.897774
2	3068521	2068488	32.59006	2481280	1416088	42.92914	1426499	867700	39.17276	756948	429898	43.20641
3	3434566	2002039	41.7091	1960083	1406444	28.24568	1190415	867800	27.10105	540928	426984.7	21.06441
4	3296667	1955890	40.67069	1670806	1265224	24.27466	1087442	1025500	5.69612	520935	425822.6	18.25803
size	20			24			30			50		
layer	Initial	After	Impr.(%)									
1	402727	374055.9	7.119245	306305	284694.5	7.055213	179830	144876.5	19.43694	76029	65249.01	14.17879
2	376586	267665.8	28.92306	233595	209355.5	10.37671	171607	138397.8	19.35191	77779	51459.46	33.83888
3	342506	267051.1	22.03023	312435	209345.3	32.99558	189715	114490.8	39.65118	75363	51431.96	31.75437
4	364044	264589.4	27.3194	315484	201379.7	36.16802	236068	113913.1	51.74565	73227	49503.64	32.39701

Table 2.6: Improvement data for different sub matrix sizes for a 10 X 10 matrix.

<i>3 X 3 submatrix</i>												
size	6			12			15			30		
layer	Initial	After	Impr.(%)									
1	2580359	1701793	34.04822	899203	497299.4	44.69553	478172	340554.1	28.78	139354	85114.88	38.92183
2	2525728	1690050	33.08663	798622	495788.7	37.91948	491355	337653.6	31.28114	119807	82380.52	31.23897
3	2120105	1686864	20.43489	652688	492331.2	24.56868	481576	331673.9	31.1274	142228	81981.4	42.35917
4	2228214	1610719	27.71256	589051	487298.8	17.27393	429273	329591.4	23.22102	136291	79350.67	41.77849
<i>4 X 4 submatrix</i>												
size	12			20			32					
layer	Initial	After	Impr.(%)	Initial	After	Impr.(%)	Initial	After	Impr.(%)			
1	574643	462013.7	19.59987	239570	167357.4	30.14257	97702	71592.9	26.72319			
2	650340	461712.3	29.00447	292921	158860.2	45.76689	97572	71592.9	26.62556			
3	690167	444064.4	35.65842	247931	156592.6	36.84025	85487	65582.53	23.28362			
4	666003	435103.9	34.66937	267009	156419.2	41.41801	105291	65420.44	37.86701			

2.6.1 Structure and results for MSP

Since this algorithm does not require running the thermal analysis tool in every iteration, hence one can use larger number of dies in a stack. Therefore a 4 die structure is used as shown in Figure 2.29. No TSVs are initially placed in the structure. The internal setup of each die is similar to Figure 2.2 except for the RDL.

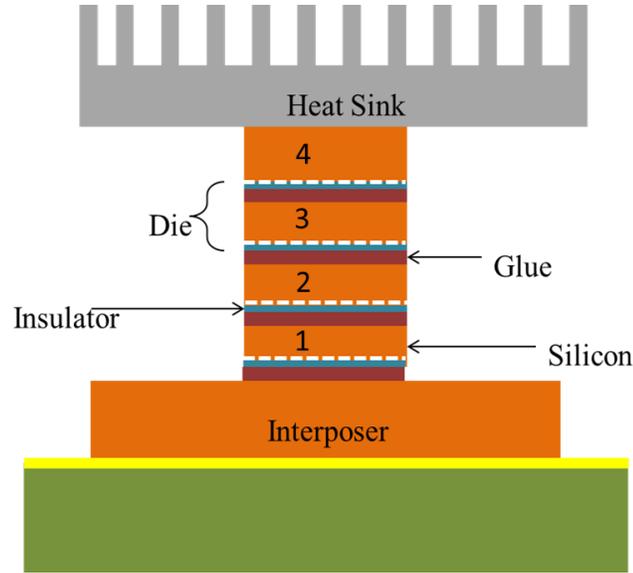


Figure 2.29: 4 die setup for MSP.

The RDL used in previous case (Figure 2.4), can result in a large number of unknowns even for a 2 die simulation. Therefore to simulate the effects of metal in insulator the concept of effective metallization is used.

The effective metallization of RDL layer is calculated as

$$\kappa_{eff} = \kappa_{TSV}m_{TSV} + \kappa_{oxide}m_{oxide} \quad (2.2)$$

where κ is the thermal conductivity, m is the percentage of material.

In order to pick the correct m , the percentage of metal is varied in the insulator in all the dies and maximum temperature is recorded. For this simulation the setup used is shown in Figure 2.29. where 100 TSVs per die were placed in the structure. The RDL

used previously has 100 intersections between the power traces which correspond to potential TSV positions in the die, hence a maximum of 100 TSVs can be placed in a die.

Figure 2.30 shows temperature versus metallization density.

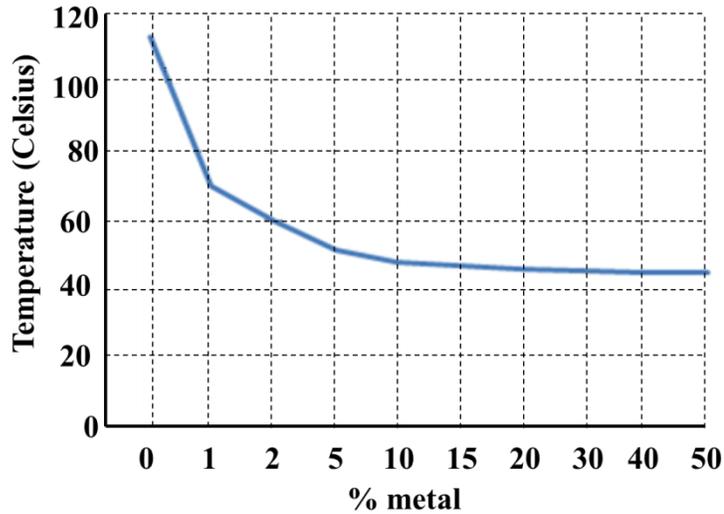


Figure 2.30: Temperature vs. metallization density.

We see that the temperature saturates around 10/12% of metal. Hence we use 15% metallization density. We use a total power density $2e10^8 W/m^2$ with an average of $0.5 W/m^2$ per die. The power density map for each die is meshed as $10 X 10$ matrices. The submatrix size used is $2 X 2$. Figure 2.31 shows the temperature profiles before and after applying MSP.

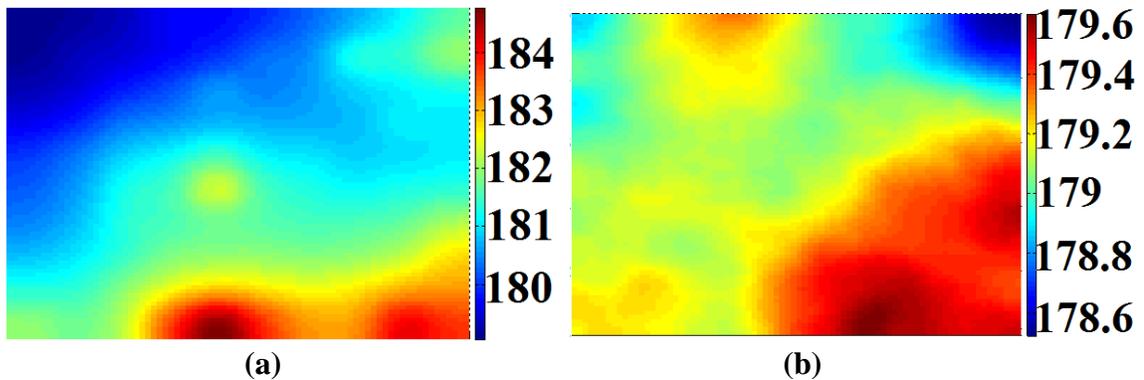


Figure 2.31: Temperature on bottom die (a) before applying MSP, (b) after applying MSP (Unit: °C).

Again die 1 which is the bottommost die will have the maximum temperature because it is the farthest from the heat sink. Figure 2.32 shows frequency of occurrence of temperatures on the bottommost die.

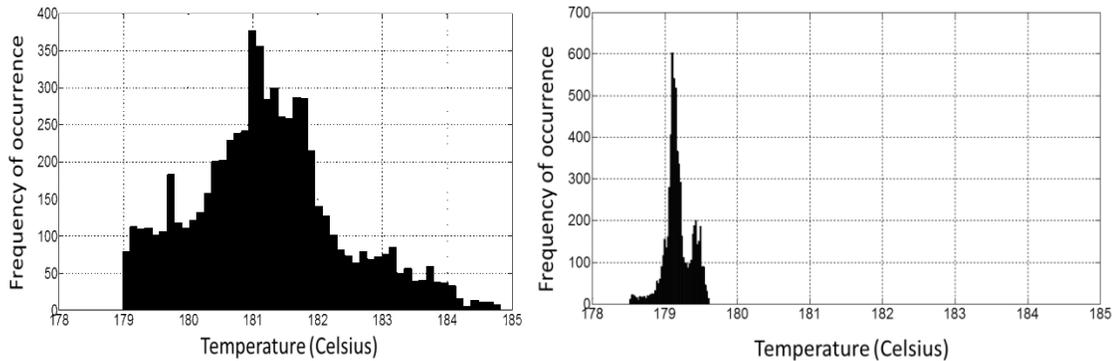


Figure 2.32: Frequency of occurrence on bottom die, (a) before MSP, (b) after MSP.

From Figure 2.32 it is clear that the MSP approach not only reduces peak temperature but also reduces the thermal gradient across a die. As shown in tables 24-2.6 this method can be used for a large number of layers and big matrix sizes. The code has been developed in MATLAB® and it does not require the solver after each run. Hence the method is fast, but does not capture the actual thermal effects after each iteration. Since the algorithm only manipulates the numbers representing power densities and does not call the solver until the code has terminated, it cannot capture the effects on intradie routing metal or the inter die connections using TSVs

2.7 Effects of TSVs on thermal profile

TSVs are filled with metal form high heat conducting paths from bottom die to the top die. But, they do not affect heat convection system. Hence the effects of TSVs cannot be neglected. On the other hand TSVs consume a lot of real estate, can cause stresses in a stack and are difficult to fabricate. Therefore, to maintain thermal integrity with use of

minimum number of TSVs is a key factor in cost reduction and proper functioning of dies. To study the effect of TSVs a uniform array of TSVs is added to Figure 2.2. The array size is gradually increased till all possible TSV positions are occupied in the interposer and die 1. Table 2.7 shows the maximum, minimum and gradient of the temperature for different array sizes. Figure 2.33 shows the variation of the temperature with different array sizes.

Table 2.7: Temperature variation with number of TSVs (Unit: °C)

TSV array	Maximum	Minimum	Gradient
0	112.62	36.85	75.77
4	106.88	36.87	70.01
9	101.3	36.92	64.38
16	96.152	36.92	59.232
25	90.84	36.89	53.95
36	86.59	36.85	49.74
49	82.8	36.67	46.13
64	78.74	36.63	42.11
81	73.56	36.86	36.7
100	70.63	37.06	33.57

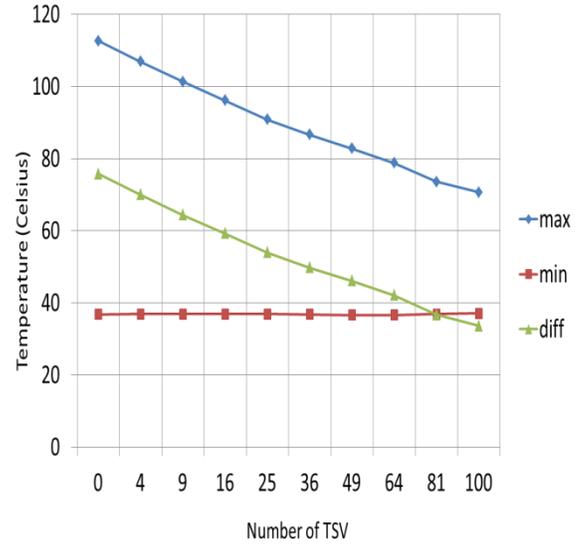


Figure 2.33: Variation of temperature with number of TSVs

A critical observation made from our experiments is that inserting TSVs reduce the maximum temperature in the 3D IC stack. However it does not reduce the minimum temperature and that may even increase slightly. In other words the role of TSV is “soothing or averaging” the maximum temperature of 3DIC than shifting down the working temperature level as a whole.

2.8 Residual TSV removal Algorithm

This algorithm aims at removing the unwanted TSVs. The structure used is same as Figure 2.3 for electrical simulations and Figure 2.29 for thermal simulations. The simulation starts with TSVs in all possible locations in the stack. Then TSVs are removed

iteratively based on a specific condition until a threshold voltage is reached. Figure 2.34 shows the flowchart and for electrical simulations for TSV removal.

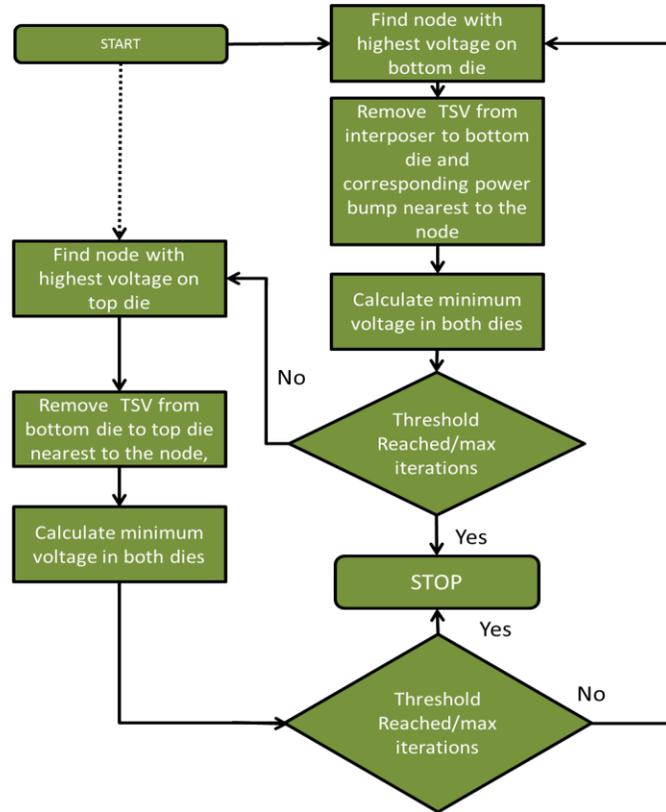


Figure 2.34: Flowchart for TSV removal algorithm in electrical simulation.

A node with a TSV connected to it will have a very low voltage drop associated with it. The algorithm targets such nodes where the voltage is much higher than the required threshold. It removes TSVs from such nodes thereby reducing the voltage or increasing the voltage drop at that particular node. This process is repeated till the particular voltage threshold is reached. The algorithm starts with 300 TSVs. 100 each from power plane to interposer, interposer to die 1 and die 1 to die 2. The threshold level for minimum voltage on the 3D stack is arbitrary set to 900mV. This threshold is flexible and can be set as per requirement of the die manufacturer. This algorithm can also be customized to set a threshold for a particular die instead of a complete stack. Moreover there is no restriction

on number of dies that can be used. The dotted line in the flowchart denotes the fact that the first iteration of the algorithm for finding the highest voltage drop node can be started with either die without much change in the final result. Figure 2.35 shows number of TSVs versus the minimum voltage.

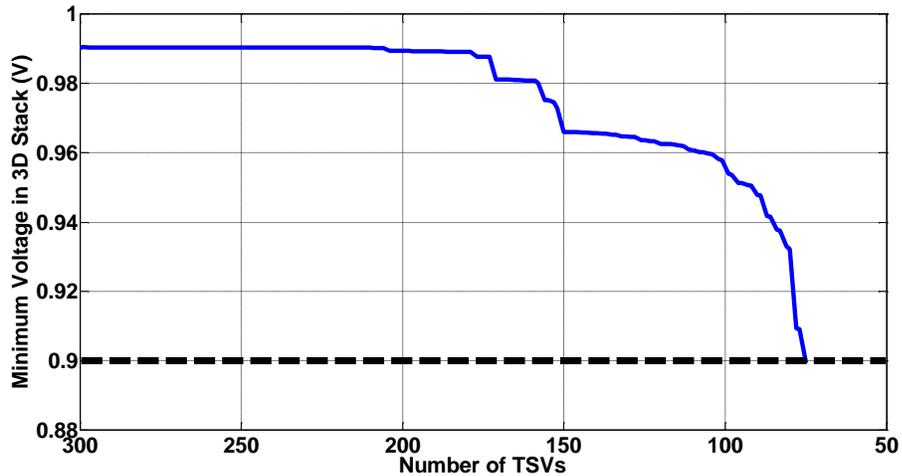


Figure 2.35: Number of TSVs vs minimum voltage on the stack.

We observe that all the TSVs positions are not required to maintain a particular voltage drop. As we can see from the above graph, from 175 to 300 TSVs the voltage is nearly constant. The voltage begins to fall rapidly after a specific number of TSVs which is 100 in the above case. Figure 2.36 shows the RDL map of die 2 after placing the TSVs

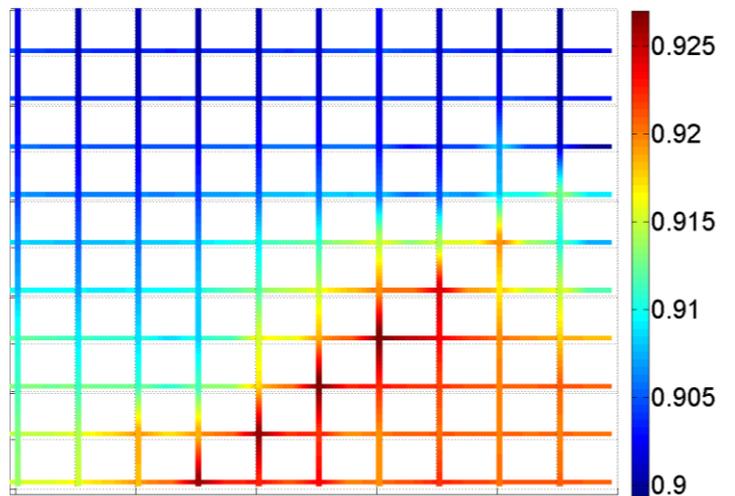


Figure 2.36: Voltage plot of RDL on die 2 after TSVs are placed (Unit: Volt).

Similar logic is used for thermal simulations as well. TSVs provide high heat conducting paths; they remove heat away from the active regions in a die. For each particular die level the coldest node is found. The TSV nearest to the coldest node and all TSVs corresponding to that node in dies above that particular die are removed. TSVs are iteratively removed by considering the coldest region in each die until a given temperature threshold is reached. Figure 2.37 shows the general steps in algorithm for thermal simulations.

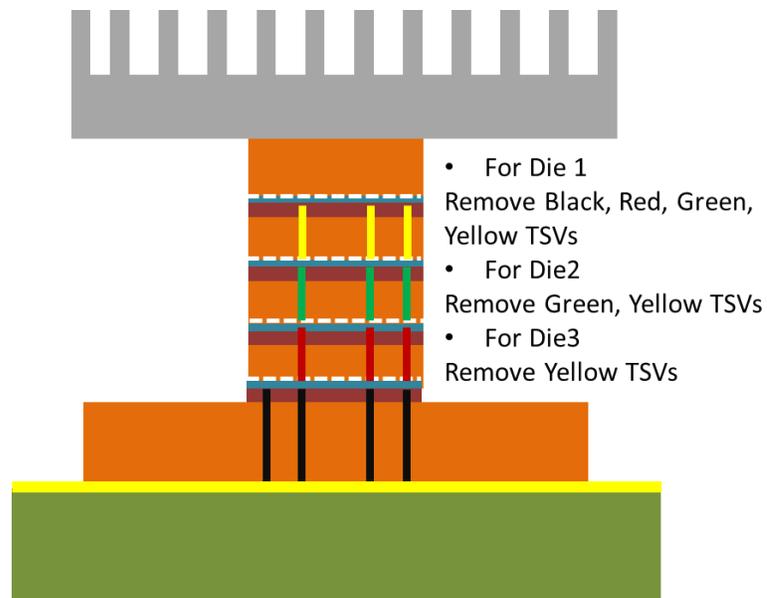


Figure 2.37: Steps for TSV removal algorithm in thermal simulation.

Since there are 100 possible TSV positions per die, so the simulation starts with 400 initial TSVs which are then iteratively removed till the temperature reaches a specified threshold. The threshold temperature chosen is 90°C. The algorithm is applied on the MSP optimized structure given in Figure 2.31(b).

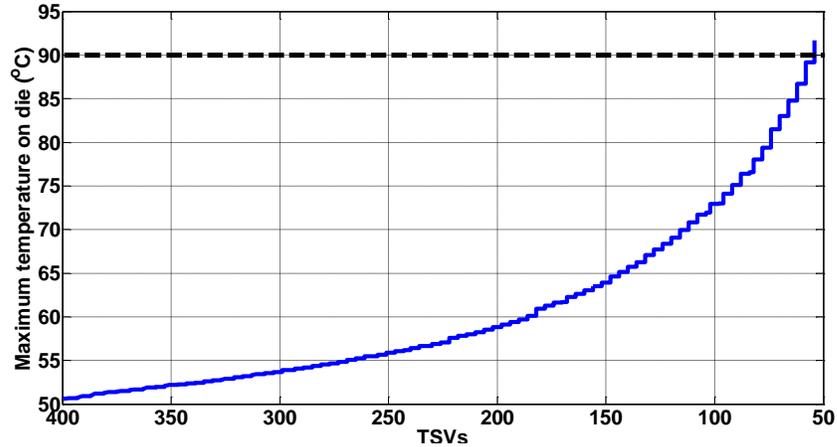
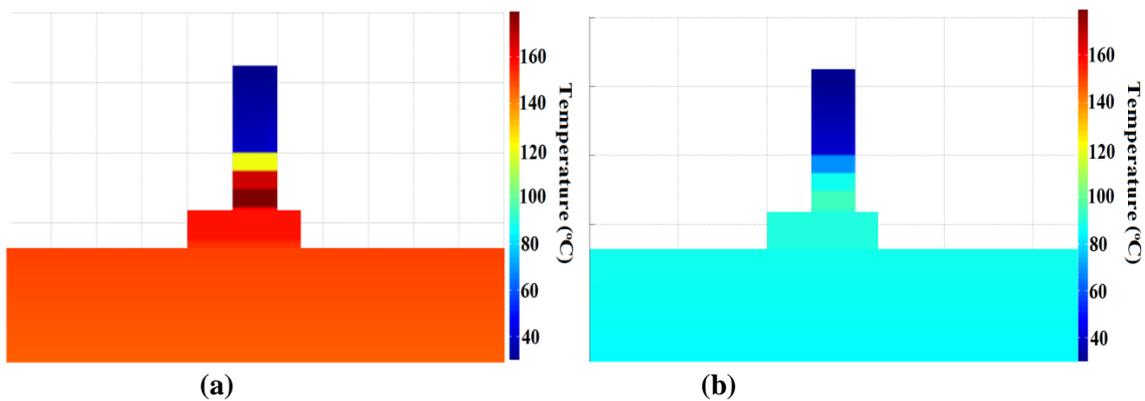
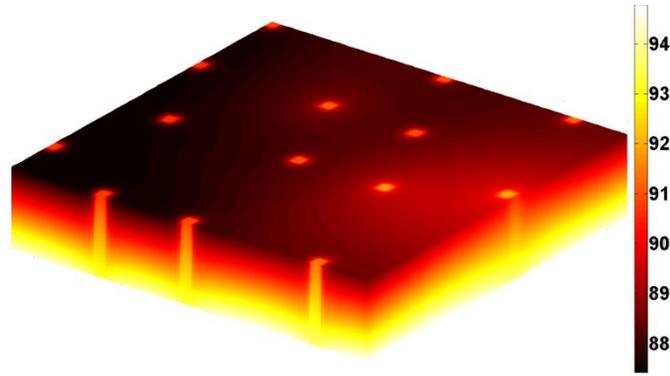


Figure 2.38: Number of TSVs vs maximum temperature on the stack.

Figure 2.38 shows the maximum die temperature versus number of TSVs. Figure 2.39 shows the 3D structure of the complete stack before and after TSVs have been placed. We can see that as discussed in section 2.7 the maximum temperature of the 3DIC has decreased, but the minimum temperature is the same. From Figure 2.38 we observe an exponential increase in temperature as number of TSVs start to reduce. Figure 2.39(c) shows the cross-section of the bottom die after TSV insertion. The deep red/black areas are the low thermal conductivity (κ) glue layer between bottom die and the die above it. These low κ layers provide the most hindrance in the efficient conductivity of heat. As can be seen from Figure 2.39c, TSVs provide a good heat conducting path through these low κ layers in the 3D stack.





(c)

Figure 2.39: Thermal profile of the 4 die stack (a) after MSP, (b) after MSP and TSV placement, (c) cross section of the bottom die and glue layer above it.

2.9 Summary

In this chapter, a genetic algorithm based approach for DC IR drop and thermal optimization of a 3D stack is presented. We utilize GA optimization engine for minimizing temperature and voltage drop with fixed die power and TSV maps. The simulation results show that 20% improvement in temperature and voltage drop can be obtained. The optimization method can help different IC vendors optimize for thermal and voltage integrity of a 3D stack. The simulation results also indicate the importance of voltage drop and thermal co-optimization. A method based on matrix synthesis process is introduced. It is modified for a four die thermal optimization, which can be extended to more dies as well. Both approaches above not only reduce the maximum temperature of the stack but also help in spreading heat by considerably reducing the thermal gradient. A TSV removal algorithm is introduced to minimize the number of TSVs that can be used to achieve a given voltage drop or temperature. The simulation results prove that not all TSV positions need to be occupied for best results. Hence reducing number of TSVs plays an important role in minimizing costs, while maintaining electrical and thermal integrity.

CHAPTER 3

DESIGN EXCHANGE FORMATS

3.1 Introduction

The emerging TSV technology enables Three Dimensional (3D) stacking of Integrated Circuits (ICs), which help to continue miniaturizing integrated systems and increasing their functionality. Due to the continuing growth of integration density, the power density of IC chips is expected to increase beyond 100 W/cm^2 in 2016 according to the International Technology Roadmap for Semiconductors (ITRS) [28]. In order to reduce the power consumption and increase functionality, the power supply voltage of IC chips has been reduced to 1.2 V and below with the scaling of IC fabrication technology [29]. In particular, due to stacking of ICs together in the vertical direction, the power density of 3D integrated systems is expected to become much larger than for the corresponding 2D system implementation.

To aid in a smooth paradigm change from 2D design to next-generation designs for 3D ICs, it is necessary to develop standards for 3D IC design. The design of a 3D stack assumes that there are DRAMs, logic (chips), interposer, package and PCB which make up a whole system. In today's industry scenario each component of the system is being designed by a different vendor. With different companies battling over patents and copyrights it is unlikely that the DRAM and logic vendor will be willing to share circuit level IP, detailed layout information, and the details of the material stack up in their chip. Thus the main purpose of a Design Exchange Format (DEF) is to permit sharing of information necessary for design by external parties without disclosing this IP.

This chapter presents an initial effort towards prototyping an design exchange format for power delivery networks (PDNs) in 3D ICs. Steady state (DC) and thermal analysis is performed on a 3D stack to understand the parameters that may affect the exchange of different design parameters from one die to the other. The primary question that we try to address here is that- *“given a set of stacked dies, what is the complete list of items of design information that any one die must know about the others, to ensure compatibility with each other?”*

3.2 Simulation Setup

The main motivation behind this chapter is abstraction of the sensitive IPs of various chips. In order to facilitate this, two basic simulation problems are setup where the focus is on IR drop and heat dissipation. These two parameters are chosen here due to their interdependencies through joule heating. First a simulation is run with a full 3D stack and electrical and thermal properties are observed separately. In the second set of simulations a single die is simulated, where the simulations are run with some *‘information’* from the top die. With given inputs from the top die the same set of electrical and thermal parameters are observed as in the first set of simulations as shown in Figure 3.1. With results from two separate scenarios, the error or deviation is calculated. Since the vendor of die 2 needs to protect the IP from die1, they can pass a specific set of parameters for die 1, as illustrated in Figure 3.1(b). These parameters can be the total power consumption of die 2, the TSV distribution for TSVs going from die 1 to die 2 or the power map of die 2 in addition to total power consumption.

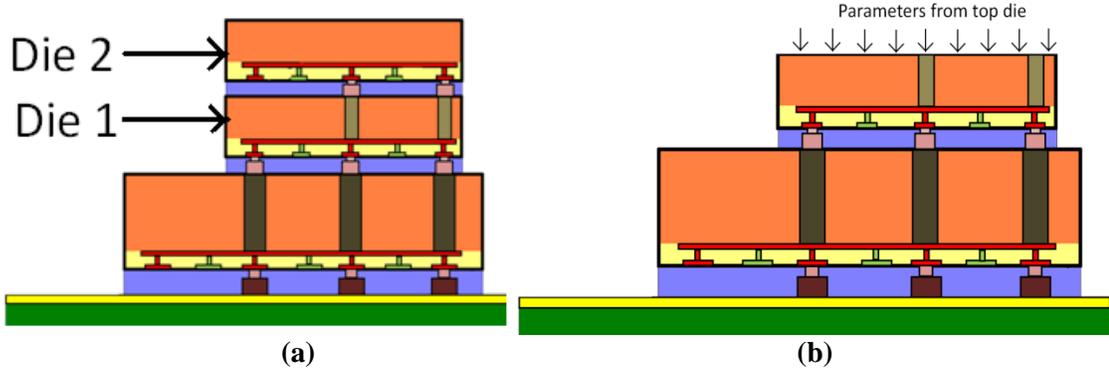


Figure 3.1: Two sets of simulations used for calculating the error, (a) Full 3D 2 die simulation, (b) Single die simulation with some information passed from the top die.

The error between the parameters is computed as

$$error = \frac{P(two\ dies) - P(single\ die)}{P(two\ dies)} \quad (2)$$

where P denotes parameters for a particular kind of simulation. For electrical simulation P is the voltage on die 1, while for thermal simulations it is the temperature on die 1.

3.3 Simulation Parameters for electrical and thermal analysis

A Finite Volume Method based solver was used for the simulation [22-24]. The simulation considered is for a two die stack connected to a PCB board through an interposer as shown in Figure 3.2.

Two basic types of steady state simulations are used for comparison namely IR drop and thermal simulation. Since the simulations are steady state, the transient effects are not taken into account in any of the simulations. Electrical simulation setup only considers the IR drop from the voltage source to the end of TSVs. Effects of substrate, adhesives, PCB on the steady state voltage drop are neglected because they do not affect the steady

state end result for IR drop. This is equivalent to calculating the IR drop for just the voltage supply. However, these effects are taken into account in the thermal simulations. Electrical resistivities of materials other than conductors are very high, so that they can be neglected for IR drop calculations. However this is not true for their thermal resistivities. Hence ignoring them in thermal simulations can lead to large errors.

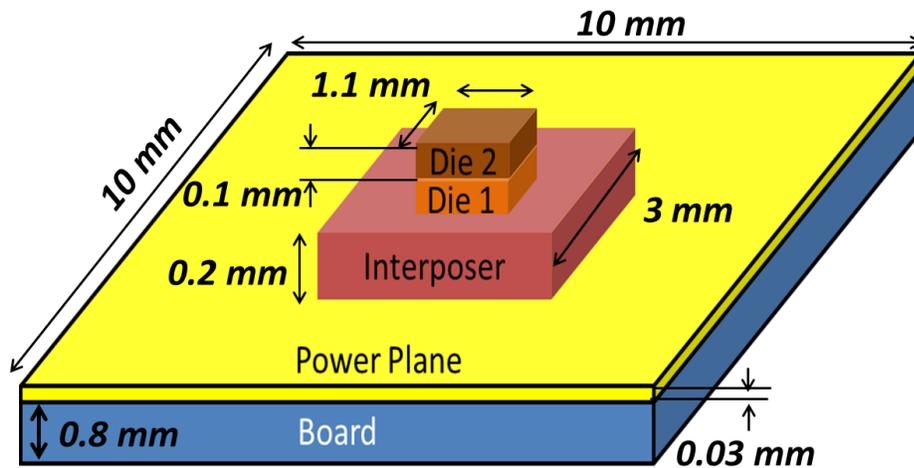


Figure 3.2: Structural overview for simulation setup.

3.3.1 Steady State (DC) Electrical Analysis

Figure 3.3 shows the details of structure used for electrical simulation.

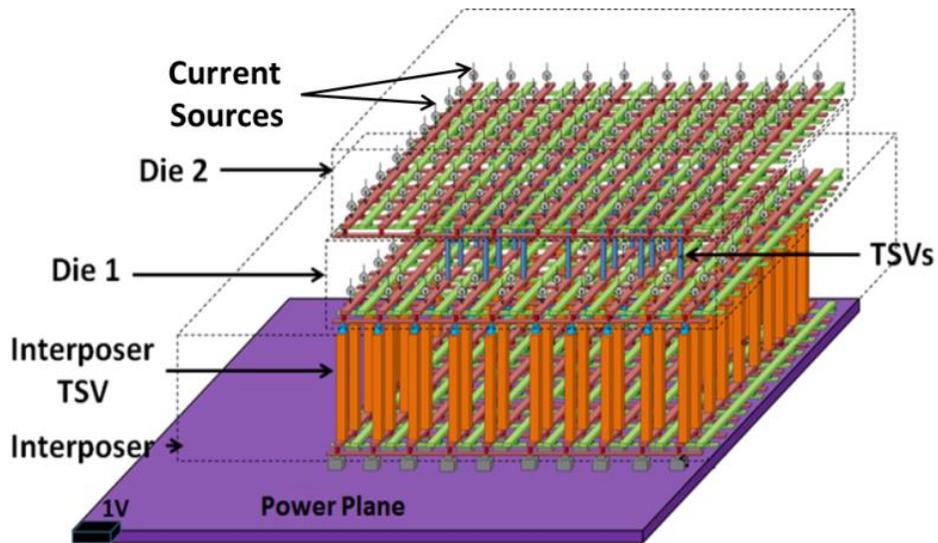


Figure 3.3: Structure used in electrical simulation.

Each part of the 3D stack contains one set of Redistribution Layers (RDL) and TSVs. The dies are connected in face- to- back configuration [6]. Hence no TSVs are required in die 2. The interposer is connected to the power plane through bumps in form of a uniform array. The two dies are connected to each other using micro bumps. A voltage source is used at the bottom corner as shown in Figure 3.3. Current sources are used to simulate the active devices. For a given amount of power and input voltage the required current values can be calculated. For the simulations a 1 V voltage source was used in the bottom left corner of the power plane.

Figure 3.4 shows the layout of the RDL layers in each die and the interposer. It comprises of two layers of metal rows placed orthogonally on top of each other. Power and ground rows alternate in each layer. The corresponding power/ground rows in each layer are connected to each other through metal connectors which are referred as micro interconnects in Figure 3.4. For sake of simplicity ground vias are not taken into account. This kind of setup is analogous to considering the ground plane at infinity which is fine for DC analysis. The RDL layer at each level gives the flexibility to route the power from one part of the die to the other. All components including bumps, micro bumps and TSVs are rectangular in cross section. Table 2.2 in chapter 2 gives all the details about the structure used in the electrical stimulation.

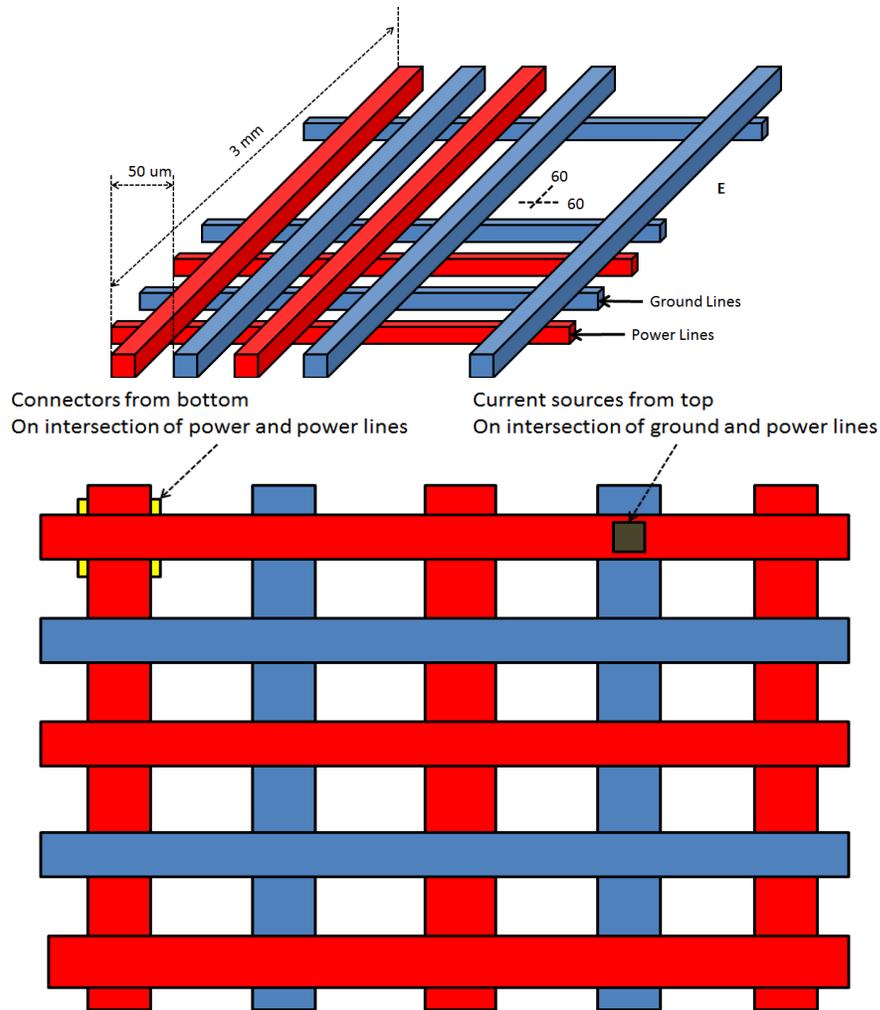


Figure 3.4: Modeled RDL layer in the 3D Stack.

The RDL layer has length (L) = 3 mm for the interposer and 1.1 mm for each of the dies. The thickness (T) of power/ ground conductors is 1 μm . The width (W) is 10 μm and the pitch (P), which is the gap between power and ground conductor is set to 50 μm . The TSV pitch used is 100 μm .

3.3.2 Parameters for Thermal Analysis

For thermal simulations, thermal properties of all the materials are considered. Each die consists of two portions, silicon dioxide insulator and a silicon substrate as shown in Figure 3.5. The interposer and the two dies are bonded together using an adhesive. The

power plane was used in the FR4 board to spread the heat. Power densities were defined for each die to replicate the effect of active devices. The board, substrate, and TSV dimensions were the same as that used for electrical simulations. For simulation purpose isothermal boundary conditions were used at the top to simulate ideal heat sink, with a constant temperature of 30°C. Convection boundary condition with a heat transfer coefficient $10 \text{ Wm}^{-2}\text{K}^{-1}$ was used on the board. Table 2.1 in chapter 2 provides the details of material properties used in thermal simulation.

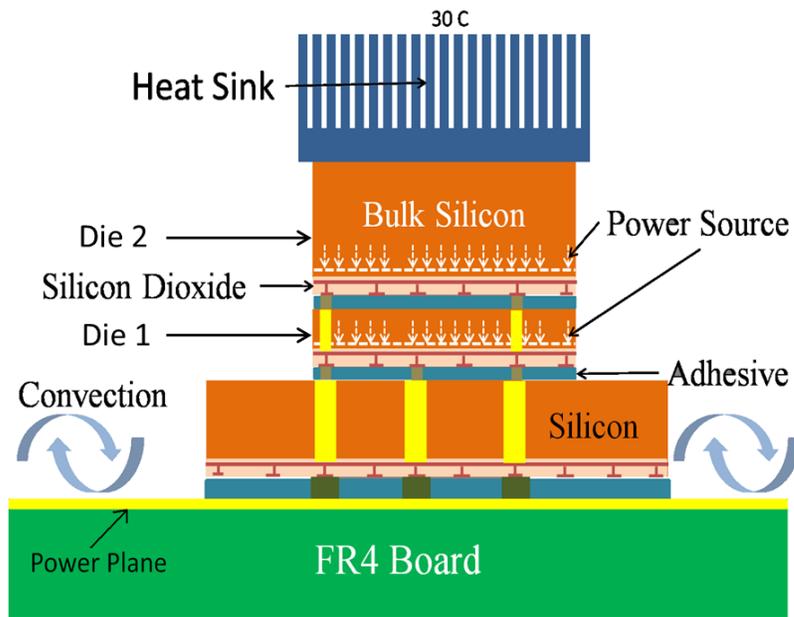


Figure 3.5: Structure used in thermal simulation.

3.4. Simulations

In electrical simulations top and bottom die have power consumption of 5W and 2W respectively and in thermal simulation the power densities of the two dies are taken to be $1\text{W}/\text{mm}^2$ which represents a high heat density. For electrical simulations a 1V supply voltage is chosen. The error is calculated taking the voltage drop on die 1 as the reference. For thermal simulations, temperature on die 1 is chosen to be the reference. The error is calculated for each type of simulation in accordance with equation (2).

Electrical simulations

The TSV maps used in IR drop simulations are shown in Figure 3.6. Map 1 corresponds to the TSVs from interposer to die 1. Map 2 corresponds to the TSVs from die 1 to die 2. The TSV maps are chosen in a random manner and kept constant for each electrical simulation. The simulations were performed in the following order. First a two die simulation is performed observing the voltage on the die 1, followed by a single die simulation. For a single die simulation the information provided is the TSV map 2 and the power consumed by the die 2.

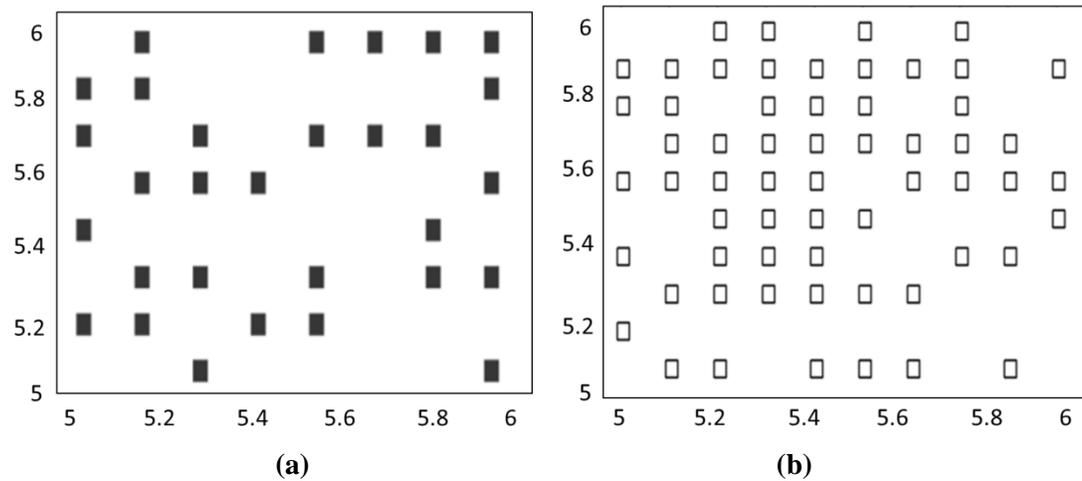


Figure 3.6: TSV maps. (a) Interposer to die 1 (Map 1), (b) Die 1 to Die 2 (Map 2).

Voltage was observed on the RDL layers of die 1 which is just below the active device. The voltage profile for a two die simulation is shown in Figure 3.7. The solid squares denote the TSV positions from interposer to die 1, while the hollow squares denote TSV positions from die 1 to die 2.

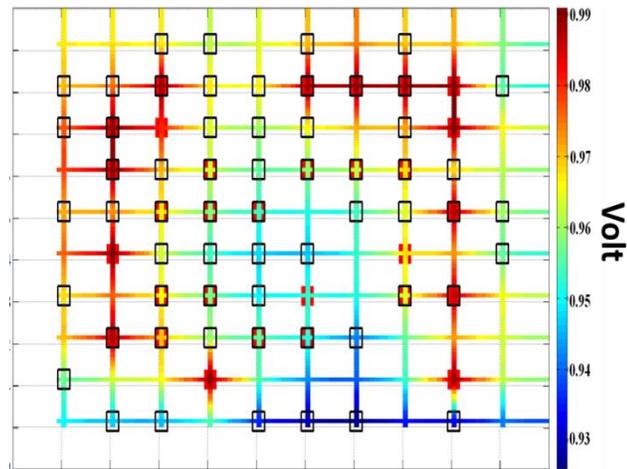
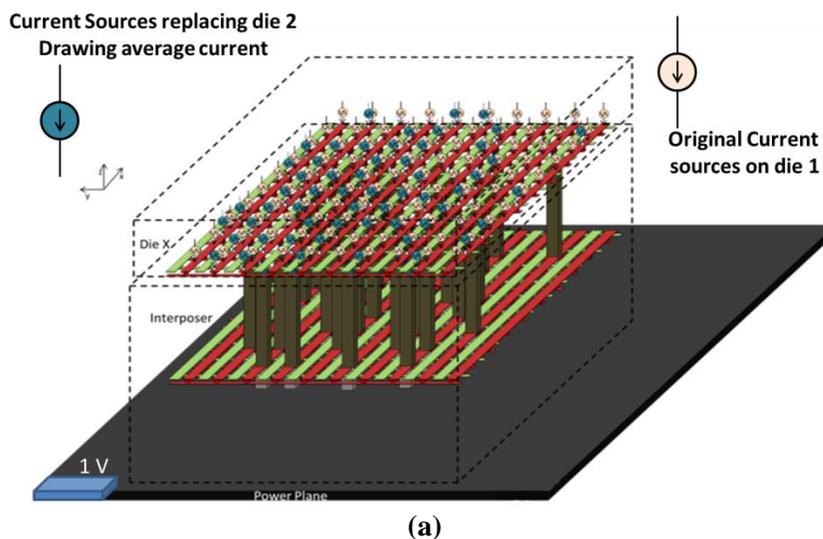


Figure 3.7: Voltage profile on the RDL layer of die 1.

In the second set or single die simulation only die 1 is considered. The information that is shared is the TSV positions from die 1 to die 2 and the total power consumed by die 2. To simulate the effects of power being consumed by the top die, new current sources were added on the bottom die. Current sources are placed on top of these TSVs. With total power and voltage known, the total current was calculated. This current is then equally distributed on the TSVs. Figure 3.8 shows the single die simulation scenario and the resultant voltage map on die 1.



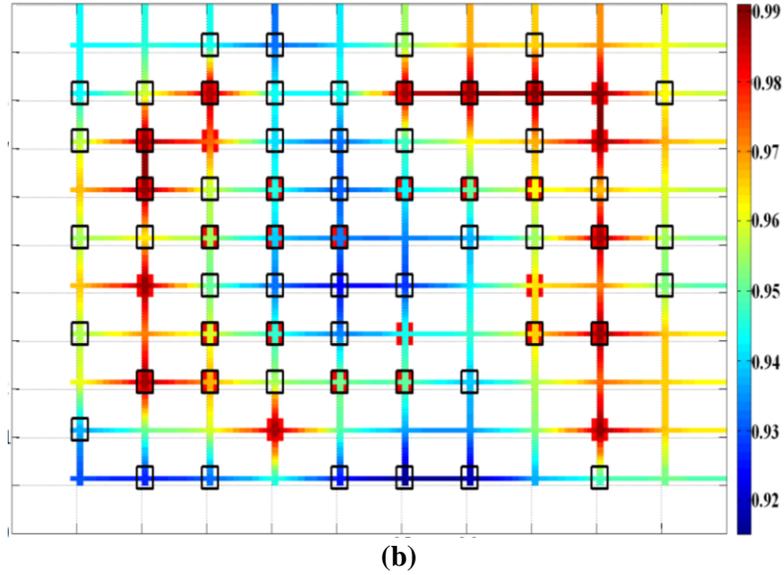


Figure 3.8: (a) Structure for one die simulation, (b) Voltage map of die 1.

The error between the maps shown in Figure 3.9 gives the error when abstraction is applied, where the details of the RDL layer of die 2 is not included.

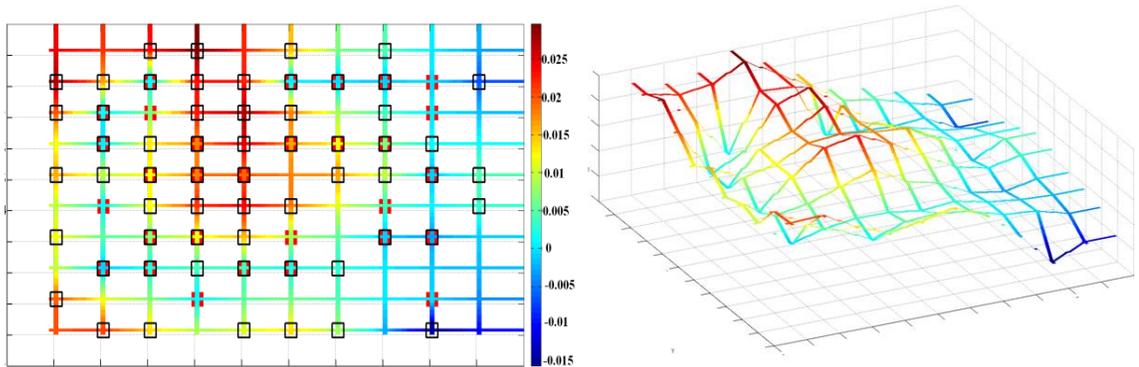


Figure 3.9: The error map. (left) 2D, (right) 3D.

There are a couple of observations that can be made based on the 2D error map. The error for absolute voltages is large where a hollow black square does not have a corresponding solid square at the bottom. This means, if there is no 1:1 correspondence between the TSVs the error tends to increase. Since actual current consumption from TSVs is not known due to the abstraction of RDL layer of die 2, error is more significant at these positions. Also one can see that if a hollow square with no corresponding solid

square at bottom is surrounded by a group of solid squares, the error tends to decrease. We observe that the error is less at positions where there is TSV going from interposer to die1 (solid squares). So, adding more TSVs from interposer to die 1 tends to have an averaging effect on high error areas and reduces the error. From Figure 3.9 we can see the error is only 2 or 3 %. *So does that mean that we have successfully abstracted the data?* The major concern in 3D ICs is voltage drop across various layers of a stack instead of the absolute voltage. Hence it will be more meaningful if error in voltage drop is taken into account. Until then the abstraction of data may not be complete.

A more interesting result is seen when the error in voltage drop is considered instead of absolute voltages. Figure 3.10 shows the voltage drop for one die simulation.

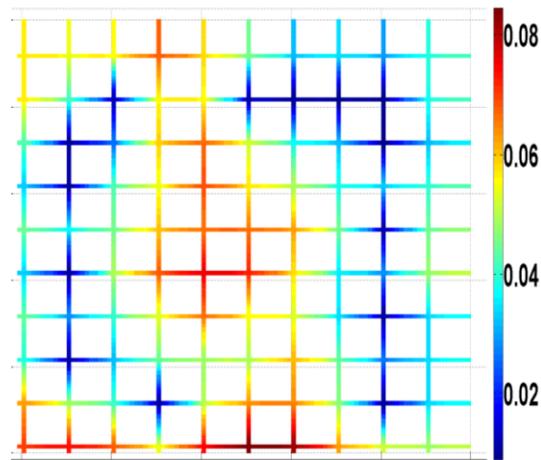


Figure 3.10: Voltage drop in a 1 die simulation (Units Volt).

The surface plot shown in Figure 3.11 gives the error when the details of the RDL layer of die 2 are not passed to die 1. Die 1 uses equivalent current sources to simulate the effect of die 2. In Figure 3.11, the negative error indicates an over estimation of voltage drop while the positive error is an under estimation. We can see that the percentage error is very large as compared to the error in absolute voltage value.

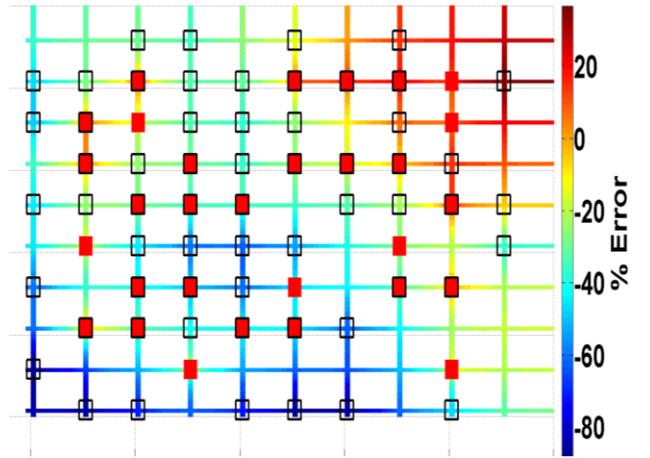


Figure 3.11: The error map for voltage drop.

Another set of simulations was performed where the actual power map information shown in Figure 3.12a is shared between dies. The bottom die still has a uniform distribution. Since top half of the die consumes 80% of power hence 80% of the current was uniformly distributed among top half TSVs while performing a single die simulation. Since the top die consumes 5 W of power, hence its top half will consume 4 W drawing a total current of 4 A from a 1 V supply voltage. Let there be n TSVs in the top half of die 2. So for a single die simulation all current sources at these TSV positions will consume an average of $4/n$ A of current each.

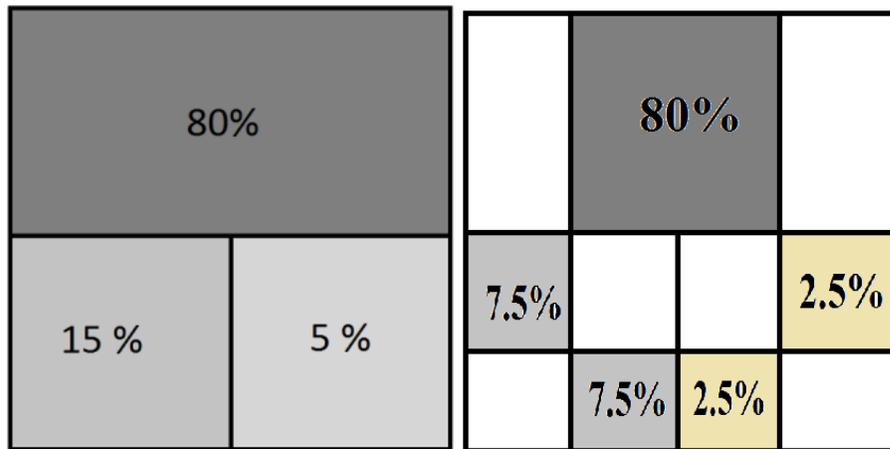


Figure 3.12: (a) power map of the top die, (b) power map of bottom die

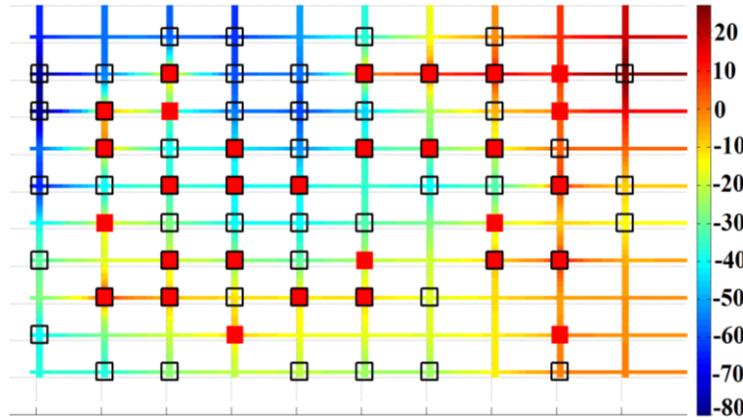


Figure 3.13: Error (%) map when the power map is supplied from die 2.

We see that there is a slight improvement in the error profile, with 5-10% error. This indicates there is critical data that is missing. The current carried by the TSVs in single die simulation is assumed to be uniformly distributed throughout, which most probably is not true.

Two different methods are discussed here to equalize current based on the top die power distribution. Figure 3.14 shows the general RDL and TSV distribution on top of die1.

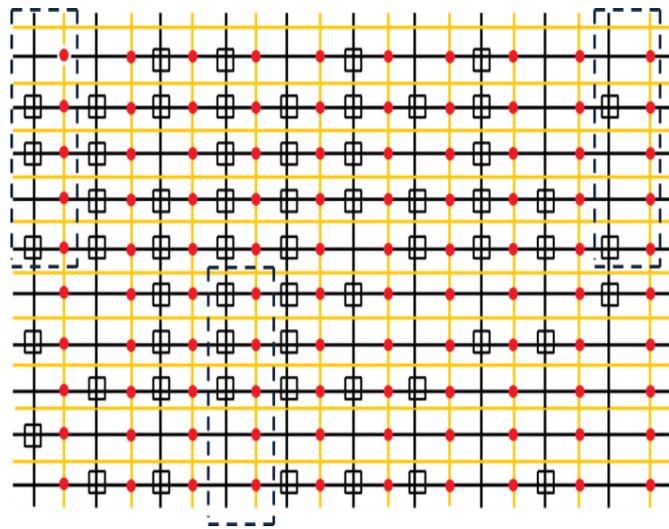


Figure 3.14: Setup 1 for current equalization

The top half die is consuming $4W$ (80%) out of the $5W$ of power. Now in two die case $4W$ is distributed evenly among 50 current sources resulting in $0.08 A$ of current in each source. The current redistribution over TSVs is done on the basis of total current being carried by the left side group of original current sources. So for the top left dotted box let the current carried by each TSV be $I A$. The dots correspond to original current sources, while the square represent the TSVs going from die 1 to die 2.

$$3_{TSVs} * I = 0.08 * 5_{current\ sources}$$

$$I = 0.133 A$$

Figure 3.13 shows the second setup for current equalization.

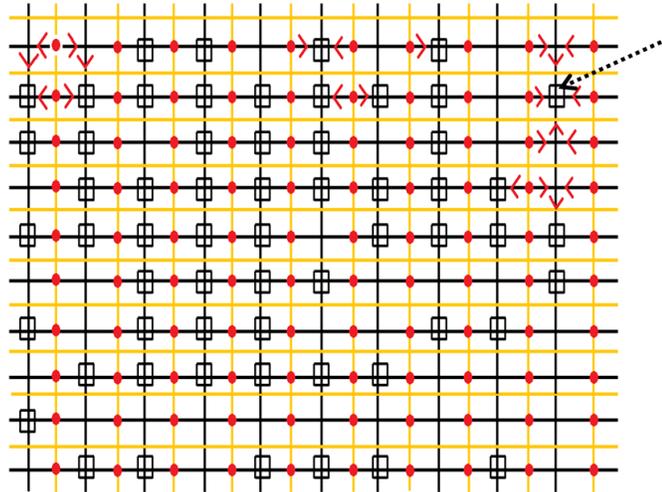


Figure 3.15: Setup 2 for current equalization.

In setup 2, the method is to distribute the current in each TSV (square) according to number of original current sources (dots) around it. Current in each TSV is directed using the nearest TSV approach. If there are two of them then current is divided equally. Hence we assume that current from a current source will flow through its nearest TSV. For example, the top right corner TSV (square) will draw a large current because it has large number of current sources surrounding it (dots). Figure 3.16 shows the error profile obtained from the two setups.

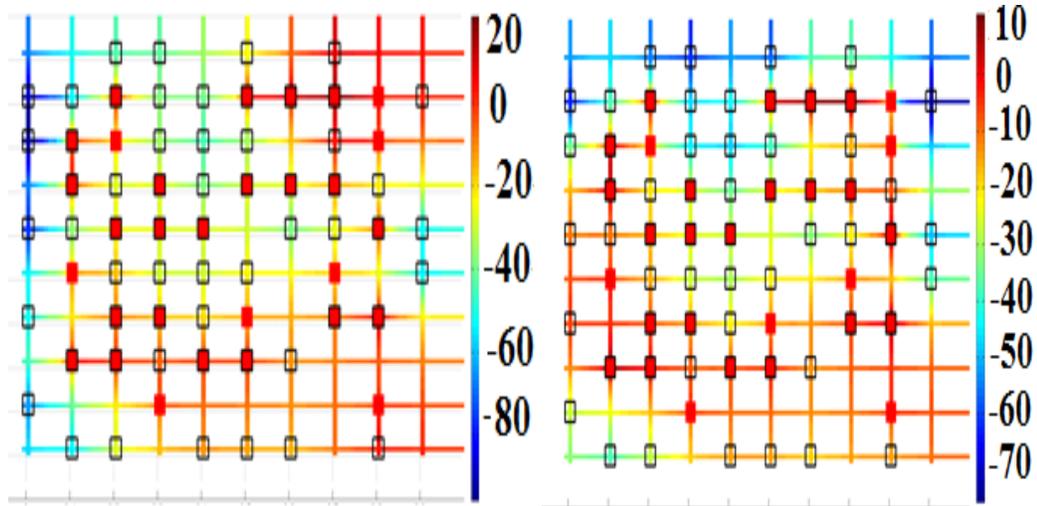
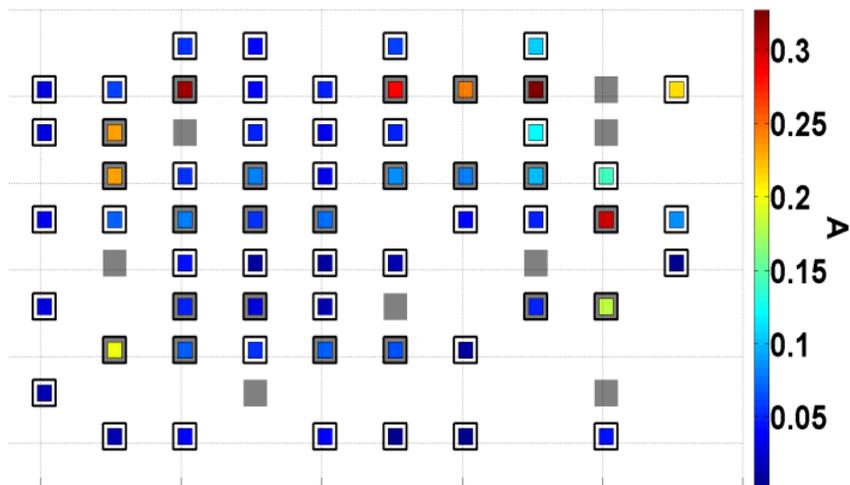


Figure 3.16: Error (in %) plots for (left) setup 1, (right) setup 2.

As can be observed from Figure 3.16 that current carried by the TSVs plays a vital role in reducing the error. To confirm this hypothesis a simulation is performed here. Actual current from a two die simulation is fed as the current values for the TSVs in the single die simulation setup. Figure 3.17a illustrates the current distribution in TSVs. Figure 3.17b shows the error when these current values are used in a single die simulation.



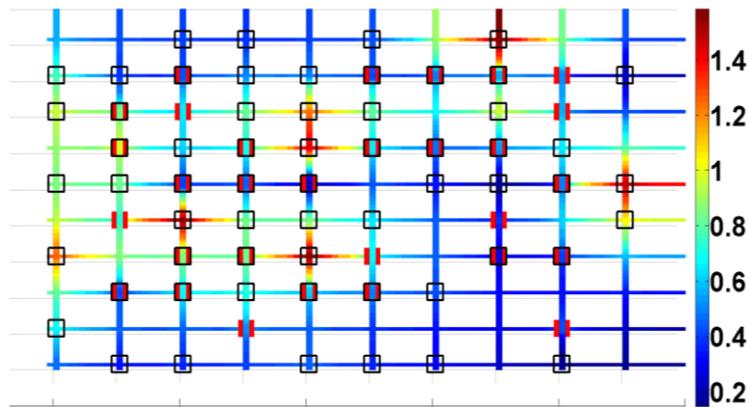
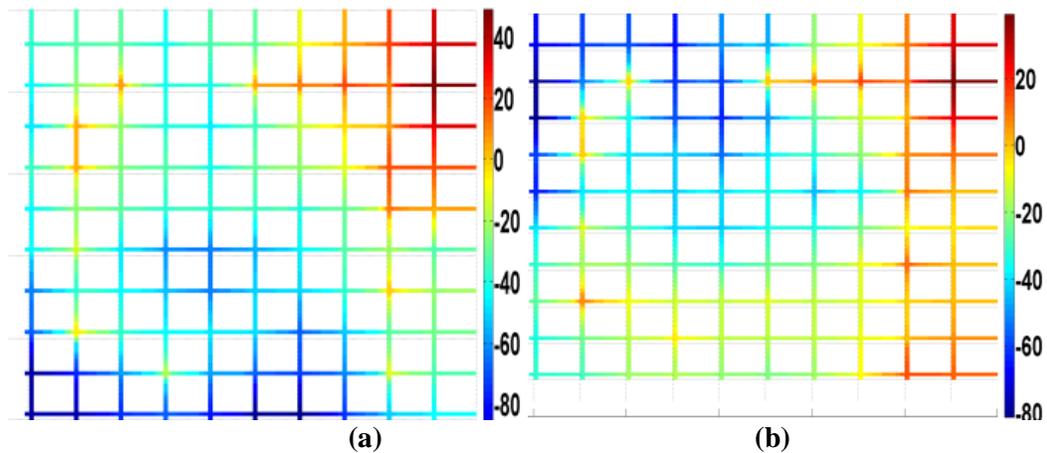


Figure 3.17: (top) Current distribution plot in TSVs from die 1 to die 2 in a two die simulation, (bottom) error (%) plot when these current values are plugged in a single die simulation.

From the current plot we can see that the current is

- **High:** where there is 1:1 correspondence between TSVs in different dies.
- **Medium:** where the TSVs from die 2 to die 1 (hollow) have some TSVs from die 1 to the interposer (solid).
- **Low:** where the TSVs from die 2 to die 1 are somewhat isolated.

A final set of simulations is performed when the bottom die also has a non uniform power map as shown in Figure 3.12b. The results of the simulation are shown in Figure 3.18.



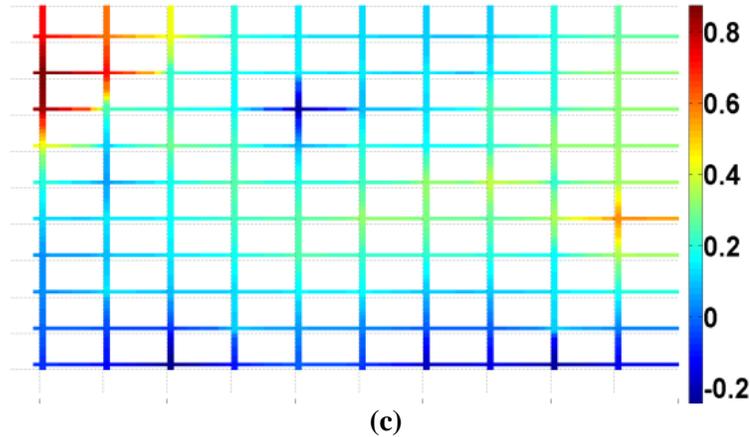


Figure 3.18: (a), Error (%) when only TSV map and total power consumption is given from die 2 to die 1, (b) Error (%) power map is also given and (c) Error (%) when current through TSVs is also given.

Some of the key conclusions that can be made from the above simulations are that as more information is provided the error tends to reduce. Maximum error reduces as the power map information is provided by die 2 in addition to the total power consumption. Hence the vendor of die 1 can minimize the error in the estimation of the voltage drop on die 1 in the presence of die 2 without providing any vital information about die 2 if the user is provided with a power distribution profile of sufficient granularity by the vendor of die 2 in addition to total power consumed by die 2. The granularity of the power map in Die 2 ultimately determines the error. But, in order to significantly reduce the error current drawn by the TSVs should be known. If power map is provided in sufficient detail then currents can be calculated with enough accuracy. The power map profile can aid in deciding the number and position of TSVs to not only minimize voltage drop but also to ensure that maximum current limits of $1.5 \times 10^{11} \text{ Am}^{-2}$ through copper TSVs are not violated, which denotes the electromigration limit for copper.

Thermal Simulations

The same set of simulations were performed with the thermal simulator. For a single die simulation the information passed were the TSV positions, power consumed, the die size and the die material used. The same power map was used for die 2 used as in the case of electrical simulations as shown in Figure 3.12. Figure 3.18 provides the TSV map used for thermal analysis. The dark squares represent TSVs going from interposer to die 1, while the light smaller squares show TSVs from die 1 to die 2.

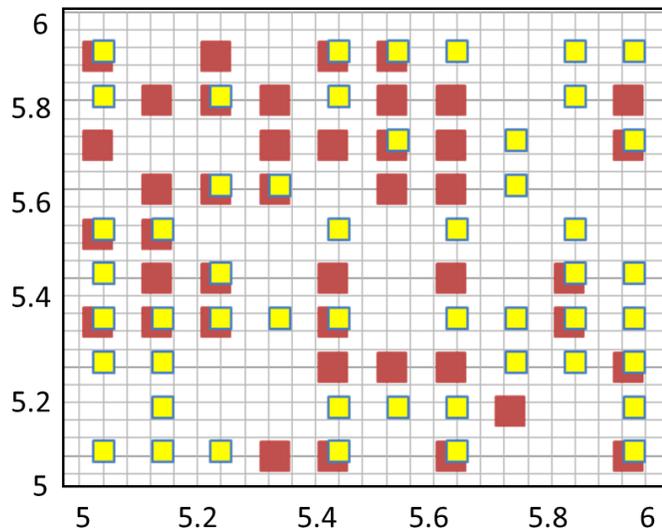


Figure 3.19: TSV map for thermal simulation.

For error calculations we use the temperature profile of die 1 for a complete two die simulation as shown in Figure 3.20. When TSV map and power map are not given die 1 assumes uniform distribution of both based on total power consumption and total number of TSVs.

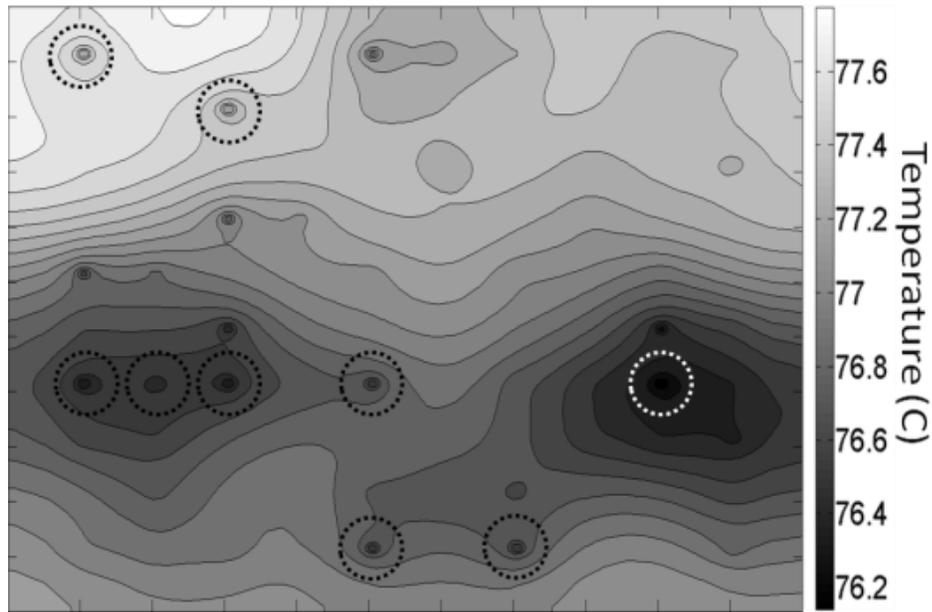


Figure 3.20: Temperature (in $^{\circ}\text{C}$) on die 1 for a complete 2 die simulation.

From Figure 3.20 we can see that there are localized cold spots on die 1 where a TSV going from die 1 to die 2 is directly above a TSV going from the interposer to die 1 (Circled spots). Since TSVs are the primary sources of heat removal from the dies, they conduct away all the heat from die 1 towards the heat sink on the top and towards the bottom resulting in cold spots at these locations.

For single die simulations four possible scenarios were taken into account namely,

- 1) That only the total number of TSVs and total power consumption of die 2 is passed from die 2 to die 1,
- 2) The power distribution profile of die 2 is also provided
- 3) The actual TSV map is also given with total power consumed and
- 4) Power map of the die 2 and TSV map both are passed from die 2. No RDL information is shared in any of these scenarios.

Error for four scenarios when bottom die has a uniform power map has been calculated and shown in Figure 3.21.

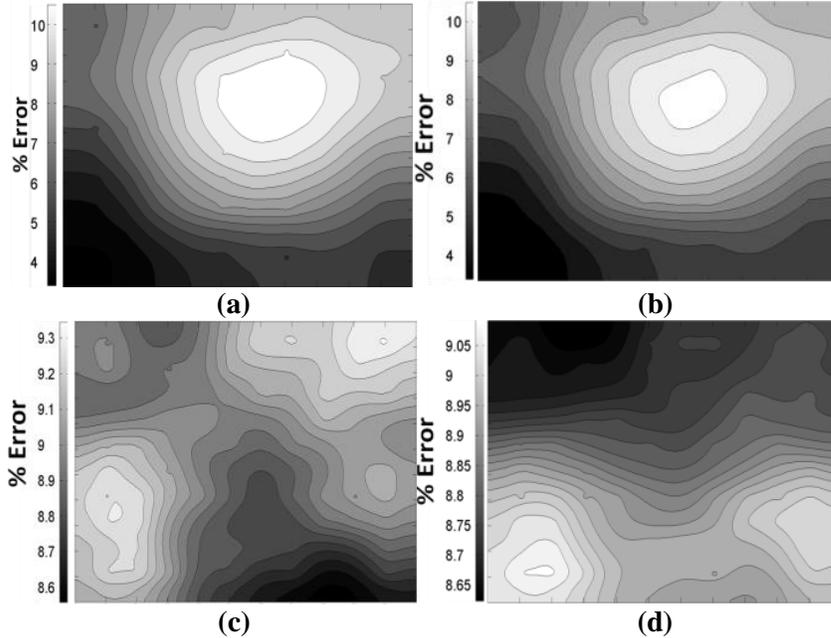
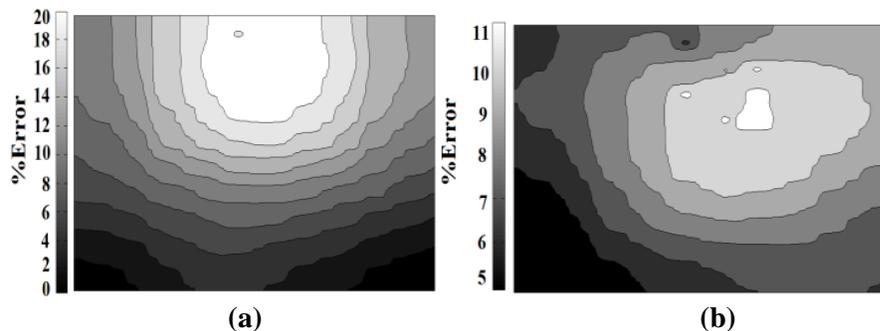


Figure 3.21: When bottom die has a uniform power map. Error maps (White areas show high error, while black areas have low error). (a) No power map or TSV map is given, (b) When power map is given but no TSV map is given. (c) When TSV map is given but power map is not given and (d) when power map and TSV map is given.

We can see that as more information is transferred from die 2 to die 1 the error reduces as it occurred in the case of electrical analysis. Not only does the absolute value of error change, but the error profile also varies along the die. The error is more sensitive to TSV map than the power map of the top die, since error reduction is more significant from Figure 3.21, 3.22b to Figure 3.21, 3.22c than from Figure 3.21, 3.22c to Figure 3.21, 3.22d. For a single die, in case of thermal simulations the RDL layer in die 2 is modeled as an effective metallized layer.

Error for four scenarios when bottom die has a non-uniform power map is calculated and shown in Figure 3.22.



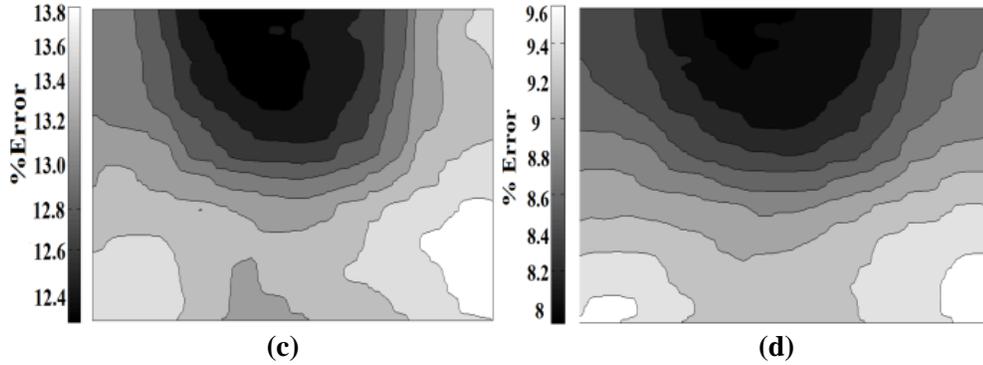


Figure 3.22: When bottom die has a non-uniform power map. Error maps (White areas show high error, while black areas have low error). (a) No power map or TSV map is given, (b) When power map is given but no TSV map is given. (c) When TSV map is given but power map is not given and (d) when power map and TSV map is given.

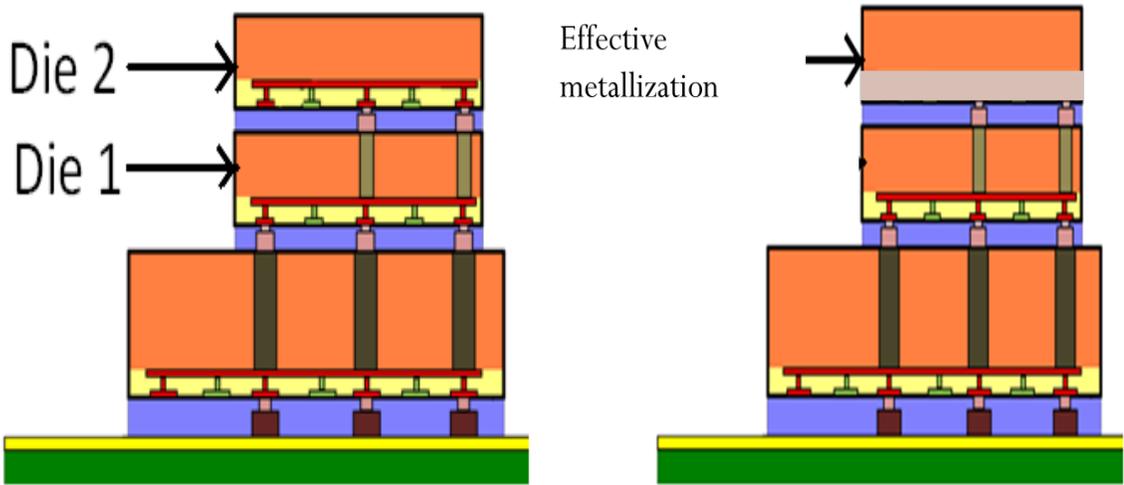


Figure 3.23: Effective metallization used in single die thermal simulation.

The effective metallization of the RDL layer is calculated as

$$\kappa_{eff} = \kappa_{TSV}m_{TSV} + \kappa_{oxide}m_{oxide} \tag{3.1}$$

Where κ is the thermal conductivity and m is the percentage/ fraction of material present. Here no RDL information is passed. Both dies may use same RDLs, same number of metal layers or different metal layers and patterns. As long as the amount of metal used in the metallization layer is passed by die 2 vendor, the die 1 vendor can accurately estimate the temperature on his die.

Figure 3.24 show the temperature profile on top of die 1 for various equivalent metallization values.

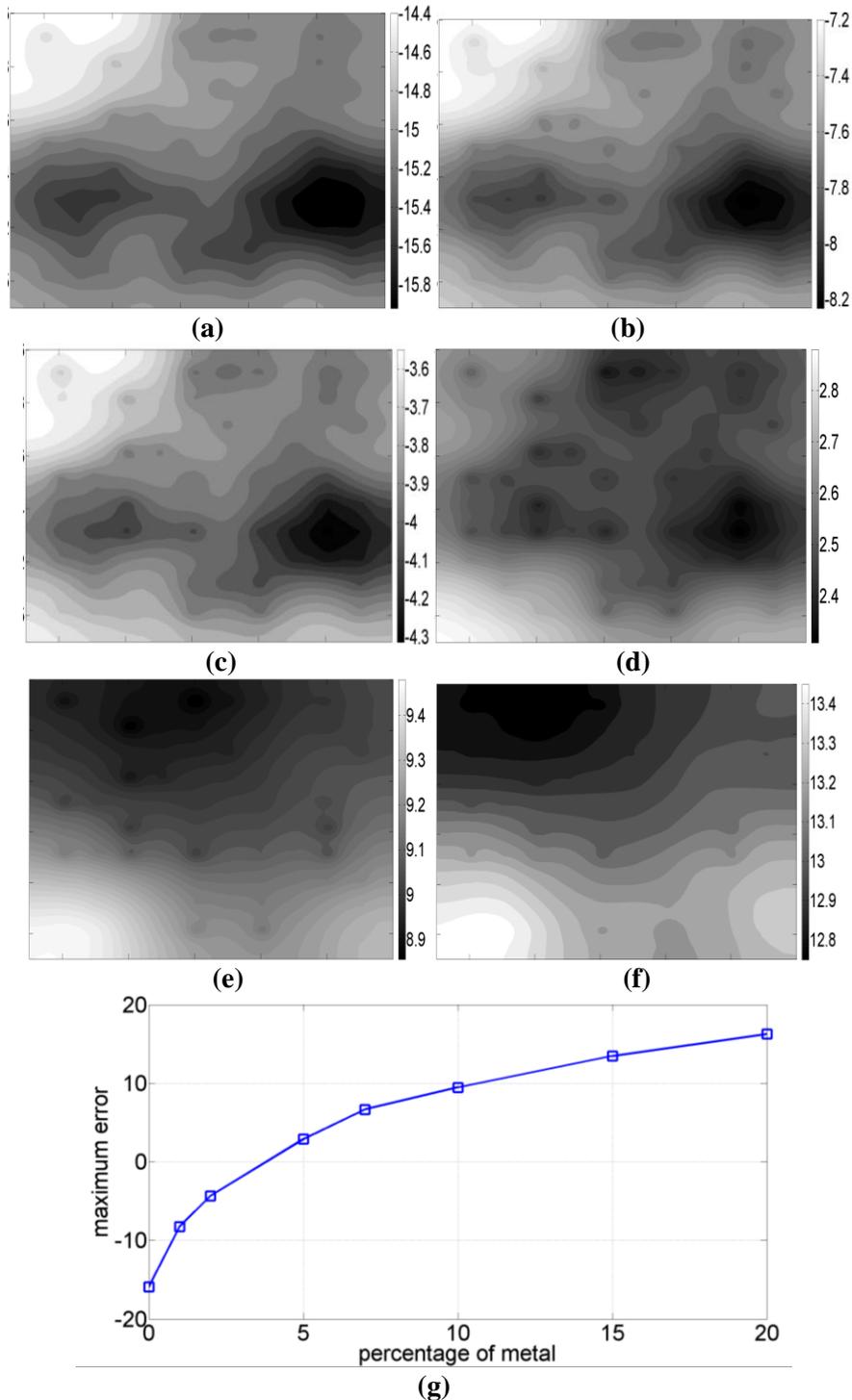


Figure 3.24: (a) SiO₂=100%, Metal = 0%; (b) SiO₂=99%, Metal = 1%; (c) SiO₂=98%, Metal = 2%; (d) SiO₂=95%, Metal = 5%; (e) SiO₂=90%, Metal = 10%; (f) SiO₂=85%, Metal = 15%; (g) Error Vs metallization plot.

3.5 Discussion of Results

For electrical simulations the exact TSV locations and total power consumption of die 2 must be passed to die 1. With this information shared one can estimate the steady state electrical behavior of die 1 in the presence of die 2 as shown in Figure 3.11. Moreover, as shown in Figure 3.13 this estimate can be slightly improved if the actual power map of die 2 is also passed to die 1. But in order to considerably improve the voltage drop estimation, one must know the current passing through the TSVs as accurately as possible as shown in Figure 3.17b.

For thermal simulations a larger set of information needs to be shared by die 2. Thermal profile of a die depends on all the material properties of the die, so sharing only the TSV positions is not sufficient. All material properties and dimensions of die 2 must be shared by die 2. Also power consumed by die 2 and total number of TSVs connecting die 1 and die 2 should be passed along. Simulation results in Figure 3.21a show that even if the actual TSV distribution or power distribution is not shared by die 2, one can get a good estimate of the temperature on die 1. However this estimate can be significantly improved if the actual power map and TSV map is also shared by die 2. This can be observed in Figure 3.21 b-d.

Another conclusion inferred is that the error improvement is more significant when the bottom die has a non-uniform power map. This can be seen in Figure 18a-c for electrical simulations, when the error reduced from 80% to 0.9%. Whereas for thermal simulations, Figure 3.22 a-d shows that the error reduced from 20% to 9% when the bottom die had a non uniform power map. So looking at the thermal simulations, one can say that if a 10% error is tolerable then only the total power consumption of the top die is required if the bottom die has a uniform power distribution. On the other hand if the bottom die has a

non-uniform power map then only passing the total power consumption of the top die can result in large error. Hence the actual power map or the power distribution profile needs to be exchanged. Table 3.1 provides the general parameters that will be required for transfer of parameters from Die 2 to Die 1.

Table 3.1: DEF parameters.

Data in DEF	IR Drop	Thermal Analysis
Power	Total Power consumption of the top die 2 Power map of die 2 with sufficient granularity.(That can be used to determine the current carried by the TSVs from die 1 to die 2)	Total Power consumption of the top die 2 Power map of die 2
TSVs	X, Y coordinates and height of TSVs, materials used in TSV	X, Y coordinates and height of TSVs, materials used in TSV
Materials	No die or interface material information is required	Material properties (dielectric constant, thermal conductivity) used in the die and interface have to be specified.
Ambient	No ambient required	Ambient properties (room temperature, convection coefficient) needs to be specified.

3.6 Design Exchange Format

For IR drop analysis, die 2 provides power map profile of sufficient granularity to Die 1 along with voltage information. These can be in the form of blocks of power maps. Die 1 uses this information to compute the current being drawn by each block. Manufacturer

of die 1 then creates the TSV distribution with (x,y) coordinates and dimension from Die 1 to Die 2 and interposer and starts simulating the IR drop in Die 1 using the power map in Die 1. The voltage drop at the TSV at the top of Die 1 is then passed on to Die 2 along with (x,y) coordinates and dimension for Die 2 to ensure that the voltage drops are adequate for the functioning of Die 2.

Hence, the vendors should provide with details on the position of the voltage and ground bumps, with the maximum allowed IR drop at each of the bump. The current profiles provided in the pin outs will enable the designer of the bottom IC to ensure that there is minimum overlap between the high current areas in the bottom IC based on the current map of the top IC.

Similarly, for thermal simulations die 2 vendor provides the power map and the material properties used in die 2 to die 1. Die 1 vendor then creates a TSV distribution and simulates to get a temperature profile on top of die 1. This temperature profile on top of die 1 can be fed as a boundary condition to the simulator while simulating the temperature profile of die 2, to ensure that the temperature in die 2 does not exceed maximum permissible limits.

So, the 2D power map of each die can be exchanged to facilitate accurate thermal analysis. The 2D power map along with the TSV density map (i.e. thermal conductivity map) of die 1 will allow designers of die 2 to obtain an accurate estimate of temperature behavior of the 3D stack. Therefore, the 2D power map is useful if higher accuracy thermal analysis of the 3D design is desired by vendors of any tier.

3.7 Summary

From the simulations and analysis shown in this chapter it is clear that as more information is exchanged between the top and the bottom die, the vendor of the bottom die can estimate performance of his die in presence of the top die. For electrical simulations the TSV map and the power map need to be passed from die 2 to die 1. Additionally, the better granularity of the power map profile of die 2 provided to die 1, the smaller will be the error in computing the performance of die 1 in the 3D stack. For thermal analysis a more specific set of parameters need to be passed, which include the material parameters and the metallization density in the RDL of die 2 in addition to the TSV and power map.

Some error is bound to occur as actual current path across the RDL cannot be predicted with complete accuracy. Also the assuming uniform metallization in case of thermal simulation is highly idealized as metal traces are not distributed uniformly in an insulator in die 2.

Moreover, as information regarding wiring, routing or RDL is not transferred the sensitive IPs of the dies can be protected.

CHAPTER 4

CONCLUSION AND FUTURE WORK

4.1 Conclusion

Two fundamental issues of 3D IC design were covered in the thesis, namely pathfinding/optimization and standardization for heterogeneous IC integration. Both issues were evaluated using steady state thermal and electrical simulations. These two were considered because they are coupled due to Joule heating.

First thermal and electrical optimization was performed resulting in improved thermal and electrical performance of the complete stack. The optimization considered a two die stack with both dies consuming equal power. For both electrical and thermal simulations, the bottom die power map was optimized while keeping the rest of the 3D structure unaltered. Such a scenario can occur if the dies in a stack are fabricated by two different vendors. Hence altering the properties (power map, TSV map) of the other die was restricted.

Genetic algorithm was used for DC IR drop and thermal optimization and its efficiency was verified by applying it to a two die 3D stack. The simulation results showed 20% improvement in temperature and voltage drop after optimization. It is shown from the thermal optimization results that with a fixed TSV distribution, the best thermal results in a stack occur when the hotspots, which are produced by high power density blocks, are not vertically aligned in a stack. The simulation results also indicated the importance of voltage drop and thermal co-optimization. Hence if a vendor designs the die for low thermal gradient they might end up designing a die which results in a

large voltage drop in the other die. The optimization results presented can help different IC vendors share necessary and sufficient information amongst themselves for effective co-design for a complete 3D stack. One possible application for co design can be optimizing the die for a particular objective. For example, evaluating the delay of an inverter for various optimized thermal and IR drop maps.

A Matrix Synthesis Process (MSP) based algorithm was introduced which can be implemented for thermal optimization for any number of the dies in a 3D stack. The method is fast, memory efficient and can cover a variety of die sizes. Since it does not involve any thermal analysis, it is therefore inadequate in capturing the effect of 3D interconnects like TSVs and RDL layers in the dies. However the results do show that it is an effective approach for reducing thermal gradient when the 3D stack has a large number of layers.

Finally, a TSV Removal algorithm is proposed, which can capture the effects of TSV in a 3D stack. Based on the analysis it was concluded that not all TSV spots are required to maintain a particular voltage drop or temperature. Results from the proposed TSV removal algorithm demonstrated a method to achieve a minimum voltage threshold or maximum temperature limit while minimizing the number of TSVs. The proposed algorithm is flexible and can be tuned for any desired threshold level. Moreover it can be used to minimize TSVs for a particular die layer rather than the whole stack.

The second issue taken into account in the thesis was formulating standards for information exchange between die vendors of a 3D IC. From the simulations and analysis shown in Chapter 3 for design exchange formats it can be concluded that sharing of

information between different die vendors is necessary for effective implementation 3D ICs.

Based on the results it can be inferred that as more information is exchanged between the top and the bottom die, the vendor of the bottom die can accurately predict the functional parameters of their die inside a complete 3D stack.

Granularity or detail of the power map profile of die 2 which is provided to die 1 emerged as a critical factor in improving the error estimate in case of DC IR drop analysis. For the case of thermal analysis, the amount of metal used by die 2 proved to be of critical importance. In sharing of the abovementioned information between different vendors, information regarding wiring, routing or actual placement of active devices is not shared. Hence, the vendors can share adequate information without disclosing their sensitive IPs .

4.2 Future Work

The power maps used in optimization for this thesis have uniform mesh, which is highly idealized. The optimization concept can be extended to non-uniform meshes as well. Figure 4.1 shows a non-uniform mesh power map. Such a mesh not only captures non uniform power distribution but also captures the effect of active area that consumes power. Here P_i/A_i denotes power and area respectively.

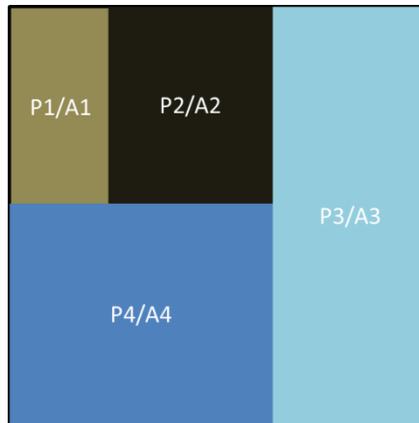


Figure 4.1: Power map with non-uniform mesh.

With the above power map the proposed genetic algorithm can be used to optimized other cost related issues like die area and wire length.

The MSP algorithm does not capture the effects of vertical alignment of hotspots in a 3D stack. Figure 4.2 shows one such case.

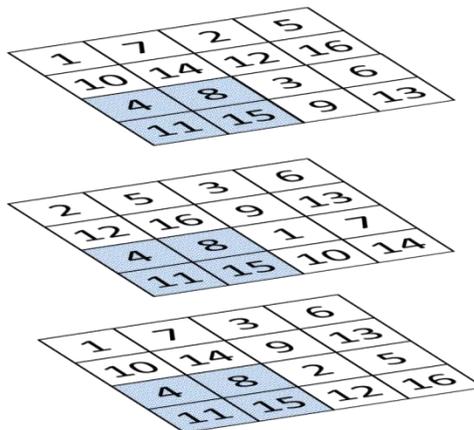


Figure 4.2: Vertical alignment of hotspots in MSP.

In Figure 4.2 the numbers denote the power densities and the shaded region shows the maximum sum sub matrix. We see that all high power density areas are located at the bottom right corner of the stack. This will result in a very high temperature around that region. A possible approach can be a post MSP process which swaps the submatrices such that the maximum sum sub matrix is not aligned as shown in Figure 4.3

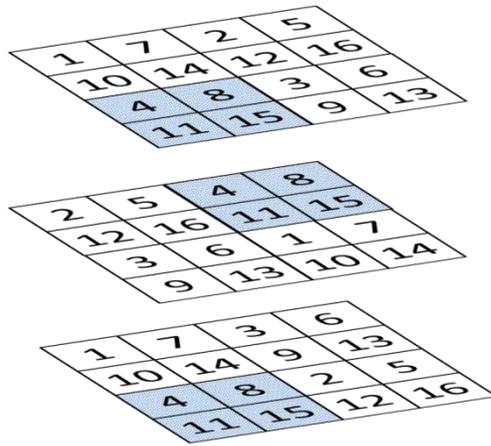


Figure 4.3: Post MSP vertical re alignment of hot spots.

The TSV optimization algorithm has a tendency to get stuck during thermal analysis if there is an insignificant change in the thermal profile after removing the TSV in a particular iteration. The algorithm can be modified to search for the next suitable node for the TSV removal so that it does not get caught in a loop.

From Figure 4.4 a higher granularity power map will result in a better estimation of parameters, but can lead to less level of abstraction. Hence an extensive analysis can be performed from very coarse to very fine meshed power maps and by calculating the error thresholds for both electrical and thermal simulations. This will lead to a large data base which can aid in building the DEF.

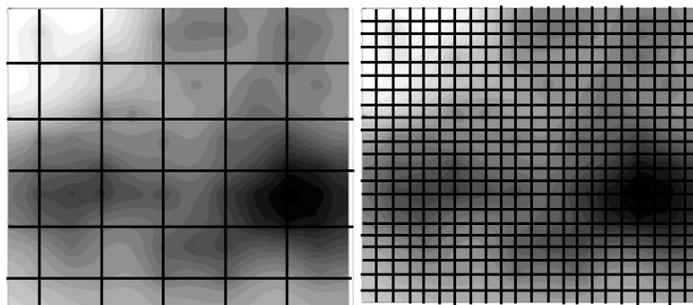


Figure 4.4: Different granularity levels of the power map.

Simulations performed in Chapter 3 can be performed for inductive and capacitive drops as well. Inductive drops can be difficult to model because current return path needs

to be defined, which was omitted in the DC IR drop analysis. This can result in a large problem both for computation and time consumption. One way to tackle the problem is to convert inductive noises in time domain to impedances in frequency domain. Such an interface standard may require only impedance values to be shared between the dies.

For thermal aspect, creating a thermal sensitivity map can be of importance. This map will be generated for each die to inform the sensitivity of “critical parameters” at different locations of a die. The critical parameters can be performance, noise margin, and/or power (static power). Improvements can be made in the current thermal analysis tool such that the temperature map of die 1 can be used by designers of die 2 as the boundary condition during thermal analysis of die 2. This can result in complete abstraction of die 2 parameters. Even the material information or effective metallization parameters need not be provided in the exchange format.

APPENDIX A

ELECTRICAL AND THERMAL TOOL: *POWER ET*

The tool used is a three dimensional DC IR drop solver for simulation of 3D power delivery networks. The tool uses Finite Volume Method (FVM) [22-24] with non-uniform grid. The tool has the capability to solve for inhomogeneous power delivery networks. The tool is able to solve for at least 10 million unknowns on a 3GB machine. The thermal analysis tool also uses FVM to solve the steady state heat equation. Both Joule heating effect from the PDN and convection effect are considered. In this thesis Joule heating effect was not considered.

Implementation	: Matlab
Platform	: Windows
Input Format	: ASCII text file (.txt)
Output Format	: Matlab Data file (.mat)

APPENDIX B

INPUT FILE FORMAT

This is a steady-state electrical-thermal simulation input file

Material parameters

number	E_resistivity	T_coefficient	T_conductivity (x,y,z)			thermal_coefficient(dielectric)
7						
0	1000000000	0	0	0	0	0
1	1.68e-008	0.0039	385	385	385	0
3	1000000000	0	110	110	110	0
4	1000000000	0	0.25	0.25	0.25	0
7	1000000000	0.0045	0.3	0.3	0.3	0
8	1000000000	0.0045	58	58	58	0

#

Object Parameters (Body)

number	x1	y1	z1	x2	y2	z2	material
8							
1	0	0	5	11	11	5.85	4
2	4	4	5.850	7	7	5.890	7
3	4	4	5.890	7	7	6.090	3
3	4	4	6.090	7	7	6.100	8
1	5	5	6.100	6	6	6.120	7
1	5	5	6.120	6	6	6.130	8
1	5	5	6.130	6	6	6.230	3

#

Electrical Excitation (Ebody)

number	x1	y1	z1	x2	y2	z2	material	type	value
10									
1	0	0	5.82	1	1	5.85	1	0	1
302	5.05	5.01	6.13	5.06	5.02	6.14	1	1	-0.0035

#

Thermal Excitation (Tbody)

number	x1	y1	z1	x2	y2	z2	material	type	value
10									
7	5	5	7.119	6	6	7.12	1	0	30
1	5	5	6.13	5.1	5.1	6.13	3	1	596000
1	0	0	5	11	11	5	1	2	10

#

There are four blocks in the file namely material parameters, object parameters, electrical excitation and thermal excitation. The first number after the labels (shown in red) in each body denoted the number of columns in the body. All individual blocks are ended with three ‘#’ signs. Materials in all the blocks should correspond to the same material number in material parameters. All units are in millimeters.

Object parameters:

Every object is a cuboid. The vectors specified denote the two ends of the diagonal of the cuboid.

Electrical excitation:

Type = 0 for voltage excitation (Unit: Volt).

Type = 1 for current excitation (Unit: Ampere). Negative sign is for current consumed and positive for current delivered.

Thermal excitation:

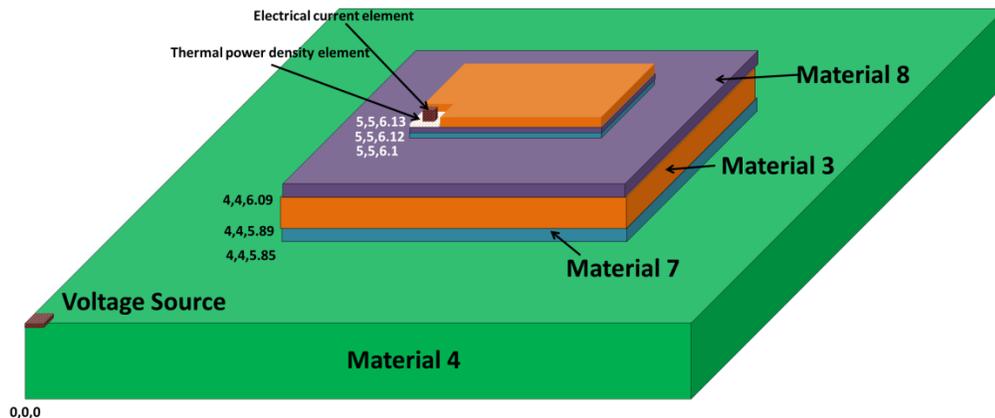
Type = 0 for constant temperature boundary condition (Unit: °C).

Type = 1 for power density. When $z_1=z_2$ then surface power density (Unit: W/m^2). When $z_2>z_1$ then volumetric power density (Unit: W/m^3).

Type = 3 for convection boundary condition (Unit: W/m^2K).

While defining surface excitations care should be taken that surface excitation should not go beyond the structure definition in the object parameter block.

Figure below shows the structure created by the above input file.



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