Modeling and Co-simulation of Signal Distribution and Power Delivery in Packaged Digital Systems

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Modeling and Co-simulation of Signal Distribution and Power Delivery in Packaged Digital Systems

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To My Family,

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TABLE OF CONTENTS

DEDICATION . . . . . **iii**

ACKNOWLEDGEMENTS . . . . . **iv**

LIST OF TABLES . . . . . **viii**

LIST OF FIGURES . . . . . **ix**

SUMMARY . . . . . **xiv**

I INTRODUCTION **1**

1.1 Need for modeling and co-simulation in PCB/package design 3

1.2 Extraction of switching noise current 7

1.2.1 Analytical estimation of switching noise current 7

1.2.2 Measurement based switching noise current extraction for ASICs . 9

1.2.3 Switching noise current extraction using clock modulation 11

1.3 Conversion of a PDN response to the time domain 12

1.3.1 Macro-modeling 12

1.3.2 Direct simulation using S-parameters 15

1.4 Proposed research and dissertation outline 17

II WAVELET BASED DE-NOISING AND MODELING OF TRANSIENT WAVEFORMS **22**

2.1 Discrete wavelet packet transform 23

2.1.1 Optimal basis selection 26

2.2 Noise estimation and thresholding 28

2.3 Modeling using generalized pencil-of-function method 29

2.4 Test results 31

2.4.1 Simulation test case 31

2.4.2 Measurement test case 36

2.5 Summary 42

III MODELING OF SWITCHING NOISE CURRENT SIGNATURES . **44**

3.1 Functioning Sun Microsystems computer system 46

3.1.1 Description of the setup 46

3.1.2 Switching noise current signature extraction 49
3.1.3 Simulation of SSN 51
3.2 IBM Power5 microprocessor 56
3.2.1 Description of the setup 56
3.2.2 Study of the sensitivity of the waveform measurement duration on its spectral content 59
3.2.3 Switching noise current signature extraction 63
3.3 Summary 63
IV TRANSIENT CO-SIMULATION OF SIGNAL AND POWER NETWORKS WITH CAUSALITY ENFORCEMENT 66
4.1 Causality enforcement in transient simulation 68
4.1.1 The causality violation problem 68
4.1.2 Delay extraction from frequency response of passive networks . . . 70
4.1.3 Causality enforcement using signal flow graphs 74
4.2 Implementation of fast convolution 77
4.2.1 Fast convolution using Lagrange approximation 79
4.2.2 Performance analysis of the fast convolution algorithm 82
4.2.3 Miscellaneous computational aspects in the SFG based transient simulation 87
4.3 Transient co-simulation of passive systems 89
4.3.1 Integration of the SDN and the PDN 91
4.3.2 Test case 93
4.4 Summary 97
V SIGNAL INTEGRITY ANALYSIS OF PASSIVE SYSTEMS USING TRANSIENT CO-SIMULATION 100
5.1 Single conductor transmission line systems 102
5.1.1 Stripline interconnect 103
5.1.2 Microstrip interconnect with via transitions 105
5.2 Multiconductor transmission line systems 107
5.2.1 Coupled microstrip interconnects 107
5.2.2 32-bit microstrip interconnect bus 108
5.2.3 64-bit microstrip interconnect bus 112

5.3 Analysis of noise coupling between the SDN and the PDN 113
5.3.1 Simulation of an 8-bit interconnect bus 114
5.3.2 Analysis of the noise coupling on a quiet line adjacent to a noisy 8-bit bus 115
5.4 Real world examples 120
5.4.1 IBM HyperBGA package 120
5.4.2 PCI Express I/O interface 126
5.5 Summary 133
VI CONCLUSION AND FUTURE WORK 135
6.1 Conclusion 136
6.2 Future work 138
6.3 Publications 139
APPENDIX A — TOTAL LEAST SQUARES DECONVOLUTION . . 142
APPENDIX B — MIXED MODE S-PARAMETERS 144
APPENDIX C — NODAL ADMITTANCE METHOD AND STAMP RULE 147
REFERENCES 150
VITA 154

LIST OF TABLES

1 λ_n for various thresholding techniques and data lengths 29

2 List of complex pole pairs used in the simulation test case 31

3 De-noising results using the proposed technique 35

4 Delay extraction for differential transmission lines 74

5 Simulation of a stripline interconnect system 105

6 Simulation of a microstrip interconnect system with a via discontinuity . . . 106

7 Simulation results for coupled microstrip interconnects 109

8 Simulation results for 32-bit microstrip interconnect bus 112

9 Simulation results for 32-bit microstrip interconnect bus 113

10 Simulation results for IBM HyperBGA package 122

11 Component values for the PCI-X I/O interface model 128

12 Simulation results for PCI-X I/O interface 129

13 Simulation results for overclocking of the PCI-X I/O interface 130

LIST OF FIGURES

1 Operating frequency trends in Intel microprocessors 2
2 Partial simulation approach to PCB/package design 2
3 Traditional approach for post-layout simulation 4
4 Influence of SSN on the simulation of an SSTL-2 interface 5
5 Flow chart for system level SI-PI analysis through macro-modeling 6
6 Triangular approximation of transient switching noise current 7
7 A modelled switching noise current spectrum 8
8 Schematic layout for noise current spectrum determination 9
9 Equivalent circuit model of the ASIC board 10
10 Switching noise current spectrum for an ASIC 10
11 Clock gating mechanism 11
12 Switching noise current spectrum for IBM POWER4 chip 12
13 Generation of lumped-element-circuits using rational function approximation 13
14 Causality violation in transient simulation using macro-modeling 14
15 Schematic of network used for the definition of modal S-parameters 15
16 Signal flow graph of a two port S-parameter network 15
17 Signal flow graph of coupled transmission lines with nonlinear terminations 16
18 Proposed approach for transient co-simulation 18
19 Steps involved in de-noising and modeling of transient signals 24
20 Fixed scale wavelet packets 25
21 DWPT representation of a data vector at 4 different scales along with the sfp values of each packet wavelet coefficient 26
22 Transient response obtained using pole pairs from Table 2 32
23 S-plane plots of the extracted poles for $\sigma = 0.01$ 32
24 S-plane plots of the extracted poles for $\sigma = 0.1$ 33
25 S-plane plots of the extracted poles for $\sigma = 0.15$ 33
26 S-plane plots of the extracted poles for $\sigma = 0.2$ 34
27 S-plane plots of the extracted poles for $\sigma = 0.25$ 34
28 S-plane plots of the extracted poles for $\sigma = 0.3$ 35

29 Comparison of % error in the imaginary part of extracted poles 36
30 Comparison of the time and frequency domain measurements of the SSN voltage waveform 37
31 Optimal DWPT representation of the measured SSN voltage waveform . . . 38
32 Comparison of the measured SSN waveform with its de-noised version . . . 39
33 Singular value decomposition of the SSN voltage waveform 39
34 Comparison of the de-noised and modelled SSN waveform with its SA measurement 40
35 Comparison of the modelled and measured SSN waveform in the time domain 41
36 Time domain comparison over 200ns interval around noise peak 41
37 SSN model from Figure 34 with a higher noise floor 42
38 Transient waveform generated using Hilbert transform on the magnitude spectrum 43
39 Flow diagram for extraction of switching noise current signatures 45
40 Top view of the functioning board 46
41 Circuit schematic of test system along with port locations 47
42 SSN measured at port 2 of the computer system 48
43 SSN measured at port 1 of the computer system 48
44 Equivalent Z-parameter circuit 49
45 Frequency spectrum of I_{Noise} at port 2 50
46 Frequency spectrum of I_{Noise} at port 1 51
47 Two port equivalent circuit of the PDN 52
48 Spectral content of I_{SSN} 53
49 Time domain signature of I_{SSN} 53
50 Measurement-simulation correlation of SSN using measured Z_{12} 54
51 Measurement-simulation correlation of SSN using modelled Z_{12} 55
52 Relative error between measured and modelled values of Z_{12} 55
53 Comparison between the spectra of the two simulated SSN waveforms . . . 56
54 SSN measured on the PDN of an IBM Power5 microprocessor 57
55 Frequency domain comparison of the SSN in an IBM Power5 microprocessor 58
56 Magnitude of PDN impedance computed using the clock gating technique . 58
57 Real and imaginary parts of the PDN impedance profile 59

58 Spectral content of SSN measurement 4096 samples in length 60
59 Spectral content of SSN measurement 8192 samples in length 61
60 Spectral content of SSN measurement 16384 samples in length 61
61 Spectral content of SSN measurement 32768 samples in length 62
62 Spectral content of SSN measurement 65536 samples in length 62
63 Time signature of the mid-frequency switching noise current 64
64 Spectral content of the mid-frequency switching noise current 64
65 Multiple causality conditions on a transmission line 68
66 Causality violations in transient simulation of a transmission line 70
67 Z-parameter magnitude response for the plane 73
68 Z-parameter phase response for the plane 73
69 Magnitude response for $Z12_{min}$ and $Z12_{AP}$ 74
70 Phase response for $Z12_{min}$ and $Z12_{AP}$ 75
71 Signal flow graph of the transmission line circuit 75
72 Causal transient simulation of the transmission line circuit 77
73 Minimum eigenvalue plot with and without causality enforcement 78
74 A typical impulse response for a lossy passive network 80
75 Fast convolution using impulse response partition 80
76 Accuracy of the fast convolution method for a single transmission line system 82
77 Magnification around one of the signal peaks from Figure 76 83
78 Error tradeoff for the fast convolution algorithm 84
79 Speedup obtained using the fast convolution algorithm 84
80 Transient simulation of a 130-port network using fast convolution 85
81 Error tradeoff for the 130-port network simulation 86
82 Speedup obtained for the 130-port network simulation 86
83 Time-lines of the simulation progress using normal convolution and fast convolution 87
84 Kaiser windows with different shape parameters 89
85 Flow chart of the SDN-PDN co-simulation methodology 90
86 Microstrip transmission line referenced to non-ideal power/ground planes . 93
87 Integration of the SDN and the PDN using ADS (Screen shot) 94

88 Magnitude response of $s12$ and its minimum phase and all pass components 95
89 Phase response of $s12$ and its minimum phase and all pass components . . . 96
90 Circuit schematic of the microstrip system simulated using ADS 96
91 Comparison of the transient waveforms obtained using SFG and using ADS 97
92 Comparison of the Vdd waveforms obtained using SFG and using ADS . . . 98
93 Steps involved in the transient co-simulation methodology applied in this chapter on various test structures 101
94 Stripline interconnect referenced to non-ideal power/ground planes 103
95 Causal simulation of stripline interconnect 104
96 Non-causal simulation of stripline interconnect 104
97 Microstrip interconnect with a via discontinuity and non-ideal reference planes 105
98 Causal simulation of microstrip interconnect with via discontinuity 106
99 Non-causal simulation of microstrip interconnect with via discontinuity . . . 107
100 Coupled transmission lines referenced to a non-ideal PDN 108
101 Causal simulation of coupled microstrip interconnects 108
102 Non-causal simulation of coupled microstrip interconnects 109
103 32-bit microstrip bus referenced to a non-ideal PDN 110
104 Causal simulation of 32-bit microstrip interconnect bus 111
105 Non-causal simulation of 32-bit microstrip interconnect bus 111
106 Causal simulation of 64-bit microstrip interconnect bus 112
107 Non-causal simulation of 64-bit microstrip interconnect bus 113
108 8-bit microstrip bus referenced to a non-ideal PDN 114
109 System output when only a single driver is switching 115
110 System output when all 8 drivers are switching 116
111 System for analyzing noise coupling on a quite line in the presence of a noisy bus 117
112 Peak noise on the quiet line 118
113 RMS noise value on the quiet line 118
114 Transfer impedances between the quiet line locations and the 8-bit bus . . . 119
115 Spectral content of the switching current generated by the 8-bit bus 119
116 Signal layer on the IBM HyperBGA package 121
117 Coupling between adjacent traces on the IBM HyperBGA package 121

118 Eye-diagram observed on a signal net in the IBM HyperBGA package . . . 122
119 Eye-diagram observed on the signal net in the presence of SSN 123
120 Screen shot of BEMP macro-modeling the PDN 125
121 Schematic of a PCI-X bus 126
122 Simulation model for the PCI-X I/O interface 127
123 Causal simulation of PCI-X I/O interface 128
124 Non-causal simulation of PCI-X I/O interface 129
125 Transient output of the PCI-X I/O interface circuit 130
126 Causal (left) and non-causal (right) simulation of the PCI-X I/O interface circuit at 1 GHz 131
127 Causal (left) and non-causal (right) simulation of the PCI-X I/O interface circuit at 1.5 GHz 131
128 Causal (left) and non-causal (right) simulation of the PCI-X I/O interface circuit at 2 GHz 132
129 Causal (left) and non-causal (right) simulation of the PCI-X I/O interface circuit at 2.5 GHz 132
130 Percentage error due to causality violations against operating frequency . . 133
131 A mixed-node circuit being simulated using the CFDRC developed simulator interface 139
132 Incident and reflected power waves in a 4-port network 144
133 A circuit to illustrate the principles of Nodal Admittance method 147

SUMMARY

The pursuit for higher performance at a lower cost is driving rapid progress in the field of packaged digital systems. As the complexity of interconnects and packages increases, and the rise and fall time of the signal decreases, the electromagnetic effects in distributed passive structures become an important factor in determining the system performance. Hence there is a need to accurately simulate these parasitic electromagnetic effects that are observed in the signal distribution network (SDN) and the power delivery network (PDN) of an electronic system. The accurate simulation of high-speed systems requires information on the high frequency transient currents that are injected into the power distribution network causing simultaneous switching noise. Existing techniques for determining these transient currents are not sufficiently accurate. Furthermore existing transient simulation techniques suffer from two major drawbacks: 1) they are not scalable and hence cannot be applied to large sized systems, and 2) the time domain simulations violate causality. This dissertation addresses the above-mentioned problems in the domain of high-speed packaging. It proposes a new technique to accurately extract the transient switching noise currents in high-speed digital systems. The extracted switching noise currents can be used in both the frequency domain and the time domain to accurately simulate simultaneous switching noise. The dissertation also proposes a methodology for the transient co-simulation of the SDN and the PDN in high-speed digital systems. The methodology enforces causality on the transient simulation and can be scaled to perform large sized simulations. The validity of the proposed techniques has been demonstrated by their application on a variety of real-world test cases.

CHAPTER I

INTRODUCTION

The scaling of the CMOS transistor over the past decade has resulted in an ever increasing number of transistors being integrated on a single chip. Based on Moore's Law, this number virtually doubles every 18 months. This high level of integration at the semiconductor level has already enabled the design of microprocessors in the Gigahertz range. Figure 1 shows the operating frequency trends in Intel microprocessors over the last few years. Based on the International Technology Roadmap for Semiconductors (ITRS) [2], this rapid increase in the system clock frequency is expected to continue over the coming years for both desktop and mobile computers. To make efficient use of this enhanced on-chip processing capability, the board and package level signal and power distribution networks are expected to improve in performance at a comparable rate. This has created a major design challenge for the reliable and efficient distribution of signal and power in high performance digital systems. The cause for this design challenge is two-fold: 1) the increasing frequencies and miniaturization of the signal and power distribution networks requires analysis of various parasitic effects that could be ignored in the past, and 2) the shortening life-cycles of electronic products have squeezed the design-cycle time that is available to a design engineer.

A typical approach that is used in the industry for the design of printed circuit boards (PCBs) and packages is shown in Figure 2 [5]. This approach is called the partial-simulation approach to PCB/package design and involves making modifications to an original design layout based on rigorous simulations and analyses. In this approach a design engineer develops an initial layout of a system based on the design specifications of the product and the design rules of the fabrication process. The signal distribution network (SDN) and the power delivery network (PDN), which are a part of this layout are then analyzed using rigorous post-layout simulations. The simulation and analysis of the SDN, termed as signal integrity (SI), is typically carried out in the time domain and involves analyzing voltage

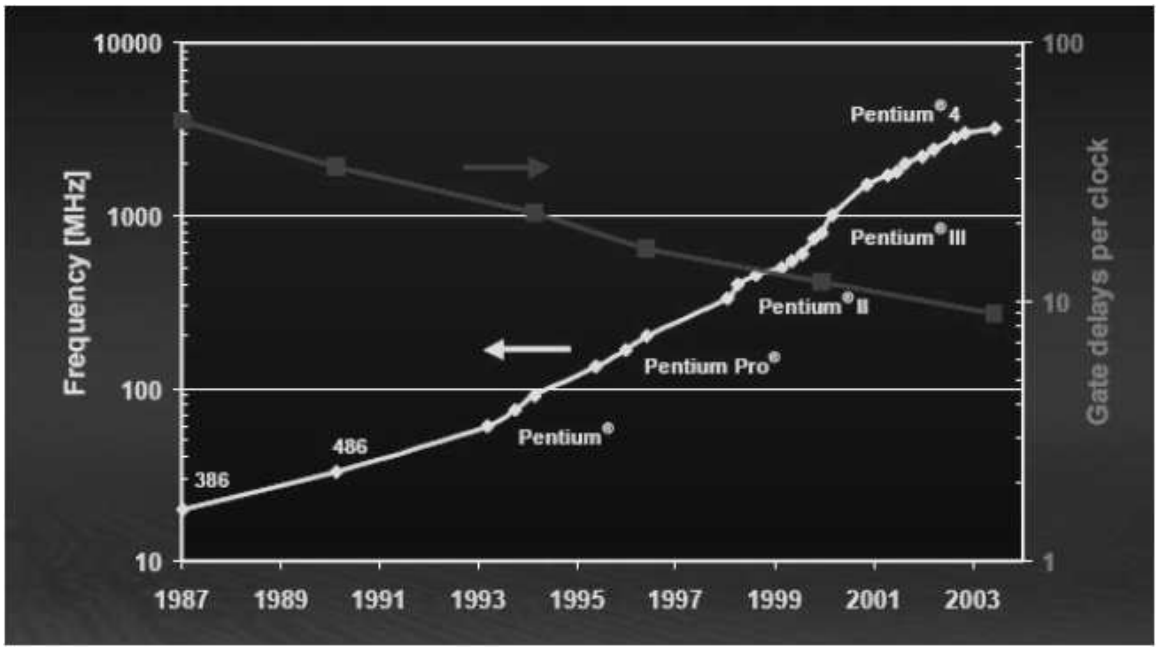

Figure 1: Operating frequency trends in Intel microprocessors

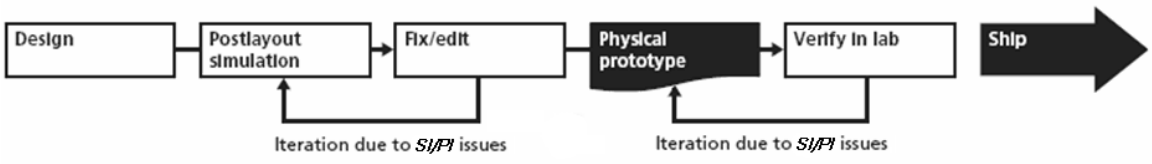

Figure 2: Partial simulation approach to PCB/package design

drops on interconnects, conductor and substrate losses, reflections on electrically long interconnects, impedance mismatches, and transmission line discontinuities like vias and bends. On the other hand the simulation and analysis of the PDN, termed as power integrity (PI), is performed in the frequency domain and primarily involves analyzing power/ground planes, decoupling capacitors, and simultaneous switching noise (SSN). The original layout is modified based on these SI and PI analyses to account for any design flaws. This process is often iterated through multiple times till the SI and PI analyses are satisfactory. The layout is then sent for fabrication. The physical prototype obtained from fabrication is measured and analyzed in a laboratory. Design flaws arising due to parasitic effects that could not be captured in the simulation phase are accounted for here by performing the necessary layout modifications. This modified layout is then re-fabricated and re-measured till a working prototype of the required system is obtained.

1.1 Need for modeling and co-simulation in PCB/package design

The goal of a PCB/package design engineer is to obtain a functioning prototype of the design using minimum number of design iterations. Since the generation and modification of a design layout is a time consuming process, and prototype fabrication is expensive, increased number of iterations in the design phase is expensive both from a time and a cost standpoint. Accurate modeling and simulation of the SDN and the PDN enables a design engineer to identify potential design flaws upfront, resulting in design time reduction and cost savings. Hence extensive research is being carried out on the problems associated with the simulation of the SDN and the PDN in high speed digital systems [15] [13] [24].

Traditionally the analyses of the SDN and the PDN have essentially been carried out independently. This is shown in the flowchart in Figure 3. From the flowchart it is seen that the layout of a package is first processed to separate the SDN and the PDN. The PDN is then modelled using one of the several existing techniques in the literature. Examples include the Transmission Line Method [40], [50], which uses a two dimensional array of transmission lines or distributed RLGC elements in SPICE, the cavity resonator method [38], [39], and the

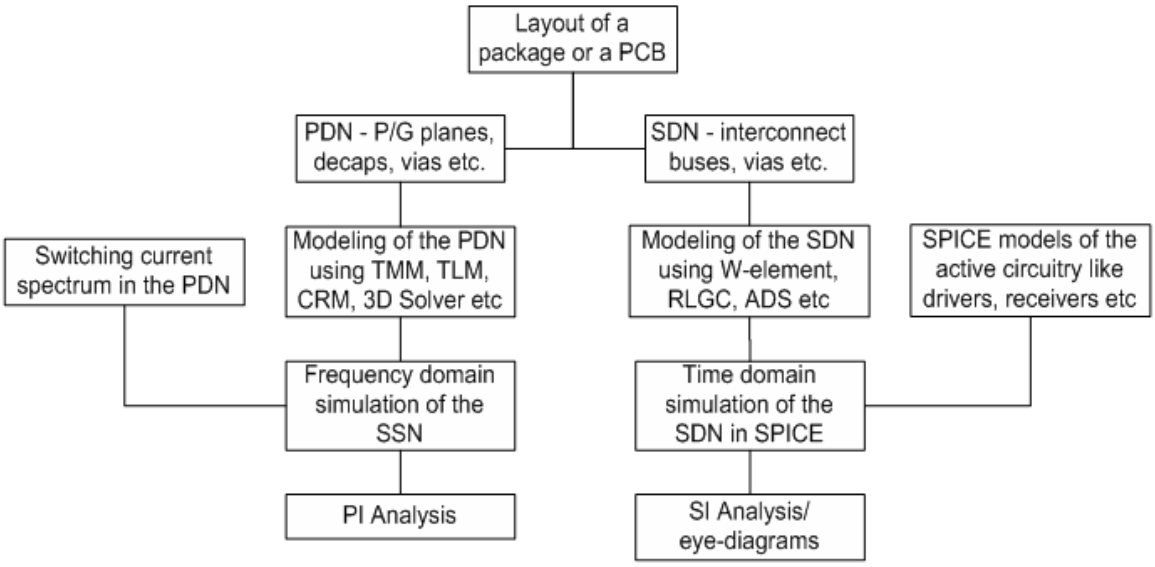

Figure 3: Traditional approach for post-layout simulation

Transmission Matrix Method [30], [29], [31]. The PDN model thus obtained is simulated in the frequency domain to estimate the spectrum of the SSN in the system. Based on this simulation the PI analysis of the system is performed. In a similar fashion, the SDN is modelled using existing techniques like W-elements [42], or RLGC parameters. These models which are SPICE compatible, are then combined with the SPICE netlists of the drivers and receivers, and simulated in the time-domain to perform an SI analysis of the system.

However it is known that effects like simultaneous switching noise (SSN) that occur in the PDN can affect the quality of the signal that propagates through the SDN. Analyzing the two networks separately fails to account for these effects and hence compromises on the quality of the SI analysis. An illustration of this effect is shown in Figure 4 where the voltage across the load in the SDN of a stub-series terminated logic (SSTL-2) standard interface is simulated in the absence and presence of SSN [24]. SSN is caused due to the non ideal nature of the PDN. The PDN supplies power to the core and I/O drivers on the chip. Since the necessary current cannot be supplied instantaneously, simultaneous switching of transistors causes voltage fluctuations on the power/ground rails. These voltage fluctuations are detrimental to the performance of the electronic system and are termed as

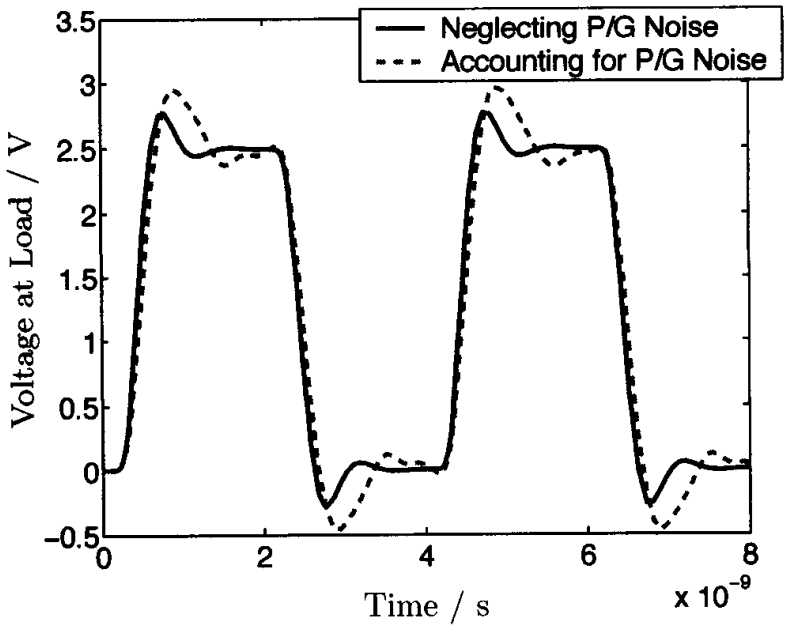

Figure 4: Influence of SSN on the simulation of an SSTL-2 interface

SSN (or power/ground noise). It is evident from Figure 4 that neglecting the effects of SSN gives an optimistic result. In case of the SSTL-2 standard interface, the simulation that neglects SSN would not forecast the excessive overshoot in the voltage, which should not exceed 2.8V. This example underlines the importance of including the effects of SSN in the simulation of the SDN.

The simplest way of co-simulating the SDN and the PDN is by representing the PDN in a SPICE compatible format using the Transmission Line method [40] and then combining it with the SPICE based models of the SDN. However for complex distributed passive systems, the transmission line representation of the PDN results in thousands of elements that becomes very difficult to simulate in SPICE. A popular solution to this problem is the use of macro-modeling, which converts the frequency domain response of a PDN into a comparatively smaller SPICE compatible format that can be combined with the SPICE based SDN models to carry out a system co-simulation [37] in the time domain. A block diagram for this kind of approach to a system level SI-PI analysis is shown in Figure 5. Although this addresses some of the issues concerning the system parasitics, macro-modeling has its own

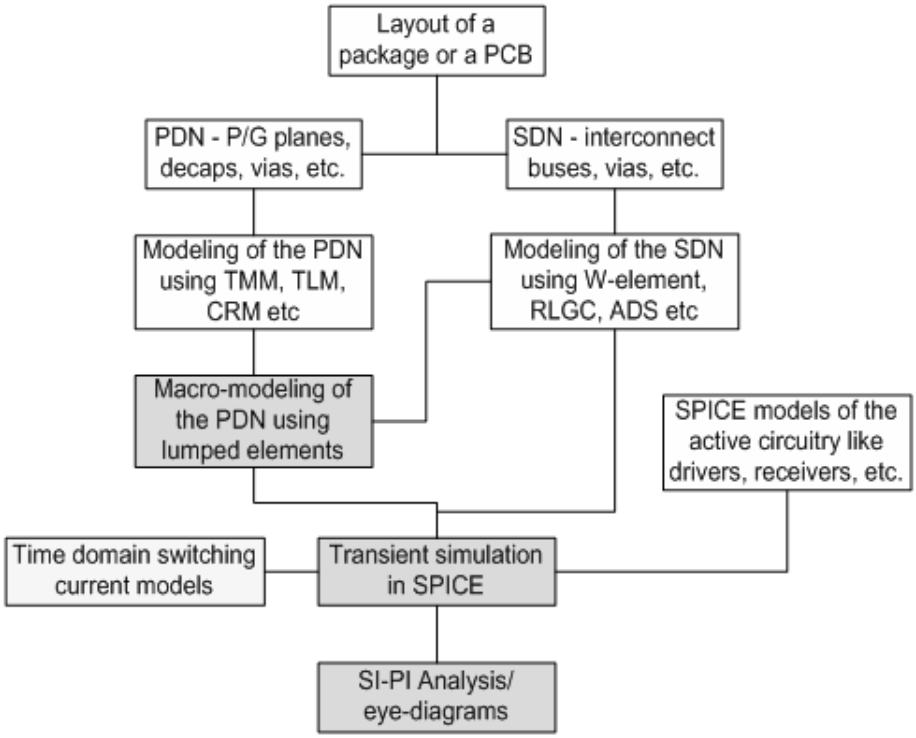

Figure 5: Flow chart for system level SI-PI analysis through macro-modeling

limitations. The accurate simulation of SSN in a system requires the knowledge of the transient switching currents flowing in the PDN of the system. However accurate time-domain models of switching currents do not exist especially for complex digital systems. For small integrated circuits (ICs), a method has been proposed that uses IC parameters like power dissipation capacitance and switching time interval to estimate the switching noise current [34]. Another method that estimates the magnitude of the switching current spectrum based on a frequency domain measurement has been proposed in [33]. A brief description of these methods is given in section 1.2. These methods are inadequate for generating time-domain models of switching currents in complex digital systems. In addition macro-modeling typically requires some function based approximation of the frequency response data which limits the size of the problem (in terms of ports and bandwidth) that can be handled. Also, the macro-models obtained using bandlimited frequency response data are unable to accurately capture distributed effects like delay leading to causality violations in the transient simulations. Furthermore, macro-modeling based SPICE netlists representing the PDN in complex digital systems can still be prohibitively large or inefficient to simulate. Another

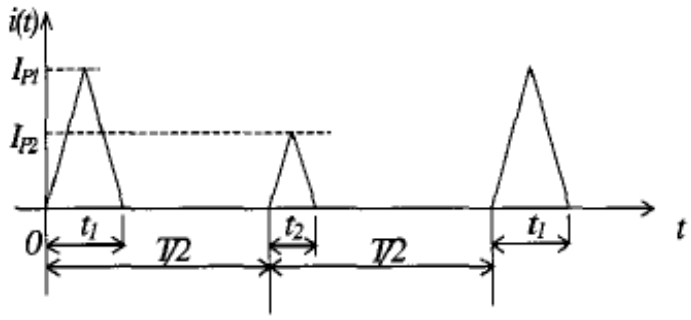

Figure 6: Triangular approximation of transient switching noise current

solution for converting the frequency domain response of a passive network into the time domain is through the direct simulation of S-parameters using signal flow graphs as given in [49]. However this technique too suffers from scalability and causality violation issues. A brief description of the macro-modeling and the signal flow graph techniques along with their limitations is given in section 1.3.

1.2 Extraction of switching noise current

The simulation of SSN in a packaged digital system requires information on the transient switching noise currents that are injected into the PDN. However, little work has been done in the area of switching noise current modeling especially for high speed systems. The existing noise current extraction techniques, which are either theory based [34] or measurement based [33] [52], have limited scalability and provide only the magnitude information of the switching noise current spectrum. This section briefly describes each of these techniques along with their limitations.

1.2.1 Analytical estimation of switching noise current

Analytical estimation of the switching noise current is done by modeling the shoot-through current, the load current, and the power dissipation capacitance in a digital circuit. This method has been successfully demonstrated on the modeling of the switching noise caused by clock buffers [34]. First, the transient current obtained from the power bus is approximated using a triangular source as shown in Figure 6. The current I_{P2} is the portion due to

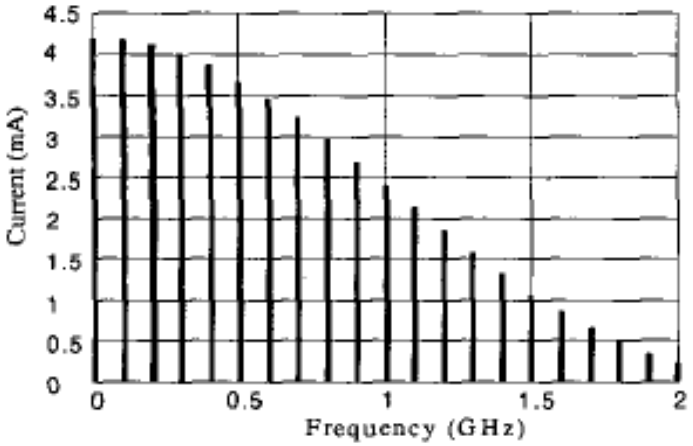

Figure 7: A modelled switching noise current spectrum

the shoot-through current, which can be estimated using the power dissipation capacitance C_{PD}. The current I_{P1} is the sum of I_{P2} and the load current for all I/O drivers. I_{P2} is calculated using the equation

$$I_{P2} = C_{PD} \times m \times V_{CC} \times \Delta t_2 \tag{1}$$

where V_{CC} is the DC power bus voltage, Δt_2 is the switching time of the IC, and m is the number of outputs switching. Calculation of I_{P1} is done using the peak value of the load current I_{PL}, which is obtained using the equation

$$I_{PL} = C_L \times n \times V_{CC} \times \Delta t_1 \tag{2}$$

where V_{CC} is the DC power bus voltage, Δt_1 is the charging time of the load IC, and n is the number of loaded outputs. Once the transient waveform of the current is obtained, its spectrum is calculated using the Fourier Transform. An example of a modelled switching noise current spectrum is shown in Figure 7.

The primary limitation of this technique is its scalability since the parameters required for estimating the switching noise current using equations 1 and 2 are not easily known for large systems. This is due to the fact that at the system level for each clock cycle, there are thousands of circuits switching at different frequencies giving rise to a complex switching noise current waveform.

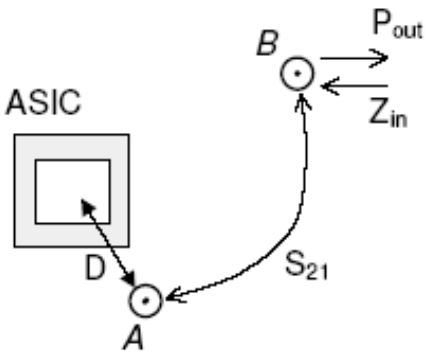

Figure 8: Schematic layout for noise current spectrum determination

1.2.2 Measurement based switching noise current extraction for ASICs

Analytical techniques for estimating the switching noise current cannot be followed for application specific integrated circuits (ASICs) due to their complex circuitry. Since analytical estimation of the switching noise current in ASICs is difficult, a measurement based technique has been proposed for the purpose [33]. The technique defines two ports on the system board as shown in the schematic layout in Figure 8. If D is less than $\lambda/8$, where λ is the wavelength corresponding to the highest frequency, the distributed effects of the power/ground planes are negligible and the port A can be assumed to be located at the center of the ASIC. With this setup, three measurements are required to estimate the switching noise current in the ASIC without knowing its internal circuitry:

1. Power spectrum P_{out} at port B with the board in operation
2. Input impedance Z_{in} at port B with the power supply switched off
3. $|S_{21}|$ between the ports A and B with the power supply switched off

From the measurement results, a two port equivalent circuit model of the system board is generated as shown in Figure 9. Using this model, the switching noise current I_{noise} is determined as given by

$$I_{noise} = \sqrt{\frac{P_{out}}{25\Omega}} \frac{|(Z_{22} + j\omega L_{SMA}) + 50\Omega|}{|Z_{21}|} \tag{3}$$

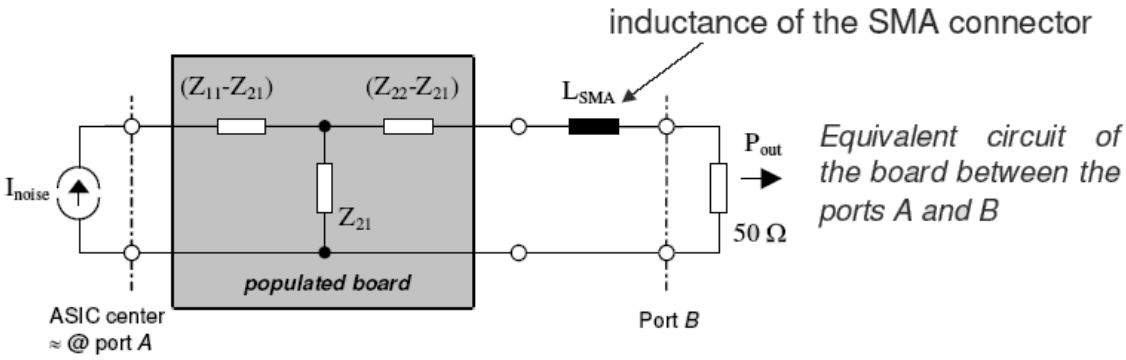

Figure 9: Equivalent circuit model of the ASIC board

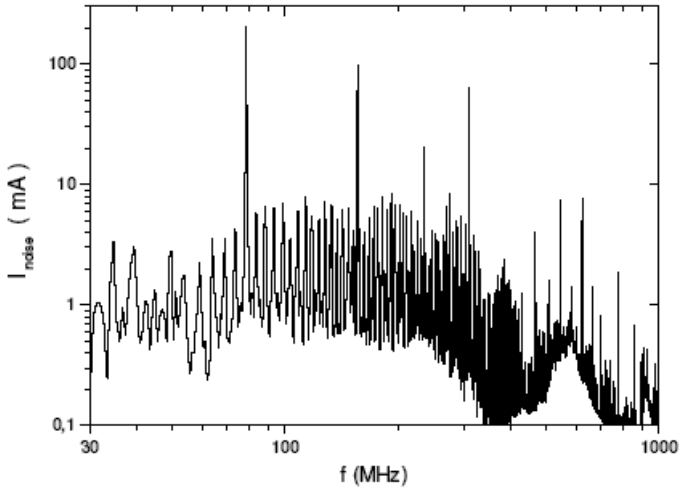

Figure 10: Switching noise current spectrum for an ASIC

where $Z_{22}+j\omega L_{SMA}$ is the input impedance Z_{in} measured at port B, L_{SMA} is the connector inductance, and $|Z_{21}|$ is obtained from $|S_{21}|$ using the relation

$$|Z_{21}|_{dB} \approx |S_{21}|_{dB} + 28dB. \tag{4}$$

An example of the extracted switching noise current spectrum for an ASIC is shown in Figure 10.

The primary limitation of this technique is that it extracts only the magnitude response of the switching noise current spectrum but provides no information on its phase response. Hence, the extracted switching noise current cannot be converted into the time domain to perform a transient SSN simulation. Since most of the SI analysis on the SDN is performed

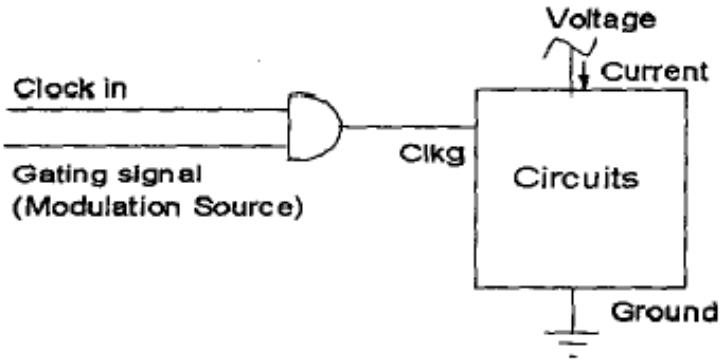

Figure 11: Clock gating mechanism

in the time domain, this is a major drawback.

1.2.3 Switching noise current extraction using clock modulation

The central idea of the clock modulation method for switching noise current extraction is to provide a means for gating the switching activity of electronic circuits [52]. The gating action switches the electronic circuits from a minimal level of activity to a higher level of activity such that the current drawn from the voltage source powering those circuits is changed significantly between the gated and non-gated states. A modulation source is then used to control the gating action such that the current drain from the voltage source is excited with a controlled binary pattern. The clock gating mechanism is shown in Figure 11. As the gating signal is swept through a large frequency range, the AC voltage as a function of frequency is monitored using a spectrum analyzer. Only the AC voltage corresponding to the first harmonic of the gating signal is used. The power of the high and low activity states during the modulation is determined by measuring the DC currents under the two cases. The difference in these DC currents is used to translate the measured AC voltage to impedance of the PDN as a function of frequency. Once the impedance response is obtained, the switching noise current at a particular workload is determined by measuring the PDN voltage for that workload and dividing it by the impedance response obtained earlier. The switching noise current spectrum for an IBM POWER4 chip obtained using this technique is shown in Figure 12 [52]. This technique extracts only the magnitude of the current spectrum and hence has the same drawback as that for the previous technique.

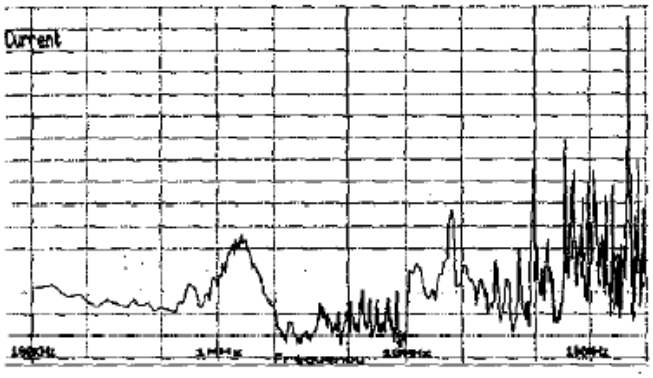

Figure 12: Switching noise current spectrum for IBM POWER4 chip

1.3 Conversion of a PDN response to the time domain

The conversion of the frequency response of a PDN into a time domain compatible format for co-simulation with the SDN has traditionally been done either using macro-modeling [37] or through direct simulation of the scattering parameters [49].

1.3.1 Macro-modeling

Macro-modeling of a passive network involves development of a black-box representation of the network which approximates it's port-to-port behavior [36][7][6][44][10][11][17]. Such a representation is generated by approximating the frequency response of the network using complex poles and residues in the form

$$H(s) = \sum_{n=1}^{N} \frac{r_n}{s - p_n} + k_d + k_l s \tag{5}$$

where p_n are the complex poles, r_n are the complex residues and $s = j\omega$ where ω is the angular frequency. $H(s)$ generated this way is stable if all the poles p_n lie in the left half of the complex s-plane. To ensure passivity of $H(s)$ several methods have been proposed in the literature [37][48][25]. For instance, the one described in [37] rewrites equation 5 using

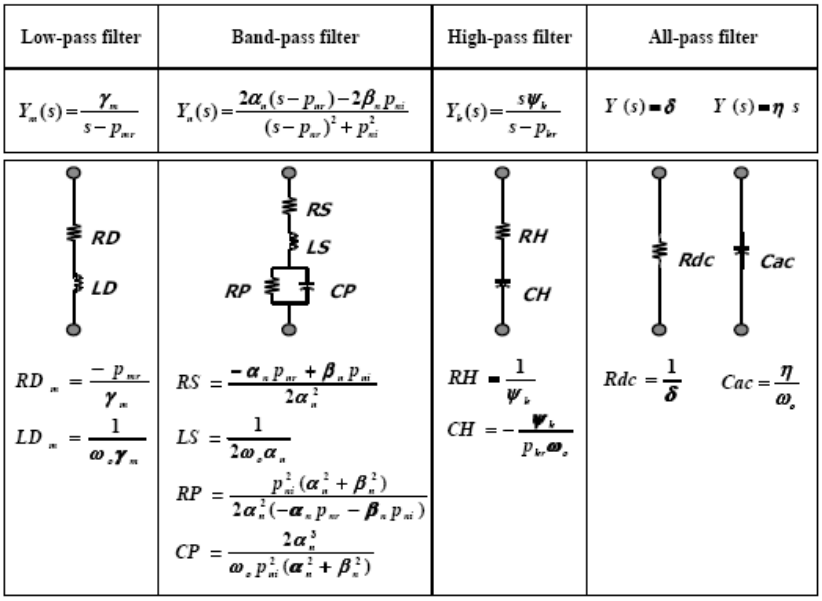

Figure 13: Generation of lumped-element-circuits using rational function approximation

low pass (LPN), band pass (BPN), high pass (HPN), and all pass filters to obtain

$$H(s) = \begin{array}{l} \sum_{m=1}^{LPN} \frac{\gamma_m}{s-p_{mr}} \\ + \sum_{n=1}^{BPN} \frac{2\alpha_n(s-p_{nr})-2\beta_n p_{ni}}{(s-p_{nr})^2+p_{ni}^2} \\ + \sum_{k=1}^{HPN} \frac{\psi_k s}{s-p_{kr}} \\ +\delta + \eta s \end{array} \tag{6}$$

The method then imposes a set of conditions on the residues γ_m, α_n, β_n, ψ_k and δ, to ensure that the developed macro-model is passive. These conditions are given as

$$\begin{aligned} \gamma_m &\geq 0 \\ -\alpha_n p_{nr} \pm \beta_n p_{ni} &\geq 0 \\ \psi_k &\geq 0 \\ \delta &\geq 0 \end{aligned} \tag{7}$$

Once the poles and residues are known, they can be represented in a lumped-element-circuit form as shown in Figure 13, which is SPICE compatible. Macro-models developed using these techniques satisfy stability and passivity, but not causality. Causality is defined as a property of a system by which the future values of the input are not required to determine

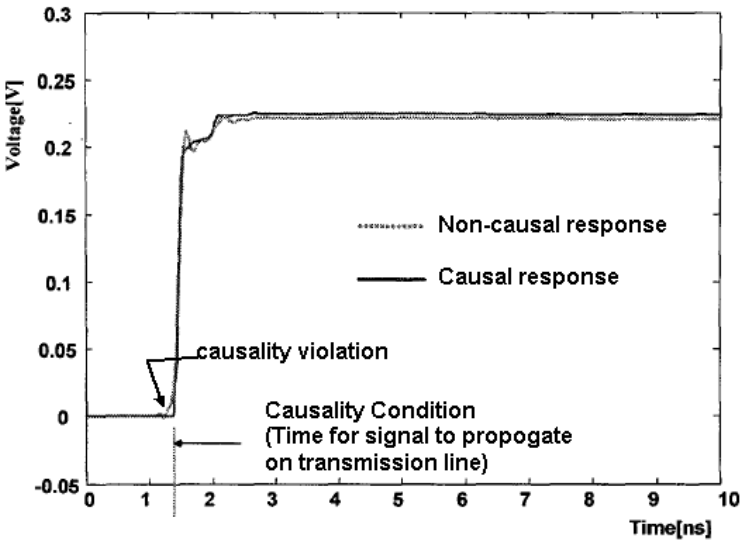

Figure 14: Causality violation in transient simulation using macro-modeling

its output [3]. This property of causality can be characterized in terms of the impulse respose $h(t)$ of a linear time-invariant system as; $h(t) = 0$ for $t < 0$. For multiport linear time-invariant systems, if there exists a certain delay t_d between two ports, then causality states that if one of the ports is excited by a source at time 0, the output at the other port should remain 0 for $t < t_d$.

Distributed passive systems like transmission lines have infinite poles, and equation 5 approximates their response using only bandlimited frequency response data. This prevents $H(s)$ from accurately capturing the delay in the network, since capturing delay using a function in the pole-residue form shown in equation 5 would require an infinite number of poles N along with an infinite bandwidth frequency response. This problem is illustrated in Figure 14 where the technique described in [36] was used to macro-model a transmission line using it's bandlimited frequency response. The transient response obtained using the macro-model was non-causal. Another limitation of these macro-modeling techniques is their scalability. Since the rational function approximation involved in macro-modeling requires large-sized matrix inversion, these methods can be effectively applied only for systems having around 20-30 ports. For larger systems, generating the macro-model takes a prohibitively large amount of time and the accuracy of the macro-model is also compromised.

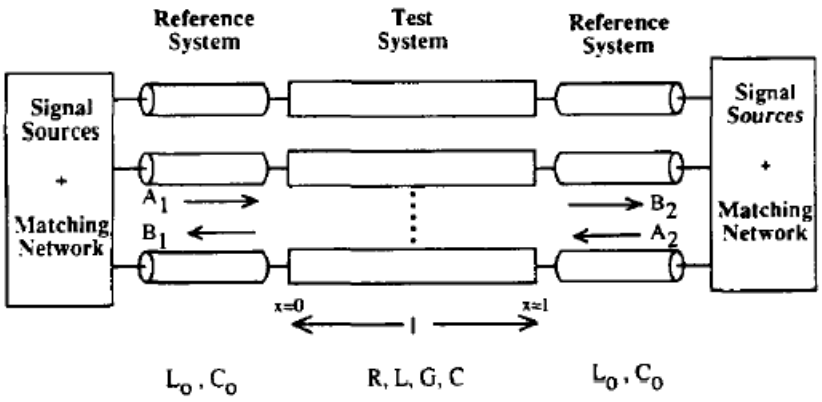

Figure 15: Schematic of network used for the definition of modal S-parameters

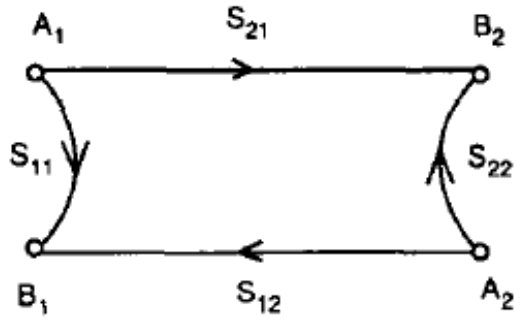

Figure 16: Signal flow graph of a two port S-parameter network

Another drawback of this approach is that the SPICE netlists representing distributed passive structures can be extremely large and hence simulating them in SPICE can be very inefficient.

1.3.2 Direct simulation using S-parameters

Direct simulation methods employ some form of Fourier transformation technique along with convolution to implement transient simulation using network parameter data. A technique of this type is described in [49], where S-parameters have been used to implement transient simulation of coupled transmission lines. The method begins by defining the frequency domain modal S-parameters for a test system as shown in Figure 15. Once the S-parameters are obtained, a signal flow graph of the network topology is setup. A sample signal flow graph for a coupled transmission line network is shown in Figure 16. Such a signal flow

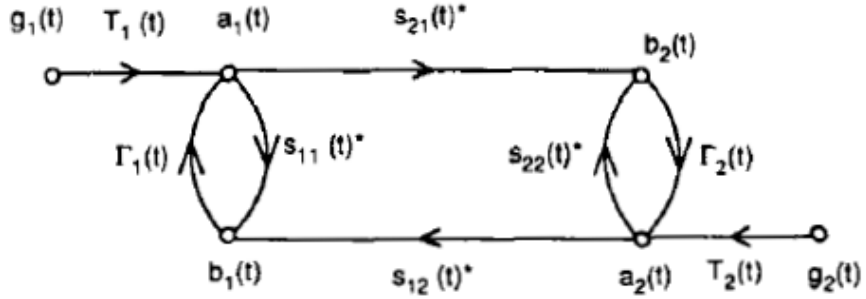

Figure 17: Signal flow graph of coupled transmission lines with nonlinear terminations

graph satisfies the relation

$$\begin{aligned} B_1 &= S_{11}A_1 + S_{12}A_2 \\ B_2 &= S_{21}A_1 + S_{22}A_2 \end{aligned} \tag{8}$$

where S_{11},S_{12},S_{21}, and S_{22} are the frequency domain modal scattering parameters. This relation when transformed to the time domain takes the form

$$\begin{aligned} b_1(t) &= s_{11}(t) * a_1(t) + s_{12}(t) * a_2(t) \\ b_2(t) &= s_{21}(t) * a_1(t) + s_{22}(t) * a_2(t) \end{aligned} \tag{9}$$

The addition of excitation sources and non-linear terminations results in the modification of the signal flow graph (Figure 17) along with the addition of the termination relation

$$\begin{aligned} a_1(t) &= T_1(t)g_1(t) + \Gamma_1(t)b_1(t) \\ a_2(t) &= T_2(t)g_2(t) + \Gamma_2(t)b_2(t) \end{aligned} \tag{10}$$

where $T_1(t)$ and $T_2(t)$ are the time dependant transmission coefficients, and $\Gamma_1(t)$ and $\Gamma_2(t)$ are the time dependant reflection coefficients. The solution of 9 and 10 at each time step gives the required transient simulation result. However, the transient simulation result thus obtained also violates causality. This is primarily due to the fact that the computation of $s_{11}(t)$, $s_{12}(t)$, $s_{21}(t)$, and $s_{22}(t)$ is done using bandlimited frequency response data. In addition, there exists no mechanism to explicitly enforce causality on the transient simulation. Another limitation of this technique is that its application has been limited to transmission lines and coupled interconnects. A literature survey conducted did not yield any reference material on the application of $transformation-convolution$ based techniques

for transient simulation of arbitrary passive structures like power/ground planes, vias, and interconnect networks referenced to non-ideal power/ground planes.

1.4 Proposed research and dissertation outline

The focus of this dissertation is on the development of new modeling and co-simulation techniques that enable an efficient and accurate SI-PI analysis of packaged digital systems resulting in a reduction in their design-cycle time. From section 1.1 two key limitations in the post-layout simulation process can be identified that bottleneck the design-cycle of packaged digital systems:

1. SSN is an important parasitic phenomenon that occurs in the PDN of a system and if left unchecked can be detrimental to the system performance. Hence accurately simulating the SSN generated in a system is important. The simulation of SSN in a system requires a model of passive PDN as well as information of the transient switching currents that are injected into the PDN. Existing techniques for determining the time-domain models of these switching noise currents are inadequate especially for complex digital systems.

2. Parasitic effects like SSN that occur in the PDN of a digital system affect the signal distribution in the SDN of the system. This coupling between the SDN and the PDN needs to be accurately captured in the system simulation. Macro-modeling based techniques enable the co-simulation of the SDN and the PDN by representing the PDN in a SPICE compatible format. However the transient simulation of the macro-modeling based SPICE representation of a PDN is often inefficient, and is plagued by scalability and causality violation issues.

The goal of this dissertation is to effectively address these limitations in the modeling and simulation environment of packaged digital systems using the approach shown in Figure 18. Using this approach, the SDN and the PDN (i.e., the passive modules) in a digital system are simulated using a new transient co-simulation methodology while the non-linear modules of the system (like drivers and receivers) are simulated using SPICE. Since both

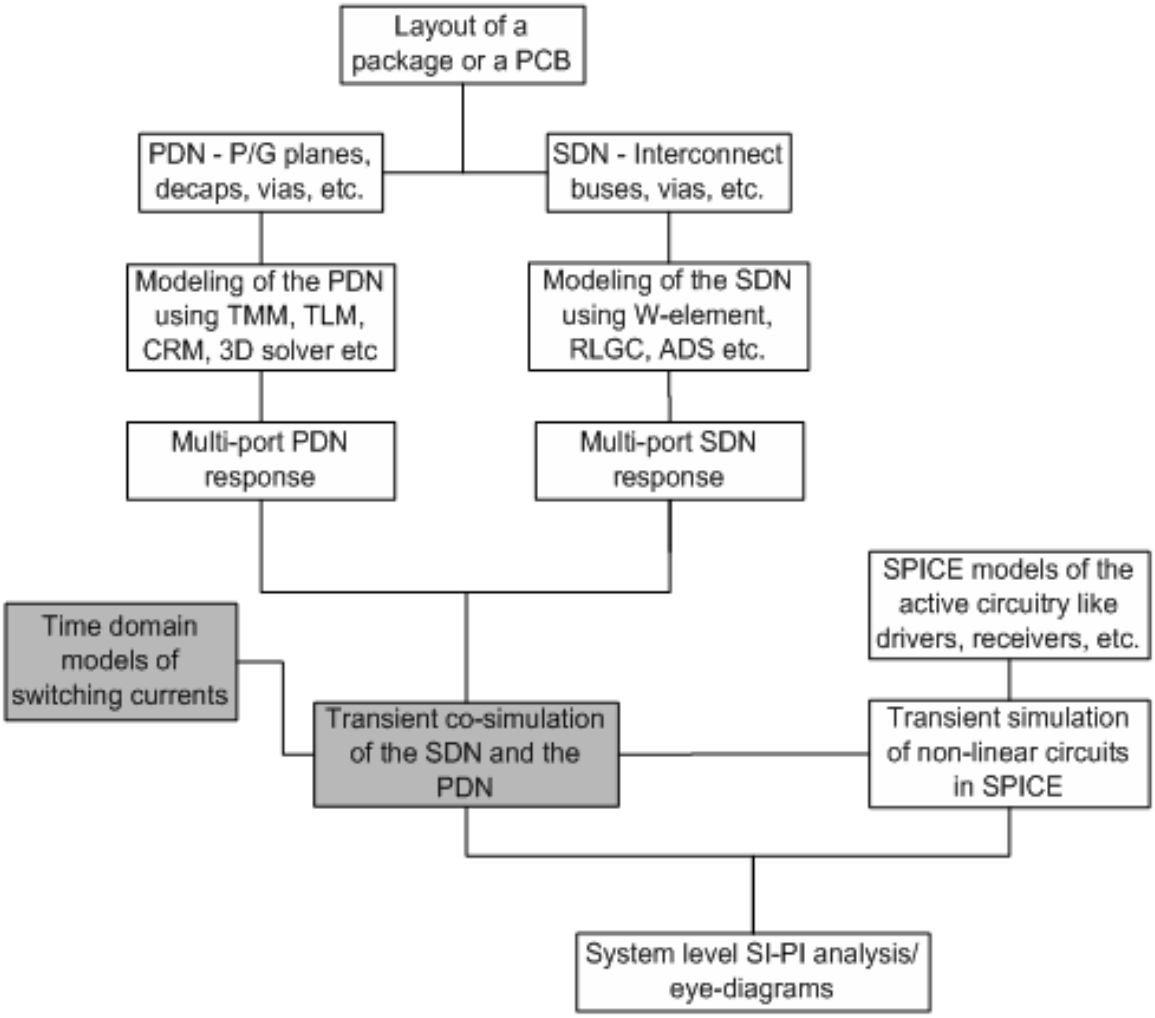

Figure 18: Proposed approach for transient co-simulation

the simulations environments proceed on a time-step basis, they can be interfaced to perform a complete system co-simulation. The proposed transient co-simulation methodology includes a novel delay extraction technique that enables the enforcement of causality on the transient simulation. It also includes an implementation of fast-convolution that increases the efficiency of the transient simulation algorithm. The methodology effectively accounts for all the system parasitics in the simulation and enables an accurate SI-PI analysis at the system level. The dissertation also demonstrates the application of this methodology in simulating a variety of structures including large sized problems. In addition, a new measurement based technique is proposed in this dissertation to accurately extract the transient switching noise currents in high speed digital systems. The extracted switching noise currents enable accurate simulation of SSN in both the frequency domain and the time domain. The development of this switching current extraction technique requires measurements of transient switching noise voltages in the PDN of a system. Since the measurement of such waveforms is plagued with measurement noise, the waveforms need to be de-noised before they are processed. This dissertation describes a wavelet based technique that de-noises measured transient waveforms.

The work accomplished in this dissertation can be listed as follows

1. A wavelet based technique that de-noises a measured time-domain waveform has been proposed. The technique requires an optimal basis representation of the input transient waveform. The discrete wavelet packet transform (DWPT) along with a library of orthogonal wavelet filters have been used for this purpose. The de-noising technique has been successfully demonstrated on simulated and measured transient data.

2. Using the transient waveform de-noising technique, a measurement-based method to extract the switching noise current signatures in packaged digital systems has been developed. The extracted switching noise current signature has magnitude and phase information and can be used to simulate simultaneous switching noise (SSN) in the time and frequency domain. The method has been successfully applied to extract the switching noise currents in the power distribution network of a functioning Sun

Microsystems workstation and in an IBM Power5 microprocessor.

3. A technique that extracts the port-to-port delay directly using multiport frequency domain network parameters has been proposed. The technique accepts multiport S, Y or Z parameters and performs a Hilbert Transform based separation to extract the delays between the various ports. The technique has been validated by comparing the delay extracted for certain test structures to that calculated using their dimensions and material properties. The technique has also been extended for extracting the even and odd mode delays in mixed-mode passive structures.

4. Using the delay extraction technique that has been proposed, a signal flow graph based transient simulation technique that enforces causality has been developed. Transient simulations carried out on a variety of structures using the developed technique have been shown to satisfy the causality criteria.

5. A technique that performs the convolution integration in an efficient way has been implemented in the transient co-simulation methodology. This fast-convolution technique enables a reduction in the computational complexity of the convolution integral from $O(N^2)$ to $O(NlogN)$ where N depends on the problem size.

6. The developed transient simulation technique has been used in integrating the SDN and the PDN of packaged digital systems to perform a transient co-simulation. The simulations assist in analyzing the parasitic noise that can creep into the SDN due to the non-ideal nature of the PDN. This co-simulation methodology has been demonstrated on a variety of passive structures including microstrip interconnects, stripline interconnects, and an IBM ASIC package

7. The developed transient simulation methodology has been used to perform a SDN-PDN co-simulation of a 64-bit interconnect bus. The 64-bit bus referenced to non-ideal power/ground planes resulted in an overall system network consisting of 130 ports, which was simulated effectively using the proposed methodology. Existing macro-modeling techniques are able to handle no more than 25-30 ports.

The remainder of this dissertation is organized as follows. Chapter 2 describes the discrete wavelet packet transform based technique for de-noising and modeling measured transient waveforms. The technique is tested using noisy transient waveform data. Chapter 3 uses the technique developed in Chapter 2 for modeling switching noise current signatures in packaged digital systems. The chapter demonstrates the extraction of switching noise currents in the power distribution network of a functioning Sun Microsystems workstation and in an IBM Power5 microprocessor. Chapter 4 describes the methodology for the co-simulation of the SDN and the PDN in packaged digital systems. The chapter includes a novel delay extraction technique that enables the enforcement of causality on the transient simulation, and a description of a fast-convolution technique that has been implemented for computational efficiency. Chapter 5 describes the application of the proposed transient co-simulation methodology on a variety of test cases. The results obtained from these test cases demonstrate the accuracy, efficiency, and scalability of the proposed methodology. Finally in Chapter 6 the conclusions are presented and some future work is recommended.

CHAPTER II

WAVELET BASED DE-NOISING AND MODELING OF TRANSIENT WAVEFORMS

A major problem encountered in the design of complex digital systems is the accurate estimation of simultaneous switching noise (SSN). SSN is caused due to the non ideal nature of the power distribution network (PDN). The PDN supplies power to the core and I/O drivers on the chip. Since the necessary current cannot be supplied instantaneously, simultaneous switching of transistors causes voltage fluctuations on the power/ground rails. These voltage fluctuations are detrimental to the performance of the electronic system and are termed as SSN. If left unchecked SSN can lead to unwanted effects like ground bounce, excessive clock skew, flase triggering of gates, and coupling in mixed signal systems. Hence while designing or analyzing the PDN in a digital system, the SSN needs to be simulated accurately. This requires a model of the passive PDN as well as the transient currents that are injected into the PDN at each clock cycle. Since such transient currents in high speed digital systems are too complex to be determined analytically, several measurement based techniques have been proposed for this purpose [33] [52]. However these techniques rely on the frequency domain measurents of the voltage waveforms done using a spectrum analyzer (SA). Since a spectrum analyzer provides only magnitude information but no phase and it also has a high noise floor, the extracted switching noise currents are in the form of a magnitude spectrum. This information cannot be converted into the time domain to carry out a transient simulation of SSN (that is often required). The extraction of the phase information from the magnitude spectrum is possible for linear time-invariant systems using the Hilbert Transform [43]. However since in complex digital systems the system impedance characteristics are sometimes nonlinear, it is not always possible to know whether one can apply the Hilbert Transform to extract phase from the magnitude. Even if the system impedance is assumed to be linear, another problem with the Hilbert Transform approach

is that the SA magnitude spectrum measurement has a high noise floor. As will be seen later in the chapter, this introduces considerable error in the phase computation.

A possible solution to this problem is using time domain measurements of the SSN done using a digital sampling oscilloscope (DSO). Since the DSO measurements provide both magnitude and phase, a DSO measurement can be easily used to verify if the impedance characteristics of the system are linear. However it is seen that DSO measurements are plagued with considerable measurement noise. Hence to make any kind of effective use of the DSO measurements, they need to be de-noised first. Since the SA measurements have only magnitude information they cannot be effectively de-noised. This chapter describes a wavelet based technique that de-noises and models measured transient waveforms. A flow diagram of the proposed de-noising and modeling technique is shown in Figure 19. The technique begins with the time domain measurement of the transient waveforms using a DSO. These measured waveforms are run through a set of wavelet filters to obtain an optimum wavelet representation. This optimal representation is used to estimate the level of noise in the measurement. Once this estimation is complete, a suitable thresholding method is applied on the wavelet representation to de-noise the signal. This de-noised signal is then modelled in terms of its dominant singularities using the generalized pencil-of-function method. Section 2.1 provides a brief introduction on the periodized discrete wavelet packet transform (DWPT) that is used in the proposed technique and proceeds to describe the process for selection of an optimal wavelet basis for a particular transient data. Section 2.2 explains the nonparametric regression (NR) technique that forms the core of the de-noising procedure. Section 2.3 describes the generalized pencil-of-function technique that models transient waveforms based on their singularities. Finally Section 2.4 describes the application of the proposed de-noising technique and analyzes its performance in de-noising transient data.

2.1 Discrete wavelet packet transform

Wavelet packets can be described as superposition or a linear combination of wavelets. They retain most of the orthogonality, smoothness and localization properties of their parent

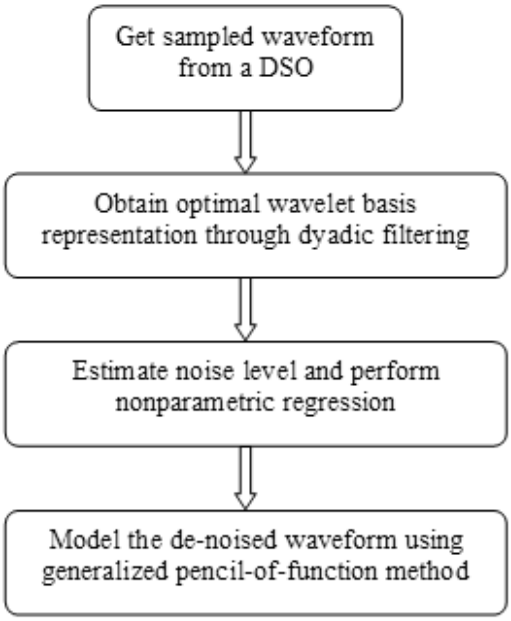

Figure 19: Steps involved in de-noising and modeling of transient signals

wavelets. The discrete wavelet packet transform (DWPT) is computed through a very efficient recursive algorithm and provides enhanced time localization at low frequencies and better frequency resolution at high frequencies as compared to the discrete wavelet transform (DWT). Consider the following set of equations [53]

$$\psi_0 \equiv H\psi_0; \quad \int_R \psi_0(t)dt = 1 \tag{11}$$

$$\psi_{2n} \equiv H\psi_n; \quad \psi_{2n}(t) = \sqrt{2}\sum_{j\in Z} h(j)\psi_n(2t-j) \tag{12}$$

$$\psi_{2n+1} \equiv G\psi_n; \quad \psi_{2n+1}(t) = \sqrt{2}\sum_{j\in Z} g(j)\psi_n(2t-j) \tag{13}$$

Here ψ_0 is the basic scaling function and ψ_1 (when $n = 0$) is the mother wavelet associated with H and G. H and G are conjugate quadrature filters from an orthogonal set or in other words orthogonal wavelet filters such that

$$\sum_j h(j) = \sqrt{2} \tag{14}$$

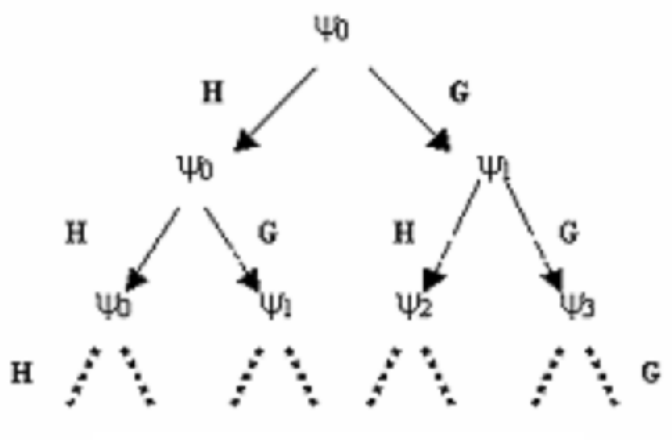

Figure 20: Fixed scale wavelet packets

$$\sum_j h(2j) = \sum_j h(2j+1) \tag{15}$$

$$\sum_j h(j)h(j-2k) = \delta(k) \tag{16}$$

$$g(j) = (-1)^j h(N-j) \tag{17}$$

Equation 14 is the weak condition for a scaling function, Equation 15 is the fundamental condition, Equation 16 gives the required condition for orthogonality, and Equation 17 generates the wavelet dilation coefficients from the scaling function dilation coefficients.

The set of functions ψ_n from Equations 12 and 13 form the wavelet packets associated with H and G. The recursive nature of the formulae leads to the formation of a binary tree as shown in Figure 20. All the ψ_n on any single horizontal level put together, form a fixed scale wavelet packet basis for R such that any signal x(t) can be represented as

$$x(t) = \sum_{s,f,p} c_{sfp}\psi_{sfp}(t) \tag{18}$$

From all such orthogonal basis sets, each wavelet packet can be uniquely identified by a set of 3 indices: the scale index s, the frequency index f and the position index p such that

$$\psi_{sfp}(t) \equiv 2^{-s/2}\psi_f(2^{-s}t - p) \tag{19}$$

Figure 21 shows the spf values for the DWPT coefficients of a sampled sequence x[n] of length 8 at 4 different scales. It is seen from the figure that the scale 1 DWPT representation

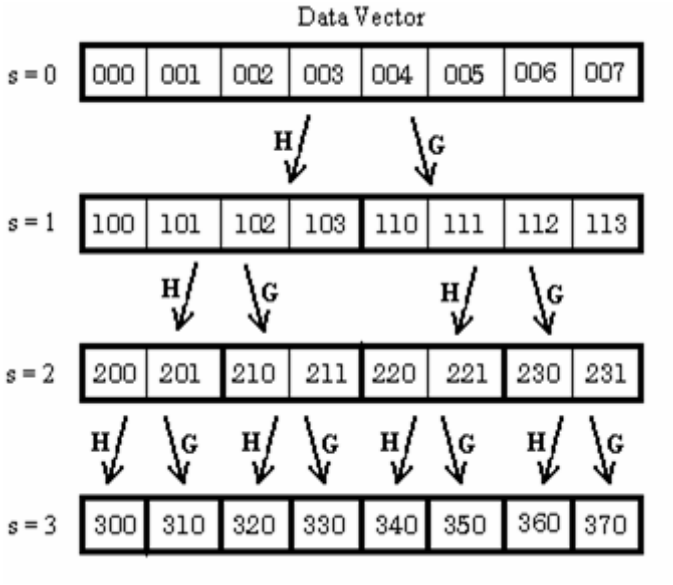

Figure 21: DWPT representation of a data vector at 4 different scales along with the sfp values of each packet wavelet coefficient

of a data vector is obtained by simply convolving the vector with the H and G wavelet filters and retaining alternate samples from the convolution results. Thus, the output of each convolution is a vector half the size of the original vector. Concatenating the two results gives the scale 1 DWPT representation. To obtain the scale 2 DWPT representation, the H and G filters are applied on each of the sections of the scale 1 representation. This process is called recursive dyadic filtering. Thus, given a sampled data signal and a library of orthogonal wavelet filters (H's and G's), dyadic filtering can be recursively applied to the data to compute its DWPT representations for various scales and wavelet filters.

2.1.1 Optimal basis selection

Given the multiple representations of the data signal obtained as explained above, the focus now shifts on picking the optimum DWPT representation of the signal that would aid in de-noising the signal in the best possible way. This necessitates the need for defining some form of a cost function to compare the various representations of the data signal. The entropy of a sequence x[n] is defined as

$$H(x) = \sum_n p(n) \log \frac{1}{p(n)} \tag{20}$$

where, $p(n) = |x(n)|^2/||x||^2$ is the normalized energy of the n^{th} sample of the sequence and $plog(1/p) = 0$ if $p = 0$ [19]. $H(x)$ can then be viewed as the entropy of the energy distribution function given by p. Based on this entropy, we define the cost function as the theoretical dimension of the sequence given by

$$\dim = \exp\left(\sum_n p(n) \log \frac{1}{p(n)}\right) \tag{21}$$

By this definition of the theoretical dimension of a sequence, it can be easily inferred that if x[n] is a N point sequence then its theoretical dimension will range between 1 and N. The former is obtained when the signal has all its energy concentrated in a single sample such that $p(n) = 1$ for $n = i$; $p(n) = 0$ for $n \neq i$ while the latter is seen when the signal energy is equally distributed over all its samples such that $p(1) = p(2) = ... = p(N) = 1/N$

An important observation is that no matter which orthogonal basis set is used to represent white Gaussian noise in the wavelet domain, the theoretical dimension of the representation will always tend to N or its entropy will always tend to log(N). As against this the wavelet representation of a deterministic signal depending upon the basis set chosen will have a relatively lesser dimension. Now, if the noise present in a signal is assumed to be uncorrelated to the signal, the energy distributions of the noise and the signal will also be uncorrelated. Hence the theoretical dimension of the composite noisy signal will be determined by its noise-free component. Therefore the optimal basis for representation of such a noisy signal should be the same as that for the underlying noise-free component. If the optimal DWPT representation is chosen as the one with the least theoretical dimension, in such a representation, bulk of the signal information will be concentrated over fewer samples as compared to the original data. The remaining samples which consist mostly of the noise present in the measurement can subsequently be used to estimate the noise level and de-noise the signal. The nonparametric regression technique described in the next section exploits this property of the DWPT representations to carry out de-noising of the measured data.

2.2 Noise estimation and thresholding

Nonparametric regression (NR) has been a fundamental tool in recovering an unknown function using sampled data that has been corrupted by additive noise. NR has also been seen to work in tandem with parametric regression models such that a NR estimate will suggest a relatively simpler parametric model.

Using the optimal basis representation of the transient data as explained in the previous subsection, carrying out NR requires the level of noise present in the measurement to be estimated. A robust noise level estimation technique developed by Donoho and Johnstone is suggested in [22]. This technique is based on Median Absolute Deviation and assumes that the wavelet coefficients in a wavelet transform at the finest resolution comprise mostly of noise. Under this assumption, the standard deviation σ of the noise in the data is given by

$$\sigma = \frac{median(|d_k|)}{0.6745} \tag{22}$$

where d_k are the wavelet coefficients at the finest resolution. Prior to applying this formula in the proposed technique, it should be noted that this formula has been defined for the conventional wavelet transform. Since this work uses the DWPT, the location of the high resolution coefficients has to be carefully decided before applying the formula. As will be seen later, this decision can be made once the optimal basis representation of the noisy signal is obtained. The noise level in the measured data estimated using Equation 22 is then used by wavelet thresholding or wavelet shrinkage estimators to de-noise the signal. These estimators carry out a term-by-term analysis of the DWPT such that if a coefficient is sufficiently large in magnitude as compared to a predetermined threshold, it is appropriately shrunk or retained; otherwise it is neglected. However since thresholding is essentially a nonlinear process, a simple "shrink or kill" (soft thresholding) or "keep or kill" (hard thresholding) often results in excessive bias and unnecessary oscillations in the output [21] [9]. Since the output is to be used for capturing the singularities in the signal, such errors compromise on the accuracy of the generated model. Making a tradeoff between complexity and model accuracy, the Smoothly Clipped Absolute Deviation (SCAD) thresholding

Table 1: λ_n for various thresholding techniques and data lengths

n	128	256	512	1028
Hard	2.913	3.117	3.312	3.497
Soft	1.669	1.859	2.045	2.226
SCAD	1.691	1.881	2.061	2.241

method has been used in this work. This method does not over penalize large wavelet coefficients and hence avoids excessive bias. The thresholding for SCAD is given by

$$\delta_{\lambda}^{SCAD}(d) = \begin{cases} sign(d)\max(0,|d|-\lambda) & if \quad |d| \leq 2\lambda \\ \frac{(\alpha-1)d-\alpha\lambda sign(d)}{\alpha-2} & if \quad 2\lambda \leq |d| \leq \alpha\lambda \\ d & if \quad |d| \geq \alpha\lambda \end{cases} \tag{23}$$

where λ is the threshold value determined by the noise content, d is the DWPT coefficient and α is a constant with value 3.7. The threshold λ used in this study is the Minimax Threshold and is defined as $\lambda = \sigma\lambda_n$, where σ is the noise deviation as estimated previously and λ_n depends on the thresholding technique and the data length n as given in Table 1. For SCAD thresholding with a data length of 512, λ_n is estimated to be around 2 [9].

2.3 Modeling using generalized pencil-of-function method

An important area of interest in the system modeling domain is the extraction of the complex poles and residues from the time-domain response of a system. System representation and modeling using these extracted singularities (complex poles and residue) is handy not only from the point of view of incorporating the system into larger simulations but also that these parameters contain physical information about the system. Several methods along with improvisations have been developed in the past that have targeted this problem [45] [12] [27]. The Generalized Pencil-Of-Function (GPOF) method [26] was developed as a computationally efficient procedure of extracting the poles of a system by solving a generalized eigenvalue problem instead of the conventional two-step process used by techniques like the Prony method. It was also observed that the GPOF method was more robust in

the presence of additive noise in the system response data. A brief description of the GPOF method can be given as follows.

Consider a system with $\mathbf{M}$ complex poles and residues composing its response y_k. Hence

$$y_k = \sum_{i=1,M} b_i \exp(z_i \delta t k) \qquad k = 1...\mathbf{N}-1 \tag{24}$$

where b_i are the complex residues and z_i are the complex poles of the system. The GPOF method forms the 'information vectors' $\boldsymbol{y_0, y_1, ..., y_L}$ based on the response where $\boldsymbol{y_i} = [y_i, y_{i+1}, y_{i+2}, ..., y_{i+N-L-1}]^T$ where $\mathbf{L}$ is chose arbitrarily. From these vectors, the matrices $\mathbf{Y_1}$ and $\mathbf{Y_2}$ are constructed where

$$\mathbf{Y}_1 = [\mathbf{y_0}, \mathbf{y_1}, ..., \mathbf{y_{L-1}}] \tag{25}$$

$$\mathbf{Y}_2 = [\mathbf{y_1}, \mathbf{y_2}, ..., \mathbf{y_L}] \tag{26}$$

The method states that if $\mathbf{M} \leq \mathbf{L} \leq \mathbf{N} - \mathbf{M}$ the poles of the system $\{z_i : i = 1...\mathbf{M}\}$ are the generalized eigenvalues of the matrix pencil $\mathbf{Y_2}$ - $z\mathbf{Y_1}$. Consider the pseudo inverse $\mathbf{Y_1^+}$ as computed through the singular value decomposition (SVD) of $\mathbf{Y_1}$ as follows

$$\begin{aligned} \mathbf{Y}_1 &= \sum_{i=1...\mathbf{M}} \sigma_i \mathbf{u}_i \mathbf{v}_I^H \\ &= UDV^H \end{aligned} \tag{27}$$

$$\mathbf{Y}_1^+ = VD^{-1}U^H \tag{28}$$

where $U = [\mathbf{u_1}, \mathbf{u_2}, ..., \mathbf{u_M}]$, $V = [\mathbf{v_1}, \mathbf{v_2}, ..., \mathbf{v_M}]$ and $D = diag([\sigma_1, \sigma_2, ..., \sigma_M])$. Using the above decomposition it can be shown that the eigenvalues of the matrix pencil $\mathbf{Y_2}$ - $z\mathbf{Y_1}$ are the eigenvalues of a $\mathbf{MxM}$ matrix $\mathbf{Z}$ where

$$\mathbf{Z} = D^{-1}U^H Y_2 V \tag{29}$$

It is seen that in the noiseless case, the number of poles $\mathbf{M}$ can be estimated form the singular values $\{\sigma_1 \geq \sigma_2 \geq ... \geq \sigma_M \geq ... \geq \sigma_{min(N-L,L)}\}$, since $\sigma_{M+1} = ... = \sigma_{min(N-L,L)} = 0$. For noisy y_k however the $\mathbf{M}$ most largest singular values of $\mathbf{Y_1}$ are chosen. The singular values provide the ability to reduce the model order at the cost of losing a little bit of accuracy. The

Table 2: List of complex pole pairs used in the simulation test case

Real part	Imaginary part
-0.082	±0.926
-0.147	±2.874
-0.188	±4.835
-0.220	±6.800
-0.247	±8.767
-0.270	±10.733

larger singular values form the more dominant components of system response. Depending on the level of accuracy that is desired, the number of dominant singular values that are included in a model can be adjusted suitably. Once the poles of the system are known, the residues can be computed from Equation 24 using a suitable least squares formulation.

2.4 Test results

This section demonstrates the application of the proposed de-noising technique on simulated and measured noisy transient data.

2.4.1 Simulation test case

To demonstrate the advantage achieved by using the proposed de-noising and modeling technique, a simulation test case [12] was created where a transient response consisting of 6 pole pairs (listed in Table 2) was generated. The residue accompanying each of the poles is taken to be unity. The waveform obtained, 512 samples in length, is shown in Figure 22. To test the proposed de-noising technique, white Gaussian noise of increasing standard deviation (from 0.01 to 0.35) was added to the simulated transient response. For each of the noisy responses the dominant poles of the system were extracted first using the GPOF method on the noisy data (referred to as ND and plotted using '$*$') and then using it on the NR estimate (plotted using '$\diamond$'). The extracted poles for 6 different cases, plotted in the negative S plane, are shown in Figures 23 to 28. The true poles of the system are plotted using a '$\circ$'.The figures clearly demonstrate that the NR estimate provides significant improvement in terms of accuracy in extracting the poles from the noisy data. Since the noise variance in the measured waveform is required for the process of thresholding but is

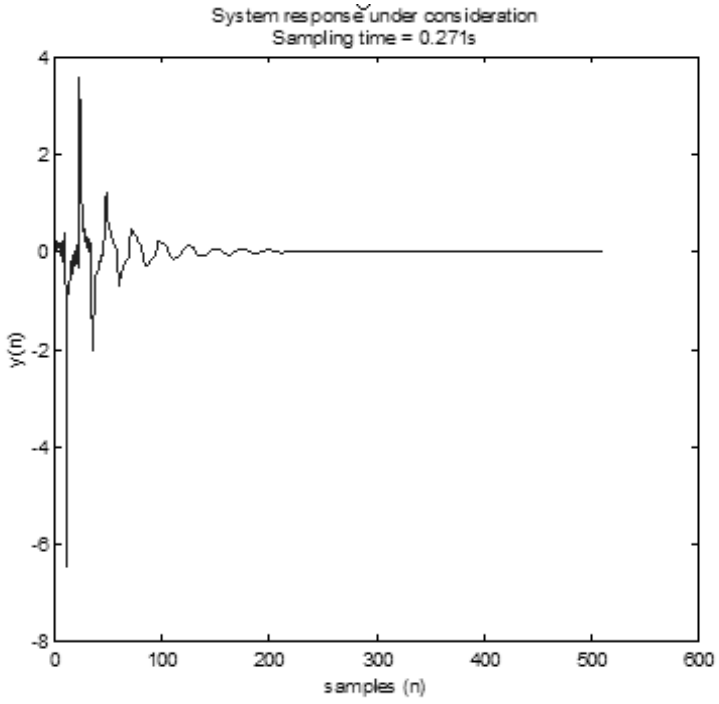

Figure 22: Transient response obtained using pole pairs from Table 2

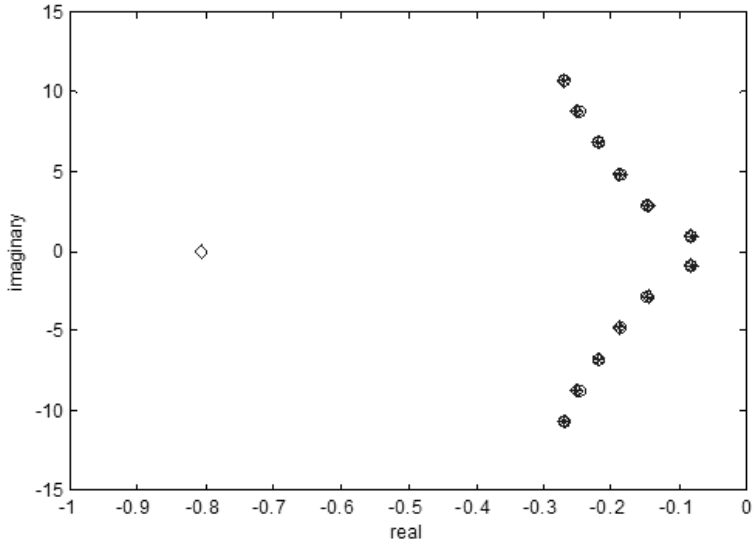

Figure 23: S-plane plots of the extracted poles for $\sigma = 0.01$

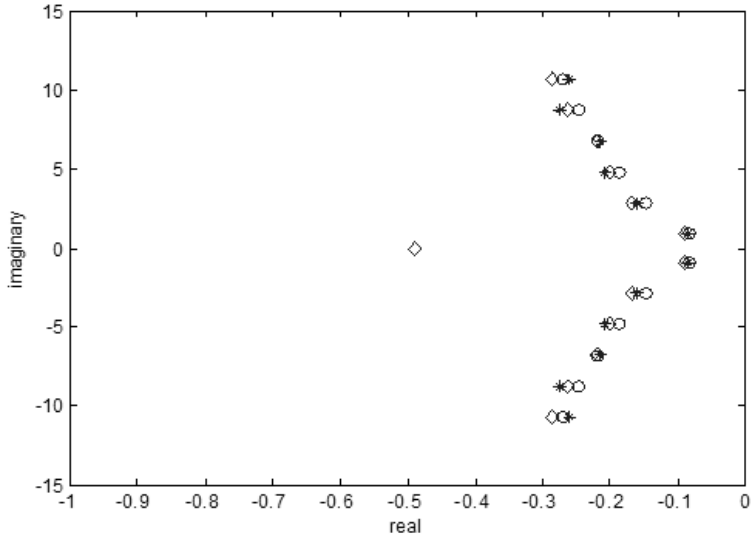

Figure 24: S-plane plots of the extracted poles for $\sigma = 0.1$

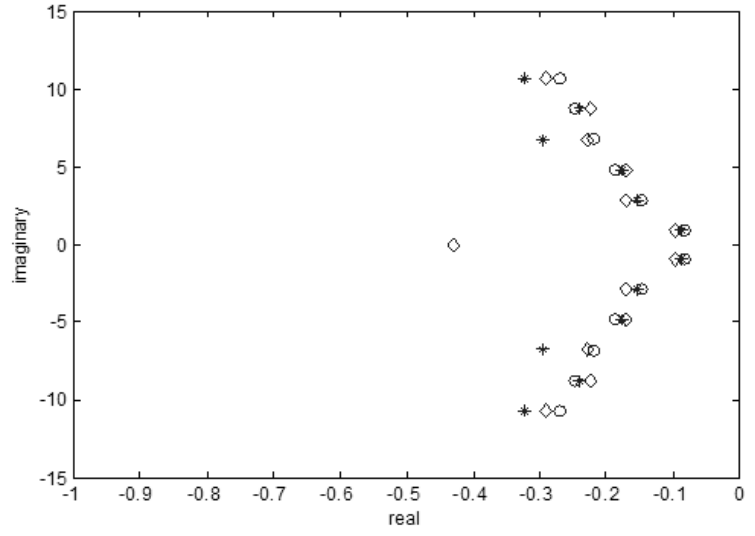

Figure 25: S-plane plots of the extracted poles for $\sigma = 0.15$

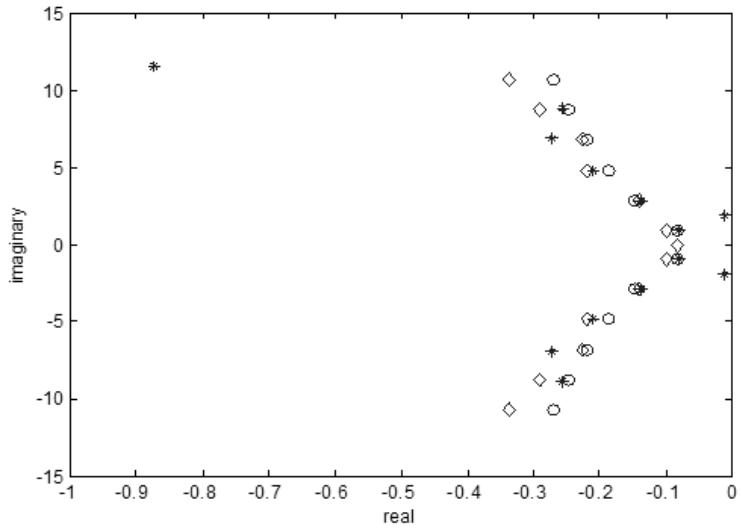

Figure 26: S-plane plots of the extracted poles for $\sigma = 0.2$

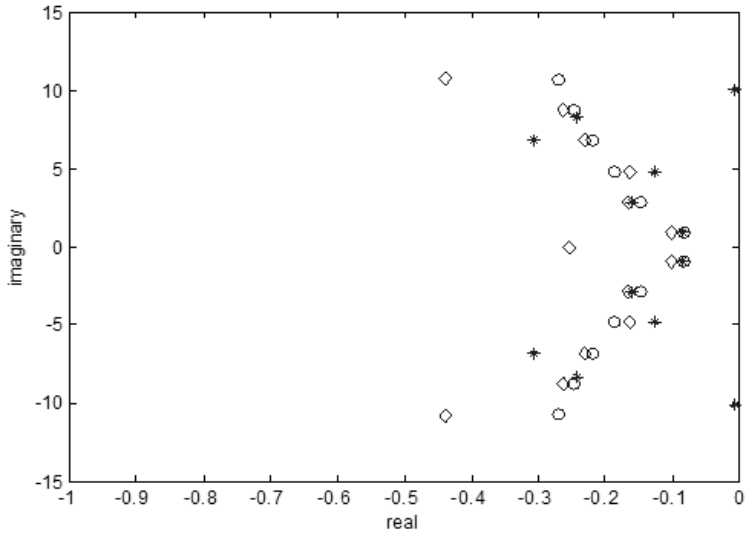

Figure 27: S-plane plots of the extracted poles for $\sigma = 0.25$

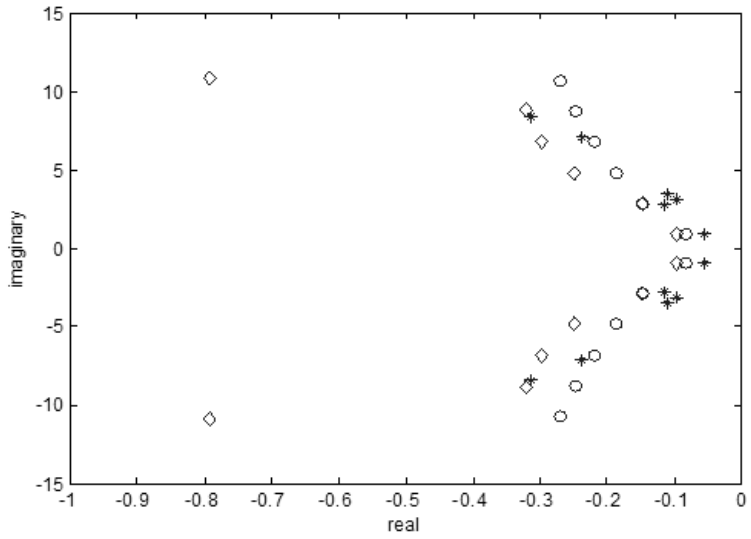

Figure 28: S-plane plots of the extracted poles for $\sigma = 0.3$

Table 3: De-noising results using the proposed technique

σ	Estimated σ	Optimal basis	SNR (dB)	%error (real part) ND	%error (real part) NR	%error (imag part) ND	%error (imag part) NR
0.01	0.0146	DB1	31.67	0.01	0.01	0.02	0.01
0.1	0.0914	DB1	12.05	0.35	1.1	0.21	0.1
0.15	0.1559	DB1	8.27	0.56	0.59	0.24	0.43
0.2	0.213	DB1	5.847	0.87	1.01	8.5	0.98
0.25	0.2632	DB1	4.06	3.2	2.6	8.8	0.63
0.3	0.336	DB1	1.30	3	2.37	34.9	0.18

often unknown in real world measurements, the noise variance in each of the above 6 cases was determined using Equation 22 and compared with the true noise variance. The results are tabulated in Table 3. The percentage error in extracting the real and the imaginary parts of the resonances is defined as given in [12] by

$$\%error(real) = \frac{R|S_T - S_E|}{\sqrt{S_T^2}} \tag{30}$$

$$\%error(imag) = \frac{I|S_T - S_E|}{\sqrt{S_T^2}} \tag{31}$$

where S_T is the true pole and S_E is the estimated pole. From Table 3 it can be seen that as the noise level increases, a pole-residue modeling technique finds it increasingly difficult

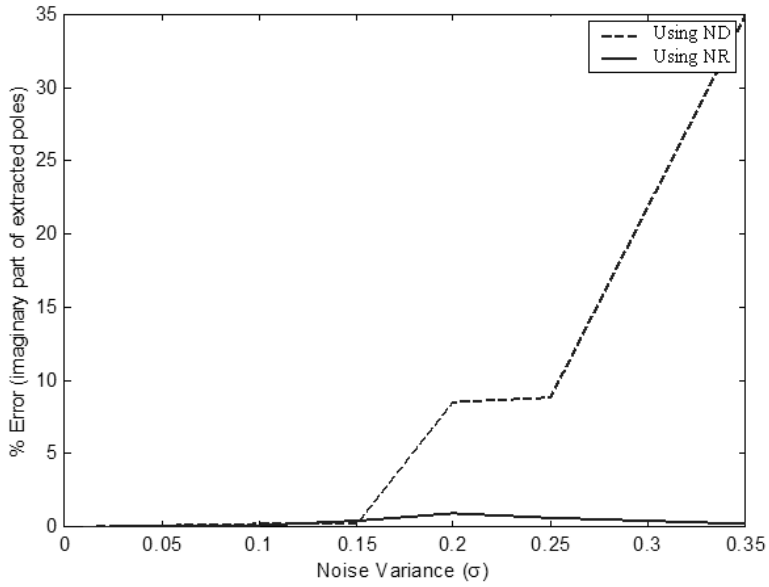

Figure 29: Comparison of % error in the imaginary part of extracted poles

to capture the true poles of the system. As compared to this, if the NR estimate is used in extracting the resonances in the measured waveform, the error obtained in the process is considerably lower. Figure 29 shows the comparison between the two cases in terms of the error in the accurate location of the signal resonances. It can be seen that as the noise variance increases, the error in the imaginary part of the recovered poles increases drastically for the ND case. In comparison, the NR estimate provides excellent results. Finally, it is interesting to note that the best basis returned by the de-noising algorithm for each noisy observation matched perfectly with that for the underlying noise free signal. The signal was best represented by the Daubechies 1 wavelet filter at a fixed scale of 1.

2.4.2 Measurement test case

Time domain measurements of transient waveforms performed using a DSO are plagued by measurement noise. To demonstrate this effect, the SSN voltage waveform on the PDN of a functioning Sun Microsystems computer system was measured using a spectrum analyzer and a sampling oscilloscope. The PDN circuitry on the computer system included two 750MHz microprocessors, a heat sink, and a pair of vdd/gnd planes with 195 decoupling capacitors. A more detailed description of the system is given in the Chapter 3. The signal

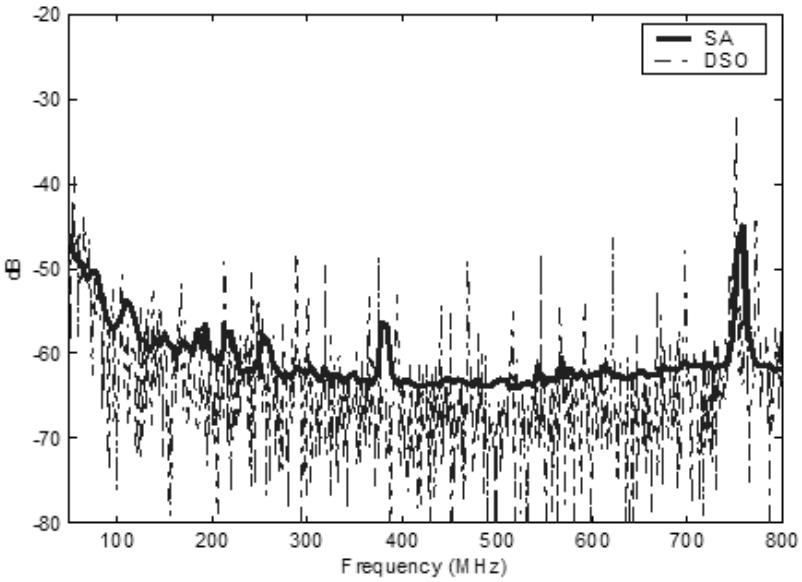

Figure 30: Comparison of the time and frequency domain measurements of the SSN voltage waveform

was measured on the PDN right underneath the microprocessor. To compare the characteristics of the two measurements the DSO measurement was converted to the frequency domain using the FFT algorithm and was plotted alongside the SA measurement. Figure 30 shows the two measurements in the frequency domain. It is seen from the figure that the DSO measurement has a high noise floor and is plagued by spurious noise spikes as compared to the SA measurement. This is due the noise present in the DSO measurement equipment. To make any effective use of the measurement, this noise will first have to be removed. The technique described in this chapter was applied on this measurement to de-noise the SSN voltage transient waveform. The wavelet filter library used for this study included the Daubechies wavelet family from DB-4 to DB-9. To obtain the best basis representation for the measured data, the various wavelet filters were sequentially used to filter the data at scales ranging from 1 to 4, and the theoretical dimensions of the resulting wavelet representations were compared. The best basis representation for the measured SSN voltage was obtained using the DB-4 wavelet filter at a scale of 4. This wavelet representation, shown in Figure 31, has a theoretical dimension of 225.5 as compared to the theoretical dimension of the measured data which is 1326. The next step involved is the

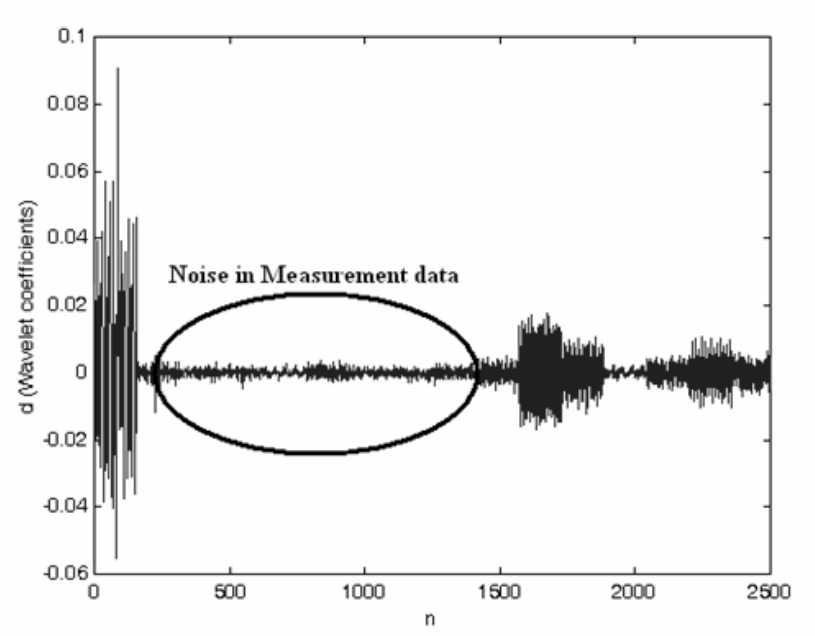

Figure 31: Optimal DWPT representation of the measured SSN voltage waveform

estimation of the noise variance using the Donoho-Johnstone formula. From Figure 31, it is noted that the wavelet transform coefficients over the finest resolution (n = 2350 to 2500) contain signal information and would be inappropriate for use in the noise estimation formula. However, since the measurement noise is assumed to be additive Gaussian white noise, its contribution to the wavelet coefficients would be constant over the entire range of the transform (n = 1 to 2500). Hence, it is proposed that the wavelet coefficients over the range n = 300 to 1400 (Figure 31) be used in Equation 22. This approach estimates the standard deviation σ of the noise in the measured data to be 9.869e-04. This variance was then used to perform SCAD thresholding on the wavelet transform. The resulting transform was then converted back to the time domain to give the NR estimate of the measured SSN waveform. The comparison of the DSO measurement with the de-noised NR estimate is shown in Figure 32. Since, as will be seen in the next chapter, this de-noised signal is used to extract mid-frequency switching currents (200-800MHz) in the PDN of the Sun workstation, it was bandlimited over that mid-frequency range. This bandlimited NR estimate was then modelled using GPOF to capture the dominant resonances in the signal. Figure 33 shows the singular value decomposition of the NR estimate of the measured SSN voltage. The 400

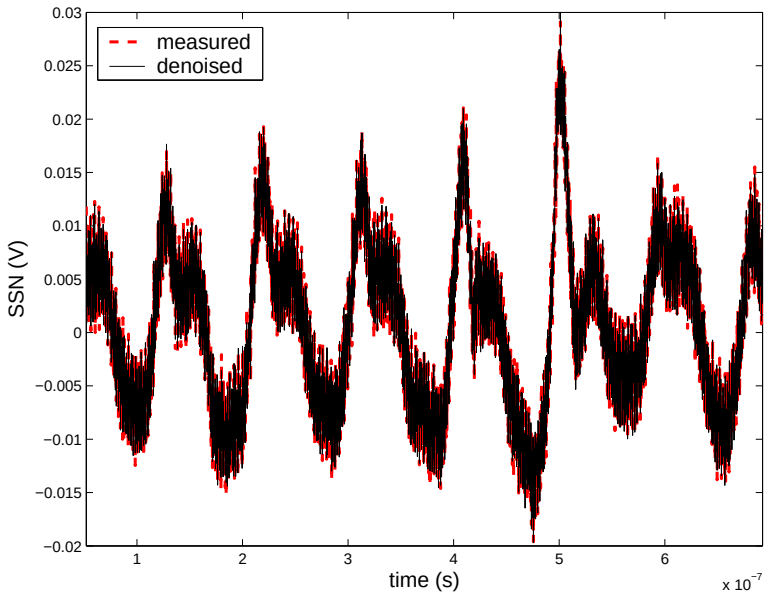

Figure 32: Comparison of the measured SSN waveform with its de-noised version

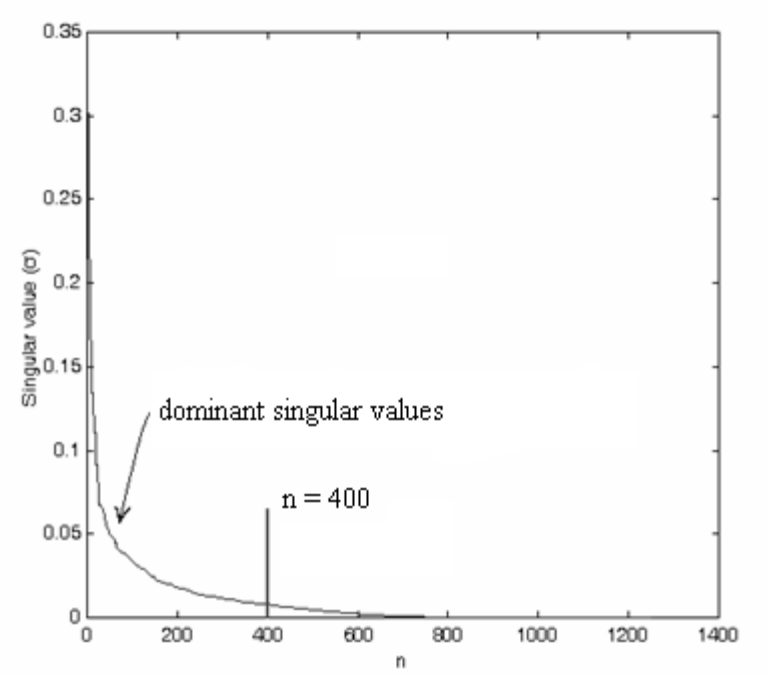

Figure 33: Singular value decomposition of the SSN voltage waveform

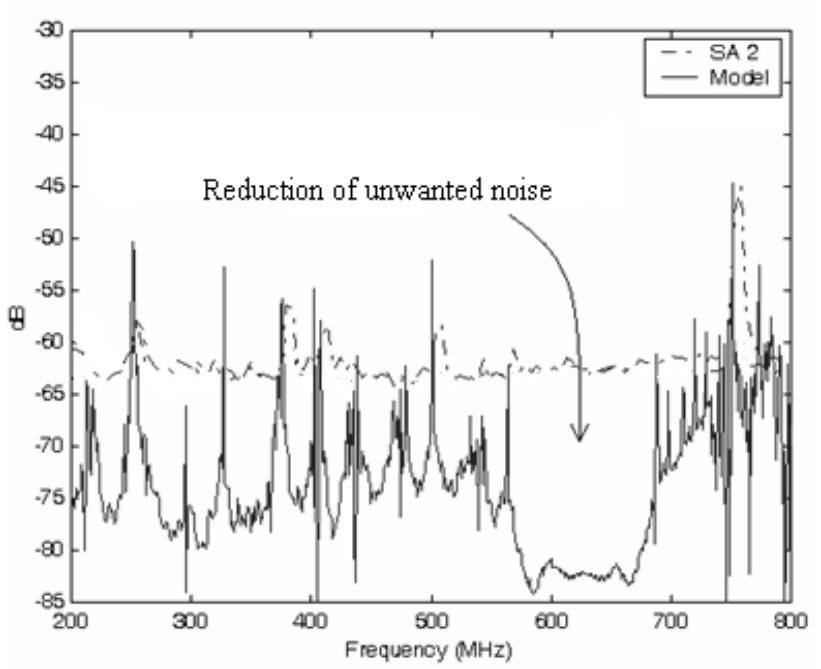

Figure 34: Comparison of the de-noised and modelled SSN waveform with its SA measurement

most significant singular values were retained to form the parametric model of the signal. The generated model is shown in both the frequency and time domains in Figures 34-36. The NR approach for modeling the SSN voltage waveform was able to efficiently capture all the dominant resonances from the measured data. In addition, the thresholding of the wavelet transform along with discarding of the unwanted singular values in GPOF, lowers the noise floor in the signal by more than -15dB over the 200-800MHz frequency band. The time domain comparison shows good correlation between the model and measurement data over the entire measurement interval of 1μs. Figure 36 guarantees that all the phase related information in the data, like the location and amplitude of the peak fluctuation noise are preserved in the model. The figure magnifies a 200ns interval around the peak noise spike.

2.4.2.1 Problem with using spectrum analyzer measurement

Even though that spectrum analyzer provides only the magnitude of the voltage spectrum, the phase spectrum could be obtained using the Hilbert transform [43]. However since the spectrum analyzer measurement is plagued by a high noise floor, it introduces considerable error in the computation of the phase spectrum. To illustrate this the model of the SSN

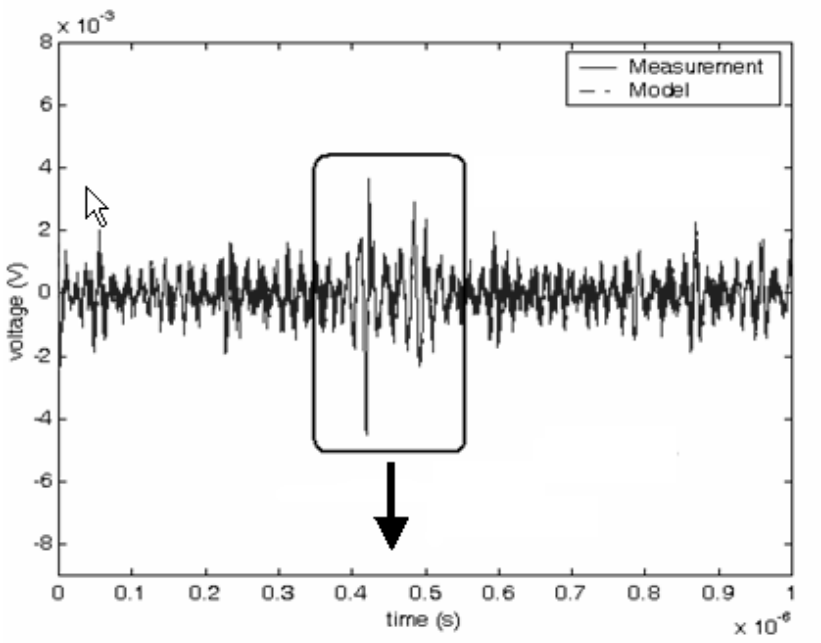

Figure 35: Comparison of the modelled and measured SSN waveform in the time domain

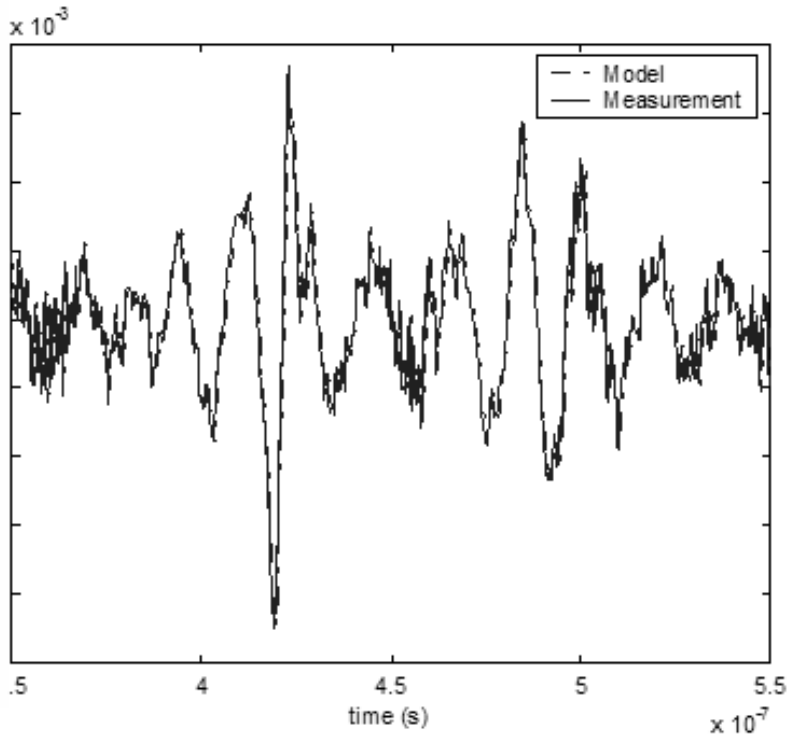

Figure 36: Time domain comparison over 200ns interval around noise peak

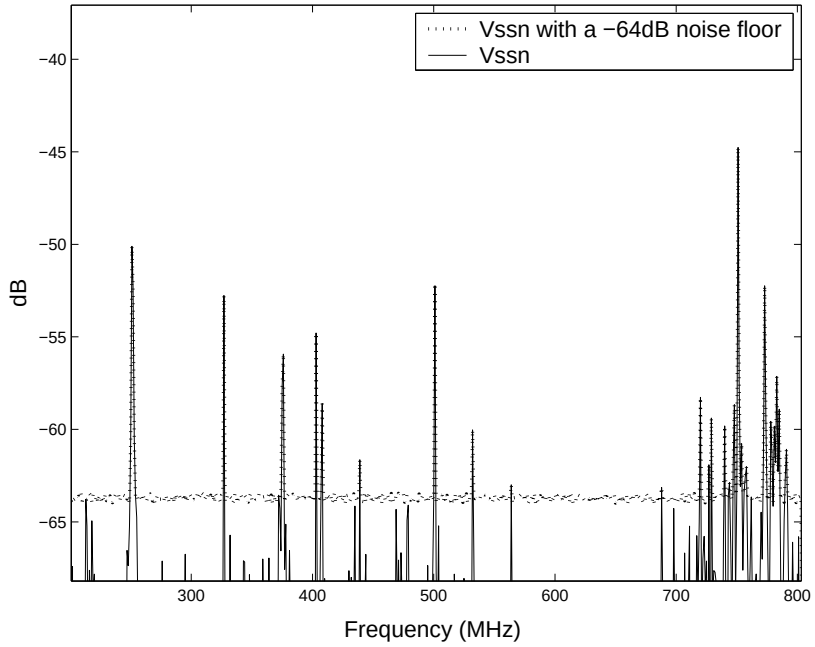

Figure 37: SSN model from Figure 34 with a higher noise floor

voltage in Figure 34 was injected with noise such that its noise floor was around -64dB (about that of the SA measurement). The magnitude spectrum of the original model and the model with the higher noise floor is shown in Figure 37. Using this new magnitude spectrum, the phase spectrum of the signal was computed using the Hilbert transform and the complete frequency response was converted to the time domain to obtain a transient waveform. This transient waveform is plotted in Figure 38 where it is compared with the time domain waveform representing the model in Figure 34. It is seen from the figure that the transient waveform obtained using Hilbert transform is completely off from the correct waveform. Both the peak as well as the phase accuracy is seen to be compromised. This shows that it is difficult to use a spectrum analyzer to extract accurate transient representations of switching waveforms.

2.5 Summary

In this chapter a wavelet based technique for de-noising and modeling transient waveforms is proposed. The technique performs the de-noising using a nonparametric regression approach and models the de-noised waveform in terms of its poles and residues using the generalized

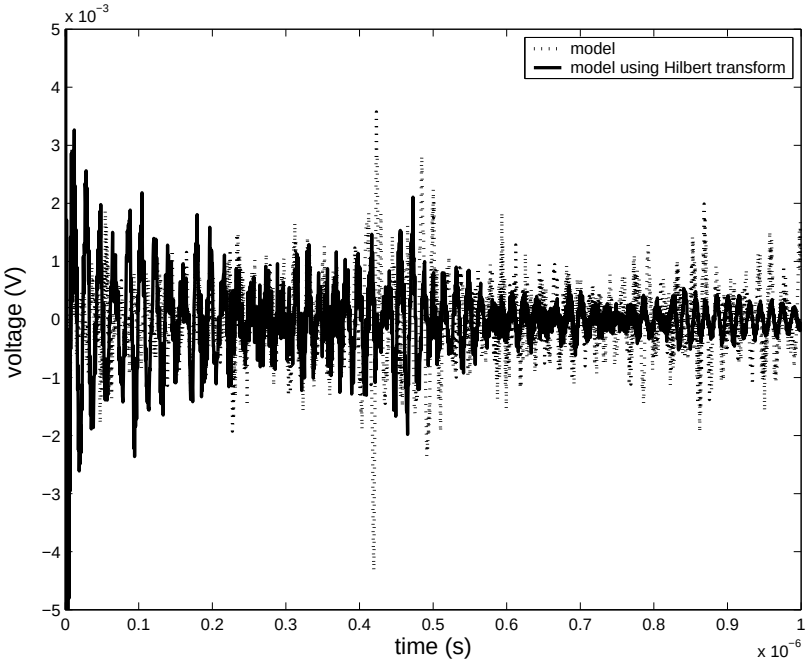

Figure 38: Transient waveform generated using Hilbert transform on the magnitude spectrum

pencil-of-function method. The technique is tested using a simulated transient waveform that is added with Gaussian noise of increasing variance. It is seen that as the noise in the transient waveform increases, it becomes increasing difficult to extract its poles and residues. The NR estimate obtained from de-noising the transient signal however accurately yields the system poles and residues. The technique is also used to de-noise a measured SSN waveform on a function computer system. The de-noised and modelled waveform is seen to retain all the dominant resonances and phase information from the measured waveform. In the next chapter this de-noising technique is used on measured transient data from functioning computer systems to extract the switching noise current signatures in those systems.

CHAPTER III

MODELING OF SWITCHING NOISE CURRENT SIGNATURES

An accurate simulation of the SSN in a complex digital system requires an accurate model of the PDN of the system and a precise knowledge of the transient switching currents that are injected into this PDN. Since these transient switching noise currents are difficult to determine analytically, some methods have been proposed in the past that rely on measurements to estimate these currents. A brief description on the prior art in this area is given in section 1.2 of Chapter 1. The key limitation of these measurement based techniques for estimating the switching noise currents can be identified to be the fact that they all rely on frequency domain measurements. Frequency domain measurements performed using a spectrum analyzer provide only a magnitude spectrum of the measured waveform. There is no phase information provided. Hence switching current extraction techniques that use these measurements can extract only the magnitude spectrum of the switching currents but not their phase spectrum. Though the magnitude spectrum of the switching noise currents is extremely useful in understanding the load exerted on the PDN of a system, it cannot be used in performing a transient simulation to simulate SSN in the system. In the design of complex digital systems having high performance requirements and low tolerances, an accurate time domain simulation of the SSN can prove invaluable. To enable such a simulation, the switching noise current spectrum should have both magnitude and phase information. This chapter proposes a new technique for extracting the switching noise current spectrum using time domain measurements such that both the magnitude and the phase information of the spectrum are extracted. With both magnitude and phase information available, the switching noise current can be transformed and viewed in the time domain as a switching noise current signature.

The key obstacle to the use of time domain measurements in switching noise current

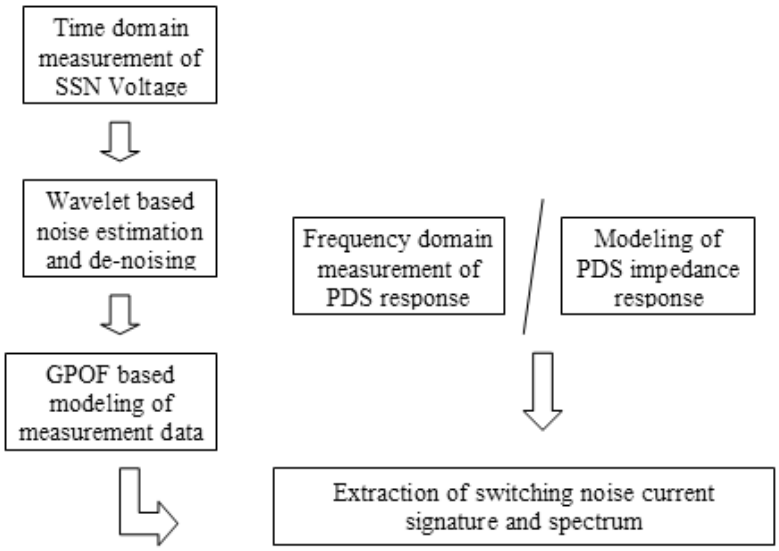

Figure 39: Flow diagram for extraction of switching noise current signatures

extraction is the measurement noise that plagues a time domain measurement. Chapter 2 proposes a solution to this problem in the form of a de-noising and modeling technique for measured transient waveforms. The methodology described in Chapter 3 uses this technique to extract switching noise current signatures in functioning digital systems. A flow diagram of the proposed switching current signature extraction methodology is shown in Figure 39. This chapter uses two real-world test cases: 1) a functioning computer system from Sun Microsystems, and 2) an IBM Power5 microprocessor to describe the details of the methodology. The remainder of the chapter is organized as follows. Section 3.1 describes the extraction of switching noise current signatures in the PDN of a functioning computer system from Sun Microsystems. The section includes the description of the system setup and the measurements performed on the system (subsection 3.1.1), the application of the switching noise current extraction procedure and the analysis of the results obtained subsection 3.1.2), and the simulation of the SSN in the system using the obtained switching current waveforms (subsection 3.1.3). Section 3.2 describes the extraction of switching noise current signatures in the PDN of an IBM Power5 microprocessor. The section includes the description of the system and the measurements carried out on it (subsection 3.2.1), a sensitivity study performed to understand the effect of data length on a waveform's

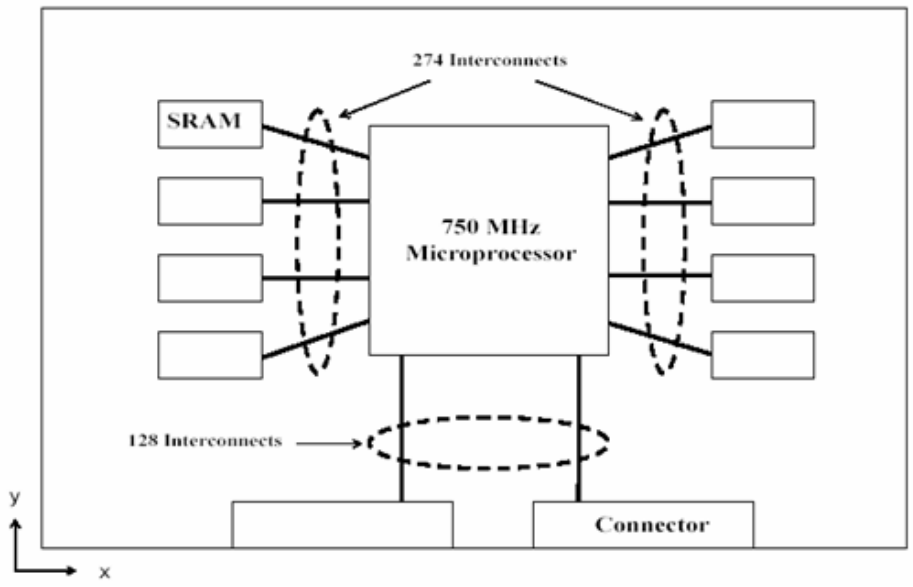

Figure 40: Top view of the functioning board

spectral content (subsection 3.2.2), and the extracted switching noise current signatures for the system (subsection 3.2.3).

3.1 Functioning Sun Microsystems computer system

This section describes the extraction of switching noise current signatures in the PDN of a functioning computer system from Sun Microsystems.

3.1.1 Description of the setup

The system used to describe the current signature extraction technique proposed in this chapter is a high-performance functioning workstation from Sun Microsystems [18]. The PDN for the core circuitry includes a dual core 750MHz microprocessor, a heat sink and a pair of core Vdd/ground planes with 195 decoupling capacitors between the planes. The top view of the functioning board is shown in Figure 40. The core PDN supplies power to the active circuitry on the microprocessor. Any switching related voltage fluctuation on the core PDN, which exceeds the noise tolerance, can cause catastrophic failure of the system. Figure 41 shows the equivalent circuit schematic of the PDN at the printed circuit board and the chip-package levels. The two ports used for measurement were located such that port

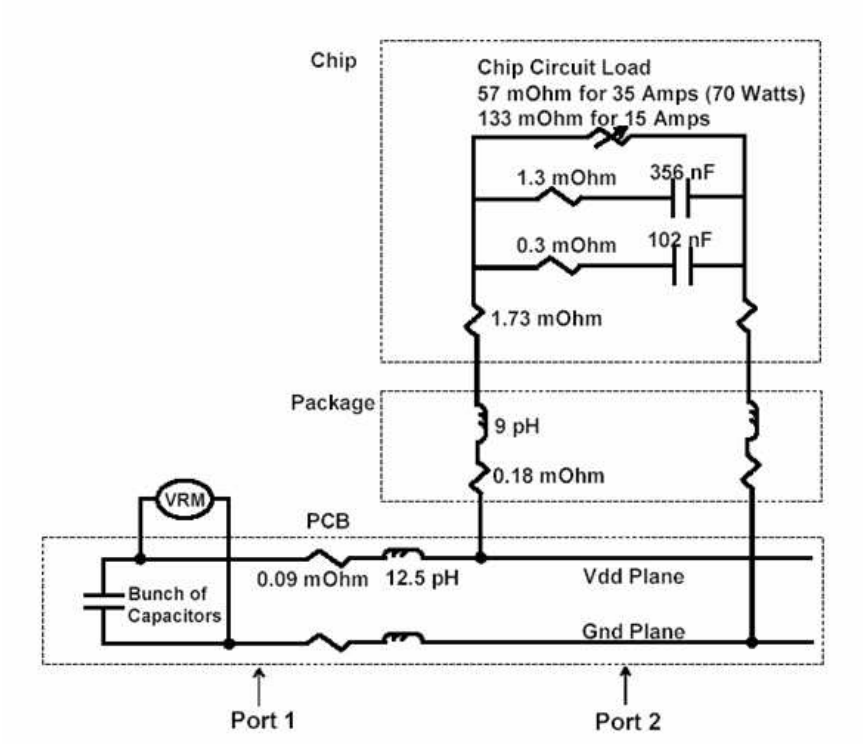

Figure 41: Circuit schematic of test system along with port locations

2 was directly beneath the microprocessor, so that the switching noise there was maximum and most relevant to guaranteeing satisfactory performance of the microprocessor. Port 1 was located away from the active circuitry. Ideally port 1 could be located near the voltage regulator module on the PCB. That way the injected current profile at port 1 would closely correspond to the supply current drawn. The SSN voltage measurements at the two ports were carried out using a DSO while the impedance profile of the PDN was measured using a vector network analyzer as described in [18]. The DSO measurements were first de-noised and modelled using the technique presented in Chapter 2. The details of this procedure for the waveform measured at port 2 are given in subsection 2.4.2. The de-noised SSN waveform at port 2 is shown in Figure 42. Similarly the SSN waveform measured at port 1 was de-noised and modelled. For this waveform the DB-9 wavelet filter at a scale 4 gave the optimum wavelet representation of the measured voltage. The standard deviation of the measurement noise was estimated to be 9.77e-04. The de-noised SSN waveform at port 1 is shown in Figure 43.

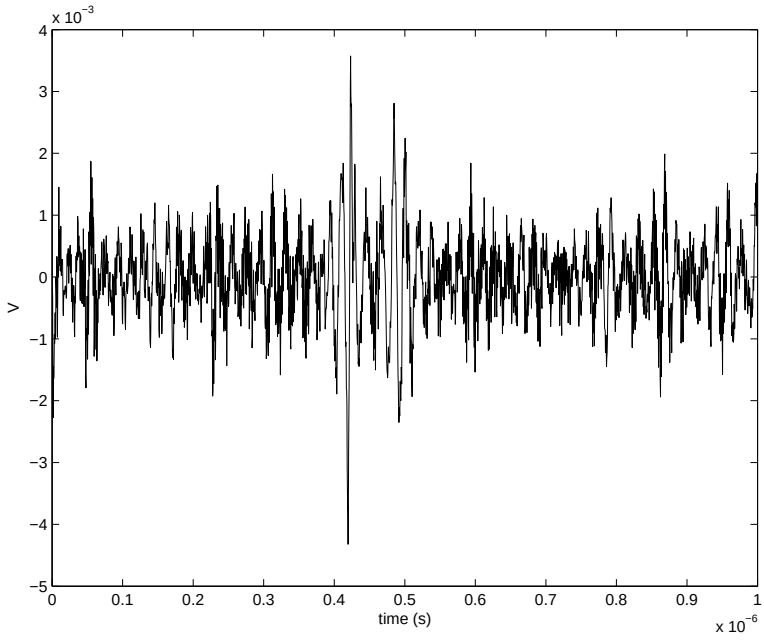

Figure 42: SSN measured at port 2 of the computer system

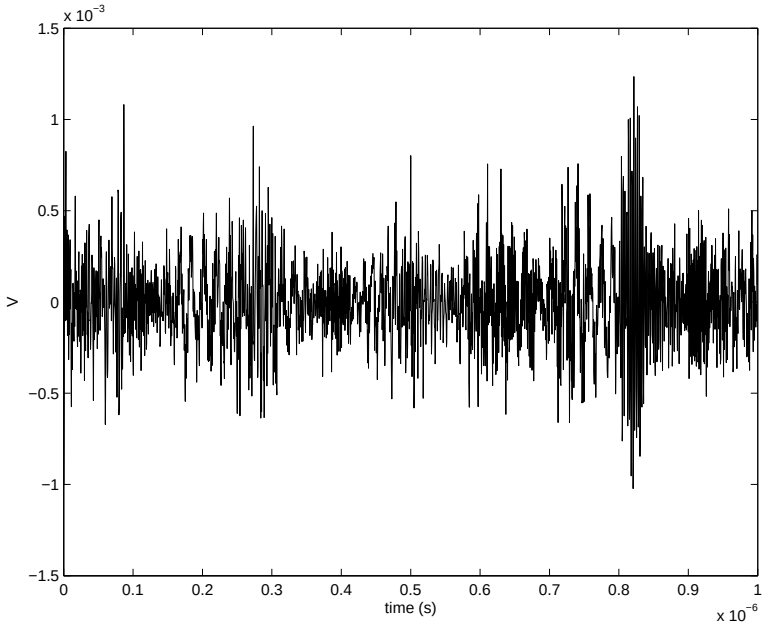

Figure 43: SSN measured at port 1 of the computer system

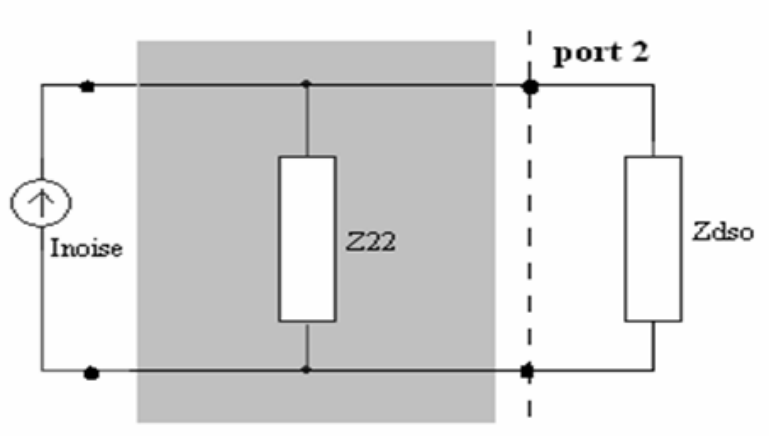

Figure 44: Equivalent Z-parameter circuit

3.1.2 Switching noise current signature extraction

Once the measured SSN waveforms have been de-noised and modelled, an equivalent Z-parameter circuit of the PDN of the test system is constructed as shown in Figure 44. The required SSN current signature is modelled as a source I_{Noise} that excites the PDN as shown in the figure. The voltage at port 2 (V_2) is taken to be the SSN voltage model extracted as described earlier and shown in Figure 42. The Z_{22} in the circuit is derived from the impedance measurements carried out on the PDN using a network analyzer. If the network analyzer outputs S-parameters, they can be easily transformed into Z-parameters using standard techniques [46]. In the above network since the input impedance of the oscilloscope (Z_{dso}) is set to the order of 1 MΩ as compared to a few mΩs range of the input impedance (Z_{22}) of the PDN, it is seen that

$$Z_{dso} >> Z_{22} \tag{32}$$

Hence, by solving the equivalent circuit in Figure 44, the voltage at port 2 is given as

$$V_2 = I_{Noise}.Z_{22} \tag{33}$$

Knowing the port voltage V_2 and the self impedance Z_{11}, the SSN current at port 2 is computed through deconvolution. Total Least Squares deconvolution has been used in this work to perform the required deconvolution [47]. Total Least Squares deconvolution solves the deconvolution problem assuming error in both the observation vector (formed using

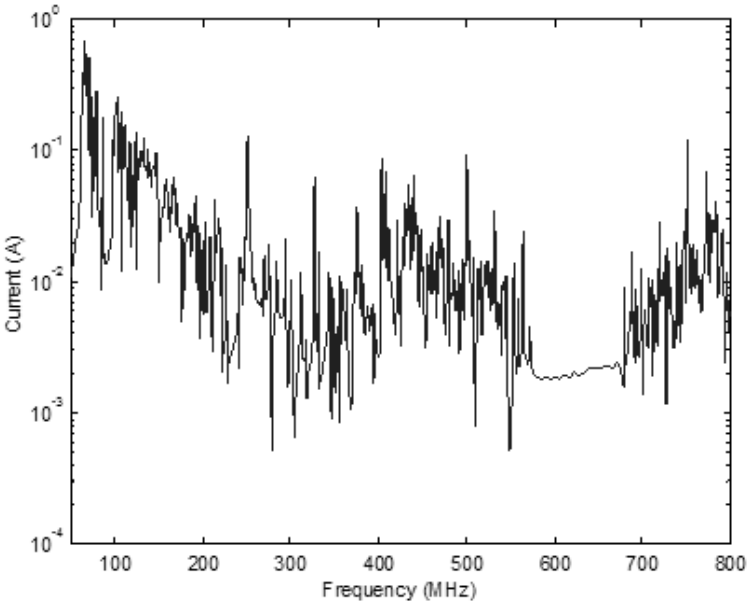

Figure 45: Frequency spectrum of I_{Noise} at port 2

V_2) and the data matrix (formed using Z_{12}). This method is particularly useful when the data matrix is singular or highly ill conditioned which is often the case when dealing with switching noise data. In addition the technique also suppresses the spurious instabilities that would arise in the extracted I_{Noise} if the computation was carried out as a simple vector division in the frequency domain. A brief description of the Total Least Squares deconvolution technique is given in Appendix A. The I_{Noise} model thus extracted has magnitude as well as phase information.

The frequency spectrum of switching noise current I_{Noise} computed for port 2 is shown in Figure 45. In the figure the fundamental clock frequencies of the different system modules, and modulation components among these clocks can be identified. For e.g., a sharp spike is seen at 750 MHz which is the fundamental clock frequency of the microprocessor. Similarly the fundamental clock frequency of the SRAM bus is seen to create a spike at 250 MHz. In addition to these fundamental frequencies intermodulation occurs amongst the clocks, giving rise to modulation components. These can be seen at 500 MHz due to modulation between the 750 MHz microprocessor clock and the 250 MHz SRAM bus, and at 375 MHz due to modulation between the SRAM bus and the 125 MHz connector bus. Finally, board resonances also result in high switching noise currents at those frequencies. These are

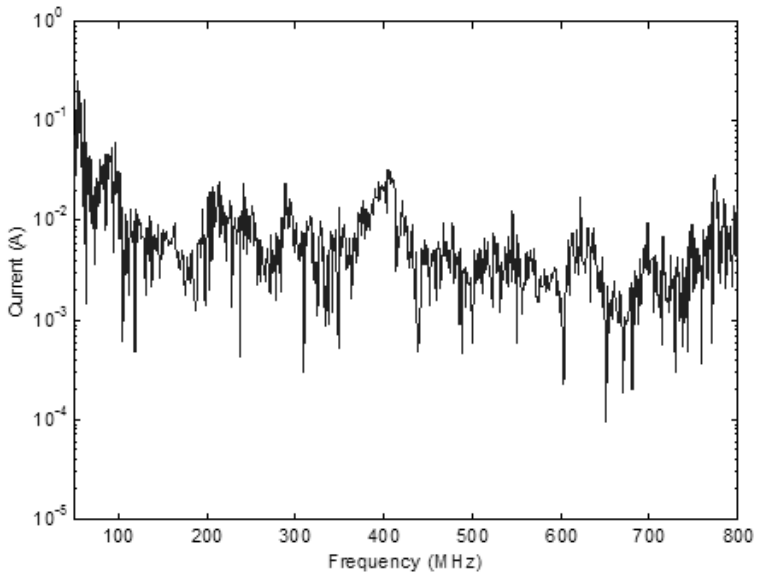

Figure 46: Frequency spectrum of I_{Noise} at port 1

frequencies where the impedance of the PDN is very low. Hence, any residual charge on the power/ground planes leads to currents at these frequencies. In Figure 45 these can be seen at 325 MHz and 530 MHz. The frequency spectrum of the switching noise current at port 1 is shown in Figure 46. As expected the characteristics of the switching noise spectrum at port 1 are found to be different from those at port 2. Since port 1 lies away from active circuitry, the switching noise there is seen to be suppressed, e.g., the current peak at 750 MHz due to the microprocessor clock is considerably smaller than at port 2. This is because the peak to peak amplitude of the noise at port 1 is only about 2mV as compared to nearly 8mV at port 2.

3.1.3 Simulation of SSN

The switching noise current extraction technique described in the previous section can be modified for the extraction of current signatures that can be used in the simulation of SSN. For this a 2-port equivalent circuit of the PDN is created as shown in Figure 47. The SSN current that excites the plane pair in the PDN is modeled as a current source I_{SSN}. The SSN voltage waveform measured at port 2 when de-noised and modelled forms V_2 in the circuit. Since the impedance of the oscilloscope is orders of magnitude greater than the

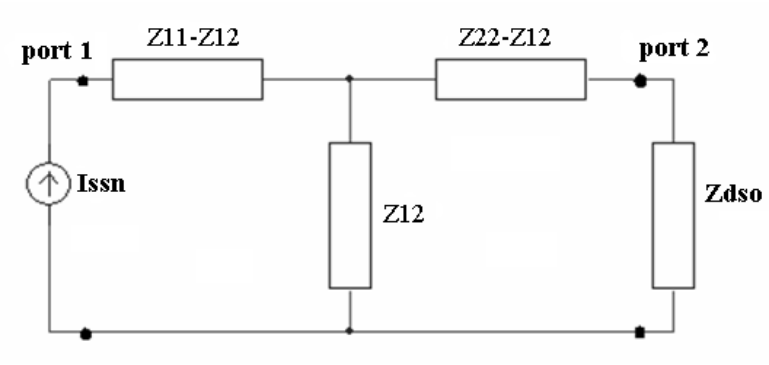

Figure 47: Two port equivalent circuit of the PDN

transfer impedance Z_{12} of the circuit,

$$(Z_{dso} + Z_{22} - Z_{12}) >> Z_{12} \tag{34}$$

Hence, by solving the equivalent circuit in Figure 47, the voltage at port 2 is given as

$$V_2 = I_{SSN}.Z_{12} \tag{35}$$

Therefore, using the de-noised and modelled port voltage and the transfer impedance, the excitation current source (I_{SSN}) can be calculated using deconvolution. The spectral content of I_{SSN} extracted as described above is shown in Figure 48. Since the extracted I_{SSN} has magnitude as well as current information, it can also be viewed as a time domain current signature as shown in Figure 49.

To test the accuracy of the extracted I_{SSN}, it was used to simulate SSN in the Sun Microsystems computer system. The SSN was simulated over a period of 1μs using the equivalent circuit in Figure 47. In the first case the measured value of the PDN impedance was used. Hence the SSN voltage is given by

$$V_2 = I_{SSN}.Z_{12(Measured)} \tag{36}$$

Figure 50 compares the simulated SSN voltage waveform with the measured voltage over an interval of 200ns around the peak noise voltage. The figure indicates excellent agreement between the simulated and measured noise waveforms. In the second case the switching noise was simulated using the modelled impedance profile of the PDN. The cavity resonator

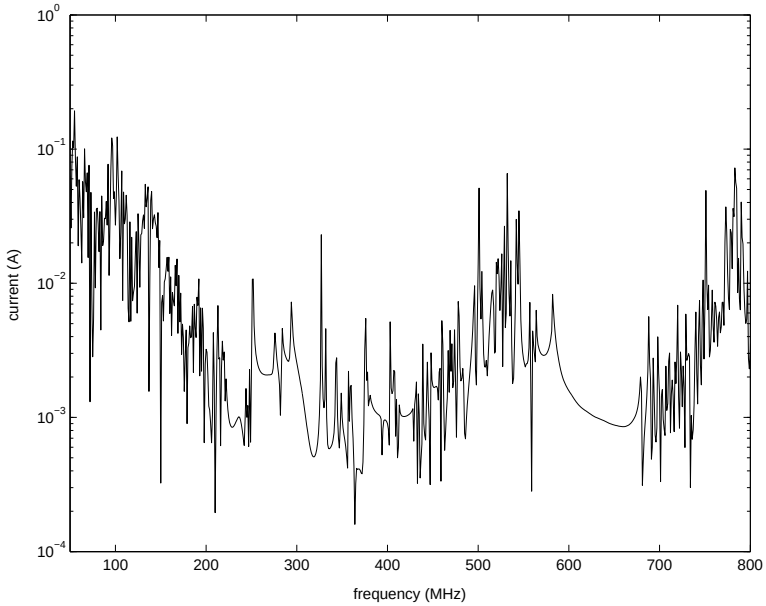

Figure 48: Spectral content of I_{SSN}

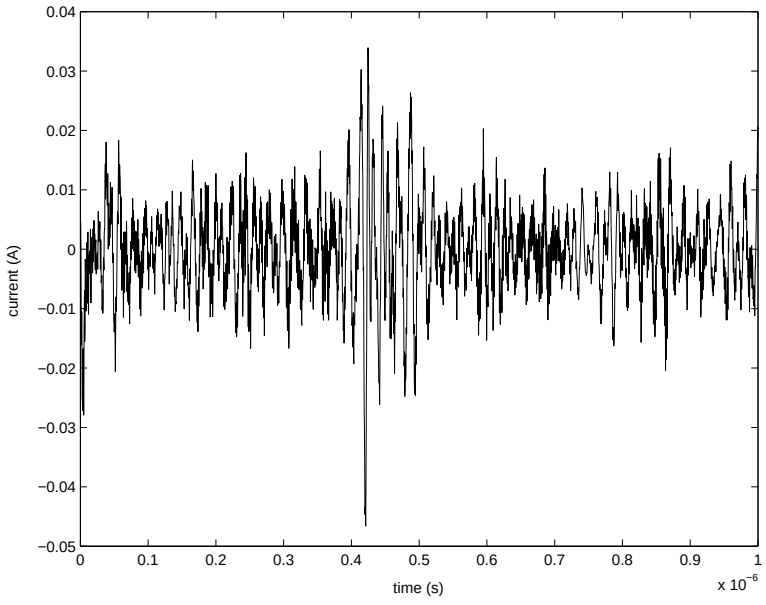

Figure 49: Time domain signature of I_{SSN}

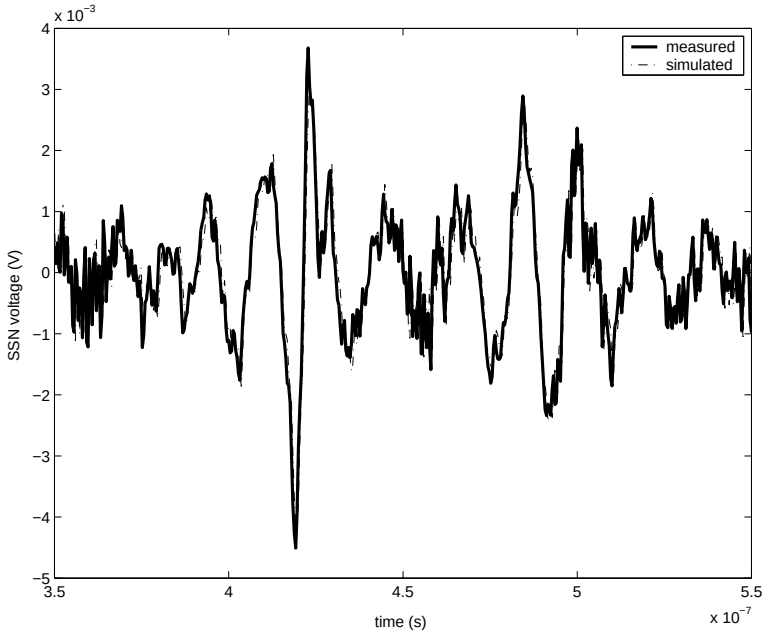

Figure 50: Measurement-simulation correlation of SSN using measured Z_{12}

method described in [18] was used for modeling the PDN. Here the SSN voltage is given by

$$V_2 = I_{SSN}.Z_{12(Modeled)} \tag{37}$$

Figure 51 compares the simulated SSN voltage waveform with the measured voltage over an interval of 200ns around the peak noise voltage. The location of the peak noise and the phase of the SSN voltage waveform are reproduced with good accuracy. The slight mismatch in the peak amplitude and the few spurious oscillations seen in the simulated waveform can be attributed to some imperfection in the modeling of the PDN. Figure 52 shows the relative error between the measured and modelled values of the transfer impedance of the system. This is calculated using the equation

$$\text{Rel.}Error = \frac{\left|Z_{12(Measured)} - Z_{12(Modeled)}\right|}{\left|Z_{12(Measured)}\right|} \tag{38}$$

The plot of the relative error shows that the accuracy of the model in tracking the system transfer impedance is relatively low at some frequencies like in the 750-800MHz range. This mismatch can give rise to some unwanted frequency components in the simulated SSN waveform over this frequency range. Figure 53 compares the frequency spectra of the two simulated SSN waveforms obtained using Equations 36 and 37. From the comparison it can

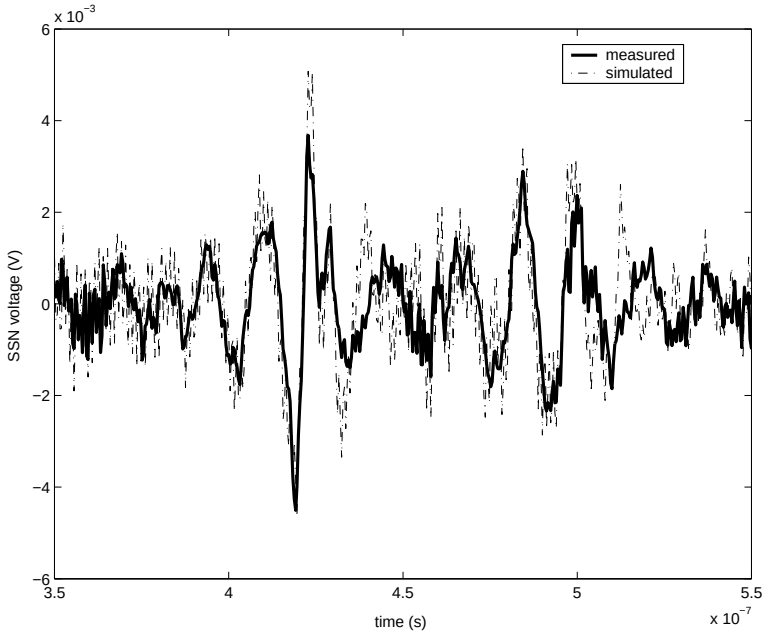

Figure 51: Measurement-simulation correlation of SSN using modelled Z_{12}

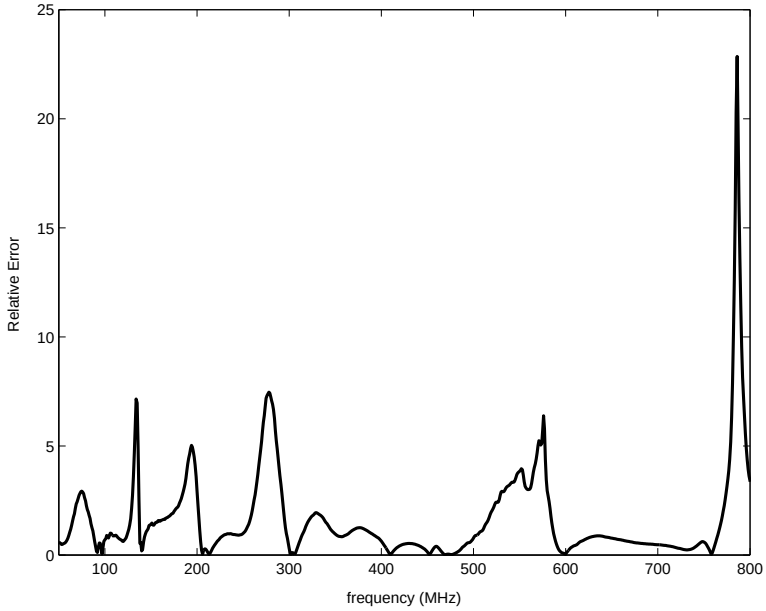

Figure 52: Relative error between measured and modelled values of Z_{12}

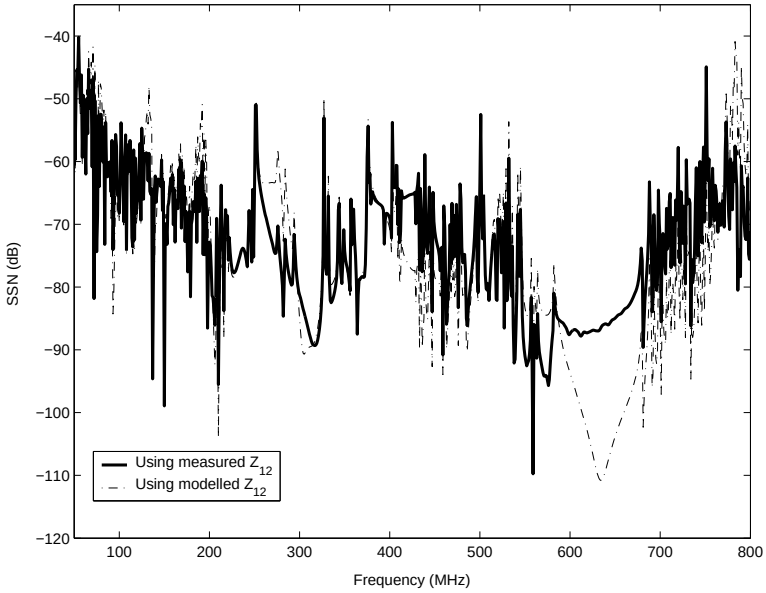

Figure 53: Comparison between the spectra of the two simulated SSN waveforms

be noted that as long as the model to hardware correlation of the transfer impedance is good, excellent correlation is obtained between the two simulations. However, inaccuracies in the impedance model make the simulated SSN waveform susceptible to unwanted frequency components in the range of the impedance mismatch.

3.2 IBM Power5 microprocessor

This section describes the extraction of mid frequency switching noise current signatures in the PDN of an IBM Power5 microprocessor.

3.2.1 Description of the setup

The system under study in this case is an IBM e-server system based on the Power5 microprocessor. The work involves the extraction of switching noise current signatures in the on-chip metallization of one of the Power5 microprocessors installed in the system. The microprocessor running at 1.65 GHz is provided with a supply voltage of 1.2V and is kept at a constant temperature of 15^oC. The system is booted using the AIX operating system and the measurements are carried out with the operating system functioning in Idle mode. The voltage on the on-chip metallization is measured with a special probing setup using a digital sampling oscilloscope in the time domain, and using a spectrum analyzer in the

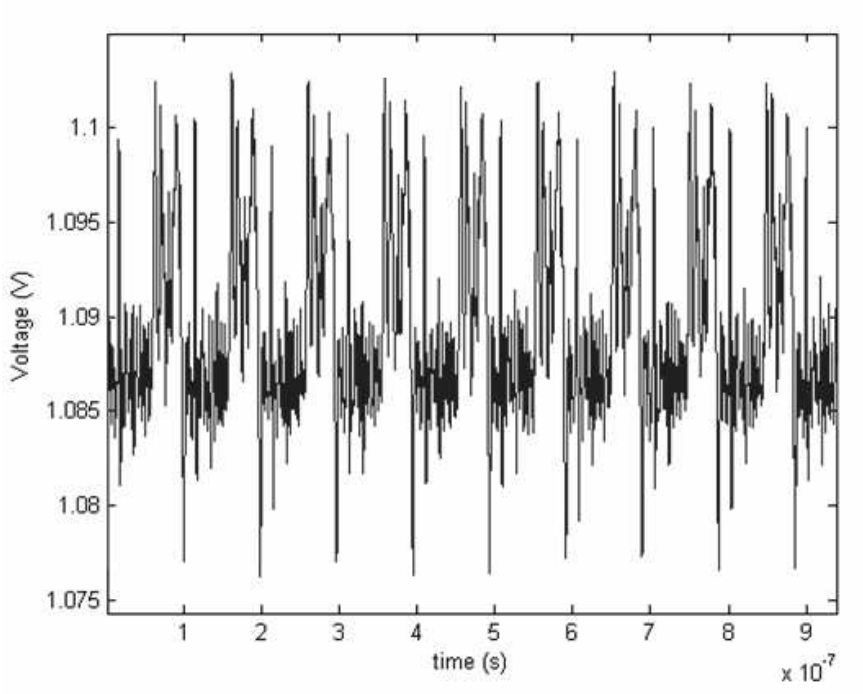

Figure 54: SSN measured on the PDN of an IBM Power5 microprocessor

frequency domain. The impedance response of the on-chip PDN is computed using a clock gating technique described in [52]. This work focusses on the extraction of switching current signatures in the mid-frequency region ranging from 5 MHz to 160 MHz.

The SSN voltage on the on-chip PDN measured using the DSO was de-noised and modelled, and is shown in Figure 54. This waveform is converted to the frequency domain and is compared with the SA measurement in Figure 55. The time domain measurement is seen to have a lower noise floor and is seen to capture the harmonics in the signal more sharply. In a functioning microprocessor because of the presence of several nonlinear circuits and loads, it is possible that the impedance response of the PDN is nonlinear. Hence the impedance response of the PDN for the Power5 microprocessor was computed using a clock-gating technique that is described in [52]. The magnitude of the impedance response is shown in Figure 56. However the switching current extraction technique described in this chapter requires the complete impedance profile of the PDN. Hence the phase profile of the PDN needs to be computed in order to proceed with current signature extraction. If the PDN impedance is assumed to linear, this can be performed using the Hilbert Transform

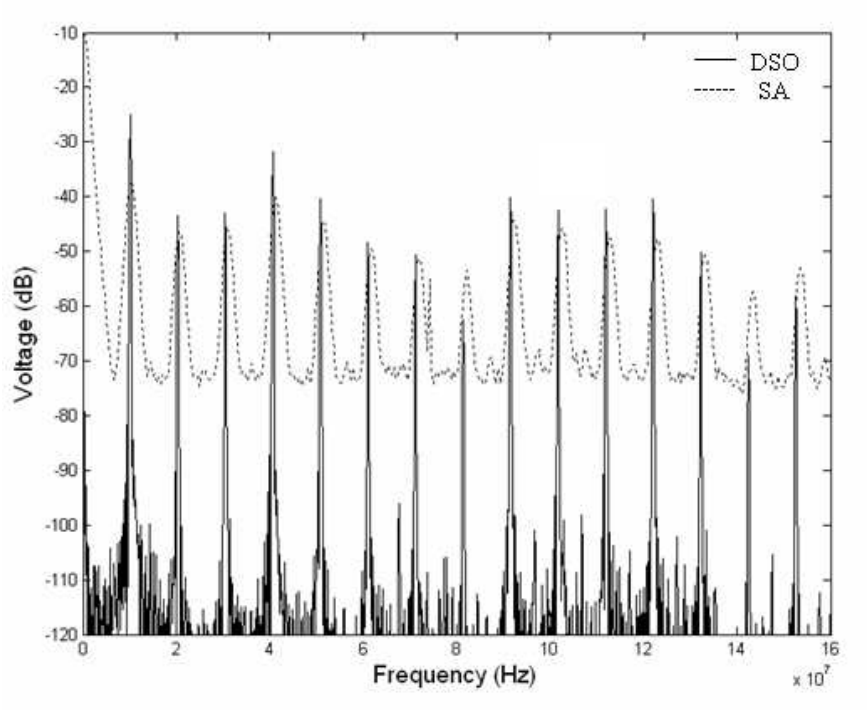

Figure 55: Frequency domain comparison of the SSN in an IBM Power5 microprocessor

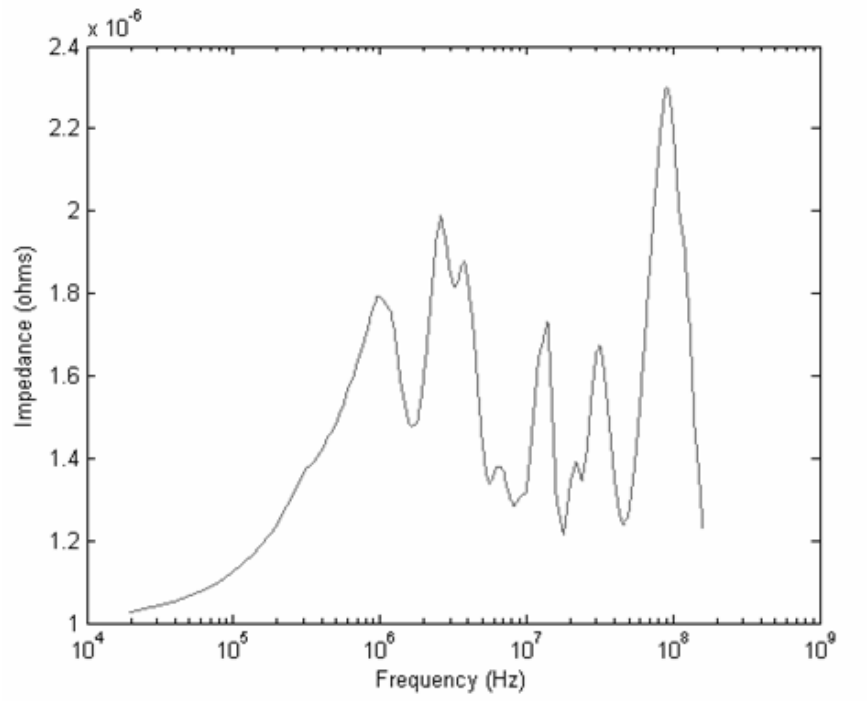

Figure 56: Magnitude of PDN impedance computed using the clock gating technique

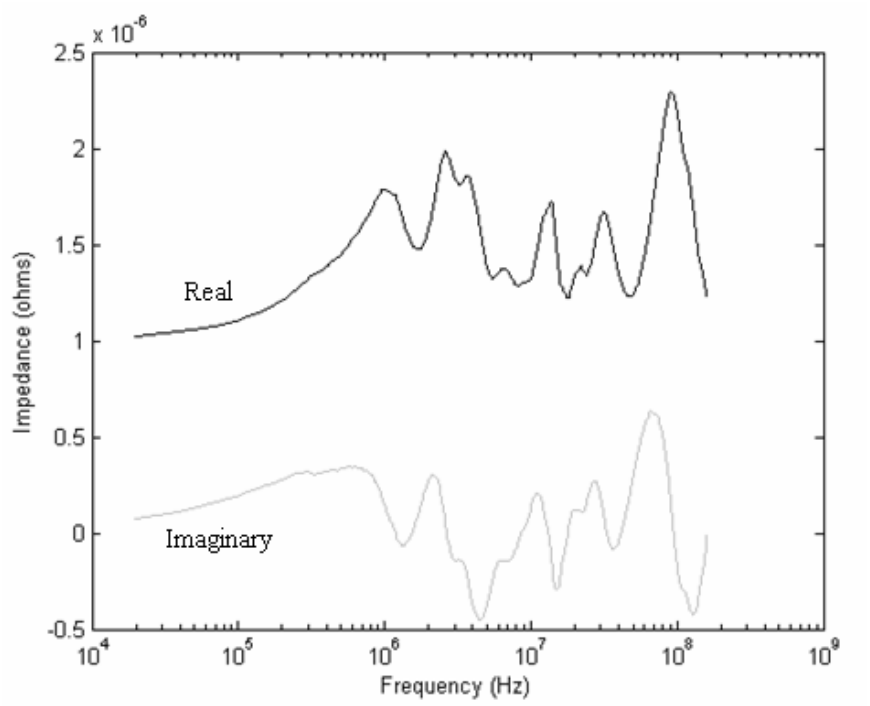

Figure 57: Real and imaginary parts of the PDN impedance profile

[43]. Since the above impedance response is the self impedance of the PDN at the port of measurement, and it is known that the self impedances of a PDN are minimum phase responses, the phase profile of the impedance response is related to its magnitude profile. This relation is given by the Hilbert Transform as

$$\angle[H(j\omega)] = -\frac{1}{2\pi}\mathrm{P}\int_{-\pi}^{\pi}\log|H(j\theta)|\cot\left(\frac{\omega-\theta}{2}\right)d\theta \tag{39}$$

where P is the Cauchy principal value. The real and imaginary parts of the complete PDN impedance response thus computed are shown in Figure 57. . Performing deconvolution on the self-impedance thus obtained along with the measured SSN voltage waveform gives the switching noise current signature in the PDN of the microprocessor.

3.2.2 Study of the sensitivity of the waveform measurement duration on its spectral content

The SSN voltage waveform measured using the DSO was sampled at 8 GHz for 65,536 samples. Using such a long sequence in the total least squares deconvolution formulation results

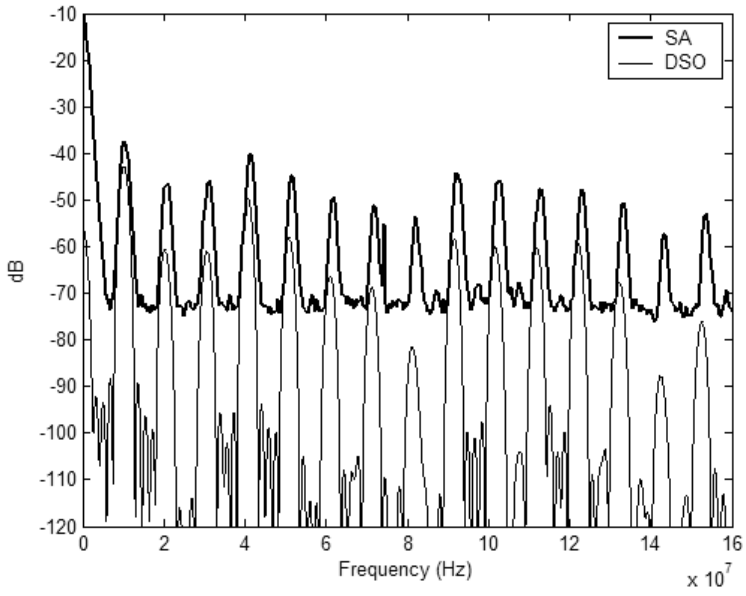

Figure 58: Spectral content of SSN measurement 4096 samples in length

in an extremely large matrix equation. Solving this equation requires considerable computing resources and time. Since the measured waveform from Figure 54 is fairly (but not perfectly) periodic a possible solution to the above problem is the use of voltage waveforms of shorter lengths. This subsection describes the study that was performed to understand the effects of using SSN waveforms of shorter lengths in the deconvolution computations. When the spectral content of the SSN voltage waveforms of different lengths was compared, the key observation was that their spectral content varied slightly with the measurement duration (or in turn their length). The SSN voltages measured on the on-chip metallization of the IBM Power5 microprocessor for different measurement durations (data lengths) are plotted in Figures 58 to 62 in contrast with the spectrum analyzer measurement. It can be seen from the figures that for voltage waveforms of extremely short lengths, the power present in each harmonic tends to diffuse into a 'hump' around that frequency. As the data length increases, each of these 'humps' become narrower and sharper. This means that the voltage waveform is able to better locate the precise location of each harmonic. However the amplitude of each of the harmonics increases as the 'humps' get skinnier. Since the harmonic amplitudes of the waveform for data length of 16,384 are seen to best match those obtained from the SA, this waveform has been used to extract the switching noise

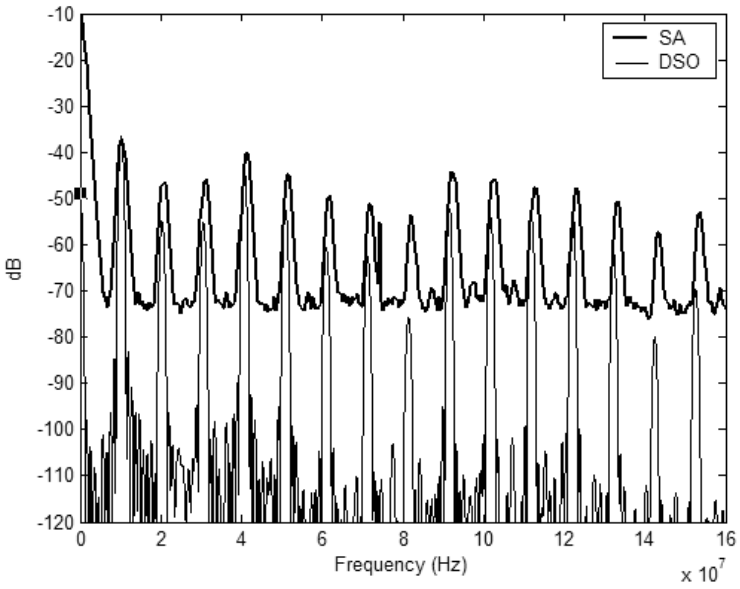

Figure 59: Spectral content of SSN measurement 8192 samples in length

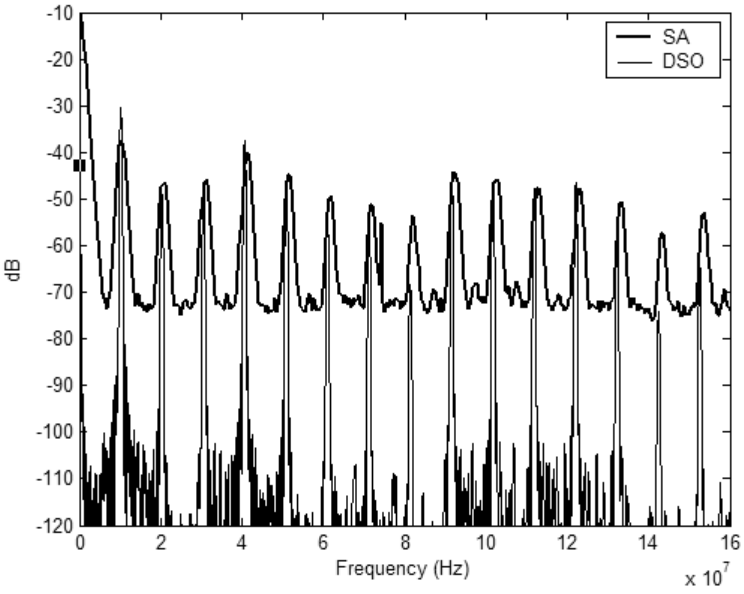

Figure 60: Spectral content of SSN measurement 16384 samples in length

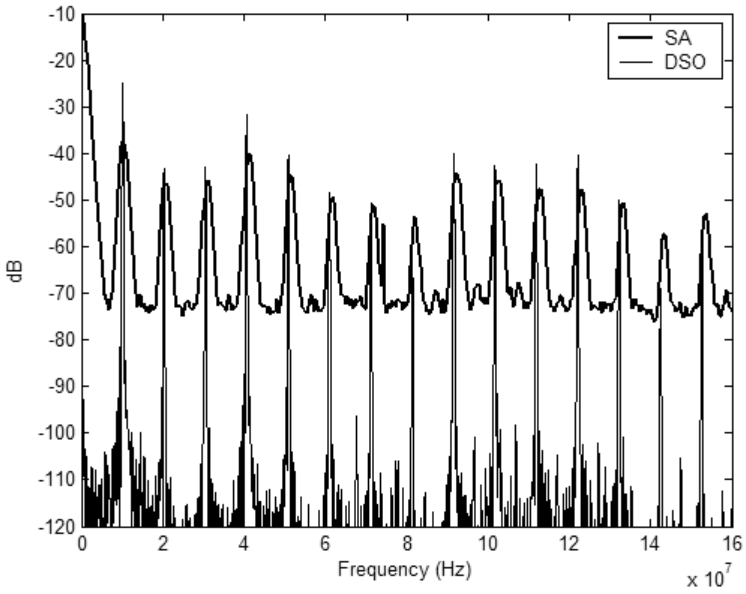

Figure 61: Spectral content of SSN measurement 32768 samples in length

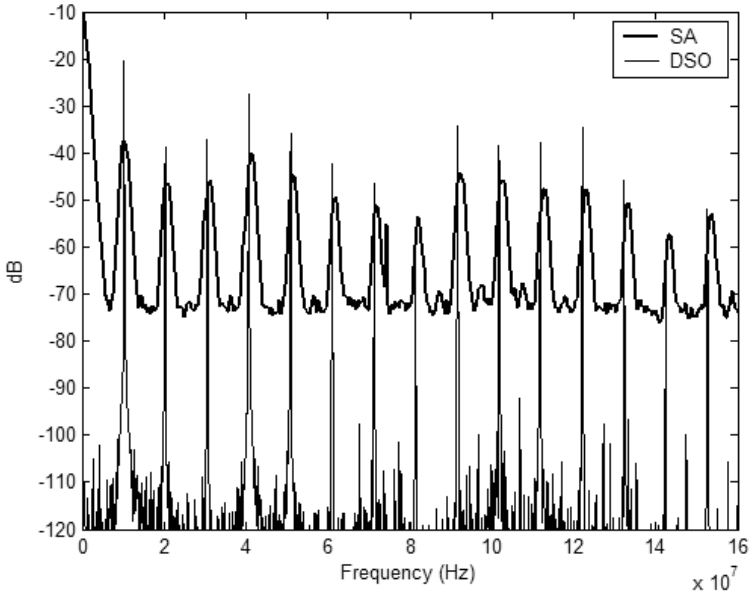

Figure 62: Spectral content of SSN measurement 65536 samples in length

current signature in the PDN. It is to be noted that though this waveform (16,384 samples) does not represent the best measurement available (longer waveforms tend to give a more accurate spectrum), it has been used for current signature extraction for two reasons:

1. The amplitudes of the harmonics for this waveform match the best with those obtained using the SA. The spectral content of the extracted current signature is later benchmarked with that obtained using the method described in [52] which uses the SA measurement.

2. The waveform considerably reduces the deconvolution problem size as compared to that using the longest available waveform.

3.2.3 Switching noise current signature extraction

Figure 63 shows the extracted current signature in the PDN of the Power5 microprocessor. The spectral content of this current signature was compared with that extracted using the clock gating technique described in [52]. This comparison is shown in Figure 64. It is seen that the switching current waveform extracted using the technique described in this chapter has a considerably lower noise floor. Also it has both the magnitude and the phase profiles and hence can be used in the time domain (Figure 63) to excite transient simulations.

3.3 Summary

This chapter describes the measurement-based extraction of switching current signatures in functioning digital systems. The proposed technique requires a model or a measurement of the impedance profile of the system PDN, and a transient measurement of the SSN at the port location. By constructing an equivalent circuit model and formulating a deconvolution problem, the switching current signature at the desired location can be extracted from the above information. The method has been successfully tested on a functioning Sun Microsystems computer system and an IBM Power5 microprocessor. One of the current signatures extracted for the Sun Microsystems test case has also been used in the simulation of SSN in the system. The simulated SSN matches well with the measured waveform. The extracted current signatures in both the test cases have magnitude as well as phase

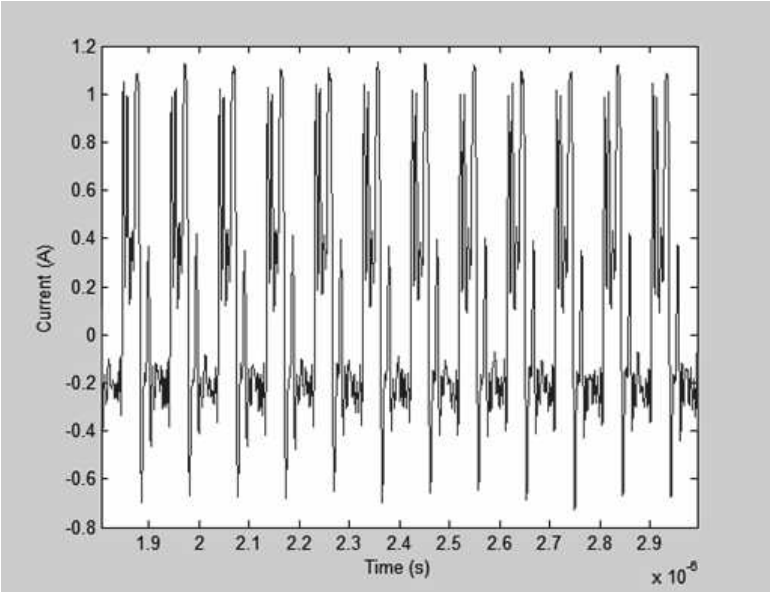

Figure 63: Time signature of the mid-frequency switching noise current

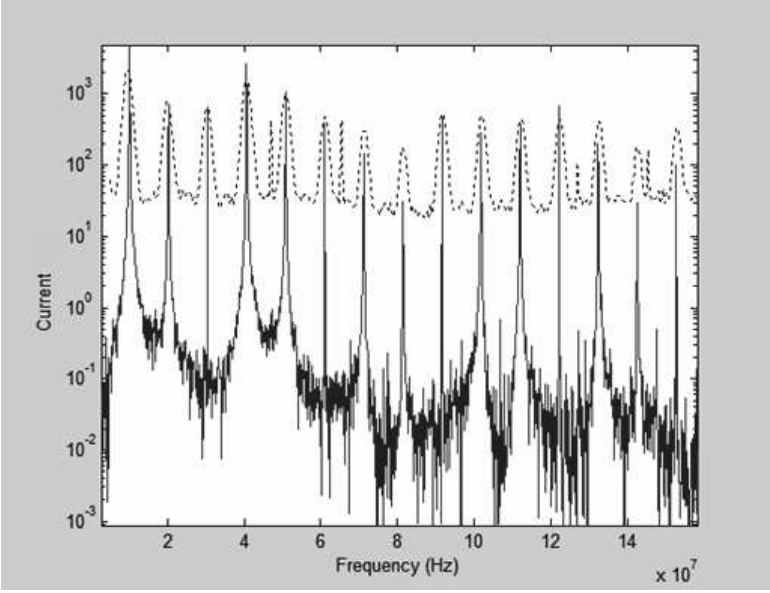

Figure 64: Spectral content of the mid-frequency switching noise current

information. None of the methods proposed in the prior art enable the extraction of both the magnitude and the phase profiles of switching currents. The Power5 microprocessor test case also includes a study that describes the effect of waveform length of a relatively periodic signal on its spectral content.

CHAPTER IV

TRANSIENT CO-SIMULATION OF SIGNAL AND POWER NETWORKS WITH CAUSALITY ENFORCEMENT

After the individual modules of a digital system are modelled accurately, they need to be simulated in order to predict the system performance. These simulations can either be done individually for each module or at a system level by integrating the different modules. Simulating the modules individually fails to account for the interactions between different modules which can sometimes be critical. In the previous chapter we have seen how the SSN in a system can be accurately simulated through the extraction of switching noise current signatures. However for a system designer, the bigger concern is how this SSN affects the performance of the other modules at the system level, primarily the SDN of the system. It is known that parasitic effects like SSN that occur in the PDN of a system affect the quality of the signals propagating through the SDN. If this coupling exceeds certain tolerance limits, it can cause catastrophic failure of the system. Traditionally, the SDN and the PDN of a system are simulated separately. An initial simulation of the SDN enables a design engineer to estimate a ballpark figure for the SSN that the system can tolerate. The PDN is designed so that the SSN generated in the system is kept well under this tolerance level in order to account for worst case scenarios. However with decreasing system tolerances and the need to keep design costs to a minimum, it is no longer viable to over-design the PDN in order to account for worst case noise. Hence it becomes important to accurately simulate the effects of SSN on the quality of the signal distribution of the system. This requires a simulation framework where the SDN and the PDN of the system can be simulated simultaneously.

This chapter describes a new technique for the co-simulation of the SDN and the PDN in packaged digital systems. The technique captures all the parasitic coupling between the

two modules enabling a combined SI-PI analysis. An added advantage of this method is that it enforces causality on the transient simulation. Causality deals with precise timing of signal propagation through distributed passive structures and is an important problem in the transient simulation of systems. Existing transient simulation techniques fail to enforce causality on the transient simulations. As will be shown in the next chapter, these causality violations can lead to significant error in the signal integrity analysis of high-speed digital systems. This chapter describes a novel causality enforcement technique based on delay extraction from the frequency domain response of passive networks. It is seen that causality enforcement provides better accuracy in the simulation of passive systems. The content in this chapter is organized as follows. Section 4.1 deals with causality enforcement in the transient simulation of passive systems. The section describes the nature of the causality violation problem in transient simulation of passive systems (subsection 4.1.1), explains in detail the extraction of port-to-port delay from the frequency response of passive systems (subsection 4.1.2), and develops a signal flow graph based transient simulation approach that uses the extracted delay to enforce causality on the transient simulations (subsection 4.1.3). Section 4.2 describes the implementation of a fast convolution technique that has been integrated into the transient simulation framework for computational efficiency. The section briefly explains the fast convolution algorithm (subsection 4.2.1), and demonstrates the performance improvement obtained through its implementation (subsection 4.2.2). The section also touches upon some miscellaneous computational aspects involved in the transient simulation using signal flow graphs (subsection 4.2.3). Section 4.3 describes the methodology for the co-simulation of the SDN and the PDN in packaged digital systems. The section describes the procedure for integrating the SDN and the PDN responses of a system into a single model (subsection 4.3.1), and demonstrates the simulation of this integrated model using the framework developed in Sections 4.1 and 4.2 for a simple test case (subsection 4.3.2).

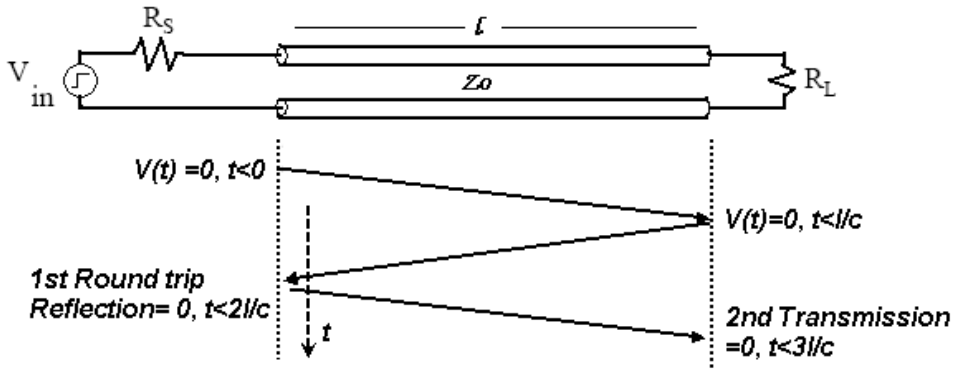

Figure 65: Multiple causality conditions on a transmission line

4.1 Causality enforcement in transient simulation

Causality, which deals with the precise timing of signal propagation through passive structures, is an important problem in the time domain simulation of distributed passive systems. If unaccounted for, it can lead to significant error in the signal integrity analysis of high-speed digital systems. This section describes a novel technique for enforcing causality on the transient simulation of passive systems.

4.1.1 The causality violation problem

At higher frequencies, since the size of passive structures is comparable to the signal wavelength, distributed effects like delay play an important role in the time domain analysis of such structures. These distributed effects imply that there are many causality conditions that need to be satisfied to generate the correct system response in the time domain. As an illustration, Figure 65 shows the multiple causality conditions due to the finite velocity of the electromagnetic waves propagating on a transmission line. As seen from the figure the ene-to-end delay of the transmission line forms the basis for these causality conditions. This delay is given by $t_d = l/c$ where l is the length of the line and c is the velocity of propagation of the electromagnetic waves. A transient analysis of such passive structures invariably involves some form of transformation of the bandlimited frequency response of the structures into the time domain. This transformation is carried out either through direct simulation using frequency domain parameters or through macro-modeling of the frequency domain response. Macro-modeling techniques like the one described in [37] approximate the

bandlimited frequency responses of such passive networks using complex poles and residues which are then translated into lumped element circuits. This bandlimited approximation of the network response is of the form

$$H(s) = \sum_{n=1}^{N} \frac{\alpha_n}{s - \beta_n} + k_d + k_l s \tag{40}$$

where β_n are the complex poles, α_n are the complex residues and $s = j\omega$ where ω is the angular frequency. Once the poles and residues are known, they can be represented in a lumped element circuit form to be used in SPICE. $H(s)$ generated this way is stable if all the poles β_n lie in the left half of the complex s-plane. To ensure passivity of $H(s)$ several methods have been proposed in literature. For instance, the one described in [37] imposes a set of conditions on the residues α_n, k_d and k_l, to ensure that the developed macro-model is passive. Macro-models developed using such techniques satisfy the stability and passivity criteria, but not causality. This is because distributed passive systems have infinite poles, and Equation 40 approximates their response using only a finite number of poles N, extracted using bandlimited frequency response data. This prevents $H(s)$ from accurately capturing distributed effects like delay in the network, since that would require an infinite bandwidth frequency response. As this is not practically possible, the transient simulations performed using such macro-models often violate the causality conditions. A similar effect is seen when bandlimited frequency response data is directly simulated using the network parameters as given in [49]. An example of such a case is shown in Figure 66 where the circuit shown in Figure 65 was simulated using its bandlimited frequency response (1 MHz to 2.5 GHz). The source and load impedances were left mismatched in order to generate reflections. From the figure it can be clearly seen that the signal propagating through the transmission line reaches the far end earlier than the delay of the line. This is theoretically impossible and is a violation of the network causality. Similar effects are seen for the reflections that follow the incident wave. Such causality violations compromise the accuracy of the signal integrity analysis and pose a problem in the accurate transient simulation of high speed systems.

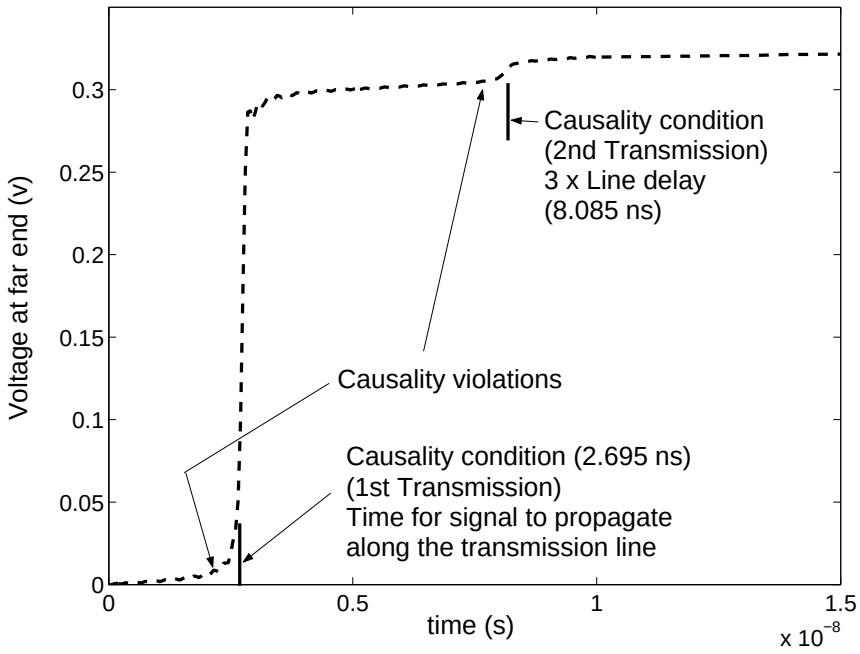

Figure 66: Causality violations in transient simulation of a transmission line

4.1.2 Delay extraction from frequency response of passive networks

It can be seen from Figure 65 that the port-to-port delay in a passive system forms the basis of its causality conditions. Extracting this delay from the frequency response is the first step towards enforcing causality on the transient simulation of passive networks. Passive networks simply absorb, transfer and dissipate electrical energy provided to them and are limited by their inability to amplify signals. This results in passive responses having minimum phase that can be used to extract the delay embedded in these networks. To understand the concept of minimum phase [43] consider a one-port passive network with impedance parameter $Z11(s)$ where $s = j\omega$ and ω is the angular frequency. If the system is stable then all the poles of $Z11(s)$ lie in the left half of the complex s-plane. Now the same system can also be represented using the admittance parameter $Y11(s)$ where $Y11(s) = 1/Z11(s)$. Since the system is stable, all the poles of $Y11(s)$ also lie in the left half of the complex s-plane. However, since the poles of $Y11(s)$ are the zeros of $Z11(s)$ and vice-versa, all the poles and zeros of $Z11(s)$ and $Y11(s)$ lie in the left half of the complex s-plane. This property constrains the phase response of the system such that

$-\pi < \angle Z11(s) < \pi$ and $-\pi < \angle Y11(s) < \pi$. Such a system is called a minimum phase system and $Z11(s)$ and $Y11(s)$ are called minimum phase functions. The phase response of such functions does not show any phase transition.

In multi-port passive networks, this property of minimum phase is observed only for the self-responses i.e., only for the diagonal elements of the system matrix. Consider a 2-port passive network represented using impedance parameters

$$Z(s) = \begin{bmatrix} Z11(s) & Z12(s) \\ Z21(s) & Z22(s) \end{bmatrix} \tag{41}$$

In this system only $Z11(s)$ and $Z22(s)$ are minimum phase functions. The transfer impedances $Z12(s)$ and $Z21(s)$ are stable but do not exhibit minimum phase. This is because of the port-to-port delay embedded in these transfer impedance responses. Let Td be the delay between ports 1 and 2 in the above system. Then $Z12(s)$ can be written as

$$Z12(s) = Z12'(s)e^{-sTd} \tag{42}$$

According to linear system theory [43] any stable system function can be represented as a product of a minimum phase function and an all-pass function, where an all-pass function is one whose magnitude is unity over the entire frequency range. Therefore

$$Z12(s) = Z12_{\min}(s).Z12_{AP}(s) \tag{43}$$

Comparing equations 42 and 43 and noting that e^{-sTd} has unity magnitude, it can be seen that if $Z12(s)$ is separated into a product of a minimum phase function and an all-pass function, the all-pass function will represent the delay between the two ports. This separation can be performed using the Hilbert Transform [43].

The Hilbert Transform relates the magnitude and phase of a minimum phase function $H_{\min}(j\omega)$ through the equation

$$\angle[H_{\min}(j\omega)] = -\frac{1}{2\pi}\mathrm{P}\int_{-\pi}^{\pi} \log|H_{\min}(j\theta)| \cot\left(\frac{\omega-\theta}{2}\right) d\theta \tag{44}$$

where P is the Cauchy Principal value. Since an all-pass function has unity magnitude, the magnitude response of the minimum phase function $Z12_{\min}(s)$ in Equation 43 is the same

as that of $Z12(s)$. Therefore the port-to-port delay Td embedded in the transfer impedance parameter $Z12(s)$ can be determined as follows

$$|Z12_{\min}(j\omega)| = |Z12(j\omega)| \tag{45}$$

$$\angle[Z12_{\min}(j\omega)] = -\frac{1}{2\pi}\mathrm{P}\int_{-\pi}^{\pi} \log|Z12(j\theta)| \cot\left(\frac{\omega-\theta}{2}\right) d\theta \tag{46}$$

$$Z12_{AP}(j\omega) = \frac{Z12(j\omega)}{Z12_{\min}(j\omega)} = e^{-j\omega Td} \tag{47}$$

$$Td = -\frac{\arg(Z12_{AP}(j\omega))}{\omega} \tag{48}$$

This technique can be used to determine the delay from the S, Y or Z parameter representation of a passive system.

4.1.2.1 Examples illustrating delay extraction

To demonstrate the proposed technique, a power/ground PCB plane pair was analyzed using the cavity resonator method [18] to obtain its Z-parameter representation. The plane pair was 25cm x 25cm with 8mil separation and the two ports on the network were located at (1.67,2.33)cm and (22.67,2.33)cm respectively. Using the velocity of propagation of electromagnetic waves in a dielectric medium, the delay between the two ports was found to be about 1.5ns. Next, the proposed technique was used to determine the delay between the two ports in the network. Starting with the Z-parameters, Figures 67 and 68 show the comparison between the magnitude and phase responses of $Z11$ and $Z12$. From the phase response, it can be easily inferred that $Z11$ is a minimum phase response as against $Z12$ which has two phase transitions. Using Equation 45 through Equation 48 $Z12$ was separated into a minimum phase function $Z12_{min}$ and an all-pass function $Z12_{AP}$. The magnitude and phase responses for $Z12_{min}$ and $Z12_{AP}$ are shown in Figures 69 and 70. Since $Z12_{AP}$ is of the form e^{-sTd} the port-to-port delay Td can be computed as the negative gradient of the phase of $Z12_{AP}$. The minor deviations from the ideal magnitude and phase responses of $Z12_{AP}$ seen in Figures 69 and 70 can be eliminated by averaging. The delay thus determined was found to be 1.517ns, which is in good agreement with the theoretical value.

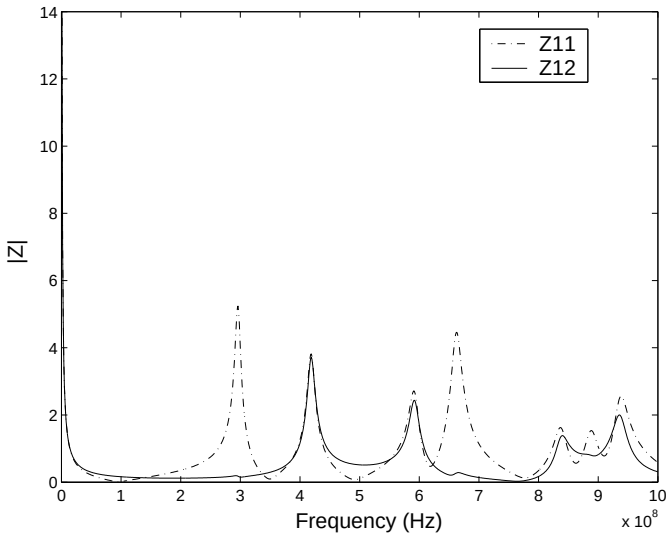

Figure 67: Z-parameter magnitude response for the plane

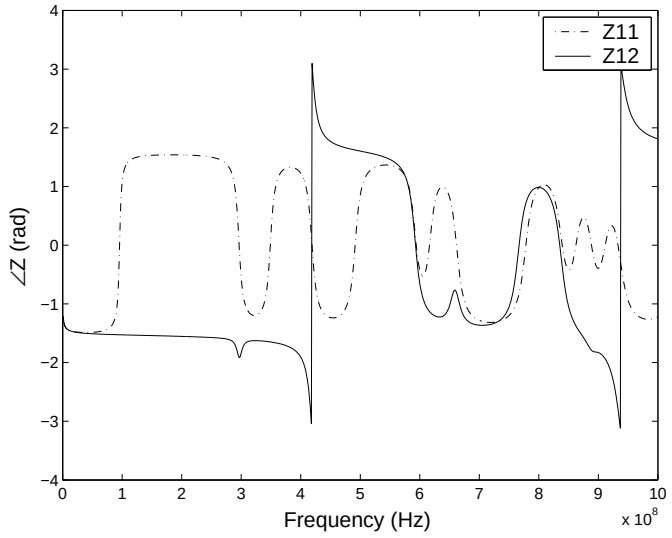

Figure 68: Z-parameter phase response for the plane

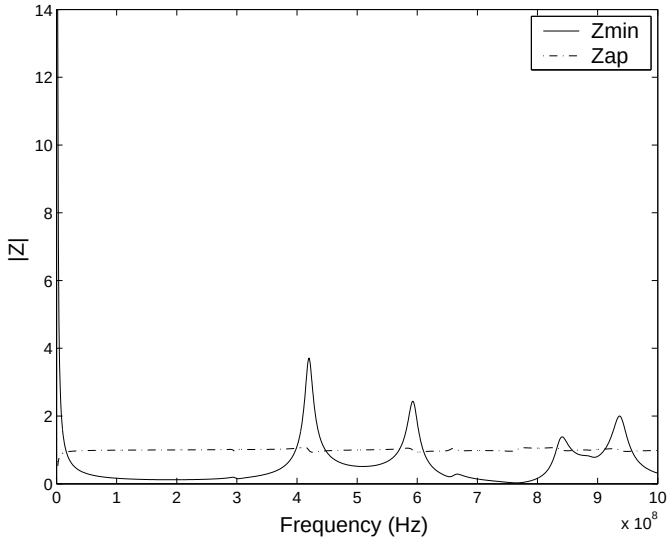

Figure 69: Magnitude response for $Z12_{min}$ and $Z12_{AP}$

Table 4: Delay extraction for differential transmission lines

	Measured		Extracted	
	Even	Odd	Even	Odd
Microstrip	230ps	239ps	230.5ps	236.8ps
Stripline	247ps	247ps	243.3ps	242.6ps
Buried microstrip	229ps	240ps	227.7ps	237ps

In another illustration of the delay extraction technique, the 4-port S-parameter measurements of a variety of differential transmission line structures were processed to extract their respective delays. For differential structures, the scattering parameters are first transformed into mixed mode parameters followed by their separation into minimum phase and all-pass components to get even and odd mode delays. A brief description of conversion of 4-port S-parameters into mixed mode S-parameters is given in Appendix B. The extracted delay values were compared with the delays observed using the TDT waveform computed through Agilent's PLTS system. The comparison chart is shown in Table 4. As seen from the chart, the measured and extracted delay values are in good agreement.

4.1.3 Causality enforcement using signal flow graphs

Signal flow graphs (SFGs) have been previously used in the transient simulation of passive systems [49]. One of the key advantages they provide is that it is possible to perform transient simulation without any kind of approximation/interpolation of the frequency response

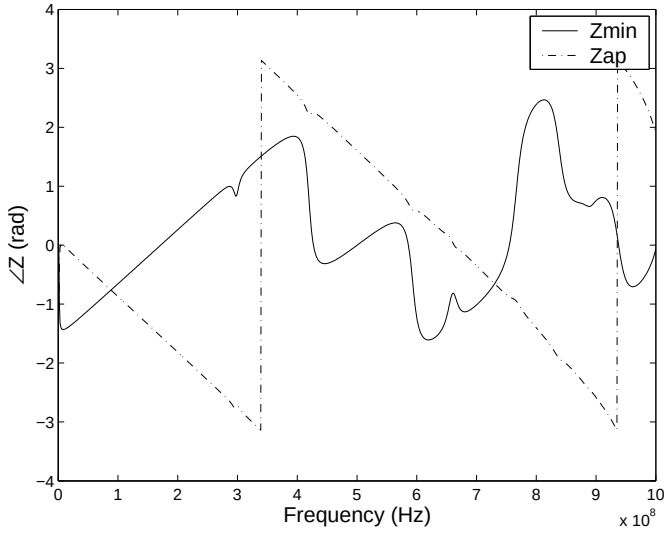

Figure 70: Phase response for $Z12_{min}$ and $Z12_{AP}$

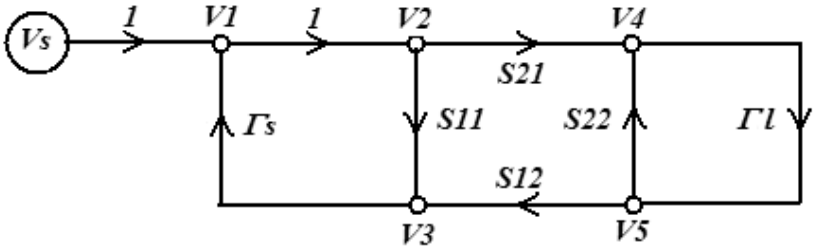

Figure 71: Signal flow graph of the transmission line circuit

data. Since this approximation step is a key bottleneck for the scalability of macro-modeling techniques, signal flow graphs are capable of handling larger sized simulation problems. In order to demonstrate the enforcement of causality on transient simulation using signal flow graphs, consider the SFG of transmission line circuit shown in Figure 65. The SFG, shown in Figure 71, results in a system of equations which need to be solved in order to generate the transient response of the circuit. These equations are given as

$$V_1(t) = V_S(t) + V_3(t) \otimes \Gamma_S \tag{49}$$

$$V_2(t) = V_1(t) \tag{50}$$

$$V_3(t) = V_2(t) \otimes s11(t) + V_5(t) \otimes s12(t) \tag{51}$$

$$V_4(t) = V_2(t) \otimes s21(t) + V_5(t) \otimes s22(t) \tag{52}$$

$$V_5(t) = V_4(t) \otimes \Gamma_L \tag{53}$$

where $s11(t)$, $s12(t)$, $s21(t)$ and $s22(t)$ are the respective impulse responses of the transmission line structure. From the delay extraction technique it is evident that $s12(t)$ and $s21(t)$ are each composed of a minimum phase component and an all-pass component where the all-pass component determines the port-to-port delay. This indicates that a voltage change at $V2$ does not reach $V4$ for a time period given by the delay. A similar case can be made for the voltage change at $V5$ affecting the voltage $V3$. These conditions can be used to rewrite the Equation 51 and Equation 52 as

$$V_3(t) = V_2(t) \otimes s11(t) + V_5(t - Td) \otimes s12_{\min}(t) \tag{54}$$

$$V_4(t) = V_2(t - Td) \otimes s21_{\min}(t) + V_5(t) \otimes s22(t) \tag{55}$$

where $s12_{min}(t)$ and $s21_{min}(t)$ are the transfer impulse responses of the transmission line after the delay portion has been removed. This new system of equations explicitly enforces the delay and the resulting transient simulation satisfies the causality conditions. The transient simulation of the circuit in Figure 65 using causal signal flow graph equations results in the waveform shown in Figure 72. It is seen by comparing Figure 72 with Figure 66 that the transient output obtained using causal SFG equations satisfies all causality conditions. This results in a more accurate transient simulation as compared to macro-modeling or direct S-parameter simulation based techniques.

4.1.3.1 Passivity preservation in SFG based causal transient simulation

An important consideration in the transient simulation technique using SFGs is the preservation of the passivity property of the original frequency data. Since this method involves no form of approximation/interpolation of the original data, the passivity violations are minimized. To double-check this, after the impulse responses have been computed and causality has been enforced, the data is converted back to the frequency domain and swept for eigenvalues violations using the criterion

$$\min(eigenvalue(I - SS^H)) \geq 0 \qquad \forall \quad \omega \tag{56}$$

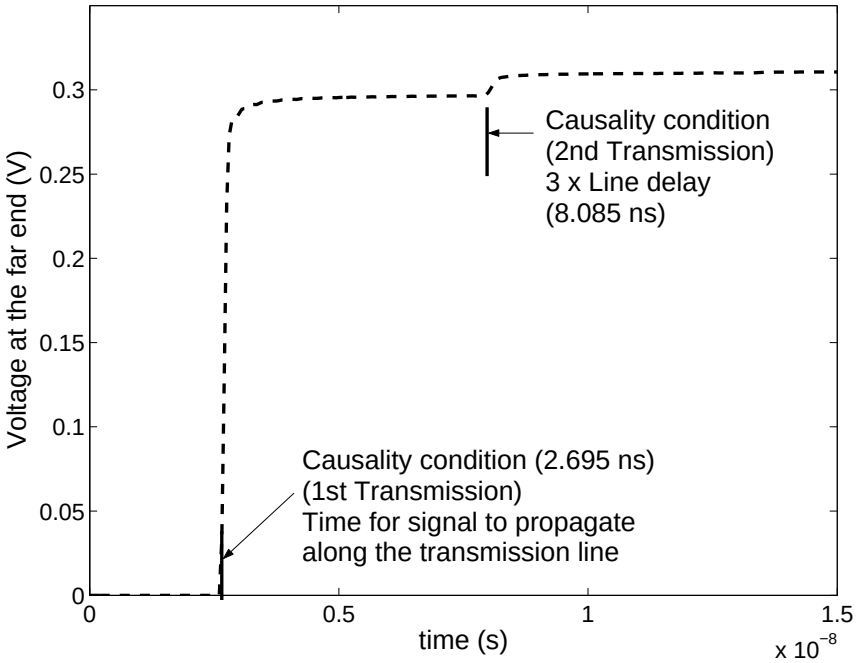

Figure 72: Causal transient simulation of the transmission line circuit

where I is the identity matrix and H is the Hermetian operator. The eigenvalue plot is shown in Figure 73. From the figure it is seen that the causality enforcement process does not violate the passivity of the original data. However this procedure simply checks for passivity violation and does guarantee a passive transient simulation. Finding closed form expressions for guaranteeing passivity in delay extracted-multiport frequency response data is an area open for future research.

4.2 Implementation of fast convolution

The solution to the set of causal signal flow graph equations at each time step requires the evaluation of the convolutions seen on the right hand side of the individual equations respectively. If the source and load terminations are resistors as in the case of the circuit in Figure 65, then Γ_S and Γ_L are just one sample in length and their convolution simplifies down to a single multiplication. However for the above 2-port signal flow graph, the four convolutions given in Equations 54 and 55 still need to be evaluated at each time step. Generalizing this observation, the simulation of an N-port S-parameter network using signal flow graphs will require at least N^2 convolutions to be performed to setup the system matrix

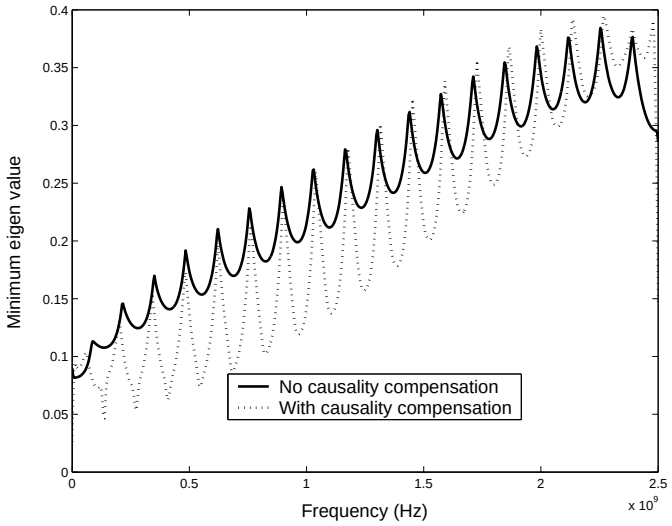

Figure 73: Minimum eigenvalue plot with and without causality enforcement

for each time step. Since discrete convolution performed using the conventional multiply-and-add algorithm is a computationally expensive process, it bottlenecks the efficiency of the SFG based simulation approach for systems with a large number of ports.

The conventional implementation of the convolution integral has an $O(N^2)$ computational efficiency where N is the time of simulation. To improve the simulation efficiency for large sized problems, this section describes a fast convolution technique that has been implemented and integrated into the SFG based transient simulation framework. Several techniques have been proposed in literature that address the problem of improving the computational efficiency of the convolution integral [8][41][16][28]. Amongst these [8] is based on number theoretic transforms and requires prior knowledge of the both the sequences involved in the convolution. Hence this technique cannot be used in a SFG based framework which proceeds one time-step at a time. [41] uses recursive convolution that requires rational function approximation of the frequency response of the network being simulated. Since rational function approximation itself is limited by the network-size (rational function approximation of a large network is often an ill-condition problem [37]) this technique is unsuitable for simulating large sized networks. [16] and [28] describe fast convolution techniques based on the partitioning of the network impulse responses. These techniques are supposed to improve the computational efficiency to $O(Nlog^2N)$ for [16] and $O(NlogN)$

for [28], and are suitable for integration into an SFG based simulation framework. Since [28] provides the better performance improvement of the two, it has been integrated into the causal transient simulation technique developed in the previous section. However this algorithm is defined for infinite length impulse responses. Since the SFG based simulation technique developed in this dissertation uses finite impulse responses, the algorithm from [28] has been modified accordingly. The following subsection briefly describes the modified algorithm.

4.2.1 Fast convolution using Lagrange approximation

Let $y(t)$ be the convolution result obtained using a time domain signal $x(t)$ and an impulse response $h(t)$. Then $y(t)$ is denoted as $y(t) = x(t) \otimes h(t)$ and is given by

$$y(t) = \int_{-\infty}^{t} h(t-\tau)x(\tau)d\tau \tag{57}$$

In the discrete time domain with finite length impulse responses, this convolution integral is implemented as

$$y(t_n) = \sum_{i=n-l}^{n-1} h(t_n - t_i)x(t_i)\Delta t \tag{58}$$

where t_n is the time at which the convolution is being computed, l is the length of the impulse response, and Δt is the interval between consecutive time samples. The fast convolution method described in [28] decomposes this summation into two parts given as

$$y(t_n) = \sum_{i=n-l}^{s} h(t_n - t_i)x(t_i)\Delta t + \sum_{i=s+1}^{n-1} h(t_n - t_i)x(t_i)\Delta t \tag{59}$$

where $n - l < s < n - 1$. In [28] the first part of the summation is computed using Lagrange interpolation while the second part is computed using the conventional convolution algorithm. For real world systems that are lossy, the variations in $h(t)$ become lesser and lesser as $t \to \infty$. This is shown in Figure 74 which shows a typical $h(t)$ for a lossy passive network. In Figure 74, a point s can be chosen on the time axis such that most of the energy in $h(t)$ lies in the darker shaded region. Now if $h(t)$ is to be convolved with an input signal $x(t)$ as shown in Figure 75, the portion of the convolution from the darker shaded region (which corresponds to the second summation in Equation 59) will have a much higher

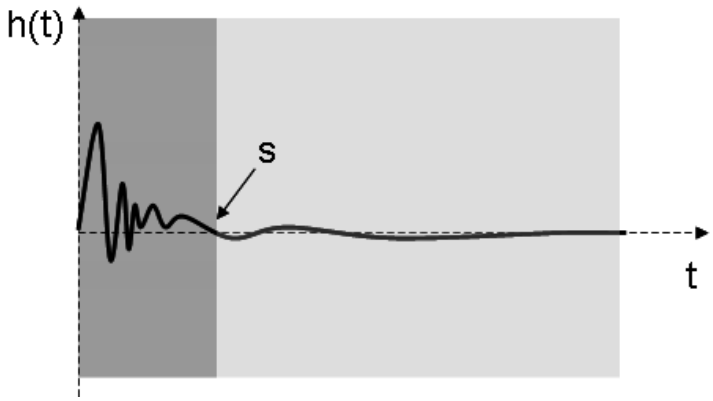

Figure 74: A typical impulse response for a lossy passive network

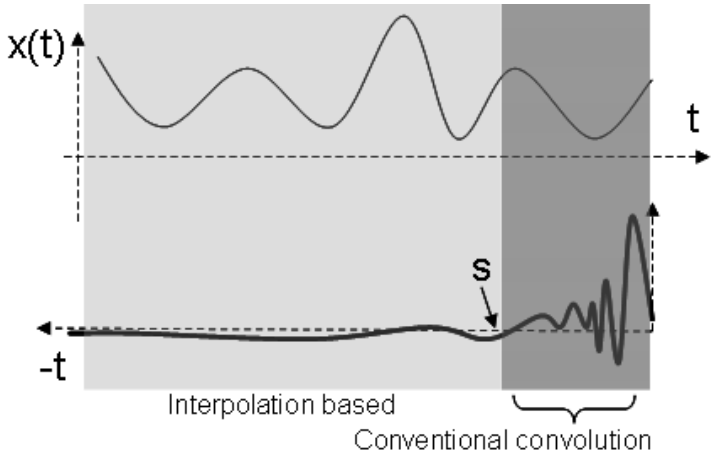

Figure 75: Fast convolution using impulse response partition

value as compared to that from the lighter shaded region (which corresponds to the first summation in Equation 59). This property will remain true even as $x(t)$ changes as $y(t)$ is computed for successive values of t. Also since $h(t)$ itself has minimal variation in the lighter shaded region, the variation in the contribution of the first summation in Equation 59 for successive values of t will be relatively smaller. The fast convolution algorithm makes use of this property by computing the first summation in Equation 59 for only certain discrete points over a block of time and then using Lagrange interpolation for calculating it at each time step t over that block of time.

Now, consider that $y(t_n)$ has been evaluated till t_a. Let $t_b - t_a = n - s - 1 = q$ be the

length of a time block over which $y(t_n)$ has to be computed. Let

$$g(t_n) = \sum_{i=s+1}^{n-1} h(t_n - t_i)x(t_i)\Delta t \tag{60}$$

denote the contribution by the first summation from Equation 59. It is seen the for $t_a < t_n < t_b$, all values required for the computation of $g(t_n)$ are already known. However $g(t_n)$ need not be computed for each time step. Instead we express the signal $h(t - t_i)$ in terms of a Lagrange basis as

$$h(t - t_i) = \sum_{m=1}^{p} \mu_m(t)h(c_m - t_i) \tag{61}$$

where μ_m is the m^{th} Lagrange polynomial of degree $p - 1$ and c_m are Chebyshev nodes given by

$$c_m = \frac{t_a + t_b}{2} + \frac{t_b - t_a}{2} \cos \frac{(2m - 1)\pi}{2p} \tag{62}$$

Using this expansion $g(t)$ can be represented as

$$g(t) = \sum_{i=n-l}^{s} (\sum_{m=1}^{p} \mu_m(t)h(c_m - t_i))x(t_i)\Delta t \tag{63}$$

Interchanging the order of the summation in Equation 63 yields

$$g(t) = \sum_{m=1}^{p} \mu_m(t) \sum_{i=n-l}^{s} h(c_m - t_i)x(t_i)\Delta t \tag{64}$$

Now if we define ψ_m given by

$$\psi_m = \sum_{i=n-l}^{s} h(c_m - t_i)x(t_i)\Delta t \tag{65}$$

we get

$$g(t) = \sum_{m=1}^{p} \mu_m(t)\psi_m \tag{66}$$

where ψ_m is simply the value of $g(c_m)$. Hence the computation of each value of $g(t_n)$ requires only $O(p)$ operations. Since the computation of each ψ_m requires $O(k)$ operations where $k = s - n - l + 1$, the computation of $g(t_n)$ for all q values in the block requires $O(pq + kp)$ operations. In comparison with this a "direct convolution" implementation to obtain all q values requires $O(qk)$ operations. Since the impulse responses of realistic passive networks become "smooth" as $t \to \infty$ it is found that the typical value of p required to achieve a desired accuracy in the evaluation of $g(t_n)$ is much much smaller as compared to k. When this is true, the proposed approach for implementing convolution is much faster.

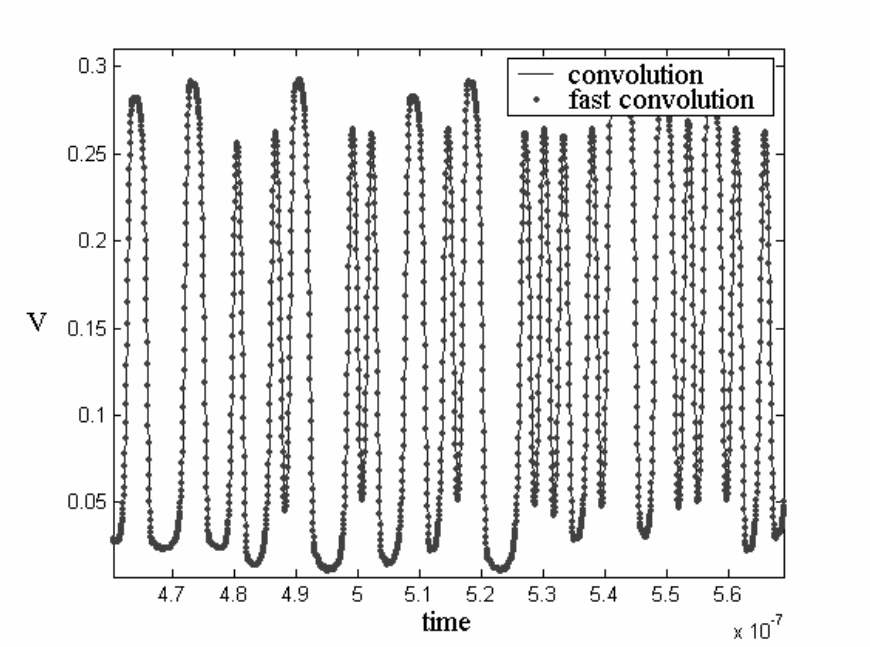

Figure 76: Accuracy of the fast convolution method for a single transmission line system

4.2.2 Performance analysis of the fast convolution algorithm

To gauge the performance improvement achieved in transient simulation by implementing convolution using the above algorithm, a simple microstrip transmission line circuit was designed and simulated. The specifications of this circuit are discussed in detail in the next chapter, which deals with signal integrity using transient simulation. For now it is sufficient to know that the transmission line circuit was decomposed into its signal flow graph that was solved to obtain the transient output of the circuit. The SFG equations were solved using both the conventional convolution implementation and the fast convolution implementation. A comparison of the outputs obtained using the two techniques is shown in Figure 76. From the figure it is seen that the two methods give virtually identical results. Because of the approximation used in the algorithm, some error does creep into the result. This can be seen in Figure 77 where the transient outputs are magnified around one of the peaks. However this error is negligible and can controlled using the number of Lagrange bases used in the algorithm. Thus the fast convolution algorithm performs satisfactorily in preserving the accuracy of the simulation result. As the number of bases used is increased, the error in the simulation reduces at the cost of a reduction in the speedup obtained. For the transmission

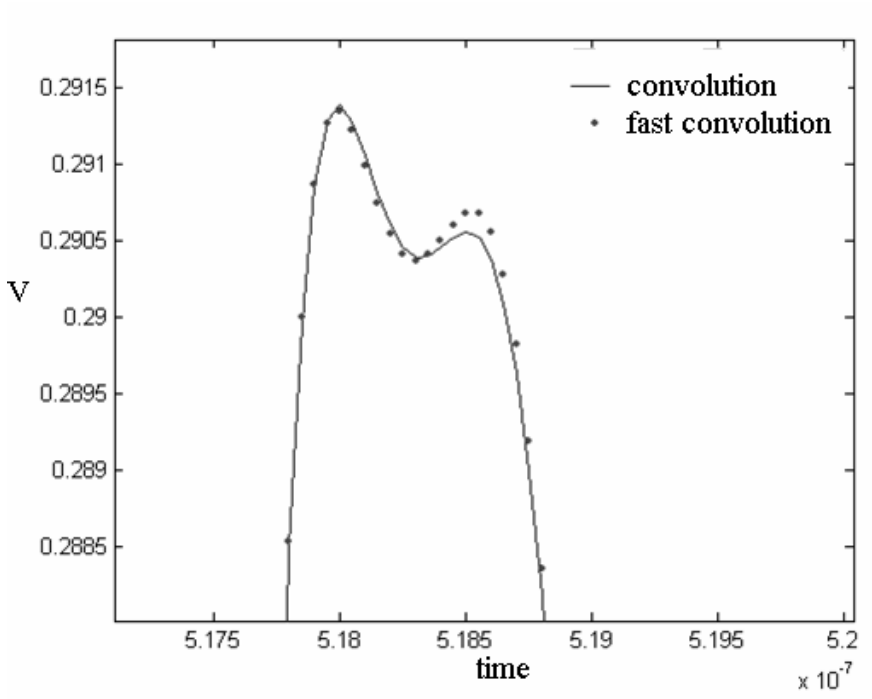

Figure 77: Magnification around one of the signal peaks from Figure 76

line circuit being simulated, the trade-off between the error introduced in the simulation and speedup obtained using the fast convolution algorithm is shown in Figures 78 and 79. It is seen that the fast convolution implementation provides about 30-40% speedup for a reasonably low error of less than 0.5%. A slight increase in error is seen for the cases using 40 and 45 basis functions respectively. This could either mean that there exists an optimal number for the basis functions to achieve minimum error or more likely the observation could just be due to some abnormal property of this particular system. In general (as will be seen for the next case), as the number of basis functions increase, the error curve is seen to flatten out but not climb up. One of the reasons for the relatively modest speedup for this case could be the fact that the circuit being simulated is relatively small. If a large sized system is simulated, where thousands of convolutions need to be performed at each time step, the performance improvement obtained using fast convolution would be more perceptible. To verify this a 64-bit interconnect bus referenced to a non-ideal PDN was simulated using SFGs. The specifications for this system are also given in the next chapter where the test case is discussed in detail. In general for a N-port network, an SFG

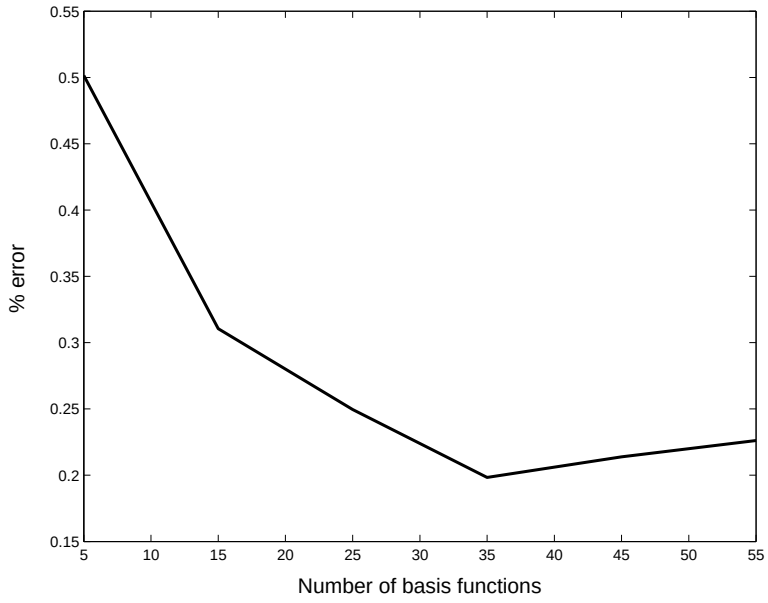

Figure 78: Error tradeoff for the fast convolution algorithm

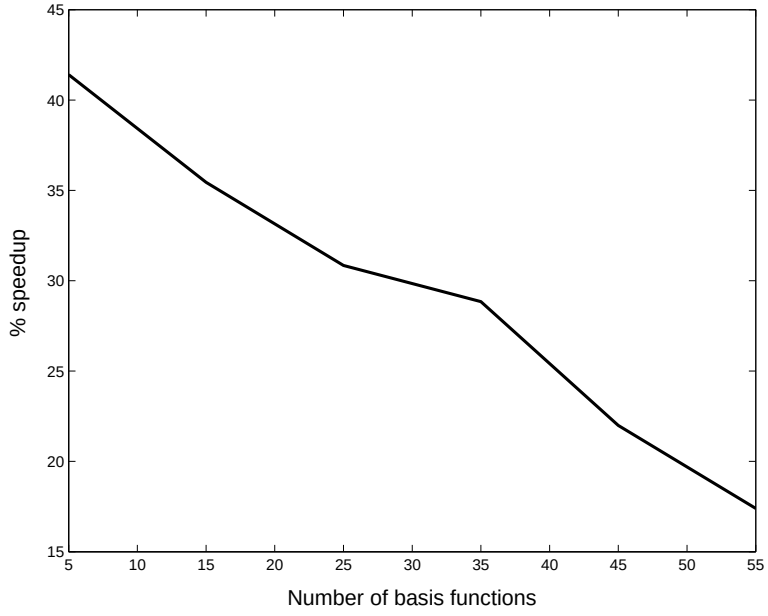

Figure 79: Speedup obtained using the fast convolution algorithm

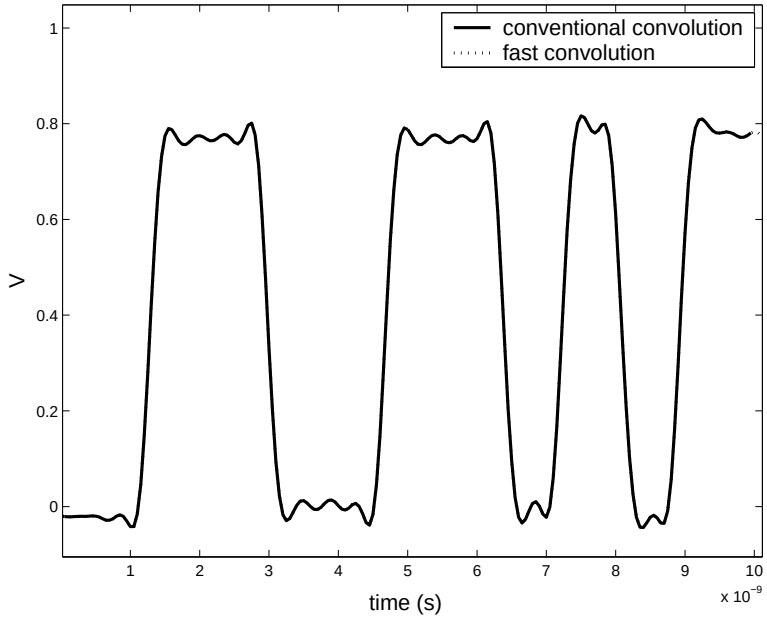

Figure 80: Transient simulation of a 130-port network using fast convolution

based simulation requires the computation of atleast N^2 convolutions at each time step. The system under consideration resulted in a 130-port network that was simulated using SFGs. A comparison of the outputs obtained on one of the interconnects using conventional convolution and fast convolution is shown in Figure 80. The output waveforms are seen to virtually overlap one another. The tradeoff between the error introduced by fast convolution and the speedup provided by it is shown in Figures 81 and 82 respectively. It can be clearly seen that for larger problem sizes, the fast convolution approach provides about 250-280% speedup. Since the simulation times for large sized systems run into hours, this kind of speedup can prove extremely valuable. Finally, Figure 83 plots the time-line of the two convolution methods for simulating the response of the 130-port network for a period of 70 ns. The y-axis plots the time taken in minutes to perform the convolutions. The plot for the fast convolution approach clearly shows its block-based nature. It is seen that for each block the algorithm requires a setup time where it needs to compute the coefficients of the Lagrange bases. However once this is done, the simulation progresses much faster as compared to conventional convolution.

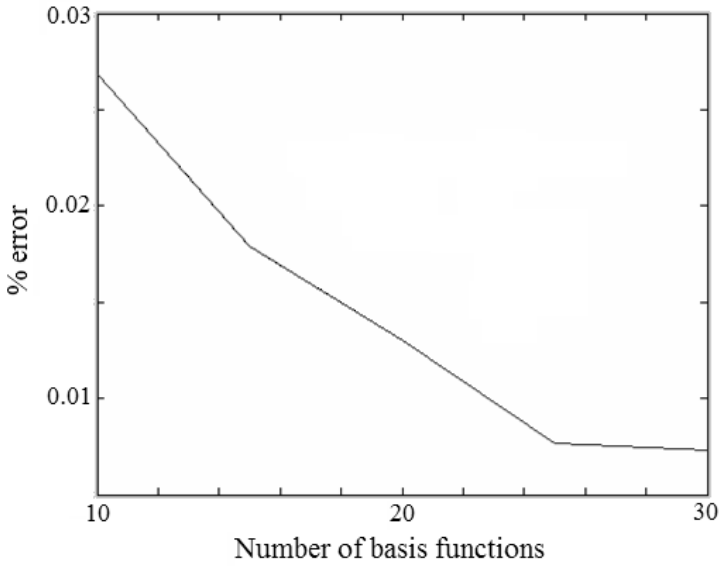

Figure 81: Error tradeoff for the 130-port network simulation

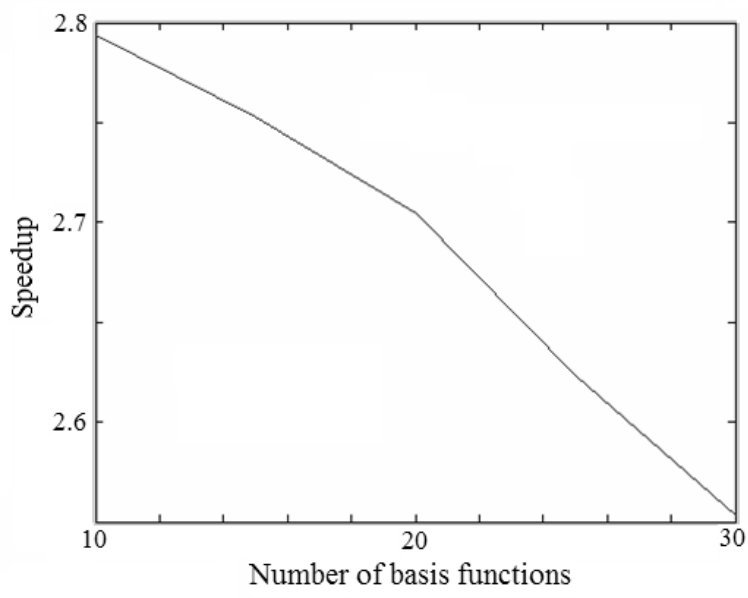

Figure 82: Speedup obtained for the 130-port network simulation

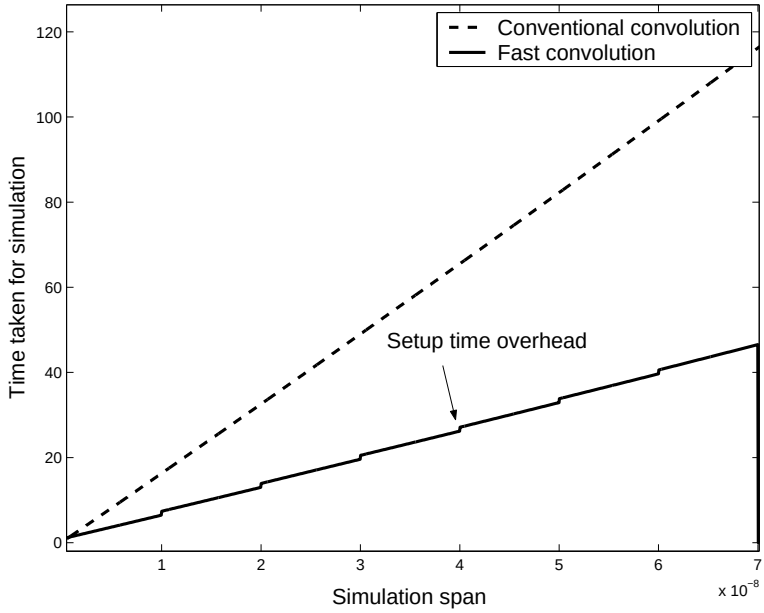

Figure 83: Time-lines of the simulation progress using normal convolution and fast convolution

4.2.3 Miscellaneous computational aspects in the SFG based transient simulation

An SFG based transient simulation performed using frequency domain network parameters poses several computational challenges. Following are some important issues that need to be given careful consideration while developing the SFG based transient simulation framework.

4.2.3.1 Inverse Z-Transform

One of the considerations in transient simulation using SFGs is the need to convert bandlimited frequency domain data of multi-port passive networks into their impulse responses. The simplest way to perform this transformation is using the Fast Fourier Transform (FFT) as given in [43]. However the FFT algorithm requires frequency data at equal intervals all the way from DC up to the sampling frequency. This is often not available in real cases. For example if the S-parameter data is obtained using measurements, then the DC and low frequency data is not available. To circumvent this problem, the SFG simulation technique developed in this dissertation uses the Inverse Z-Transform (IZT) [43]. The IZT is in fact a generalized version of the FFT. The IZT allows for arbitrary location of the frequency samples in the data and hence can be used even with measured S-parameter data. The

Z-Transform of a transient data sequence is given by

$$X(z) = \sum_{n=-\infty}^{\infty} x[n]z^{-n} \tag{67}$$

Hence to recover a transient data sequence (impulse response) back from the frequency response, a matrix equation of the following form needs to be solved.

$$\begin{bmatrix} Z(\omega_1) \\ : \\ Z(\omega_k) \end{bmatrix} = \begin{bmatrix} 1 & \omega_1^1 & \omega_1^n \\ : & : & : \\ 1 & \omega_k^1 & \omega_1^n \end{bmatrix} \begin{bmatrix} x[0] \\ : \\ x[n] \end{bmatrix} \tag{68}$$

Therefore the flexibility provided by the IZT comes at a cost. The IZT requires a matrix inversion to compute each impulse response as against the FFT which requires just a bunch of multiplications. However it can be seen from Equation 68 that the matrix to be inverted (called the Vandermonde matrix) depends only on the locations of the frequency samples (ω_k) in the S-parameter data. This means that this matrix can be inverted once and then stored for computing all the impulse responses.

4.2.3.2 Windowing

Another important consideration while obtaining the impulse response of a network using bandlimited frequency domain data is the abrupt change in the frequency response at the edges of the band. Such changes in the frequency response can lead to spurious spikes or oscillations in the computed impulse response. To suppress these effects windowing has been used in the signal processing domain. Windowing involves multiplication of the bandlimited frequency data with a suitably generated window before it is converted into the impulse response using IZT. Impulse responses obtained using windowed frequency data show reduced spurious spikes and oscillations. However windowing a frequency response using a higher order window (window with a very sharp cut off) results in inaccuracies in the impulse response especially at high frequencies. Hence there is always a tradeoff involved in window selection. Kaiser windows [43] have been extensively used in the past to perform such windowing. They are relatively easy to generate using the function

$$w[n] = \begin{cases} \frac{I_0[\beta(1-[(n-\alpha)/\alpha]^2)^{1/2}]}{I_0\beta} & 0 \leq n \leq M \\ 0 & otherwise \end{cases} \tag{69}$$

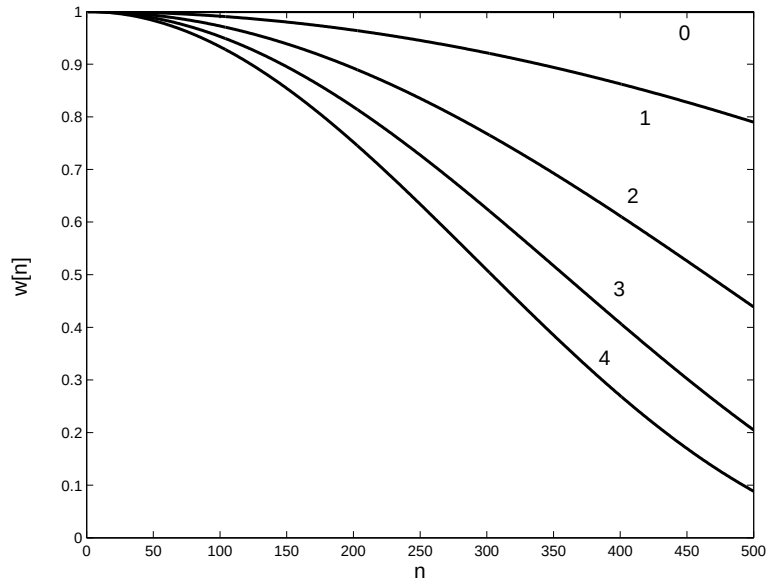

Figure 84: Kaiser windows with different shape parameters

where $\alpha = M/2$, β is the shape parameter and $I_0(.)$ represents the zeroth order modified Bessel function of the first kind. Figure 84 shows a few Kaiser windows of increasing shape parameters. For most of this work, Kaiser windows with shape parameters of 1 or 2 were used on the frequency data.

4.3 Transient co-simulation of passive systems

The previous two sections of this chapter develop a transient simulation framework wherein the S-parameters of a multi-port passive network can be simulated for arbitrary excitations. This section describes how the SDN and the PDN in a digital system can be simulated using this framework. The flowchart for the simulation approach is shown in Figure 85. Once the layout of a package or a PCB is available, the post-layout simulation phase begins by performing a layout extraction to obtain the layouts of the signal and the power networks. Once these layouts are obtained, they are modelled using several existing modeling techniques. The PDN can be modelled using either the Transmission Line Method [40], [50] that uses a two dimensional array of transmission lines or distributed RLGC elements in SPICE, or the cavity resonator method [38], [39], or the Transmission Matrix Method [30],

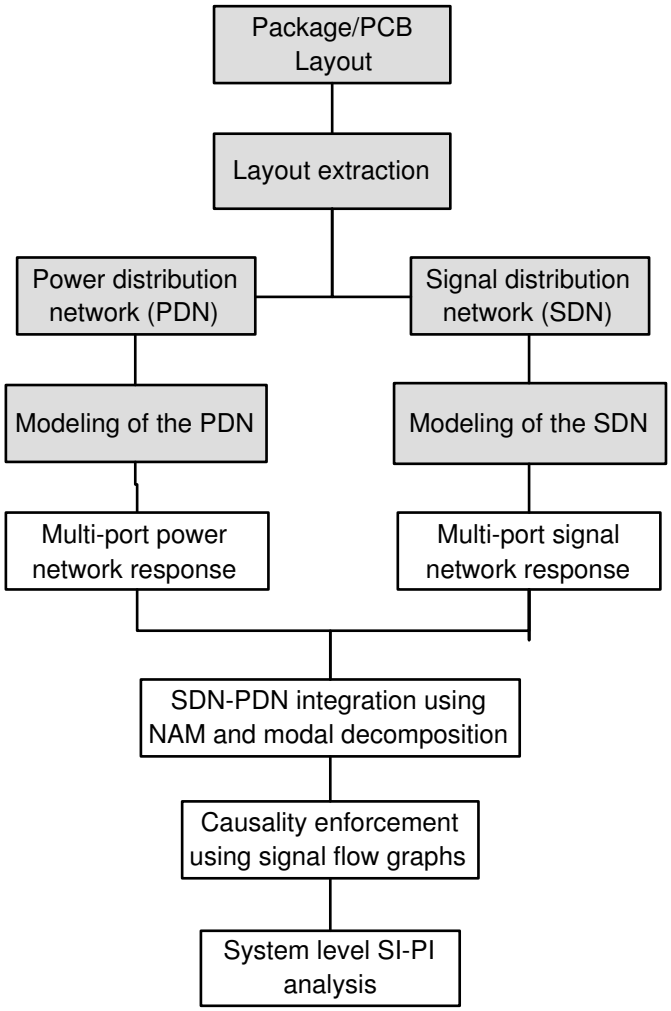

Figure 85: Flow chart of the SDN-PDN co-simulation methodology

[29], [31]. Similarly the SDN can be modelled using W-element models [42] or using non-physical RLCG models [32]. Using these modeling techniques, multiport responses of the SDN and the PDN can be obtained in the frequency domain. These are usually in terms of the S, Y, or Z parameters of the networks. All the steps involved in the flow chart until this point are based on techniques already existing in literature. That is indicated by boxes shaded in gray in Figure 85. Once these multiport responses are available the co-simulation methodology described in this section proceeds by integrating them into a single network. This integration has to accurately capture all the parasitic coupling between the two networks. The integrated multiport network thus formed is then reduced and simulated using the SFG based simulation technique described in Section 4.1. The simulation results thus obtained capture all the system parasitics and can be analyzed using tools like eye-diagram generation to gain insight into the signal integrity and the power integrity performance of the system.

4.3.1 Integration of the SDN and the PDN

The integration of the SDN and the PDN frequency response parameters is carried out in the frequency domain using matrix based techniques like the Nodal Admittance Method and the Stamp rule [20] [51]. A brief description of the Nodal Admittance method and the Stamp rule is given in Appendix C. The integration ensures that all parasitic effects due to the non-ideal nature of the PDN and the coupling between the PDN and the SDN are accurately accounted for in the transient simulation. As an example consider a simple circuit having a microstrip transmission line referenced to a pair of power ground planes. If the SDN and the PDN of this system are separated, the SDN will consist of a microstrip line referenced to ideal ground. The PDN will consist simply of the two power/ground planes. In the above system, consider a pair of ports on the power/ground plane pair right under the near and far ends of the transmission line. Now using existing modeling techniques, the two port frequency responses of the SDN and the PDN can be computed. Assume those to be the two port admittance responses (Y-parameters) for this case. In this kind of a structure, the TEM wave propagation can be broken into two modes [24], a transmission line mode

which propagates between the microstrip line and the ideal ground, and the parallel plate mode which propagates between the power/ground plane pair. Since for this system, the transmission line and parallel-plate modes are not coupled, the integration of the SDN and the PDN responses can be carried out by simply combining the two Y-matrices as given by

$$\begin{bmatrix} I_p^i \\ I_p^o \\ I_m^i \\ I_m^o \end{bmatrix} = \begin{bmatrix} Y_p & 0 \\ 0 & Y_m \end{bmatrix} \begin{bmatrix} V_p^i \\ V_p^o \\ V_m^i \\ V_m^o \end{bmatrix} \tag{70}$$

where Y_p and Y_m are the Y-matrices of the power/ground planes and the microstrip interconnect (considering ideal reference) respectively, while I and V are the vectors defining the currents and the voltages at the input (near-end) and output (far-end) ports.

However if the SDN consisted of a stripline interconnect, then the transmission line mode and the parallel plate modes in the structure would be coupled. In that case, modal decomposition techniques will have to be incorporated to accurately integrate the SDN and the PDN responses. For a stripline transmission line referenced to non-ideal power/ground planes the integration of the SDN and the PDN using modal decomposition [23] is given by

$$\begin{bmatrix} I_p^i \\ I_p^o \\ I_m^i \\ I_m^o \end{bmatrix} = \begin{bmatrix} k^2Y_s + Y_p & kY_s \\ kY_s & Y_s \end{bmatrix} \begin{bmatrix} V_p^i \\ V_p^o \\ V_m^i \\ V_m^o \end{bmatrix} \tag{71}$$

where Y_p and Y_s are the Y-matrices of the power/ground planes and the stripline (considering ideal reference) respectively, and k is constant determined from the layout. Once the integration is complete, line terminations and other lumped components in the system can be added to the overall system matrix using the stamp rule [20][51]. Since the transient response is often required only at particular locations in the system, the overall system matrix can be reduced to include ports only at those locations where the system is being excited or probed. For a m-port overall system matrix that needs to be reduced to n (external) ports, the m-port Y-matrix is reordered such that the desired n port locations appear in the top

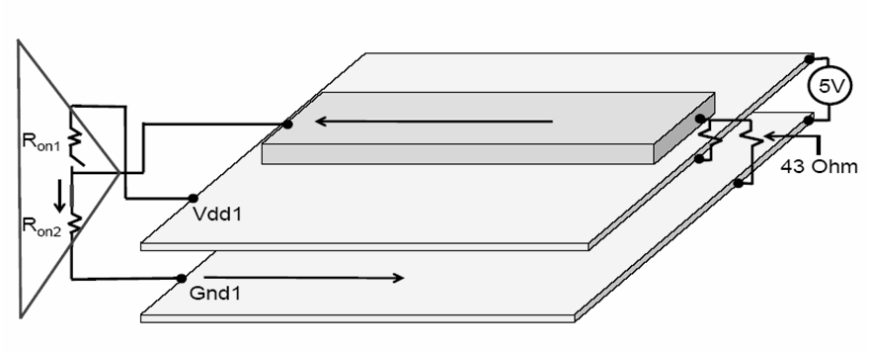

Figure 86: Microstrip transmission line referenced to non-ideal power/ground planes

left corner of the matrix [20]. This is shown in the following equation where Y_{ee} and Y_{ii} refer to the internal and external (required) ports respectively.

$$\begin{bmatrix} Y_{11} & \cdots & Y_{m1} \\ \vdots & \ddots & \vdots \\ Y_{1m} & \cdots & Y_{mm} \end{bmatrix} \rightarrow \begin{bmatrix} [Y_{ee}]_{nxn} & [Y_{ei}]_{nx(m-n)} \\ [Y_{ie}]_{(m-n)xn} & [Y_{ii}]_{(m-n)x(m-n)} \end{bmatrix} \tag{72}$$

From this reordered Y-matrix, the reduced n-port representation of the system is obtained using the equation

$$[Y]_{nxn} = Y_{ee} + Y_{ei}(-Y_{ii}^{-1}Y_{ie}) \tag{73}$$

The reduced-order system matrix thus obtained captures all the parasitics in the system. This system matrix is then converted into S-parameters that can be simulated using the causal SFG based transient simulation technique described in Section 4.1 to perform a SI-PI analysis.

4.3.2 Test case

This subsection describes the application of the complete co-simulation methodology on a simple test case and shows how the developed transient simulation technique provides a more accurate result as compared to existing transient simulation engines. The system under consideration is a microstrip transmission line referenced to non-ideal power ground planes. The system is shown in Figure 86. The line has a characteristic impedance of 22Ω and has a "nearly" matched load consisting of two 43Ω resistors to the power and ground planes respectively. The plane pair is powered by a 5V DC source and the transmission line

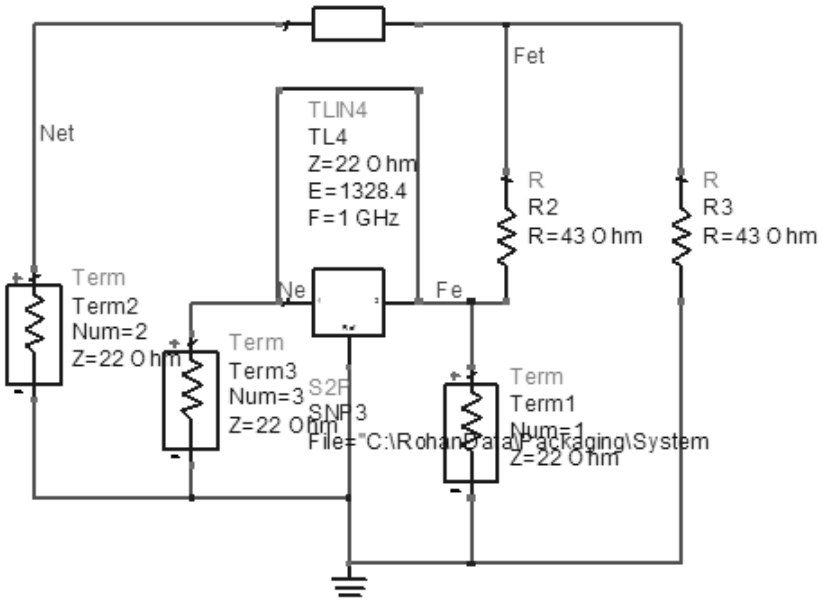

Figure 87: Integration of the SDN and the PDN using ADS (Screen shot)

is driven using a digital driver. The line and the planes were all 20 in. in length and the planes were 0.3 in. wide. The transmission line was 30 mils wide.

The modeling of the system begins by separating the SDN and the PDN. The SDN consists of just a microstrip line referenced to ideal ground. This was modelled using Agilent's Advanced Design System (ADS) to obtain a two-port Y-parameter representation of the transmission line [1]. Similarly the PDN consisting of a pair of power/ground planes was modelled using ADS to get a two-port Y-parameter representation. These two Y-parameter representations were then integrated using Equation 70. The line termination impedances were then added to the system matrix using the Stamp rule. Finally the system was reduced to a 3-port network. Port 1 is the output port and is located at the far end of the transmission line with respect to ground. Port 2 is located at the near end of the transmission line and Port 3 is located right below port 2 on the power plane. To verify the accuracy of the SDN-PDN integration method, The SDN and the PDN were integrated using ADS. A screen capture from ADS showing the integration of the SDN and the PDN is shown in Figure 87. The figure clearly shows the two blocks representing the SDN and the PDN, the termination impedance added externally, and port terminations defined to obtain the 3-port S-parameters. The 3-port network parameters computed using the two methods

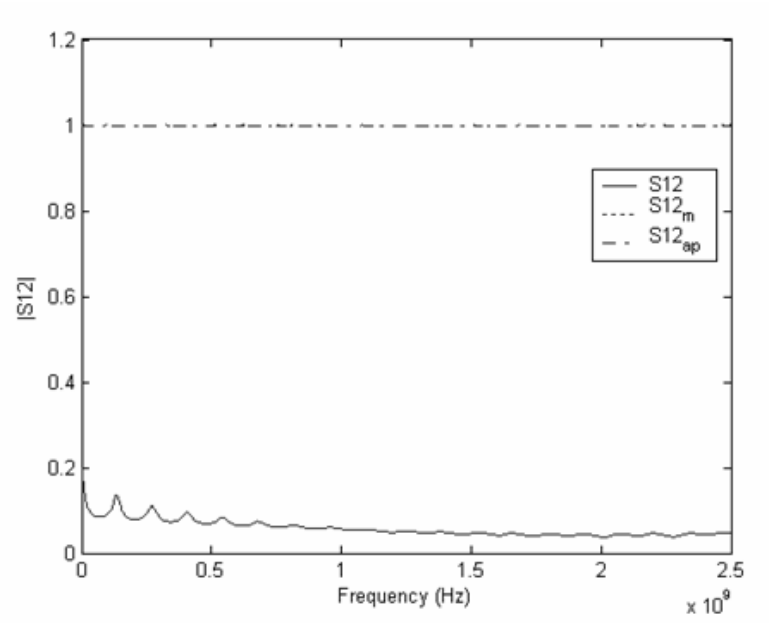

Figure 88: Magnitude response of $s12$ and its minimum phase and all pass components

showed perfect correlation. The 3-port S-parameters are then subject to delay extraction. It is clear that the given network will have delay between ports 1 and 2, and between ports 1 and 3. Consequently $s12$, $s21$, $s13$, and $s31$ are decomposed into their respective minimum phase and all pass components and the delays embedded in each of those transfer responses are extracted. Figure 88 and Figure 89 show the magnitude and phase responses of $s12$, $s12_{min}$, and $s12_{ap}$ respectively. Using $\angle s12_{ap}$ the delay embedded in $s12$ was found to be 3.6 ns. After extracting the delays for the remaining transfer functions similarly, the causal SFG equations for the system were setup and solved. The driver was replaced by an empirical model that consisted of two current sources placed at ports 2 and 3 respectively. The rise time of the driver was 0.5 ns which resulted in the frequency spectrum of the driver output to span from DC to 667 MHz. To verify the transient simulation result, the same circuit was also simulated using the transient simulation engine in ADS [1]. A screen shot of the circuit schematic from ADS is shown in Figure 90. Identical portions of the transient waveforms obtained at the output of the transmission line using the SFG based simulation technique and using the ADS transient simulator are compared in Figure 91. The figure also compares the waveforms on the power plane right below the near end of the transmission

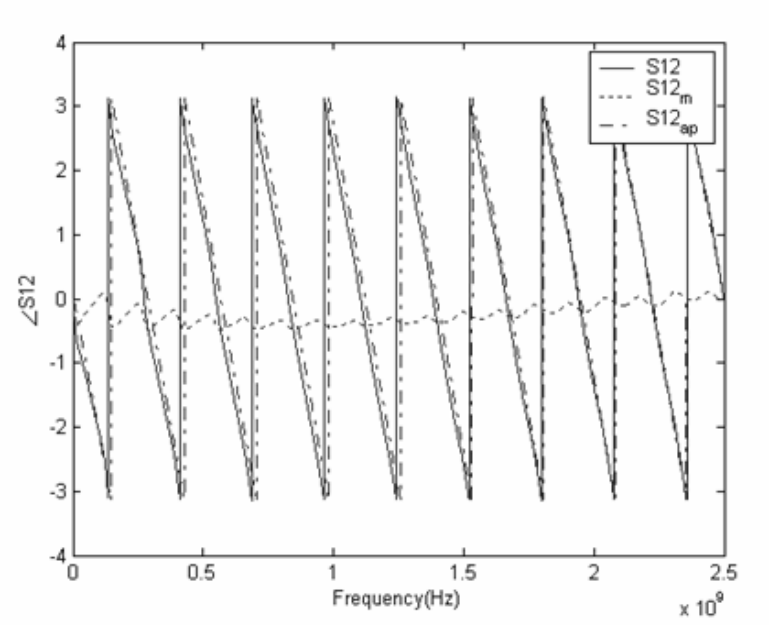

Figure 89: Phase response of $s12$ and its minimum phase and all pass components

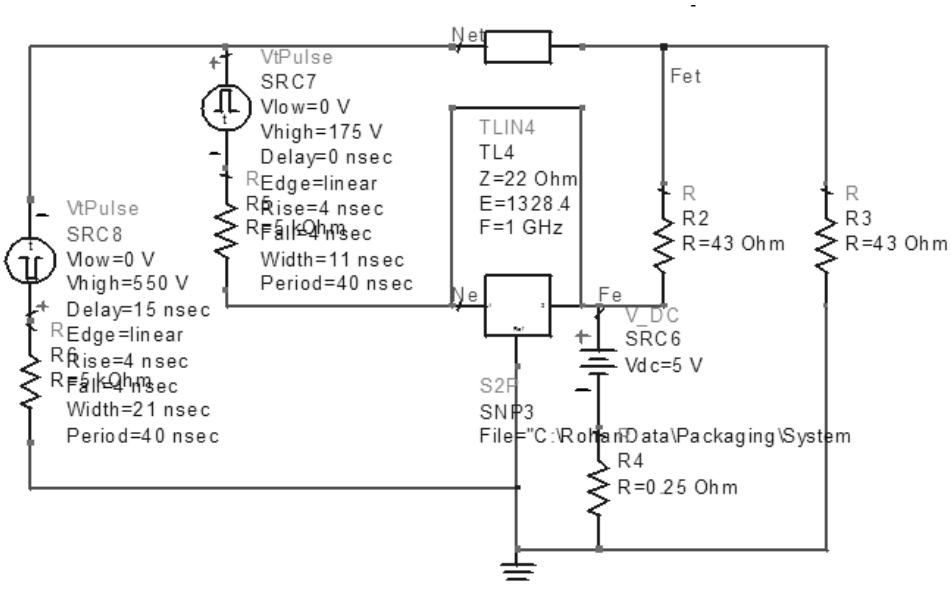

Figure 90: Circuit schematic of the microstrip system simulated using ADS

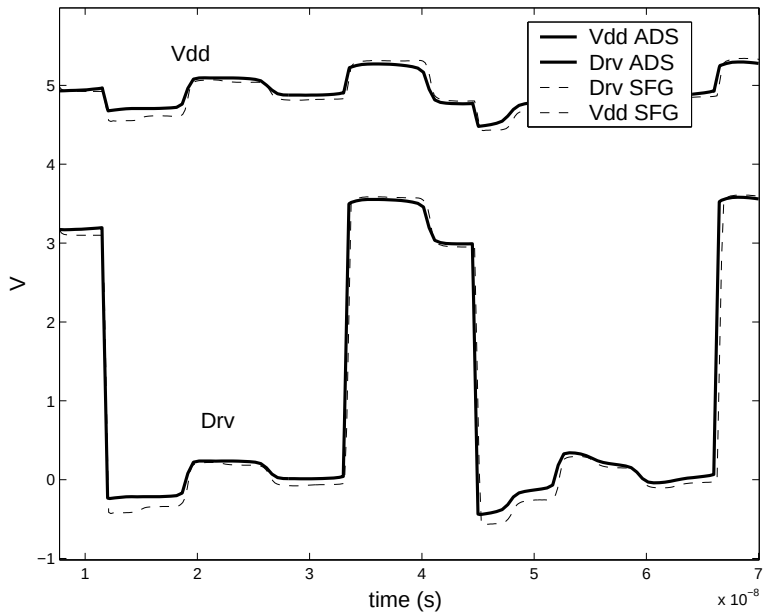

Figure 91: Comparison of the transient waveforms obtained using SFG and using ADS

line. From the figure it is seen that the two waveforms show good correlation. However looking closely at the waveforms on the power plane (Figure 92) it can be seen that the output of the ADS transient simulator violates causality. The arrow on the left indicates the instant when the output of the driver switches from low to high. The arrow to the right indicates the time instant when the reflection from the far end of the line should arrive at the driver output causing the voltage there to dip a little. This is given by the round trip time of the system and is equal to 7.2 ns (2 times the 3.6 ns delay). It is seen that the waveform obtained from ADS starts dipping before this instant indicating a causality violation. The SFG based simulation on the contrary satisfies this criterion and hence provides a more accurate result. In the next chapter it will be shown how these apparently minor inaccuracies affect the quality of the signal integrity analysis of a digital system.

4.4 Summary

This chapter describes a methodology for the transient co-simulation of the SDN and the PDN in a digital system with causality enforcement. Causality deals with the precise timing of signal propagation through distributed passive systems and is an important problem in their transient simulation. Commercially available circuit solvers (example ADS) do

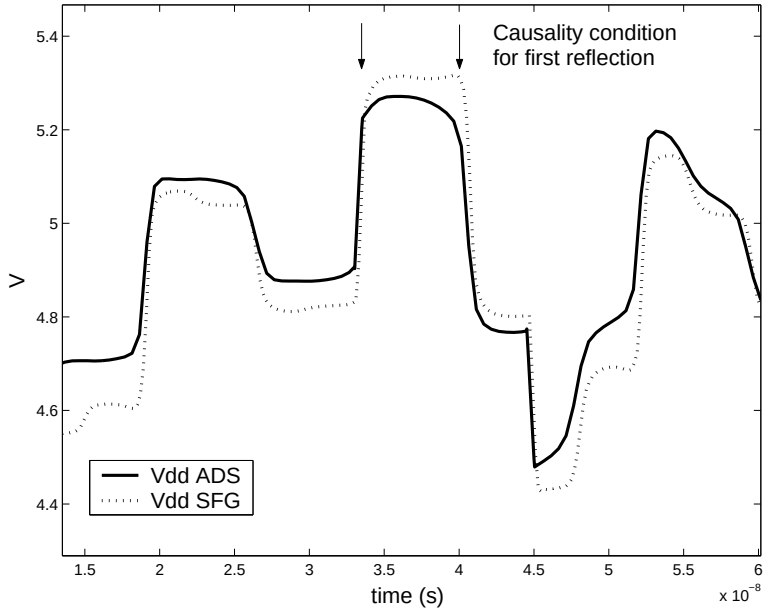

Figure 92: Comparison of the Vdd waveforms obtained using SFG and using ADS

not enforce causality in their transient simulations. This chapter describes a novel delay extraction method which enables the enforcement of causality in a transient simulation. The method involves decomposing a network transfer frequency response into its minimum phase and all-pass components, and proceeds by using the all-pass component to estimate the delay embedded in the response. Once this delay is known, it is explicitly included in the signal flow graph equations that are used for simulating the network. The transient response obtained using these signal flow graph equations satisfies causality. A passivity check is also performed to ensure that the transient simulation does not violate the passivity of the original system. Furthermore the solution of a system of signal flow graph equations requires multiple convolutions to be performed at each time step, which is a computationally expensive procedure ($O(N^2)$). This chapter describes the implementation of a fast convolution technique ($O(NlogN)$) that has been integrated into the SFG framework to enhance its computational efficiency. This algorithm has been tested in the simulation of small as well as large sized systems and shows up to 280% improvement in computational speed. Finally using this transient simulation technique, the chapter describes the co-simulation of the SDN and the PDN in a sample test case. The co-simulation methodology begins by separately modeling the SDN and the PDN in the system to obtain their multiport

frequency responses. These are then integrated using the Nodal Admittance method and the stamp rule to obtain a system matrix that is simulated using signal flow graphs. The integration process ensures that all the coupling parasitics are accurately accounted for in the simulation. The simulation results obtained for the test case are compared with those obtained from a commercial transient simulator (ADS). It is seen that the results obtained using the methodology described in this chapter are more accurate as compared to ADS.

CHAPTER V

SIGNAL INTEGRITY ANALYSIS OF PASSIVE SYSTEMS USING TRANSIENT CO-SIMULATION

Traditionally in packaged systems the analyses of the signal distribution network (SDN) and the power distribution network (PDN) have been carried out independently. Once the layout of a system is available, geometrical information is extracted to obtain the PDN and the SDN separately. However as shown in the previous chapters, effects like simultaneous switching noise (SSN) that occur in the PDN can affect the quality of the signal that propagates through the SDN. Analyzing the two networks separately fails to account for these effects and hence compromises on the quality of the SI analysis. A methodology for the co-simulation of the two networks has been presented in Chapter 4. This methodology accurately captures all the parasitic coupling between the SDN and the PDN and is scalable to perform large sized simulations. In this chapter this methodology is applied on a variety of test structures to analyze the eye-openings obtained in the SDN in the presence of switching noise in the PDN.

The step-wise flow of the co-simulation methodology as applied on each of the test structures is shown in Figure 93. The methodology begins by separating the system layout into the SDN and the PDN. The PDN is modelled using the Transmission Matrix method (TMM). The TMM method as described in [30] has been implemented in a software tool called SWITCH that has been developed at Georgia Tech. Using a parser, a Gerber file describing the system layout is directly imported into SWITCH to obtain the PDN layout. Then using its graphic user interface, input and output ports are defined at the desired locations. Finally using the TMM engine in SWITCH, the PDN layout is simulated to obtain a multiport frequency response of the network. The SDN in the layout is modelled using the ADS LineCalc tool [1]. Using this tool, the SDN is also reduced to a multi-port frequency response. Once the multi-port frequency responses (in terms of Y-parameters)

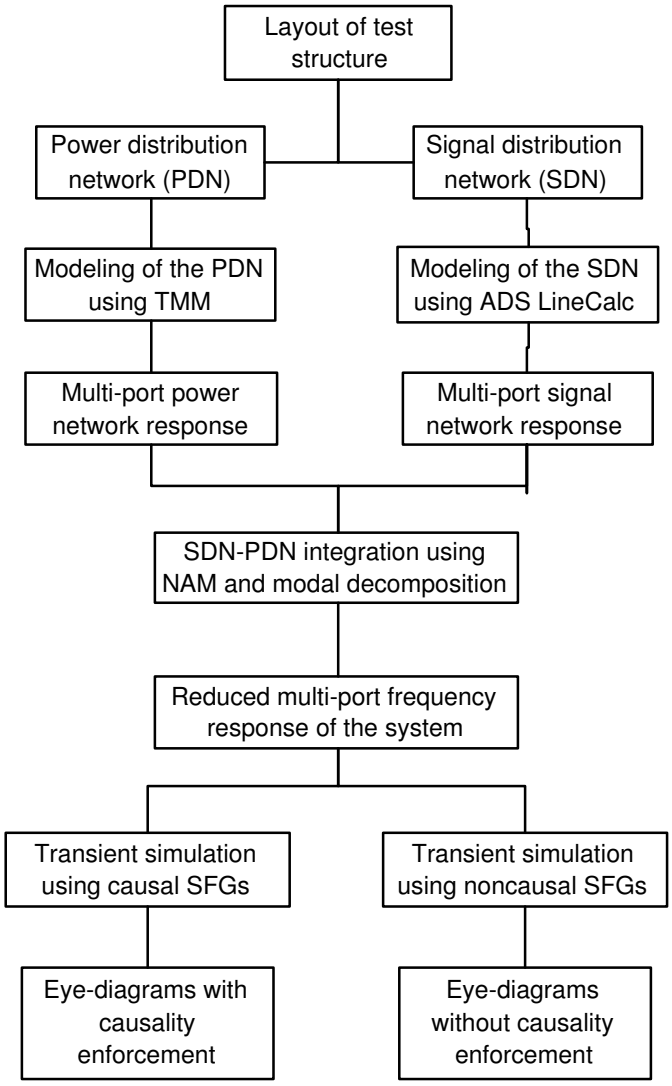

Figure 93: Steps involved in the transient co-simulation methodology applied in this chapter on various test structures

of the PDN and the SDN are obtained, they are integrated using the Nodal Admittance method and the Stamp rule as described in [51]. The integrated response is then subject to a reduction in order (reduction in number of ports), by retaining only those ports where the system is either being excited by an input or being probed for an output. For some test structures the integration of the SDN and the PDN frequency responses was performed using ADS. Finally, this reduced system is simulated using the signal flow graph method described in Chapter 4. To understand the effects of causality violations on the signal integrity analysis of digital systems, the reduced system network is simulated using the causal as well as the non-causal SFG equations. The outputs obtained for the two cases are compared in using eye-diagrams. It is seen that the eye-openings obtained for the two cases vary substantially for some of the test structures.

The test structures on which the proposed co-simulation methodology has been applied have been categorized as follows. Section 5.1 describes co-simulation of simple systems having a single transmission line referenced to non-ideal power/ground planes. These include a stripline interconnect system, and a microstrip interconnect system with via transitions. Section 5.2 describes the co-simulation of systems having multiconductor interconnect buses referenced to non-ideal power ground planes. This includes amongst others, the simulation of a pair of coupled transmission lines, and a 64-bit interconnect bus that resulted in a 130-port system network. Unlike the first two sections, which essentially demonstrate the effects of causality violations on the SI analysis of passive systems, Section 5.3 focuses on the effects of noise coupling between the signal and power networks in passive systems. The section describes how these coupling effects can be accurately simulated using the co-simulation methodology discussed in this dissertation. Finally Section 5.4 describes the application of the co-simulation methodology on real world test cases which include an IBM HyperBGA package and a PCI Express interconnect circuit.

5.1 Single conductor transmission line systems

This section describes the application of the transient co-simulation methodology on a couple of single conductor transmission line systems. For each of the test structures, the

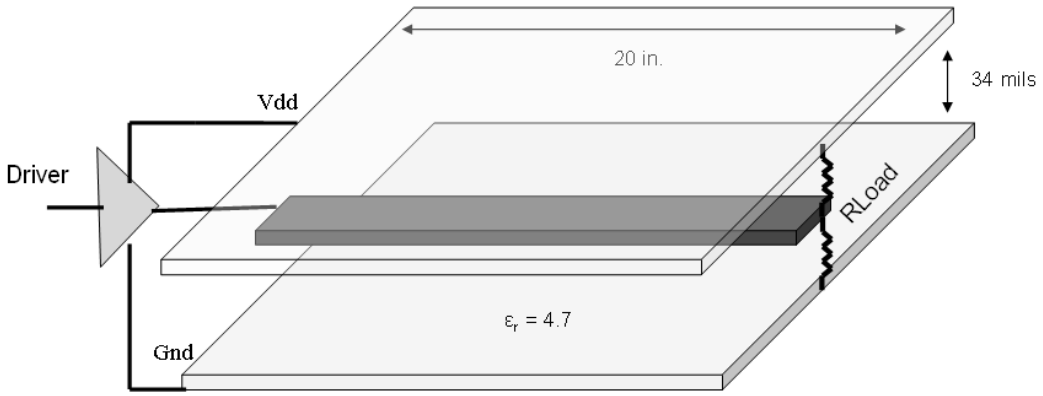

Figure 94: Stripline interconnect referenced to non-ideal power/ground planes

system layout is presented followed by a description of the excitation pattern applied to the system. Finally the eye-diagrams obtained through simulations using the causal and the non-causal SFG equations are compared and analyzed.

5.1.1 Stripline interconnect

The first test structure was a simple stripline interconnect referenced to non-ideal power/ground planes and terminated with a nearly matched impedance. The structure is shown in Figure 94. The stripline interconnect had a characteristic impedance of 22Ω and was terminated using two 43Ω resistors connected one each to the power and the ground planes. Both the line and the power/ground planes were 20 in. in length. The planes were 0.3 in. wide while the stripline was 30 mils in width. The planes were separated by 34 mils of dielectric substrate with an ϵ_r of 4.7. The frequency responses of the SDN and the PDN were simulated separately up to 2.5 GHz and then integrated using the modal decomposition formula given by Equation 71 in Chapter 4. A random bit pattern source with a rise time of 150ps was used to excite the line at the near end and the output of the system was observed at the far end of the line. The comparison of the eye-diagrams obtained at the output from causal and non-causal simulation of the system are shown in Figures 95 and 96. It can be seen that the non-causal simulation results in an artificial eye-closure of about 50 mV. The spread obtained in the eye in both the figures is primarily due to two effects: 1)

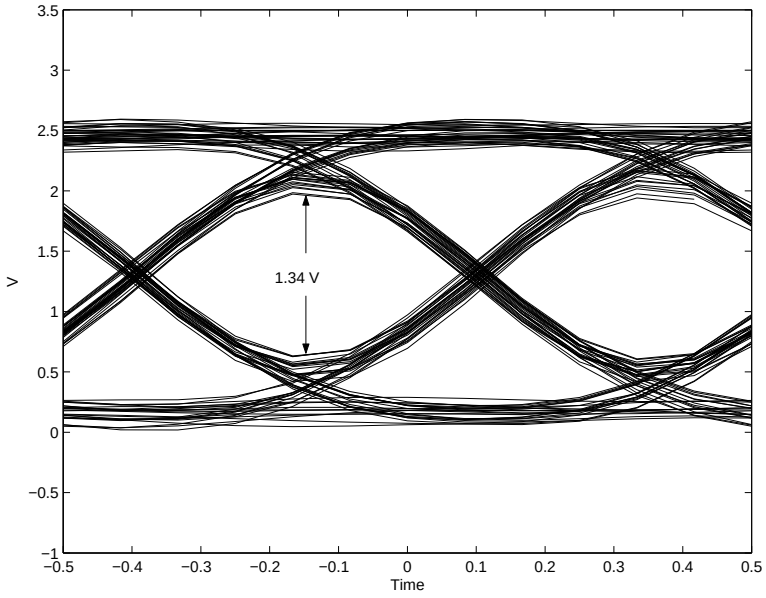

Figure 95: Causal simulation of stripline interconnect

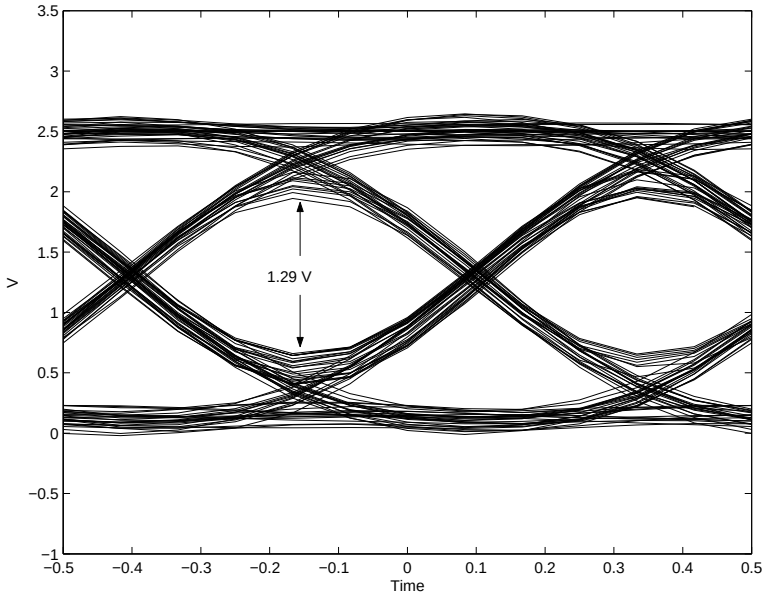

Figure 96: Non-causal simulation of stripline interconnect

Table 5: Simulation of a stripline interconnect system

Characteristic impedance	22 Ω
Bandwidth of system response	2.5 GHz
Rise time of driver	150 ps
Random bit pattern length	500 bits
No. of ports in the system network	4
Eye-opening with causal simulation	1.34 V
Eye-opening with non-causal simulation	1.29 V
Artificial eye-closure	50 mV

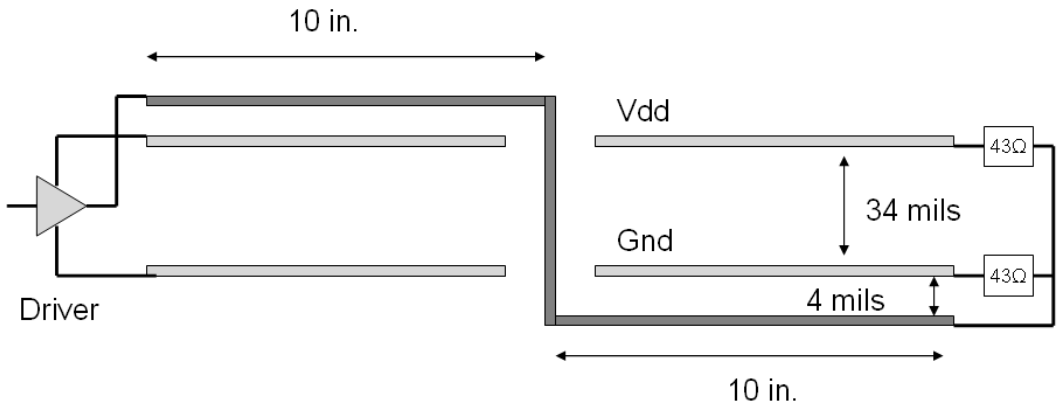

Figure 97: Microstrip interconnect with a via discontinuity and non-ideal reference planes

the slight mismatch in the termination impedance of the line causes reflections, and 2) the switching of the driver causes noise fluctuations (SSN) on the power ground planes. Since in a stripline system, the parallel plate mode is coupled to the stripline mode, a portion of these SSN fluctuations get coupled onto the stripline output. Integrating the SDN and the PDN responses using the appropriate modal decomposition technique ensures that this coupling is accurately captured in the simulation. The simulation parameters and results for the stripline system are summarized in Table 5.

5.1.2 Microstrip interconnect with via transitions

The second test case was a microstrip interconnect passing through a via discontinuity as shown in Figure 97. The microstrip line was 20 in. in length with a 42 mil via located at the midpoint. The characteristic impedance of the line was 22 Ω and it was terminated with two 43 Ω resistors connected one each to the power and the ground planes respectively. The PDN was modelled using SWITCH while the SDN was modelled using ADS. The via discontinuity

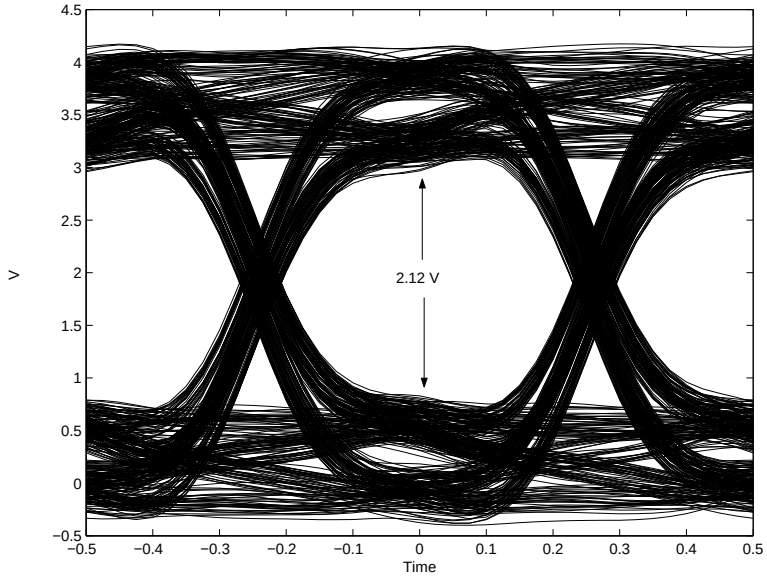

Figure 98: Causal simulation of microstrip interconnect with via discontinuity

Table 6: Simulation of a microstrip interconnect system with a via discontinuity

Characteristic impedance	22 Ω
Bandwidth of system response	2.5 GHz
Rise time of driver	400 ps
Random bit pattern length	1000 bits
No. of ports in the system network	4
Eye-opening with causal simulation	2.12 V
Eye-opening with non-causal simulation	2.02 V
Artificial eye-closure	100 mV

was modelled in Ansoft HFSS to obtain its two-port S-parameter representation which was then integrated with the other modules to obtain the system network response. The system was simulated using a random bit pattern source having a rise time of 400 ps. The eye-diagrams obtained at the far end of the transmission line with and without causality enforcement are shown in Figures 98 and 99. From the figures it can inferred that for this structure, the causality violations cause an artificial eye-closure of about 100 mV. In the design of high performance low cost systems, where the tolerances of the various system modules are really small, simulation inaccuracies of the order of a few tens of millivolts can prove critical. The simulation parameters and results for the above microstrip interconnect system are summarized in Table 6.

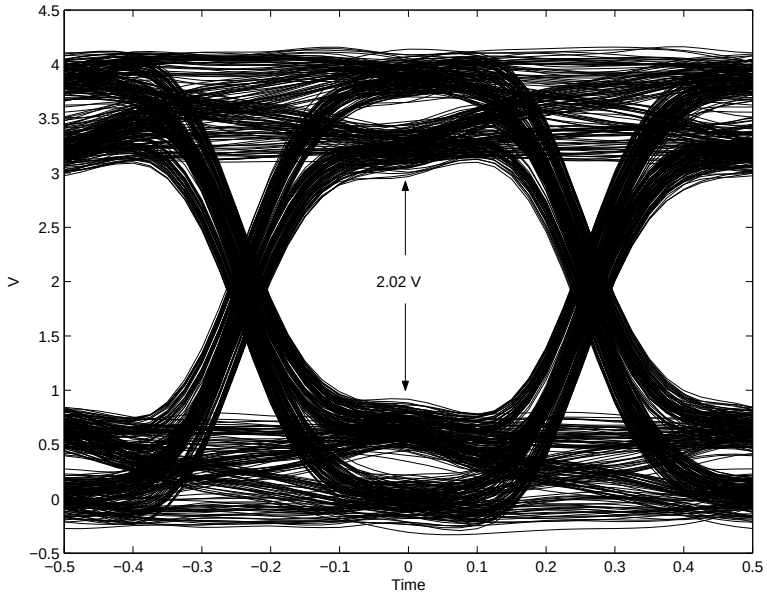

Figure 99: Non-causal simulation of microstrip interconnect with via discontinuity

5.2 Multiconductor transmission line systems

The previous section considered simple single conductor transmission line systems where the SDN could be represented using a 2-port S-parameter network (or multiple 2-port S-parameter networks for the via case). However if there exists direct coupling between adjacent signal lines, then a higher order SDN network is required. This section describes the co-simulation of coupled transmission lines referenced to a non-ideal PDN. It also describes the co-simulation of multiconductor buses of varying sizes all referenced to non-ideal PDNs. For one such 8-bit bus, the section clearly demonstrates how the SSN in the PDN can couple into the SDN and affect the quality of the signal propagation.

5.2.1 Coupled microstrip interconnects

For the coupled microstrip interconnect case, a pair of microstrip interconnects were referenced to a pair of power ground planes that were 20 in. in length and 0.3 in. in width. The planes were separated by 34 mils of dielectric substrate with a ϵ_r of 4.7. The two signal lines were 3 mils apart and had a substrate thickness of 4 mils resulting in a characteristic impedance of 22 Ω. The coupled line setup is shown in Figure 100. The lines were driven using a random bit pattern source having a 500 ps rise time and were terminated using 43

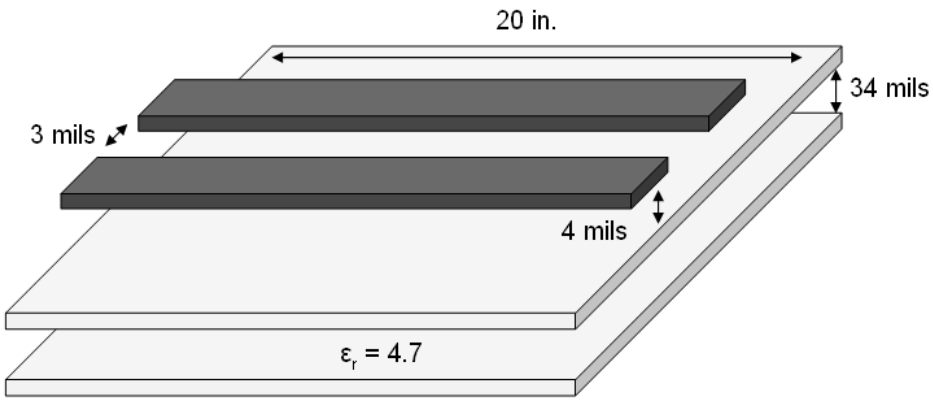

Figure 100: Coupled transmission lines referenced to a non-ideal PDN

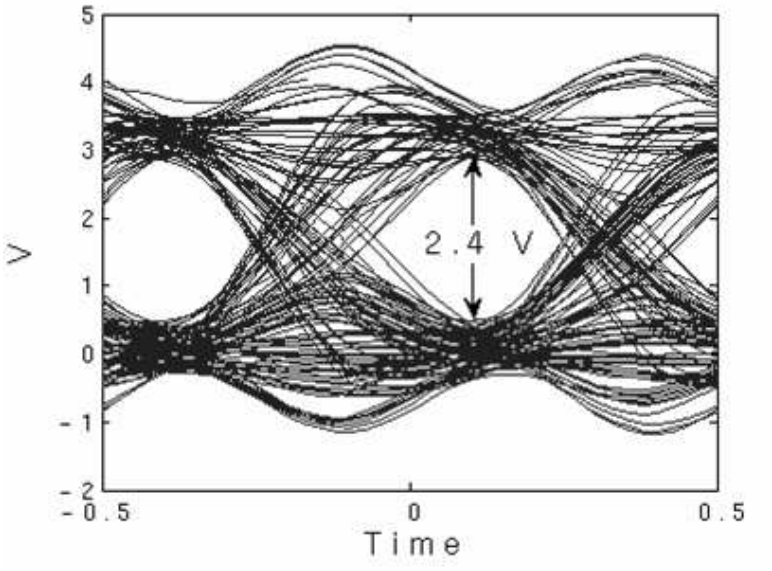

Figure 101: Causal simulation of coupled microstrip interconnects

Ω resistors as shown in the single conductor examples. The output was observed at the far end of one of the lines with respect to ground. Figures 101 and 102 show the eye-diagrams obtained at the output using causal and non-causal transient simulations. It is seen that in this case the causality violations result in an artificial eye-closure of about 200 mV. The simulation parameters and results are summarized in Table 7.

5.2.2 32-bit microstrip interconnect bus

This test case consisted for a 32-bit microstrip interconnect bus referenced to non-ideal power ground planes. The power ground planes were 5 in. x 5 in. is size and were

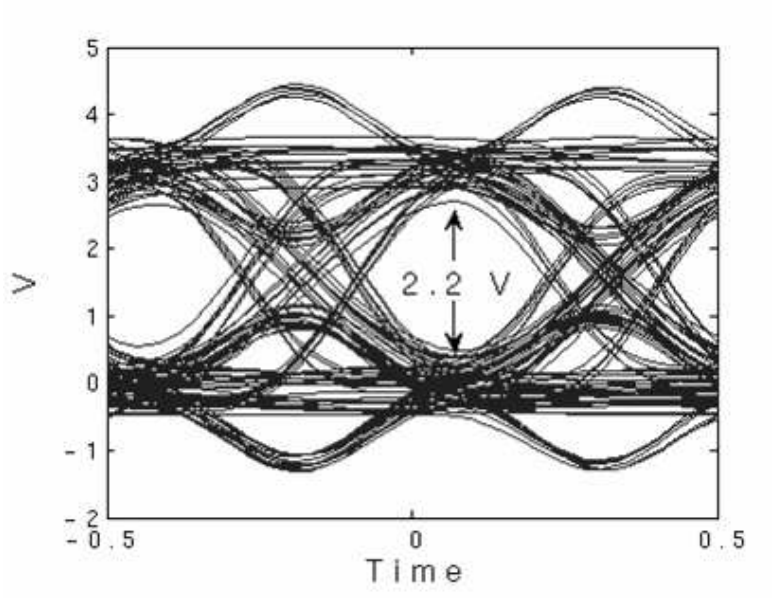

Figure 102: Non-causal simulation of coupled microstrip interconnects

Table 7: Simulation results for coupled microstrip interconnects

Characteristic impedance	22 Ω
Bandwidth of system response	2.5 GHz
Rise time of driver	500 ps
Random bit pattern length	500 bits
No. of ports in the system network	6
Eye-opening with causal simulation	2.4 V
Eye-opening with non-causal simulation	2.2 V
Artificial eye-closure	200 mV

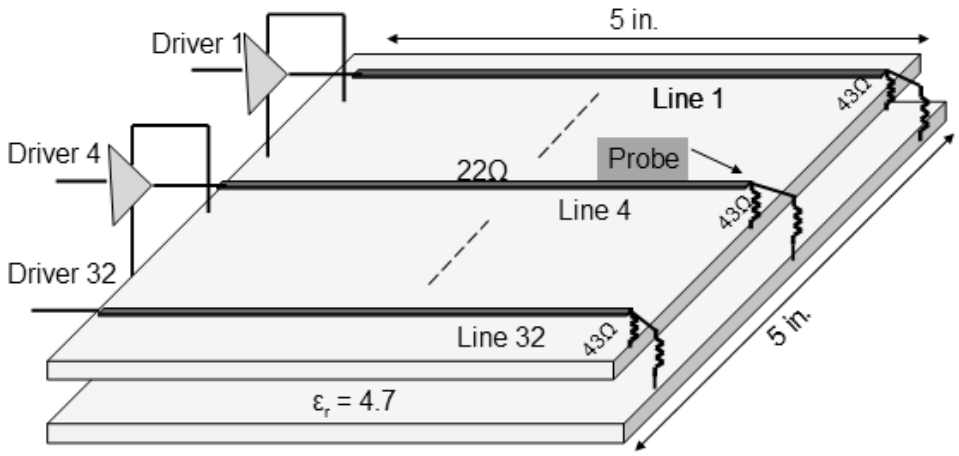

Figure 103: 32-bit microstrip bus referenced to a non-ideal PDN

separated by 34 mils of dielectric with an ϵ_r of 4.7. 32 microstrip interconnects each with a characteristic impedance of 22 Ω were referenced to these power/ground planes. The lines were separated from the closest plane by 4 mils of dielectric. The spacing between two signal lines was designed to be 20 mils so that there would be no direct coupling between adjacent interconnects. The structure is shown in Figure 103. The PDN was modelled using TMM as a 64 port network. Since there is negligible coupling between adjacent signal lines, the SDN was modelled as 32 separate 2-port networks using ADS LineCalc. The two were integrated using the methodology described in Chapter 4 and termination impedances were added to the system network using the Stamp rule. Finally the system matrix was reduced to a 66-port S-parameter network that was simulated using signal flow graphs. Each of the 32 interconnects were driven by random bit pattern sources with 400 ps rise time. The eye-diagrams obtained at the output of one of the 32 interconnects using causal and non-causal SFGs are shown in Figures 104 and 105 respectively. In this case the causality violations result in an artificial eye-closure of about 160 mV. The simulation parameters and results are summarized in Table 8. This test case also shows that the transient co-simulation methodology proposed in this dissertation is able to accurately simulate a 66-port S-parameter network. Macro-modeling techniques like the one described in [37] can handle only about 20 to 30 ports.

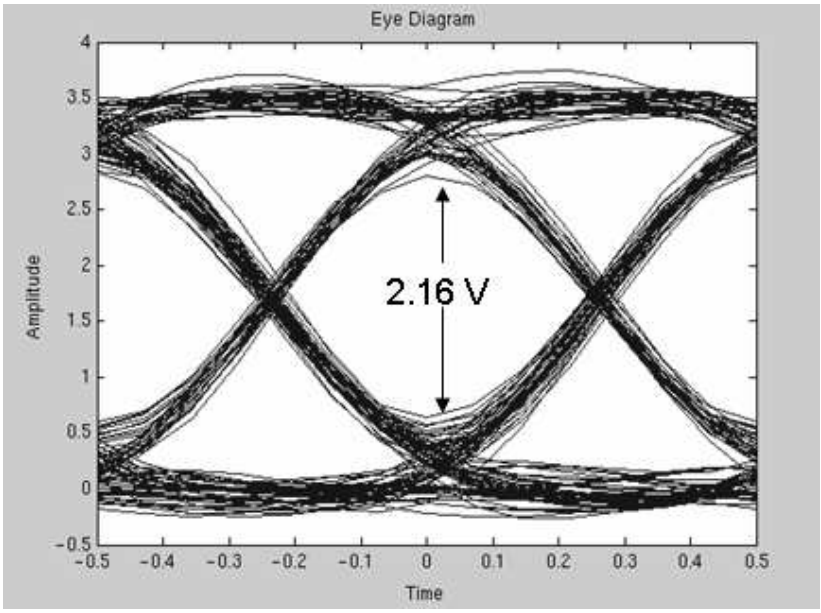

Figure 104: Causal simulation of 32-bit microstrip interconnect bus

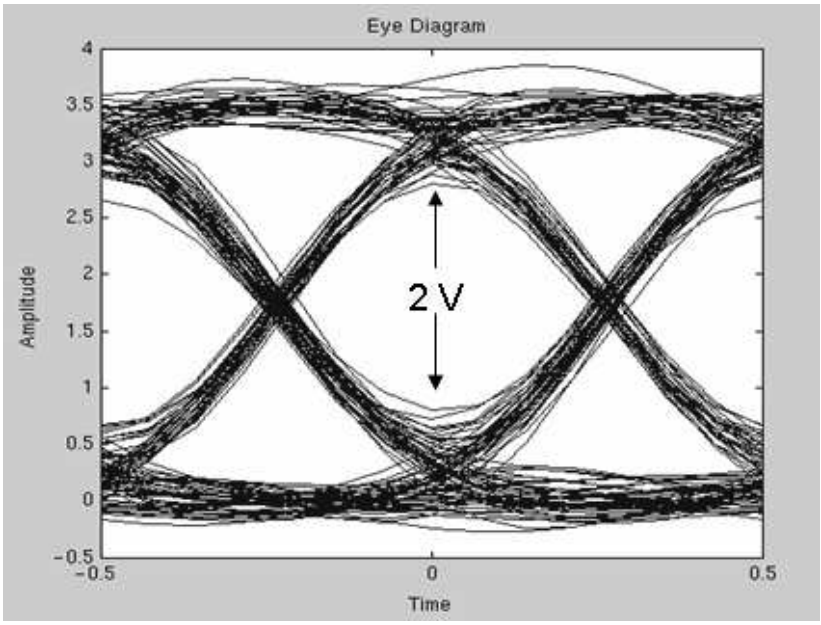

Figure 105: Non-causal simulation of 32-bit microstrip interconnect bus

Table 8: Simulation results for 32-bit microstrip interconnect bus

Characteristic impedance	22 Ω
Bandwidth of system response	2.5 GHz
Rise time of driver	400 ps
Random bit pattern length	350 bits
No. of ports in the system network	66
Eye-opening with causal simulation	2.16 V
Eye-opening with non-causal simulation	2.0 V
Artificial eye-closure	160 mV

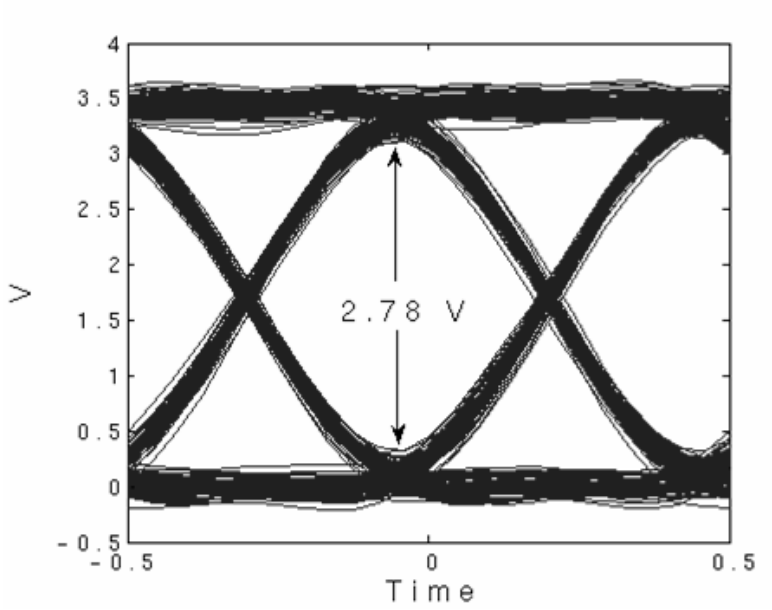

Figure 106: Causal simulation of 64-bit microstrip interconnect bus

5.2.3 64-bit microstrip interconnect bus

To test the scalability of the co-simulation methodology being used in this chapter, the structure from the previous example was cranked up to form a 64-bit microstrip interconnect bus. The dimensions of the planes and other design specifications remained the same. The PDN for this case was modelled using TMM as a 128-port Y-parameter network. The integration of the SDN and the line terminations resulted in a consolidated system network defined by a 250-port Y-parameter matrix. Using the model reduction formula this was reduced to a network containing 130 ports. This 130-port system was transformed to S-parameters and simulated using causal and non-causal SFG equations. The eye-diagrams obtained for the two cases are shown in Figures 106 and 107 respectively. It is seen that

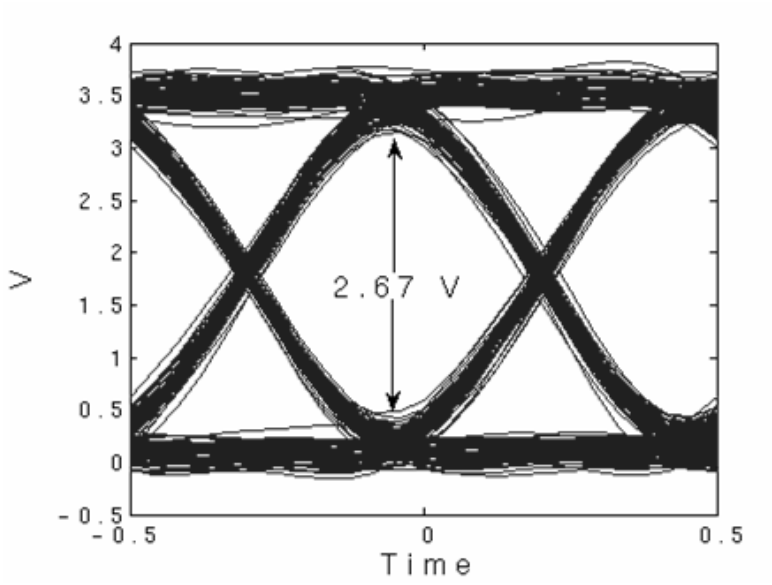

Figure 107: Non-causal simulation of 64-bit microstrip interconnect bus

Table 9: Simulation results for 32-bit microstrip interconnect bus

Characteristic impedance	22 Ω
Bandwidth of system response	2.5 GHz
Rise time of driver	500 ps
Random bit pattern length	500 bits
No. of ports in the system network	130
Eye-opening with causal simulation	2.78 V
Eye-opening with non-causal simulation	2.67 V
Artificial eye-closure	110 mV

for this test case the causality violations resulted in a 110 mV eye closure. The simulation parameters and results for the 64-bit bus are summarized in Table 9. From this test case it can be concluded that the proposed SFG based transient co-simulation technique can effectively simulate large sized networks consisting of over a hundred ports.

5.3 Analysis of noise coupling between the SDN and the PDN

The focus of the previous two sections has been on the analysis of the effects of causality violations on the accuracy of transient simulation of passive systems. This section shifts the focus onto the analysis of the coupling between the SDN and the PDN, and how that coupling can be accurately simulated using the transient co-simulation methodology developed

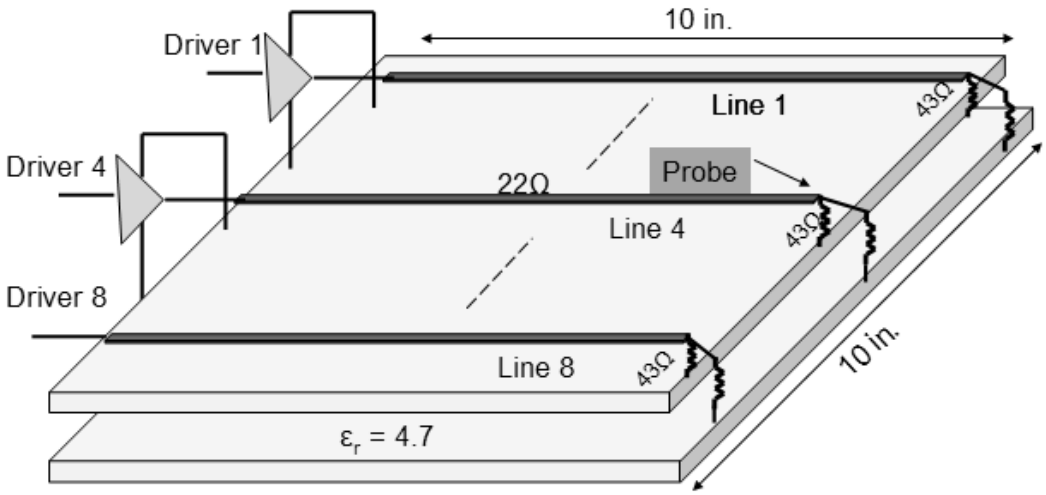

Figure 108: 8-bit microstrip bus referenced to a non-ideal PDN

in this dissertation.

5.3.1 Simulation of an 8-bit interconnect bus

The first test case in this section concerns the simulation of an 8-bit microstrip interconnect bus referenced to non-ideal power ground planes. The structure being simulated is shown in Figure 108. The planes are 10 in. X 10 in. in size are are separated by 7 mils of dielectric substrate with an ϵ_r of 4.7. The microstrip interconnects are designed with a substrate thickness of 4 mils and a width of 23 mils. That results in a characteristic impedance of 22 Ω for each of the 8 interconnects. The spacing between two lines was designed to be much larger than the line width so that there would be no direct coupling between adjacent signal lines. Hence any coupling observed between adjacent signal lines can be assumed to occur through the PDN of the system. Each of the 8 interconnects was driven using a random bit pattern source with a 150 ps rise time and a 400 ps period. The lines were terminated using two 43 Ω resistors connected one each to the power and the ground planes. The output was observed at the load end of line 4 as shown in Figure 108. In the first simulation case, only the driver on line 4 was switched using a random bit pattern. The eye-diagram obtained at the output is shown in Figure 109. It is seen that a relatively clean eye is obtained with an eye-opening of about 3.48 V. The small spread obtained in the eye is due to two reasons: 1) The termination on the line is not perfectly matched resulting in

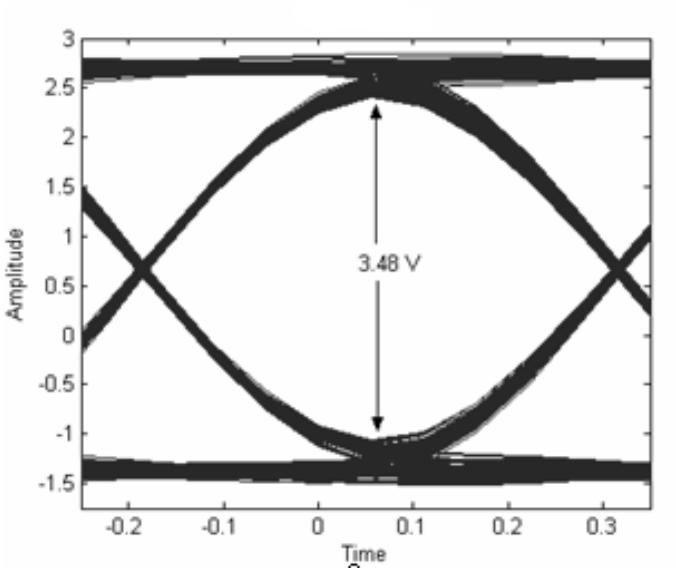

Figure 109: System output when only a single driver is switching

reflections that contribute to the spread, and 2) The switching action of the driver generates fluctuations on the power/ground planes that couple onto the signal line. As we shall see for the second case, this coupling can be substantial when the number of drivers contributing to the switching noise in the PDN is large. In the second case, all 8 drivers in the system were switched using 8 different random bit pattern sequences. The output observed that the load end of line 4 in this case is shown in Figure 110. A substantial reduction (about 920 mV) can be seen in the eye-opening as compared to Figure 109. Since there is no direct coupling between signals on adjacent lines in this system, the increased spread in the eye is due to the SSN in the PDN of the system that get coupled onto the SDN. Simulating the SDN and the PDN separately would not be able to capture this line to line coupling (through the PDN) in the system. However with the co-simulation methodology discussed in this dissertation, this can be accurately captured as seen here.

5.3.2 Analysis of the noise coupling on a quiet line adjacent to a noisy 8-bit bus

In a complex digital system, different circuits can tolerate different levels of noise. Hence if a particular module generates a lot of noise, it is important to accurately analyze how this noise gets coupled to the adjacent modules. In this test case, an 8-bit microstrip interconnect

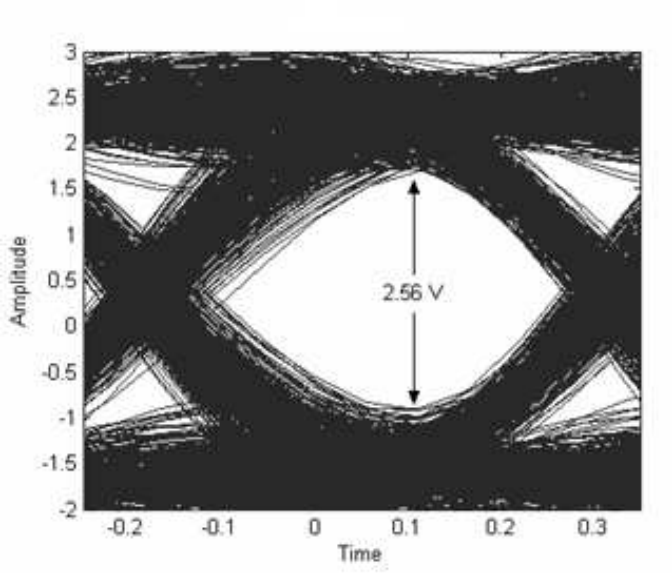

Figure 110: System output when all 8 drivers are switching

bus is rerefenced to a 10 in. x 10 in. power/ground plane pair like in the previous example. The plane pair also as acts as a reference to an isolated quiet line (microstrip). The design parameters for the system and the substrate properties are the same as in the previous test case. The structure is shown in Figure 111. During the course of this experiment the distance of the quiet line from the 8-bit bus is varied and the noise coupled onto the quiet line is probed when the bus is driven using random bit pattern drivers. The isolated line is placed at four different locations

1. 0 in. : In this case the isolated line is right next to the 8-bit bus which is located over one end of the power/ground plane pair.

2. 3 in. : In this case the isolated line is 3 inches away from the 8-bit bus

3. 6 in. : In this case the isolated line is 6 inches away from the 8-bit bus

4. 10 in. : In this case the isolated line is located over the opposite end of the plane pair as compared to the 8-bit bus

For each of the above quiet line locations, the 8-bit bus is driven for 8 different cases using random bit patterns that are 500 bits in length. In the first case, only one of the 8 drivers is switching (SSN generated is minimum), while in the last case all 8 drivers on the bus are

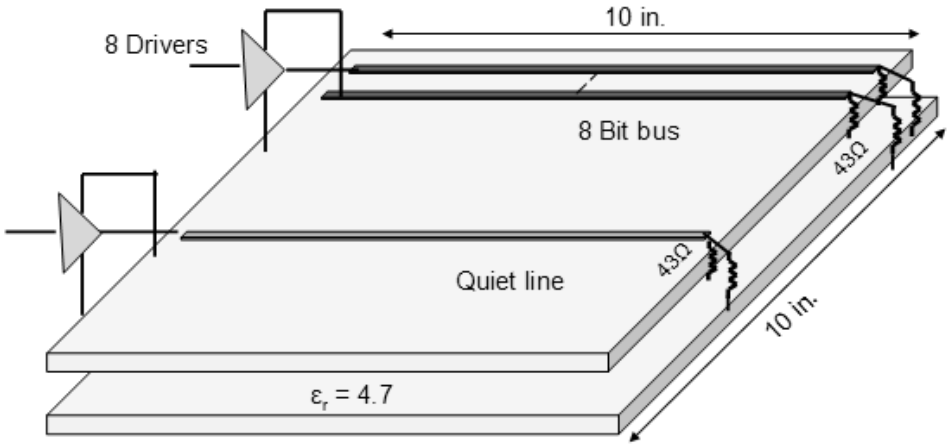

Figure 111: System for analyzing noise coupling on a quite line in the presence of a noisy bus

switching (SSN generated is maximum). The noise on the quiet line is probed for the entire duration of the simulation, and its peak and rms (root mean square) values are calculated for each of the 32 simulations. Figures 112 and 113 show the plots of the peak noise and the rms noise values respectively on the quiet line at 4 different locations, as the number of switching drivers on the 8-bit bus is increased. As expected an increase in the number of active drivers increases the level of noise that gets coupled onto the quiet line in all the cases. However comparing the noise values for the 4 different quiet line locations leads to an interesting observation. Intuitively, the further the quiet line from the 8-bit bus the lesser is the SSN that is expected to couple on to the line. However by looking at the plots in Figures 112 and 113 it can be seen that the SSN seen on the quiet line when it is 10 in. away from the bus is more than the SSN seen on the quiet line when it is 3 in. or 6 in. away from the bus. To investigate this phenomenon, the transfer impedance of the power/ground planes was computed between two ports, one located under the 8-bit bus while the other located under the quiet line. The plots of the transfer impedances are given in Figure 114. Along with the impedances, the spectral content of the SSN current generated by the 8-bit bus was computed using the technique described in Chapter 3 and is plotted in Figure 115. From the figure it can be seen that most of the power in the switching noise current is located upto 1.5 GHz. From Figure 114 it is seen that the transfer impedance curve for the 10 in. location has more peaks in this frequency region as compared to the impedance

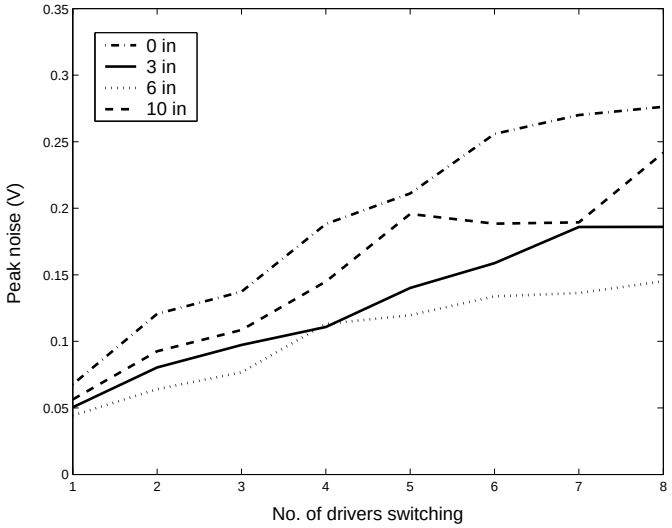

Figure 112: Peak noise on the quiet line

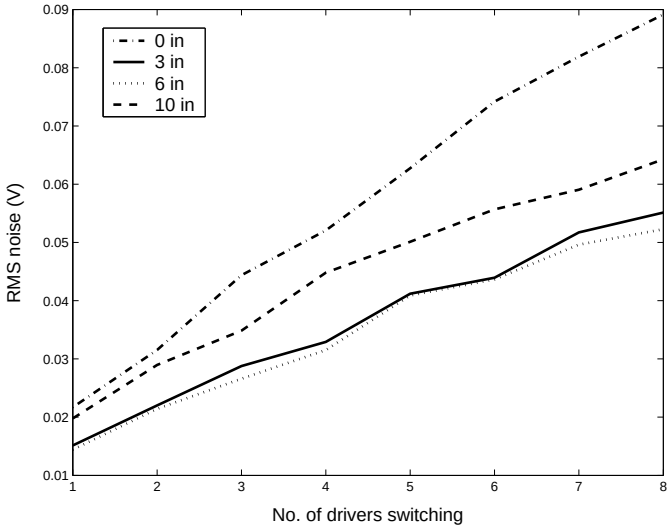

Figure 113: RMS noise value on the quiet line

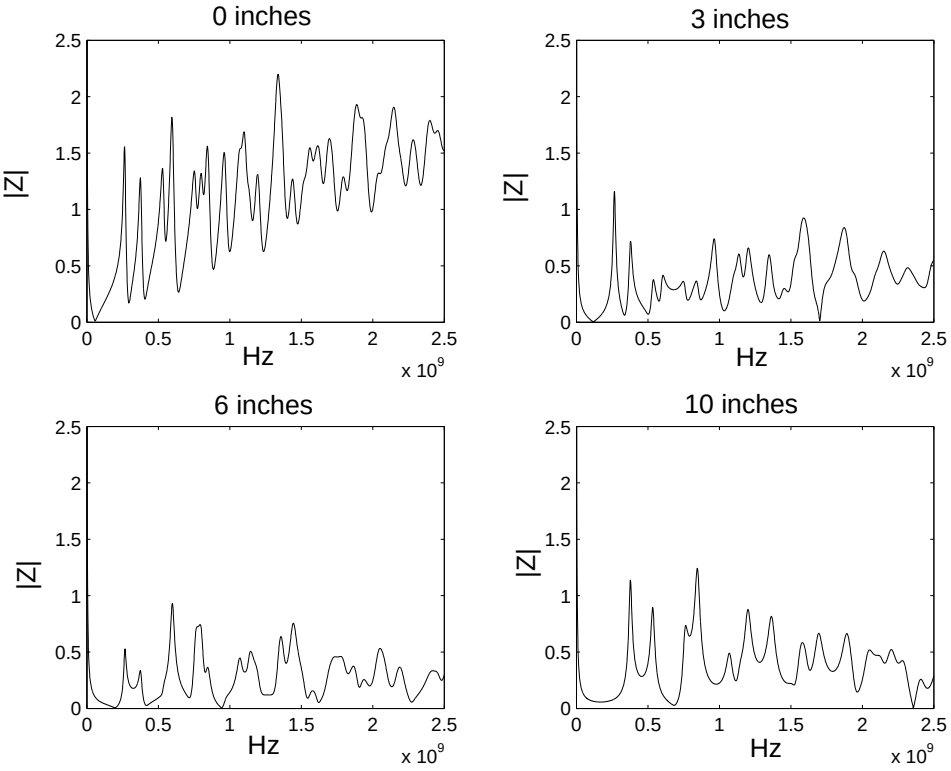

Figure 114: Transfer impedances between the quiet line locations and the 8-bit bus

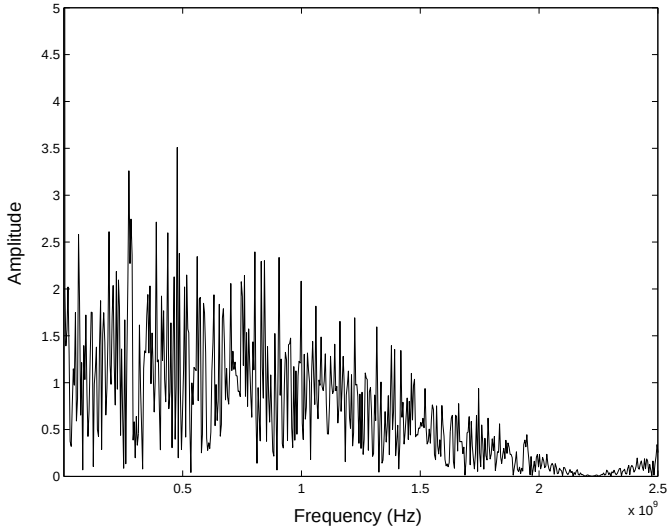

Figure 115: Spectral content of the switching current generated by the 8-bit bus

curves for the 3 in. and the 6 in. locations respectively. This results in more noise getting coupled 10 inches away form the bus as compared to 3 inches away from the bus. It should be noted that these results depend upon the shape and size of the power/ground planes and big changes in them could alter the results considerably. Therefore for systems like these it is essential to co-simulate the PDN with the SDN in order to gain an accurate insight in to their exact performance.

5.4 Real world examples

The final section in this chapter deals with the application of the transient co-simulation methodology on some real world packaged digital systems.

5.4.1 IBM HyperBGA package

The first system under consideration was an IBM HyperBGA package and the aim of the simulation was to analyze the parasitic coupling between adjacent signal lines on the signal layer S1 that occurs through the power/ground network. The package under consideration is a multi-layer HyperBGA package and its layout was provided by IBM. This test case simulated a group of stripline interconnects on the S1 layer that are referenced by the V1 (Power) and the Gnd1 (Ground) layers on the top and bottom respectively. The signal layer S1 in the package is shown in Figure 116. The box indicates the group of interconnects that were considered for this transient co-simulation. The power (V1) and ground (Gnd1) layers were modelled directly in SWITCH by importing the package layout into the software. The PDN model obtained was in the form of a 12-port passive network defined by its Y-parameters. The SDN was modelled using ADS as a group of individual stripline interconnects with ideal references. This was possible because the line-to-line spacing in the package was far greater than an individual line width leading to almost negligible coupling between adjacent signal lines. An illustration of this is shown in Figure 117 that plots the coupling between two adjacent signal lines in the IBM HyperBGA package. Ports 1 and 2 are located at the near and far ends of a signal trace respectively, while port 3 line located at the near end of an adjacent trace. It can be seen that adjacent line coupling (S13) is well below -80 dB over the entire bandwidth of simulation. The models of the PDN and the

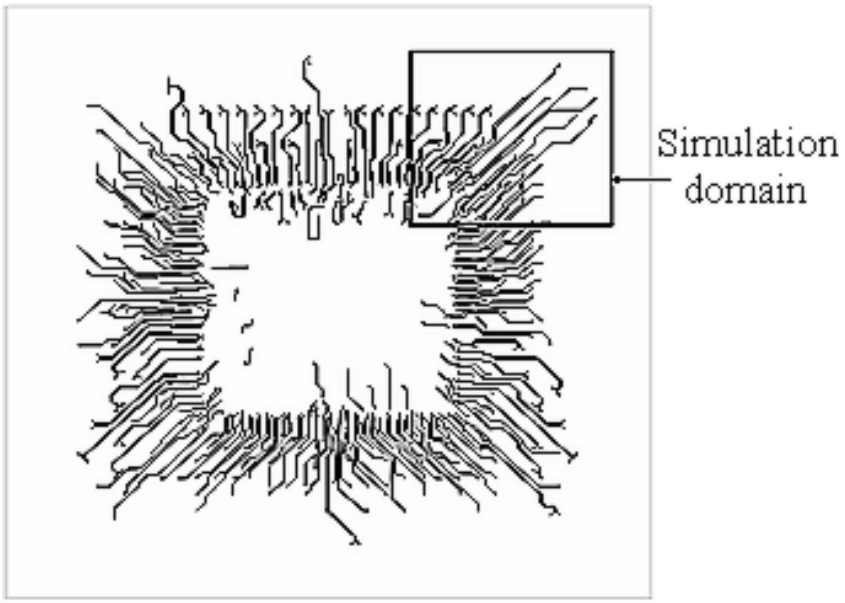

Figure 116: Signal layer on the IBM HyperBGA package

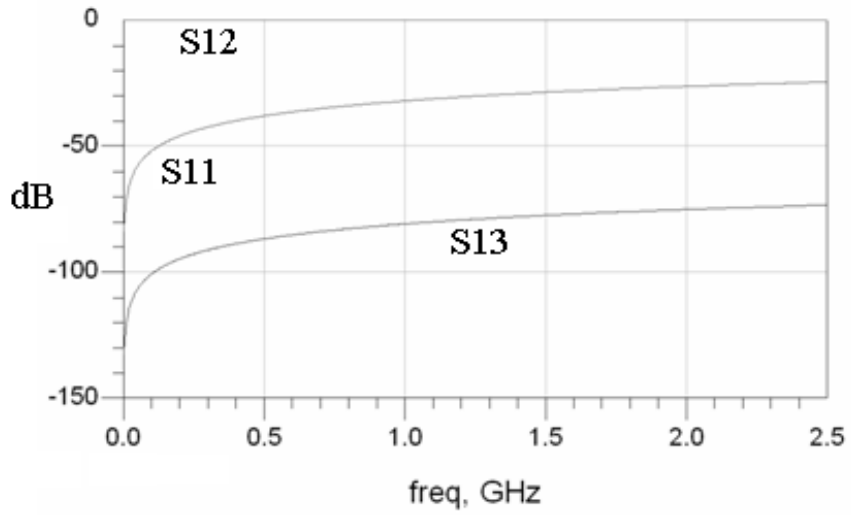

Figure 117: Coupling between adjacent traces on the IBM HyperBGA package

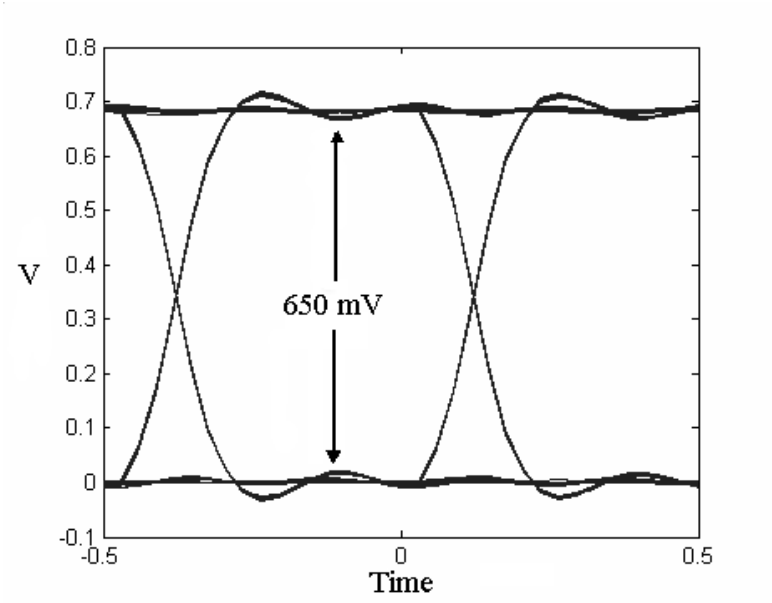

Figure 118: Eye-diagram observed on a signal net in the IBM HyperBGA package

Table 10: Simulation results for IBM HyperBGA package

Characteristic impedance	50 Ω
Bandwidth of system response	2.5 GHz
Rise time of driver	200 ps
Operating frequency of the drivers	625 MHz
Random bit pattern length	500 bits
No. of ports in the system network	24
Eye-opening with causal simulation	650 mV
Eye-opening with non-causal simulation	650 mV

SDN were integrated using the modal decomposition technique for stripline interconnects described in Chapter 4, resulting in a system network consisting of 24 ports. This network was simulated using signal flow graphs and the transient output was observed on one of the signal nets. The interconnects were driven using random bit pattern drivers running at 625 MHz and having a rise time of 200 ps. The simulation parameters and results are summarized in Table 10. The eye-diagram observed at the output is shown in Figure 118. It can be seen from the eye-diagram that the package traces show good signal integrity characteristics. Since the package traces are electrically short, causality violations do not affect the eye-opening considerably. A simulation performed using non-causal SFG equations also yielded an almost identical eye-opening.

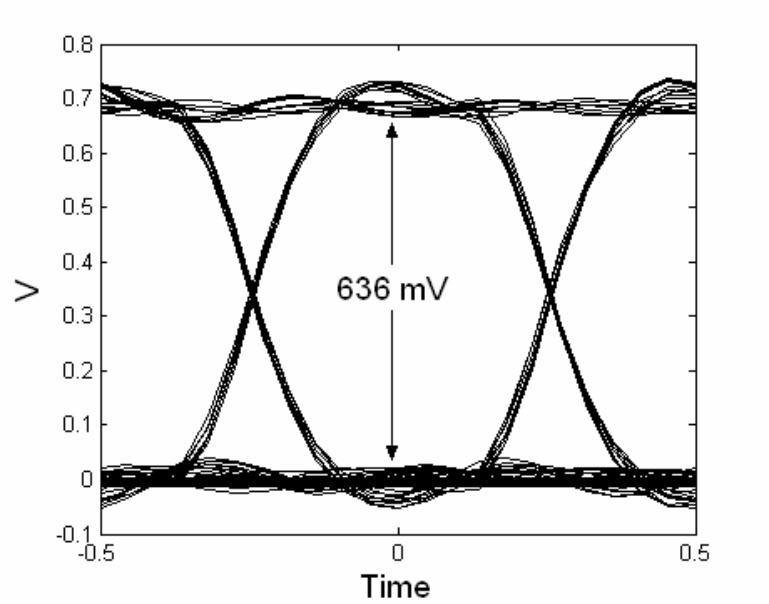

Figure 119: Eye-diagram observed on the signal net in the presence of SSN

One of the reasons for this clean eye-diagram is the relatively lower level of switching noise in the PDN. A more realistic eye-diagram for the system could be obtained if the actual switching noise currents in the PDN were used in the simulation. Since the transient measurements of the SSN voltage on the package PDN were not available, the technique described in Chapter 3 could not be used to obtain the switching noise current. However Chapter 3 describes the extraction of the switching noise current signature in the PDN of an IBM Power5 microprocessor functioning in the 'Idle' mode. Though this current signature will be considerably different from the one generated by the ASIC whose package is being analyzed, it is still a good representation of the switching currents generated by complex digital circuits. Hence using this current signature to excite the PDN, the transient co-simulation of the IBM HyperBGA package was repeated. The eye-diagram obtained on the same interconnect as in the first case is shown in Figure 119. It can be seen from the figure that the noise generated in the PDN due to simultaneous switching of digital circuits gets coupled onto the SDN thereby reducing the eye-opening. It is to be noted that the current signature used in this simulation was for the Power5 microprocessor operating in 'Idle' mode. In the 'Active' mode, with most of the digital circuits switching, the switching currents and hence the noise coupled on to the SDN will be much higher. Hence accurately

simulating the eye-patterns on the SDN for such systems is very critical.

5.4.1.1 Comparison of the complexities of the macro-modeling and SFG based approaches

One of the advantages of the SFG based transient simulation approach is the fact that it can efficiently handle large sized problems. To illustrate this, using the IBM HyperBGA package as an example, a study comparing the complexities of the macro-modeling and SFG based approaches was performed.

- **Macro-modeling based transient simulation:**

  Consider that a N port system network needs to be simulated in the time domain using the macro-modeling approach. The network is represented using the N-port system matrix defined at f frequency samples. In order to simulate this network, it must first be converted into a SPICE compatible format. This is done using a rational function approximation of the system frequency response. If p is the order of the system (if the system has p poles), then the computation of the rational function approximation will require the solution of a $2f$xp matrix. Since f is usually greater than p in most systems, the matrix solution will require $O(f^3)$ operations. In reality since the rational function approximation of a system with a large N is an ill-conditioned problem, the method described in [37] computes the approximation in a iterative fashion using vector fitting. Vector fitting provides better accuracy but still requires the same order of computations. For e.g., the rational function approximation of the 12-port PDN of the IBM HyperBGA package using BEMP required over 10 hrs. to complete. A screen shot of BEMP performing the rational function approximation is shown in Figure 120. It is seen from the figure that inspite of taking 10 hrs to perform rational function approximation, BEMP could not completely capture the system response. BEMP returned three real poles (low-pass filters) and three pairs of complex conjugate poles (band pass filters) to represent the system response accurately up to 1.23 GHz. From Figure 13 it is seen that synthesizing a circuit for a real pole requires 2 lumped elements while that for a complex conjugate pole-pair requires 4 lumped elements respectively.

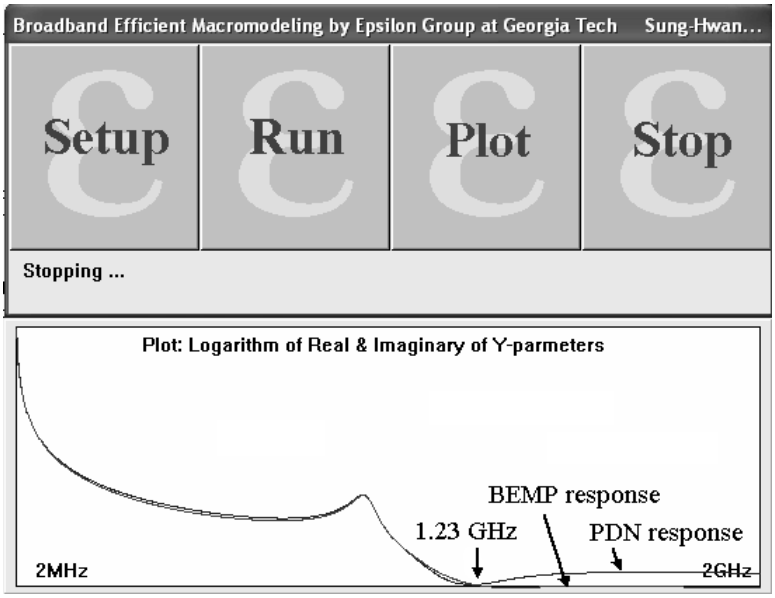

Figure 120: Screen shot of BEMP macro-modeling the PDN

Hence for a N-port common pole system, if p_r is the number of real poles and p_c is the number of complex conjugate pole pairs, then the SPICE netlist representing the system will have $(2p_r+4p_c)N^2$ elements. Hence the SPICE netlist representing the 12-port PDN in the abpve system will have 2,592 lumped elements. Adding the models for the SDN resulted in a complete system matrix of about 3000 elements. To perform a transient simulation on this netlist, SPICE will have to setup an Modified Nodal Analysis (MNA) matrix that would need to be solved at each time step. Assuming there are no non-linear sources, SPICE will need to perform LU decomposition just once and then use back-substitution for each of the remaining time steps. Since this process requires $O(n^2)$ operations where n is the size of the MNA matrix, the transient simulation of $(2p_r+4p_c)N^2$ elements would require $O((p_r+p_c)^2N^4)$ operations at each time step. The simulation of the IBM HyperBGA package in HSPICE for a random bit source, 100 bits in length, required over 20 minutes to complete.

- **SFG based transient simulation:**

  The SFg based transient simulation of the above problem requires two steps. First the N-port system matrix is converted into impulse responses using IZT. Since this requires the inversion of a fxf Vandermonde matrix where f is the number of frequency

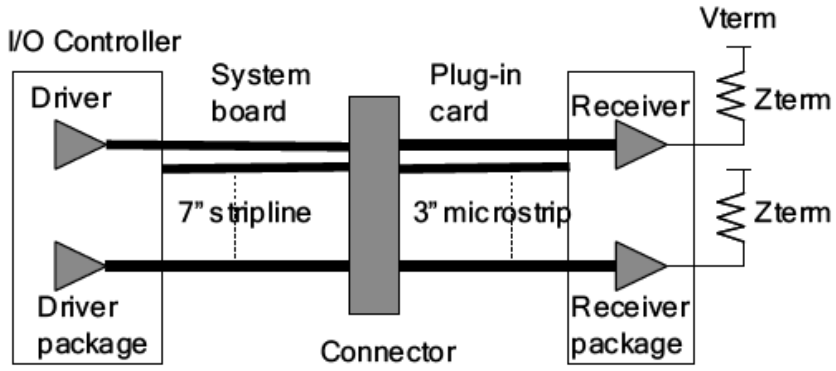

Figure 121: Schematic of a PCI-X bus

samples in the data, the first step requires $O(f^3)$ operations. The computation of the impulse responses of the 24-port system matrix representing the IBM HyperBGA package required a little over 8 mins. Let l be the length of each impulse response. It has been shown in the previous chapter that the transient solution of a N-port S-parameter matrix using SFGs requires atleast N^2 convolutions to be performed at each time step. Since l is the length of each impulse response, each of the convolutions would require $O(llogl)$ operations. Computing the solution of the system of SFG equations will require an additional $O(N^2)$ operations at each time step. Hence for each time step the SFG based transient simulation technique will require $O((llogl + 1)N^2)$ operations. Comparing this with the complexity of the macro-modeling based approach, it can be seen that SFG based approach is of $O(N^2)$ complexity as compared to the $O(N^4)$ complexity of the macro-modeling based approach, and hence is considerably more efficient. The SFG based simulation of the IBM HyperBGA package required just under 4 minutes to complete.

5.4.2 PCI Express I/O interface

The example considered in this study is a PCI-X (peripheral component interface - express) 533 MHz local bus that is used to interconnect peripheral components and add-in cards to the processor and memory systems in a computer. A schematic of the PCI-X bus is shown in Figure 121. An I/O interface circuit in this system, was modelled in [35] as shown in Figure 122. The system consists of an I/O driver, a 7 in. stripline transmission line

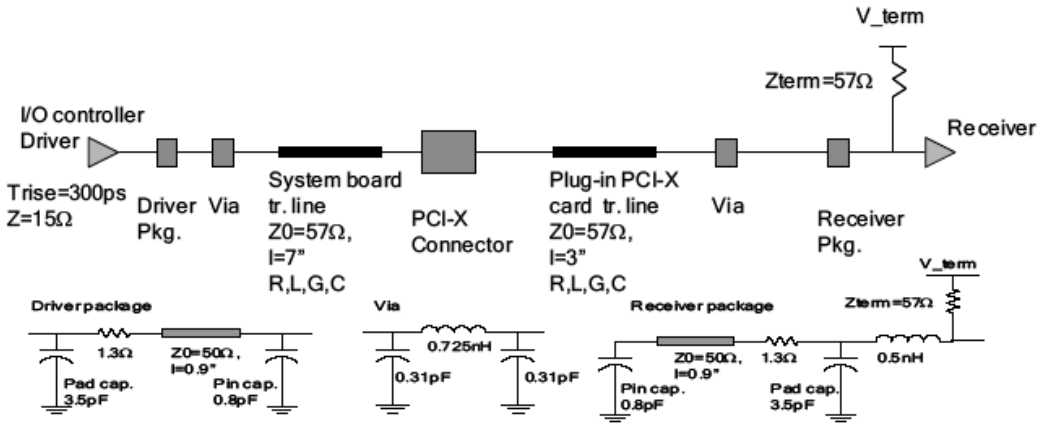

Figure 122: Simulation model for the PCI-X I/O interface

on the system board, a plug-in card connector, a plug-in card with 3 in. of microstrip interconnect, and a receiver on the plug-in card. The nominal values used for modeling the system components are indicated in Figure 122 and listed in Table 11. The individual modules of the system were modelled and integrated using ADS. The system network was first excited using a random bit pattern driver operating at 770 MHz with a rise time of 250 ps. The object of the experiment was to analyze the performance of the 533 MHz I/O interface when overclocked at higher frequencies. The eye-diagrams obtained at the input of the receiver using causal and non-causal simulations are shown in Figures 123 and 124 respectively. The figures show that the bus performs satisfactorily under when overclocked at 770 MHz. The simulation results are summarized in Table 12. It is seen that in this experiment the causality violations actually cause the eye-opening to increase by 6 mV. To understand this phenomenon, a portion of the transient output obtained using the causal and non-causal simulations is plotted in Figure 125. The figure also plots the random bit pattern input along side the outputs. From the figure it is seen that unlike other test cases described previously in this dissertation, the non-causal response of the PCI-X I/O interface circuit actually overshoots in a direction opposite to the input transition i.e., it overshoots in the negative direction for a low-to-high transition and vice-versa. This results in a smaller eye opening for the causal simulation output. This indicates that the change in the eye-opening due to causality violations is system dependant. For some systems, the causality violations can cause a reduction in the eye-opening while for other systems they

Table 11: Component values for the PCI-X I/O interface model

Characteristic impedance of driver package	50 Ω
Driver package trace length	0.9 in.
Characteristic impedance of receiver package	50 Ω
Receiver package trace length	0.9 in.
Characteristic impedance of board trace	57 Ω
System board trace length	7 in.
Characteristic impedance of card trace	57 Ω
Plug-in card trace length	3 in.
Components in the driver package model	3.5 pf
	0.8 pf
	1.3 Ω
Components in the receiver package model	3.5 pf
	0.8 pf
	1.3 Ω
Components in the PCI-X connector model	0.31 pf
	0.31 pf
	0.725 nH

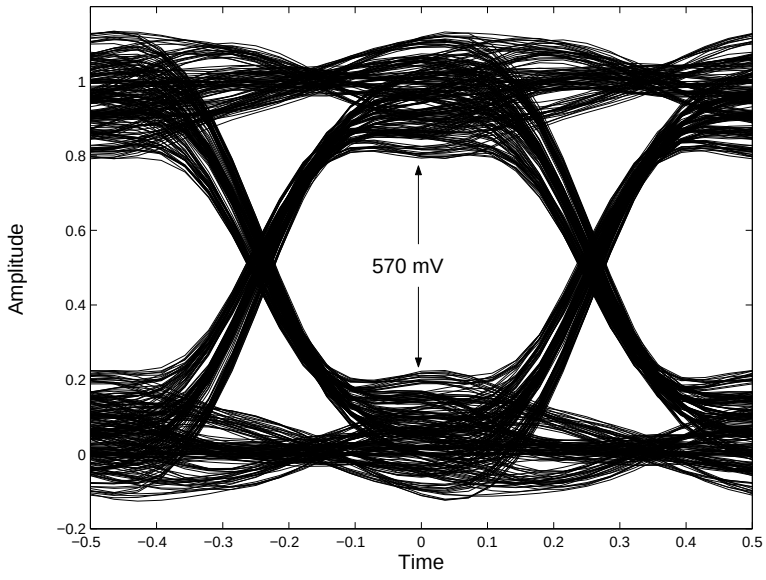

Figure 123: Causal simulation of PCI-X I/O interface

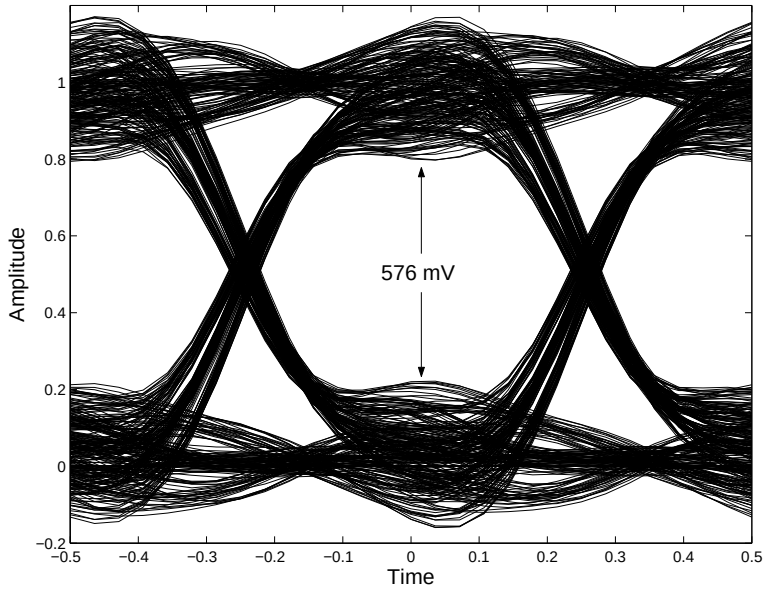

Figure 124: Non-causal simulation of PCI-X I/O interface

Table 12: Simulation results for PCI-X I/O interface

Characteristic impedance	57 Ω
Bandwidth of system response	2.5 GHz
Rise time of driver	250 ps
Operating frequency of the drivers	770 MHz
Random bit pattern length	1000 bits
No. of ports in the system network	3
Eye-opening with causal simulation	570 mV
Eye-opening with non-causal simulation	576 mV

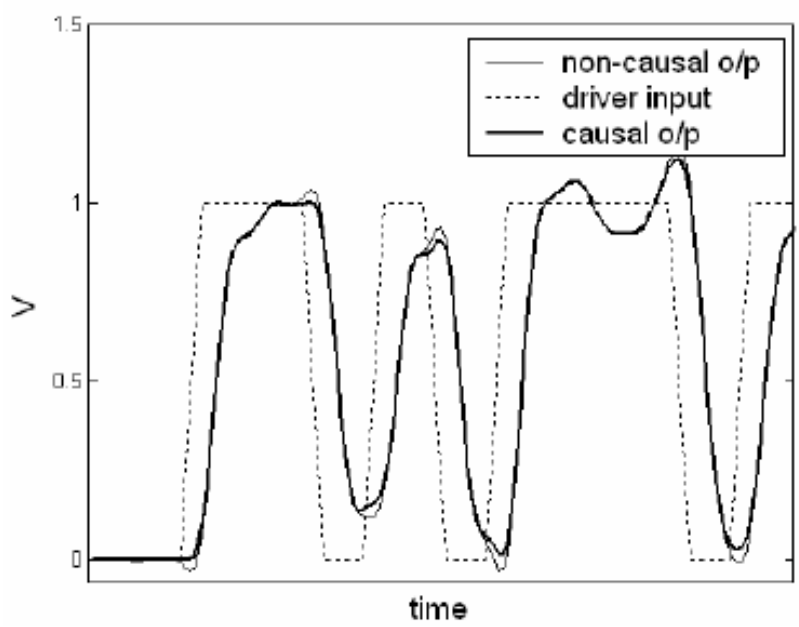

Figure 125: Transient output of the PCI-X I/O interface circuit

Table 13: Simulation results for overclocking of the PCI-X I/O interface

Clock freq	Rise time	Causal eye	Non-causal eye	error	%error
770 MHz	250 ps	570 mV	576 mV	6 mV	1.05
1 GHz	200 ps	611 mV	630 mV	19 mV	3.1
1.5 GHz	125 ps	576 mV	610 mV	34 mV	5.9
2 GHz	100 ps	465 mV	495 mV	35 mV	7.6
2.5 GHz	100 ps	251 mV	274 mV	23 mV	9.16

lead to an increase. Therefore to accurately simulate the transient response of a system, it is important to enforce causality in the transient simulation.

Since the PCI-X bus I/O interface circuit provides a sufficiently clean eye at 770 MHz, the driver operating frequency was cranked up further to analyze the performance of the circuit in the GHz range. To simulate such high frequencies, the PCI-X I/O interface circuit was modelled up to 5 GHz. Using this model, the system was simulated for driver frequencies up to 2.5 GHz with rise time of 100 ps. The comparison of the eye-diagrams obtained for each case with causal and non-causal simulations is shown in Figures 126 through 129 and the results are summarized in Table 13. It is seen that as the driver operating frequency increases and its rise time decreases, the eye-opening on the PCI-X I/O interface circuit diminishes rapidly. Further more as the eye-openings decrease, the impact of the causality

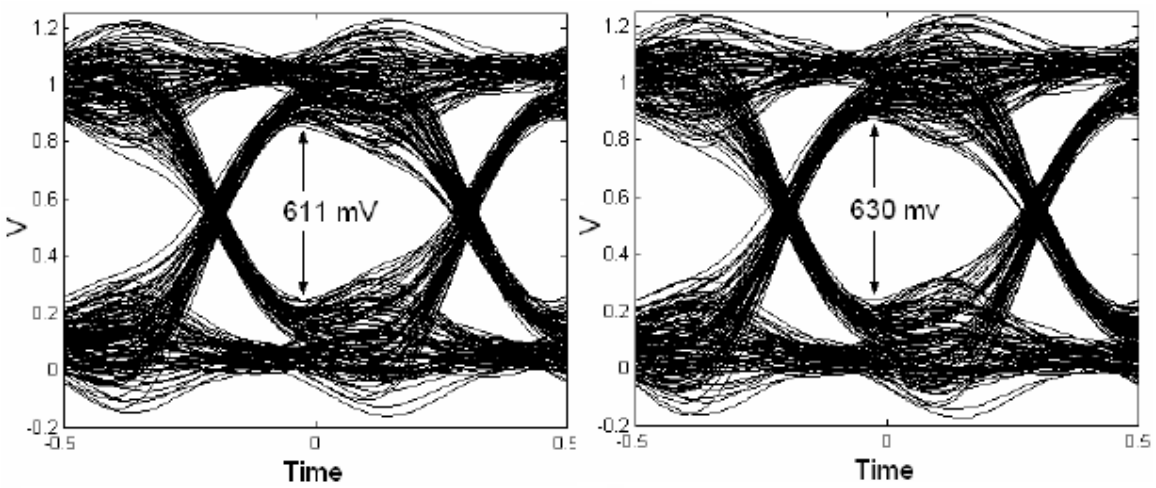

Figure 126: Causal (left) and non-causal (right) simulation of the PCI-X I/O interface circuit at 1 GHz

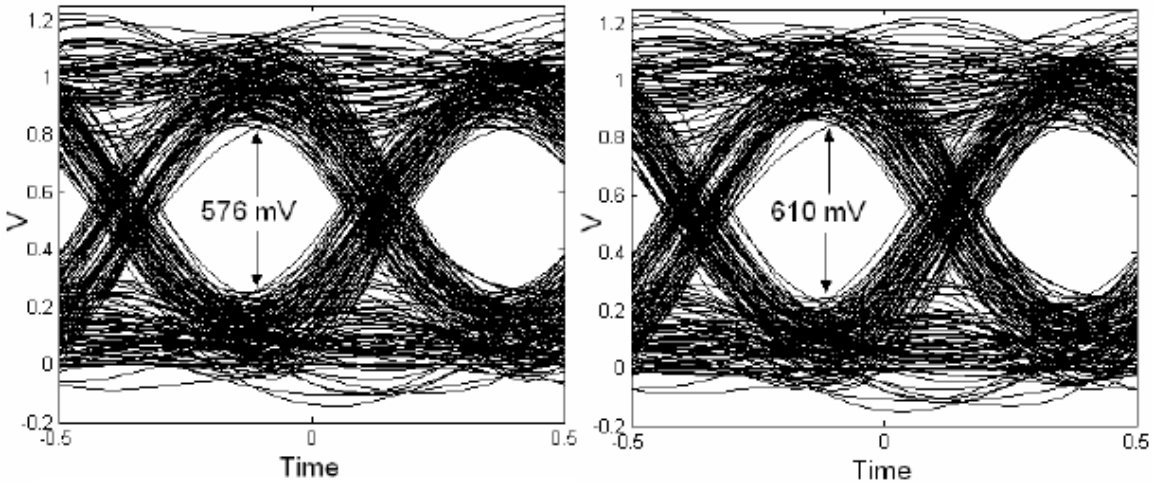

Figure 127: Causal (left) and non-causal (right) simulation of the PCI-X I/O interface circuit at 1.5 GHz

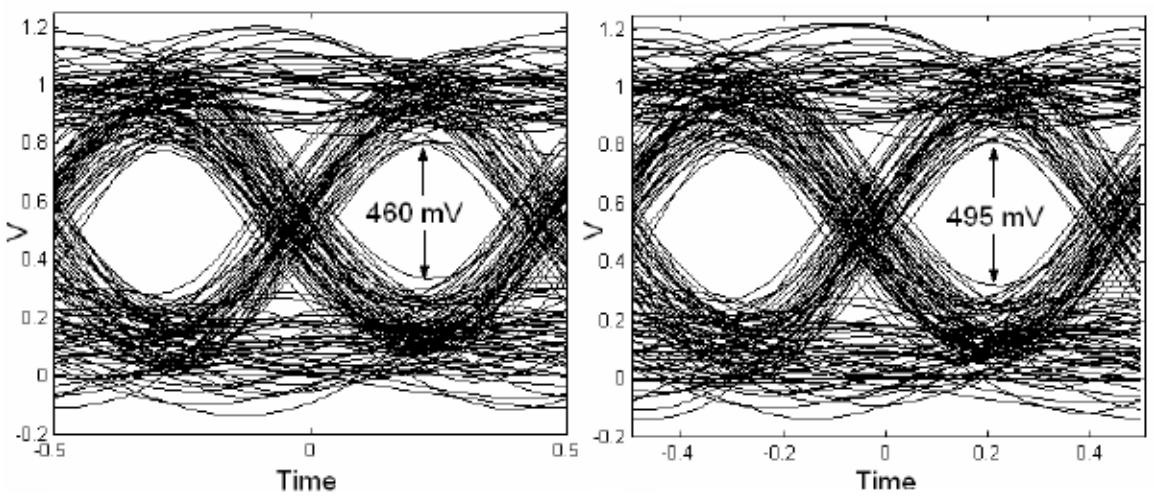

Figure 128: Causal (left) and non-causal (right) simulation of the PCI-X I/O interface circuit at 2 GHz

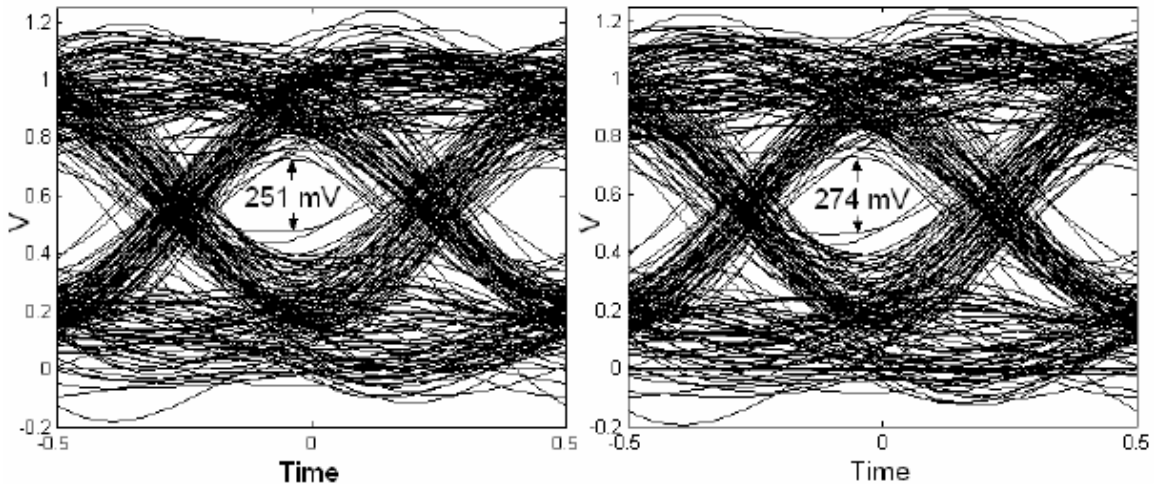

Figure 129: Causal (left) and non-causal (right) simulation of the PCI-X I/O interface circuit at 2.5 GHz

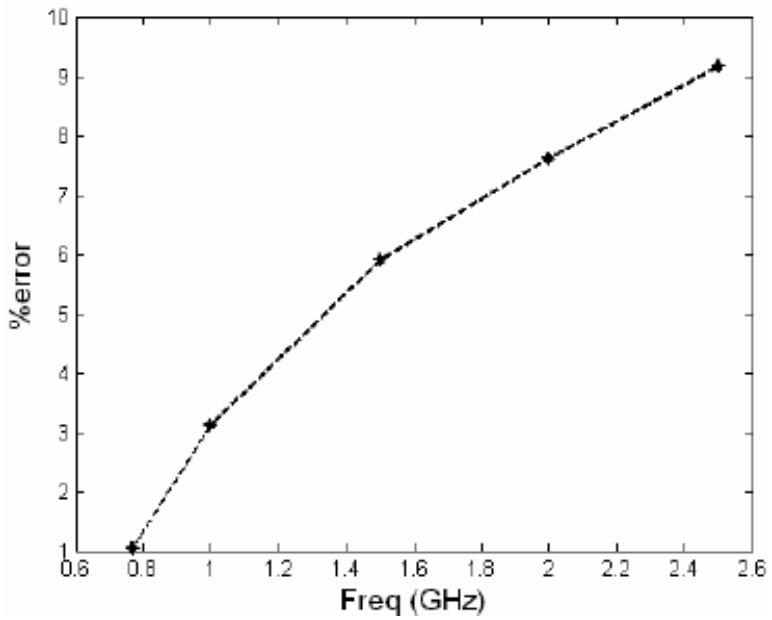

Figure 130: Percentage error due to causality violations against operating frequency

violations on the accuracy of the transient simulation increases. Thus, while the causality violations resulted in only about 1% error at 770 MHz, they result in nearly 10% error at 2.5 GHz. Figure 130 plots the percentage error due to causality violations against the operating frequency of the driver. In the future as the operating frequencies of the different modules in a computer system increase even further, the causality violations will play a major role in determining the accuracy of a transient simulation.

5.5 Summary

In this chapter the transient co-simulation methodology developed in this dissertation has been applied on a variety of test systems. These include simple systems consisting of single and coupled transmission lines to more complex systems consisting of multiconductor interconnect buses with non-ideal references. The test cases also include a couple of real world examples in the form of an IBM HyperBGA package and a PCI-X I/O interface circuit. For most of the test cases, the system networks have been simulated using the causal as well as the non-causal SFG equations. The key observations that can be made from these test cases are:

1. Causality violations are an important problem in transient simulation of passive systems and if unaccounted for, can lead to considerable simulation error. For digital systems with interconnects, where the SI analysis is performed using eye-diagrams, causality violations cause an artificial change in the opening of the eye. For moderately sized systems like the the 32-bit interconnect bus simulated in this chapter, this error was seen to be in excess of 150 mV. As operating frequencies and system size increase, this problem is expected to worsen.

2. The switching noise that is generated in the PDN of a system couples into the SDN causing a degradation in the signal quality. In order to accurately predict the system performance in the presence of such parasitics effects, this coupling between the SDN and the PDN has to be simulated accurately. The test case that simulates the noise coupled on to a quiet line from a neighboring active bus clearly demonstrates this need. In that test case it is seen that moving the quiet line further and further away from the active bus does not always result in a decrease in the coupled noise. To accurately predict the coupling a co-simulation is necessary. The co-simulation methodology proposed in this dissertation is able to accurately simulate the coupling in the system.

CHAPTER VI

CONCLUSION AND FUTURE WORK

As the complexity of interconnects and packages increases, and the rise and fall time of the signal decreases, the electromagnetic effects in distributed passive structures become an important factor in determining the system performance. Hence while designing complex digital systems, these electromagnetic parasitic effects need to be modelled and simulated accurately. An important parasitic effect in the design of power distribution for high-speed systems is the occurrence of SSN. SSN can significantly impact the performance of a system by causing false triggering of gates, excessive clock skew, and a general degradation of the system signal integrity. An accurate prediction of the SSN generated in a system requires a knowledge of the high frequency transient currents that are injected into the system PDN. Existing techniques for determining these transient currents are not sufficiently accurate. One of goals of this research work is the development of a technique to accurately extract the switching noise currents in high-speed digital systems. The extracted switching currents would provide a way to accurately simulate the SSN generated in the PDN of a digital system.

Another important parasitic effect observed in digital systems is the coupling of SSN on to the signal network of the system. When SSN couples on to the SDN, it appears as a noise voltage on the signal lines. To accurately predict this phenomenon, the SDN and the PDN of a system need to be simulated together. Since these two system modules are traditionally simulated separately, the simulations fail to account for the coupling between them. Furthermore, the transient simulation techniques used to simulate these modules (especially the SDN) suffer from two major drawbacks: 1) they are not scalable and hence cannot be applied to large sized systems, and 2) the time domain simulations violate causality. One of the goals of this research work is to develop a transient co-simulation methodology

for simulating the SDN and the PDN in a digital system. The methodology should accurately capture the coupling between the two modules, preserve their inherent properties like passivity and causality, and be scalable in order to handle large sized systems.

6.1 Conclusion

Based on the work presented in Chapters 2 to 5, the contributions of this research can be listed as follows:

1. A wavelet based technique that de-noises a measured transient waveform has been developed. The technique helps in de-noising the measured transient switching noise voltage waveforms that are required for extracting switching noise currents in digital systems. The effectiveness of the proposed technique has been demonstrated on simulated as well as measured transient data. In both the cases the developed de-noising technique has been shown to extract all the dominant resonances from a transient waveform in a noisy environment.

2. Using the transient waveform de-noising technique, a measurement based method to extract the switching noise current signatures in packaged digital systems has been developed. The extracted switching noise current signatures have magnitude as well as phase information, and can be used to simulate SSN in the time or the frequency domain. The method has been successfully applied to extract the switching noise currents in the power distribution network of a functioning Sun Microsystems workstation and an IBM Power5 microprocessor. The extracted switching noise currents have been used in accurately simulating the SSN in the PDN.

3. A technique that extracts the port-to-port delays in a network directly from its multiport frequency response parameters has been developed. The technique accepts multiport S, Y, or Z parameters and performs a Hilbert Transform based separation on the frequency responses to extract the delays between the various ports. The technique has been validated on simulated and measured frequency response data. The technique has also been extended to extract the even and odd mode delays in

mixed-mode passive structures.

4. A simulation technique based on signal flow graphs has been developed for performing transient simulations on multiport frequency response data from passive systems. The SFG formulation process in this simulation technique uses the delay extraction mechanism developed in this dissertation to represent a passive system using causal SFG equations. A solution to these causal SFG equations produces in a transient result that satisfies all the causality criteria. Existing commercial transient simulators do not enforce causality in their transient simulations. A comparison of the developed simulation technique with existing transient simulators demonstrates the causality enforcement and improved accuracy provided by the developed technique.

5. To enhance the simulation efficiency of the developed transient simulation technique, an algorithm that computes a convolution integral in a more efficient way has been implemented and integrated into the simulation technique. The fast-convolution technique is based on Lagrange approximation and enables a reduction in the computational complexity of the convolution integral from $O(N^2)$ to $O(NlogN)$ where N depends on the problem size. The performance improvement achieved by this algorithm has been shown in the context of a simulation of a 64-bit interconnect bus referenced to non-ideal power ground planes. It is seen that the fast convolution implementation provides a 2.5X speedup over a conventional implementation of convolution.

6. The scalability of the proposed transient simulation technique has been demonstrated through the simulation of a 130-port system using the developed technique. Conventional simulation methods that incorporate macro-modeling suffer from poor scalability. These methods can only simulate multiport passive networks of the order of 25 30 ports. For higher number of ports, these methods have accuracy and convergence issues. The transient simulation method developed in this dissertation has been shown to successfully handle over a 100 ports.

7. The developed transient simulation methodology has been used to perform a co-simulation of the SDN and the PDN in a packaged digital system. The SDN and

the PDN in the system are integrated using modal decomposition techniques and the integrated system network is simulated using the SFG based transient simulation framework. The transient co-simulation accurately captures the coupling between the two modules, and provides valuable insight on the signal integrity performance of the system that would otherwise have not been possible. In this work the transient co-simulation technique has been applied on a variety of test cases including stripline interconnects, coupled transmission lines, multiconductor buses, an IBM HyperBGA package and a PCI-X I/O interface circuit. In most cases it is seen that the developed transient co-simulation technique provides for a more accurate analysis of the eye-diagrams on the signal lines and/or the SSN coupling in the system.

6.2 Future work

Passivity is an important property of the power and signal distribution networks at the package and board level. The property of passivity requires that a passive circuit does not create energy. It only dissipates or transfers the energy provided to it through excitation sources [37]. The passivity conditions for a multi-port network ($G(s)$) are two-fold: 1) $[G(s*)]$=$[G*(s)]$ for all s, where * is the complex conjugate operator, and 2) $[G(s)]$ is a positive real matrix, i.e., the product $z*^{T}[G^{T}(s*)+G(s)]z>0$, for all s with $Re(s)>0$ and any arbitrary vector z. If these conditions are violated it can result in spurious and unstable oscillations in the result of a transient simulation. Hence passivity enforcement is an important challenge in the simulation domain. Though several algorithms exist for enforcing passivity on various different system representations, none of them address the passivity enforcement on delay-extracted system response matrices. The transient simulation methodology proposed in this dissertation only checks for passivity violations but does not guarantee passivity. Deriving closed form expressions for passive enforcement in delay-extracted system response matrices could be a good extension to the work accomplished in this dissertation.

Another area of extending the work described in this dissertation is the interfacing of the SDN-PDN co-simulation framework with SPICE so that all the non-linear elements in

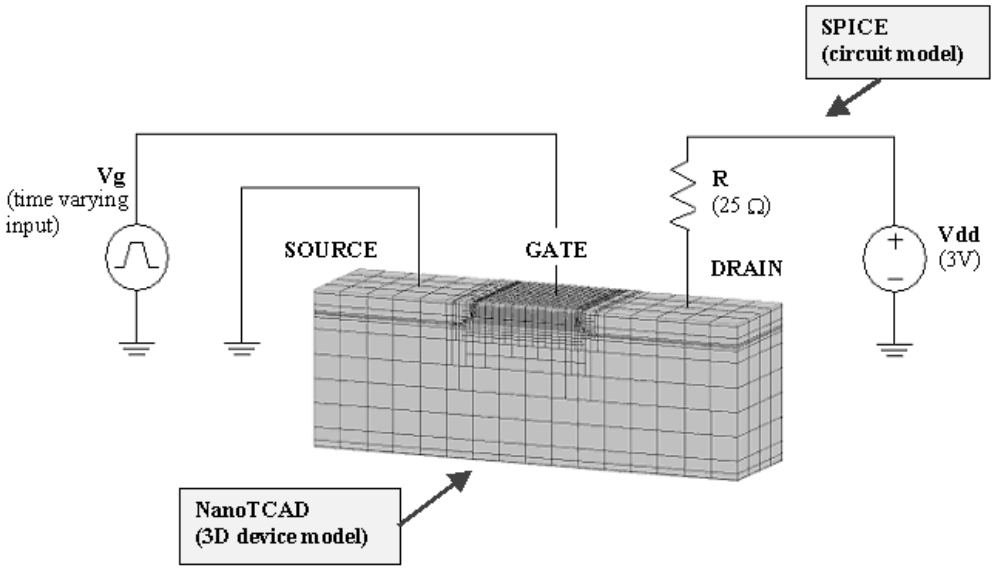

Figure 131: A mixed-node circuit being simulated using the CFDRC developed simulator interface

a system can be co-simulated with the distributed passive modules. Since the SFG based transient simulation proceeds on a time-step basis as does SPICE, the interfacing of the two can be conceptually visualized. Interfacing of external time-domain tools with SPICE has already been carried out in the past. As an example, CFDRC has developed a mixed-mode simulator that has a software coupling mechanism to enable the interface of 2D and 3D semiconductor device simulations with the Berkeley SPICE circuit simulator [4]. An illustration of such a mixed-mode circuit is shown in Figure 131. The simulation engine starts instances of both solvers, coordinates information exchange between both solvers at each time step, and controls the progress of the simulation based on convergence criteria, tolerances etc. A similar approach could be used to interface the SFG based simulation engine with SPICE. Using this interface the passive modules in a packaged digital system can be simulated efficiently using SFGs while all the non-linear elements can be simulated efficiently using SPICE.

6.3 Publications

The following publications have resulted from this work.

- **R. Mandrekar**, M. Swaminathan, S. Chun, "Extraction of current signatures for simulation of simultaneous switching noise in high speed digital systems", Electrical Performance of Electronic Packaging, 2003 27-29 Oct. 2003 Page(s):41 - 44 *(Was awarded the IBM Corp. Best Student Paper Award)*

- **R. Mandrekar**, M. Swaminathan, "Wavelet based nonparametric regression approach for de-noising and modeling of transient switching noise measurements", Electronics Packaging Technology, 2003 5th Conference (EPTC 2003) 10-12 Dec. 2003 Page(s):39 - 44

- **R. Mandrekar**, M. Swaminathan, S. Chun, "Application of wavelets and generalized pencil-of-function method for the extraction of noise current spectrum and simulation of simultaneous switching noise", VLSI Design, 2004. Proceedings. 17th International Conference on 2004 Page(s):995 - 1000

- **R. Mandrekar**, M. Swaminathan, "Extraction of noise current signatures using wavelets in packaged digital systems", Advanced Packaging, IEEE Transactions on [see also Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on] Volume 28, Issue 1, Feb. 2005 Page(s):45 - 56

- **R. Mandrekar**, M. Swaminathan, "Delay extraction from frequency domain data for causal macro-modeling of passive networks", Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on, 23-26 May 2005 Page(s):5758 - 5761 Vol. 6

- **R. Mandrekar**, M. Swaminathan, "Causality enforcement in transient simulation of passive networks through delay extraction", Signal Propagation on Interconnects, 2005. Proceedings. 9th IEEE Workshop on 10-13 May 2005 Page(s):25 - 28

- **R. Mandrekar**, B. Mutnury, M. Swaminathan, M. Cases "Modeling of interconnects, drivers and receivers in packaged systems" Proceedings of IBM Centre for Advanced Studies Conference, Feb. 2005

- J. Choi, V. Govind, **R. Mandrekar**, S. Jaganama, M. Swaminathan, "Noise reduction and design methodology in mixed-signal systems with alternating impedance

electromagnetic bandgap (AI-EBG) structure", Microwave Symposium Digest, 2005 IEEE MTT-S International 12-17 June 2005 Page(s):849 - 852

- **R. Mandrekar**, K. Srinivasan, E. Engin, M. Swaminathan, "Co-simulation of signal and power delivery networks with causality", Electrical Performance of Electronic Packaging, 2005. IEEE 14th Topical Meeting on Oct. 24-26, 2005 Page(s):337 - 340

- **R. Mandrekar**, K. Srinivasan, E. Engin, M. Swaminathan, "Causality enforcement in transient co-simulation of signal and power delivery networks", Accepted for publication in the IEEE Transactions on Advanced Packaging

- K. Srinivasan, **R. Mandrekar**, E. Engin, M. Swaminathan, "Power integrity/signal integrity co-simulation for fast design closure", Accepted for presentation in the Electronic Packaging Technology Conference, 2005

- K. Srinivasan, P. Muthana, **R. Mandrekar**, E. Engin, J. Choi, M. Swaminathan, "Enhancement of signal integrity and power integrity with embedded capacitors in high speed packages", Accepted for presentation in the International Symposium on Quality Electronic Design, 2006

- **R. Mandrekar**, K. Bharath, K. Srinivasan, E. Engin, M. Swaminathan, "System level signal and power integrity analysis methodology for System-In-Package applications", submitted for the Design Automation Conference, 2006

APPENDIX A

TOTAL LEAST SQUARES DECONVOLUTION

Deconvolution is the process of finding the impulse response vector x of a system from the known values of the input $u(t)$ and the output vector b. It involves solving the equation $Ax = b$ where A is given by

$$A = \begin{bmatrix} u(1) & 0 & \cdots & 0 \\ u(2) & u(1) & \cdots & 0 \\ \vdots & \vdots & \ddots & \\ u(n) & u(n-1) & \cdots & u(1) \\ \vdots & \vdots & & \vdots \\ u(m) & u(m-1) & \cdots & u(m-n+1) \end{bmatrix}_{mxn} \tag{74}$$

A normal least squares solution assumes a perfect error-free A to compute a x_{LS} that minimizes $Ax_{LS} = b + r$. A total least squares solution assumes perturbations in b as well as in the input $u(t)$ (and hence in A). Hence it tries to find a solution x_{TLS} which satisfies $(A + E)x_{TLS} = b + r$ such that $[E : r]$ is minimized. E and r are the error matrix and the error vector respectively.

Consider a matrix C given as $C = [A : b]$. The singular value decomposition of C can be written as

$$C = [A : b] = U\Sigma V^H = \sum_{i=1}^{n+1} \sigma_i u_i v_i^H \tag{75}$$

According to the total least squares algorithm proposed in [47], if r is the rank of the matrix A, then x_{TLS} can be found using the $'n+r-1'$ right singular vectors of the matrix C which are associated with its $'n + r - 1'$ smallest singular values.

If $\bar{V}_r$ is a matrix given by

$$\bar{V}_r = \begin{bmatrix} v_{r+1} & \vdots & \cdots & \vdots & v_{n+1} \end{bmatrix} \in C^{(n+1)x(n+1-r)} \tag{76}$$

then the total least squares solution to the problem $(A+E)x_{TLS} = b + r$ is given as

$$\begin{bmatrix} x_{TLS} \\ -1 \end{bmatrix} = \frac{-1}{e_{n+1}^T \bar{V}_r V_r^H e_{n+1}} . \bar{V}_r \bar{V}_r^H e_{n+1} \tag{77}$$

where

$$e_{n+1} = \begin{bmatrix} 0 & 0 & \cdots & 0 & 1 \end{bmatrix} \in R^{(n+1)X1} \tag{78}$$

Using Equation 77, x_{TLS} can be simplified as

$$x_{TLS} = \frac{\left(\sum_{i=1}^{r} v_{n+1,i} \begin{bmatrix} v_{1,i} & v_{2,i} & \cdots & v_{n,i} \end{bmatrix}^H \right)}{\left(1 - \sum_{i=1}^{r} v_{n+1,i}^2 \right)} \tag{79}$$

APPENDIX B

MIXED MODE S-PARAMETERS

For a differential transmission line structure that consists of a pair of transmission lines referenced to a common ground (shown in Figure 132), the standard 4-port S-parameters are defined as

$$S_{ij} = \left.\frac{b_i}{a_j}\right|_{\substack{a_k = 0 \\ k \neq j}} \tag{80}$$

where a_i and b_j are the incident and reflected waves at the respective ports when they terminated with the characteristic impedance. Each of the ports in this case is referenced to a common ground. The standard S-parameters can be expressed in matrix form as $[b] = [S][a]$, where $[a]$ and $[b]$ are 4x1 column vectors, and $[S]$ is a 4x4 matrix. The mixed-mode scattering parameters of this structure as defined in [14] are obtained by defining differential-mode and common-mode power waves. For this purpose, ports 1&2 are grouped together as one "differential" port, while ports 3&4 are grouped together as the other. A differential-mode signal is generated at the first differential port by exciting port 1 with respect to port 2. A common-mode signal is generated by exciting both the ports equally with respect to ground. Hence the mixed-mode incident and reflected power waves at the

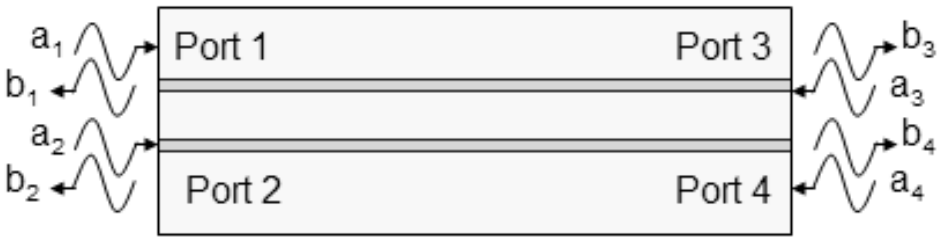

Figure 132: Incident and reflected power waves in a 4-port network

two "differential" ports can be given as

$$\begin{aligned} a_{d1} &= \tfrac{a_1 - a_2}{\sqrt{2}} \quad a_{c1} = \tfrac{a_1 + a_2}{\sqrt{2}} \\ b_{d1} &= \tfrac{b_1 - b_2}{\sqrt{2}} \quad b_{c1} = \tfrac{b_1 + b_2}{\sqrt{2}} \\ a_{d2} &= \tfrac{a_3 - a_4}{\sqrt{2}} \quad a_{c2} = \tfrac{a_3 + a_4}{\sqrt{2}} \\ b_{d2} &= \tfrac{b_3 - b_4}{\sqrt{2}} \quad b_{c2} = \tfrac{b_3 + b_4}{\sqrt{2}} \end{aligned} \tag{81}$$

A convenient matrix representation of these equations is given by

$$\begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \tag{82}$$

$$\begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} \tag{83}$$

If a matrix M is defined as

$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \tag{84}$$

then Equations 82 and 83 can be represented compactly as $a^{mm} = Ma^{std}$ and $b^{mm} = Mb^{std}$ respectively. Now from the definition of mixed-mode S-parameters (S^{mm}) as given in [14] we have

$$\begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} S_{dd11} & S_{dd12} \\ S_{dd21} & S_{dd22} \end{bmatrix} & \begin{bmatrix} S_{dc11} & S_{dc12} \\ S_{dc21} & S_{dc22} \end{bmatrix} \\ \begin{bmatrix} S_{cd11} & S_{cd12} \\ S_{cd21} & S_{cd22} \end{bmatrix} & \begin{bmatrix} S_{cc11} & S_{cc12} \\ S_{cc21} & S_{cc22} \end{bmatrix} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} \tag{85}$$

which can be written in short as

$$b^{mm} = S^{mm} a^{mm} \tag{86}$$

Using the conversion from a^{mm} and b^{mm} to a^{std} and b^{std} respectively we get

$$S^{mm} = M S^{std} M^{-1} \tag{87}$$

In this dissertation, the mixed-mode S-parameters thus obtained have been used to extract the even and odd mode delays embedded in a differential structure. For example, S_{dd12} will give the odd-mode delay of a differential transmission line while S_{cc12} will give its even-mode delay.

APPENDIX C

NODAL ADMITTANCE METHOD AND STAMP RULE

Consider a circuit presented in Figure 133. The admittance matrix for this circuit is given by $[Y]$ where

$$[Y]\begin{bmatrix} V_{N1} \\ V_{N2} \\ V_{N3} \end{bmatrix} = \begin{bmatrix} I_{N1} \\ 0 \\ 0 \end{bmatrix} \tag{88}$$

To derive the nodal admittance matrix for the circuit, the following rules can be used.

1. A passive admittance connected between nodes i and j contributes a term to the nodal admittance matrix given by

$$\begin{bmatrix} & \vdots & & \vdots & \\ \cdots & Y & \cdots & -Y & \cdots \\ & \vdots & & \vdots & \\ \cdots & -Y & \cdots & Y & \cdots \\ & \vdots & & \vdots & \end{bmatrix} \tag{89}$$

   where the Y's are located at the intersections of the i^{th} and j^{th} rows and columns respectively. This is also called the Stamp rule. If i is the reference node then the

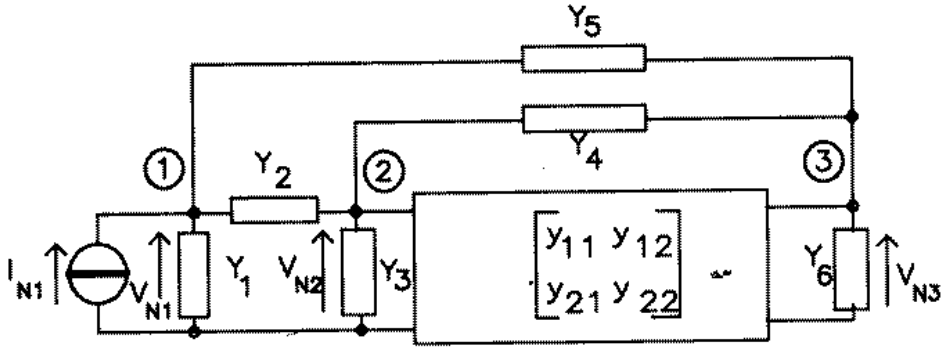

Figure 133: A circuit to illustrate the principles of Nodal Admittance method

entry is reduced to a single Y on the main diagonal in the element Y_{jj}

2. An independent current source between nodes i and j, in the direction $i \rightarrow j$, contributes a term to the right hand vector I_N as

$$\begin{array}{c} \\ i \\ \\ j \\ \\ \end{array} \begin{bmatrix} \vdots \\ -I \\ \vdots \\ I \\ \vdots \end{bmatrix} \tag{90}$$

3. An independent voltage source with source admittance y between nodes i and j, in the direction $i \rightarrow j$, contributes a term to the right hand vector I_N as

$$\begin{array}{c} \\ i \\ \\ j \\ \\ \end{array} \begin{bmatrix} \vdots \\ -yE \\ \vdots \\ yE \\ \vdots \end{bmatrix} \tag{91}$$

4. Multi-terminal elements represented using their admittance matrices can be integrated into the system admittance matrix as follows. Consider a three terminal device connected between nodes i, j, and k. This can integrated into the system matrix as given by

$$\begin{bmatrix} & \vdots & & \vdots & & \vdots & \\ \cdots & y_{11} & \cdots & y_{12} & \cdots & y_{13} & \cdots \\ & \vdots & & \vdots & & \vdots & \\ \cdots & y_{21} & \cdots & y_{22} & \cdots & y_{23} & \cdots \\ & \vdots & & \vdots & & \vdots & \\ \cdots & y_{31} & \cdots & y_{32} & \cdots & y_{33} & \cdots \\ & \vdots & & \vdots & & \vdots & \end{bmatrix} \begin{array}{c} \\ i \\ \\ j \\ \\ k \\ \\ \end{array} \tag{92}$$

Using these rules, the nodal admittance matrix of the circuit in Figure 133 can be computed to be

$$\begin{bmatrix} Y_1 + Y_2 + Y_5 & -Y_2 & -Y_5 \\ -Y_2 & Y_2 + Y_3 + Y_4 + y_{11} & -Y_4 + y_{12} \\ -Y & -Y_4 + y_{21} & Y_4 + Y_5 + Y_6 + y_{22} \end{bmatrix} \tag{93}$$

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