DESIGN OF BALUNS AND LOW NOISE AMPLIFIERS IN INTEGRATED MIXED-SIGNAL ORGANIC SUBSTRATES

A Dissertation
Presented to
The Academic Faculty

by

Vinu Govind

In Partial Fulfillment
Of the Requirements for the Degree
Doctor of Philosophy in Electrical and Computer Engineering

Georgia Institute of Technology

August 2005

TABLE OF CONTENTS

Acknowledgements **iv**

List of Tables **x**

List of Figures **xi**

Summary **xvii**

Chapter 1: Introduction **1**

1.1. Multiband Radio Architectures 4

1.2. Mixed-Signal Integration 8

1.2.1. Low Temperature Co-fired Ceramic (LTCC) Technology 13

1.2.2. Organic Technology 16

1.3. Organic SOP-Based Mixed-Signal System Integration 21

1.3.1. Design of Multiband RF Components 23

1.3.2. Design Partitioning 24

1.3.3. Measurement and Analysis of Signal Coupling 26

1.3.4. Research Objectives 27

1.4. Research Accomplishments 32

1.4.1. Original Contributions 34

1.5. Dissertation Outline 35

Chapter 2: Design of Baluns for Multiband Radios **37**

2.1. Multiband Baluns 38

2.1.1. Theory 43

2.1.2. Design 48

2.1.3. LCP Based SOP Technology for Large Area Manufacturing 49

2.1.4. Fabrication and Measurements 52

2.2. Extension of the Theory of Multiband Marchand Baluns – Wideband Singleband Baluns 57

2.2.1. Design, Fabrication and Measurements 57

2.3. Narrowband Lumped-Element Baluns 64

2.3.1. Design 65

2.3.2. Fabrication and Measurements 66

2.4. Summary 71

Chapter 3: Design of Filter-Balun Networks **73**

3.1. Baluns with Frequency Rejection 74

3.2. Cascaded Filter-Baluns 82

3.2.1. Implementation 83

3.3. Summary 87

Chapter 4: Design of Low Noise Amplifiers Using Embedded Passives **88**

4.1. Chip-Package Co-Design of CMOS LNAs 91

4.1.1. Noise Analysis 94

4.1.2. Inductor Optimization 97

4.2. Multiple Embedded Passives: Analog-Analog Signal Coupling 103

4.2.1. Modeling – Using Field Solvers 107

4.2.2. Modeling – Using Transmission Lines 110

Chapter 5: Digital-Analog Coupling in Mixed Signal Integration **115**

5.1. EMI Based Noise Coupling 119

5.1.1. Indirect Coupling 121

5.1.2. Direct Coupling 124

5.2. Power Supply Based Noise Coupling 128

5.3. Electromagnetic Isolation 132

5.4. Mixed-Signal System Integration Using EBG-Based Power Distribution 137

5.5. Wideband Noise Suppression 142

5.6. Summary 143

Chapter 6: Conclusions and Future Work **145**

6.1. Future Work 147

Appendix A: Publications Resulting from this Research **149**

Appendix B: Patents and Invention Disclosures Resulting from this Research 152

References 153

LIST OF TABLES

Table 1.1 Comparison of discrete, SOC, LTCC, MCM-D/TFOS and SOP-L integration technologies. 20

Table 2.1. Measured performance of the balun. 55

Table 2.2. Performance summary of the balun, with a comparison with a commercially available Marchand balun from Anaren, Inc. 63

Table 2.3. Performance summary of the balun, with a comparison with a commercially available LTCC balun (*Note: The Murata balun was chosen for comparison because it specs the lowest loss for an 0805 balun in the market today. However, the amplitude and phase imbalance information was not available for the LDB21G410C-001. Typical industry standard numbers have been used for the imbalance comparisons). 70

Table 3.1. Measured performance of the filter-balun, with a comparison with a commercially available LTCC filter-balun from Soshin. 86

Table 4.1. Survey of past work done on CMOS LNAs for long-distance communication protocols. 91

Table 4.2. Variation of inductor Q with area. 100

LIST OF FIGURES

Figure 1.1. Global mixed-signal market, and its composition 2

Figure 1.2. a) Multiband architecture, with each device operational at a single band, and switching between frequency bands in the baseband. b) Concurrent multiband architecture, with each component functional at multiple frequency bands. 5

Figure 1.3. Switched semi-concurrent multiband receiver architecture, showing four paths with each path supplying one signal concurrently to the baseband processor. Paths (i) and (ii) are multiband in functionality, with the selector switch between the SIMO filter and the rest of the front-end circuitry determining the choice of signal to pass-through. Paths (iii) and (iv) are singleband in functionality. 7

Figure 1.4. a) Printed Wiring Board (PWB) based integration, with packaged chips and passives assembled onto a PWB substrate b) SOC-based integration, with on-chip passives c) SOP-based integration, with embedded passives in the package. 12

Figure 1.5. LTCC based integrated Bluetooth transceiver module from Kyocera. 14

Figure 1.6 Embedded passives on **a**) MCM-D substrate. b) TFOS substrate. c) SOP-L (Vialux™) substrate. 17

Figure 1.7. Mixed-signal SOP-based test vehicle, with integration of semi-concurrent multiband RF front-end and high-speed digital computing. 28

Figure 1.8. SOP implementation, with heterogenous MCM-L substrate. Multiple chips, some low-profile passive components and a few discrete passives are attached to the top, and the whole structure is overmolded. 29

Figure 2.1. Functional representation of a balun. 37

Figure 2.2. a) Coaxial balun b) Simplified schematic 39

Figure 2.3. S-parameter simulation of the balun showing input match (S11) and power loss (S21 and S31) in the 800 MHz and 2.1 GHz frequency bands. 42

Figure 2.4. Schematic of the new balun, with two frequency dependent impedances (*X/2*) added in series with the load. 43

Figure 2.5. Plot of $F_1(\theta)$ and $F_2(\theta)$ with respect to frequency a) X=1.5pF b) X=10nH 46

Figure 2.6. S-parameter simulation of the balun, showing input match (S11) and power loss (S21 and S31) in the 830 MHz and 1.93 GHz frequency bands. 49

Figure 2.7. Large area manufacturing process. 50

Figure 2.8. a) 3-metal layer organic stack-up and b) photograph of the balun fabricated on LCP substrate. The device measures 1.5 cm x 0.6 cm, including the CPW ground rings and probe-pads. 53

Figure 2.9. Simulated (Sonnet) and measured results for the fabricated balun a) Input match (S11) b) Power transfer (S21 and S31). Solid line with dots represent measured values, dashed line represents simulated results. 54

Figure 2.10. Measured a) amplitude and b) phase imbalance for the balun. 56

Figure 2.11. a) Cross-section of the substrate. b) Photograph of a cross-section. 58

Figure 2.12. a) Layout of the planar balun, and b) the cross-section of the device cut along the A-A’ axis. 59

Figure 2.13. a) Plot of Im(Z_d) vs. frequency showing the zero crossings (using the optimized values for L_x and Z_{ab}) b) Variation of S_{11} with frequency, calculated using (2). 60

Figure 2.14. Photograph of the balun. 61

Figure 2.15. Measured balun response a) S_{11}, S_{21} and S_{31} b) amplitude and phase imbalance. 62

Figure 2.16. Lattice balun schematic. 66

Figure 2.17. 4-metal layer stack-up with high-K dielectric layer. 67

Figure 2.18. a) Photograph of the fabricated 9'x12' panel showing the baluns laid out in six coupons, and b) close-up of the device after dicing, showing the input and output ports. 67

Figure 2.19. Measured values for S11, S21 and S31. 68

Figure 2.20. Measured values for a) Amplitude imbalance and b) Phase imbalance. 69

Figure 3.1. Functional block diagram of a receiver showing the filter and balun. 73

Figure 3.2. Lumped-element model of a capacitor. 75

Figure 3.3. Matching network schematic. 76

Figure 3.4. a) 1.2pF capacitor layout, and b) simulated response 77

Figure 3.5. Simulated response of the matching network, with without the capacitor resonance 78

Figure 3.6. Lattice balun with inductors and capacitors replaced with resonators. 79

Figure 3.7. Simulated response of the balun. 79

Figure 3.8. Modified Marchand balun for operation in the 5-6GHz, with resonators for frequency selection. 80

Figure 3.9. Simulated response (S21) of the balun. 81

Figure 3.10. Filter-balun schematic. 82

Figure 3.11. LCP stack-up used to implement the filter-baluns. 83

Figure 3.12. Photograph of the fabricated 12"x18" panel showing the devices laid out in six coupons, and close-up of the devices showing probe pads. 84

Figure 3.13. Measured and modeled values of S11, S21 and S31. Dotted line shows Sonnet simulations while continuous line shows the measured data.. 85

Figure 3.14. Measured amplitude and phase imbalance. 85

Figure 4.1. Functional block diagram of a receiver showing the LNA. 88

Figure 4.2. Classical LNA design, showing matching networks. 90

Figure 4.3. LNA with inductive degeneration. R_g and R_s are parasitic resistances of the inductors L_g and L_s. The bias circuitry has not been shown for simplicity's sake. 90

Figure 4.4. Variation of *NF* with transistor width (for different values of Q_g), for a 1.9 GHz CMOS LNA designed for the AMI 0.5μ process. 95

Figure 4.5. Variation of *NF* with Qg, for a 1.9 GHz CMOS LNA designed for the AMI 0.5μ process. 96

Figure 4.6. Inductor lumped-element model. 97

Figure 4.7. a) Photograph of the fabricated inductor (the CPW ground ring around the inductor is not shown) b) Cross-section of the substrate. 99

Figure 4.8. Variation of inductor area and *NF* with Q_g. 100

Figure 4.9. Chip and package layouts of the proposed integrated LNA. 101

Figure 4.10. a) Layout and cross-section of the inductor used (9 nH CPW topology) with b) measured Q values, c) simulated gain and NF numbers, and d) photograph of an initial prototype showing the embedded inductor in the package and the wirebonded IC. 102

Figure 4.11. a) LNA with impedance transformation networks (pi networks) and implementation of the output pi using embedded passives. b) Actual layout of the output pi, showing the embedded inductors and capacitor. 105

Figure 4.12. a) Two reference ground layout topologies for the output pi. b) SONNET simulations for both layouts. 106

Figure 4.13. Measured S11 values for amplifiers using the two pi topologies of Figure 4.11a, showing the effect of the reference ground layout on LNA performance. 107

Figure 4.14. a) ADS circuit model for the LNA, along with the mutual inductance that was necessary to model the instability. b) Modeled (ADS) S11 results showing instability 108

Figure 4.15. Sonnet simulations of the unstable LNA layout, with the use of jumpers for current re-routing. 109

Figure 4.16. Coupled-line modeling of two inductors a) Layout and segmentation of the inductors b) ADS multilayer coupled line model of the inductors c) Cross-section of one of the segment (Segment 4). 111

Figure 4.17. Modeled (ADS) S11 results showing instability. 112

Figure 4.18. a) Photograph of the fabricated device. b) Modeled and measurement data. 113

Figure 5.1. Mixed-signal test-vehicle showing an RF circuit (LNA) in close proximity to digital circuits (FPGAs) 117

Figure 5.2. Board stack-up. 119

Figure 5.3. a) Test vehicle A. b) Test vehicle B. c) Test vehicle C. 120

Figure 5.4. Cross-section of the 6-metal layer board substrate, showing the routing of the signal line beneath the LNA (for boards A and B). 121

Figure 5.5. Measurement setup. 122

Figure 5.6. LNA output spectrum of Test vehicle A 122

Figure 5.7. LNA output spectrum a) Test vehicle B. b) Test vehicle C. 123

Figure 5.8. Routing of the digital trace (metal layer 4) with respect to the LNA layout (metal layers 1 & 2; not shown) and the corresponding slot (metal layer 3). a) Test vehicle A. b) Test vehicle B. 124

Figure 5.9. Via transition in the signal path, showing the discontinuity in the return current path. 125

Figure 5.10. LNA output spectrum a) Test vehicle A. b) Test vehicle B. c) Test vehicle C. 126

Figure 5.11. S11 measurements at the input of the 50Ω microstrip signal line (on Testbed A), with and without capacitors. 127

Figure 5.12. Measurement setup. 129

Figure 5.13. Measured frequency spectrum at the output of the LNA, with the input shorted to ground and a) system powered on, but with

FPGA quite (not switching) b) system powered on and the FPGA driving the bus with a 300MHz clock. 131

Figure 5.14. Simulated isolation of the Murata ferrite bead. 133

Figure 5.15. a) AI-EBG implementation b) Unit cell of the EBG structure. 135

Figure 5.16. a) Photograph of an AI-EBG implementation. b) FR-4 stackup used. c) Model-to-hardware correlation for isolation (S21) in the structure. 136

Figure 5.17. Simulated transmission coefficient of the EBG. 137

Figure 5.18. a) Frequency domain simulation of the mixed-signal system. Figure shows the definition of the two ports. b) Simulated LNA output spectrum. The red lines (and marker m2 at 2.1GHz) show the noise coupled through an ordinary plane pair, while the blue lines (and marker m1 at 2.1GHz) represent noise coupled through the AI-EBG-based power system. 139

Figure 5.19. a) Photograph of the test-vehicle b) 3-metal layer FR-4 stack-up used to implement the system. 140

Figure 5.20. a) Comparison of LNA output spectrum, with and without the AI-EBG–based power distribution scheme. b) Comparison of 7th harmonic noise peak at 2.1 GHz for the mixed-signal systems with and without the AI-EBG AI-EBG–based power distribution scheme. 141

Figure 5.21. Simulated performance comparison of different combinations of EBG-based structures and ferrite beads. 143

SUMMARY

The integration of mixed-signal systems has long been a problem in the semiconductor industry. CMOS System-on-Chip (SOC), the traditional means for integration, fails mixed-signal systems on two fronts; the lack of on-chip passives with high quality (Q) factors inhibits the design of completely integrated wireless circuits, and the noise coupling from digital to analog circuitry through the conductive silicon substrate degrades the performance of the analog circuits.

Advancements in semiconductor packaging have resulted in a second option for integration, the System-On-Package (SOP) approach. Unlike SOC where the package exists just for the thermal and mechanical protection of the ICs, SOP provides for an increase in the functionality of the IC package by supporting multiple chips and embedded passives. However, integration at the package level also comes with its set of hurdles, with significant research required in areas like design of circuits using embedded passives and isolation of noise between analog and digital sub-systems.

The key contributions of this work are envisioned to be the development of novel RF circuit topologies utilizing embedded passives, and an advancement in the understanding and suppression of signal coupling mechanisms in mixed-signal SOP-based systems. The former will result in compact and highly integrated solutions for RF front-ends, while the latter is expected to have a significant impact in the integration of these communication devices with high performance computing.

CHAPTER 1

INTRODUCTION

In recent years, the marriage of high-speed computing and wireless communication has emerged as a formidable driving force in the global electronics industry. This has resulted in products with both computing and communication capabilities, and has engineered a tremendous surge of interest in the mixed-signal market [1]. Figure 1.1 shows the global mixed-signal market and its composition [2].

For example, Intel, Corp. has announced a "Radio Free Intel©" initiative, adding communication capability to high-performance computing by the merger of CMOS wireless radios and microprocessor chip-sets [3]. Intel envisages a future where a user with a mobile computer can seamlessly move between different wireless networks (long-distance as well as short-distance), achieving "ubiquitous wireless connectivity" for a computing device. At the same time, Nokia Corp., the world's largest manufacturer of cell-phones, has announced the "N-Gage" gaming device platform where customers all over the world can compete with each other wirelessly [4]. With the processing power in these gaming consoles expected to be equal to or more than a consumer laptop, this would represent an unprecedented increase in the computing power of a commercial wireless communication device.

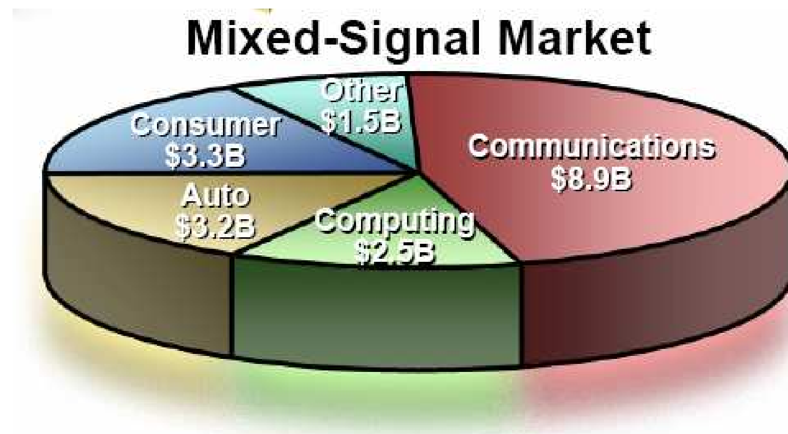


Figure 1.1. Global mixed-signal market, and its composition.

Although the term "mixed-signal" is a generic one and deals with the integration of multiple signal domains, in the particular context of today's commercial applications, it has come to represent the blurring of the hitherto concrete lines separating digital and analog/RF domains.

As shown in the examples mentioned above, the next-generation mixed-signal systems will be expected to provide high-performance computing and wireless connectivity to a mobile user. But with a proliferation of communication standards geared towards different applications, these computing-communicating-hybrids will need to support multiple communication protocols at multiple frequency bands [5] to achieve this goal of ubiquitous connectivity. As an e.g. (a rather futuristic one), a mobile user engaging in a video-conference via his cell phone can expect his call to be routed over a Wideband CDMA (WCDMA) network as he walks across the parking lot, with a

seamless hand-off to a Wireless LAN (WLAN) based network as he enters his office. At the same time, a GPS signal from his cell phone continuously communicates his position to a satellite, while the Bluetooth protocol is used to synchronize the contents of his phone-based calendar with the one in his office computer.

Ever since the invention of the Integrated Circuit (IC), miniaturization and integration have been key drivers in the growth of the semiconductor industry. Consumer-driven devices like the computing-communicating-hybrids (described in the previous section) also need miniaturization (through integration), to achieve goals of low-cost and high performance. In fact, with wireless mobility as a key distinguishing feature, these mixed-signal systems impose additional constraints of size, thickness and weight on the integration technologies.

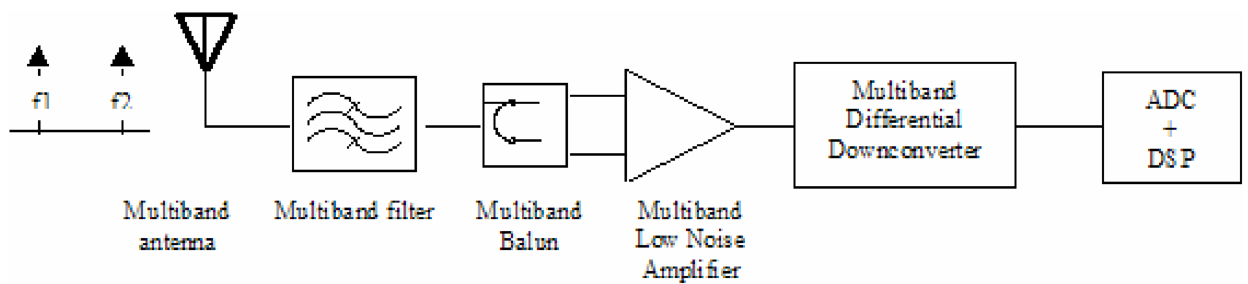
An integrated multi-frequency mixed-signal system can lead to a number of design complexities, primary of which are the suppression of signal coupling between the different signal domains and the design of the multiband radio architecture. Suppression of digital switching noise is very much dependant on the level of integration in the system, and is thus tightly coupled to the technology used for integration. It will therefore be dealt with later in this chapter, after looking at the different integration technologies available for mixed-signal systems.

1.1. Multiband Radio Architectures

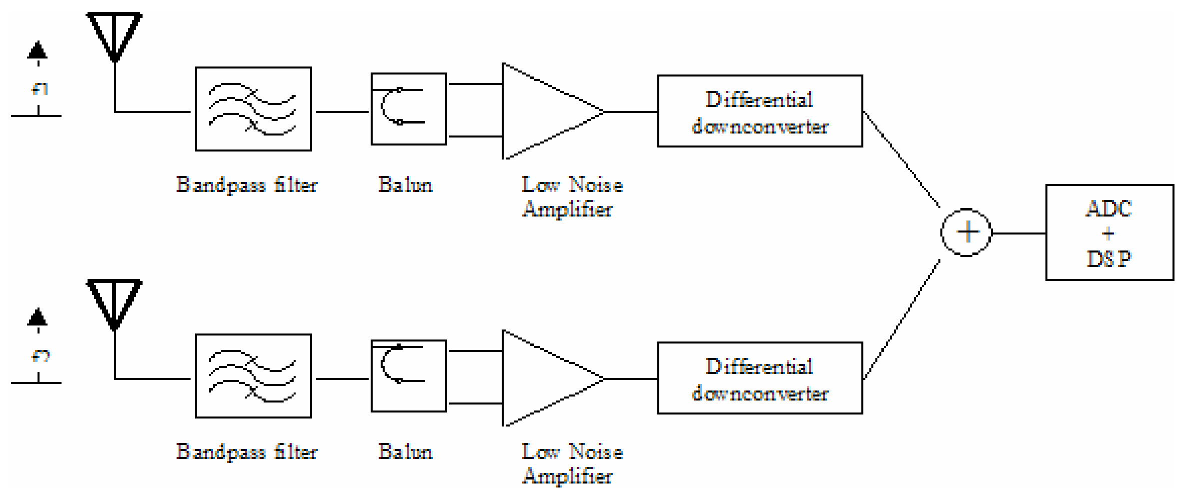
Figure 1.2 shows two possible multiband receiver implementation schemes, based on functionality. Figure 1.2a shows multiple parallel paths (each of which is single-band in nature) stacked together. Each path is a complete receiver chain, with a single-band antenna, single-band filter, single-band balun, single-band Low Noise Amplifier (LNA) and a single-band differential down-converter (with a single-frequency Voltage Controlled Oscillator (VCO)). A common back-end baseband unit contains the Analog-to-Digital Converter (ADC) (Digital-to-Analog Converter (DAC) in case of a transmit chain) and the Digital Signal Processor (DSP). The multiple receiver paths provides the baseband circuit with signals at multiple frequencies simultaneously, but the choice of the signal to be processed (and by extension, the receiver path to be used) is made at the baseband level. This is a viable architecture in a scenario where the multiband radio is expected to receive signals at multiple frequencies, *but process only one at any single instance of time*. A good example is a multiband "world-phone" which is operational at the 850MHz, 900MHz, 1800MHz and 1900MHZ to service the GSM-USA, EGSM, DCS and PCS protocols. Although the RF front-end is capable of processing signals in any of these frequency bands, the baseband chooses only one at any instance of time based on availability of service and/or signal strength.

Figure 1.2b shows an alternate architecture, where each device in the receiver path is functional at multiple frequency bands. The receiver consists of a multiband antenna, a multiband filter, a multiband LNA, a multiband differential down-converter (with a

multiband VCO) and a baseband unit, and can thus *process multiple signals at different frequencies simultaneously*. As an example, a receiver functional at 1900MHz and 2.4GHz concurrently can enable the user to make a phone call using the PCS protocol even as he receives data from the WLAN router simultaneously.



a)



b)

Figure 1.2. a) Multiband architecture, with each device operational at a single band, and switching between frequency bands in the baseband. **b)** Concurrent multiband architecture, with each component functional at multiple frequency bands.

The "multiple single-band" architecture of Figure 2a suffers from high power consumption and large size, due to the multiplicity of receiver paths. The concurrent architecture of Figure 2b, meanwhile, can result in saturation of the active circuitry in the presence of a high power signal in *any* of the bands it is designed for. This can degrade the sensitivity of the receiver for signals in the other operating frequency bands, limiting its concurrent functionality.

In practice, a combination of the two architectures, with multiple receiver paths each involving singleband/multiband devices, will offer the optimum performance and size. Figure 1.3 shows one such implementation, where switches have been used in the receiver chain to ensure that high-power out-of-band signals do not saturate the active circuitry. The frequencies/protocols have been divided based on concurrent and non-concurrent functionality requirements, and have been allocated distinct receiver paths. For each receiver path (after the switch), the components have been designed for multiband functionality, resulting in optimized sizes and power consumption.

As an example, consider a quad-band (850MHz, 900MHz, 1800MHz and 1900MHz) cell-phone with dual-band (2.4GHz and 5GHz) WLAN capability. As only one of the four bands available for voice communications need to be used at any instance, they can all be grouped into one multiband receiver path operational at all four frequencies. Similarly, the two WLAN bands can also be grouped into one multiband path. However, since a user needs to make a phone call *and* receive signals from the WLAN router *simultaneously*, the two paths can be classified as concurrent, and can be designed such that the baseband processor receives *one* signal from each path *concurrently*.

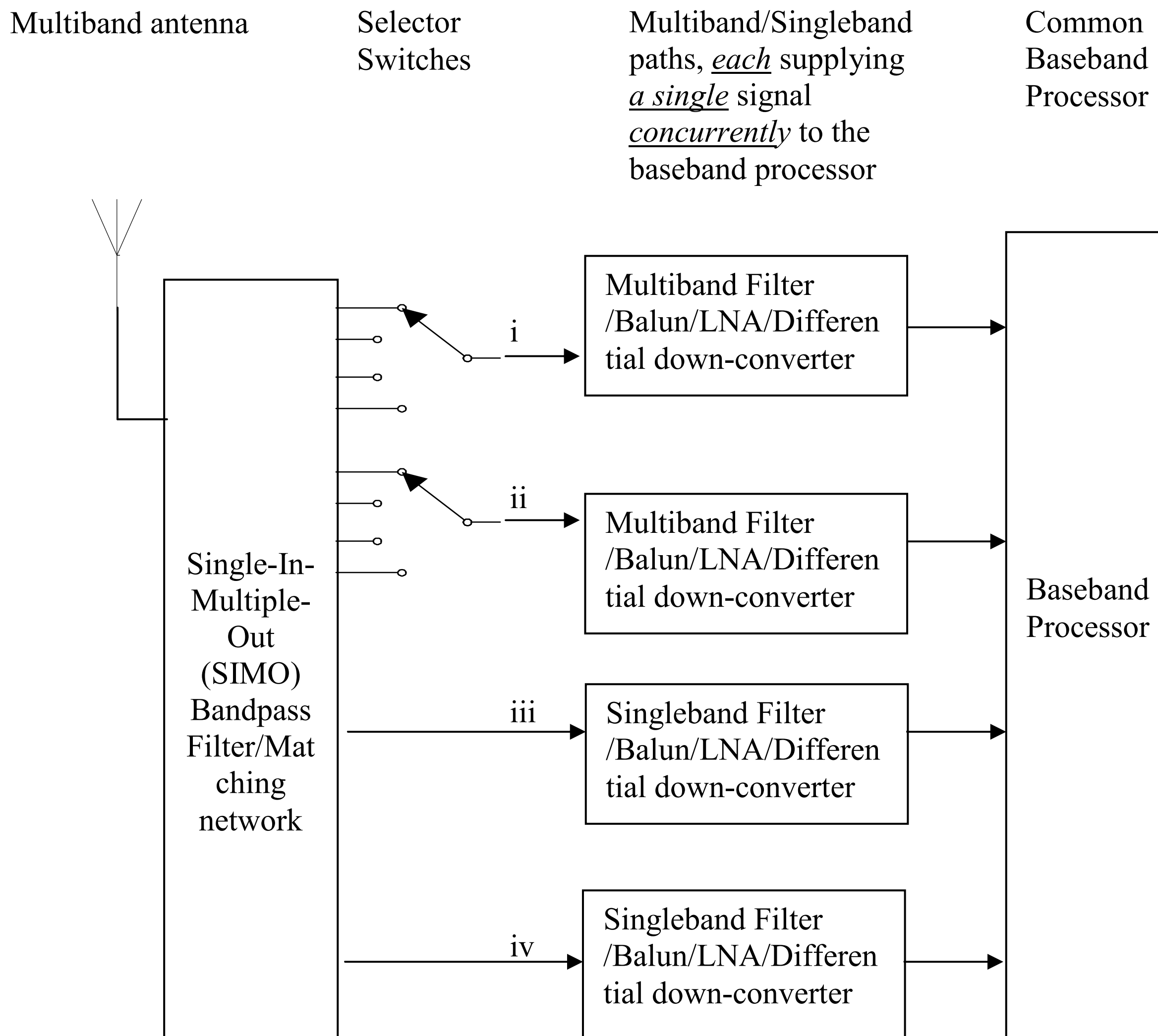


Figure 1.3. Switched semi-concurrent multiband receiver architecture, showing four paths with each path supplying one signal concurrently to the baseband processor. Paths (i) and (ii) are multiband in functionality, with the selector switch between the SIMO filter and the rest of the front-end circuitry determining the choice of signal to pass-through. Paths (iii) and (iv) are singleband in functionality.

The design methodology for the switched architecture can thus be summarized as follows:

1) Functional division of the frequency spectrum under consideration, based on concurrent or non-concurrent operation.

2) Design of each path using multiband components for concurrent operation.

The first step in the implementation of mixed-signal systems with multiband radios is the design of multiband front-end components (comprising of antennas, band-pass filters, baluns, LNAs, VCOs and mixers). As in the case of the suppression of noise coupling between the digital and analog signal domains, this is highly dependant on the level of integration required in the system. A solution for implementing multiband components in a mixed-signal environment would therefore be incomplete (and inappropriate) without looking at the various integration technologies available for such a solution.

1.2. Mixed-Signal Integration

Traditionally, mixed-signal systems have been implemented at the Printed Wiring Board (PWB) level, by simply soldering multiple ICs and discrete passives onto a low-cost epoxy-based board. With improvements in semiconductor technology, the number of transistor per die has increased, leading to a scenario where entire systems can be implemented in a single chip. This approach, also called the System-On-Chip (SOC)

implementation, has been particularly successful in the case of CMOS digital circuit design, where single-chip solutions with millions of transistors have become very common (E.g. [6]).

However, the single-chip integration methodology of SOC has been singularly unsuccessful in the integration of the mixed-signal computing-communicating-hybrids described in the previous section. Although several system-level examples (E. g. [3], [7]) have been reported on high-performance mixed-signal (analog/RF and digital) functionality, none of them are single-chip solutions. The SOC-based examples that *do* exist tend to be low-performance applications. For example, Broadcom has announced a single-chip transceiver solution for wireless audio processing, the BCM 2037 IC. However the Bluetooth protocol that it uses for communication reduces the range of operation, and the meager 120kB of memory that it contains is insufficient for any meaningful computing functionality. It is important to note that Broadcom's own BCM2004 IC, a single-chip Bluetooth solution designed for use in a Qualcomm cellphone, still requires an external filter to function in the multiband environment. SOC thus fails in the integration of high-performance computing and long-range communication protocols like WiMax and WCDMA.

By its very nature of bringing together computing and communication, mixed-signal systems require a wide range of technological capabilities. For example, the power amplifier (PA) of a radio transmitter needs the high rail-to-rail power supplies of Gallium Arsenide (GaAs) technology while the baseband circuits require the reduction in size and power consumption afforded by CMOS technology. Unlike digital integration where any possible function can be implemented using standard transistors in a standard CMOS

technology, mixed-signal integration thus calls for multiple technological capabilities. And studying the previous published examples ([3], [7]), it becomes clear that one of the main impediments to CMOS SOC based mixed-signal integration schemes is the inability to pick and choose the correct technology required for a particular application [8].

Another problem in SOC based integration is the lack of high Quality (Q) on-chip passives. The thin metal layers and the lossy nature of the silicon substrate lead to higher parasitics for on-chip inductors and capacitors (E.g. [9]). This is primarily a concern in RF/analog circuit design, where the low-Q passives make design of completely integrated filters and LNAs for high sensitivity applications like long-distance communication protocols next to impossible ([10]-[13]).

A third impediment to mixed-signal on-chip integration is noise coupling from digital circuitry to components of the wireless receiver chain ([14]-[17]). As the incoming RF signals are in the order of microvolts, any in-band noise reaching the receiver corrupts the signal. The switching of digital circuits couples with package parasitics to produce power supply noise, as well as directly coupling to the analog circuitry through the conductive silicon substrate. The LNA is the first active device in any receiver chain, and is particularly susceptible to this noise.

Developments in packaging technology have led to a second option for integration, the System-on-Package (SOP) approach. Unlike SOC where the package exists just for the thermal and mechanical protection of the ICs, SOP provides for an increase in the functionality of the IC package by supporting multiple chips and embedded passives [18].

Depending on the packaging technology used, there are two main approaches for SOP integration; namely 1) Low-Temperature Co-fired Ceramic (LTCC) technology [19] and 2) Organic technology ([20]-[22]). The dielectric materials and highly conductive copper layers of these packaging substrates makes high-Q embedded inductors and capacitors possible ([19]-[22]). These passives can be used to design RF front-end components like antennas, filters and baluns embedded in the packaging substrate, which combined with the on-chip circuitry, leads to completely integrated modules. The use of multiple chips for the RF transceiver and the digital baseband processor also reduces the noise that would have otherwise coupled through a common silicon substrate, along with opening up the possibility of using multiple technology ICs for implementing multiple functions.

Figure 1.4 summarizes the various integration options available to the mixed-signal system designer today.

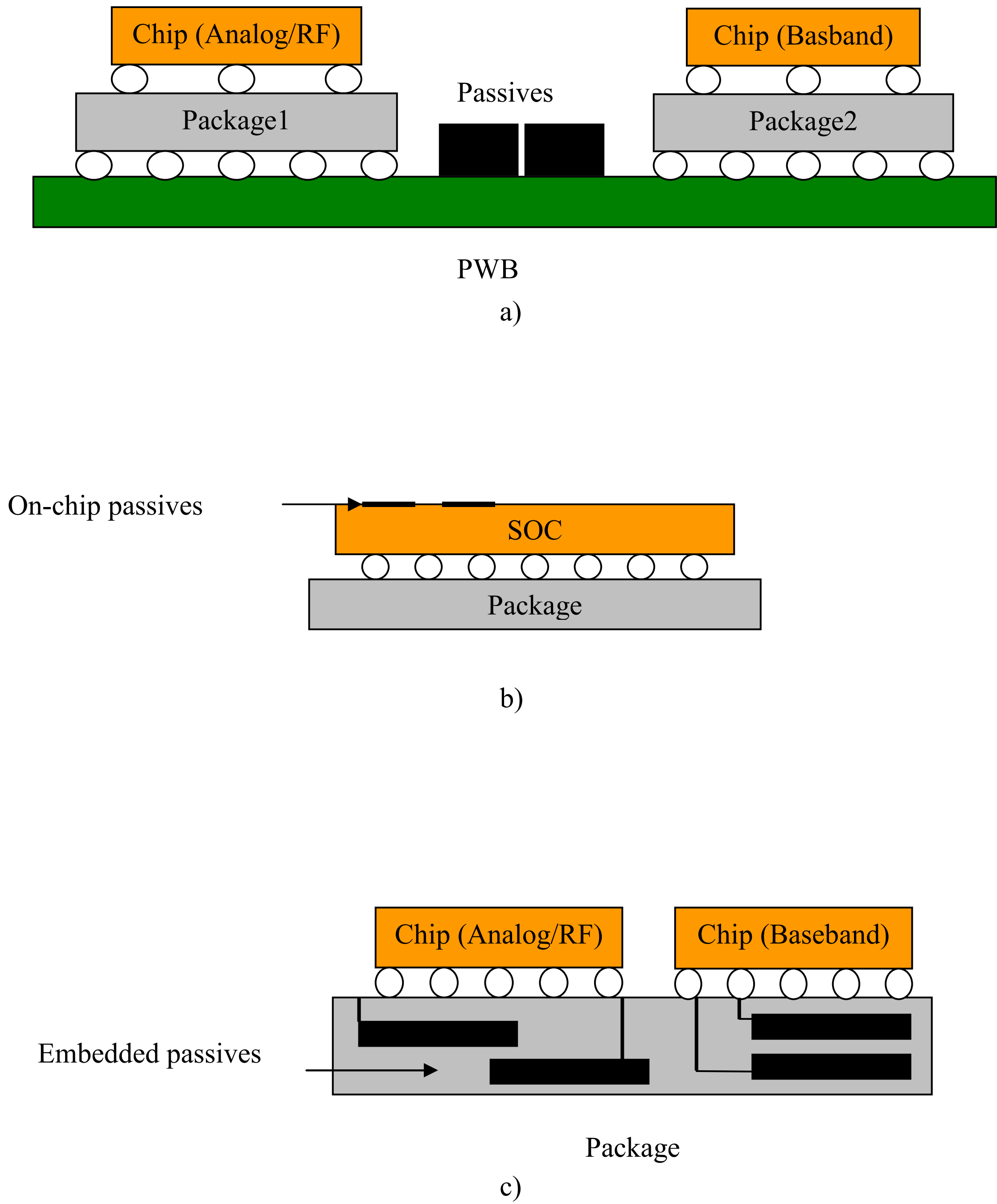


Figure 1.4. a) Printed Wiring Board (PWB) based integration, with packaged chips and passives assembled onto a PWB substrate **b)** SOC-based integration, with on-chip passives **c)** SOP-based integration, with embedded passives in the package.

Conceptually, SOP offers the best solution possible for a mixed-signal environment. As such, it makes sense to go more into the details of the two main SOP-based technologies, so as to determine the optimum solution for mixed-signal integration.

1.2.1. Low-Temperature Co-fired Ceramic (LTCC) Technology

LTCC technology (also known as Multi-Chip Module – Ceramic (MCM-C)) is a multi-layer ceramic process, where the ceramic layers are tape-cast in their pre-fired "green state" and the tape is then cut to the required size [23]. Registration holes, via holes and cavities are then punched or drilled into the different tape layers. Via holes are normally filled (often with silver), and then thick-film processing is used to print metallization patterns on the tapes. The layers are then registered and laminated to each other, and then co-fired at about 850°C.

The main electrical properties of LTCC can be summarized as follows [23]:

- Low loss tangent ($0.003<\tan\delta<0.009$ from 1-10GHz)
- Dielectric constants ranging from 5-20, enabling the integration of a wide-range of functionalities
- High dielectric layer count (as high as 50)

These characteristics have propelled the development of LTCC into the "technology of choice for RF integration" [23]. Inductors ranging from 1nH to 25nH and capacitors ranging from 1pF to 30pF have been demonstrated on LTCC substrates [24]. Depending on topology, these passives exhibit a Q of 50-150 for inductors and 50-200 for the capacitors. They can then be used for the design of circuits like filters and baluns

that are completely integrated in the substrate. Several modules involving active circuits attached to these LTCC substrates (via flip-chip or wire-bond or simply soldering pre-packaged components) are available in the commercial market today. Although PA modules remain the single-largest application for LTCC substrates, Antenna Switch Modules (ASM) used to isolate RF signals so that they may share one antenna patch, VCOs to provide stable reference frequencies for down-conversion and Surface Acoustic Wave (SAW) filter based high-Q filtering modules have also proved to be major LTCC applications. In addition, completely integrated RF transceivers in module forms have also been implemented using LTCC (Figure 1.5).

Figure 1.5. LTCC based integrated Bluetooth transceiver module from Kyocera.

Although significant advancements have been made in the use of LTCC for microwave applications, the question still arises as to whether they are truly the technology of choice to meet the integration needs of next-generation computing-communication-hybrids. And the answer is a resounding no, due to the following reasons:

1. Although LTCC has been commercially proven for *today's* RF modules and components, fundamental processing issues place limits on the amount of future integration possible. This can be described as follows:

    - The screen-printing process in LTCC limits via size to 0.1mm and 1:1 aspect ratio. Combined with limitations on minimum line-widths possible (due to the screen-printing process), this results in low component-density substrates. Although per-volume component count can be increased today by stacking multiple dielectric layers, future trends in wireless packaging points to low-profile devices, making such a multi-layer LTCC platform non-competitive with regards to thickness.
    - LTCC process starts with "green-sheet", resulting in 10-25% shrinkage during fabrication. This affects the yield of the devices.
    - The screen-printed conductor profile results in rough interfaces. At microwave frequencies, this results in higher metal losses due to Skin Effect.

2. Processing limitations results in poor yields for large metal planes in LTCC substrates, which are very important for use as power distribution planes in digital systems. This results in poor signal and power integrity in the system, ultimately resulting in failure of high-speed digital systems.

3. Finally, LTCC is a high-temperature (800°C) process. Combined with the fact that current commercial manufacturers are set-up for processing "green" sheets in lot-sizes of 8"x8", it makes LTCC a high-cost process.

1.2.2. Organic Technology

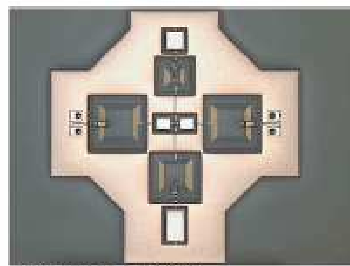
Integrated organic technology can be further classified as Multi Chip Module-Deposition (MCM-D) and SOP-Laminate (SOP-L), depending on whether the organic films are deposited or laminated onto the mechanical substrate to form functional layers.

MCM-D consists of deposition of thin (<15μm) polymer dielectric films deposited onto a stable base substrate such as silicon/glass or alumina. Thin (2-5μm) conductor film, usually copper, is then deposited and processed photolithographically. Benzo Cyclo Butene (BCB) (ε_r=2.65 and tanδ=0.0008) is a polymer that has been widely used for such applications (e.g. [25], Figure 1.6a). The ability to have microvias as well as very thin line-widths increases the component density of the technology. However, it is also important to note that it is difficult to fabricate multilayer substrates with large number of layers in this process. Combined with the fact that it is a high-temperature process (450°C) and can only be processed on wafers with 4-6" diameter makes MCM-D a comparatively high-cost technology for high-volume manufacturing.

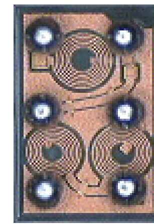
A variation of MCM-D is the Thin-Film-On-Glass (TFOG) or Thin-Film-On-Silicon (TFOS) process (Figure 1.6b). Copper metal (10μm thick) is deposited onto an insulated surface if silicon (with 25μm silica (SiO_2) layer on top). Low-loss low dielectric constant materials like BCB are spun onto this layer to add two more metal layers. Microvias are available between all three metal layers. Further, the technology also offers precision Nickel-Chromium (NiCr) resistors and Silicon Nitride (SiN) capacitors. Like MCM-D, these processes provide high component density with the possibility of integration with CMOS active circuitry. But again, like MCM-D, they also have the

drawbacks of high-temperature processing and fabrication in lots of 6” wafers. The technology also limits the number of metal layers possible (currently three).

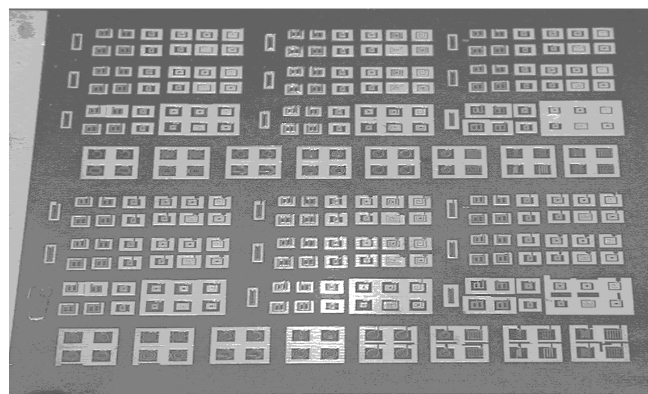
SOP-L is based on technology developed for the fabrication of PWBs. A thick copper-cladded (9-35μm) FR-4 organic substrate (epoxy-glass fiber composite) is used as the mechanical core [26]. Further layers are formed by laminating copper-clad dielectric layers onto the core, with the multiple copper layers insulated from each other using thin-film epoxy-glass composites (25-100μm thick). Patterns are formed on the copper layers using photolithographic techniques, resulting in minimum line-width and minimum line-spacing as low as 25μm (Figure 1.6c).



a)



b)



c)

Figure 1.6. Embedded passives on **a)** MCM-D substrate. **b)** TFOS substrate. c**)** SOP-L (Vialux™) substrate.

Some of the processing and electrical advantages of this technology are as follows:

1) Heterogeneous stack-ups with different electrical properties (ε_r and tanδ) and thickness (4μm-1mm) for each layer allows for fulfilling the disparate needs of different signal domains. For example, it is possible to realize a multilayer stack-up with a high-loss high dielectric constant (K) layer for power-supply decoupling, low-loss low-K layer for high-speed digital signal routing and a low-loss high-K layer for the design of RF passives.
2) Availability of microvias as small as 1mil in diameter combined with minimum line-width/line-spacing of 1mil and thin dielectric layers (as low as 4μm) allows for component densities higher than that of LTCC and comparable to that of MCM-D.
3) High conductivity copper metallization (12-36μm) helps reduce losses in transmission lines and passive devices compared to the losses in deposition and ceramic processes.
4) It is a low-temperature process (<250°C) that can be processed in lot-sizes as large as 18"x24" making SOP-L a low-cost technology for high-volume production.

A wide variety of organic laminates (with a wide range of electrical properties) are available today, for use in heterogeneous SOP-L stack-ups for mixed-signal integration. Low-cost epoxy based laminates used in traditional PWB industries form the bottom of the heap. They have high tanδ (0.015-0.025) and high coefficient of moisture absorption, which results in a variation of their electrical properties with temperature. As a result, embedded passives designed on these substrates have low Q-factors and also

change their electrical properties with temperature. Their usage is thus limited to routing of low-speed digital signals.

Thin high-K laminates such as Oak-Mitsui's FaradFlex™ (ε_r ranging from 4.4 to 30 and thickness ranging from 24μm to 8μm) and 3M's C-Ply™ (ε_r of 16 and thickness ranging from 8μm to 16μm) comes next. The high capacitance density that a combination of high ε_r and low thickness provides (as high as 11nF/inch^2) allows the use of these laminates for embedded power supply decoupling applications. A comparatively high tanδ and coefficient of moisture absorption limits their application in the design of high-precision low-loss embedded passive circuits; however, by packaging the layers in such a way that they are not exposed to the outside air, they can still be useful for the realization of specific miniature RF circuits where dielectric loss is really not a concern (e.g. low-pass or high-pass filter structures for baluns).

At the top of the pyramid comes the new breed of high performance laminate solutions like Asahi-PPE™, Rogers 4350, Liquid Crystalline Polymers (LCP) and Teflon. Boasting low tanδ and low moisture absorption coefficient, these materials can be used in the realization of precision RF circuitry with virtually no change in frequency characteristics with temperature variation. Although Teflon is comparatively higher cost and harder to fabricate, the others are usable within a standard PWB-based processing flow, reducing their cost structure. With high line densities and the availability of small microvias, their component densities are comparable to that of LTCC and MCM-D.

It can be seen that a combination of the above materials, in a heterogeneous multi-layer stack-up, can meet all the packaging needs of mixed-signal computing-

communication-systems. It is thus clear that laminate-based SOP could be the technology of choice for mixed signal integration.

Table 1.1 summarizes the characteristics of the various integration technologies covered so far.

Table 1.1. Comparison of discrete, SOC, LTCC, MCM-D/TFOS and SOP-L integration technologies.

Technology	Advantages	Concerns
Discretes on PWB	• Low-to-mid Q passives • Readily available	• Low density, large size • Component variation
SOC	• Compact • High integration in digital circuits	• Low-Q passives • No single technology platform covers all mixed-signal system requirements
LTCC	• High-Q passives • High integration • High density	• CTE mismatch • Shrinkage • Future scalability • Lack of metal planes
MCM-D/TFOS	• High density	• Low-Q passives • Low integration
SOP-L	• High Q passives • High integration • High density • Availability of large metal planes • Large area manufacturing	• Hermiticity

(**Note**: In addition to the above-mentioned technologies, Micro-Electro-Mechanical-System (MEMS) (where passive physical structures including inductors and capacitors are realized on SOC-based silicon wafers using conventional and non-conventional semiconductor processing steps) has also emerged as a technology candidate to implement mixed-signal systems. In fact, a few devices incorporating a CMOS digital IC with a MEMS-based gyroscope has appeared on the commercial market for automotive and cellular application [27]. However, these are niche devices at best, with several problems such as packaging the moveable physical components and integrating the non-conventional processing steps with conventional CMOS SOC manufacturing procedures preventing across-the-board adoption of a MEMS-based platform for mixed-signal integration. As such, it is perceived that MEMS (along with other exotic technologies like piezoelectric Surface Acoustic Wave (SAW) and Bulk Acoustic Wave (BAW) resonators) will become *a part* of an SOP-based system integration scheme. In such a scenario, each component will provide its own niche functionality, acting in a complementary fashion rather than competing with the laminate-based SOP base process).

1.3. Organic SOP-Based Mixed-Signal System Integration

Given the choice of technology for mixed-signal integration, it is important to revisit the two main concerns that were raised and set-aside earlier – design of multiband

components for multiband radio architectures, and the analysis of noise coupling between the digital and analog/RF sub-sections. In addition, the parasitic inductance and capacitance of chip-package interconnects become significant and can result in signal degradation at high frequencies. This becomes significant for circuits like LNAs, VCOs and Power Amplifiers (PA), which reside at the interface between the package and chip domains. The back-and-forth transfer of signals between the package and chip domains necessitate a design partitioning methodology to decide the distribution of circuit components within the package or within the chip. The use of multiple embedded passives in the substrate can also generate undesirable resonance and feedback, jeopardizing the functionality of the system [28].

Integration at the package level leads to changes in priority at the design phase. With the availability of high-Q passives embedded in the package, the *number* of lumped components becomes less important than the *value* of each of these components. (In contrast, designs utilizing discrete passives are more concerned with the total number of passives and not the individual values of each; the cost of assembly depends only on the number of discrete elements to be soldered on board, and the packaged size for different values of capacitance or inductance usually remains the same for commercially available discrete devices). This requires novel designs for RF components using these embedded passives, with priorities shifting from reducing the component count to keeping the value of the passives low.

Noise coupling between digital and analog circuits remains a problematic issue even in SOP-based implementations. Although coupling through the silicon substrate of an SOC chip is now eliminated, new noise sources like Electromagnetic Interference

(EMI) from high-speed signal lines, fluctuations in power plane etc. arise, which have to be dealt with through careful modeling and analysis.

1.3.1. Design of Multiband RF Components

Multiband functionality in components can be achieved in the following ways:

1) Devices with wide bandwidths capable of operating at different frequency bands.

2) Multiple single-band devices with matching networks at input and output producing a Single-Input-Single-Output (SISO) component. Each single-band device has narrow operating bandwidth, and multiband operation is achieved for the component by switching between the different single-band circuits (i.e. the component outputs only a single frequency at any given time) [29]

3) Concurrent devices that achieve simultaneous multiband functionality (sampling one or more frequencies at a time depending on application) [30].

Option 1 is difficult to implement due to technological concerns and the presence of large blocker signals close to the frequency bands of interest. Option 2 is a component-scale replica of the multiband architecture discussed in Figure 2a, and as such exhibits problems such as large size and high power consumption. In contrast, Option 3 (the use of true multiband devices) leads to lower power consumption and a vastly reduced footprint.

Research is replete with examples of multiband antennas ([30]-[33]). Multiband band-pass filters using varactor diodes have also been reported [34]. As these diodes exhibit Q-factors of the order of 30 and results in an increase in the noise figure (NF) of the device, solutions like stacking separate single-band passive filters on a single package has also been attempted [35]. Further, a multiple frequency generator using high-Q embedded passives on an organic substrate, where two clock signals are generated concurrently, has been proposed recently [36]. Finally, multiband LNAs (through the use of resonant passive networks [5] or by stacking multiple single-band devices [37]) have also been reported.

All of the above examples have either been demonstrated directly using SOP based packaging technologies, or can easily be ported to one. From a design perspective, the only new RF device required to implement a completely integrated multiband receiver (like the one shown in Figure 1.2b or Figure 1.3) is a balun that is functional at multiple frequency bands.

1.3.2. Design Partitioning

The passive devices like antennas, filters and baluns are completely embedded in the package. For the circuit components lying at the interface of the chip and package domains (the LNA, the VCO and the PA), design partitioning and optimization is required, to take into account the parasitics involved in a chip-package signal transition. Examples of PAs with the output matching networks implemented using embedded

passives and VCOs with high-Q embedded inductors for improvement in phase noise has been reported in the literature ([38]-[40]).

It would be a relatively simple process to achieve complete integration by embedding passives in the package. However, this approach neglects the fact that compared to on-chip inductors with low Q values and discrete passives with fixed Q's, the use of embedded passives leads to the development of the passive Q as a new variable in circuit design. With Q values ranging from 20-200 (E.g. [21]), designers now have a choice in the value of Q they want for a particular component. Higher Q values result in new tradeoffs, particularly with respect to device size, and a design partitioning and optimization strategy is thus required to ensure efficient use of the packaging substrate. This has to be incorporated into the design methodology of each circuit, for optimal system performance. Although [39] has mentioned that there is very little reduction in VCO phase noise with improvement in inductor Q beyond a certain value for Q, the implication of this with respect to module size has not been fully investigated.

References [10]-[13] reports LNAs for long-distance communication protocols; none of these devices are completely integrated solutions, and an external discrete inductor is used in each case to make the circuit functional. The multiband LNA reported by Hashemi et al. [5] also relies on external discrete passives to implement the input resonant network. Design of completely integrated CMOS LNAs is possible by using embedded passives in the package. However, the common CMOS LNA design methodology of [10] has to be updated to take into account the tradeoff of higher inductor size for higher Q.

1.3.3. Measurement and Analysis of Signal Coupling

With the high sensitivity requirements for radio circuits necessitating the handling of microwatts of input signal power, noise coupling from digital to analog domains has become a major impediment to mixed-signal integration. Noise is generated in digital circuits when many static gates change state simultaneously, causing a spike in current flow through parasitic resistances and inductances in the circuit [16]. This results in a spike in the power supply, which can couple into the analog circuits through a common power distribution system. The noise can also appear in analog circuits through capacitive coupling to and from the highly doped silicon substrates used in SOC systems. [14-17, 41-47].

However, with the use of SOP based schemes, new noise coupling and propagation mechanisms come into play. With the use of power planes in the package for power distribution, ground bounce and simultaneous switching noise (SSN) become important factors in mixed-signal design. High speed signal lines also end up radiating energy, resulting in Electro-Magnetic Interference (EMI) acting as a major source of noise.

The main digital-analog noise coupling mechanisms in mixed-signal SOP based systems can thus be summarized as follows:

- Through a common power supply
- Through EMI from high-speed signal lines

In addition, coupling within the analog signal domain through closely spaced multiple embedded passives also results in performance degradation of the RF circuitry.

The low-loss power-distribution networks used in SOP-based systems produces sharp resonances that do not exist in a higher-loss SOC-based power system [48]. The modeling of noise propagation through power planes has been extensively covered for printed wiring boards (PWB) [49-52]. Many of these methodologies are directly applicable to SOP based integration schemes. The analysis of EMI has also been analyzed from a PWB perspective [53-54]. However, the effect of this noise on a practical RF circuit, using multiple embedded passives and a package-based power supply scheme, has not been fully analyzed yet.

1.3.4. Research Objectives

The main research objectives of SOP based mixed-signal system integration can be summarized as follows:

1) *Design* of novel integrated RF front-end components using embedded passives
2) *Optimization* and *Design Partitioning*
3) *Modeling and Analysis* of analog-analog and analog-digital signal coupling.

Figure 1.7 shows a test-vehicle highlighting these issues, comprising of a multiband wireless receiver supporting multiple communication protocols, and a high-speed baseband (digital) processor.

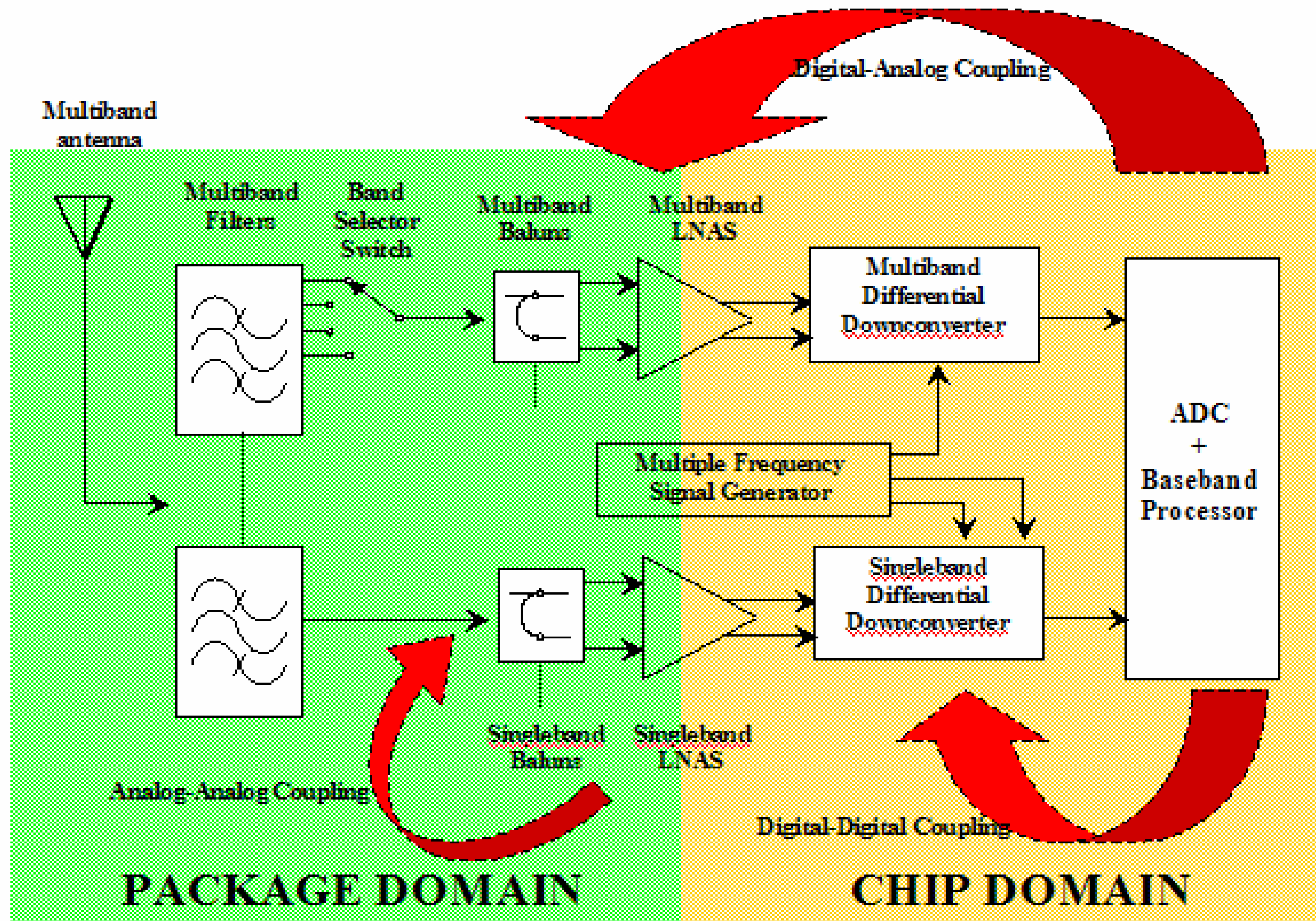


Figure 1.7. Mixed-signal SOP-based test vehicle, with integration of semi-concurrent multiband RF front-end and high-speed digital computing.

Figure 1.8 shows a possible SOP-based integration scheme, showing a heterogeneous SOP-L substrate with ICs and some passive components mounted on the surface. The assembled substrate is then overmolded, making the SOP integration invisible to the end-user.

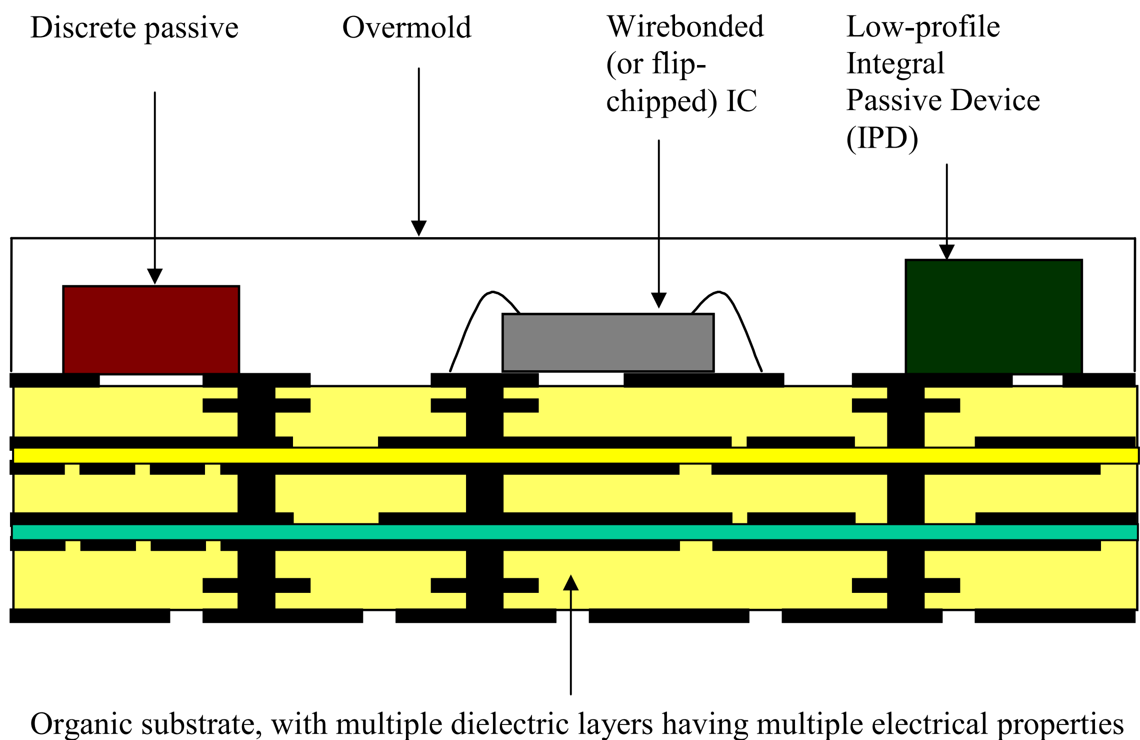


Figure 1.8. SOP implementation, with heterogenous MCM-L substrate. Multiple chips, some low-profile passive components and a few discrete passives are attached to the top, and the whole structure is overmolded.

In such an implementation scheme, the passive functionality is divided between embedded circuits in the substrate and low-profile soldered-on components on the top surface. Capacitance or inductance values that are very much higher than the SOP component densities are automatically implemented as surface mount devices (SMD) soldered on top of the substrate surface. For example, RF bypass and/or power-supply decoupling capacitors have values in the range of 0.1-10μF, and are implemented by soldering on 0402 or 0201 chip capacitors to the substrate surface. For implementing passive circuits with values of inductance and capacitance lower than or approaching the SOP component density, there exist two options:

1) Substrate:
   - Passive functionality embedded in the packaging substrate.
   - ICs and SMDs attached on the top surface.
   - Internal routing and redistribution layers.
   - *Custom designs*, with pin-outs, foot-prints and land-patterns varying with each chip-set and application.
2) Integral Passive Device (IPD):
   - Passive circuits fabricated on a low-profile stack-up. They are then singulated and attached on top of the module substrate like any other SMD.
   - Complete or partial shielding based on application.
   - *Standard designs*, with standard pin-outs and land-patterns that can be used in multiple applications with multiple chip-sets.

Although they are technologically very similar (the stack-ups for both substrate and IPD could be the same, for example), the difference in post-fabrication handling

makes the choice of implementing a particular functionality as a substrate or an IPD a very important one. Typically, the surface-mount components (IC, IPD or other SMDs) are assembled on to the substrates post-processing. They are then overmolded, pressed and singulated to obtain integrated modules, which are then tested for their functionality. Any failures in the substrates at this point results in the wastage of the entire module, leading to the requirement that the functionality embedded in the substrate needs to be highly yieldable. Although testing of the substrates could occur before assembly, the mechanization of the assembly process again means that the substrates need to have high yields (in the order of 85% and above) for the modules to become economically viable.

The IPDs, on the other hand, are completely electrically tested before assembly. This makes them the technology of choice for implementing designs with low-yields. The critical factor in the design of these IPDs is usually the maximum thickness possible. For the computing-communication-hybrids discussed in previous sections, the thickness of the complete module needs to remain in the 0.8mm-1.2mm range (depending on application). The substrate and the soldered-on components have to be co-designed to make the final module meet the thickness criterion, and with the substrates typically reaching 0.5-0.7mm in height, the maximum possible thickness of the IPDs is limited to 0.3-0.5mm.

1.4. Research Accomplishments

The objectives of this research are twofold – 1) the development of novel RF circuit topologies utilizing embedded passives in organic substrates (with the resulting design partitioning), and 2) an advancement in the understanding and suppression of signal coupling mechanisms in mixed-signal SOP-based systems. In this regard, the accomplished research can be sub-divided as follows:

1) *Choice of multiband architectures for next-generation radios*

   A survey of various architectures for multiband radios has been addressed, with an analysis of the tradeoffs involved.

2) *Design and implementation of novel concurrent multiband baluns*

   A novel concurrent balun topology has been developed. Passives have been used in conjunction with a Marchand balun to reduce the size of the device, as well as to make it functional at multiple frequencies with controllable bandwidth. A design methodology for the multiband baluns has been developed. To prove the validity of the theory, a balun operating at 900MHz and 2GHz has been designed and implemented on an LCP-based organic substrate. The measurements show good correlation with the models.

3) *Extension of multiband balun theory for the design of compact wideband baluns*

   The multiband Marchand balun theory has been extended for the design of compact wideband baluns. Proof-of-concept devices operating at 5GHz have been implemented in a multilayer LCP substrate.

4) *Design and implementation of singleband baluns in high-K organic substrates*

   Narrowband baluns measuring 1.25mm x 2mm in area have been designed for operation at 2.44 GHz. Using a novel high-K organic stack-up, the thickness of the baluns have been restricted to 0.5mm.

5) *Design and implementation of singleband filter-baluns*

   As an extension of the design of narrowband baluns, the devices have been cascaded with a band pass filter to form an integrated filter-balun, reducing the system component count. Measurements show good model-hardware correlation.

6) *Design partitioning and passive-Q based optimization of CMOS LNAs*

   The NF of a cascode CMOS LNA has been derived as a function of the Q factors of its inductors. It has been shown that beyond a certain inductor Q, the NF becomes almost independent of Q. The tradeoff of higher inductor size for higher Q, has been analyzed. Design partitioning of the CMOS LNA has been addressed, with the source and output inductors placed on-chip and with only the gate inductor embedded in the package. The inductor Q has been used as a design variable, and has been incorporated into the LNA design methodology.

7) *Study of return current routing in RF systems with multiple embedded passives*

   The effect of return current layout and coupling between multiple embedded passives on system performance has been studied using an LNA as a test-vehicle. A modeling approach to integrate system-level full-wave solvers into the design flow of integrated systems with active devices and multiple embedded passives has been proposed, and validated through measurements. A computationally efficient circuit based modeling strategy using transmission line theory has also

been used to predict the effect of coupling between embedded passives in SOP based schemes.

8) *Experimental study of digital-analog signal coupling mechanisms in mixed-signal systems*

   Direct and indirect noise coupling from high-speed digital signal lines to RF circuitry has been studied by means of test-vehicles. The noise coupling through a common-power supply has also been studied.

9) *Design and implementation of mixed-signal systems with EBG-based noise suppression scheme*

   A practical mixed-signal system involving an FPGA driving a high-speed bus (300MHz) and an LNA operating at 2.1GHz has been designed and fabricated. An EBG-based noise suppression scheme has been used for the design of the power distribution network. Measurements (and modeled results) show a suppression of the in-band noise for the LNA.

1.4.1. Original Contributions

To summarize, the following original research contributions have been reported in this dissertation:

- Development of a novel concurrent multiband balun topology, and extension of the theory of multiband baluns for the design of compact wide-band baluns.
- First demonstration of baluns on multilayer LCP substrates.
- First demonstration of low-profile baluns on high-K organic substrates.

- First study of NF of a CMOS LNA as a function of passive Q, and usage of inductor Q as a design variable.
- First demonstration of the use of Electronic Band Gap (EBG) for isolation in SOP-based integrated mixed-signal systems.

1.5. Dissertation Outline

This dissertation is organized as follows. In Chapter 2, the design of baluns operational at multiple frequencies is covered. The design methodology as well as a proof-of-concept implementation on an LCP substrate has been discussed. Further, the design of compact wideband baluns is developed as an extension of the multiband balun theory. Finally, the design and implementation of low-profile single-band devices on high-K organic substrates is presented. Chapter 3 covers the extension of the narrowband balun design by cascading it with a bandpass filter, forming an integrated filter-balun. Chapter 4 covers design partitioning and optimization of LNAs using embedded passives in the package. The NF of a cascode CMOS LNA is derived as a function of the Q factors of its inductors. It is shown that beyond a certain inductor Q, the NF becomes almost independent of Q. The effect of return current routing and passive-to-passive coupling in a substrate with multiple embedded passives is also studied. Chapter 5 describes the effect of digital noise on the RF circuitry. A practical mixed-signal test-vehicle comprising of an FPGA driving a 300MHz digital signal bus and an LNA operating at

1.8GHz-2.1GHz is implemented on an SOP-based substrate. Noise coupling from high-speed digital signal lines (through EMI) and power supply switching noise (through a common power distribution network) is experimentally studied using the test-vehicles. An EBG-based power delivery system is then used to suppress the power supply noise coupling, with final measurements correlating with models to show a reduction in the propagated noise. Finally, Chapter 6 concludes the dissertation and recommends future work.

CHAPTER 2

DESIGN OF BALUNS FOR MULTIBAND RADIOS

Baluns are three-port devices that provide balanced outputs from unbalanced inputs [55]-[57] (Figure 2.1). Electrically, this means that the input signal power is split into two channels that are equal in magnitude but opposite in phase (by 180°). They are thus required in almost all RF front-end architectures, and their design for multiband radio architectures becomes a key challenge in SOP based integration.

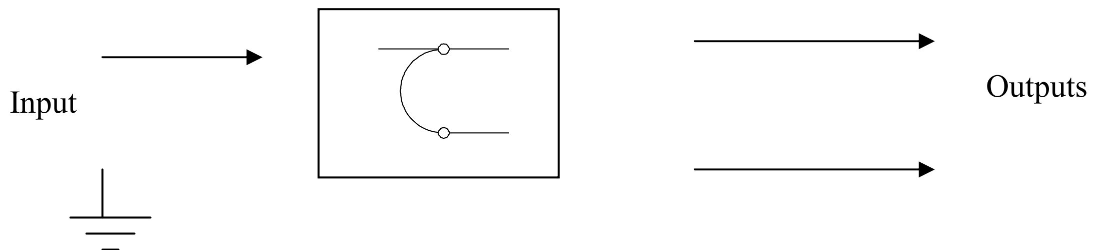


Figure 2.1. Functional representation of a balun.

Traditionally, baluns have been implemented using distributed components ([55]-[60]). Although this works very well from a performance standpoint, it also leads to large sizes for the devices at low frequencies. Lumped-element implementations (using coupled transformers or impedance matching networks) have been proposed as a means for size reduction ([61]-[63]). As with any lumped-element approximation, this also

results in degradation in performance, particularly in amplitude imbalance across the frequency bands.

Based on bandwidth of operation, baluns can be divided into wideband and narrow-band devices. Almost all the cell-phone frequency bands, along with GPS and the 2.4GHz ISM band applications (WLAN and Bluetooth), can be classified as narrow-band, with the operating bandwidths and percentage bandwidths ranging from 60MHz to 100MHz and ~3% to ~5% respectively. As shown in Figure 1.7, both single-band and multiband devices (with narrow or wide bandwidths at their frequencies of operation), are required in a multiband architecture.

The rest of the chapter is organized as follows: Section 2.1 deals with the development of multiband balun theory and Section 2.2 with the extension of the theory for the design of compact wideband baluns. Examples have been implemented in both cases to verify the design methodology. Finally, Section 2.3 covers the design of completely shielded low-profile narrow-band baluns on high-K organic substrates. Again, the designs have been verified by fabricating and measuring test-devices.

2.1. Multiband Baluns

Traditionally, the Marchand topology has been the preferred means for implementation of baluns ([55]-[57]), because of its low loss and wide bandwidth. It uses two $\lambda/4$ coupled-line pairs, and exhibits very good amplitude and phase balance. Figure

2.2 shows the simplified schematic of a Marchand balun ([56], [58]). Owing to the use of distributed elements, the size of the balun becomes prohibitively high at low frequencies, as mentioned above. Several methods (impedance variation, capacitive loading etc.) have been suggested ([58], [64]-[65]) for reducing the balun size; however, they all result in a reduction of the percentage bandwidth also.

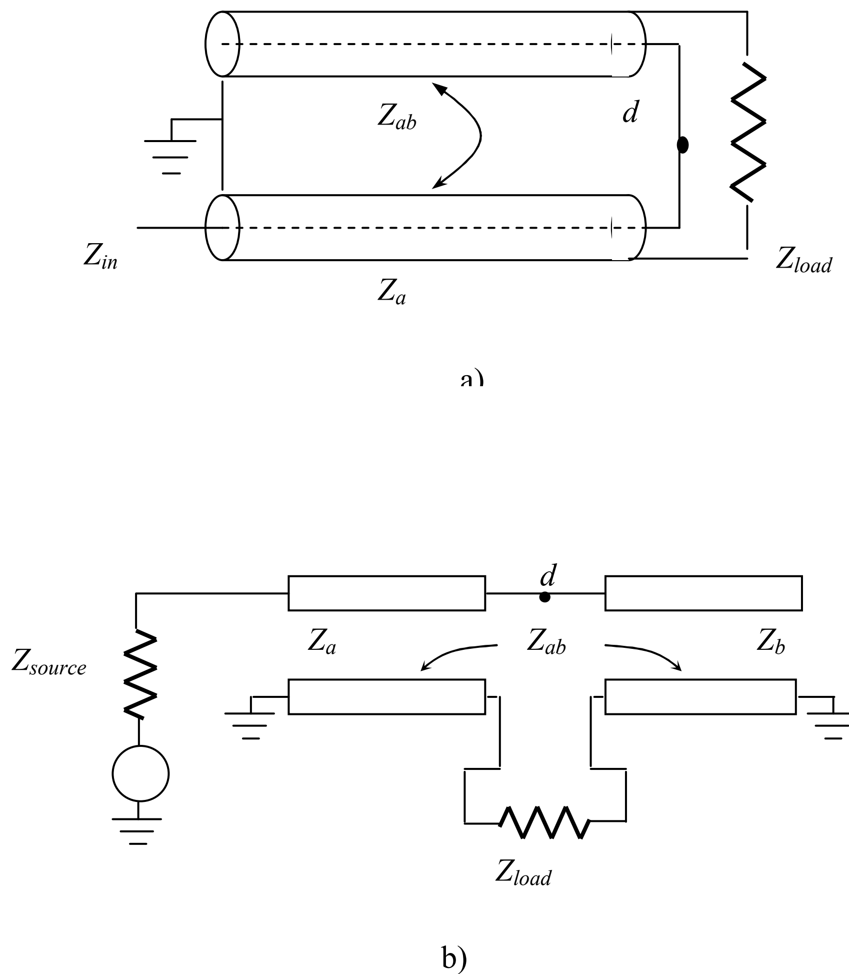


Figure 2.2. **a)** Coaxial balun **b)** Simplified schematic

The input impedance seen at *d* has been derived as [56]

$$Z_d = \frac{Z_{load}}{\frac{Z_{load}^2}{Z_{ab}^2 \tan^2\theta} + 1} + \frac{jZ_{load}^2 Z_{ab} \tan\theta}{Z_{load}^2 + Z_{ab}^2 \tan^2\theta} - jZ_b \cot\theta \qquad (2.1)$$

where θ is the electrical length of the transmission line segments, and the rest of the variables are as shown in Figure 2.2. The impedance seen by the source (Z_{in}) can then be calculated by transforming Z_d with a length of transmission line with characteristic impedance Z_a (assuming lossless operation), as

$$Z_{in} = Z_a \frac{Z_d + jZ_a \tan\theta}{Z_a + jZ_d \tan\theta} \qquad (2.2)$$

The input return loss S_{11} is thus a function of Z_a, Z_b, Z_{ab}, Z_{load}, Z_{source} and θ. Perfect matching ($\mathrm{Im}(Z_{in}) = 0$ and $\mathrm{Re}(Z_{in}) = Z_{source}$, leading to $S_{11} = 0$) occurs when Z_a is set equal to $(Z_{source}.Z_{load})^{1/2}$ and the lengths of the transmission line segments are chosen such that $\theta = 90°$. However, it has been shown in [58] that a perfect input match can be achieved at two angles θ_1 and θ_2, by setting:

$$Z_{ab} = Z_{load}, \qquad Z_a = Z_b = Z_{load} \sin^2\theta_{1,2} \qquad (2.3)$$

θ_1 and θ_2 are obtained by the input/output impedance ratios, and lie symmetrically above and below 90°. The input match at the band-center (corresponding to $\theta = 90^{\circ}$) is reduced as a result, but the *S11* is still less than -15 dB, meeting most specifications. In (2.3), θ_1 and θ_2 are functions of frequency, and are given by:

$$\theta_1 = \frac{\pi}{2}\frac{f_1}{f_0} \qquad \theta_2 = \frac{\pi}{2}\frac{f_2}{f_0} \qquad (2.4)$$

where f_0 is the frequency corresponding to 90°. It can thus be seen that by extending this analysis further, it is possible to create baluns that are simultaneously functional at two different frequencies f_1 and f_2, by choosing appropriate values for Z_a, Z_b, Z_{ab}, Z_{load} and Z_{in}.

Both [56] and [58] have used examples where θ_1 and θ_2 are obtained above and below 90° by using $Z_{load} \neq Z_{source}$. However, the source and load impedances are usually set by system requirements, and are beyond the control of the balun designer. Setting Z_a different from Z_b offers the designer an extra degree of freedom, and makes it possible to make the frequencies of operation independent of the load and source impedances. (This also results in the degradation of the input match at the center frequency f_0. However, as the applications are usually narrow band in nature, the low *S11* obtained at the two frequencies f_1 and f_2 are sufficient to make the balun functional).

As an example, a balun operating at both 900 MHz and 1.9 GHz with source and load impedances of 50Ω each was designed using the above methodology. The center frequency was chosen to be 1.45 GHz. Using (2.3), this yields values of 50Ω and 29.045Ω for Z_{ab} and Z_b respectively. By choosing Z_a = 64Ω, *S11* is obtained to be -16.575 dB at 800 MHz and 2.1 GHz. The *S11* at the center frequency (1.45 GHz) is -12.32 dB. Figure 2.3 shows the simulation (HP-ADS™) results of the device.

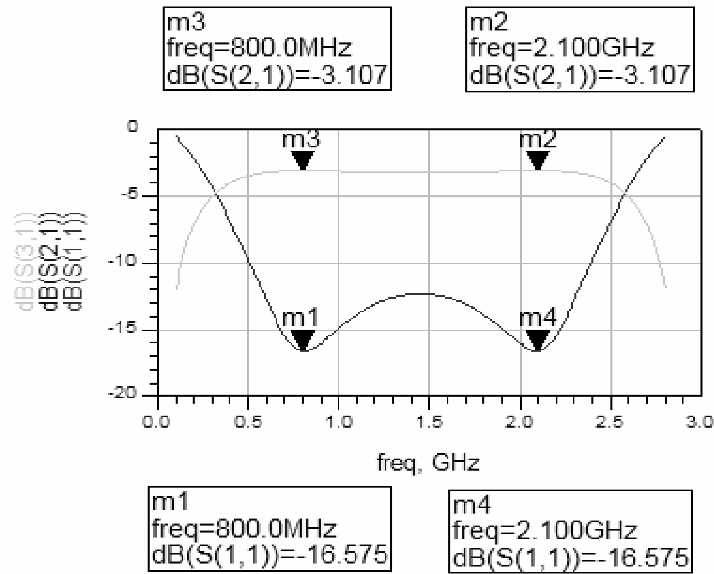


Figure 2.3. S-parameter simulation of the balun showing input match (S11) and power loss (S21 and S31) in the 800 MHz and 2.1 GHz frequency bands.

As has been shown in [66], any significant capacitive loading for reduction in device size also results in a reduction in the operational bandwidth as well, resulting in a tradeoff of larger size for higher bandwidth. In several dual-band applications, it is important to have a control over the individual bandwidth as well. For e.g., a WLAN access device supporting the 802.11a/b/g protocols requires a 100 MHz bandwidth centered around 2.44 GHz (for 802.11b/g) while a 1 GHz bandwidth centered around 5.4 GHz is required for 802.11a. A modification in the basic Marchand topology is thus required to achieve multiband functionality with controllable bandwidth at each frequency.

2.1.1. Theory

Figure 2.4 shows the schematic of a novel dual band balun. The device has a basic Marchand topology, but adds a frequency dependent imaginary impedance *X* (by way of inductors or capacitors) in series with the output load Z_{load}.

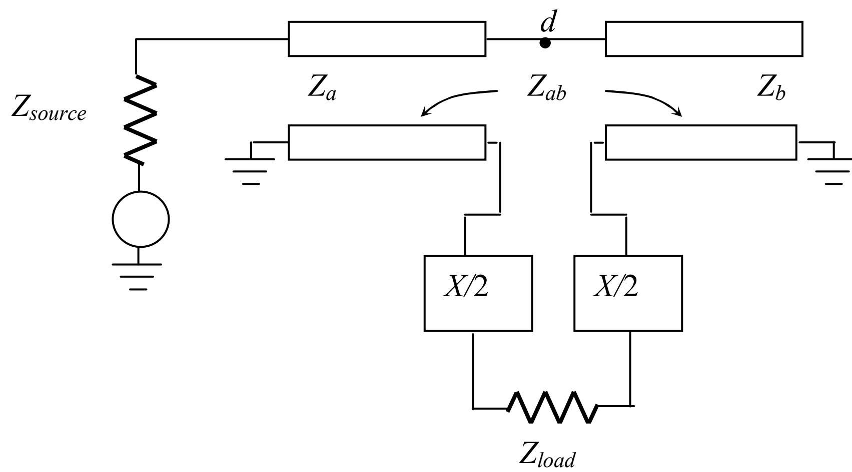


Figure 2.4. Schematic of the new balun, with two frequency dependent impedances (*X/2*) added in series with the load.

Equation (1) can be re-derived for the new topology as:

$$\mathrm{Re}(Z_d) = \frac{Z_{load} Z_{ab}^2 \tan^2\theta}{Z_{load}^2 + (X + Z_{ab}\tan\theta)^2} \tag{2.5a}$$

and

$$\text{Im}(Z_d) = F_1(\theta) - F_2(\theta) \tag{2.5b}$$

where

$$F_1(\theta) = \frac{Z_{ab}\tan\theta(Z_{load}^2 + X^2 + XZ_{ab}\tan\theta)}{Z_{load}^2 + (X + Z_{ab}\tan\theta)^2} \tag{2.5c}$$

and

$$F_2(\theta) = Z_b \cot\theta \tag{2.5d}$$

Plotting $F_1(\theta)$ and $F_2(\theta)$ with respect to frequencies, the imaginary part of Z_d becomes zero at frequencies where the $F_1(\theta)$ and $F_2(\theta)$ curves cross each other. *Assuming the values of impedances Z_a, Z_b, Z_{ab} and X can be chosen such that Z_{in} presents a matched load to Z_{source} at these frequencies,* a balun operating at multiple frequencies can be implemented.

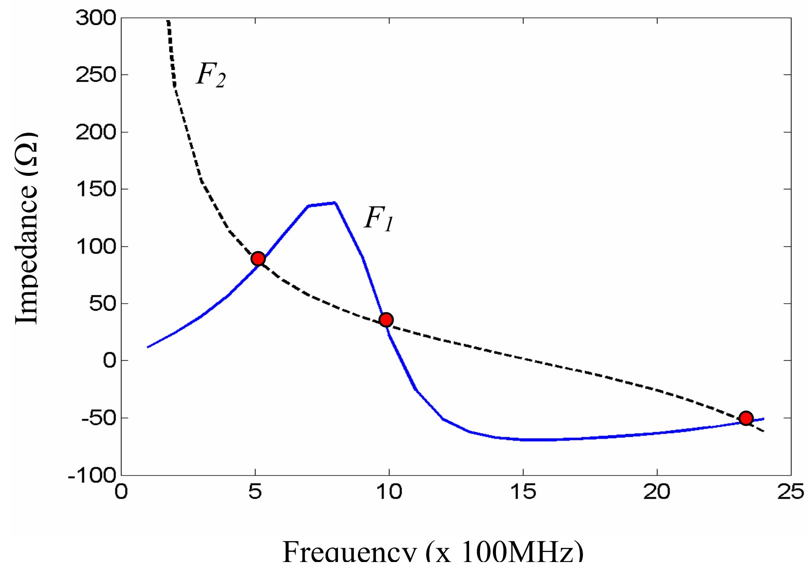
As an example, Figure 2.5a shows the plot of $F_1(\theta)$ and $F_2(\theta)$ with respect to frequency, with the length of the transmission line segments chosen to be $\lambda/4$ at 1.53GHz (midway between 0.93 and 2.13GHz). For the calculations, Z_a and Z_b have been set as 50Ω, Z_{ab} as 100Ω and Z_{source} and Z_{load} as 50Ω. X has been represented using a 1.5pF capacitance. As can be observed, for the given conditions, the curves cross each other at three frequencies, at ~0.5, ~0.9 and ~2.2GHz.

Based on the plots, the following observations can be made:

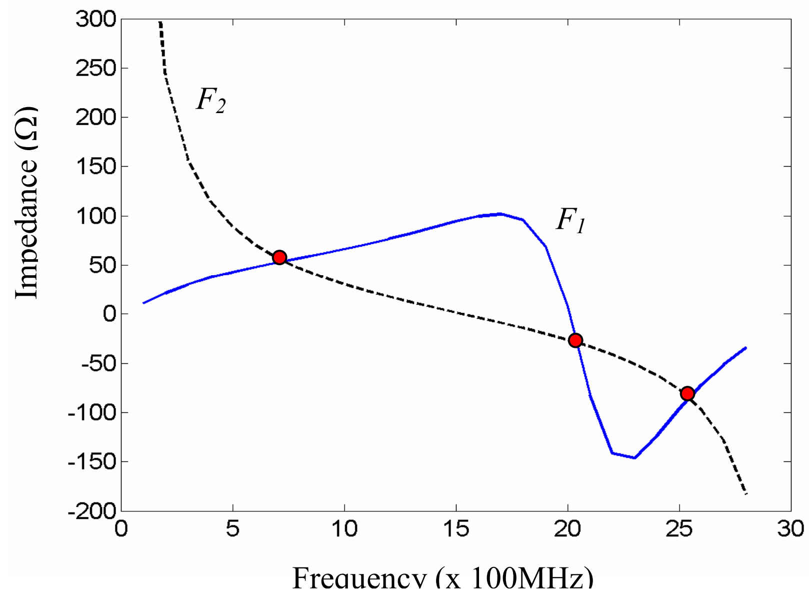
1. Im(Z_d) has three zero crossings. The length of the coupled-line segments determines two of the zero-crossings (0.9 and 2.2GHz) while the choice of Z_b, Z_{ab} and X determines the third.
2. The slopes of the curves (or the angle between the curves) at the frequencies where they intersect determine the bandwidth of the balun at that frequency. For the above

example, the angles of intersection at 0.5 and 0.9GHz are much larger than the angle at 2.2GHz, predicting narrow lower band and wide upper band for a potential multiband balun.

3. The *shape* of the curve $F_1(\theta)$ is dependant on the sign of the reactance X. The use of a 10nH inductance in place of the capacitance in the above example results in a drastically different graph (Figure 2.5b). The angle of intersection at the lower frequency is now much smaller than the one at the upper frequency, predicting a wide lower-band and narrow upper-band of operation for this device.



a)



b)

Figure 2.5. Plot of $F_1(\theta)$ and $F_2(\theta)$ with respect to frequency **a)** X=1.5pF **b)** X=10nH

The use of the two extra components thus gives the designer an extra degree of freedom, which can be used to control the operation of the balun at different frequencies with controllable bandwidth at each of the frequency bands.

The condition for input match (and hence S_{11}=0) is satisfied when $Z_{in} = Z_{source}$. Assuming Im(Z_d) = 0, this results in the condition

$$Z_{source} = Z_a \frac{\mathrm{Re}(Z_d) + jZ_a \tan\theta}{Z_a + j\,\mathrm{Re}(Z_d)\tan\theta} \tag{2.6}$$

Separating the imaginary and real parts and equating them, we get the following condition:

$$\mathrm{Re}(Z_d) = Z_{source} = Z_a \tag{2.7}$$

Given that (2.5b) shows $F_1(\theta) = F_2(\theta)$ for Im(Z_d) = 0, we now have a methodology for the design of the baluns:

Step1: Choose $Z_a = Z_b = Z_{source}$

Step2: Choose the two frequencies of operation for the multiband balun (the farther the upper frequency band is from the lower band, the larger the reduction in size). Choose the length of the coupled-line segments such that they are λ/4 at the frequency approximately midway between the two operational frequencies.

Step3: Plot Im(Z_d) and Re(Z_d) with respect to frequency for different values of X (the reactance at the output) and Z_{ab}. Choose values of X, Z_{ab} that simultaneously satisfies Im(Z_d) = 0 and Re(Zd) = Z_{source} at the frequencies of interest.

It is to be noted that the use of inductors or capacitors in series with the load changes the electrical length of the transmission line segments. Inductors result in electrically shorter devices, which require an increase in the physical size of the device. Capacitors on the other hand lead to an increase of electrical length, effectively reducing the physical size of the device. Capacitive loading of the transmission line segments can be done independent of the load elements used, leading to further reductions in device size.

2.1.2. Design

To validate the theory of multiband Marchand baluns, a 50Ω-100Ω balun for use in the 930MHz and 2130MHz frequency bands was designed for a 3-metal layer LCP process. It consisted of a 1-mil diclad low loss laminate, LCP, ($\tan\delta = 0.002$, $\varepsilon_r = 2.95$) laminated onto a low loss core layer that is 30 mils thick (Fig 2.6).

Two capacitors of 3.5 pF each were used in series with the load impedance to make the balun functional at both frequencies. To further reduce the size of the device, capacitive loading was employed with the use of four more embedded capacitors (each 2.5 pF in value). This resulted in the physical length of the transmission line segments being $\lambda/10$ (or $\theta = 35.47^{\circ}$) at 1.53 GHz (the frequency midway between 930 MHz and 2130 MHz). Figure 2.6 shows the circuit simulation results (using HP-ADS™).

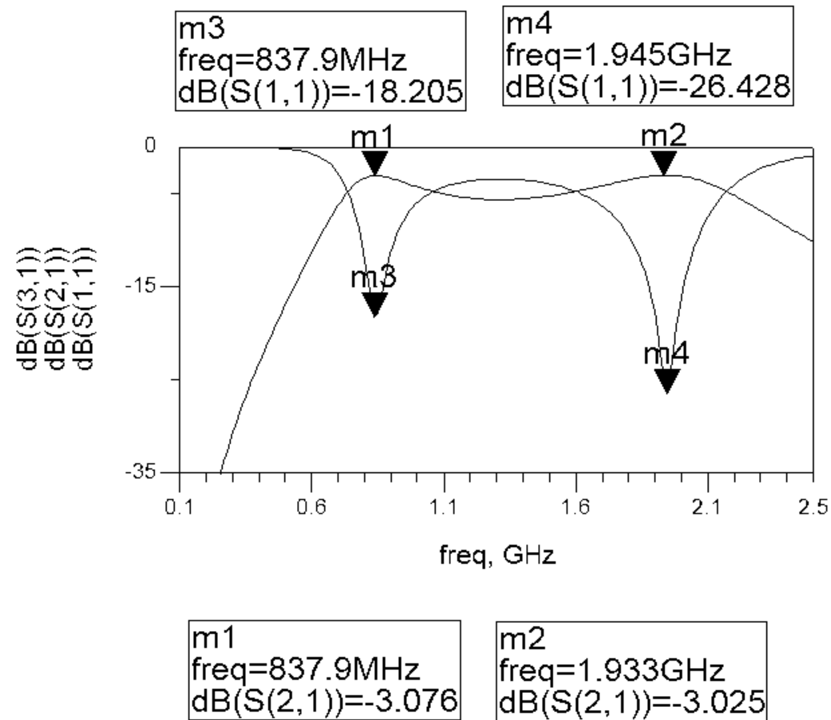


Figure 2.6. S-parameter simulation of the balun, showing input match (S11) and power loss (S21 and S31) in the 830 MHz and 1.93 GHz frequency bands.

2.1.3. LCP-Based SOP Technology for Large Area Manufacturing

An LCP-based SOP technology was used for implementing the baluns [63]. It combines 25μ thick LCP dielectric with low tanδ glass-reinforced organic prepregs in a multilayer stack-up with 3-24 metal layers. Through-holes are mechanically drilled and plated to form interconnections, while lasers are used to create microvias as small as 100μ in diameter in the LCP layers. All the passive circuits are embedded in the internal

LCP layers, which are then packaged using low-loss laminate layers to provide mechanical strength and enhanced reliability. The low-loss dielectric layers combined with thick metallization results in high-Q inductors (Q of ~120) and capacitors (Q of ~200). The outer layers of the final packaged devices are protected using liquid photoimageable soldermask layers, and the exposed bond pads and/or terminals are plated with electroless nickel or immersion gold finish.

The devices are laid out in panels of size 9”x12” and 12”x18” using large area PWB tooling (Figure 2.7) [63], resulting in a low-cost implementation that can be easily scaled to 18”x24” panel size for further cost reduction (recall here that typical LTCC components are manufactured on substrate sizes less than 8"x8" in area). The fabrication of components on 18"x24" size substrates results in more than a 10X increase in the number of yielded components for a given board over ceramics. For example, a single 18”x24” panel can yield *more than 50,000 0805 devices (packaged size of 2mm x 1.25mm)*.

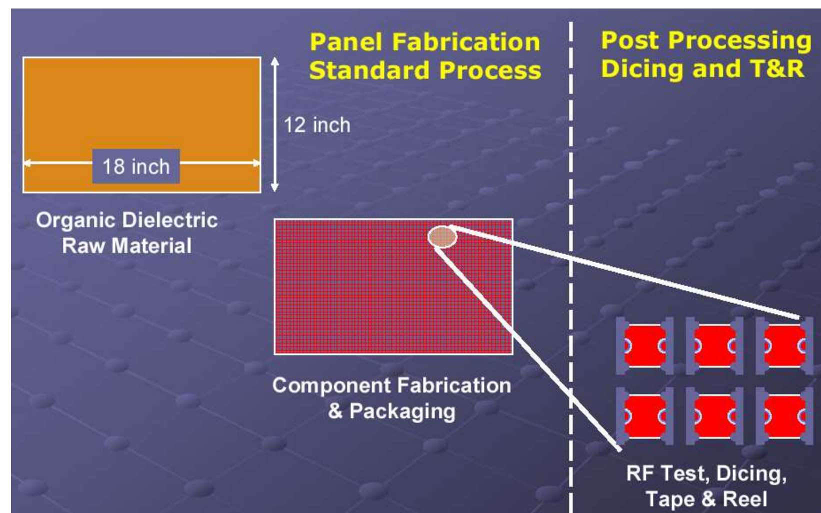


Figure 2.7. Large area manufacturing process.

IC assembly, high frequency electrical/full functional test and over-molding operations are performed on sub-panels of 6”x6” size prior to dicing of the individual modules. The technology includes a novel structure that allows for on-board RF shielding of each of the devices prior to singulation, thereby precluding the need for EMI cans which increases both cost and size.

All processes including lamination (at temperatures <200°C), electroless and electrolytic copper plating and dry film photoresists are compatible with standard FR-4/PWB manufacturing processes. However, the organic dielectrics this process technology utilizes have extremely low moisture uptake (unlike conventional PWB materials). Typical moisture uptake rates for the packaging materials are <0.05% and lead to ceramic-like near-hermetic packaging at organic PWB manufacturing costs.

The fully packaged substrate has a CTE matched to typical organic materials used in PWB technology like FR-4 with coefficient of thermal expansion (CTE) around 18-20ppm/°C. The CTE match allows for large modules to be implemented with very high reliability. Further, the material set can be adjusted to tailor the package CTE in the 3-20ppm/°C range, resulting in expansion matched packages and modules for various RF IC platforms like CMOS, SiGe and GaAs.

The technology has been validated for up to 12 LCP layers. Depending on component density requirements, the stack-up can be designed to have all or some of these multiple LCP layers. The technology is also versatile enough to include multiple dielectric layers with electrical properties vastly different from that of LCP. For e.g., the integration of Oak-Mitsui’s BC12TM (with ε_r of 10 and $\tan\delta$ of 0.02) into the basic stack-up has been successfully demonstrated, paving the way for heterogenous stackups that

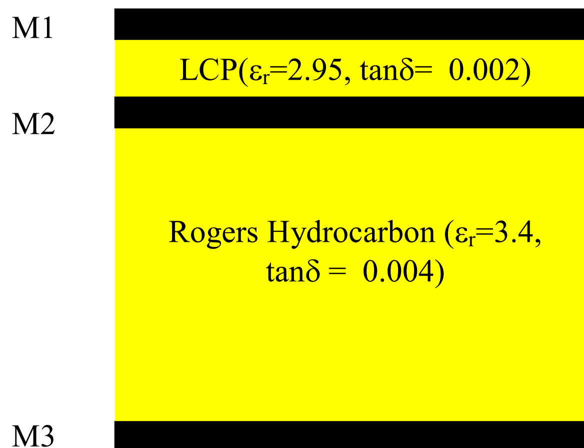
will provide functional dielectric layers with both low-loss/low-K and high-loss/high-K properties.

This novel LCP-based stack-up thus provides all the features and benefits envisaged in an ideal organic mixed-signal SOP technology in Chapter 1 (Figure 1.8). It provides a heterogenous stack-up for the efficient implementation of different functions. It is also amenable to large area manufacturing, resulting in low cost devices. The low moisture uptake of the laminate materials used results in near-hermetic packaging for the devices. Finally, it is versatile enough to be used in the implementation of devices either in a substrate or as an IPD. This LCP-based SOP approach thus results in an organic integration platform, resulting in devices with much lower manufacturing cost and significantly higher performance compared to ceramics.

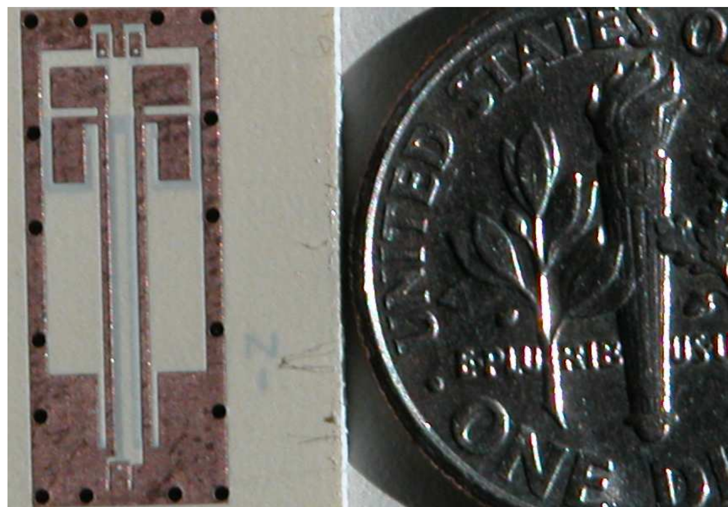
2.1.4. Fabrication and Measurements

Figure 2.8a shows the stack-up used to implement the multiband baluns. A single layer of LCP was attached to a 30mil low-loss laminate using 4mil low-loss prepreg. The coupled line segments were implemented as edge-coupled devices, with the required values of odd and even mode impedances achieved by placing each line of a coupled line pair in each of the two metal layers (M1 and M2) on both sides of the LCP layer. The reference ground was laid out in conductor-backed Co-Planar Waveguide (CPW) fashion, with the ground structures on M1 and M2 connected to the ground plain on M3 using through-holes.

Figure 2.8b shows the photograph of the fabricated balun. The device measures 1.5 cm x 0.6 cm, including co-planar waveguide (CPW) ground rings and probe pads. Figure 2.9 shows the measured values for *S11*, *S21* and *S31*, along with post-layout full-wave simulation results (Sonnet™, a commercial 2.5D Method-of-Moments tool, was used as the full-wave solver).

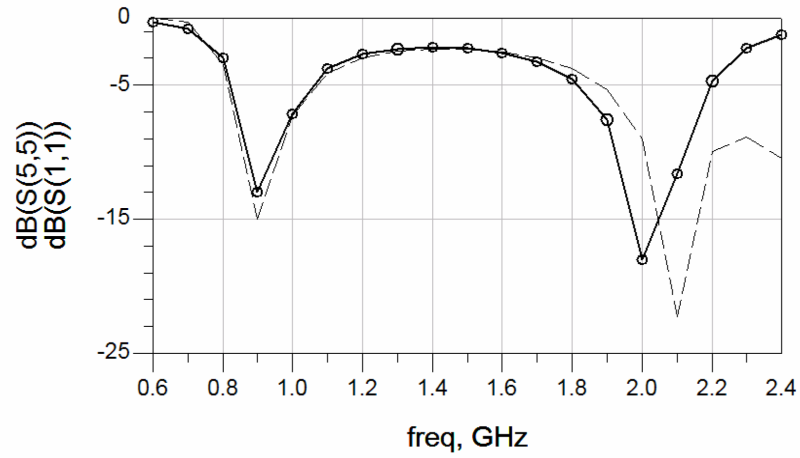


a)

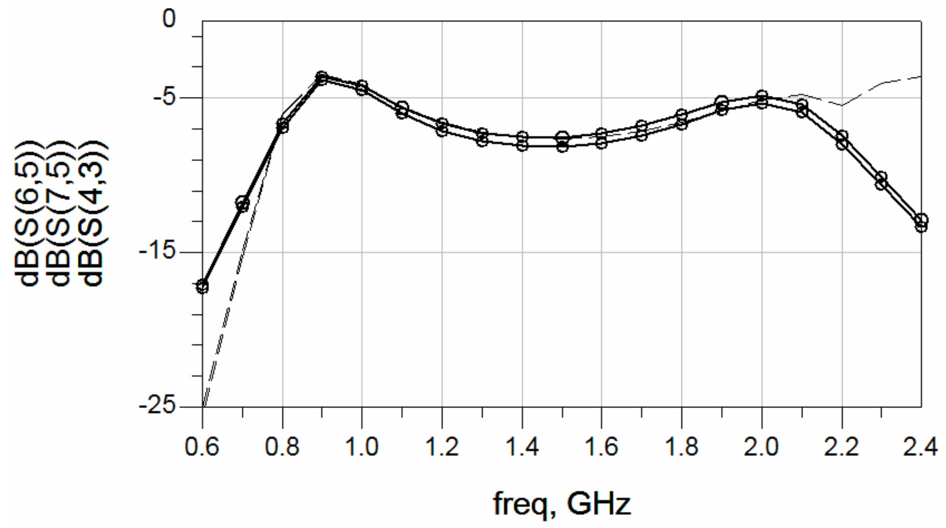


b)

Figure 2.8. a) 3-metal layer LCP-based stack-up and **b)** photograph of the fabricated balun. The device measures 1.5 cm x 0.6 cm, including the CPW ground rings and probe-pads.



a)



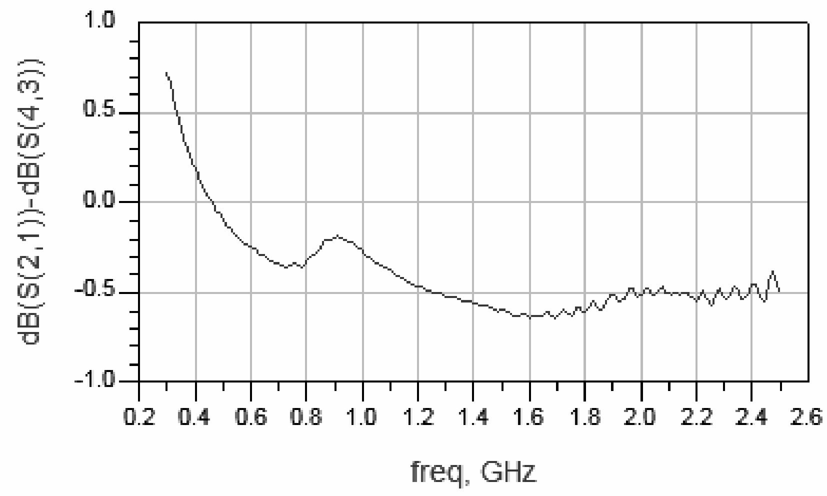
b)

Figure 2.9. Simulated (Sonnet) and measured results for the fabricated balun **a)** Input match (S11) **b)** Power transfer (S21 and S31). Solid line with dots represent measured values, dashed line represents simulated results.

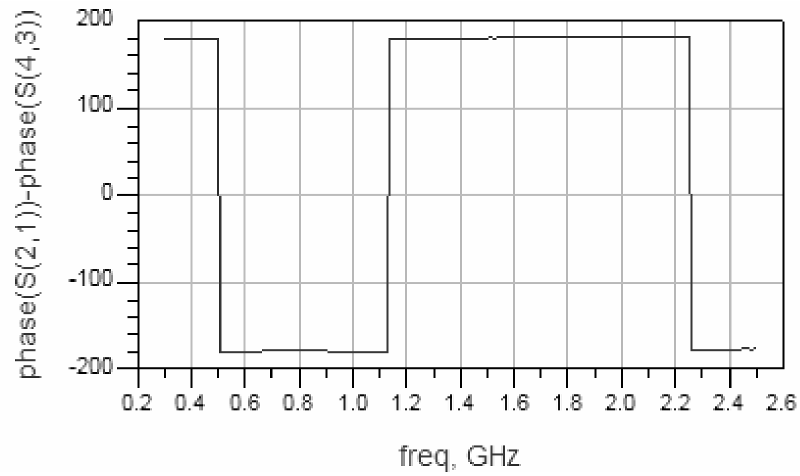
The measured *S11* dips to -14.5 dB at 920 MHz. However, the upper band exhibits a downward shift in frequency, with *S11* reaching a minimum of -32.4 dB at 2.03 GHz rather than at 2.13 GHz based on the design. A small shift in layer-to-layer alignment during fabrication contributed to this frequency shift. The loss, which is less than a dB in the lower frequency band increases beyond 1 dB for the upper band. This is due to significant back coupling between the output capacitors and the coupled line segments. The need to minimize device size resulted in a very compact layout. The phase balance is less than a degree in the lower band, but increases to a maximum of 2.5° in the upper band. The amplitude balance is less than 0.25 dB in the lower band while it increases to a maximum of 0.6 dB in the upper band. Figure 2.10 shows the measured amplitude and phase imbalance. Table 2.1 summarizes the measurement results for the balun.

Table 2.1: Measured performance of the balun.

	920 MHz	**2.03 Ghz**
Bandwidth	70 MHz	160 MHz
S11	-14.5 dB	-32.4 dB
S21	-3.54 dB	-4.93 dB
S31	-3.73 dB	-5.35 dB
Amplitude Imbalance	0.19 dB	0.42 dB
Phase Imbalance	0.73°	1.9°



a)



b)

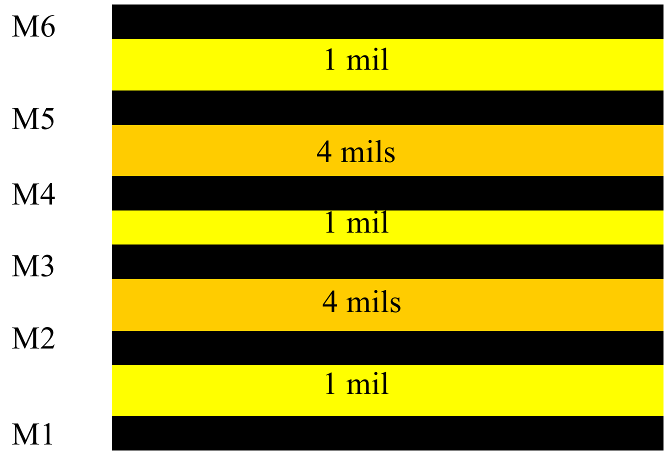
Figure 2.10. Measured **a)** amplitude and **b)** phase imbalance for the balun.

2.2. Extension of the Theory of Multiband Marchand Baluns – Wideband Singleband Baluns

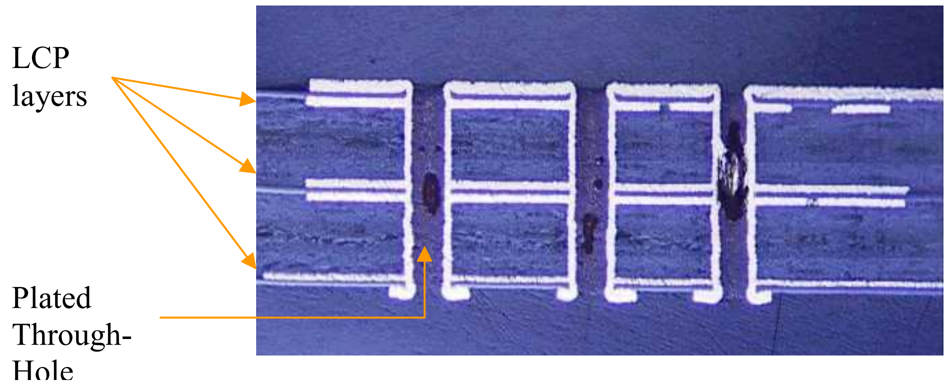
The multiband balun theory just described can be applied in the design of compact single-band baluns with wide bandwidths [67]. As shown in Figure 2.5b, the use of an inductance to implement the reactance X results in a multiband balun with a wide lower-band and narrow upper-band of operation. The length of the coupled-line segments are $\lambda/4$ at a frequency approximately midway between the upper and lower bands of operation. Neglecting the upper band of operation, the device can be thought of as a single-band balun, but now with an effective electrical length of the coupled line segments considerably lower than $\lambda/4$ (θ=90°). A size reduction has thus been achieved without the use of any capacitive loading. In fact, a small amount of capacitive loading (depending on the bandwidth requirements of the balun) can be used in conjunction with this technique for a further reduction in size.

2.2.1. Design, Fabrication and Measurements

Figure 2.11 shows the cross section of the packaging substrate used. Based on the LCP stack-up described in Section 2.1.3, the 6-metal layer technology incorporates three diclad LCP layers that are bonded together by a lower-melt adhesive. The adhesive layers have a loss tangent of 0.0035 with a dielectric constant of 3.38. The top and bottom metal layers (M1 and M6) are used to provide complete shielding, to minimize EMI and radiation.



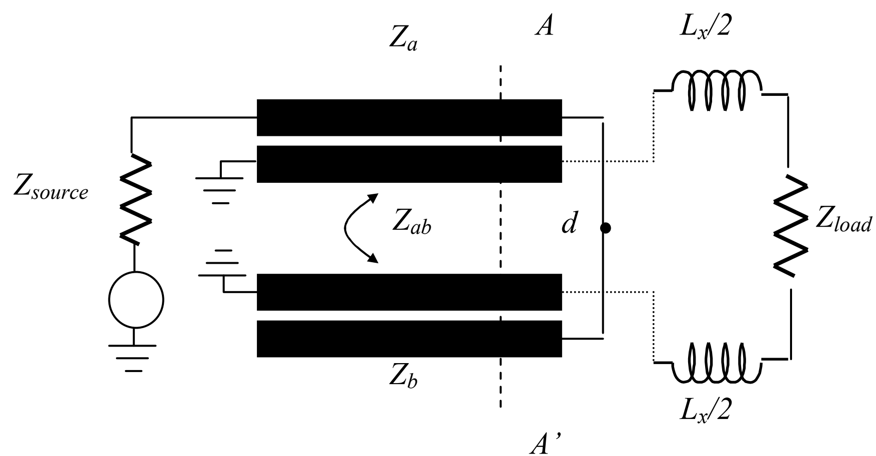
a)



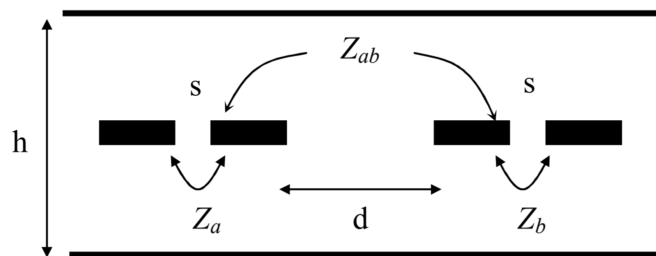
b)

Figure 2.11. **a)** Cross-section of the substrate **b)** Photograph of a cross-section

Figure 2.12 shows the layout of the balun in planar form. The cross-section of the balun along the A-A' axis and the implementation of the coupled-line segments in stripline topology is also shown in Figure 2.12. In the figure, h represents the total height of the substrate, s the spacing between the coupled lines and d the spacing between the coupled-line segments. Z_a, Z_b and Z_{ab} for the cross-section shown were calculated using a combination of Sonnet™ and Advanced Design System (ADS™), for different values of d, s and h.

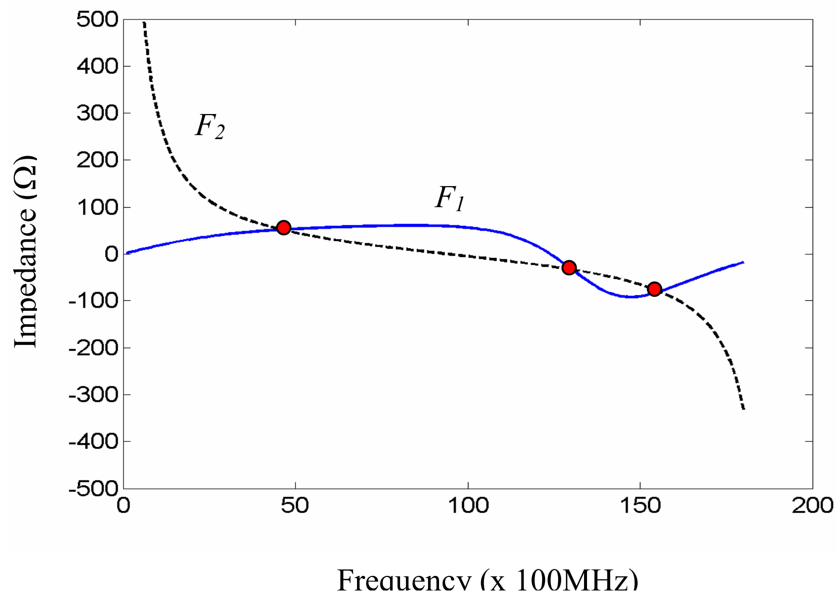


a)

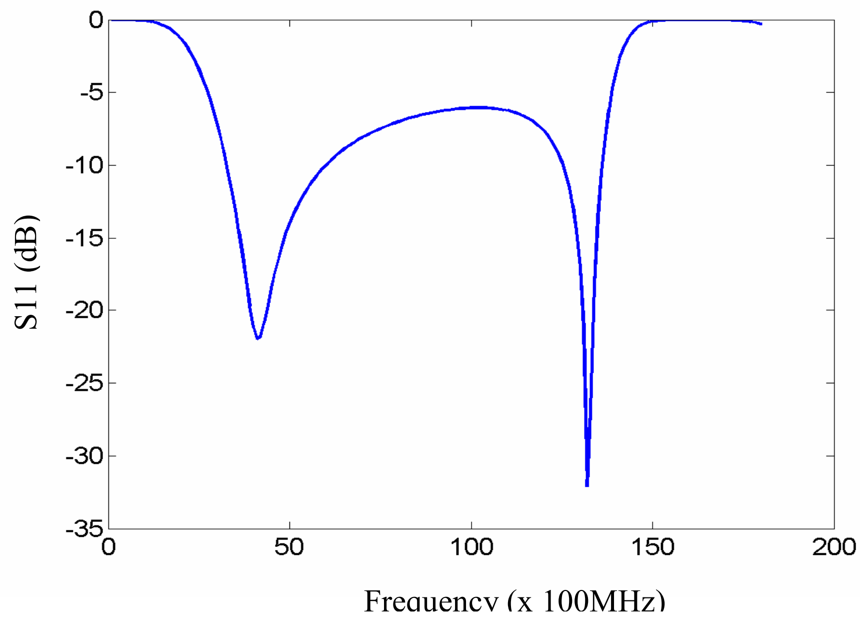


b)

Figure 2.12. **a)** Layout of the planar balun, and **b)** cross-section of the device cut along the A-A' axis.



a)



b)

Figure 2.13. **a)** Plot of Im(Z_d) vs. frequency showing the zero crossings (using the optimized values for L_x and Z_{ab}) **b)** Variation of S_{11} with frequency, calculated using (2).

As proof-of-concept for the design methodology, a 50-100Ω balun operating in the 4.9-5.9GHz band was designed for the LCP substrate technology described in the previous section. Figure 2.13a shows the optimized plot of Im(Z_d) with respect to frequency, where the values of the variables have been set as follows: $Z_a = Z_b = 50\Omega$, $Z_{ab} = 88\Omega$, $L_x =$ 1.5nH, frequency bands = 5.4 and 10.8GHz. The three zero crossings occur at 4, 11.3 and 13.3GHz, with the Re(Z_d) = ~Z_{source} (resulting in good input match) in the 5GHz and 13GHz frequency bands. The S_{11} calculated using (2.4)-(2.6) is also shown (Figure 2.13b). The plot predicts a wide lower band around 5.5GHz and a narrow upper band at 13.5GHz.

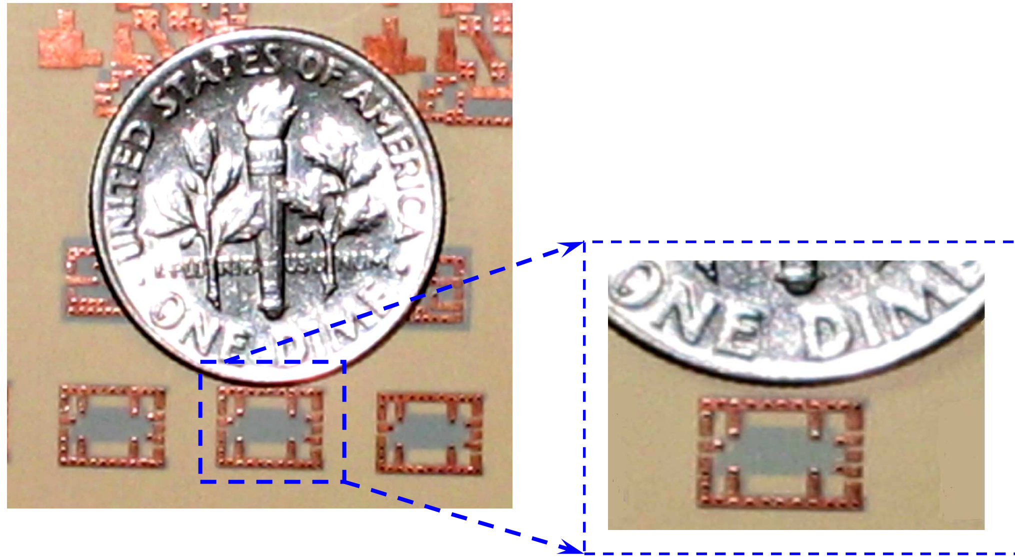
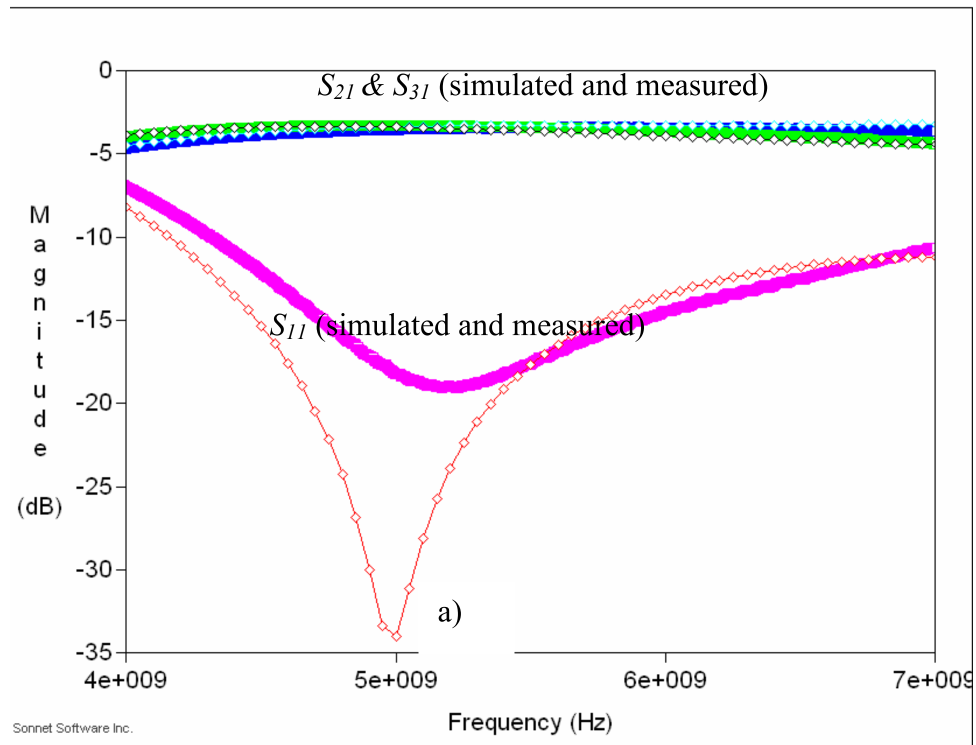


Figure 2.14. Photograph of the balun.



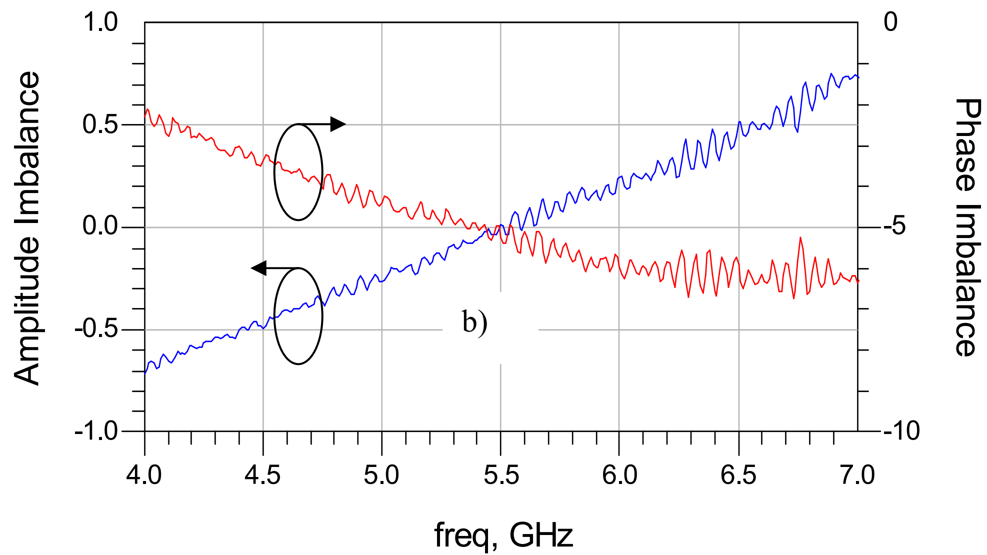


Figure 2.15. Measured balun response **a)** S_{11}, S_{21} and S_{31} **b)** amplitude and phase imbalance

The fabricated balun measures 3.85x1.34 mm^2 in area (Figure 2.13). The length of each coupled line segment is 119 mils, representing a ~64% size reduction over a conventional Marchand balun. Figure 2.14a shows a comparison of the measurements to the modeled (post-layout, full-wave simulation using Sonnet™) results. Figure 2.14b shows the measured amplitude and phase balance. There is good correlation between measured and modeled data for S_{21} and S_{31}. However, S_{11} shows a minimum of only –20dB, while the models predict a minimum of almost –35dB. This was traced to the value of L_x being lower than the 1.5nH required in the design. The default metal model in Sonnet does not consider the skin-effect, which is an important factor in the 5GHz frequency band. With currents now flowing on the top and bottom surfaces of a thick metal, the effective inductance is reduced, which Sonnet failed to predict (the latest version of Sonnet includes a thick-metal model which specifically addresses this concern). As such, the balun still exhibits a percentage bandwidth of 53% around 6.2GHz (for S_{11}<-10dB).

Table 2.2 shows the performance comparison of the balun with a commercially available Marchand balun (Model 4859B50-50C) from Anaren, Inc., also built on an organic substrate. As can be observed, the current balun matches the performance of the Anaren balun while effecting a 42% reduction in size.

Table 2.2. Performance summary of the balun, with a comparison with a commercially available Marchand balun from Anaren, Inc.

Device	**Anaren Balun**	**LCP Balun**
Frequency	4.8-5.9GHz	4.8-5.9GHz
Return Loss (S11) (min)	16dB	-15.5dB
Insertion Loss (max)	0.6dB	0.57dB
Amplitude Imbalance (max)	0.6dB	0.33dB
Phase Imbalance (max)	5°	6°
Area	9mm^2	5.16mm^2

2.3. Narrowband Lumped-Element Baluns

As mentioned earlier, lumped-element baluns have lower operating bandwidths compared to distributed-element designs. But in several narrow-band applications like cell-phone (bandwidth ranging from 20MHz to 75MHz) and WLAN at 2.4GHz (100MHz bandwidth), they are more preferable due to their small size.

In a SOP-based module strategy like the one shown in Figure 1.8, the small size of these baluns makes them prime target for implementation as stand-alone devices attached to the top of the substrate. The implications of such an approach are two-fold:

1. The thickness of the baluns needs to be kept as low as possible, so that the total height of the module after assembly remains low. This rules out the use of multilayer packaging for the implementation of the balun. With the design restricted to a single dielectric layer, the size of the device is directly proportional to the dielectric constant of the material. To achieve the low sizes required to make the module implementation possible, this necessitates high-K substrates with high capacitance density.
2. Commonly used material for the overmold exhibits high tanδ and high coefficient of moisture absorption. To prevent variation in performance with temperature, this necessitates the balun to be completely shielded, ruling out unshielded microstrip-based implementation schemes for the lumped elements.

2.3.1 Design

The lattice topology [63] is a commonly used lumped-element solution for implementing small size narrow-band baluns (Figure 2.16). A combination of low-pass/high-pass networks allows the splitting of input signal into two output signals that are equal in power but with a 180° phase difference. The low-pass/high-pass networks can be implemented with as low a number as four passives (two inductors and two capacitors), leading to small sizes (with the tradeoff of narrow-band operation). The circuit topology also lends itself well to impedance transformation.

The design equations for the device are as follows:

$$Z_0 = \sqrt{R_{source1} . R_{load}} \quad (2.8)$$

$$L = \frac{Z_0}{\omega_0} \qquad C = \frac{1}{Z_0 \omega_0} \quad (2.9)$$

where R_{source} and R_{load} are the source and load impedances, and $\omega_0 = 2\pi f_0$ is the frequency of operation,.

As a proof-of-concept device, a balun operating at 2.44GHz (with a 100MHz bandwidth) was designed for the high-K stack-up. For R_{source} and R_{load} of 50Ω and 100Ω respectively, this yielded values of 0.92pF and 4.6nH for the capacitance and inductance.

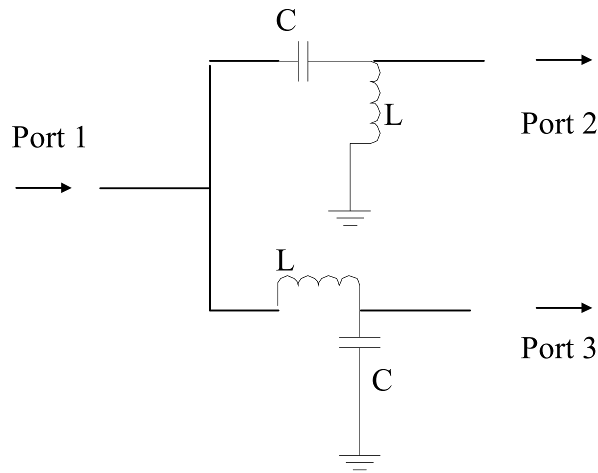


Figure 2.16. Lattice balun schematic

2.3.2 Fabrication and Measurements

With the thickness limitation restricting the use of multiple dielectric layers and size limitations restricting the use of low-K materials, the use of the dielectric stack-up of the previous sections (involving LCP, ε_r of 2.95) is not possible. Figure 2.17 shows a 0.5mm thick novel stack-up incorporating Oak-Mitsui's FaradFlex™ BC-12TM. With tanδ of 0.019, ε_r of 10 (both defined at 1MHz) and thickness of 12μm, the material has been developed for embedded digital decoupling applications. However, the high capacitance density (11nF/inch^2 at 1MHz) makes this a suitable candidate for small size low-profile baluns also. In fact, the lattice topology is particularly suitable for design on this material, as it uses low-pass/high-pass structures that are more tolerant to dielectric losses compared to band-pass structures.

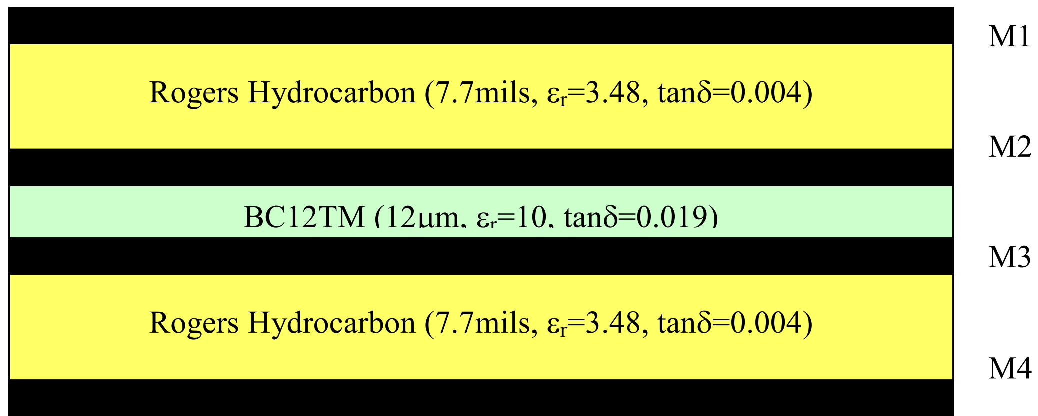


Figure 2.17. 4-metal layer stack-up with high-K dielectric layer

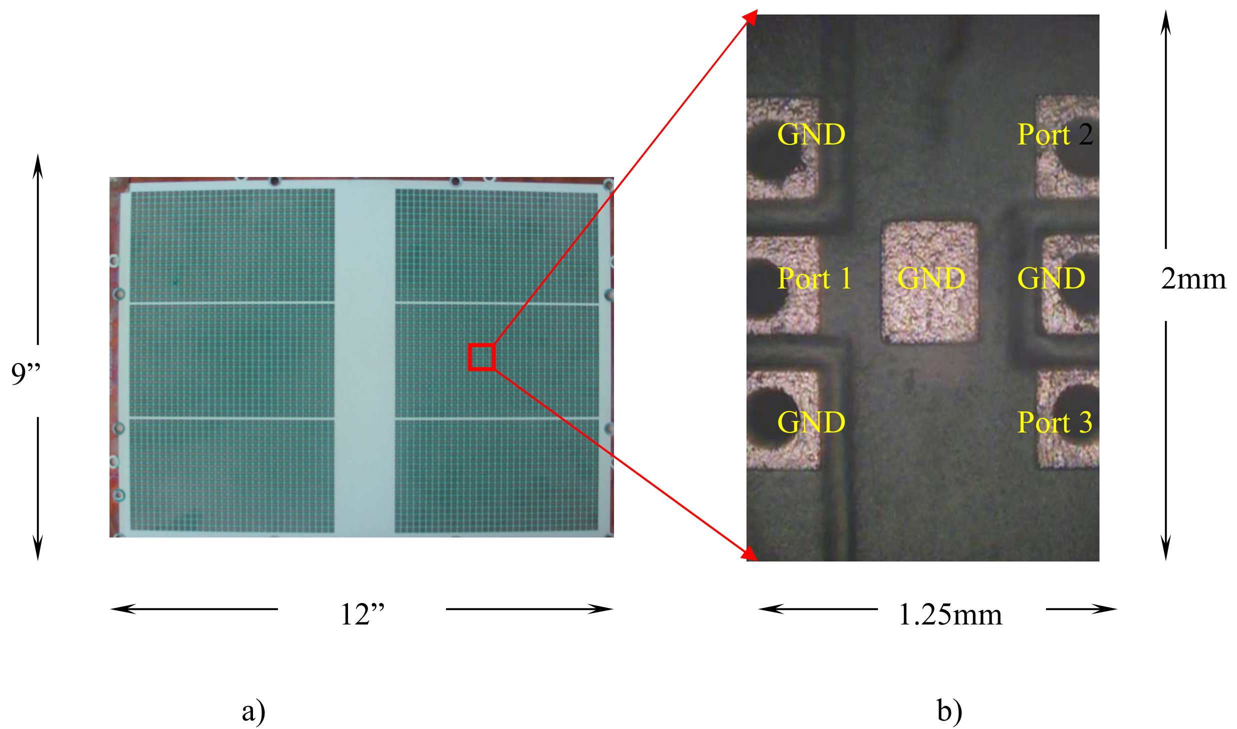


Figure 2.18. a) Photograph of the fabricated 9'x12' panel showing the baluns laid out in six coupons, and **b)** close-up of the device after dicing, showing the input and output ports.

Figure 2.18a shows the fabricated 9”x12” panel with the baluns laid out in six coupons, and Figure 2.18b shows the photograph of a fabricated device. The device measures 1.25mm x 2mm in area, with a thickness of 0.507mm. Fig 2.19 shows the measured return loss and insertion loss of the balun in the frequency band of interest. Figure 2.20 shows the measured amplitude and phase imbalance.

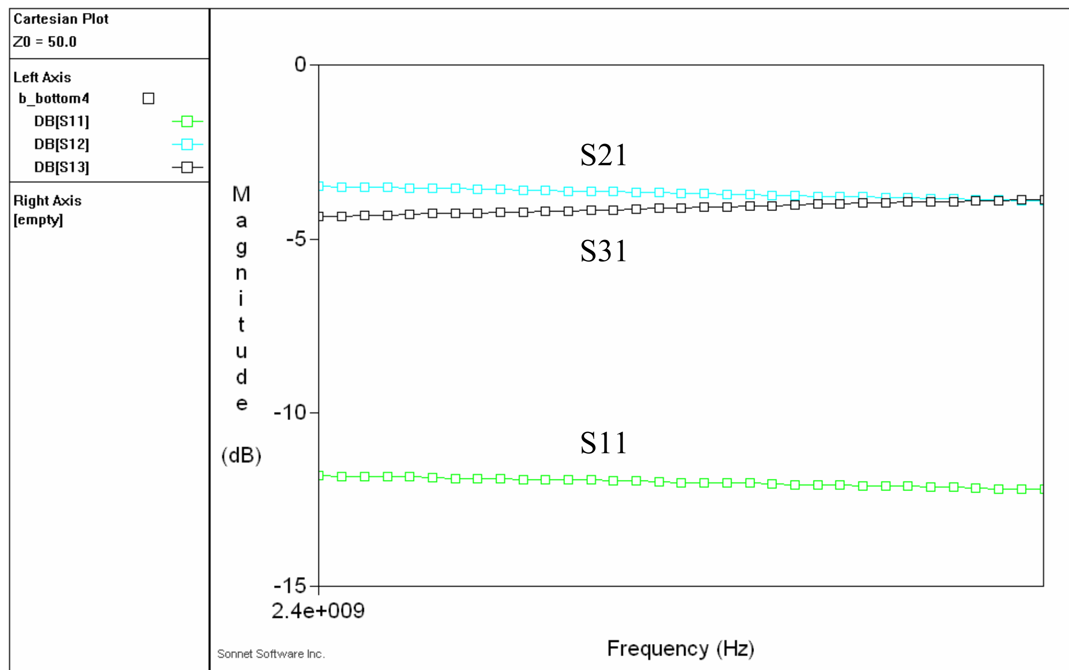
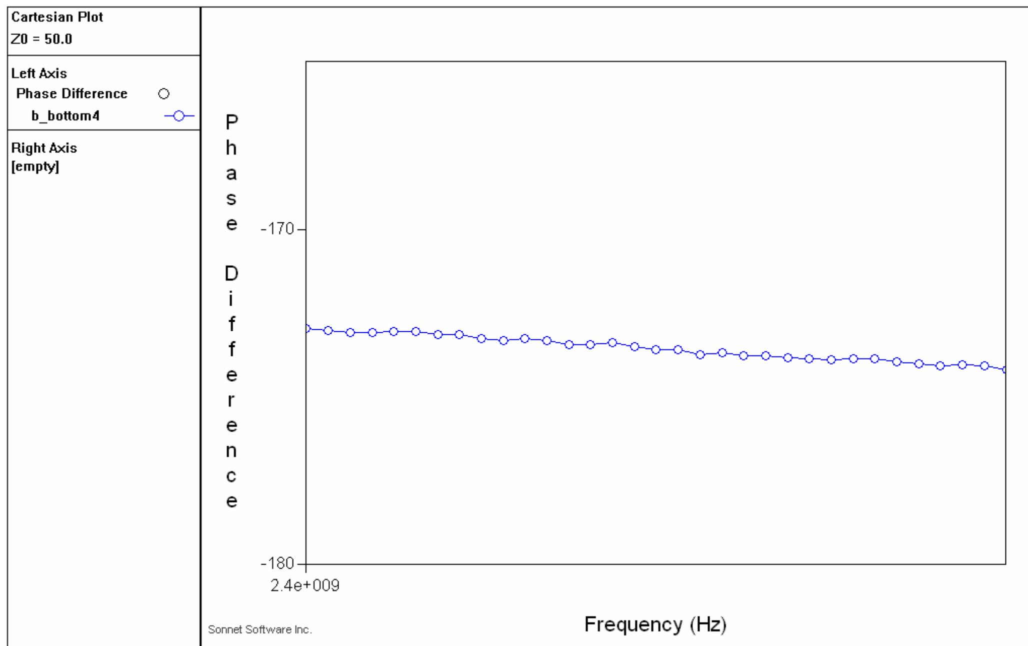
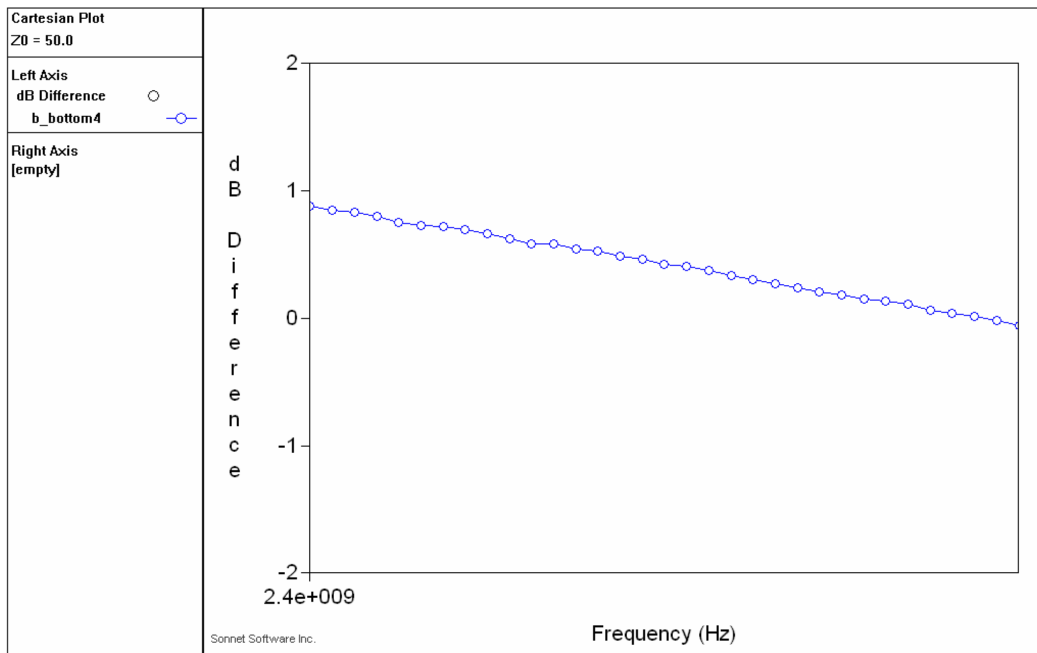


Figure 2.19. Measured values for S11, S21 and S31.



a)



b)

Figure 2.20. Measured values for **a)** Amplitude imbalance and **b)** Phase imbalance.

Table 2.3 summarizes the performance of the balun, along with a comparison with a commercially available LTCC balun (Murata LDB21G410C-001) of the same size. As can be observed, the organic balun meets the performance of the LTCC device in almost all the specifications, at the same time achieving a height reduction of almost 45%.

Table 2.3. Performance summary of the balun, with a comparison with a commercially available LTCC balun (*Note: The Murata balun was chosen for comparison because it specs the lowest loss for an 0805 balun in the market today. However, the amplitude and phase imbalance information was not available for the LDB21G410C-001. Typical industry standard numbers have been used for the imbalance comparisons).

Parameter	**LTCC Balun**	**Organic Balun**
Size	2mm x 1.25mm (+/- 0.1mm for both axes)	2mm x 1.25mm
Thickness	0.95mm	0.5mm
Insertion Loss	0.9dB max (@25C)	1dB
Amplitude Imbalance *	2dB	2dB
Phase Imbalance *	180+/-10 degrees	180+/-10 degrees
Shielding	?	Yes

2.4. Summary

The design of both multiband and single-band baluns have been covered in this chapter. The multiband baluns have been implemented using a modified Marchand architecture, resulting in good input impedance match at multiple frequencies. As the Marchand topology ensures good amplitude and phase balance, this results in a balun operational at multiple frequencies. As an extension of the theory, compact wideband baluns have been developed. By using only the lower operational band of a multiband balun, the effective electrical length of the transmission line segments in the Marchand topology can be reduced below 90°. The theory also provides for controlling the bandwidth of operation at this frequency (by varying the sign of the reactance used in series with the output impedance), resulting in an alternative to the use capacitive loading for size reduction in transmission line baluns. All the designs have been fabricated on LCP-based stack-ups. As such, they can be implemented as embedded circuits in a substrate topology, with the ICs being mounted on the top.

Narrow-band baluns have also been realized using lumped elements. Using just two inductors and capacitors, these baluns provide sufficient performance in a narrow band but allows for a reduction in size compared to transmission line baluns, especially at low frequencies (<3GHz). Further, with the use of high-K materials with high component density, the number of dielectric layers required to implement the balun can be reduced. As a proof-of-concept device, a narrow band balun operating at 2.4GHz has been designed as an IPD using a high-K organic stack-up. Due to the high component density,

the entire design was accomplished using a single dielectric layer, resulting in final packaged thickness of the IPD being only 0.5mm.

The design of baluns (and filter-baluns) in both substrates and IPD format paves the way for true 3D SOP integration. The compact substrate baluns are embedded in the package and leads to integration in the x-y plane, while the low-profile baluns are attached to the top of the substrate and provides for integration in the z direction as well. Keeping the total thickness of the substrate and IPD low results in low-profile modules that meet the thickness requirements of modern mobile applications.

CHAPTER 3

DESIGN OF FILTER-BALUN NETWORKS

In a receiver, the signal coming in from the antenna is single-ended in nature but the active circuitry (beginning with the LNA) is usually differential (Figure 3.1). The single-ended signal is filtered using a band-pass filter, and then converted to differential mode using a balun. With SOP-based implementation, it is useful to use a circuit embedded in the substrate that combines functionality of both a balun and a filter.

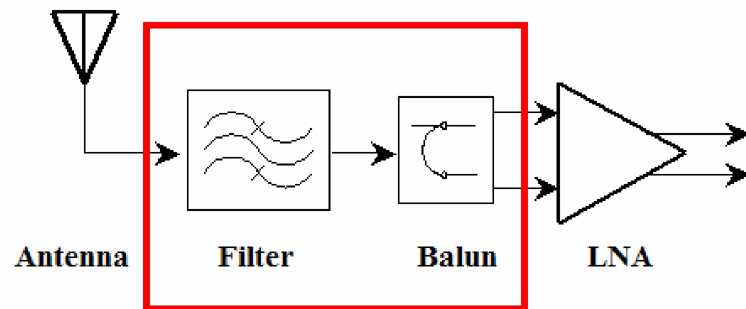


Figure 3.1. Functional block diagram of a receiver showing the filter and balun.

Any single-ended circuit can be made into a balanced network (with differential inputs and differential outputs) using network theory [68]. Balanced band-pass filters can also be designed in this fashion. However, this technique also results in an increase in the number of components. It leads to doubling of the capacitance values required in the series path [68], which can lead to large device sizes in embedded circuits where the

device size is directly proportional to the capacitance or inductance value required. Lattice filters have also been used in the past to achieve balanced filter topologies ([69]-[70]).

Although they provide both frequency selectivity and differential outputs, both these approaches require additional matching circuits for single-ended to differential conversion at the input port. Two alternate approaches are adding frequency selectivity to existing balun circuits and cascading a balun with a band-pass filter.

The rest of the chapter is organized as follows: Section 3.1 examines the possibility of designing filter-baluns by the use of resonators in baluns. Section 3.2 covers the design of filter-baluns by cascading a band-pass filter with a balun. The design has been verified by fabricating and measuring test-devices on an LCP-based substrate. Finally, Section 3.3 summarizes the results.

3.1. Baluns with Frequency Rejection

The use of resonators to reject unwanted frequencies is a well-known technique in microwave design. Adding frequency selectivity to the functionality of the baluns can potentially result in a filter.

Consider Figure 3.2, showing the two-port lumped-element model of a capacitor. It consists of a capacitor C in series with a resistor R_S (to model the conductor loss) and in

parallel with a resistor R_p (to model the dielectric loss). C1, C2, L1 and L2 represent the parasitic capacitances and inductances.

Neglecting the losses (R_s and R_p) and the parasitic capacitances, the capacitor can therefore be modeled as a series LC resonant circuit, with the resonant frequency given by

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{3.1}$$

In (3.1), L is the sum of L1 and L2 inductances.

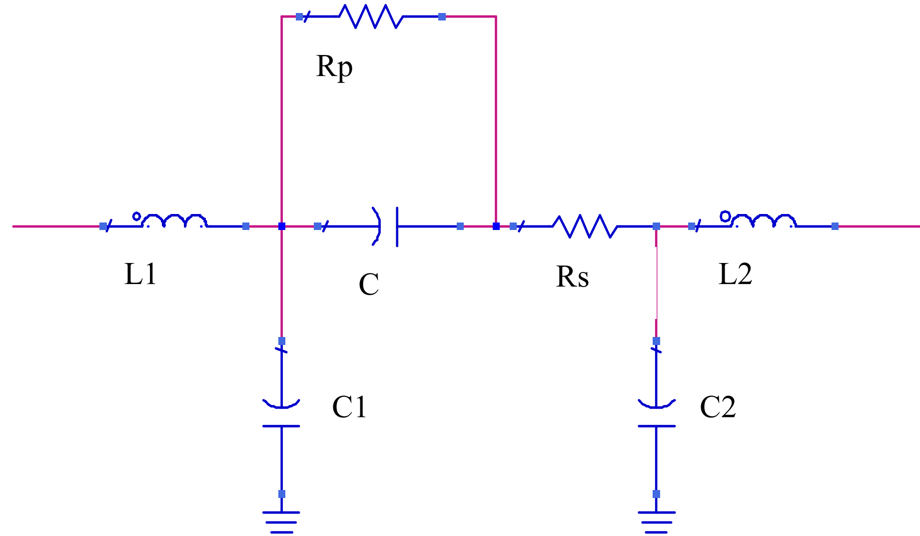


Figure 3.2. Lumped-element model of a capacitor.

At f_{res}, the inductive and capacitive part of the reactance cancels each other, creating a short circuit. A capacitor connected to ground will thus act like a notch filter, shorting all incoming signals at f_{res} to ground.

As will be shown in Chapter 4, an inductor also has parasitic capacitance. Unlike capacitors, the inductor behaves as an open circuit at its resonant frequency. If connected in series, it will block all incoming signals at its resonant frequency.

Additional inductance (or capacitance) can be added to capacitors (or inductors) to make them resonant at any frequency of interest. Although not very feasible in discrete circuits (due to the variation of the discrete elements), this is a very useful proposition for frequency rejection when the lumped elements are embedded in the package. By controlling the resonant frequencies of the lumped elements, it should be possible to add some degree of frequency selectivity to the baluns.

As an example, Figure 3.3 shows a 50Ω-20Ω impedance matching network designed for operation at 2.4GHz. The circuit consists of a T-network formed by two inductors and a capacitor. By designing the capacitor such that its self resonant frequency lies at 4.8GHz (the harmonic of 2.4GHz), it is possible to achieve impedance matching as well as harmonic rejection, without the use of any extra components.

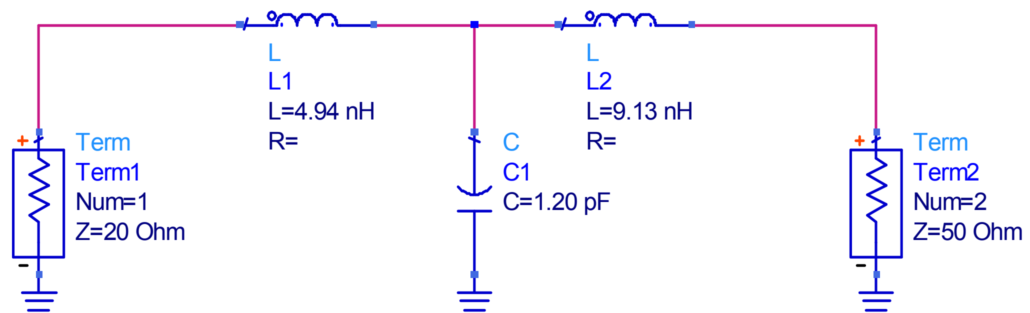
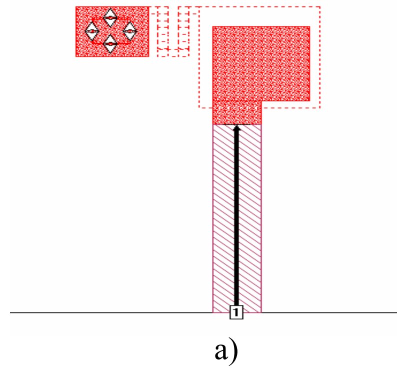


Figure 3.3. Matching network schematic.



a)

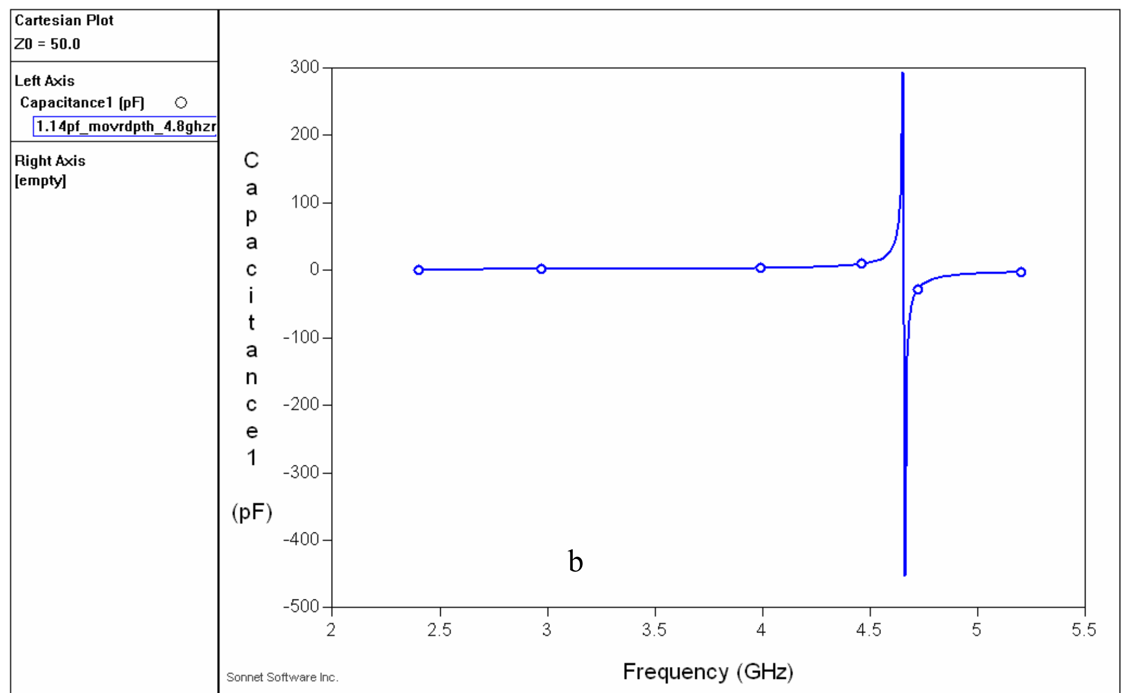


Figure 3.4. a) 1.2pF capacitor layout, and **b)** simulated response.

Figure 3.4a shows the layout of a 1.2pF one-port parallel-plate capacitor, and Figure 3.4b shows the variation in capacitance with frequency, including a resonance at 4.6Hz. Figure 3.5 shows a comparison of S21 for the matching circuit using the ideal 1.2pF capacitor and the capacitor of Figure 3.4. As can be observed, the in-band response

(about 2.4GHz) remains the same for both circuits. But S21 for the circuit using the capacitor with resonance at 4.8GHz shows a sharp notch at the second harmonic, providing the necessary

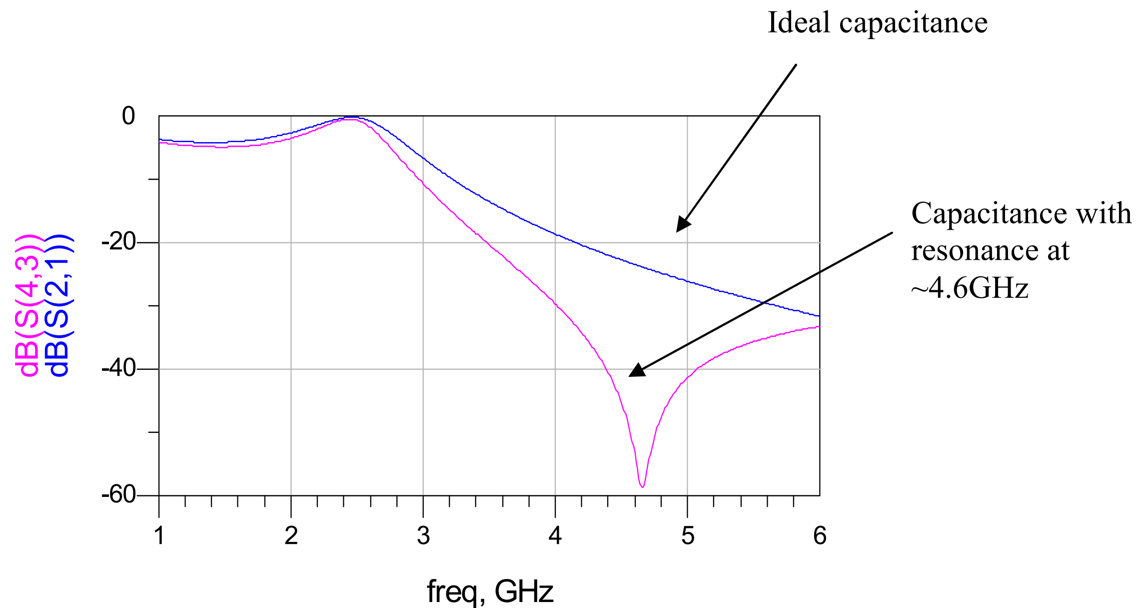


Figure 3.5. Simulated response of the matching network, with without the capacitor resonance

Figure 3.6 shows the schematic of a lattice balun of the type described in the previous section. For operation at 2.44GHz and R_{source} and R_{load} of 50Ω and 100Ω respectively, the values of capacitance and inductance required are 0.92pF and 4.6nH respectively. By replacing each inductor with a parallel combination of 3.23nH and 0.4pF, it is possible to obtain an equivalent inductance of 4.6nH at 2.44GHz, along with a resonance at 4.4GHz. Similarly, by replacing each capacitance with a series combination

of 2.7nH and 0.57pF, it is possible to obtain an equivalent capacitance of 0.92pF at 2.44GHz along with a resonance at 4GHz.

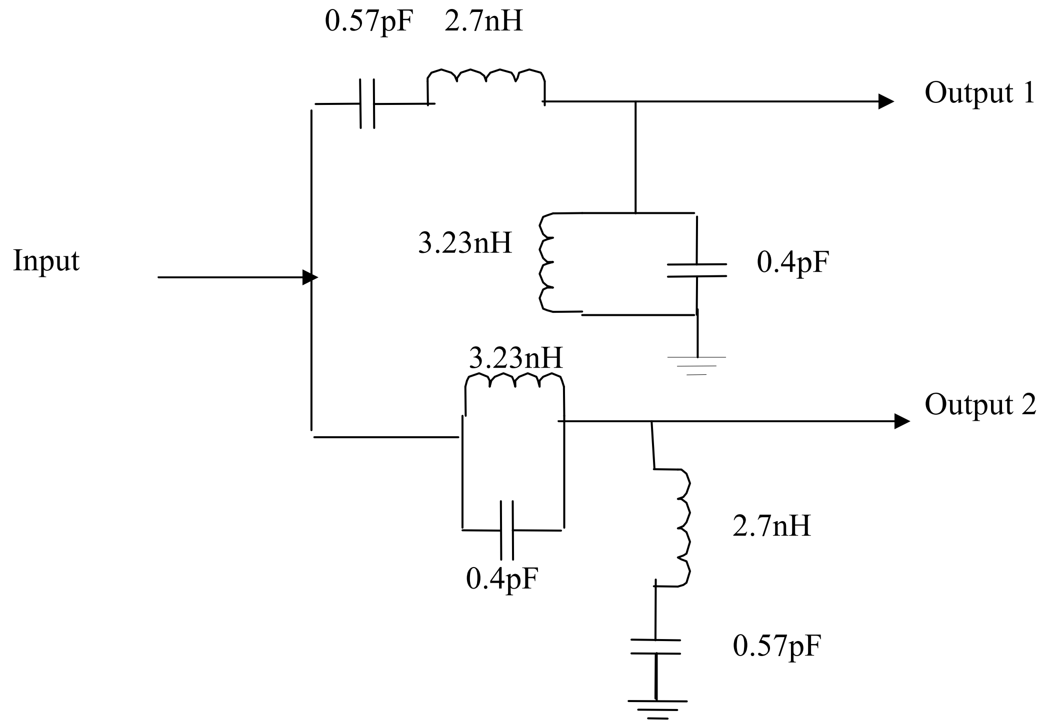


Figure 3.6. Lattice balun with inductors and capacitors replaced with resonators.

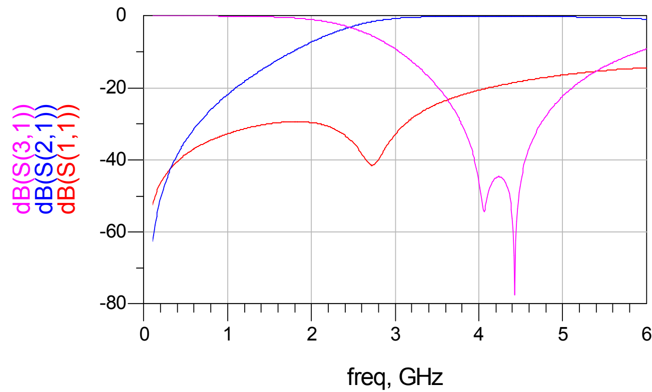


Figure 3.7. Simulated response of the balun.

Figure 3.7 shows the simulated response of the balun. S31 is the response of the low-pass arm, and exhibits notches at approximately 4 and 4.5GHz on account of the resonating inductors and capacitors. However, the high-pass arm shows no rejection at all. The topology of the circuit (the capacitor is connected in series and the inductor is connected in shunt) creates limitations in the use of resonators for frequency rejection.

The Marchand balun by its very nature has a band-pass behavior. The coupled line segments prevents the transmission of signals at low frequencies, while the transmission line behavior causes the signal transmission to fall of after the resonant frequency of the coupled lines. Implementation of the lumped elements in the modified Marchand balun using resonators allows transmission zeroes in the transfer function of the balun, leading to sharper roll-offs for the frequency response.

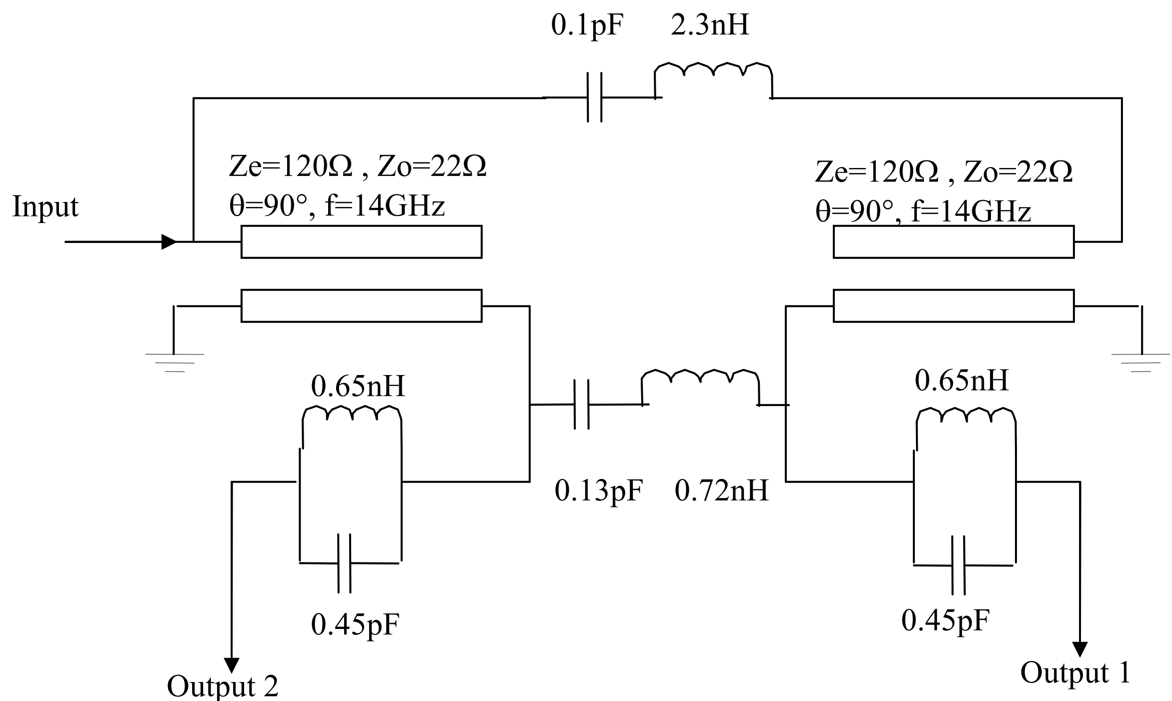


Figure 3.8. Modified Marchand balun for operation in the 5-6GHz, with resonators for frequency selection.

Figure 3.8 shows a modified Marchand balun designed for operation in the 5-6GHz frequency band. To increase high-frequency rejection, the lumped elements have been implemented using resonators. The capacitors have been replaced with two resonators (consisting of 0.72nH in series with 0.13pF and 2.3nH in series with 0.1pF) to provide transmission zeroes at ~16.5GHz and ~10.5GHz. The series inductors at the output have been replaced with 0.6nH and 0.45pF in parallel, to provide a block at 9.5GHz.

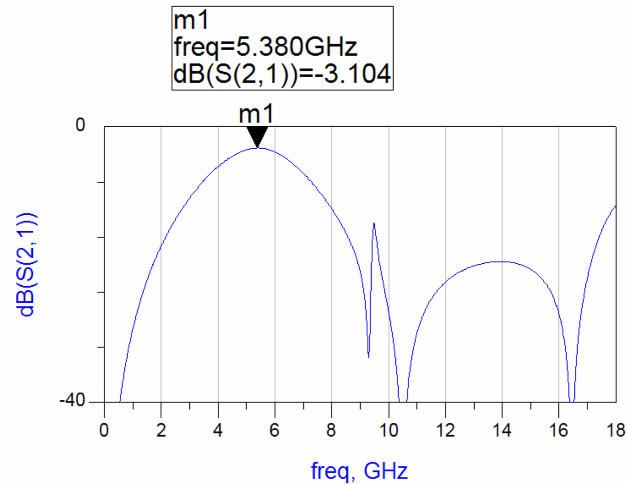


Figure 3.9. Simulated response (S21) of the balun.

Figure 3.9 shows the response of the balun. The resonators provide enough rejection at the second and third harmonics (10-12GHz and 15-18GHz) of the operational frequency. However, the rejection at frequencies lower than 5GHz (and especially in the 2.44GHz band) remains low.

It is thus clear that the use of resonators in existing balun designs to provide frequency rejection has limitations. Another option to implement the filter-baluns is to cascade a band-pass filter with a balun.

3.2. Cascaded Filter-Baluns

Figure 3.10 shows an implementation of a cascaded filter-balun. The filter (described in [26]) consists of capacitively coupled resonators, with a smaller capacitor connected between the input and output terminals connected to introduce two transmission zeroes (at 1.8GHz and 3GHz). The balun uses the lattice topology, and performs 50Ω-100Ω single-differential transformation. Both the filter and the balun have been designed for operation in the 2.4-2.5GHz band.

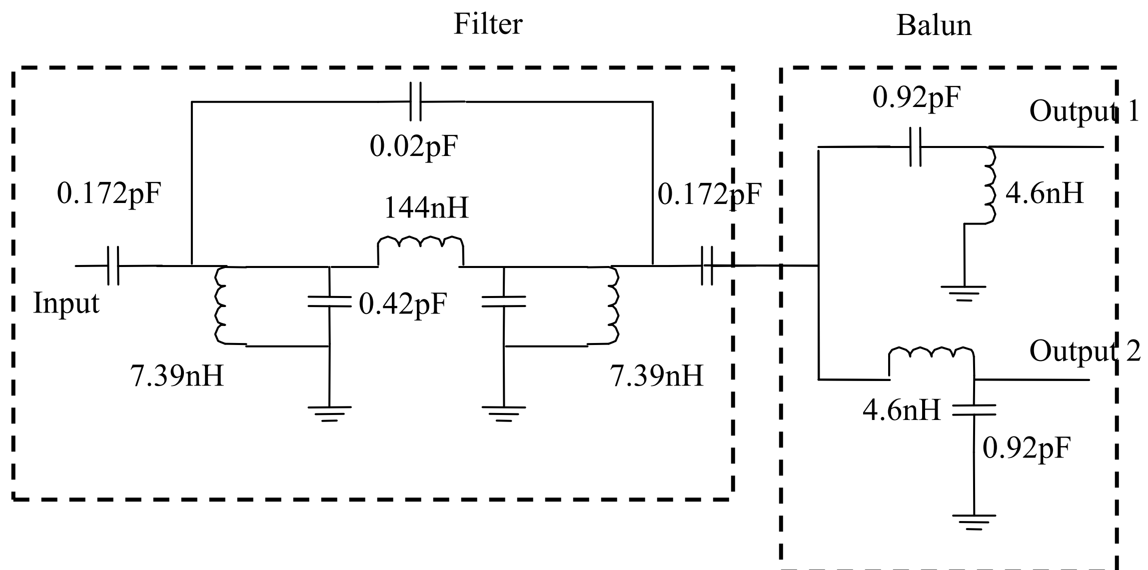


Figure 3.10. Filter-balun schematic.

The filter provides 20dB of rejection at the cell-phone frequency bands, while the balun has been optimized for low-loss in conjunction with the filter.

3.2.1. Implementation

An all-LCP stack-up was used to implement the device, primarily because of the high Qs required for the resonators in the filter (Figure 3.11). This resulted in a reduction in the component density compared to the high-K stack-up described in the previous section. To maintain the device size under control, the balun was implemented using all 6-metal layers offered by the technology – the capacitors were implemented on the LCP layer, and the inductors were implemented as meandering lines on metal layer 2 and 5.

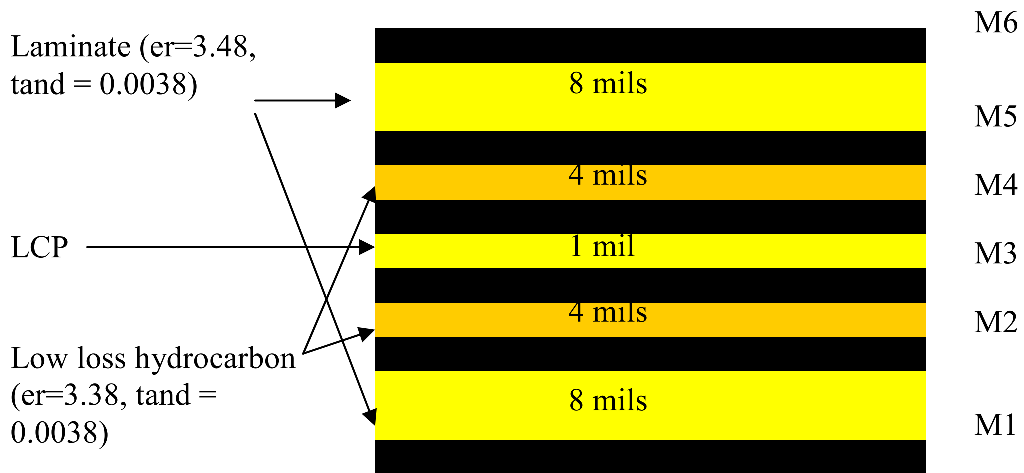


Figure 3.11. LCP stack-up used to implement the filter-baluns.

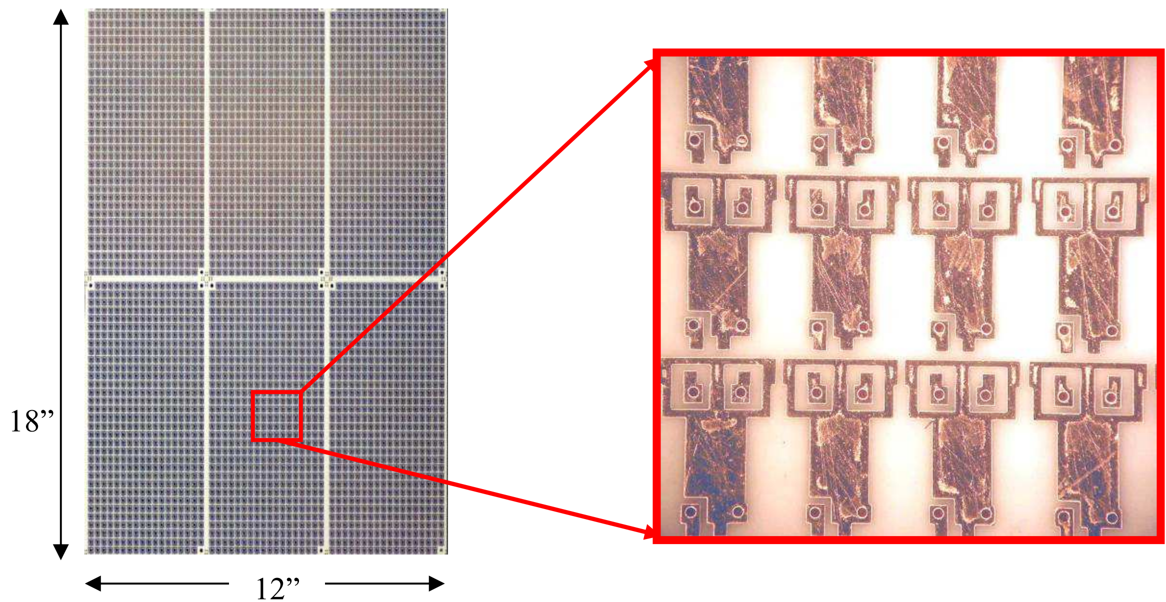


Figure 3.12. Photograph of the fabricated 12”x18” panel showing the devices laid out in six coupons, and close-up of the devices showing probe pads.

Figure 3.12 shows the photograph of the fabricated devices. After dicing off the probe pads, the devices measured 4mmx1.5mm, with a total thickness of 0.75mm. Figure 3.13 shows the measured S21 and S31 of the device, while Fig 3.14 shows the phase and amplitude imbalance. The filter provides a minimum rejection of 20dB across the cell phone bands (GSM, EGSM, PCS and DCS), while maintaining an insertion loss below 2dB. It is to be noted here that the filter itself had a loss of close to 1.7dB in [26]. By careful design of the balun to minimize return losses, it was possible to keep the total losses in the device to less than 2dB. Table 3.1 summarizes the performance of the device, along with a comparison with a commercially available LTCC filter-balun.

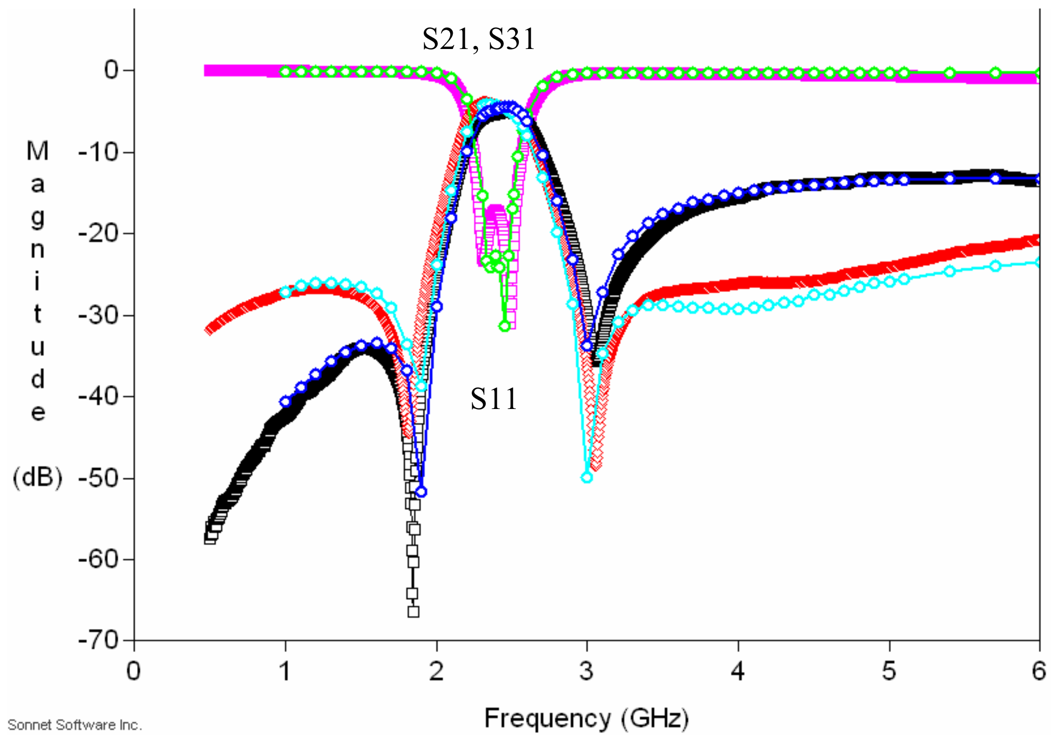


Figure 3.13. Measured and modeled values of S11, S21 and S31. Dotted line shows Sonnet simulations while continuous line shows the measured data.

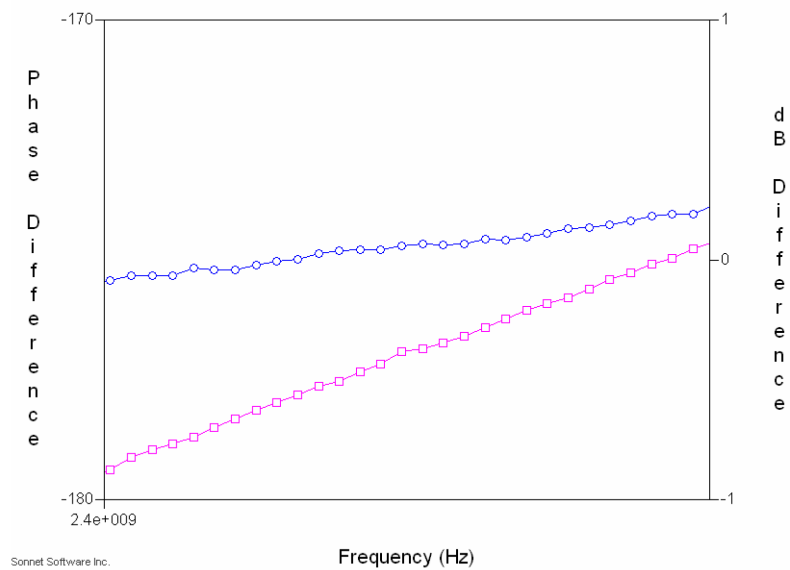


Figure 3.14. Measured amplitude and phase imbalance.

Table 3.1. Measured performance of the filter-balun, with a comparison with a commercially available LTCC filter-balun from Soshin.

Parameter	Soshin LTCC Filter-Balun	Organic Filter-Balun
Insertion Loss	2dB	2dB
Rejection	-	824-849MHz -27dB
	870-915MHz- 35dB	870-915MHz- 27dB
	1850-1910MHz- 30dB	1850-1910MHz- 30dB
	1920-1980MHz -20dB	1920-1980MHz -20dB
Phase Imbalance	180+-10°	180+-10°
Amplitude Imbalance	±1dB	±1dB
Size	$5mm^2$	$6mm^2$
Height	1.2mm	0.75mm

The fabricated device is larger in size compared to commercially available LTCC filter-baluns. However, it is only ~62% of the thickness of the LTCC device, paving the way for implementation as an embedded devices in the substrate. Further, by designing the balun and the filter in separate layers of a heterogenous stack-up (comprising of one LCP layer and one high-K dielectric layer), an all-organic filter balun with packaged size of 2.5mmx1.25mm can be easily implemented.

3.3. Summary

Lumped-element filter-baluns have been implemented by cascading a band-pass filter with a lattice balun. The fabricated device operates in 2.4GHz WLAN band and provides a minimum of 20dB of rejection across the cell-phone frequencies. This makes this suitable for use in a multiband environment, where cell-phone blockers can degrade the performance of the WLAN receiver.

CHAPTER 4

DESIGN OF LOW NOISE AMPLIFIERS USING EMBEDDED PASSIVES

The low noise amplifier is the first active device of any RF front-end architecture (Figure 4.1). Essential requirements of this amplifier circuit are reasonable gain, a good input impedance match, linearity and the lowest possible noise figure (NF). If the device is to be used in a portable device, the need for low power consumption also becomes important.

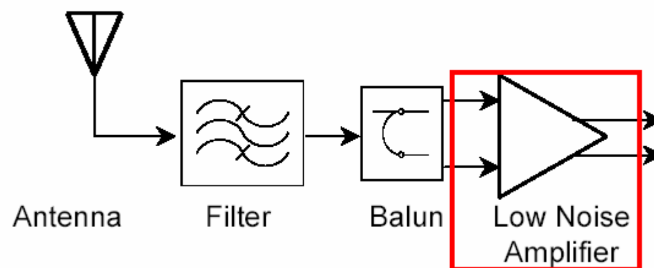


Figure 4.1. Functional block diagram of a receiver showing the LNA.

The noise factor (F) of an LNA is a measure of the amount of noise added by the circuit to the incoming signal, and is defined as the ratio of Signal-to-Noise Ratio (SNR) at the input of the device to the SNR at the output (4.1).

$$F = \frac{(SNR)_{in}}{(SNR)_{out}} = \frac{\overline{v_{ni}^2}}{\overline{v_{tx}^2}} \tag{4.1}$$

where $\overline{v_{ni}^2}$ is the total noise power at the output referred to the input, and $\overline{v_{tx}^2}$ is the thermal noise power produced by the source resistance (typically 50 Ω). The noise figure is F expressed in dB.

The classical LNA architecture consists of an active device with impedance transformation networks at the input and output (Fig 4.2). The NF is mainly affected by the noise characteristics of the transistor and the input impedance matching network. Generally, the source impedance required by the active device for minimum NF is different from the complex conjugate of the input impedance obtained looking into the base/gate of the device (the optimum impedance for maximum power transfer). This means that it is usually not possible to simultaneously achieve both maximum gain and minimum noise figure for an amplifier, and that some compromise has to be made. In addition to gain and NF, stability is also an important factor in amplifier design. This again requires careful choice of source and load impedances, so that the amplifier does not move into the unstable region of operation. The selection of the optimal source impedance Z_{opt} is achieved by plotting constant NF circles and constant gain circles along with stability circles on a Smith chart. The input impedance transformation network transforms the source impedance (typically 50Ω) to Z_{opt}. The output impedance transformation network transforms the impedance at the collector/drain of the active device to 50Ω for maximum power transfer.

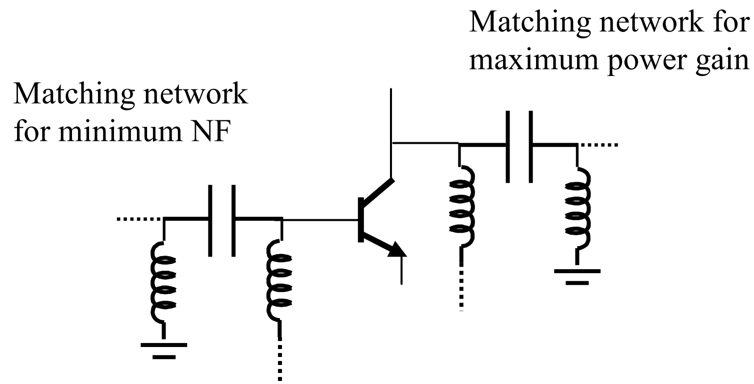


Fig 4.2. Classical LNA design, showing matching networks.

The cascode LNA architecture of Figure 4.3 has also been used widely for its low NF and high input - output isolation, particularly for single-chip solutions where the transistor parameters can be strictly controlled [10]. Table 4.1 shows examples of CMOS LNAs published over the last few years; none of them are completely integrated solutions and they all require external discrete passives for completing the circuit.

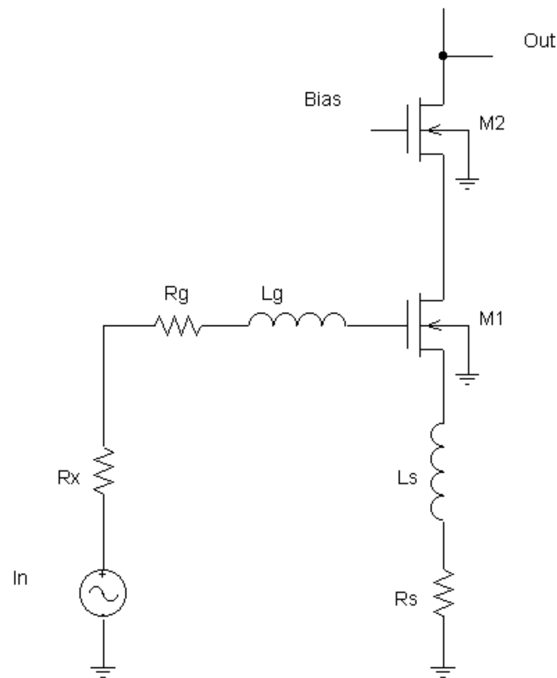


Figure 4.3. LNA with inductive degeneration. R_g and R_s are parasitic resistances of the inductors L_g and L_s. The bias circuitry has not been shown for simplicity's sake.

Table 4.1. Survey of past work done on CMOS LNAs for long-distance communication protocols.

Author	Frequency(GHz)	Technology	NF(dB)	Completely Integrated?
Shaeffer et al. [10]	1.5	0.6u CMOS	3.5	NO
Hayashi et al. [11]	0.9	0.35u CMOS	1.8	NO
Abou-Allem et al. [12]	1.9	0.5u CMOS	1.8	NO
Gramegna et al. [13]	0.9	0.35 RFCMOS	0.85	NO

4.1. Chip-Package Co-Design of CMOS LNAs

The design process for the inductively degenerated LNA consists of sweeping the NF with respect to transistor (M1) gate width. Using the RF CMOS model described in [71], the input impedance of the LNA can be calculated as

$$Z_{in} = R_g + R_s + R_{gate} + R_{ch} + \frac{g_m L_s}{C_{GS}} - jR_s g_m \sqrt{\frac{L_T}{C_{GS}}} + j\omega L_T - \frac{j}{\omega C_{GS}} \qquad (4.2)$$

where R_g and R_s are the parasitic resistances of the inductors at the gate and source respectively, R_{gate} is the resistance of the polysilicon gate, R_{ch} is the channel resistance, g_m is the transconductance, C_{GS} is the gate-source capacitance, ω is the angular frequency and L_T is the sum of inductances L_s and L_g. If the parasitic resistances (R_g, R_s and R_{gate}) can be ignored, the real part of the input impedance can be controlled by choosing appropriate values for L_s and can be set to equal the source resistance for impedance

match. The gate inductance is then chosen such that L_T resonates with C_{GS} at the operating frequency, thus canceling out all the imaginary terms and making the input impedance purely real at the frequency of operation.

Several papers have discussed optimization strategies for CMOS LNAs ([10], [72]). All of these design methodologies have assumed fixed Qs for the inductors. An SOP approach that provides embedded inductors in the package substrate allows the designer an extra design variable, namely, the Q of the inductors. Depending on their contribution to performance specifications like NF and gain, any or all of the three inductors in the LNA circuit can be implemented on-chip or embedded in the package. However, attaining a particular Q also comes with tradeoffs in size and layout. In order to incorporate these into the optimization methodology, it is necessary to derive F as a function of R_g and R_s.

The output current of the LNA (i_o) can be defined as

$$i_o = G_{mg}(v_i + v_{ng}) + G_{ms}v_{ns} + A_{ig}i_{ng} + A_{id}i_{nd} \tag{4.3}$$

where v_i is the input voltage, v_{ng} is the total noise voltage at the gate, v_{ns} is the total noise voltage at the source, and i_{ng} and i_{nd} are the gate and drain noise currents of the transistor M1. In the above equation, G_{mg}, G_{ms}, A_{ig} and A_{id} are the system gains associated with the different voltage and current sources respectively. Since the output current i_o is also given by

$$i_o = G_{mg}(v_i + v_{ni}) \tag{4.4}$$

(where v_{ni} is the total noise voltage in the FET referred to the input), combining equations (4.3) and (4.4) results in

$$v_{ni} = v_{ng} + \frac{G_{ms}}{G_{mg}} v_{ns} + \frac{A_{ig}}{G_{mg}} i_{ng} + \frac{A_{id}}{G_{mg}} i_{nd} \tag{4.5}$$

where $\overline{v_{ni}^2}$ is the total noise power at the output referred to the input, $\overline{v_{tx}^2}$ is the thermal noise power produced by the source resistance (typically 50 Ω) and SNR is the Signal-to-Noise Ratio. NF is F expressed in dB.

Including all the noise contributions of the FET and that of the parasitic resistances of the inductors, noise factor (F) can then be derived as [73]

$$\begin{aligned} F = 1 + \frac{R_g}{R_x} + \frac{R_{gate}}{R_x} + \frac{R_s}{R_x} + \frac{\beta \omega_0^2 C_{GS}^2 (\omega_0^2 L_T^2 + (R_x + R_g + R_{gate} + R_s)^2)}{5 R_x g_{do}} \\ + \frac{2c\omega_0^2 C_{GS}^2 (R_x + R_g + R_{gate} + R_{ch} + R_s)(R_x + R_g + R_{gate} + R_s)}{g_m Rx} \sqrt{\frac{\beta\gamma}{5}} \\ + \frac{\omega_0^2 C_{GS}^2 (R_x + R_g + R_{gate} + R_{ch} + R_s)^2}{g_m^2} \frac{\gamma g_{do}}{R_x} \end{aligned} \tag{4.6}$$

where R_x is the source resistance, which is typically 50Ω, β and γ are bias dependant noise parameters of the MOSFET and g_{do} is defined as the drain output conductance evaluated at Vds=0V. In (4.6), c is the correlation coefficient between the drain and gate noise currents of the FET.

Equation (4.6) shows that F is equally dependent on the parasitic resistances of both gate and source inductors (R_g and R_s). However, in practice, L_s is much smaller than L_g. Values of inductance required for L_s are typically less than 2nH, and this can be

implemented as an on-chip or bond-wire inductance whose parasitic resistance can be neglected. By careful layout, the resistance of the polysilicon gate can also be made very small [10]. However, depending on the frequency of operation, L_g can be as high as 35 nH. The parasitic resistance of L_g (R_g) is hence a very important contributor to the F of the LNA. As it is impossible to implement this inductor on-chip, an optimum solution is to embed it in the package.

4.1.1. Noise Analysis

Figure 4.4 shows the variation of *NF* with respect to transistor gate width (W), for different values of Q_g, for a 1.9 GHz CMOS LNA designed for the AMI 0.5µ process. As can be observed, there exists an optimum gate width where the NF is minimum. However, this minimum NF shifts upwards as the value of Q_g is decreased. It is also important to note that this change is not a linear function of Q_g; *the improvement in NF with an improvement in* Q_g *is much more apparent at low values of* Q_g. Current design methodologies suggest designing circuits assuming infinite Q, and then using inductors with highest possible Q. This is not a very satisfying strategy, as there are always tradeoffs involved in achieving high Qs during inductor design. The non-linear variation of *NF* with Q_g provides the scope for an optimization methodology.

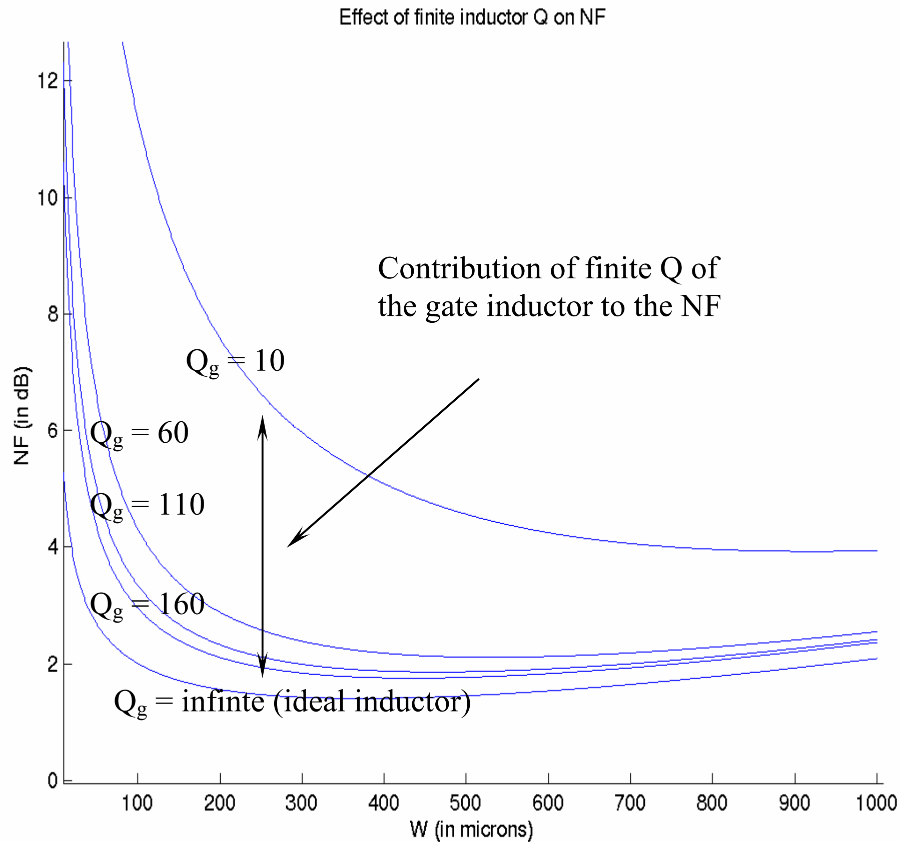


Figure 4.4. Variation of *NF* with transistor width (for different values of Q_g), for a 1.9 GHz CMOS LNA designed for the AMI 0.5µ process.

The Q of an inductor is a function of the signal loss within the device. The losses in an inductor consist of two components, namely, losses in the metal and losses in the substrate. It has been shown in [21] that the inductor can be optimized for maximum Q at the frequencies of interest (1-3 GHz). Under these conditions, conductor losses dominate the total loss (and hence the Q). The conductor losses can be reduced by increasing the conductor width (which reduces the series resistance), leading to an increase in size of the inductor, thus allowing for the tradeoff of larger size for higher Q.

By using embedded inductors in place of chip-inductors for L_g, the designer has control over the required unloaded Q for this inductor. However, due to the tradeoff with respect to size, using inductors with the maximum Q possible is not a good strategy and could lead to unnecessarily large sizes for the packaged LNA.

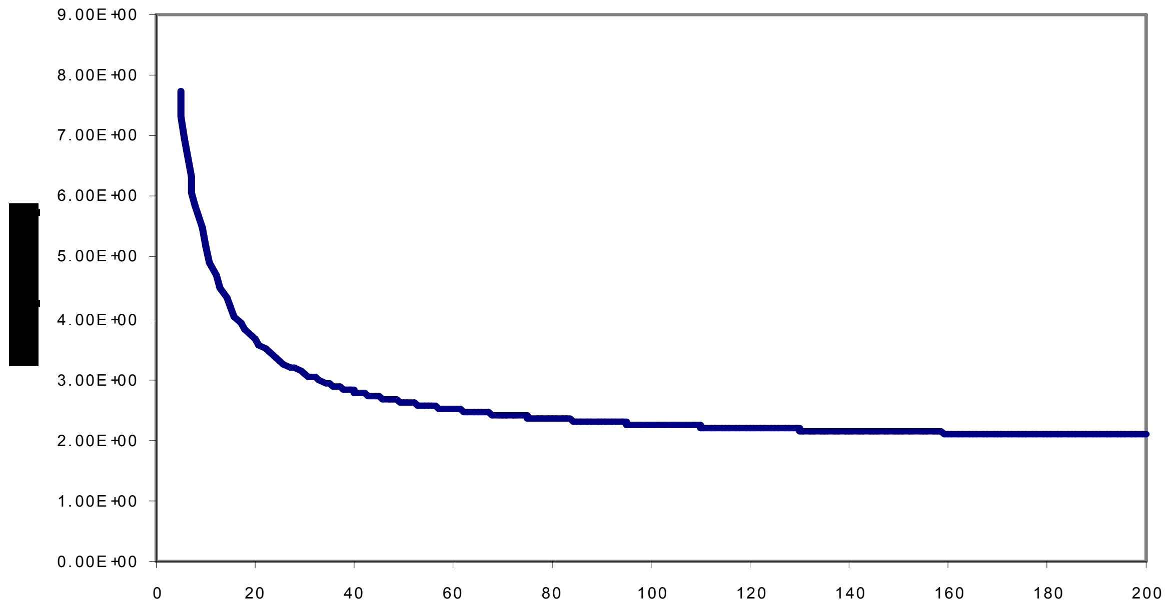


Figure 4.5. Variation of *NF* with Qg, for a 1.9 GHz CMOS LNA designed for the AMI 0.5µ process.

Equation (4.6) can be used to find the optimum Q_g, required for a particular NF. Figure 4.5 shows the variation of NF for the optimum transistor gate width. NF decreases rapidly for increasing Q_g at low values of Q_g, but the rate of change decreases at higher values of Q_g. *Hence, there is very little reduction in NF beyond a certain inductor Q.* Equation (4.6) and Figure 4.5 provides the minimum tolerable inductor Q required for satisfying the sensitivity requirements of a particular circuit. For protocols like Bluetooth and WLAN where the NF requirements are comparatively relaxed, even a Q of 25 is

sufficient to achieve a NF < 3.5 dB. Higher Qs (60-80) are required to meet the specs of long distance communication protocols like GSM and WCDMA.

4.1.2. Inductor Optimization

Lumped model equivalents for 1-port inductors fabricated using the organic process are shown in Figure 4.6. The series inductance, Ls, and the series resistance, Rs, represent the inductance and resistance of the inductor and under-routings respectively. The overlap between the inductor and the underpass allows direct capacitive coupling between the two terminals of the inductor. This feed-through path is represented by the series capacitance Cs. Components Cp and Rp capture the shunt capacitance and conductance between the inductor and the ground reference.

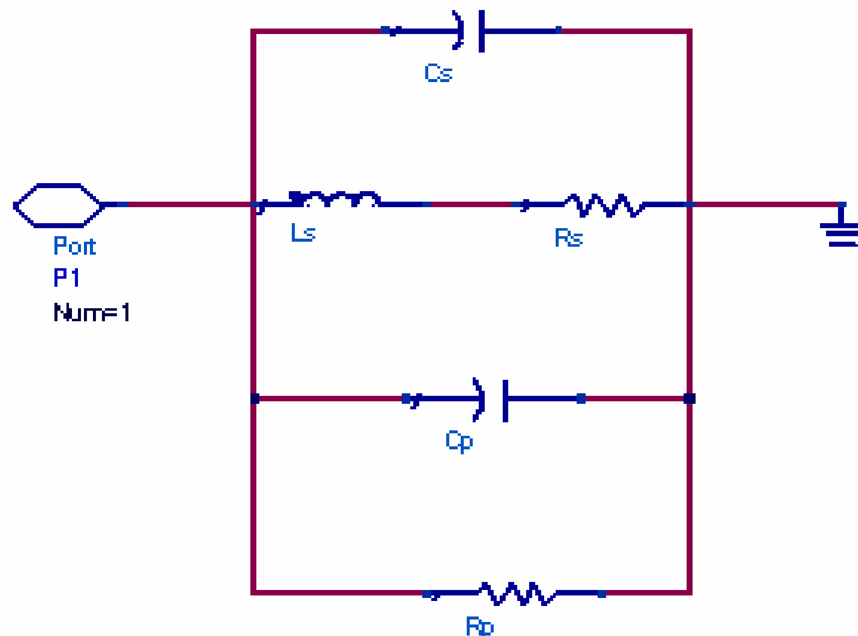


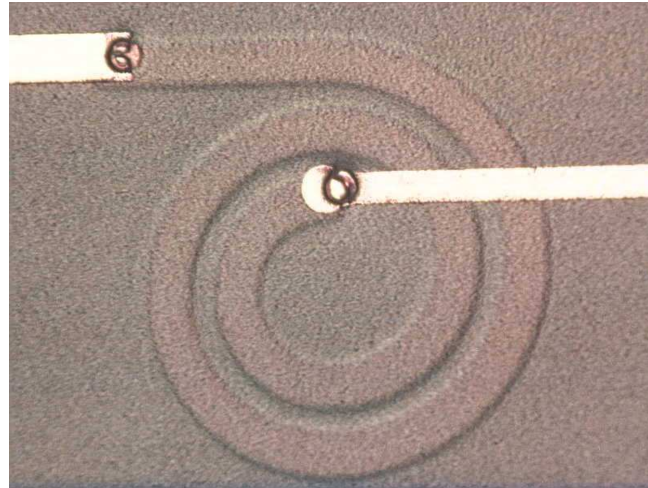
Figure 4.6. Inductor lumped-element model.

The variation in Q for two inductors with the same topology and inductance but different areas can be explained based on the model of Figure 4.6 - the smaller inductor has larger series resistance and smaller parallel resistance compared to the larger inductor, and this results in a lower value of Q for the smaller inductor. An inductor can be made smaller by increasing its proximity to the reference ground. However, this directly decreases the inductance per unit length due to the negative mutual inductance with the ground plane. Thus, there is an increase in series resistance for a smaller inductor due to the increase in the length required to achieve the same inductance compared to a larger inductor.

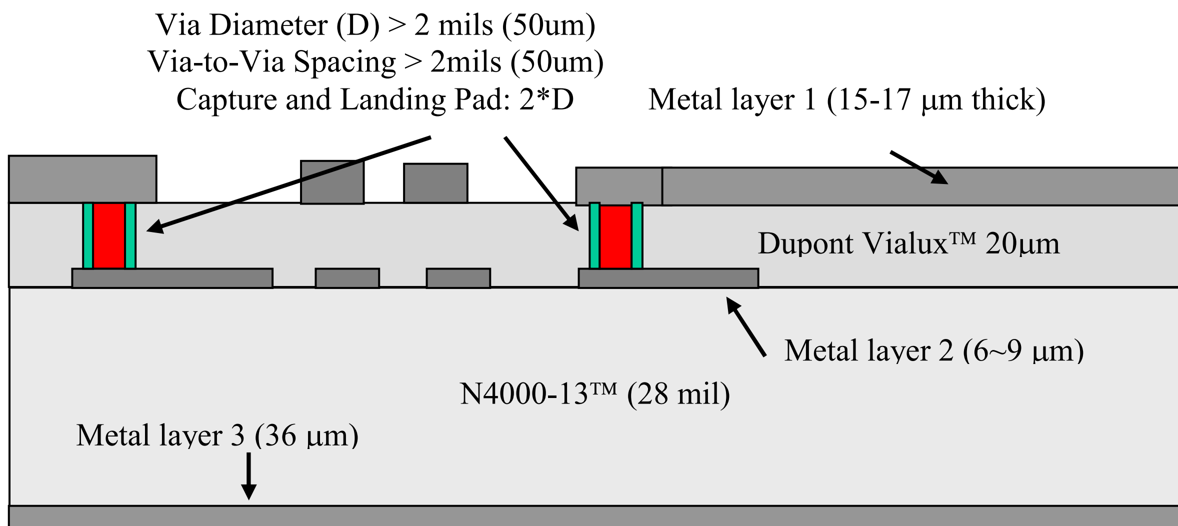
Figure 4.7a shows photograph of a spiral inductor fabricated on a 3-metal-layer organic substrate. The substrate consists of a low-cost dielectric Dupont Vialux™ (ε_r=3.4, tanδ=0.015 at 1GHz) laminated on to a conventional 28 mil core made of N4000-13™ (ε_r=3.9, tanδ=0.008 at 2.05GHz). The 1st metal layer thickness was limited to half the laminate layer thickness of 25um for ensuring a uniform dielectric layer thickness. The top metal layer was restricted to 15~17um to ensure uniform metal thickness. Figure 4.7b shows the cross-section of the substrate.

The CPW ground ring around the inductor is not been shown in the figure. There are several design variables for this inductor topology, namely the inner diameter, distance between the signal trace and the CPW ground, trace width, spacing between traces and number of turns. As an example to demonstrate the variation of Q with inductor area, three single-turn inductors were designed for the same inductance (~7.8nH) value. Table 4.2 shows the area and Q (measured at 1.83 GHz) for these inductors. As

can be observed, for a given topology (inductor shape and number of turns), there is an increase in Q with increase in device area.



a)



b)

Figure 4.7. a) Photograph of the fabricated inductor (the CPW ground ring around the inductor is not shown) **b)** Cross-section of the substrate.

Table 4.2: Variation of inductor Q with area.

Inductance (nH)	Q	Area (mm^2)
7.81	48.81	14.747
7.82	70.897	17.743
7.81	85.52	18.92

Figure 4.8 shows the variation of inductor area and NF with Q_g, for an LNA designed using these inductors. The dotted line represents the specification for NF, which in this case was 2.5 dB. The NF vs. Q_g curve shows that the minimum inductor Q required to meet this specification is 64. The Area vs. Q_g curve is then used to determine the minimum size for the inductance that provide this Q (which in this case was ~17 mm^2).

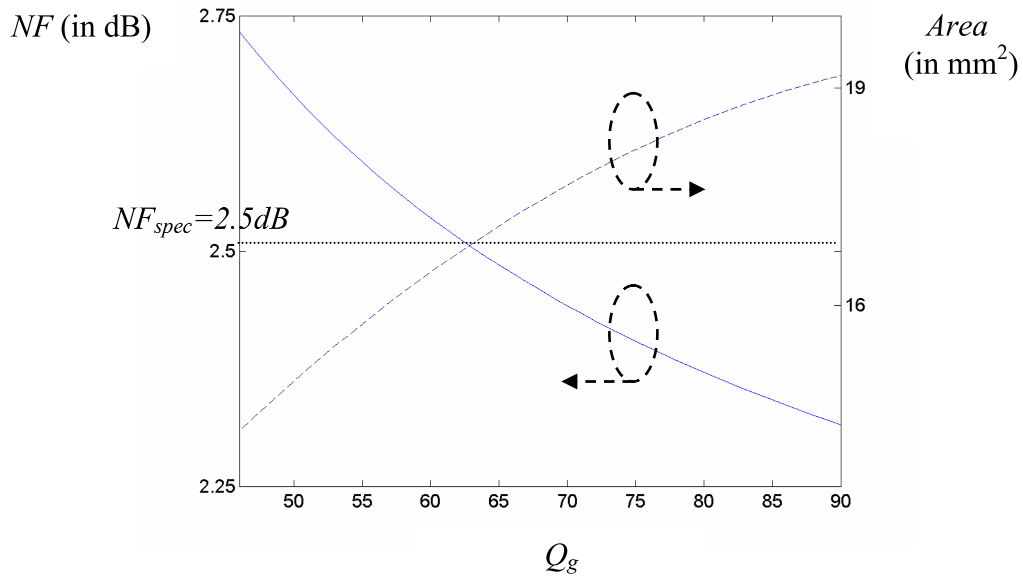


Figure 4.8. Variation of inductor area and *NF* with Q_g.

As an example of the chip-package co-design methodology discussed so far, an LNA for GSM applications was designed for AMI's 0.5µ CMOS technology, with a standard source resistance of 50Ω and an operating frequency of 1.9 GHz, leading to inductance values of 9 nH and 1.2 nH for L_g and L_s respectively. The parameter L_s was small enough to be implemented on-chip; however, L_g was too high to be implemented on-chip without a drastic increase in the NF of the circuit. Plotting the NF of the LNA versus its gate inductor Q, the NF decreases from about 5.2 dB to 2.1 dB as the Q of the gate inductor is increased from 10 to 200. However, on designing, fabricating and measuring different topologies for the gate inductance (on the organic substrate mentioned previously), it was found that its size increased from 9mm^2 for a Q of 110 to 28 mm^2 for a Q of 170. Since the NF of the LNA was not affected for an increase in Q_g beyond 70-90 and since size constraints limited the packaged device to an area of 3.5mm x 3.5mm, the inductor that provided optimum Q for a minimum size was chosen.

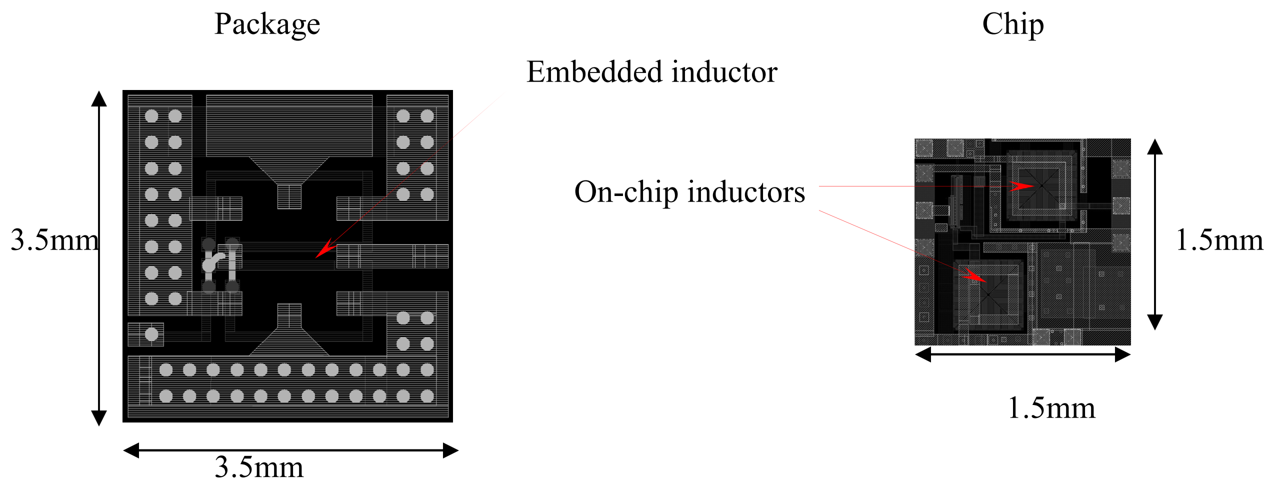
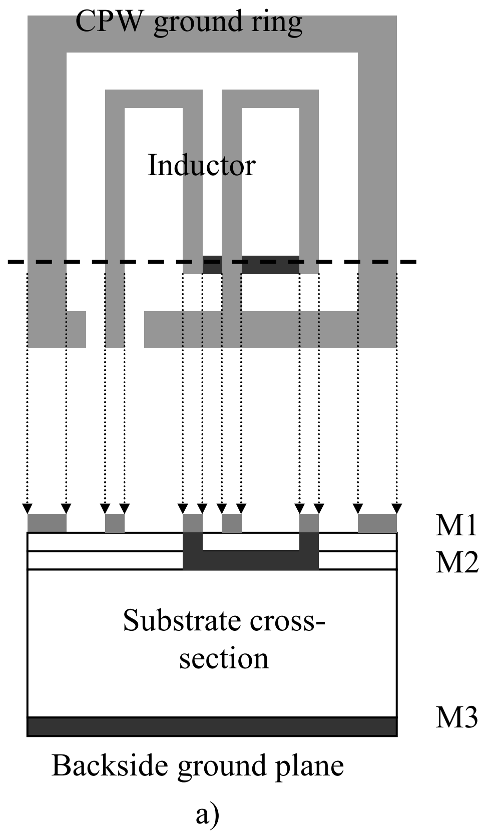
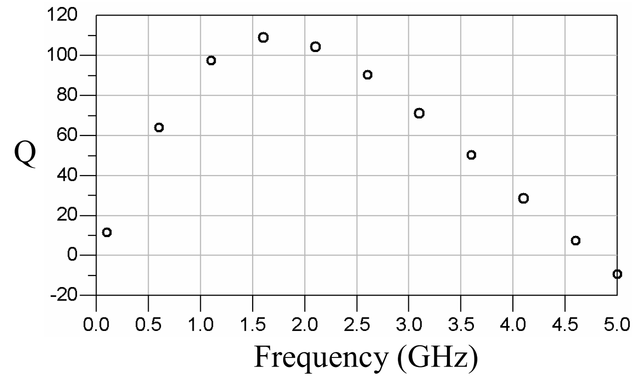


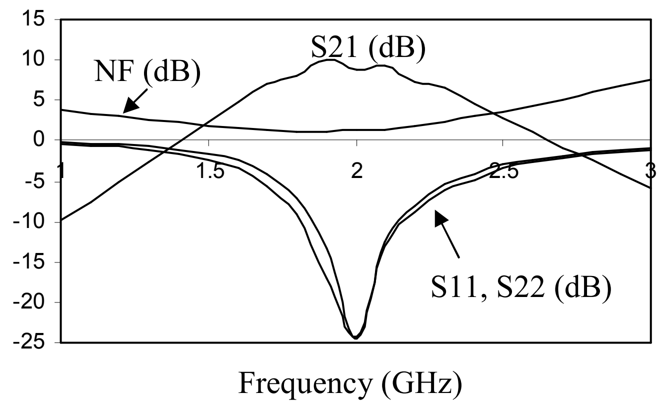
Figure 4.9. Chip and package layouts of the proposed integrated LNA.



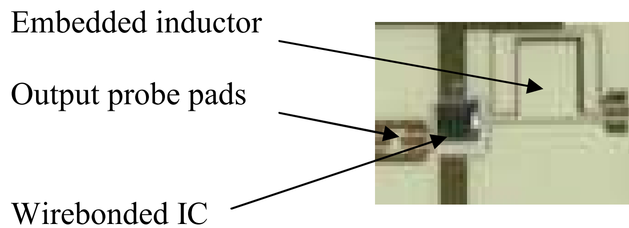
a)



b)



c)



d)

Figure 4.10. a) Layout and cross-section of the inductor used (9 nH CPW topology) with **b)** measured Q values, **c)** simulated gain and NF numbers, and **d)** photograph of an initial prototype showing the embedded inductor in the package and the wirebonded IC.

Figure 4.9 shows the package layout of the proposed LNA, along with simulated gain and NF numbers. The embedded inductor has a 2-loop CPW topology, occupies 9 mm^2 of area and has a Q of 110. The package uses a six metal layer organic packaging technology, with the inductor designed using metal layers 2 and 3. Metal layer 1 contains pads for chip attachment. The components of the equivalent circuit model (Figure 4.6) for this inductor were extracted from measurements, which translate to a series inductance (Ls) and resistance (Rs) of 7.4nH and 0.4Ω respectively, and a parallel resistance (Rp) and capacitance (Cs + Cp) of 27kΩ and 0.15pF respectively. Figure 4.10a shows the layout of the inductor and Figure 4.10b shows its measured variation in Q with frequency. It is important to note that this data has been obtained using inductors fabricated on lossy organic substrates. Figure 4.10d shows the photograph of an initial prototype showing the embedded inductor in the package and the wirebonded IC.

4.2. Multiple Embedded Passives: Analog-Analog Signal Coupling

With higher levels of system integration, multiple passives embedded in the package are necessary. For example, the phase noise of a voltage-controlled oscillator (VCO) is inversely proportional to the Q of the LC tank circuit ([74]). An SOP-based receiver could then contain embedded passives for both the LNA and VCO. As mentioned earlier, multiple embedded passives in the package leads to system-level issues like feedback and resonance, many of which are not apparent in an SOC

implementation. To study these, hybrid LNAs using a combination of discrete and embedded passives were designed for the packaging technology described in the previous section. The circuits were designed for use in the 2.1 GHz and 2.4 GHz frequency bands.

Figure 4.10 shows the schematic of the LNA, using a discrete HBFP-0420 dual emitter transistor in a SOT-343 package and the impedance transformation networks implemented using high-Q embedded inductors and capacitors. The transistor is biased in the common emitter configuration. The input and output of the transistor were matched to 50Ω by using L-C pi networks, which were embedded in the package. Though "L" networks are sufficient for a narrow-band impedance transformation, the goal was to study the layout issues and interaction between multiple embedded passives. A decision was therefore taken to maximize the number of embedded devices in the system. The output pi was designed for maximum power transfer, and thus performs impedance transformation from the complex conjugate of the collector impedance to 50Ω. The input pi was designed for minimum noise figure, and presents the Z_{opt} to the gate of the transistor. The pi networks were designed using Sonnet.

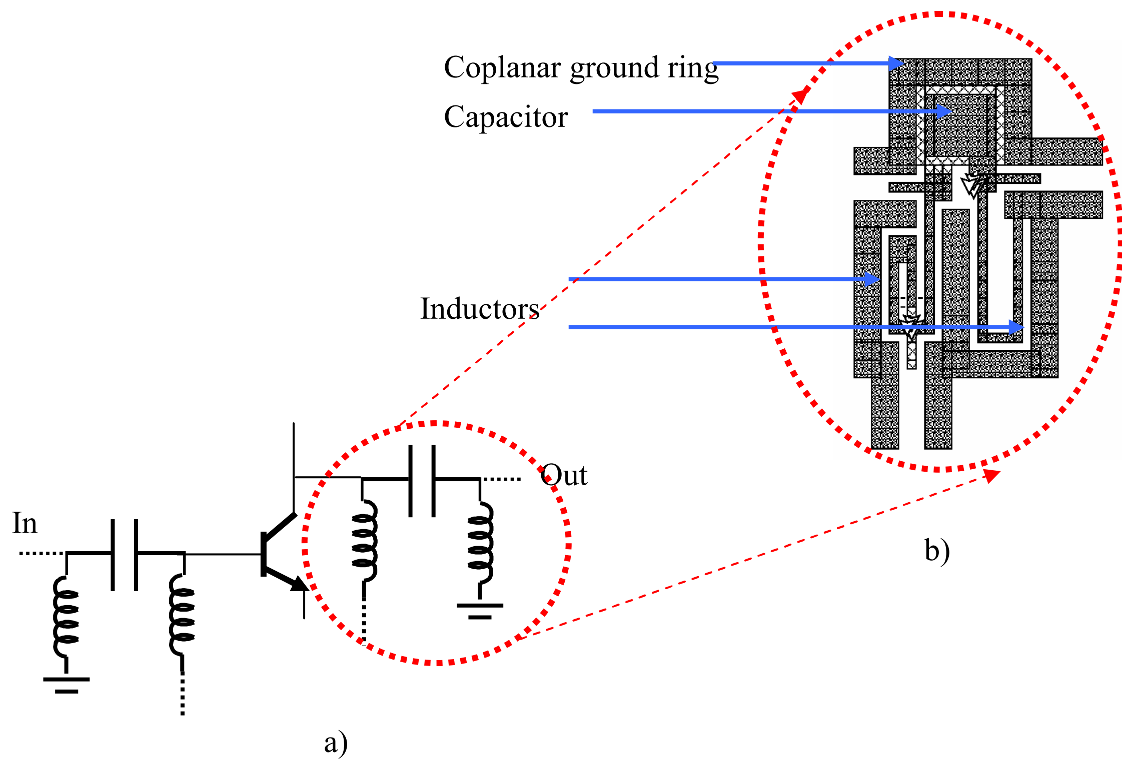
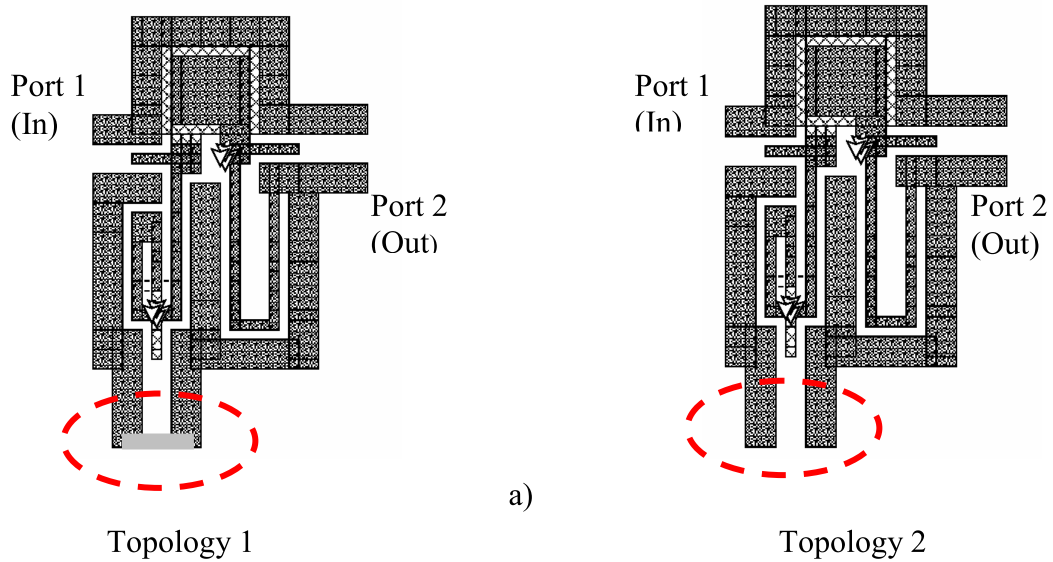


Figure 4.11. a) LNA with impedance transformation networks (pi networks) and implementation of the output pi using embedded passives. **b)** Actual layout of the output pi, showing the embedded inductors and capacitor.

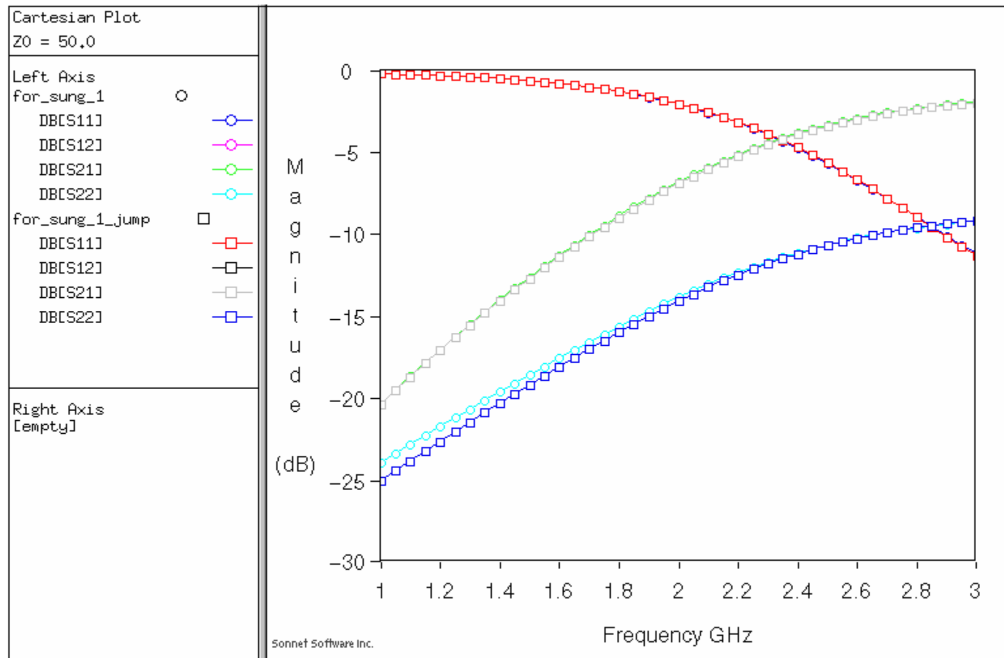
To study the effect of ground return current, pi's with different reference ground layouts were modeled and implemented, and their effect on the LNA performances was analyzed. Figure 4.11a shows two of the topologies used to implement the output pi and Figure 4.11b shows the Sonnet simulations for both the pi layouts. As can be observed (in Figure 4.11b), for the frequency band of interest, there is minimal difference in the S-parameters for the two topologies. However, Figure 4.12 shows the measured response of the amplifier circuits for the two pi topologies. The change in routing for Topology 2, caused the amplifier to move into the unstable region of operation, which could not have been predicted by simply simulating the pi's alone using full-wave electromagnetic

solvers. The instability is caused due to the influence of return currents on the transistor circuit.



a)

Topology 1 Topology 2



b)

Figure 4.12. **a)** Two reference ground layout topologies for the output pi. **b)** SONNET simulations for both layouts.

With layout of the reference ground resulting in such drastic changes in system performance, it becomes necessary to model its effect at the design stage, so that any system level instability problems can be identified and rectified. This involves the incorporation of the reference ground layout into the design and simulation methodology.

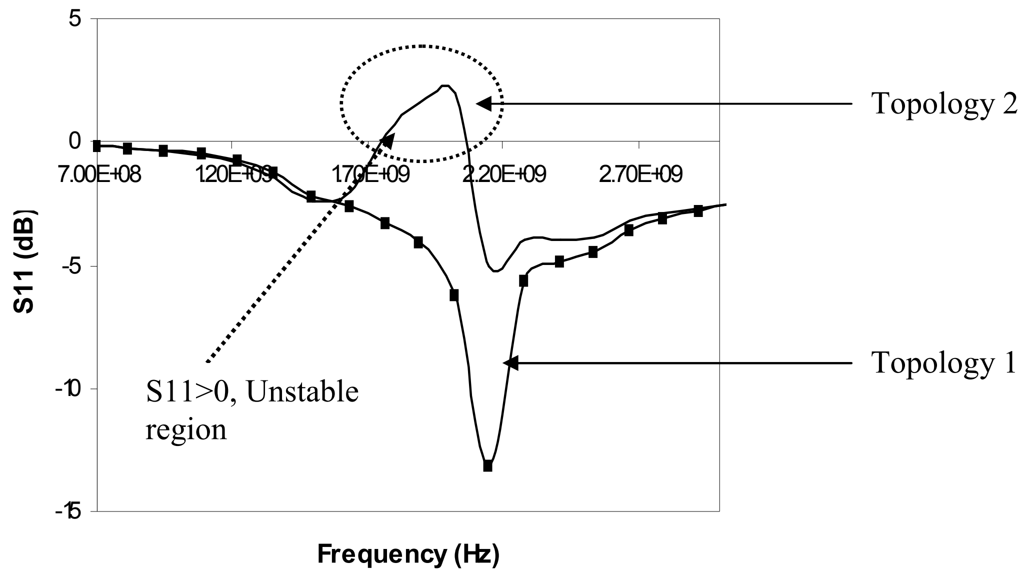
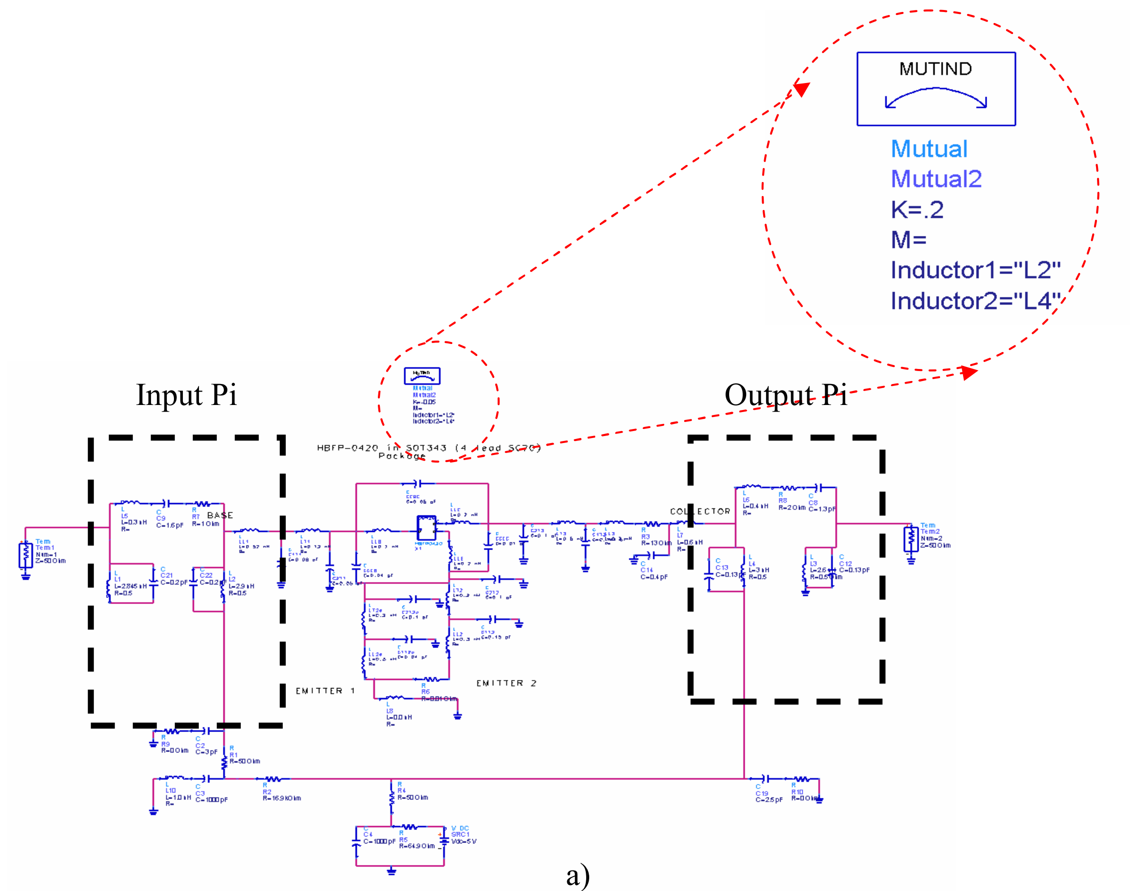


Figure 4.13. Measured S11 values for amplifiers using the two pi topologies of Figure 4.11a, showing the effect of the reference ground layout on LNA performance.

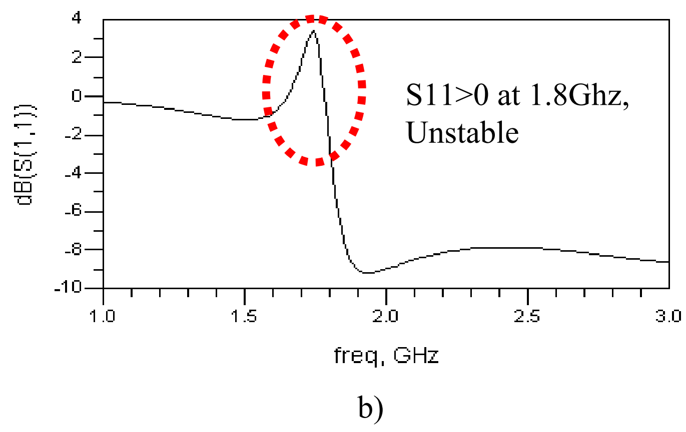
4.2.1. Modeling – Using Field Solvers

Field solvers like HFSS and Sonnet can be used to obtain an n-port S parameter file for the entire layout, which can then be used in a circuit based simulation tool like Agilent ADS. However, current modeling tools do have limitations when providing solutions for internal ports, especially for devices configured in a CPW topology. Instead, the effect of the reference ground layout can be modeled as a mutual inductance between

the inductors of the input and output pi's, with the coupling coefficient depending on both spatial orientation of the circuit components as well as the return current paths.



a)



b)

Figure 4.14. a) ADS circuit model for the LNA, along with the mutual inductance that was necessary to model the instability. **b)** Modeled (ADS) S11 results showing instability

Sonnet simulations of the complete layout for the unstable LNA showed considerable coupling between the input pi and one of the inductors of the output pi. The reference ground layout (and hence the return current path) for pi Topology 2 resulted in current crowding and signal coupling between the input and output pi's, leading to positive feedback and instability. The ratio of the current densities in the input and output pi's translated to a coupling coefficient of ~0.2, which, when used in ADS, modeled the instability (as shown in Figure 4.13). With re-routing of the excess current to prevent coupling (through the use of jumpers), it was possible to stabilize the amplifier. It is important to note that the Sonnet simulation of the LNA layout in Figure 4.14, now with better ground routing through the use of jumpers, exhibits a coupling coefficient of less than 0.05. Measured results for this LNA showed stable operation and a gain of 12dB at 2.1 GHz, proving that the instability in the earlier case was indeed because of return current routing.

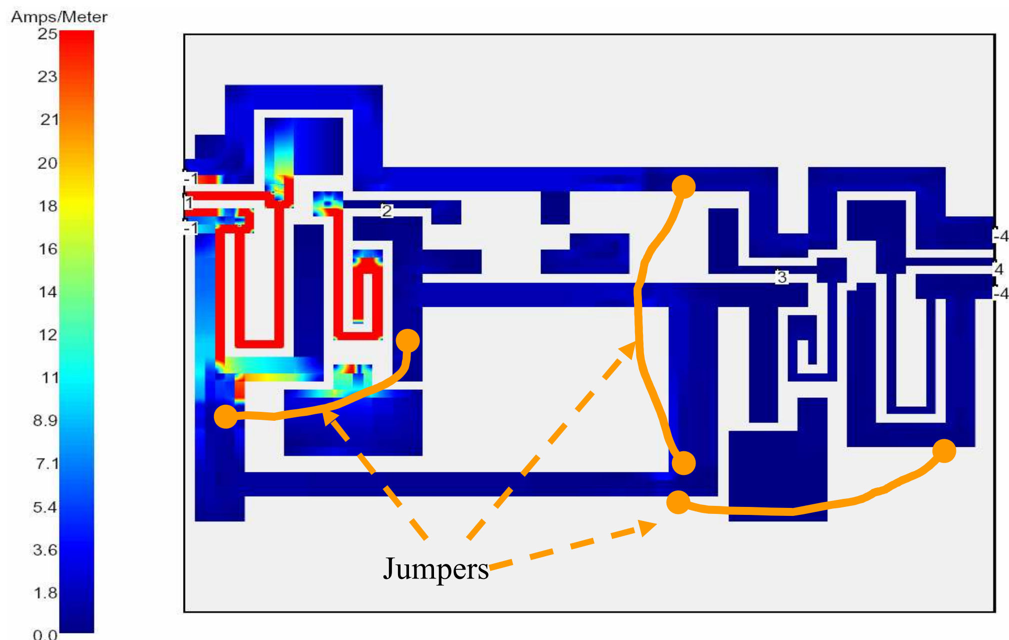


Figure 4.15. Sonnet simulations of the unstable LNA layout, with the use of jumpers for current re-routing.

4.2.2. Modeling – Using Transmission Lines

Electromagnetic solvers take long computation times, and this further increases as the number of ports is increased. This makes it difficult to use tools like Sonnet to model the mutual inductance in circuits at the design phase, when multiple simulations are required for optimizing the layout. For example, computing the coupling coefficient in the previous example at six frequencies using Sonnet required twelve minutes of simulation time on a Sunblade 1000™ workstation. To reduce computation time, a circuit based modeling methodology was also used, based on transmission line theory [75].

Modeling each pi network as an equivalent circuit consisting of two inductors and one capacitor makes it difficult to model the effect of the reference ground layout. Non-idealities in the ground distribution were therefore analyzed by segmenting the structure into various coupled line sections [73]. Figure 4.15 shows an example of the segmentation of two inductors (in CPW configuration) into several coupled line sections. Figure 4.15b shows the layout of the inductors unfolded into a cascaded structure of coupled lines. Each individual transmission line segment was defined by referencing it to the backside metallization of the packaging substrate. Figure 4.15c shows the cross-section of segment 4. The multilayer coupled line models (E.g. ML5CTL_V, ML1CTL_C etc.) in ADS were used to obtain the complete circuit model, with both signal and ground structures modeled as transmission line segments referenced to the backside metallization.

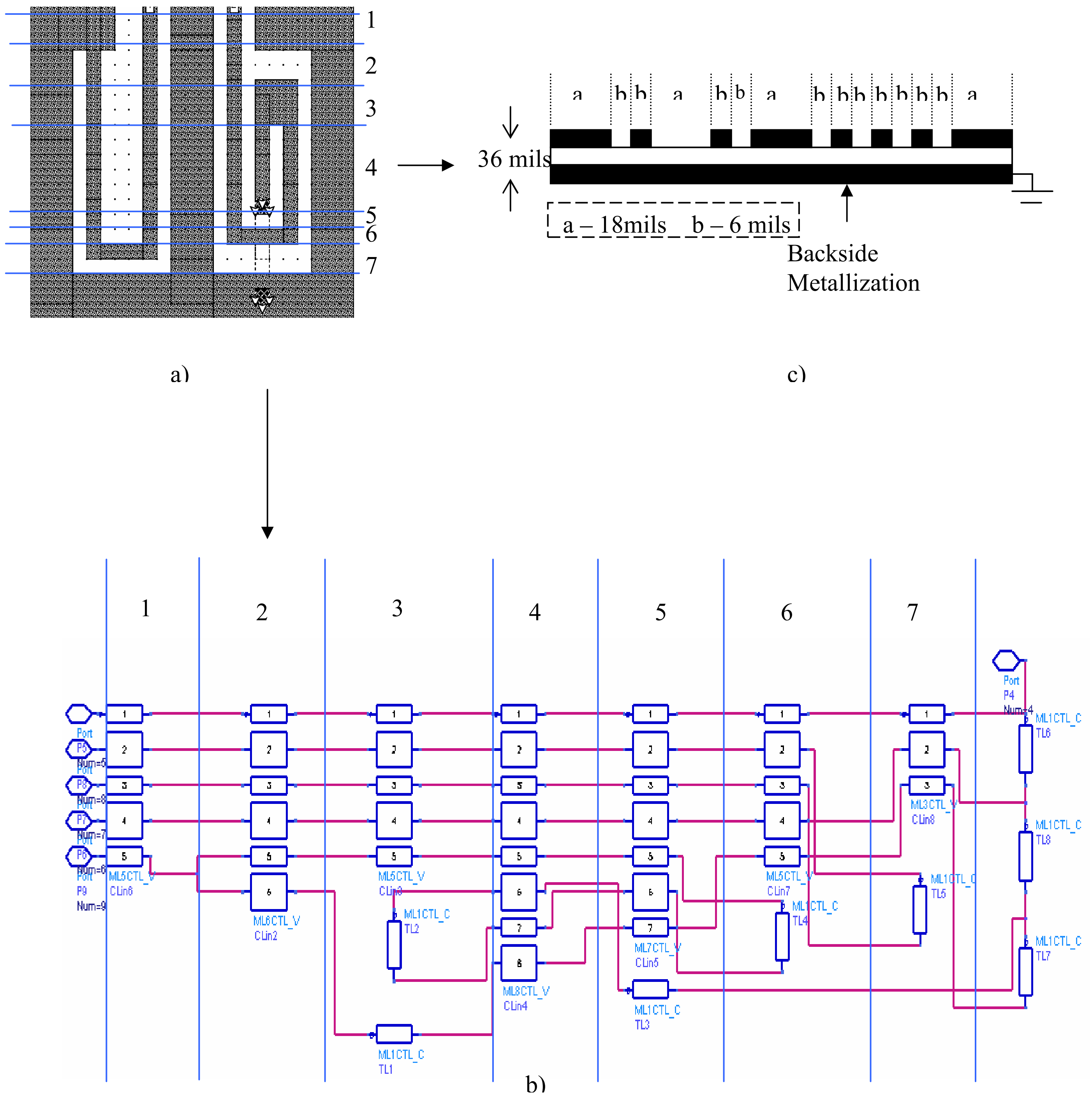


Figure 4.16. Coupled-line modeling of two inductors **a)** Layout and segmentation of the inductors **b)** ADS multilayer coupled line model of the inductors **c)** Cross-section of one of the segment (Segment 4).

Figure 4.16 shows the modeled instability (in ADS). The circuit-based model was able to predict the frequency of instability, at the same time reducing the computation time by an order of magnitude (80 seconds) as compared to modeling using Sonnet. It is to be noted here that this modeling methodology is valid only at low frequencies (<5 Ghz). The accuracy of coupled-line modeling decreases as the ratio of the wavelength to the thickness of the dielectric decreases. The effect of discontinuities is also much higher at high frequencies. In addition, the model was successfully applied only for predicting the frequency of instability, and not its amplitude.

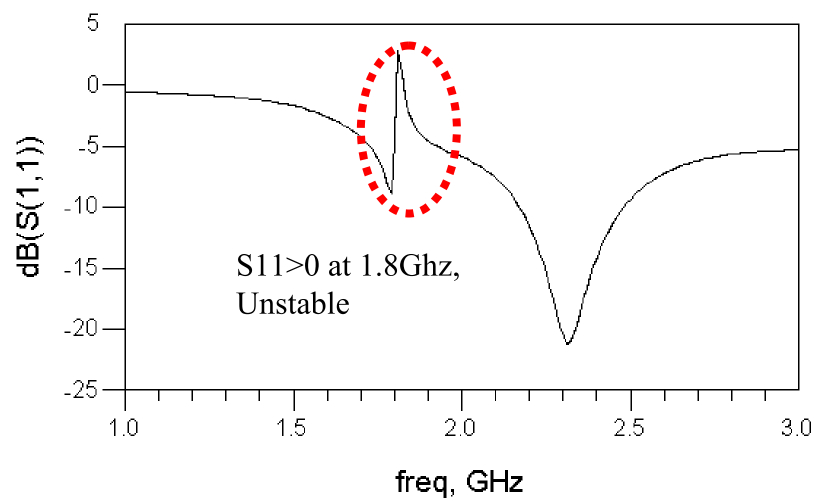
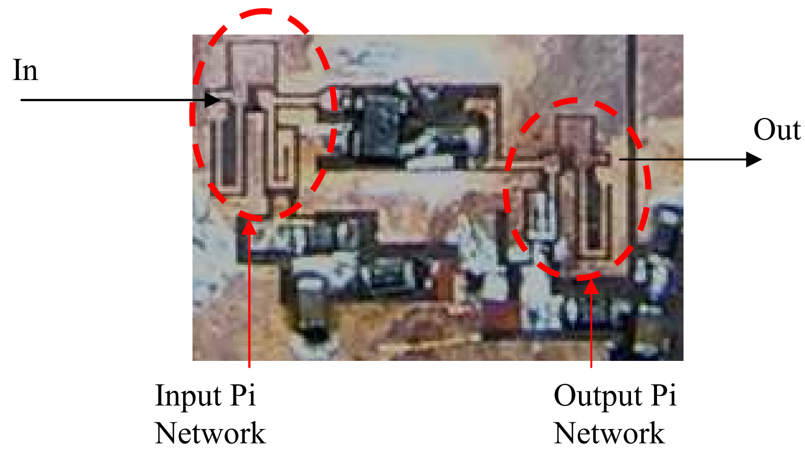
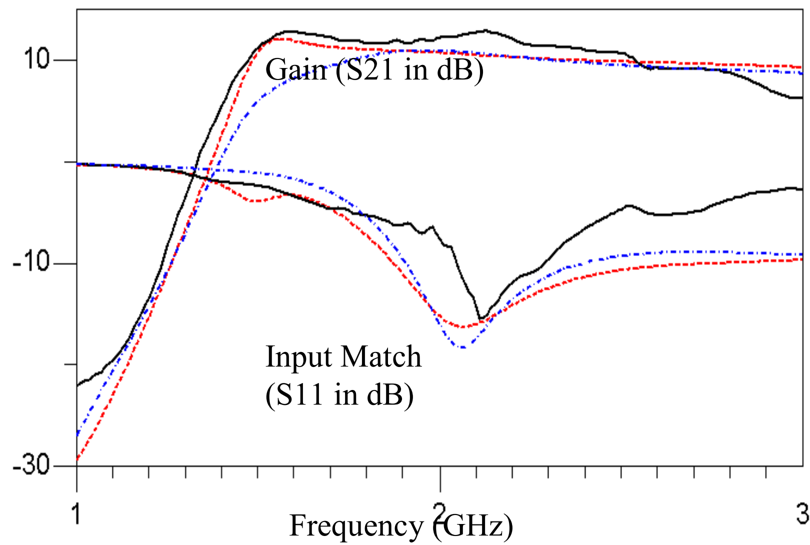


Figure 4.17. Modeled (ADS) S11 results showing instability

Figure 4.17a shows the layout and the photograph of one of the fabricated LNAs, and Figure 4.17b its measured gain (S_{21}) and impedance match (S_{11}) values. The amplifier shows a gain of 12.74 dB gain and an input match of –14.01 dB at 2.1GHz. Accounting for coupling between the input and output pi's, the plots show good correlation between measured and modeled data



a)



b)

——	Measurement
- - - -	Modeled Data (simulation in ADS; effect of return current modeled as mutual inductance, calculated using SONNET)
- · - · -	Modeled Data (simulation in ADS; effect of return current modeled using coupled line theory and transmission line network)

Figure 4.18. a) Photograph of the fabricated device. **b)** Modeled and measurement data.

To summarize, performance based design partitioning for an SOP-based CMOS LNA implementation has been completed. The NF of a cascode CMOS LNA has been derived as a function of the Q factors of its inductors. It has been shown that beyond a certain inductor Q, the NF becomes almost independent of Q. The SOP implication of this, i.e. the tradeoff of higher inductor size for higher Q, has been analyzed. In effect, the inductor Q has been used as a design variable, and has been incorporated into the LNA design methodology.

Further, the effect of analog-analog coupling in substrates with multiple embedded passives has been studied using an LNA as a test-vehicle A modeling approach to integrate system-level full-wave solvers into the design flow of integrated systems with active devices and multiple embedded passives has been proposed, and validated through measurements. A computationally efficient circuit based modeling strategy using transmission line theory has also been used to predict the effect of coupling between embedded passives in SOP based schemes.

CHAPTER 5

DIGITAL-ANALOG COUPLING IN MIXED-SIGNAL INTEGRATION

The previous chapter discussed the design of LNAs using high-Q passives embedded in the package. With integration into a mixed-signal system, the LNA also has to operate in an environment where high-speed digital circuits are placed in close physical proximity. The LNA is the most sensitive circuit in the entire RF sub-system, and hence is very susceptible to any external noise. RF signals at the input of these devices have very low power and large signals appearing in-band can move the active device to saturation, reducing its sensitivity. To prevent this, all radio architectures include filters and other narrow band circuits (Figure 1.2, Figure 1.3) between the antenna and the LNA, to prevent noise and blocker signals in the incoming spectrum from reaching the LNA. However, there are no systematic methods for filtering noise from the sources *within* a mixed-signal system. For e.g., digital noise can couple through the power supply and appear at the output of the LNA, where it can degrade the performance of the downstream circuits. For a mixed-signal integrated system with digital circuitry in close proximity to RF sub-systems, the study of noise coupling mechanisms and their suppression schemes thus become a critical design issue.

In [15], M. Xu et al. have described the study and experimental characterization of switching noise in a SOC-based mixed-signal system. The CMOS IC consisted of a

digital circuit emulator and an LNA. The noise produced by the digital switching circuits coupled into the LNA through the conductive silicon substrate, producing noise spikes at the LNA output at integral multiples of the switching frequency.

With the use of an SOP-based integration scheme with multiple chips for the RF and digital sub-systems, there is no conductive propagation of switching noise through the semiconductor substrate. However, SOP-based systems typically use power-ground planes to supply power to the various parts of the system. Phenomenon like ground bounce and simultaneous switching noise (SSN) (that have been well documented in the case of PWB system design [49]-[52]) thus become important factors in SOP-based mixed-signal design. An experimental study like the one described in [15] is required, to study the effect of digital noise coupling on an LNA from an SOP perspective.

Figure 5.1 shows a mixed-signal system comprising of two Field Programmable Gate Array (FPGA) ICs communicating with each other over a high-speed bus, with an LNA in close physical proximity. The test-vehicle has been fabricated using an organic SOP base process. This system closely approximates an actual cell-phone or WLAN-based mixed signal system. The LNA represents the sensitive RF circuitry, while the FPGAs approximate the high-speed digital baseband processor. In such a scenario, the potential digital noise coupling mechanisms can be classified as follows:

a) Through EMI from high-speed digital signals with near-field or far-field coupling mechanisms.
b) Through power supply fluctuations from a common power-distribution network.

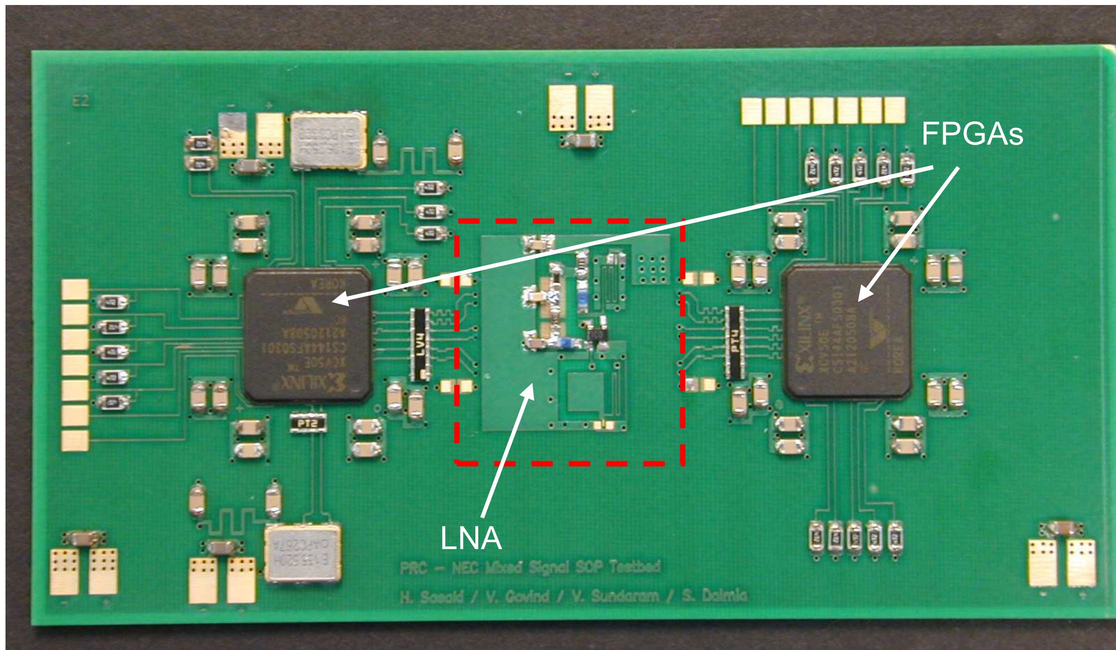


Figure 5.1. Mixed-signal test-vehicle showing an RF circuit (LNA) in close proximity to digital circuits (FPGAs).

The LNA in the mixed-signal environment can be modeled as a black box with multiple input ports and a single output port. The “actual” RF input port connected to the antenna-filter-balun receiver chain form merely one of the inputs. Various noise sources can couple into the LNA circuitry through the other input ports. Different transfer functions can then be used to describe the appearance of these signals at the LNA output port.

The effect of the noise components in the degradation of system performance is primarily determined by the location of the noise spikes in the frequency spectrum. As long as they do not have enough power to modify the bias conditions, the out-of-band noise tones appearing as spikes in the LNA output spectrum can be removed by a downstream filter and are not particularly harmful. In-band noise spikes cannot be

removed in such a manner and are passed onto downstream components. Whether high-power or not, they pose problems by reducing the dynamic range of the system. Thus, depending on the position of the noise spikes in the frequency spectrum, the noise coupling can also be classified as:

a) Direct coupling - Frequency components of noise (and their harmonics) that lie in the operational frequency band of the RF circuit, couples directly into the circuit and appear at the output.

b) Indirect coupling - Frequency components of noise form intermodulation products with the input RF signal (due to the non-linearities in the circuit), and appear at the output.

The rest of the chapter is organized as follows: Section 5.1 discusses EMI-based noise coupling from high-speed digital signal lines and Section 5.2 with power supply fluctuations from a common power-distribution network. Both phenomenon have been experimentally studied using test-vehicles, comprising of the LNA of the previous chapter in close proximity to a digital noise-source. Section 5.3 covers the use of Electronic Band Gap (EBG) structures for suppression of RF signal propagation and finally, Section 5.4 describes the implementation of a mixed-signal system using EBG for noise-suppression.

5.1 EMI Based Noise Coupling

In [76], Sasaki et al. have shown the design and fabrication of three test vehicles (A, B and C), to study the noise coupling from high-speed digital signal lines to the analog domain. Each system consists of an LNA of the type described in Chapter 4 (using three embedded passives and designed to operate at 1.83 GHz) and a 50Ω microstrip line terminated with a 50Ω 0603 resistor. The boards are 100mm x 50mm in size, and fabricated using a 6-metal layer LD-621 (tanδ = 0.005, ε_r = 3.2 at 2GHz) process (Figure 5.2). The board stack-up consists of signal, ground, power and ground, with the embedded passives of the LNA located in the top two metal layers.

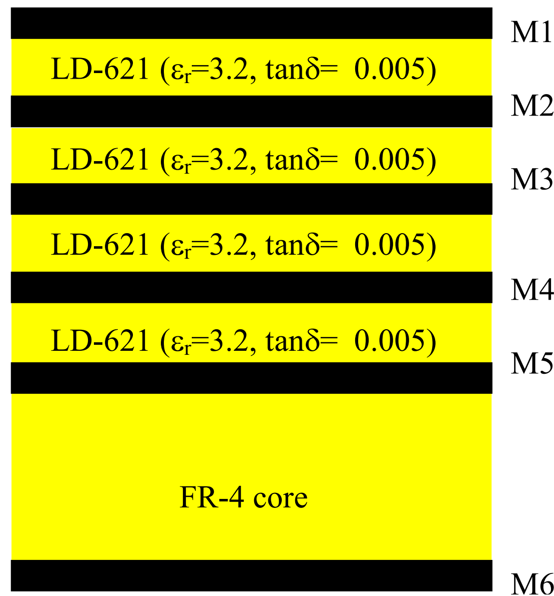
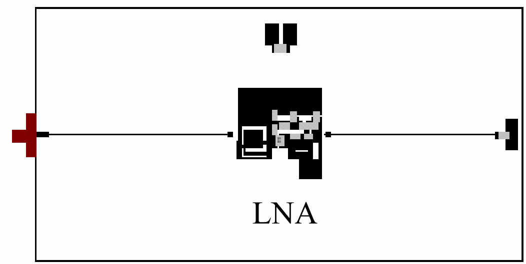
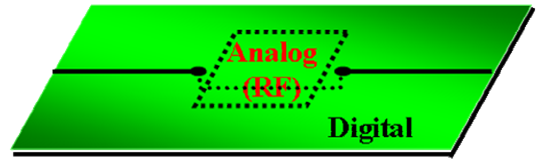
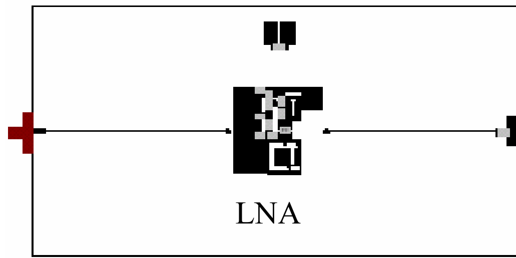


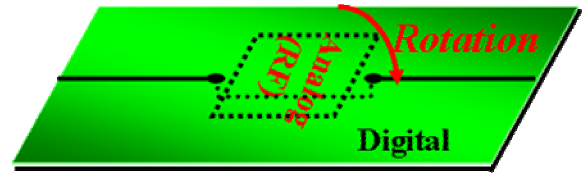
Figure 5.2. Board stack-up.



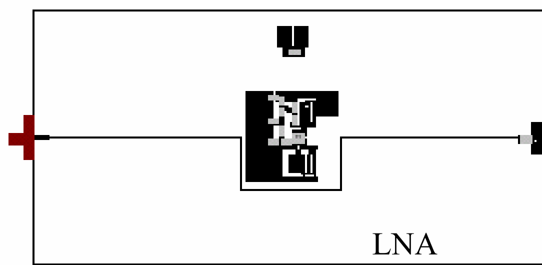


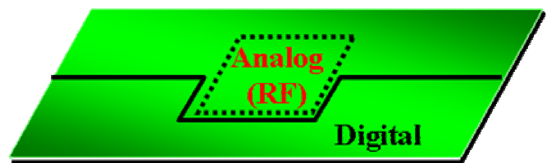
a)





b)





c)

Figure 5.3. a) Test vehicle A. **b)** Test vehicle B. **c)** Test vehicle C.

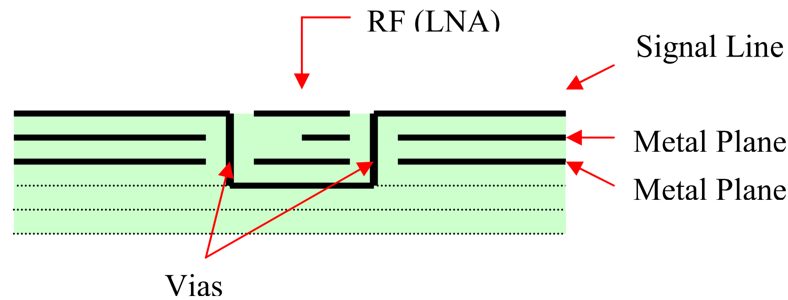


Figure 5.4. Cross-section of the 6-metal layer board substrate, showing the routing of the signal line beneath the LNA (for boards A and B).

Figure 5.3. shows the three test vehicles. The RF circuit remains the same in all three cases (although its orientation is off by 90° in the case of test vehicle B), while the routing of the signal line was changed to study the noise coupling through EMI. Board A and B have the signal line routed beneath the LNA (on metal layer 4) (Figure 5.4), while board C have the line meandered around the LNA on the top surface.

5.1.1. Indirect Coupling

Indirect noise coupling through EMI from signal lines was studied by connecting a 100 MHz, 1 Vpp clock signal to the microstrip line. The LNA was supplied with a 1.83 GHz, -15dBm sine wave signal and the output was observed using a spectrum analyzer. Figure 5.5 shows the measurement setup, and Figures 5.6 and 5.7 show the output spectrum of the LNA in the test vehicles A, B and C.

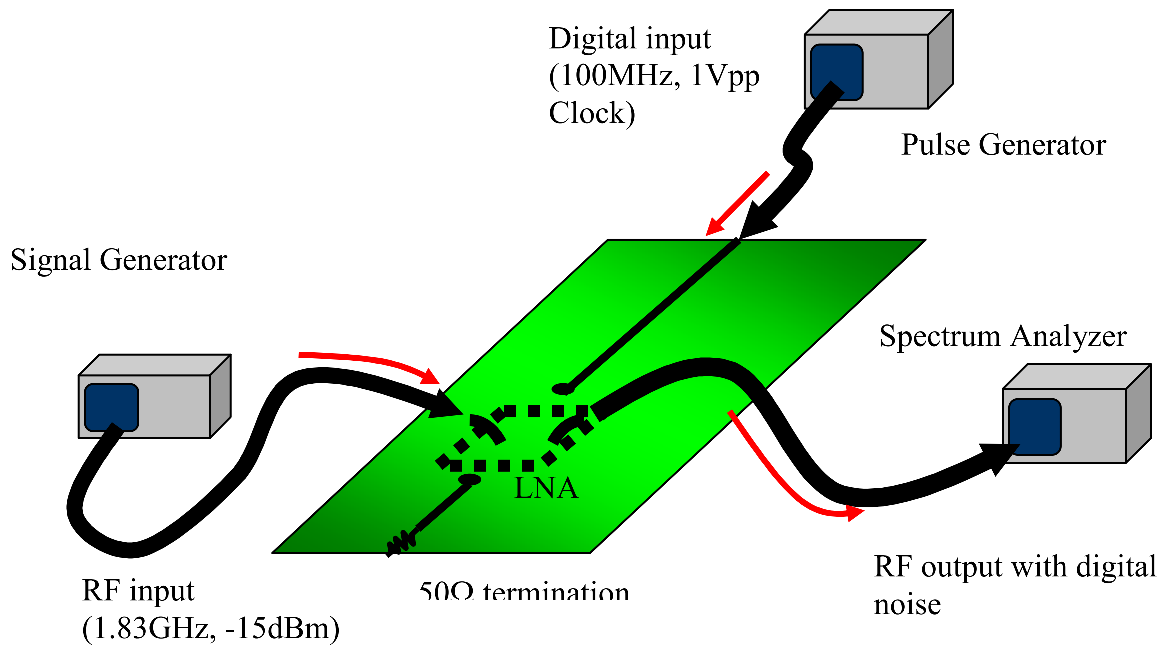


Figure 5.5. Measurement setup

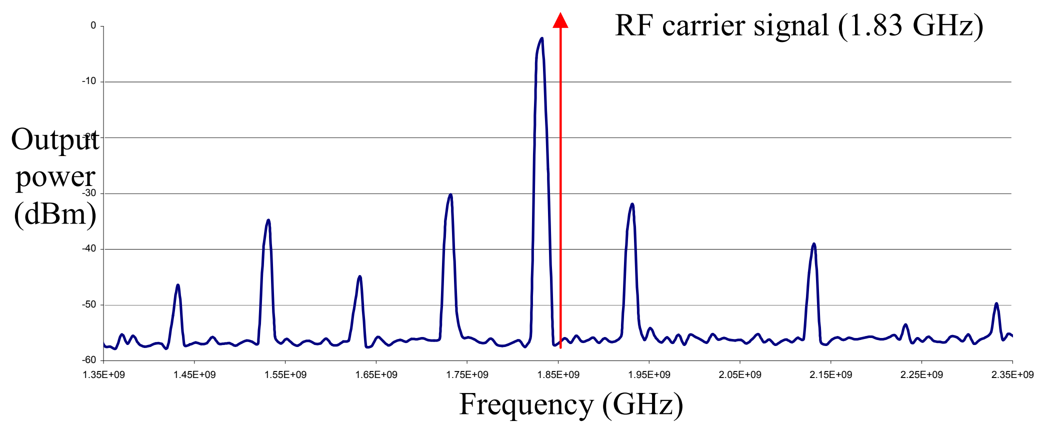
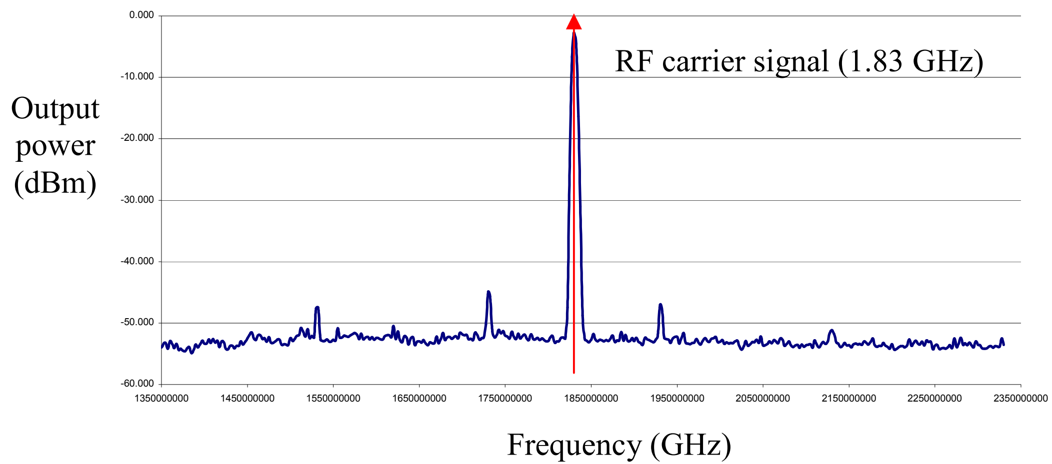
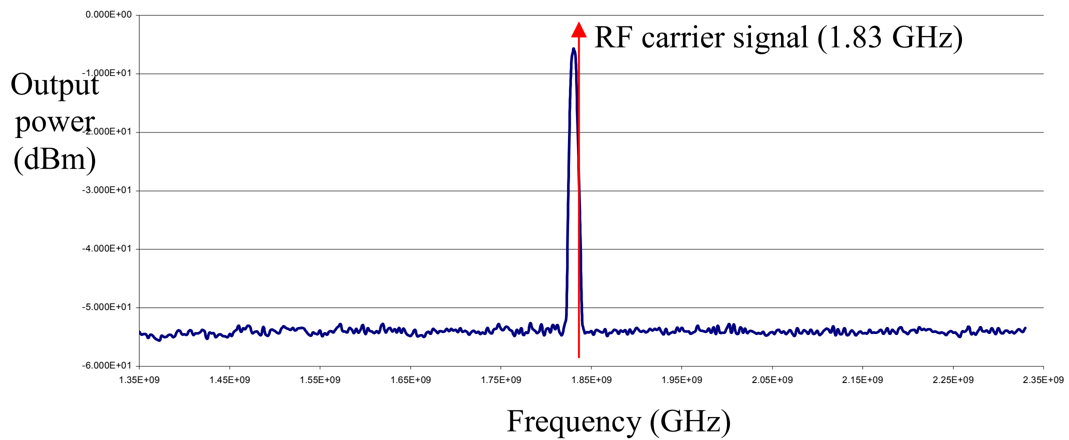


Figure 5.6. LNA output spectrum of Test vehicle A.



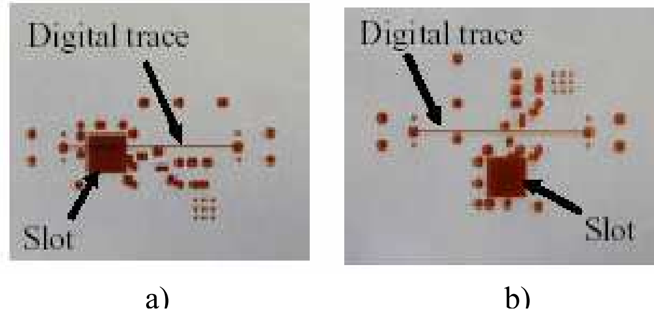
b)



c)

Figure 5.7. LNA output spectrum. **b)** Test vehicle B. **c)** Test vehicle C.

It can be observed that the output of the LNA in Testbed A exhibits maximum noise, while that of the LNA in Testbed C has minimum noise. This can be explained on the basis of the routing of the signal line on the board, and the signal coupling mechanisms existing in the system.



a) b)

Figure 5.8. Routing of the digital trace (metal layer 4) with respect to the LNA layout (metal layers 1 & 2; not shown) and the corresponding slot (metal layer 3). **a)** Test vehicle A. **b)** Test vehicle B.

Figure 5.8 shows the routing of the signal line on metal layer 4 with respect to the LNA layout for Testbeds A and B. To reduce parasitic capacitance to ground, a slot was cut on metal layer 3, beneath the bottom plate of the embedded capacitor on layer 2. It can be observed that in case of Testbed A, the signal line directly passes beneath the slot. Although the energy coupling between a signal trace and a slot has been described in [54], the size of the slot in the present case was very small compared to the wavelengths involved. Coupling through slot resonance could therefore be discarded, and most of the noise could be explained on the basis of direct capacitive coupling between signal line and lower plate of the capacitor. Testbed C, with the signal routed entirely on the top surface and a good return current path on metal layer 2 exhibits almost no noise coupling.

5.1.2. Direct Coupling

The via in the signal paths (in Testbeds A and B) results in a discontinuity in return current path, and can lead to excitation of the power-ground planes. As can be observed from Figure 5.9, the signal is initially referenced to the Ground plane in layer

M2. Near the vicinity of the RF circuit (LNA), it transitions to layer M4 through a via, with the reference plane changing from the Ground plane on M2 to the Power plane on layer M3. Except for the high impedance layer-to-layer capacitance existing between the Ground and Power planes at this point, there is no path for the return current to flow, creating a discontinuity. This provides another means for signal coupling, especially at high frequencies [76].

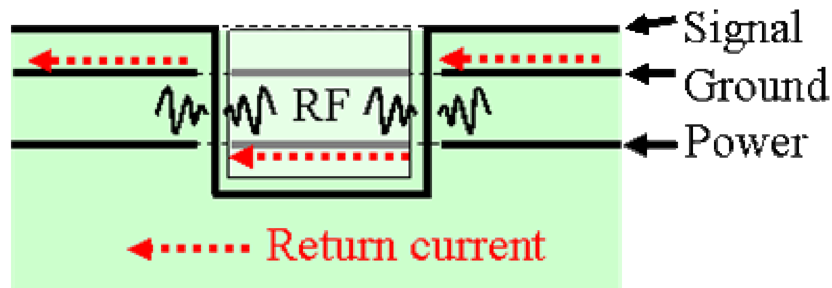
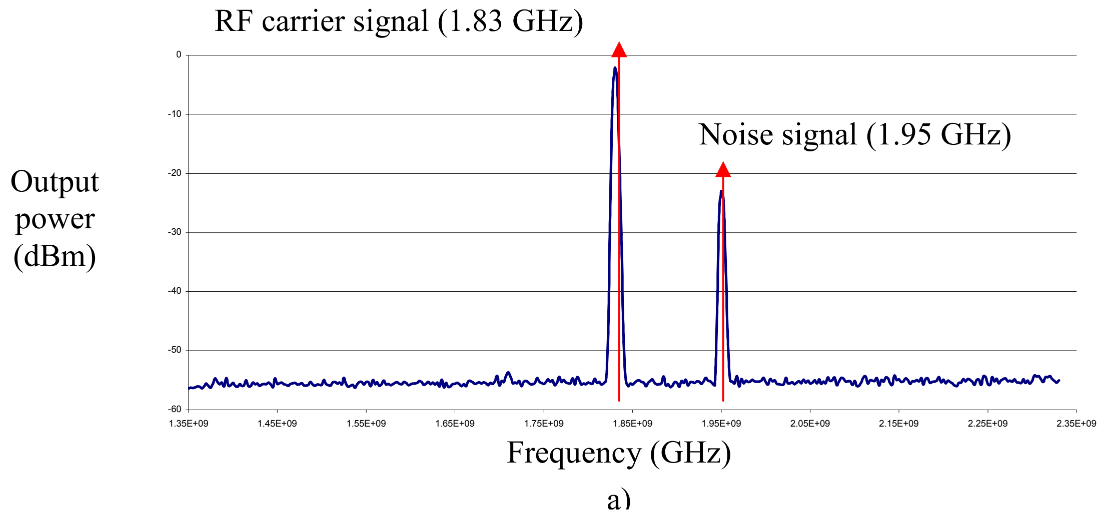
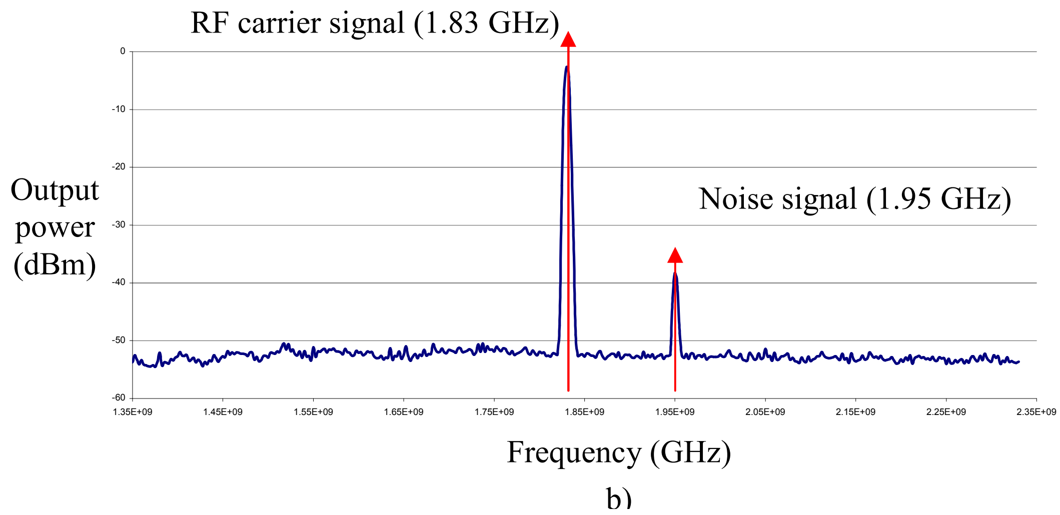


Figure 5.9. Via transition in the signal path, showing the discontinuity in the return current path.

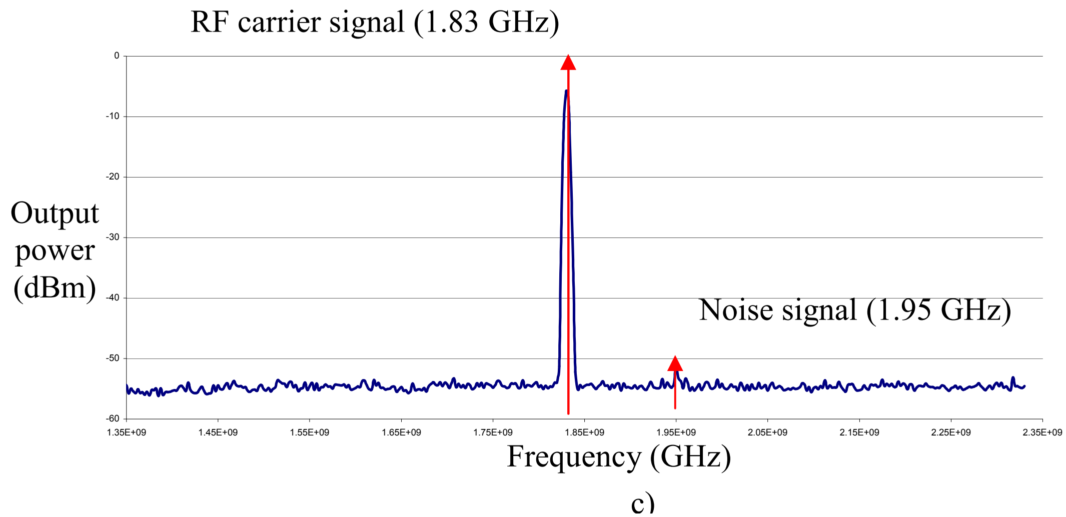
To study this effect as well as to observe direct coupling of signal energy into the operating frequency band of the LNA, a high frequency signal generator (1.95 GHz, -13 dBm sine wave) was connected to the signal line. The LNA was again supplied with a 1.83 GHz, -15dBm sine signal and the output was observed using a spectrum analyzer. Figure 5.10 shows the output spectrum of the LNAs in the test vehicles A, B and C.



a)



b)



c)

Figure 5.10. LNA output spectrum **a)** Test vehicle A. **b)** Test vehicle B. **c)** Test vehicle C.

As can be observed, Test vehicle A once again shows maximum noise coupling. To isolate the noise coupled due to the discontinuity in the return current path, 4 capacitors (0.1 uF each) were placed around the two vias in the signal path. The resulting measurements exhibited around 4 dB reduction in the amplitude of the coupled noise.

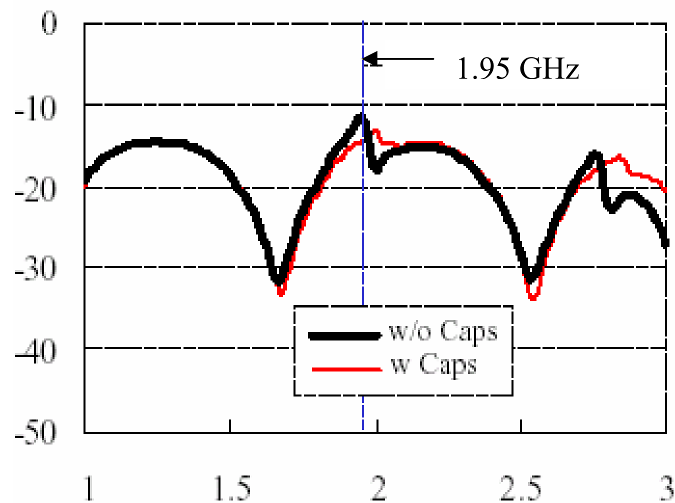


Figure 5.11. S11 measurements at the input of the 50Ω microstrip signal line (on Testbed A), with and without capacitors.

Figure 5.11 shows the S11 measurements taken at the input of the microstrip signal line, with and without the capacitors. The system showed a discontinuity at ~1.95 Ghz, without the capacitors, which explained the 4 dB of additional noise coupled at that frequency (although another glitch could be observed at ~2.7 GHz, it lay outside the operating frequency band of the LNA).

5.2 Power Supply Based Noise Coupling

Noise coupling through the power supply is a more difficult problem to solve, primarily because of the *physical* connection that it provides between the RF and digital sub-domains.

A test vehicle was designed to study noise coupling from digital to analog domain through a common power supply [77]. It consisted of an LNA of the type described in Chapter 3 (using three embedded passives and designed to operate at 2.13 GHz) and a Xilinx Virtex™ series FPGA. The FPGA drove a 300MHz signal bus, and both the LNA and the FPGA were powered using a common power supply (3.3V) distributed with a power-ground plane pair. The boards were fabricated using a 3-metal layer FR-4 ($\tan\delta$ = 0.02, ε_r = 4.4 at 1MHz) stack-up). As in the previous section, the embedded passives for the LNA were implemented using the top two metal layers. The signal bus consisted of 50Ω microstrip lines referenced to metal layer 2 (Ground), with terminations implemented using 50Ω 0603 resistors.

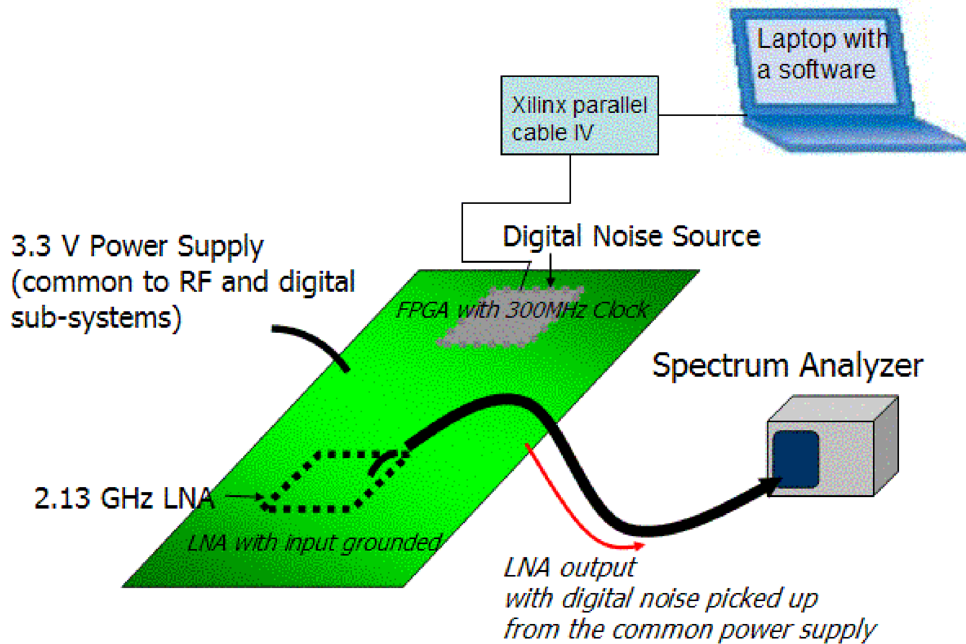


Figure 5.12. Measurement setup.

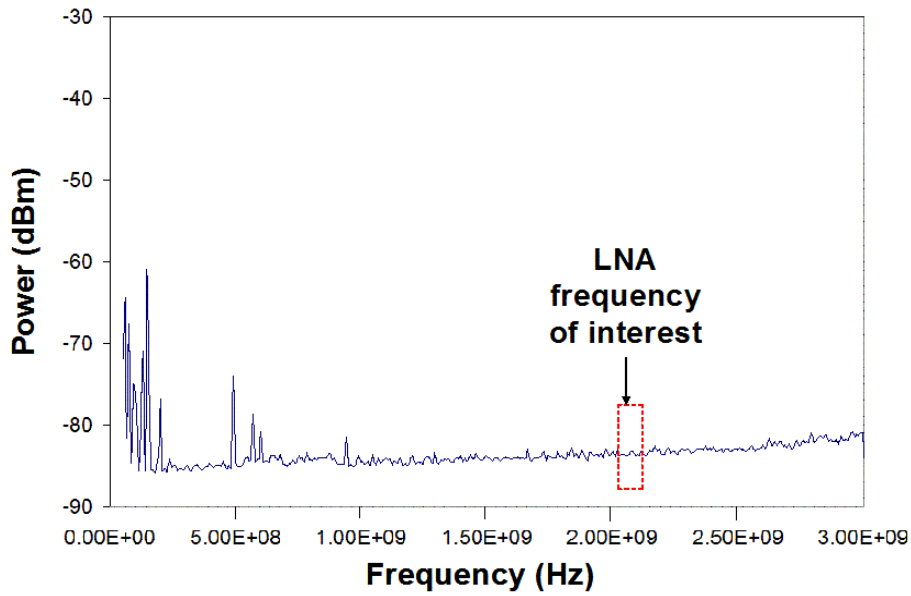
Figure 5.12 shows the measurement setup used for the experiment. The input of the LNA is shorted to the RF ground, to prevent any noise coupling through the input port. Signal coupling through EMI from the digital signal lines is minimized through careful routing of the lines (as shown in the previous section, in Testbed C).

With this set-up, the power supply becomes the only noise source for the LNA. As the FPGA begins driving the signal lines, the output drivers and internal logic circuits switch simultaneously, producing fluctuations in the power supply. In a typical power-distribution system, the power-ground planes act as electromagnetic resonant cavities, where the physical dimensions and dielectric constant of the material between the planes determine the resonant frequency ([78]-[79]). The standing waves in the cavity at resonance can produce significant coupling to neighboring circuits and transmission

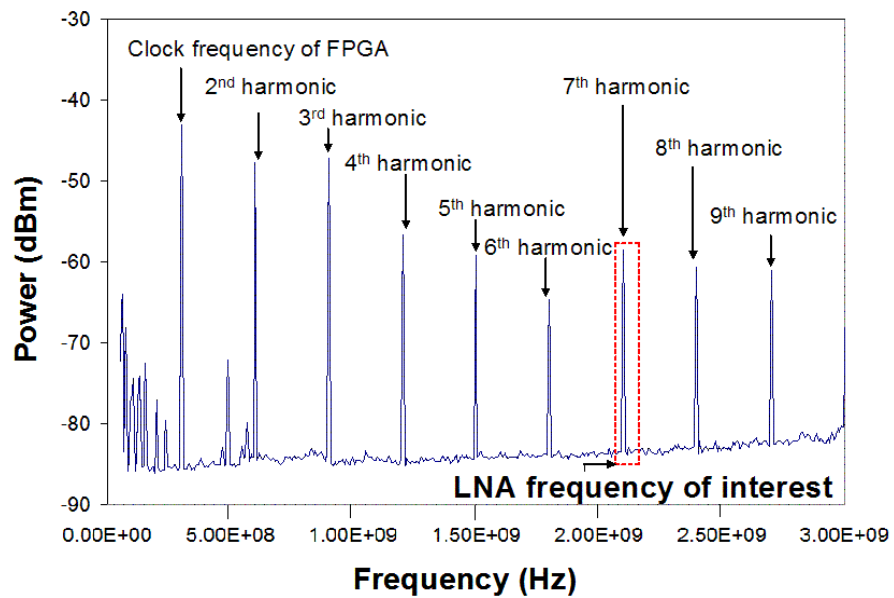
lines. Even at frequencies below the resonant frequency of the plane pair cavity, conductive coupling exists between circuits through the common power distribution system. The switching noise produced by the digital circuits thus couples into the LNA circuitry [77]. Fig 5.13 shows the Spectrum Analyzer measurements of the LNA output frequency spectrum.

Figure 5.13a shows the LNA output spectrum with the power supply turned on, but with the FPGA unprogrammed. The output drivers and internal logic circuitry of the FPGA are not operational in this stage, and the LNA output exhibits only some low-frequency noise. There are no noise spikes in or around the operational frequency band of the LNA (~ 2.1GHz), and the measurement results shows the noise floor of the Spectrum Analyzer (~-85dBm).

Figure 5.13b shows the LNA output spectrum when the FPGA is programmed to drive the signal bus with four switching drivers. As has been described previously [15], the spectral content of noise caused due to periodic digital transitions consists of discrete tones, each located at integer multiples of the digital signal. In this case, with the drivers switching at 300MHz to drive the signal bus, the noise spikes are located at integer multiples of 300MHz. In particular, the 7th harmonic of the 300 MHz FPGA clock (at 2.1 GHz) lies within the operational frequency band of the LNA, potentially degrading the receiver performance.



a)



b)

Figure 5.13. Measured frequency spectrum at the output of the LNA, with the input shorted to ground and **a)** system powered on, but with FPGA quite (not switching) **b)** system powered on and the FPGA driving the bus with a 300MHz clock.

5.3 Electromagnetic Isolation

Ideally, the LNA should be separated from the digital circuitry such that there exists *no* signal coupling between them. As the frequencies of operation increases, however, electromagnetic coupling becomes important and it becomes impossible to *completely* isolate *any* two regions of the system.

One possible solution to the problem is the use of split power and/or ground planes (with the use of multiple power supplies) [80]. However part of the electromagnetic energy can still couple through the gap, especially at higher frequencies [81]. Hence, this method only provides marginal isolation (-20 dB - ~-60 dB) at frequencies above 1 GHz, and becomes ineffective as system operating frequencies increase. With the high sensitivity requirements of long distance communication protocols (-102dBm for GSM900, -116dBm for WCDMA), the system-level isolation requirements are much higher. Further, as systems become more and more compact, multiple power supplies also become a luxury that the designer cannot afford.

With the restriction to use a single power supply for both digital and RF circuits, the need for a low-pass functional block that provides DC connectivity throughout the system but prevents the transfer of high-frequency noise components arises. In such a scenario, the analog/RF and digital sub-systems would be powered using separate sections of a common power distribution system (power planes), with the filter blocking transfer of high-frequency signal power between the sections. Several schemes involving split power planes connected using a lumped inductor, a printed inductor or a ferrite bead

have been suggested in the past ([82]-[83]). However, all of them offer maximum isolation in the order of -40dB, with significantly lower isolation numbers at resonant frequencies of the discrete components.

For e.g., Figure 5.14 shows the point-to-point isolation obtained in a system using the Murata BLM18GG471SN1 ferrite bead. As can be observed, the maximum value of isolation is obtained at ~1GHz and does not go below –25dB. Note that this is a "high-performance" ferrite bead optimized for operation at 1GHz.

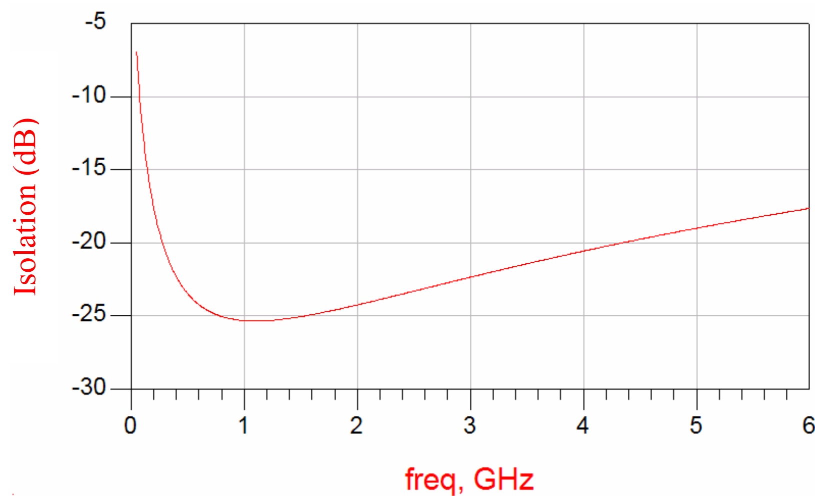


Figure 5.14. Simulated isolation of the Murata ferrite bead.

Electronic Band Gap (EBG) structures are a distributed means for implementing RF isolation. They are periodic structures in which the propagation of electromagnetic waves is forbidden in certain frequency bands [81]. Therefore, they can be thought of as

distributed low-pass filters, with the stop-band (and isolation in the stop-band) depending on the construction of the EBG cells.

In the past, EBG-based designs have been used for achieving RF isolation in antenna design [84]. And more recently, Kamgaing et. al. have used a 3-layer "mushroom-type" EBG to suppress the propagation of SSN in digital noise [85]. With good point-to-point isolations and the ability to use a single power supply, EBGs have the potential to solve the power-supply based noise coupling in SOP-based mixed-signal integration.

In [79], Jinwoo et. al. have described a novel 2-layer EBG structure achieving isolation levels greater than –100dB. The novel EBG structure consists of a two-dimensional (2-D) rectangular lattice with each element consisting of a metal patch with two connecting metal branches, as shown in Figure 5.15a. Called Alternating Impedance EBG (AI-EBG) (on account of the alternating sections with high and low characteristic impedance), this EBG structure can be realized in the ground plane or in the power plane, depending on design constraints. Such an EBG-based power distribution system would consist of metal patches connected by thin metal branches to form a distributed LC network (where L is inductance and C is capacitance). The metal branch introduces inductance while the metal patch contributes to the capacitance. The unit cell of the EBG structure is shown in Figure 5.15b.

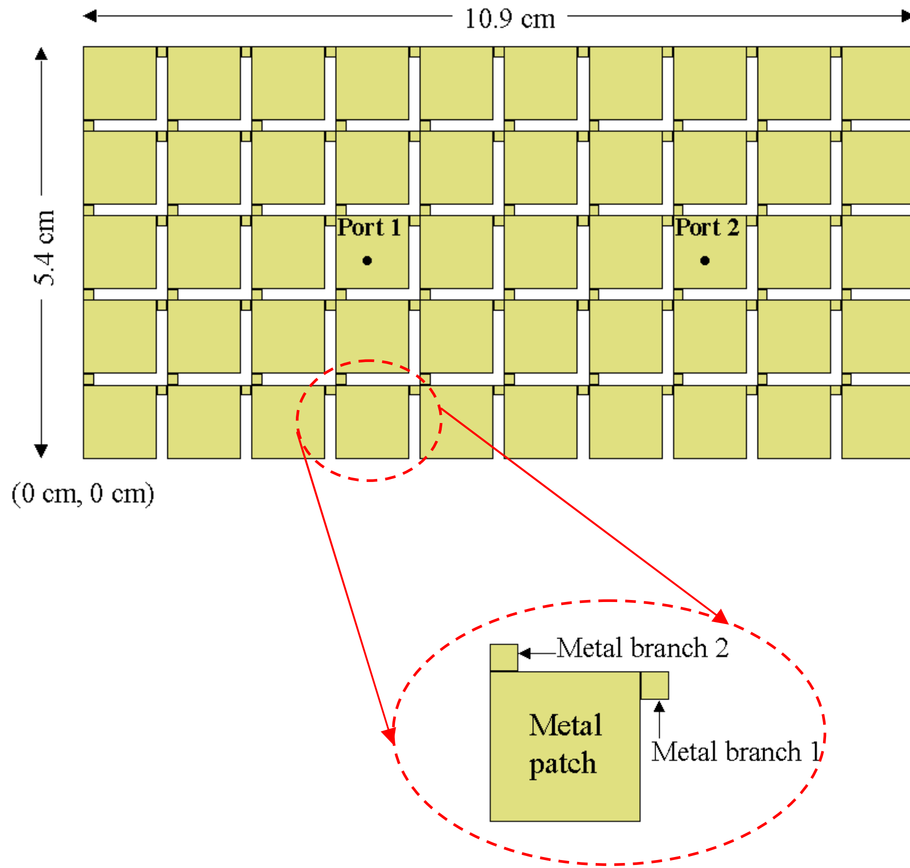


Figure 5.15. a) AI-EBG implementation **b)** Unit cell of the EBG structure.

Compared to the "mushroom-type" EBG of [83], the AI-EBG structure can be optimized for low dielectric thickness. It also uses only two metal layers, and does not require any microvias. Most importantly, it provides a much higher performance in terms of isolation. Figure 5.16 shows the photograph of an EBG implementation in a 2-layer FR-4 process (tanδ = 0.02, ε_r = 4.4 at 1MHz), and measured and modeled isolation (S21). As can be observed, the EBG provides ~-80dB isolation in the 2.4-3.5GHz frequency band.

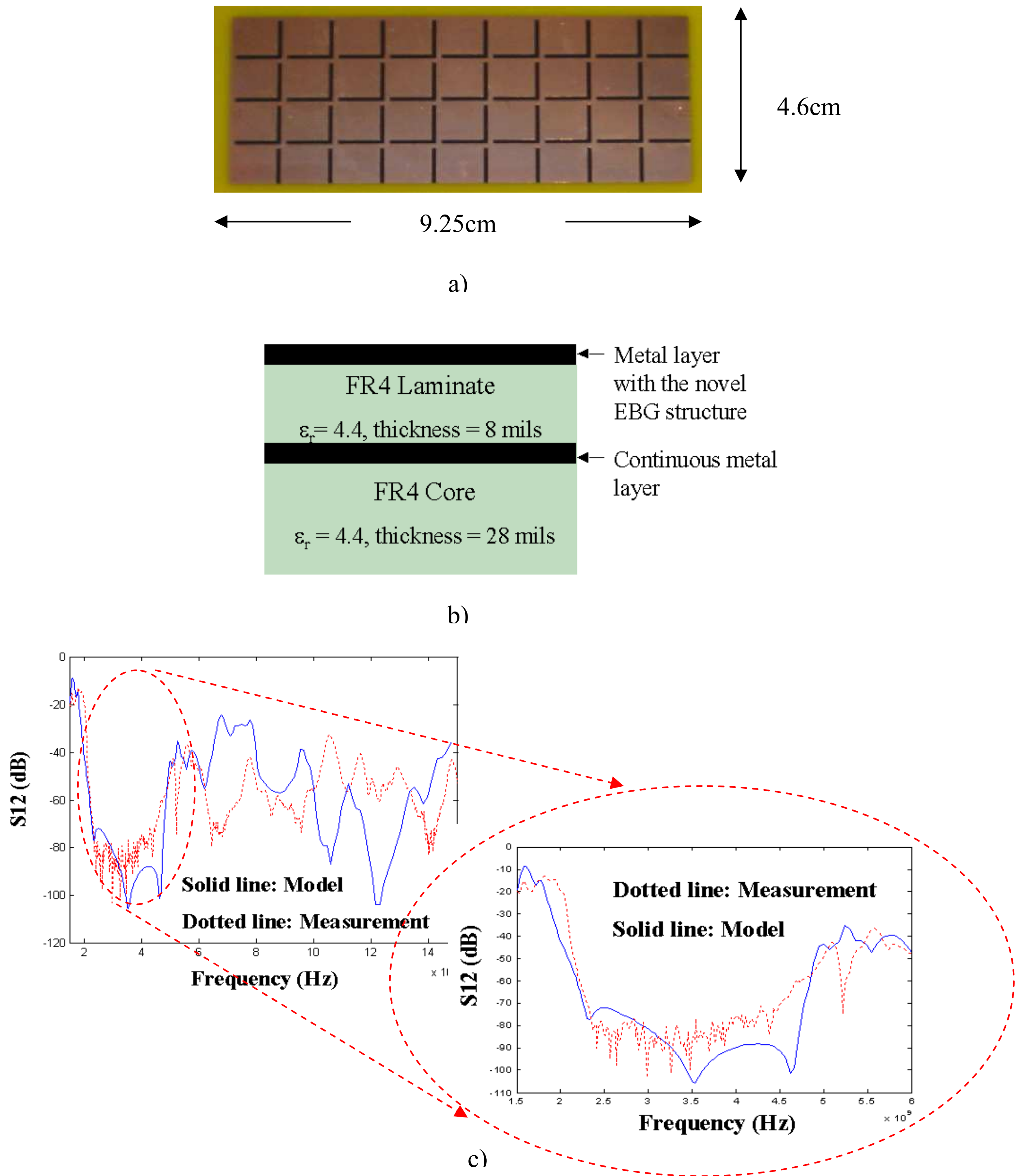


Figure 5.16. a) Photograph of an AI-EBG implementation. **b)** FR-4 stackup used. **c)** Model-to-hardware correlation for isolation (S21) in the structure.

It is evident that an AI-EBG-based power distribution scheme has the potential for suppressing power supply based noise propagation in mixed-signal systems. It also enables the use of a single power supply for the module, reducing the size and cost of the device.

5.4 Mixed-Signal System Integration Using EBG-Based Power Distribution

Figure 5.17 shows the simulated results of an AI-EBG structure specifically designed for use with the LNA described in Section 5.2 of this chapter [77].

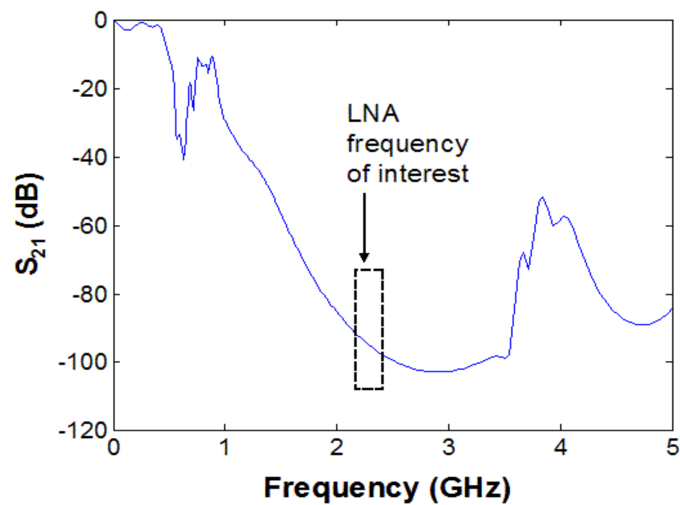
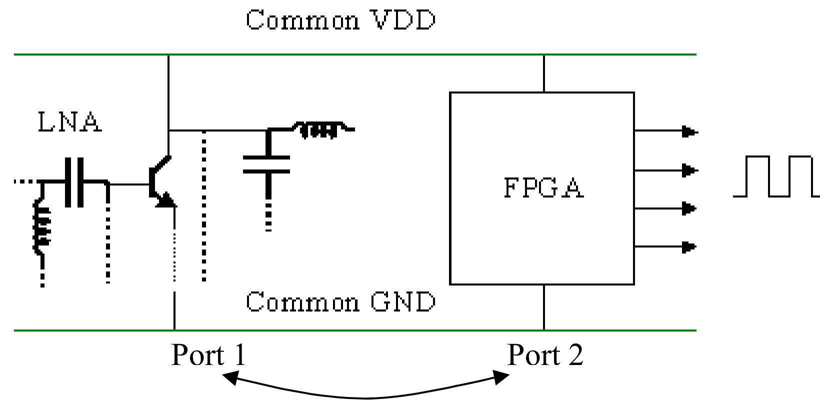


Figure 5.17. Simulated transmission coefficient of the EBG.

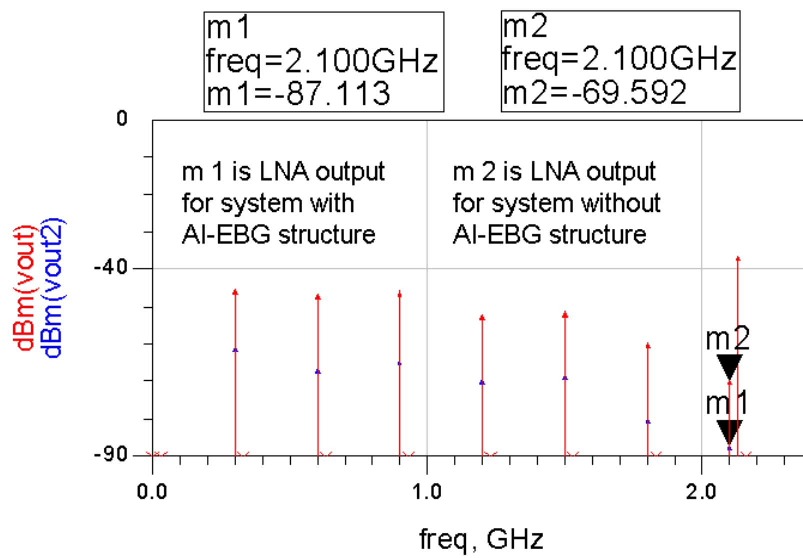
As can be observed, the isolation in the frequency band of interest of the LNA (centered around 2.14GHz) is more than 90dB. If the LNA and the FPGA can be positioned in such a way as to obtain this transmission coefficient between them, it would suppress almost all direct in-band noise coupling.

To analyze the feasibility of using EBGs for noise suppression in mixed-signal systems, the circuit shown in Figure 5.18a was simulated in HP-ADS™. The digital noise source was modeled using an ideal clock pulse in the frequency domain with a frequency of 300MHz. Two conditions were simulated – one where an ordinary power-plane pair (of the type used in the experiment of Section 5.2) was used to distribute a common power supply to the FPGA and the LNA, and a second case where the ground plane was replaced with an AI- EBG structure. In both cases, z-parameter transmission matrices were used to model the power distribution networks ([49], [77]). Figure 5.18b shows the simulated LNA output spectrum, with and without the AI-EBG-based power distribution system. Noise tones exist at integer multiples of the clock frequency (300MHz). In the figure, red lines show the noise coupled through an ordinary plane pair, while blue lines represent noise coupled through the AI-EBG-based power system. Specifically, at 2.1GHz (the operating frequency of the LNA), marker m2 using the ordinary power planes shows a noise power of ~–69.6dBm, while marker m1 using the AI-EBG-based power supply shows a decrease in noise power to ~-87dBm.

The simulation results validate the assumption that an EBG-based power distribution system would be suitable for noise suppression in a mixed-signal SOP environment.



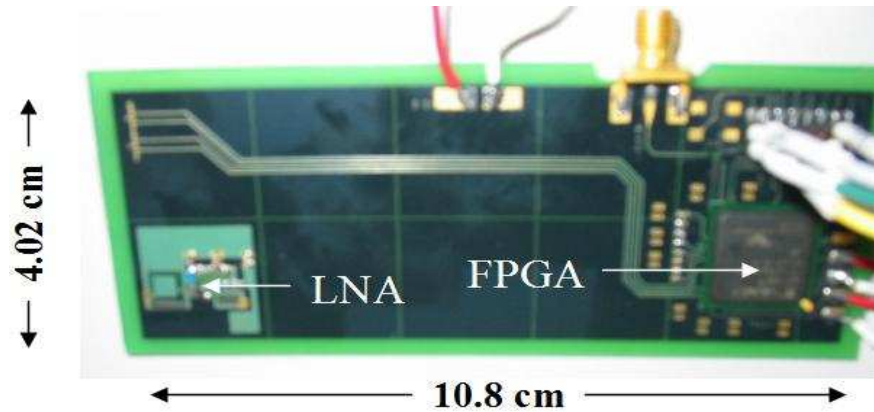
a)



b)

Figure 5.18. a) Frequency domain simulation of the mixed-signal system. Figure shows the definition of the two ports. **b)** Simulated LNA output spectrum. The red lines (and marker m2 at 2.1GHz) show the noise coupled through an ordinary plane pair, while the blue lines (and marker m1 at 2.1GHz) represent noise coupled through the AI-EBG-based power system.

Figure 5.19 shows the photograph of the fabricated mixed-signal test-vehicle. It consists of the LNA and FPGA of Section 5.2, but the ground plane has been replaced with the AI-EBG based structure. The FPGA drives four 50Ω microstrip lines, with terminations implemented using 50Ω 0603 resistors.

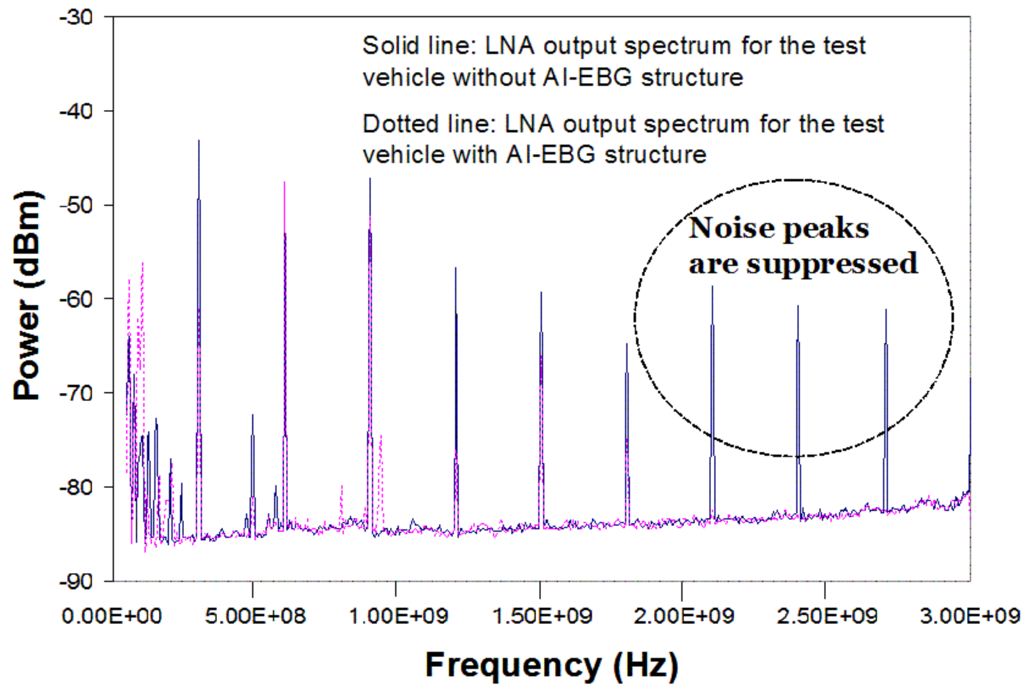


a)

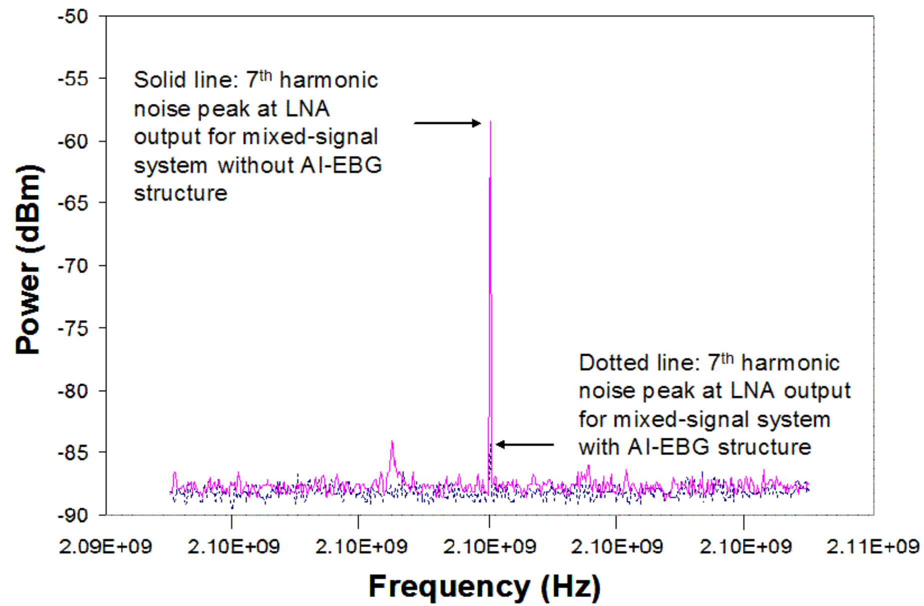
Stack-up	Layer
Copper (36 μm)	Signal layer
FR4 (ε_r = 4.4, thickness= 5 mils)	
Copper (36 μm)	Ground layer
FR4 (ε_r = 4.4, thickness= 5 mils)	
Copper (36 μm)	Power layer
FR4 (ε_r = 4.4, thickness = 28 mils)	

b)

Figure 5.19. a) Photograph of the test-vehicle **b)** 3-metal layer FR-4 stack-up used to implement the system.



a)



b)

Figure 5.20. a) Comparison of LNA output spectrum, with and without the AI-EBG–based power distribution scheme. **b)** Comparison of 7th harmonic noise peak at 2.1 GHz for the mixed-signal systems with and without the AI-EBG AI-EBG–based power distribution scheme.

Figure 5.20 shows the comparison of LNA output spectrum for the two test vehicles – the blue line represents noise coupling through ordinary power-ground plane pair, while the red line represents the noise coupled through the AI-EBG-based power distribution system. At low frequencies, where the EBG does not provide much isolation, both measurements remain similar. However at ~2GHz (where the stop band of the EBG begins), a clear distinction can be seen in the amount of coupled noise power. For the frequencies of 2.1GHz and above, there is virtually no noise power transferred in the test vehicle with AI-EBG structures, exhibiting superior EMI control.

5.5 Wideband Noise Suppression

The isolation methods explored in Section 5.3 (split planes connected using lumped or printed inductors, or ferrite beads) can be used in conjunction with the EBG-based techniques to improve performance of the system. As all of the techniques are low-pass filters in essence, they provide good isolation at low frequencies. This allows the EBG cut-off frequency to be shifted to the right, leading to smaller sizes for the unit cells. A hybrid approach can thus result in smaller system sizes and/or increased isolation in the EBG frequency band (by accommodating more number of unit cells). For e.g., Figure 5.21 shows a comparison of isolation numbers obtained using different combinations of EBG and ferrite beads. As can be observed, a series combination of EBG with ferrite

beads provides highest isolation in the stop-band, as well as improving the isolation at low frequencies.)

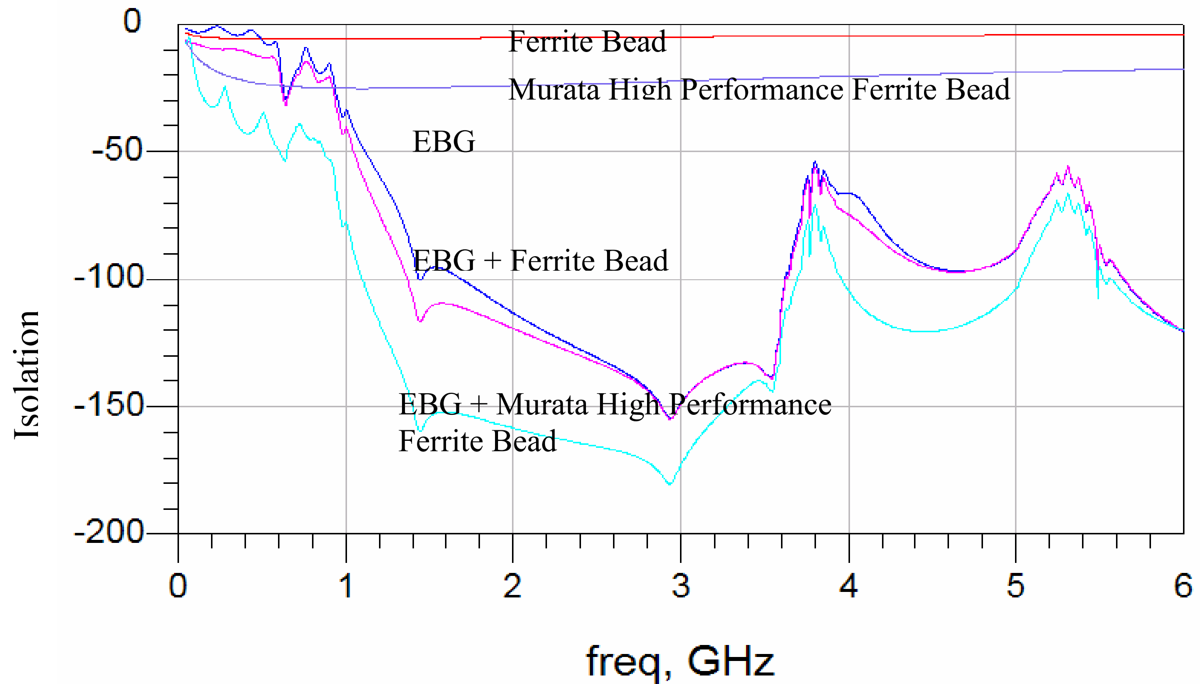


Figure 5.21. Simulated performance comparison of different combinations of EBG-based structures and ferrite beads.

5.6 Summary

The coupling of noise into RF circuitry from high-speed digital lines has been studied using test-vehicles and design rules to minimize EMI-based noise coupling in mixed-signal systems has been established. Providing a clean return-current path (by the use of sufficient number of decoupling capacitors) can minimize direct in-band high-

frequency noise coupling. Careful routing of the signal lines and layout of the embedded passives can minimize the indirect low-frequency noise coupling. As shown with the example of Test vehicle C, EMI-based mixed-signal coupling can be minimized even with the high-speed signal line laid out in close proximity to the RF circuit.

The coupling of noise into RF circuitry through a common power-supply has also been studied using test-vehicles. An EBG-based noise suppression scheme has been implemented, with much higher isolation than that provided by conventional methods such as ferrite beads. Measured results show almost complete suppression of in-band digital noise, paving the way for completely integrated mixed-signal solutions.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

This thesis reports the development of an organic SOP-based design methodology for mixed-signal integration, using multilayer heterogeneous laminates. To this purpose, multiband radio architectures were first studied, to choose the topology best suited for integrating a multiband multimode wireless transceiver with a high-speed digital base-band processor. The choice of a "multiple single-band" architecture in conjunction with an organic SOP-based implementation scheme finalized the basic building blocks required to realize such a module. From a design perspective, this required the development of novel circuit topologies and substrate stack-ups for the realization of singleband and multiband baluns. Additionally, this also necessitated a design partitioning methodology, for the use of embedded passives in the package in conjunction with on-chip active circuitry.

A novel multiband balun theory was developed, based on the classic Marchand architecture. The design is particularly useful for an SOP-based implementation scheme, as it uses both lumped and distributed components to achieve the functionality. As an extension of this theory, a design methodology for compact wideband baluns was also completed. A novel multilayer substrate using LCP was then used to implement both multiband and singleband baluns, as proof-of-concept for the design strategy. The baluns, designed for 900MHz/2.1GHz in the case of multiband functionality and 5GHz-6GHz in the case of wideband singleband functionality, showed good measurement-to-model

correlation, validating the methodology. These are the first baluns ever reported on an LCP based stack-up.

The need for low-profile components that can be attached on the top of a package substrate necessitates thin stack-ups with high component density. A novel organic stack-up involving a high-K material was used to implement narrow-band baluns with sizes as low as 2mmx1.25mm, at the same time restricting the height of the packaged device to 0.5mm. Again, these are the first baluns ever reported on an organic high-K laminate based stack-up.

To look at design partitioning issues in the RF front-end, the NF of a cascode CMOS LNA was derived as a function of the Q factors of its inductors. Beyond a certain inductor Q, the NF becomes almost independent of Q. The SOP implication of this, i.e. the tradeoff of higher inductor size for higher Q, was analyzed. A chip-package co-design strategy for integrated CMOS LNAs, with simultaneous optimization of NF and package size was developed. The inductor Q was used as a design variable, and has been incorporated into the LNA design methodology.

The effect of return current layout and coupling between multiple embedded passives on system performance was then studied, using an LNA as a test-vehicle. A modeling approach to integrate system-level full-wave solvers into the design flow of integrated systems with active devices and multiple embedded passives has been proposed, and validated through measurements. A computationally efficient circuit based modeling strategy using transmission line theory has also been used to predict the effect of coupling between embedded passives in SOP based schemes.

Finally, the important issue of digital noise coupling into RF circuitry (through a common power-supply as well as EMI from high-speed digital lines) was studied using test-vehicles. An EBG-based noise suppression scheme was implemented, with much higher isolation than that provided by conventional methods such as ferrite beads. This demonstration-system represents the first reported use of EBG for mixed signal noise suppression.

The design concepts developed in this thesis enables the development of compact, completely integrated mixed-signal modules with high-performance computing and high-speed wireless communication capabilities. As such, this facilitates the development of organic SOP into the integration platform of choice for high performance mixed-signal systems.

6.1. Future Work

The work described in this thesis removes a few roadblocks in the realization of fully integrated mixed-signal systems. However, more work needs to be done in all aspects of packaging before organic SOP integration schemes become the de facto standard in mixed-signal systems.

Development of new materials with improved properties is key to higher levels of system integration. Although the inductance and capacitance density can be increased by using novel materials and higher number of dielectric layers in the substrate stack-up, physics-based limitations restrict the size reductions that can be achieved for electromagnetic designs. It is conceivable that other physical phenomenon (e.g. organic

acoustic resonators) will need to be used in the design of communication circuits, for system size reduction.

The EBG-based power distribution scheme described in Chapter 4 can be highly miniaturized by the use of high dielectric constant materials and ferromagnetic metals. This increases the capacitance and inductance per unit area, resulting in smaller unit cells. As a result, the number of unit cells required to achieve a particular isolation level can be packed into a much smaller area. High dielectric constant materials with low thickness can also result in the integration of the power decoupling capacitance within the substrate.

Thermal issues remain one of the main impediments to SOP-based system integration. With increases in operating frequencies of the digital processors, dissipation of thermal power has turned out to be one of the biggest bottlenecks. RF power amplifiers (especially ones for long-distance communication protocols like GSM) also generate a lot of heat. Novel cooling mechanisms in the substrate as well as the chip-package interface are required to make future integrated mixed-signal systems feasible.

Finally, with developments like embedded actives, system-level testing will become one of the largest contributors to the final product cost. Novel test methodologies and strategies need to be developed to counter this.

References

[1] *The Electronics Industry Report*, Prismark Partners LLC, 2004.

[2] http://www.wsts.org

[3] http://www.intel.com/labs/features/cn09031.htm

[4] http://www.n-gage.com

[5] H. Hashemi and A. Hajimiri, "Concurrent multiband low-noise amplifiers – theory, design and applications", *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, pp. 288-301, Jan. 2002.

[6] http://howstuffworks.lycoszone.com/microprocessor1.htm

[7] T. H. Meng, B. McFarland, D. Su and J. Thomson, "Design and implementation of an all-CMOS 802.11a wireless LAN chipset", *IEEE Communications Magazine*, vol. 41, pp. 160-168, Aug. 2003.

[8] R. R. Tummala and J. Laskar, "Gigabit wireless: system-on-a-package technology", *Proceedings of the IEEE*, vol. 92, pp. 376-387, Feb. 2004.

[9] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs", *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 743-752, May 1998.

[10] D. K. Shaeffer and T. H. Lee, "A 1.5-V 1.5-GHz CMOS low noise amplifier", *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 745-759, May 1997.

[11] G. Hayashi, H. Kimura, H. Simomura and A. Matsuzawa, "A 9mW 900MHz CMOS LNA with mesh arrayed MOSFETs", *Symposium on VLSI Circuits Digest of Technical Papers*, Honolulu, HI, pp. 11-12, Jun. 1998.

[12] E. Abou-Allam, J. J. Nisbat and M. C. Maliepaard, "Low voltage 1.9-GHz front-end receiver in 0.5µ CMOS technology", *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1434-1443, Oct. 2001.

[13] G. Gramegna, M. Paparo, P. G. Erratico and P. Devita, "A sub-1-dB NF +/- 2.3-kV ESD protected 900-MHz CMOS LNA", *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1010-1017, Jul. 2001.

[14] A. L. L. Pun, T. Yeung, J. Lau, F. J. R. Clement and D. K. Su, "Substrate noise coupling through planar spiral inductor", *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 877-884, Jun. 1998.

[15] M. Xu, D. K. Su, D. K. Shaeffer, T. H. Lee and B. A. Wooley, "Measurement and modeling the effects of substrate noise on the LNA for a CMOS GPS receiver", *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 473-485, Mar. 2001.

[16] N. K. Verghese and D. J. Allstot, "Computer-aided design considerations for mixed-signal coupling in RF integrated circuits", *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 314-323, Mar. 1998.

[17] D. K. Su, M. J. Loinaz, S. Masui and B. A Wooley, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits", *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 420-429, Apr. 1993.

[18] V. Sundaram, F. Liu, S. Dalmia, G. E. White and R. R. Tummala, "Process integration for low-cost system on package (SOP) substrate", *Proceedings of the IEEE Electronic Components and Technology Conference (ECTC)*, Orlando, FL, pp. 535-540, May 2001.

[19] A. Sutono, D. Heo, Y. –J. Emery Chen and J. Laskar, "High-Q LTCC based passive-library for wireless system-on-package (SOP) module development", *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, pp. 1715-1724, Oct. 2002.

[20] S. Donnay, P. Pieters, K. Vaesen, W. Diels, P. Wambacq, W. D. Raedt, E. Beyne, M. Engels and I. Bolsens, "Chip-package codesign of a low-power 5-GHz RF front end", *Proceedings of the IEEE*, vol. 88, pp. 1583-1597, Oct. 2000.

[21] S. Dalmia, F. Ayazi, M. Swaminathan, S. –H. Min, S. H. Lee, W. Kim, D. Kim, S. Bhattacharya, V. Sundaram, G. White and R. Tummala, "Design of embedded high-Q inductors in MCM-L technology", *IEEE MTT-S International Microwave Symposium Digest*, Phoenix, AZ, vol. 3, pp. 1735-1738, May 2001.

[22] P. Pieters, K. Vaesen, G. Carchon, S. Brebels, W. de Raedt, E. Beyne, M. Engels and I. Bolsens, "Accurate modeling of high-Q spiral inductors in thin-film multilayer technology for wireless telecommunication applications", *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, pp. 589-599, Apr. 2001.

[23] *The Prismark Wireless Technology Report*, Prismark Partners LLC, Dec. 2004.

[24] K. Lim, S. Pinel, M. Davis, A. Sutono, C. –H. Lee, D. Heo, A. Obatoynbo, J. Laskar, E. M. Tentzeris and R. Tummala, "RF-System-On-Package for wireless communications", *IEEE Microwave Magazine*, pp.88-99, Mar. 2002.

[25] W. Diels, K. Vaesen, P. Wambacq, S. Donnay, W. De Raedt, M. Engels and I. Bolsens, "Single-package integration of RF blocks for 5GHz WLAN application", *IEEE Transactions on Advanced Packaging*, vol. 24, pp. 384-391, Aug. 2001.

[26] S. Dalmia, *PhD Dissertation,* School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, 2002.

[27] http://www.analog.com/en/subCat/0,2879,764%255F801%255F0%255F%255F0%255F,00.html

[28] V. Govind, S. Dalmia, J. Choi and M. Swaminathan, "Design and implementation of RF subsystems with multiple embedded passives in multi-layer organic substrates", *Proceedings of the IEEE Radio and Wireless Conference (RAWCON)*, Boston, MA, pp. 325-328, Aug. 2003.

[29] S. Wu and B. Razavi, "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications", *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 2178-2185, Dec. 1998.

[30] D. M. Pozar and S. M. Duffy, "A dual-band circularly polarized aperture-coupled stacked microstrip antenna for global positioning satellite", *IEEE Transactions on Antennas and Propagation,* vol. 45 pp. 1618-1625, Nov. 1997.

[31] L. Zaid, G. Kossiavas, J. –Y. Dauvignac, J. Cazajous and A. Papiemik, "Dual-frequency and broad-band antennas with stacked quarter wavelength elements", *IEEE Transactions on Antennas and Propagation,* vol. 47 pp. 654-660, Apr. 1999.

[32] J. Romeu and J. Soler, **"**Generalized Sierpinski fractal multiband antenna", *IEEE Transactions on Antennas and Propagation*, vol. 49, pp. 1237-1239, Aug. 2001.

[33] H. –C. Ryu, H. –R. Ahn, S. –H. Lee and W. S. Park, "Triple-stacked microstrip patch antenna for multiband system", *Electronic Letters,* vol. 38, pp. 1496-1497, Nov. 2002.

[34] K. Kageyama, K. Saito, H. Murase, H. Utaki and T. Yamamoto, "Tunable active filters having multilayer structure using LTCC", *IEEE Transactions on Microwave Theory and Techniques*, pp. 2421-2424, Vol. 49, No. 12, Dec '01.

[35] H. Miyake, S. Kitazawa, T. Ishizaki, T. Yamada and Y. Nagatomi, "A miniaturized monolithic dual band filter using ceramic lamination technique for dual mode portable phones", *IEEE MTT-S International Microwave Symposium Digest*, pp. 789-792, 1997.

[36] S. Dalmia, A. Bavisi, S. Mukherjee, V. Govind, V. Sundaram, G. White and M. Swaminathan, "A multiple frequency signal generator for 802.11 a/b/g VoWLAN type applications using organic packaging technology", *Proceedings of the IEEE*

Electronic Components and Technology Conference (ECTC), Las Vegas, NV, pp. 1664-1670, Jun. 2004.

[37] R. Magoon, A. Molnar, J. Zachan, G. Hatcher and W. Rhee, "Single-chip quad-band (850/900/1800/1900 MHz) direct conversion GSM/GPRS RF transceiver with integrated VCOs and fractional-*N* synthesizer", *IEEE Journal of Solid-State Circuits*, vol.37, pp.1710-1720, Dec. 2002.

[38] A. Raghavan, D. Heo, M. Maeng, A. Sutono, K. Lim and J. Laskar, "A 2.4 GHz high efficiency SiGe HBT power amplifier with high-Q LTCC harmonic suppression filter", *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 1019-1022, Jun. 2002.

[39] S. –W. Yoon, M. F. Davis, K. Lim, S. Pinel, M. Maeng, C. –H. Lee, S. Chakraborty and S. Mekela, "C-band oscillator using high-Q inductors embedded in multi-layer organic packaging", *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 703-706, Jun. 2002.

[40] A. Bavisi, S. Dalmia and M. Swaminathan, "A 3G/WLAN VCO with High Q embedded passives in high performance organic substrate", *Proceedings of the IEEE Asia Pacific Microwave Conference (APMC)*, Seoul, S. Korea, Nov. 2003.

[41] T. Liu, J. D. Carothers and W. T. Holman, "Active substrate coupling noise reduction method for ICs", *IEEE Electronic Letters*, vol. 35, pp. 1633-1634, Sep. 1999.

[42] M. Felder and J. Ganger, "Analysis of ground-bounce induced substrate noise coupling in a low resistive bulk epitaxial process: design strategies to minimize noise effects on a mixed-signal chip", *IEEE Transactions on Circuits and Systems – II. Analog and Digital Signal Processing*, vol. 46, pp. 1427-1436, Nov. 1999.

[43] R. C. Frye, "Integration and electrical isolation in CMOS mixed-signal wireless chips", *Proceedings of the IEEE*, vol. 89, pp. 444-455, Apr. 2001.

[44] M. Nagata, J. Nagai, T. Morie and A. Iwata, "Measurements and analyses of substrate noise waveform in mixed-signal IC environment", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, pp. 671-678, Jun. 2000.

[45] M Nagata, J. Nagai, K. Hijikata, T. Morie and A. Iwata, "Physical design guides for substrate noise reduction in CMOS digital circuits", *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 539-549, Mar. 2001.

[46] J. Briaire and K. S. Krisch, "Principles of substrate crosstalk generation in CMOS circuits", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, pp. 645-653, Jun. 2000.

[47] A. Samavedam, A. Sadate, K. Mayaram and T. S. Fiez, "A scalable substrate noise coupling model for design of mixed-signal IC's", *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 895-904, Jun. 2001.

[48] J. Mao, *PhD Dissertation*, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2004.

[49] J. –H. Kim and M. Swaminathan, "Modeling of multilayered power distribution planes using transmission matrix method", *IEEE Transactions on Advanced Packaging*, vol. 25, pp. 189-199, May 2002.

[50] I. Novak. L. Smith and T. Roy, "Low impedance power planes with self damping", *Proceedings of the IEEE Topical Meeting on Electrical Performance of Electronic Packaging (EPEP)*, pp. 123-126, Oct. 2000.

[51] J. Kim and M. Swaminathan, "Modeling of irregular shaped power distribution planes using transmission matrix method", *IEEE Transactions on Advanced Packaging*, vol. 24, pp. 334-346, Aug. 2001.

[52] S. Chun, M. Swaminathan, L. D. Smith, J. Srinivasan, Z. Jin and M. K. Iyer, "Modeling of simultaneous switching noise in high speed systems", *IEEE Transactions on Advanced Packaging*, vol. 24, pp. 132-142, May 2001.

[53] T. E. Moran, K. L. Virga, G. Aguirre and J. L. Prince, "Methods to reduce radiation from split ground planes in RF and mixed signal packaging structures", *IEEE Transactions on Advanced Packaging*, vol. 25, pp. 409-416, Aug. 2002.

[54] W. Cui, X. Ye, B. Archambeault, D. White, M. Li and J. L. Drewniak, "EMI resulting from a signal via transition through DC power bus – effectiveness of local SMT decoupling", *Proceedings of the Asia-Pacific Conference on Environmental Electromagnetics (CEEM)*, pp. 91-95, May 2000.

[55] N. Marchand, "Transmission-line conversion transformers", *Electronics*, vol. 17, no. 12, pp. 142-145, Dec. 1944.

[56] W. K. Roberts, "A new wide-band balun", *Proceedings of the IRE*, vol. 45, pp. 1628-1631, Dec. 1957.

[57] G. Oltman, "The compensated balun", *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 3, pp. 112-119, Mar. 1966.

[58] J. -W. Lee and K. J. Webb, "Analysis and design of low-loss planar microwave baluns having three symmetric coupled lines", *IEEE MTT-S International Microwave Symposium Digest*, pp. 117-120, June 2002.

[59] D. Raicu, “Design of planar, single-layer microwave baluns”, *IEEE MTT-S International Microwave Symposium Digest*, pp. 801-804, Jun. 1998.

[60] K. S. Ang, Y. C. Leong and C. H. Lee, “Multisection impedance-transforming coupled-line baluns”, *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, pp. 536-541, Feb. 2003.

[61] Y. J. Yoon, Y. Lu, R. C. Frye and P. R. Smith, “Spiral transmission-line baluns for RF multichip module packages”, *IEEE Transactions on Advanced Packaging*, vol. 22, pp. 332-336, Aug. 1999.

[62] D. -W. Lew, J. -S. Park, D. Ahn, N. -K. Ahn, C. S. Yoo and J. -B. Lim, “A design of the ceramic chip balun using the multilayer configuration”, *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, pp. 220-224, Jan. 2001.

[63] S. Dalmia, V. Sundaram, G. White and M. Swaminathan, “Liquid Crystalline Polymer based RF/wireless components for multi-band applications”, *Proceedings of the IEEE Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, pp. 1866-1873, May 2004.

[64] K. S. Ang, Y. C. Leong and C. H. Lee, “Analysis and design of miniaturized lumped-distributed impedance-transforming baluns”, *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, pp. 1009-1017, Mar. 2003.

[65] B. P. Kumar and G. R. Branner, “Optimized design of unique miniaturized planar baluns for wireless applications”, *IEEE Microwave and Wireless Components Letters*, vol. 13, pp. 134-136, Feb. 2003.

[66] V. Govind, S. Dalmia, V. Sundaram, G. E. White and M. Swaminathan, “Design of multiband baluns on Liquid Crystalline Polymer (LCP) based substrates”, *Proceedings of the IEEE Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, pp. 1812-1818, Jun. 2004.

[67] V. Govind, W. S. Yun, S. Dalmia, V. Sundaram, G. E. White and M. Swaminathan, “Analysis and design of compact wideband baluns on multilayer Liquid Crystalline Polymer (LCP) based substrates”, *IEEE MTT-S International Microwave Symposium (IMS) Digest*, Long Beach, CA, Jun. 2005.

[68] R. K. Feeney, *RF Engineering I*, Georgia Institute of Technology.

[69] K. Wang, M. Frank, P. Bradley, R. Ruby, W. Mueller, A. Barfknecht and M. Gat, “FBAR Rx filters for handset front-end modules with wafer-level packaging”, *Proceedings of the IEEE Symposium on Ultrasonics*, pp. 162-165, Oct. 2003.

[70] J. Kaitila, M. Ylilammi, J. Molarius, J. Ella and T. Makkonen, “ZnO based thin film bulk acoustic wave filters for EGSM band”, *Proceedings of the IEEE Symposium on Ultrasonics*, pp. 803-806, Oct. 2001.

[71] H. Tsui and J. Lau, “SPICE simulation and tradeoffs of CMOS LNA performance with source-degeneration inductor”, *IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing*, vol. 47, pp.62-65, Jan. 2000.

[72] J. –S. Goo, K. –H. Oh, C. –H. Choi, Z. Yu, T. H Lee and R. W. Dutton, “Guidelines for the power-constrained design of a CMOS tuned LNA”, *Proceedings of the International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Seattle, WA, pp. 269-272, Sep. 2000.

[73] V. Govind, S. Dalmia and M. Swaminathan, “Design of integrated low noise amplifiers (LNA) using embedded passives in organic substrates”, *IEEE Transactions on Advanced Packaging*, vol. 27, pp. 79-89, Feb. 2004.

[74] D. B. Leeson, “A simple model of feedback oscillator noise spectrum”, *Proceedings of the IEEE*, vol. 54, p. 329, Feb.1966.

[75] S. Dalmia, S. –H. Min and M. Swaminathan, “Modeling RF passive circuits using coupled lines and scalable models”, *Proceedings of the IEEE Electronic Components and Technology Conference (ECTC)*, Orlando, FL, pp. 816-823, May 2001.

[76] H. Sasaki, V. Govind, K. Srinivasan, S. Dalmia, V. Sundaram, M. Swaminathan and R. R. Tummala, “Electromagnetic interference (EMI) issues for mixed-signal System-On-Package (SOP)”, *Proceedings of the IEEE Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, pp. 1437-1442, Jun. 2004.

[77] J. Choi, V. Govind, R. Mandrekar, S. Janagam, and M. Swaminathan “Noise reduction and design methodology in mixed-signal systems with Alternating Impedance Electromagnetic Bandgap (AI-EBG) structure”, *IEEE MTT-S International Microwave Symposium (IMS) Digest*, Long Beach, CA, Jun. 2005.

[78] S. Pannala, J. Bandyopadhyay and M. Swaminathan, “Contribution of resonance to ground bounce in lossy thing film planes”, *IEEE Transactions on Advanced Packaging*, vol. 22, pp. 249-258, Aug. 1999.

[79] S. Chun, M. Swaminathan, L. Smith, J. Zhang and M. Iyer, “Modeling of simultaneous switching noise in high speed systems”, *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 24, pp. 132-142, May. 2001.

[80] H. Liaw and H. Merkelo, “Signal integrity issues at split ground and power planes”, *Proceedings of the IEEE Electronic Components and Technology Conference (ECTC)*, pp. 752-755, May 1996.

[81] J. Choi, V. Govind and M. Swaminathan, "A novel electromagnetic bandgap (EBG) structure for mixed-signal system applications", *Proceedings of the IEEE Radio and Wireless Conference (RAWCON)*, Atlanta, GA, pp. 243-246, Sep. 2004.

[82] M. Swaminathan, J. Kim, I. Novak and J. P. Libous, "Power distribution networks for System-on-Package: status and challenges", *IEEE Transactions on Advanced Packaging*, vol. 27, pp. 286-300, May 2004.

[83] Y. Jeong, H. Kim, J. Kim, J. Park and J. Kim, "Analysis of noise isolation methods on split power/ground plane of multi-layer package and PCB for low jitter mixed mode system", *Proceedings of the IEEE Topical Meeting on Electrical Performance of Electronic Packaging (EPEP)*, pp. 199-202, Oct. 2003.

[84] D. Sievenpiper, R. Broas and E. Yablonovitch, "Antennas on high-impedance ground planes", *IEEE MTT-S International Microwave Symposium (IMS) Digest*, pp. 1245-1248, Jun. 1999.

[85] T. Kamgaing and O. M. Ramahi, "A novel power plane with integrated simultaneous switching noise mitigation capability using high impedance surface", *IEEE Microwave and Wireless Components and Letters*, vol. 13, pp. 21-23, Jan. 2003.