Design of Integrated Low Noise Amplifiers (LNA) Using Embedded Passives in Organic Substrates

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***Abstract*—The noise figure of a low noise amplifier (LNA) is a function of the quality factor of its inductors. The lack of high-Q inductors in silicon has prevented the development of completely integrated complementery metal oxide semiconductor (CMOS) LNAs for high sensitivity applications like global system for mobile communications (GSM) (1.9 GHz) and wideband code-division multiple-access (W-CDMA) (2.1 GHz). Recent developments in the design of high-Q inductors (embedded in low cost integrated circuit (IC) packages) have made single-package integration of RF front-ends feasible. These embedded passives provide a viable alternative to using discrete elements or low-Q on-chip passives, for achieving completely integrated solutions. Compared to on-chip inductors with low Q values and discrete passives with fixed Q_s, the use of these embedded passives also leads to the development of the passive Q as a new variable in circuit design. However, higher Q values also result in new tradeoffs, particularly with respect to device size. This paper presents a novel optimization strategy for the design of completely integrated CMOS LNAs using embedded passives. The tradeoff of higher inductor size for higher Q has been adopted into the LNA design methodology. The paper also presents design issues involved in the use of multiple embedded components in the packaging substrate, particularly with reference to mutual coupling between the passives and reference ground layout.**

***Index Terms*—Embedded inductors, inductive coupling, integrated passives, low noise amplifier (LNA), organic packaging, reference ground layout, return current, system-on-package (SOP).**

I. INTRODUCTION

THE DEMAND for low-cost wireless solutions has fueled the need for highly integrated systems with communication and computing capabilities. Traditionally, the main means for system integration has been the system-on-chip (SOC) approach, which requires the implementation of all the functional blocks of a system on a single chip, to reduce cost and improve performance. With improvement in f_T to 50 GHz and beyond, the SOC approach using silicon complementary metal oxide semiconductor (CMOS) technology provides the design community with a cost-effective means for implementing the digital and analog sub-blocks of the receiver into a single chip, especially for standards like wireless local-area netork (WLAN) where sensitivity requirements aren't very stringent [1]. However, the implementation of the RF front end [consisting of the band-pass-filter (BPF) and the low noise amplifier (LNA)] in silicon has proved to be an extremely difficult task. This is primarily because of the lack of on-chip high-Q passives.

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A survey of work done in this field reveals that typical Q_s for on-chip inductors in ordinary silicon CMOS processes tend to be less than 15 [2]. The thin aluminum metal layers and the lossy nature of silicon lead to higher parasitics for on-chip inductors, which makes the design of filters and LNAs for high sensitivity applications like long-distance communication protocols next to impossible. Table I ([3]–[8]) shows examples of CMOS LNAs published over the last few years; none of them are completely integrated solutions and they all require external discrete passives for completing the circuit.

Developments in packaging technology have led to a second option for integration, the system-on-package (SOP) approach. Unlike SOC where the package exists just for the thermal and mechanical protection of the integrated circuits (ICs), SOP provides for an increase in the functionality of the IC package by supporting multiple chips and embedded passives [9]. Depending on the packaging technology used, there are three main approaches for SOP integration; namely

1) low-temperature co-fired ceramic (LTCC) [also known as multichip module ceramic (MCM-C)] [10];
2) multichip module deposition (MCM-D) [11];
3) multichip module laminate (MCM-L) [12].

The dielectric materials and highly conductive copper layers of these packaging substrates makes high-Q embedded inductors and capacitors possible ([10], [12], [13]). This in turn leads to the possibility of implementing completely integrated LNAs at the package level.

Though many papers have reported optimization techniques for CMOS LNAs ([4], [14]), all of them have assumed the use of external inductances with fixed Q_s. However, with the use of embedded passives, designers now have the flexibility of choosing the Q required for a particular circuit component and treating it as a new design variable in the optimization process. This paper presents a novel optimization strategy for integrated CMOS LNAs, with simultaneous optimization of transistor and inductor sizing in the IC and the package for minimal noise figure (NF) and device size.

System integration at the package level can lead to the use of multiple embedded passives in the packaging substrate, which can generate undesirable resonance and feedback in the circuit. Due to the small electrical sizes involved, some of these effects can be ignored for on-chip system implementations. Even for issues such as feedback that are common for both on-chip and package implementations, the mechanism for signal coupling

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TABLE I
SURVEY OF PAST WORK ON CMOS LNAS FOR LONG-DISTANCE COMMUNICATIONS PROTOCOLS

Author	Year	Frequency (GHz)	Technology	NF (dB)	Gain (dB)	Completely Integrated?
Karanicolas et al. [3]	1996	0.9	0.5u CMOS	2.2	15.6	NO
Shaeffer et al. [4]	1997	1.5	0.6u CMOS	3.5	22	NO
Hayashi et al. [5]	1998	0.9	0.35u CMOS	1.8	14.8	NO
Floyd et al. [6]	1999	0.9	0.8u CMOS	1.2	14.5	NO
Abou-Allem et al. [7]	2001	1.9	0.5u CMOS	1.8	15	NO
Gramegna et al. [8]	2001	0.9	0.35 RFCMOS	0.85	15	NO

can be very different at the chip and package levels. Along with circuit optimization, this paper also analyzes the electrical design issues involved in integrating circuits with multiple passives embedded in a multilayered substrate. To demonstrate the feasibility for integration, LNAs integrated on a multilayered organic substrate containing embedded passives have been fabricated and tested in this paper.

The paper is organized as follows: Section II discusses the contribution of finite inductor Q_s to the NF of a CMOS LNA circuit. Section III provides details on an optimization strategy for LNAs depending on NF and size requirements. Section IV describes the fabrication of embedded inductors in organic packaging substrates and the tradeoffs involved in the design of embedded high-Q inductors. Section V discusses the design of hybrid LNAs using both discrete and embedded components, as proof-of-concept devices for high-frequency applications as well as test-vehicles to study the effect of coupling between multiple embedded passives. Section VI discusses the effect that mutual coupling between embedded passives and the ground return path layout have on the performance of the LNA and finally, Section VII summarizes the findings and outlines future work.

II. CMOS LOW NOISE AMPLIFIERS AND NOISE ANALYSIS

The low noise amplifier is the first active device of any RF front-end architecture (Fig. 1). Essential requirements of this amplifier circuit are reasonable gain, a good input impedance match, linearity and the lowest possible NF. If the device is to be used in a portable device, the need for low power consumption also becomes important. The noise factor (F) of an LNA is a measure of the amount of noise added by the circuit to the incoming signal, and is defined as the ratio of signal-to-noise ratio (SNR) at the input of the device to the SNR at the output

$$F = \frac{(\mathrm{SNR})_{\mathrm{in}}}{(\mathrm{SNR})_{\mathrm{out}}} = \frac{\overline{v_{ni}^2}}{\overline{v_{tx}^2}} \tag{1}$$

where $\overline{v_{ni}^2}$ is the total noise power at the output referred to the input, and $\overline{v_{tx}^2}$ is the thermal noise power produced by the source resistance (typically 50 Ω). The noise figure is F expressed in decibals.

Though many topologies exist for LNA design, the cascode architecture of Fig. 2 has been used widely for its low NF and high input-output isolation [4]. The design process for the inductively degenerated LNA consists of sweeping the NF with respect to transistor (M1) gate width. Using the RF CMOS model

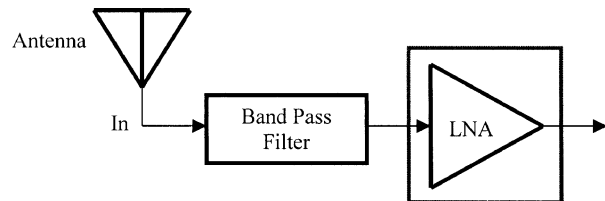


Fig. 1. Typical wireless receiver front-end.

described in [15], the input impedance of the LNA can be calculated as

$$Z_{\mathrm{in}} = R_g + R_s + R_{\mathrm{gate}} + R_{\mathrm{ch}} + \frac{g_m L_s}{C_{\mathrm{GS}}} - jR_s g_m \sqrt{\frac{L_T}{C_{\mathrm{GS}}}} + j\omega L_T - \frac{j}{\omega C_{\mathrm{GS}}} \tag{2}$$

where R_g and R_s are the parasitic resistances of the inductors at the gate and source, respectively, R_{gate} is the resistance of the polysilicon gate, R_{ch} is the channel resistance, g_m is the transconductance, C_{GS} is the gate-source capacitance, ω is the angular frequency and L_T is the sum of inductances L_s and L_g. If the parasitic resistances (R_g, R_s and R_{gate}) can be ignored, the real part of the input impedance can be controlled by choosing appropriate values for L_s and can be set to equal the source resistance for impedance match. The gate inductance is then chosen such that L_T resonates with C_{GS} at the operating frequency, thus canceling out all the imaginary terms and making the input impedance purely real at the frequency of operation.

Inductances can be modeled as equivalent circuits comprising of inductors, capacitors and resistors. The energy stored in the device is shared between the inductance and the parasitic capacitances, while the resistor represents the loss in the device. As such, the unloaded Q_s of the inductors are functions of the parasitic capacitances as well as the resistance. If the parasitic capacitances are very small and can be neglected, the unloaded Q_s (Q_g and Q_s) of the inductors (L_g and L_s) are related to their parasitic resistances by

$$R_g = \frac{L_g \omega_0}{Q_g} \qquad R_s = \frac{L_s \omega_0}{Q_s} \tag{3}$$

where ω_0 is the angular frequency of operation.

As mentioned earlier, several papers have discussed optimization strategies for CMOS LNAs ([4], [14]). All of these design methodologies have assumed fixed Q_s for the inductors. An SOP approach that provides embedded inductors in the package substrate allows the designer an extra design variable, namely,

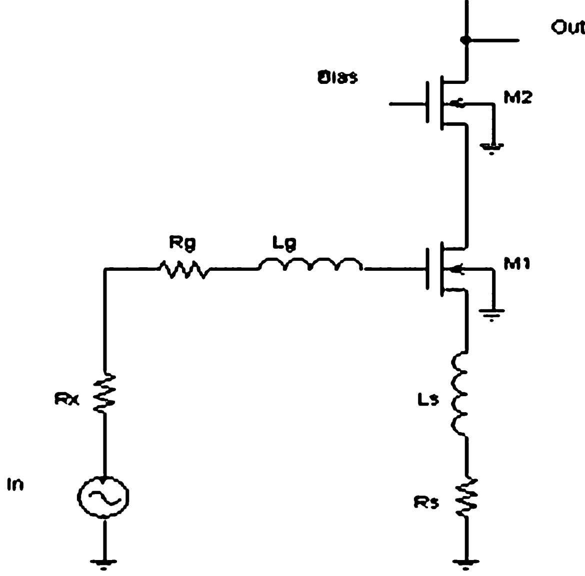


Fig. 2. LNA with inductive degeneration. R_g and R_s are parasitic resistances of the inductors L_g and L_s. The bias circuitry has not been shown for simplicity's sake.

the Q of the inductors. Depending on their contribution to performance specifications like NF and gain, any or all of the three inductors in the LNA circuit can be implemented on-chip or embedded in the package. However, attaining a particular Q also comes with tradeoffs in size and layout. In order to incorporate these into the optimization methodology, it is necessary to derive F as a function of R_g and R_s.

The output current of the LNA (i_o) can be defined as

$$i_o = G_{mg}(v_i + v_{ng}) + G_{ms}v_{ns} + A_{ig}i_{ng} + A_{id}i_{nd} \quad (4)$$

where v_i is the input voltage, v_{ng} is the total noise voltage at the gate, v_{ns} is the total noise voltage at the source, and i_{ng} and i_{nd} are the gate and drain noise currents of the transistor M1. In the above equation, G_{mg}, G_{ms}, A_{ig}, and A_{id} are the system gains associated with the different voltage and current sources respectively. Since the output current i_o is also given by

$$i_o = G_{mg}(v_i + v_{ni}) \quad (5)$$

(where v_{ni} is the total noise voltage in the field effect transistor (FET) referred to the input), combining (4) and (5) results in

$$v_{ni} = v_{ng} + \frac{G_{ms}}{G_{mg}}v_{ns} + \frac{A_{ig}}{G_{mg}}i_{ng} + \frac{A_{id}}{G_{mg}}i_{nd}. \quad (6)$$

Including all the noise contributions of the FET and that of the parasitic resistances of the inductors, F can then be derived from (1) as (7) shown at the bottom of the page [16], where R_x is the source resistance, which is typically 50 Ω, β and γ are bias dependant noise parameters of the MOSFET, and g_{do} is defined as the drain output conductance evaluated at $V_{ds} = 0$ V. In (7), c is the correlation coefficient between the drain and gate noise currents of the FET.

III. Design Optimization

Equation (7) shows that F is equally dependent on the parasitic resistances of both gate and source inductors (R_g and R_s). However, in practice, L_s is much smaller than L_g. Values of inductance required for L_s are typically less than 2 nH, and this can be implemented as an on-chip or bond-wire inductance whose parasitic resistance can be neglected. By careful layout, the resistance of the polysilicon gate can also be made very small [4]. However, depending on the frequency of operation, L_g can be as high as 35 nH. The parasitic resistance of $L_g(R_g)$ is hence a very important contributor to the F of the LNA. As it is impossible to implement this inductor on-chip, an optimum solution is to embed it in the package.

Fig. 3 shows the variation of NF with respect to transistor gate width (W), for different values of Q_g, for a 1.9 GHz CMOS LNA designed for the AMI 0.5-μm CMOS process. As can be observed, there exists an optimum gate width where the NF is minimum. However, this minimum NF shifts upwards as the value of Q_g is decreased. It is also important to note that this change is not a linear function of Q_g; the improvement in NF with an improvement in Q_g is much more apparent at low values of Q_g. Current design methodologies suggest designing circuits assuming infinite Q, and then using inductors with highest possible Q. This is not a very satisfying strategy, as there are always tradeoffs involved in achieving high Q_s during inductor design. The nonlinear variation of NF with Q_g provides the scope for an optimization methodology.

The Q of an inductor is a function of the signal loss within the device. The losses in an inductor consist of two components, namely, losses in the metal and losses in the substrate. It has been shown in [12] that the inductor can be optimized for maximum Q at the frequencies of interest (1–3 GHz). Under these conditions, conductor losses dominate the total loss (and hence the Q). The conductor losses can be reduced by increasing the metal thickness and conductor width (which reduces the series resistance), leading to an increase in size of the inductor, thus allowing for the tradeoff of larger size for higher Q.

By using embedded inductors in place of chip-inductors for L_g, the designer has control over the required unloaded Q for this inductor. However, due to the tradeoff with respect to size,

$$F = 1 + \frac{R_g}{R_x} + \frac{R_{\text{gate}}}{R_x} + \frac{R_s}{R_x} + \frac{\beta\omega_0^2C_{\text{GS}}^2\left(\omega_0^2L_T^2 + (R_x + R_g + R_{\text{gate}} + R_s)^2\right)}{5R_xg_{do}} + \frac{2c\omega_0^2C_{\text{GS}}^2(R_x + R_g + R_{\text{gate}} + R_{\text{ch}} + R_s)(R_x + R_g + R_{\text{gate}} + R_s)}{g_mRx}\sqrt{\frac{\beta\gamma}{5}} + \frac{\omega_0^2C_{\text{GS}}^2(R_x + R_g + R_{\text{gate}} + R_{\text{ch}} + R_s)^2}{g_m^2}\frac{\gamma g_{do}}{R_x} \quad (7)$$

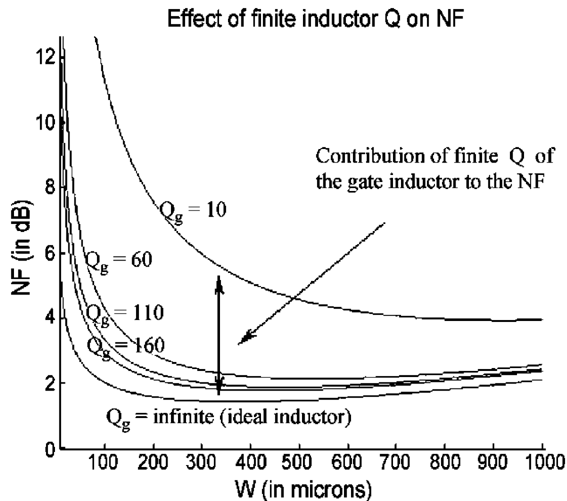


Fig. 3. Variation of NF with transistor width (for different values of Q_g), for a 1.9-GHz CMOS LNA designed for the AMI 0.5-μm CMOS process.

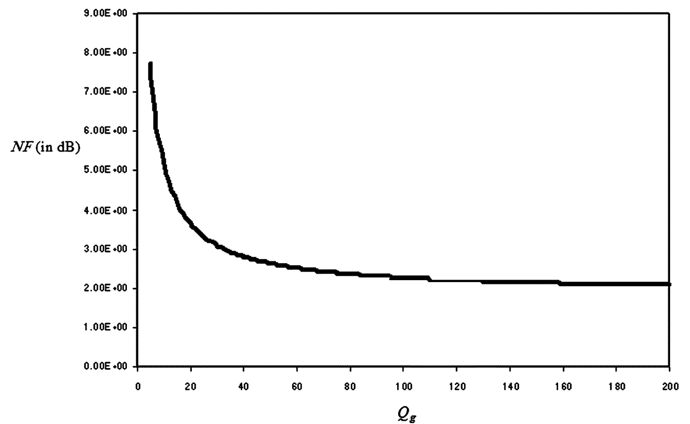


Fig. 4. Variation of NF with Q_g, for a 1.9-GHz CMOS LNA designed for the AMI 0.5-μm CMOS process.

using inductors with the maximum Q possible is not a good strategy and could lead to unnecessarily large sizes for the packaged LNA.

Equation (7) can be used to find the optimum Q_g, required for a particular NF. Fig. 4 shows the variation of NF for the optimum transistor gate width. NF decreases rapidly for increasing Q_g at low values of Q_g, but the rate of change decreases at higher values of Q_g. Hence, there is very little reduction in NF beyond a certain inductor Q. Equation (7) and Fig. 4 provides the minimum tolerable inductor Q required for satisfying the sensitivity requirements of a particular circuit. For protocols like Bluetooth and WLAN where the NF requirements are comparatively relaxed, even a Q of 25 is sufficient to achieve a NF <3.5 dB. Higher Q_s (60–80) are required to meet the specs of long distance communication protocols like global system for mobile communications (GSM) and wideband code-division multiple-access (W-CDMA).

Taking the partial derivative of F [in (7)] with respect to Q_g, results in

$$\frac{\partial F}{\partial Q_g} = -\frac{L_g\omega_0}{Q_g^2}\left[\frac{1}{R_x} + (2K_1+K_3)\left(R_x + R_{\text{gate}} + R_s + \frac{L_g\omega_0}{Q_g}\right) + (2K_2+K_3)\left(R_x + R_{\text{gate}} + R_{\text{ch}} + R_s + \frac{L_g\omega_0}{Q_g}\right)\right] \tag{8}$$

where

$$K_1 = \frac{\beta\omega_0^2 C_{\text{GS}}^2}{R_x g_{do}} \quad K_2 = \frac{\gamma g_{do}\omega_0^2 C_{\text{GS}}^2}{R_x g_m^2} \quad K_3 = \frac{2c\omega_0^2 C_{\text{GS}}^2\sqrt{\gamma\beta}}{R_x g_m}. \tag{9}$$

Equation (8) can be used to find the optimum Q_g required, at which the rate of decrease of NF meets a certain value.

IV. Embedded Passives—Optimum Q With Minimum Size

Embedded inductors and capacitors have been demonstrated on MCM-L technology developed at the Packaging Research Center, Georgia Institute of Technology [12]. The PWB/packaging substrate on which these devices were fabricated was processed by laminating a low-cost epoxy based layer, Dupont Vialux, on a conventional 28 mil ($\sim$700 μm) printed wiring board (PWB) core, N4000-13. This resulted in a two-metal layer process, which was sufficient for the design of parallel plate capacitors and under-routing capabilities. The process also offers microvias (with 100-μm diameters), which are important for the realization of minimum size passives in multilayered substrates. The first metal layer thickness was limited to half the laminate layer thickness of 25 μm for ensuring a uniform dielectric layer thickness. The top metal layer was restricted to 15$\sim$17 μm to ensure uniform metal thickness. The vendor supplied data for the two layer substrate were as follows: Dupont Vialux had a dielectric constant of 3.3 and loss tangent of 0.015 at 1 GHz and N4000-13 had a dielectric constant of 3.7 and loss tangent of 0.015 at 1 GHz. Fig. 5(b) shows the cross section of the substrate.

Inductors and capacitors were optimized for maximum Q at the appropriate frequency. Fig. 5(a) shows the top view of a 4 in $\times$ 4 in quadrant of the substrate with inductors and capacitors. Table II provides measured results for passives realized in the above technology. Microstrip type inductors use signal lines referenced to a ground directly underneath the device. With the given organic process, it was possible to have minimum line widths of 3 mils and a maximum ground to signal separation of 29 mil [Fig. 5(b)]. In coplanar waveguide (CPW) inductors, signal lines are referenced to ground rings on the same metal layer as the device. Although this eliminates the need for backside connections, it results in an increase in the area of the device. The CPW topology reduces current crowding on the ground planes (which is typical in microstrip type inductors), by forcing the currents to flow around the device in the larger area coplanar ground. Inductors with Q_s as high as 170 have been demonstrated, as shown in Table II.

Lumped model equivalents for one-port inductors fabricated using the organic process are shown in Fig. 6. The series inductance, L_s, and the series resistance, R_s, represent the inductance and resistance of the inductor and under-routings respectively. The overlap between the inductor and the underpass allows direct capacitive coupling between the two terminals of the inductor. This feed-through path is represented by the series capacitance C_s. Components C_p and R_p capture the shunt capacitance and conductance between the inductor and the ground reference.

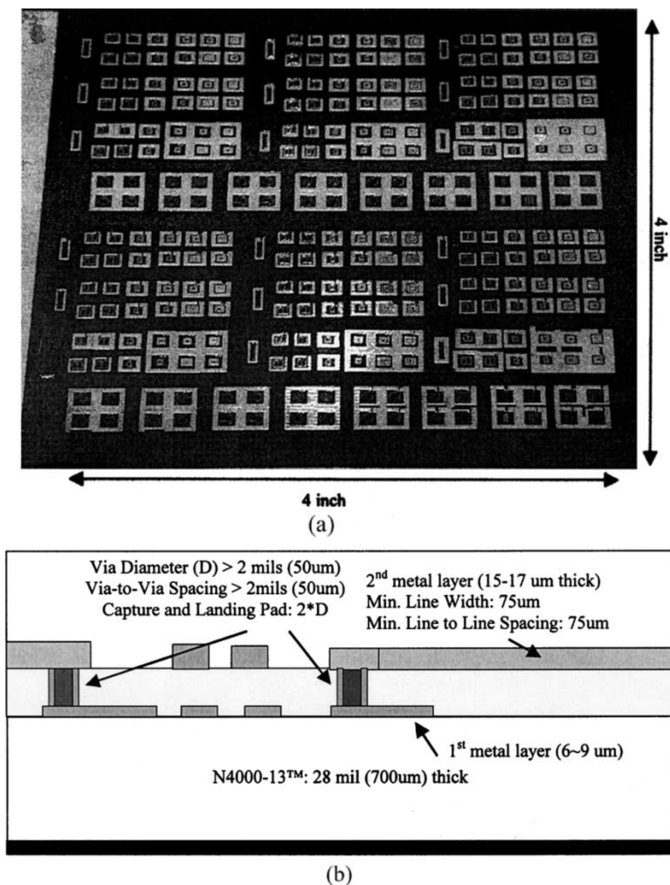


Fig. 5. (a) Photograph of fabricated passives. (b) MCM-L substrate cross section.

TABLE II
MEASUREMENT RESULTS FOR PASSIVES ON ORGANIC SUBSTRATES

Inductors	Max Q	Inductance	SRF	Area (mm^2)
CPW Circular Large	160 @ 1.8 GHz	16nH	>3.6GHz	25
CPW Circular Small	170 @ 2.2 GHz	9nH	>4.5GHz	28
1 turn microstrip	170 @ 2.4 GHz	1.6nH	>5GHz	3.5
2 turn microstrip	110 @ 2 GHz	5nH	> 5GHz	4.1
3 turn microstrip	100 @ 1.2 GHz	12nH	>3GHz	3
1.75 loop microstrip	110 @ 2.1 GHz	7.7nH	>4.3GHz	4
2 loop CPW	110 @ 1.8 GHz	9nH	>3.6GHz	9
2by2 loop CPW	80 @ 1.8 GHz	14nH	>3.6GHz	9
1.75 loop CPW	150 @ 2.2 GHz	5 nH	>4.5 GHz	9
Capacitors	**Q at 2GHz**	**Capacitance**	**SRF**	**Area (mm^2)**
Parallel Plate	33	0.92pF	>6GHz	0.6
Parallel Plate	30	1.78pF	>6GHz	1.16
Parallel Plate	28	2.72pF	>5GHz	1.87

Table II also provides measurement results for parallel plate capacitors. Compared to the inductors, the capacitors exhibit lower Q values. This is because the upper limit for the Q factor for any size capacitor implemented on this substrate at a particular frequency, ignoring conductor loss, can be approximated using $1/\tan\delta$, where $\tan\delta$ is the loss tangent of the material at the particular frequency. The Q factor is further reduced by the conductor loss. Compared to the dielectric materials used in common LTCC ($\tan\delta$ of 0.0015 at 10 MHz [10]) and MCM-D ($\tan\delta \sim 0.0008$ [11]) processes for embedding passives, the materials used in this buildup process are lossy ($\tan\delta \sim 0.015$). This sets the maximum Q possible for capacitors in the process at $\sim$65.

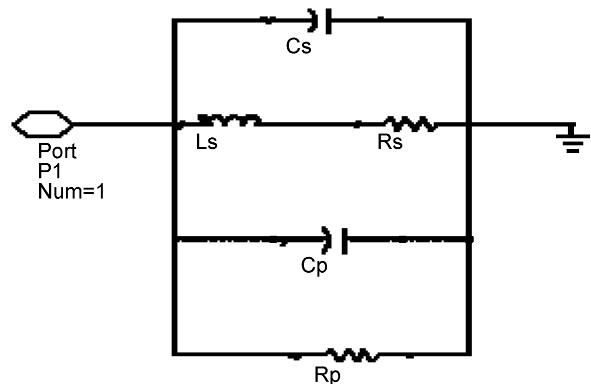


Fig. 6. Inductor lumped-element model.

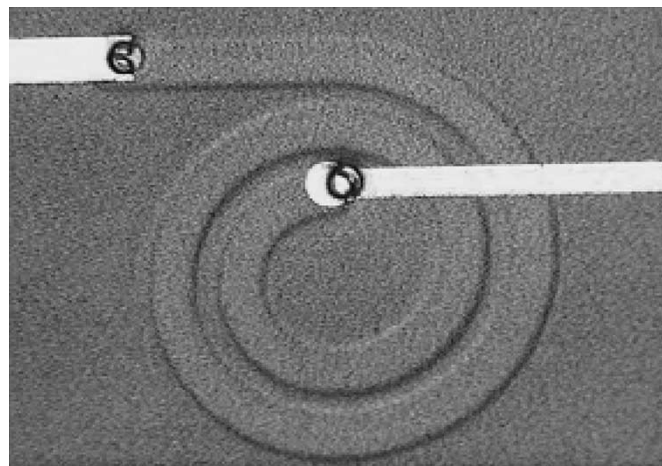


Fig. 7. Photograph of the fabricated inductor (the CPW ground ring around the inductor is not shown).

The variation in Q for two inductors with the same topology and inductance but different areas can be explained based on the model of Fig. 6—the smaller inductor has larger series resistance and smaller parallel resistance compared to the larger inductor, and this results in a lower value of Q for the smaller inductor. An inductor can be made smaller (in size) by increasing its proximity to the reference ground. However, this directly decreases the inductance per unit length due to the negative mutual inductance with the ground plane. Thus, there is an increase in series resistance for a physically smaller inductor due to the increase in the length required to achieve the same inductance compared to a larger inductor.

Fig. 7 shows photograph of a spiral inductor fabricated on an organic substrate (the CPW ground ring around the inductor is not shown in the figure). There are several design variables for this inductor topology, namely the inner diameter, distance between the signal trace and the CPW ground, trace width, spacing between traces and number of turns. As an example to demonstrate the variation of Q with inductor area, three single-turn inductors were designed for the same inductance ($\sim$7.8 nH) value. Table III shows the area and Q (measured at 1.83 GHz) for these inductors. As can be observed, for a given topology (inductor shape and number of turns), there is an increase in Q with increase in device area.

Fig. 8 shows the variation of inductor area and NF with Q_g, for an LNA designed using these inductors. The dotted line rep-

TABLE III
VARIATION OF INDUCTOR Q WITH AREA

Inductance (nH)	Q	Area (mm^2)
7.81	48.81	14.747
7.82	70.897	17.743
7.81	85.52	18.92

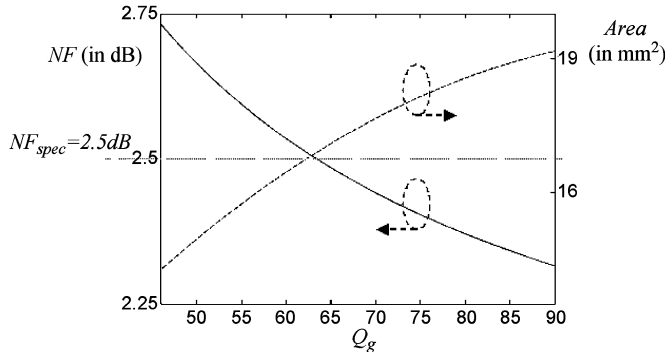


Fig. 8. Variation of inductor area and NF with Q_g.

resents the specification for NF, which in this case was 2.5 dB. The NF versus Q_g curve shows that the minimum inductor Q required to meet this specification is 64. The Area versus Q_g curve is then used to determine the minimum size for the inductance that provide this Q (which in this case was $\sim 17\ \mathrm{mm}^2$).

As an example of the chip-package co-design methodology discussed in this paper, an LNA for GSM applications was designed for AMI's 0.5-μm CMOS technology, with a standard source resistance of 50 Ω and an operating frequency of 1.9 GHz, leading to inductance values of 9 and 1.2 nH for L_g and L_s, respectively. L_s was small enough to be implemented on-chip; however, L_g was too high to be implemented on-chip without a drastic increase in the NF of the circuit. Plotting the NF of the LNA versus its gate inductor Q, the NF decreases from about 5.2 to 2.1 dB as the Q of the gate inductor is increased from 10 to 200. However, on designing, fabricating and measuring different topologies for the gate inductance, it was found that its size increased from 9 mm^2 for a Q of 110 to 28 mm^2 for a Q of 170. Since the NF of the LNA was not affected for an increase in Q_g beyond 70–90 and since size constraints limited the packaged device to an area of 3.5 mm $\times$ 3.5 mm, the inductor that provided optimum Q for a minimum size was chosen.

Fig. 9 shows the chip and package layouts of the proposed LNA, along with simulated gain and NF numbers. The embedded inductor has a two-loop CPW topology, occupies 9 mm^2 of area, and has a Q of 110. The package uses a six metal layer organic packaging technology, with the inductor designed using metal layers two and three. Metal layer 1 contains pads for chip attachment. The components of the equivalent circuit model (Fig. 6) for this inductor were extracted from measurements, which translate to a series inductance (L_s) and resistance (R_s) of 7.4 nH and 0.4 Ω, respectively, and a parallel resistance (R_p) and capacitance ($C_s + C_p$) of 27 kΩ and 0.15 pF, respectively. Fig. 9(b) shows the measured variation in Q with frequency for this inductor. It is important to note that this data has been obtained using inductors fabricated on lossy organic substrates.

V. HYBRID LNA DESIGN AND MEASUREMENTS

With higher levels of system integration, multiple passives embedded in the package are necessary. For example, the phase noise of a voltage-controlled oscillator (VCO) is inversely proportional to the Q of the LC tank circuit ([17], [18]). An SOP-based receiver could then contain embedded passives for both the LNA and VCO. As mentioned earlier, multiple embedded passives in the package leads to system-level issues like feedback and resonance, many of which are not apparent in an SOC implementation. To study these and as proof-of-concept devices for the use of embedded passives in organic technology for high-frequency applications, hybrid LNAs using a combination of discrete and embedded passives were designed for the packaging technology described in the previous section. The circuits were designed for use in the 2.1-GHz and 2.4-GHz frequency bands.

The classical LNA architecture consists of an active device with impedance transformation networks at the input and output. The NF is mainly affected by the noise characteristics of the transistor and the input impedance matching network. Generally, the source impedance required by the active device for minimum NF is different from the complex conjugate of the input impedance obtained looking into the base/gate of the device (the optimum impedance for maximum power transfer). This means that it is usually not possible to simultaneously achieve both maximum gain and minimum noise figure for an amplifier, and that some compromise has to be made. In addition to gain and NF, stability is also an important factor in amplifier design. This again requires careful choice of source and load impedances, so that the amplifier does not move into the unstable region of operation. The selection of the optimal source impedance Z_{opt} is achieved by plotting constant NF circles and constant gain circles along with stability circles on a Smith chart. The input impedance transformation network transforms the source impedance (typically 50 Ω) to $\mathrm{Z}_{\mathrm{opt}}$. The output impedance transformation network transforms the impedance at the collector/drain of the active device to 50 Ω for maximum power transfer.

Fig. 10 shows the schematic of the LNA, using a discrete HBFP-0420 dual emitter transistor in a SOT-343 package and the impedance transformation networks implemented using high-Q embedded inductors and capacitors. The transistor is biased in the common emitter configuration.

The input and output of the transistor were matched to 50 Ω by using L–C pi networks, which were embedded in the package. Though "L" networks are sufficient for a narrow-band impedance transformation, the goal was to study the layout issues and interaction between multiple embedded passives. A decision was therefore taken to maximize the number of embedded devices in the system. The output pi was designed for maximum power transfer, and thus performs impedance transformation from the complex conjugate of the collector impedance to 50 Ω. The input pi was designed for minimum noise figure, and presents the Z_{opt} to the gate of the transistor.

The pi networks were designed using SONNET, which is a commercial 2.5D method-of-moments solver. As shown in [16], unloaded Q_s of 60–80 for the passives were sufficient to attain

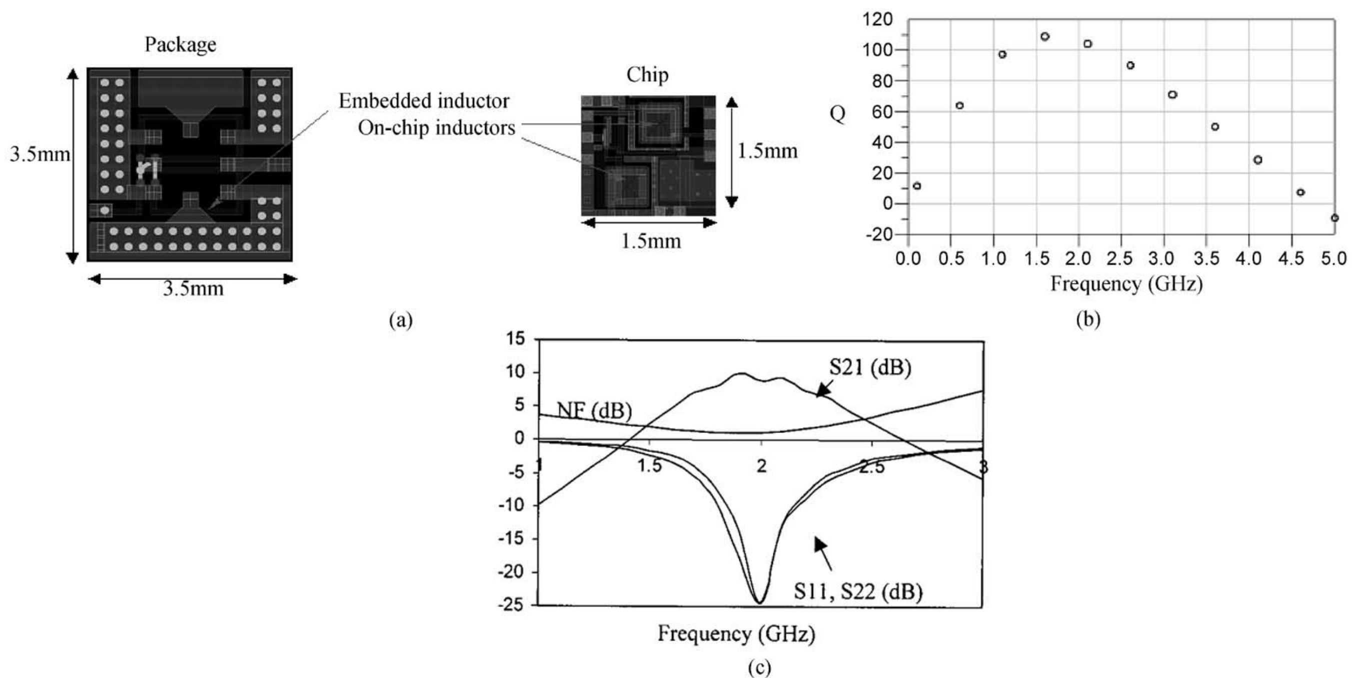


Fig. 9. (a) Chip and package layouts of the proposed integrated LNA, (b) measured Q values for the inductor used (9 nH, two-loop CPW topology), and (c) simulated gain and NF numbers.

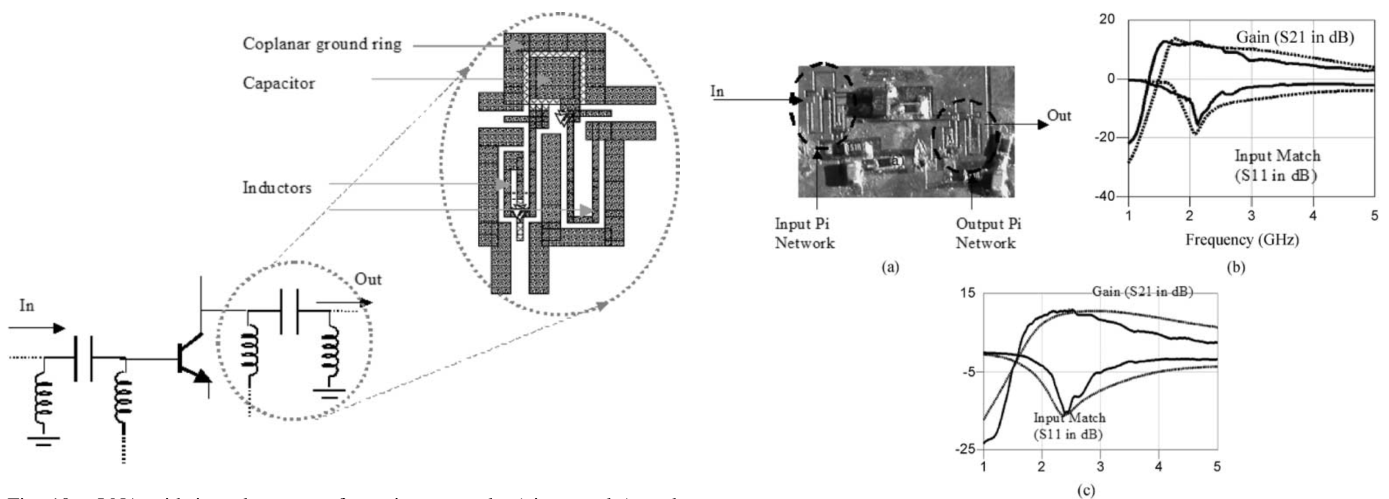


Fig. 10. LNA with impedance transformation networks (pi networks), and implementation of the output pi using embedded passives.

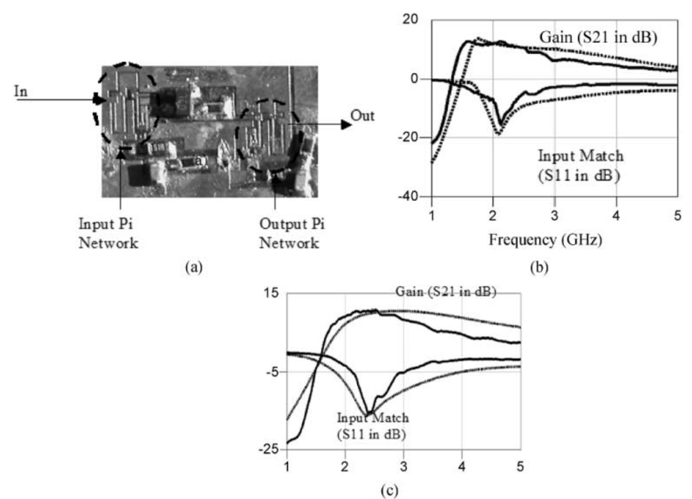


Fig. 11. (a) Photograph of a fabricated LNA. (b) and (c) Modeled and measurement data for LNAs operating at 2.1 and 2.4 GHz, respectively (the dotted line represents the modeled data and the continuous line represents the measured values).

near-minimum noise figure. Although Q_s greater than 150 were achieved in [12], the designs occupied $> 9\ \mathrm{mm}^2$ of the surface area. The design of inductors in this paper was constrained to a maximum surface area of 2 mm^2 and the overall pi area to less than 6 mm^2.

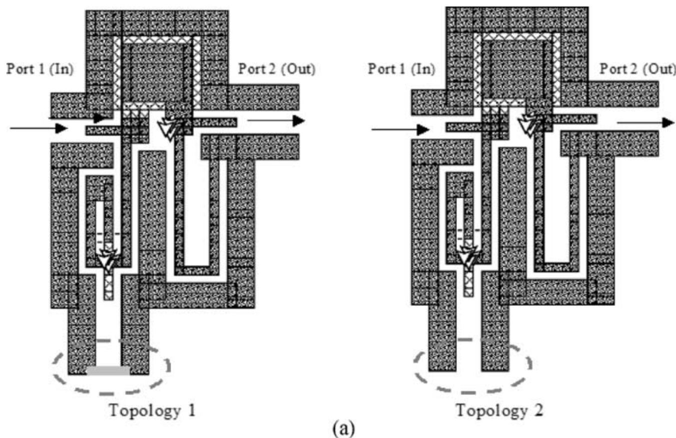
Fig. 11 shows the photograph of one of the fabricated LNAs, as well as the measured gain (S_{21}) and impedance match (S_{11}) values for two different amplifiers operating in the 2.1 GHz and 2.4-GHz frequency bands. The circuits occupied 1.4 cm^2 in area. The first amplifier, designed for WCDMA applications, shows a gain of 12.74 dB and an input match of -14.01 dB at 2.1 GHz. The second amplifier, designed for Bluetooth applications, shows a gain of 10.5 dB and an input match of -13.772 dB at 2.4 GHz. The plots show good correlation between measured and modeled data. However, as will be explained in more detail in the next section, it was necessary to account for coupling between the input and output pi's to achieve the results shown. Table IV shows the performance summary of the two amplifiers.

VI. Importance of Ground Return

Circuits with multiple passives have the problem of coupling between the passives. This can lead to feedback, instability and an overall degradation of the circuit performance. In circuits where passives are in close proximity (inside a chip, for example), coupling is mostly magnetic in nature [19]. However, in electrically larger circuits like the LNAs described above, the passives are sufficiently far apart to prevent direct magnetic coupling. Feedback is mostly caused by return currents in such

TABLE IV
LNA PERFORMANCE SUMMARY

LNA	Circuit 1	Circuit 2
Frequency	2.1 Ghz	2.44 GHz
Gain (S_{21})	12.74 dB	10.5 dB
Input Match (S_{11})	-14.01 dB	-13.772 dB
NF (simulated)	2.5 dB	2.8 dB
P_{-1}	-8.9 dB	-9.2 dB
Supply Voltage	3.5 V	3.5 V
Supply Current	7 mA	7 mA



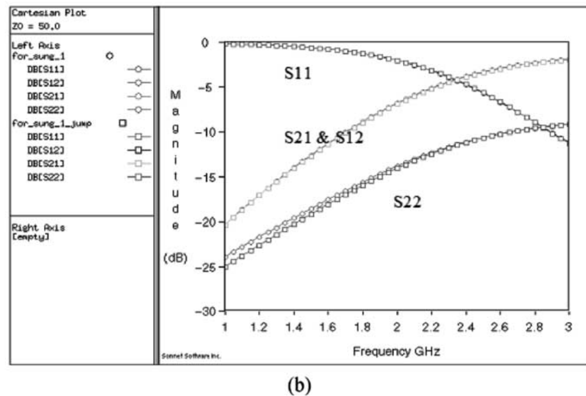


Fig. 12. (a) Two reference ground layout topologies for the output pi. (b) SONNET simulations for both layouts.

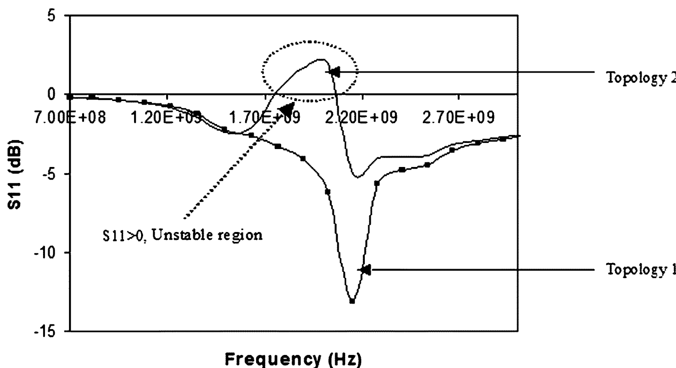


Fig. 13. Measured S_{11} values for amplifier circuits using the two pi topologies of Fig. 12(a), showing the effect of the reference ground layout on LNA performance.

cases. In either case, the relative placement of the passives and their reference grounds becomes a crucial design issue.

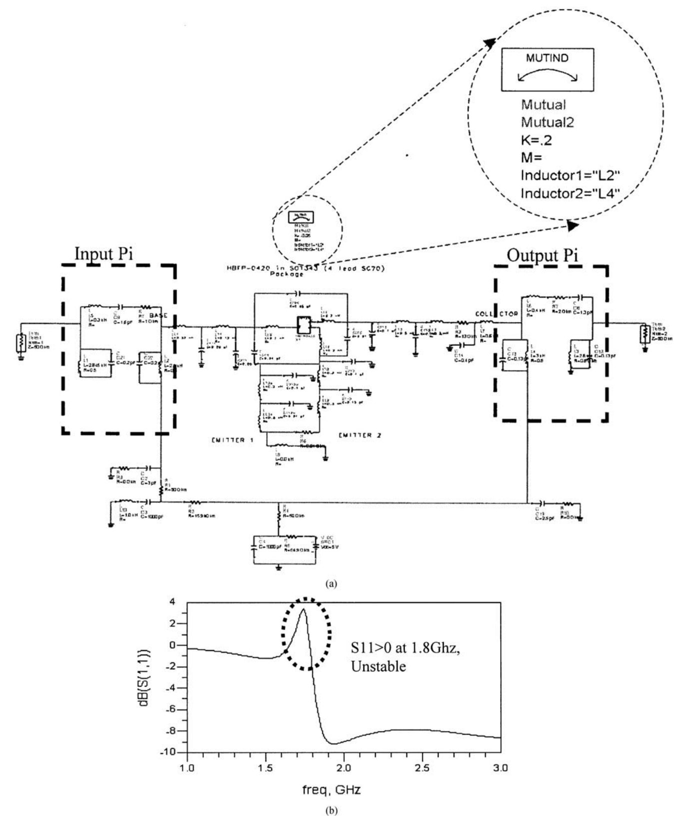


Fig. 14. (a) ADS circuit model for the LNA, along with the mutual inductance that was necessary to model the instability. (b) Modeled (ADS) S_{11} results showing instability.

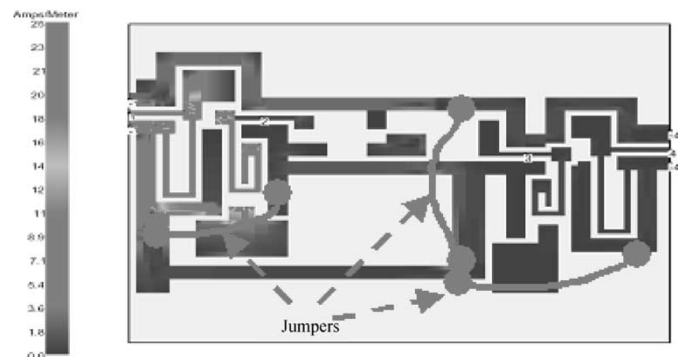


Fig. 15. SONNET simulations of the unstable LNA layout, with the use of jumpers for current rerouting.

To study the effect of ground return current, pi's with different reference ground layouts were modeled and implemented, and their effect on the LNA performances was analyzed. Fig. 12(a) shows two of the topologies used to implement the output pi and Fig. 12(b) shows the SONNET simulations for both the pi layouts. As can be observed [in Fig. 12(b)], for the frequency band of interest, there is minimal difference in the S-parameters for the two topologies. However, Fig. 13 shows the measured response of the amplifier circuits for the two pi topologies. The change in routing for Topology 2, caused the amplifier to move into the unstable region of operation, which could not have been predicted by simply simulating the pi's alone using full-wave electromagnetic solvers. The instability is caused due to the influence of return currents on the transistor circuit.

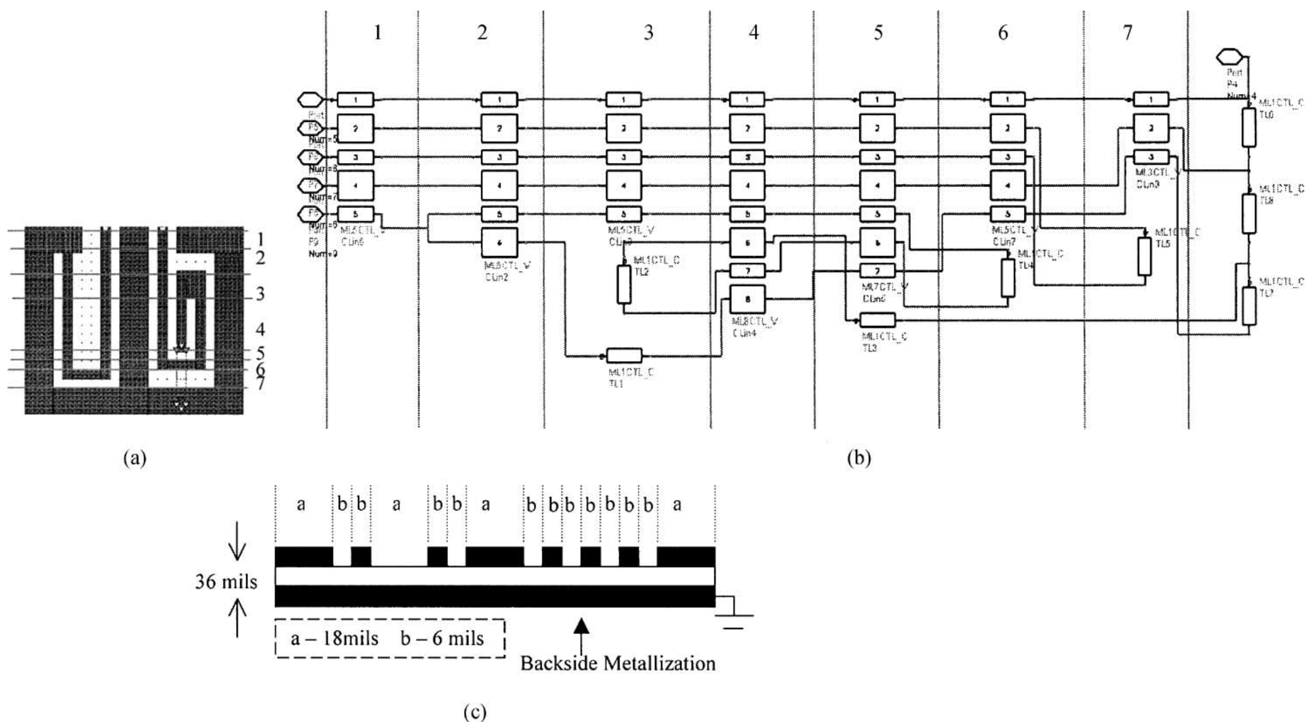


Fig. 16. Coupled-line modeling of two inductors. (a) Layout and segmentation of the inductors. (b) ADS multilayer coupled line model of the inductors. (c) Cross section of one of the segments (Segment 4).

With layout of the reference ground resulting in such drastic changes in system performance, it becomes necessary to model its effect at the design stage, so that any system level instability problems can be identified and rectified. This involves the incorporation of the reference ground layout into the design and simulation methodology.

A. Modeling—Field Solvers

Field solvers like HFSS and SONNET can be used to obtain an n-port S parameter file for the entire layout, which can then be used in a circuit based simulation tool like Agilent ADS. However, current modeling tools do have limitations when providing solutions for internal ports, especially for devices configured in a CPW topology as discussed in this paper. Instead, the effect of the reference ground layout can be modeled as a mutual inductance between the inductors of the input and output pi's, with the coupling coefficient depending on both spatial orientation of the circuit components as well as the return current paths.

SONNET simulations of the complete layout for the unstable LNA. showed considerable coupling between the input pi and one of the inductors of the output pi. The reference ground layout (and hence the return current path) for pi Topology 2 resulted in current crowding and signal coupling between the input and output pi's, leading to positive feedback and instability. The ratio of the current densities in the input and output pi's translated to a coupling coefficient of $\sim$0.2, which, when used in ADS, modeled the instability (Fig. 14). With rerouting of the excess current to prevent coupling (through the use of jumpers), it was possible to stabilize the amplifier. It is important to note that the second SONNET simulation of the same layout (Fig. 15), now with better ground routing through the use of jumpers, exhibits a coupling coefficient of less than 0.05. Measured results for this LNA showed stable operation and a gain of 12 dB at 2.1 GHz, proving that the instability in the earlier case was indeed because of return current routing. Through the use of jumpers at appropriate locations, the coupling between the pi networks could therefore be minimized.

B. Modeling—Using Transmission Lines

Electromagnetic solvers take long computation times, and this further increases as the number of ports is increased. This makes it difficult to use tools like SONNET to model the mutual inductance in circuits at the design phase, when multiple simulations are required for optimizing the layout. For example, computing the coupling coefficient in the previous example at six frequencies using SONNET required twelve minutes of simulation time on a Sunblade 1000 workstation. To reduce computation time, a circuit based modeling methodology was also used, based on transmission line theory [20].

Modeling each pi network as an equivalent circuit consisting of two inductors and one capacitor makes it difficult to model the effect of the reference ground layout. Non-idealities in the ground distribution were therefore analyzed by segmenting the structure into various coupled line sections [21]. Fig. 16 shows an example of the segmentation of two inductors (in CPW configuration) into several coupled line sections. Fig. 16(b) shows the layout of the inductors unfolded into a cascaded structure of coupled lines. Each individual transmission line segment was defined by referencing it to the backside metallization of the packaging substrate. Fig. 16(c) shows the cross section of segment 4. The multilayer coupled line models (e.g. ML5CTL_V, ML1CTL_C, etc.) in ADS were used to

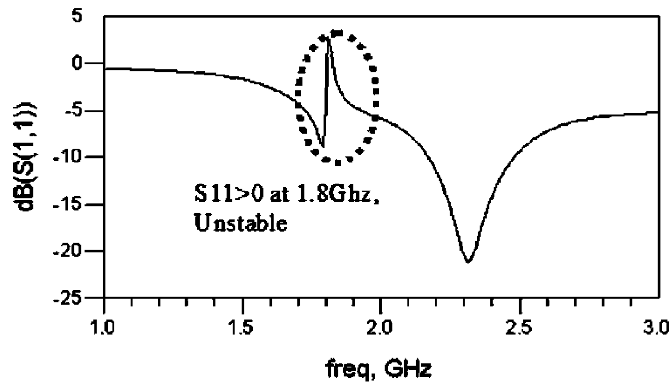


Fig. 17. Modeled (ADS) S_{11} results showing instability.

obtain the complete circuit model, with both signal and ground structures modeled as transmission line segments referenced to the backside metallization.

Fig. 17 shows the modeled instability (in ADS). The circuit-based model was able to predict the frequency of instability, at the same time reducing the computation time by an order of magnitude (80 s) as compared to modeling using SONNET. It is to be noted here that this modeling methodology is valid only at low frequencies (<5 GHz). The accuracy of coupled-line modeling decreases as the ratio of the wavelength to the thickness of the dielectric decreases. The effect of discontinuities is also much higher at high frequencies. In addition, the model was successfully applied only for predicting the frequency of instability, and not its amplitude.

VII. Conclusion

The use of high-Q passives embedded in the packaging substrate provides an opportunity for achieving complete system-level integration. Unlike discrete passives (with fixed Q_s) and on-chip inductors (with very low Q_s), the use of embedded inductors in the package (with a range of Q values from 20 to 170) results in the availability of a new design variable, namely the passive Q. However, higher inductor Q values come with the tradeoff of higher size. A novel optimization strategy incorporating the inductor Q and device size into the design methodology for integrated CMOS LNAs has been developed. It has been shown that beyond a certain inductor Q, the NF becomes almost independent of Q. This optimum Q can therefore be used to determine the optimal size of the inductor, and thus reduce the packaged device size. This methodology can be applied for designing integrated CMOS LNAs using any of the common SOP technologies. Simulations show that a completely integrated device with a gain of 10 dB and a NF of 2.2 dB can be implemented using 0.5 μm CMOS technology and an organic laminate based packaging substrate, with the packaged device measuring only 3.5 mm^2 in area.

A design and simulation methodology to integrate system level full-wave solvers into the design process for active devices with multiple embedded passives has been proposed and validated through measurement results. In addition, a computationally efficient circuit based modeling technique using coupled-line theory has also been developed, to predict the effect of coupling between multiple embedded passives in SOP based integration schemes. Hybrid LNAs using a combination of discrete and embedded components have been designed and fabricated, as test vehicles to study the effect of return current layout and coupling between multiple embedded passives on system performance. As shown in this paper, the layout of the reference ground and return current paths play a very important role in the performance of the LNA.

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