System-on-a-Package (SOP) Module Development for a Digital, RF and Optical Mixed Signal Integrated System

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Abstract

One highly integrated mixed-signal testbed has been developed to demonstrate the concept and realization of advanced System-on-a-Package concept. This experimental system, called Intelligent Network Communicator (INC), deals with three different status of the signals, digital, RF and optical, in a single packaging platform. The INC transmits and receives the high-speed digital signal and wireless signal over the embedded optical waveguide channel. After three years of development efforts, the system has been fabricated by utilizing advanced packaging and assembly processes and full functionality has been demonstrated successfully. Before the final test, each of the sub-blocks has been separately developed and tested. The test results clearly show that the developed system performance meets the design goals. The digital block generated up to 3.2 Gbps of data stream, the RF block had less than -1.5dB of insertion loss up to 6 GHz and the optical block achieved 10Gbps throughput over the embedded optical waveguide built on the low-cost organic substrate.

I. Introduction

The System-on-a-package (SOP) concept is being widely deployed as the key solution for low-cost multi-functional electronic systems. Especially, for the wired and wireless communication applications, SOP approach is more appropriate than System-on-a-Chip (SOC), because the communication modules require critical passive components that cannot be realized by IC process. The "Intelligent Network Communicator (INC)" testbed project is the symbolic showcase of SOP concept and has been driven by NSF Packaging Research Center (PRC) in Georgia Tech since 2001. [1-3] The goals and objectives of the INC System testbed were to explore new systems architectures that can be enabled by SOP technologies. All the available technologies related to micro-system development, which includes design, material, fabrication and test, are being adopted and verified through the process of building INC system hardware. The INC is composed of three functional sub-blocks: the digital, analog and optical blocks. The function of the INC is to transmit and receive the high-speed digital signals and RF signals concurrently over the optical channel. The multi-Gbps digital signal generated at the digital block is combined with the RF signal at the analog block. The combined signal is optically modulated and transferred through the embedded optical waveguide. The light wave signal is down converted to the electrical domain again and the electrical domain mixed signal is separated to the digital and RF signal by the embedded multi-layered mixed signal divider System specifications of each of the blocks has been defined to deal with their major barriers while incorporating with other blocks for single functional goal.

The system has been rigorously tested at the each of sub-system group, RF, digital and optical group in PRC. After verifying the system at the sub-system level, the overall system test has been performed. The test results clearly show that the measurement results meet the target specifications.

II. INC System Design

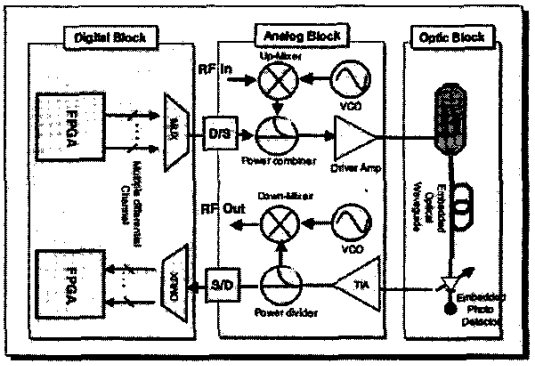


Fig.1 INC System configuration

The proposed INC system configuration is shown in fig.1. At the digital block, a multi-gigabit pseudo random digital bit sequence is generated by using FPGA and compared with the received signal after passing the analog and optical blocks. The multi-channel signals from FPGA (Virtex 50E, Xlinx) are converted into serial data stream by the transceiver IC (TLK 2701, TI), which also includes MUX, DMUX, and are fed to the analog block. The FPGA at the receiver stage compares the known input data bit stream and the recovered data from the receiver to evaluate the system performance. An FPGA is programmed to generate sixteen parallel data channel (150Mbs/c/s) which are taken by a MUX used to convert the parallel data to a 2.488 Gbs/s serial signal. This signal is the input of RF section, which is integrated into a same board. To reduce the interference from the digital part, a separated ground and power were designed. A co-planar waveguide and matching network was used for RF input and conversion of differential signal to single-ended signal.

At the analog block, two narrowband RF signals, which are generated by the Electronic Signal Generator for 802.11a/b wireless LAN signal and by the voltage controlled oscillator for 5-6 GHz range of single tone signal are being combined with the multi-Gbps digital data stream from the digital block. The high frequency component of the digital signal is truncated by the embedded low pass filter before combining. A mixed signal combiner for combining digital and RF signal is designed utilizing the multi-layer organic packaging technology. A voltage controlled oscillator IC is specially developed in MESFET process. The VCO is utilizing an embedded high-Q inductor built in the substrate to reduce the phase noise of the IC. The embedded inductor is optimized to get the best performance at 5GHz. The combined electrical signal is fed to the input of the optical modulator.

At the optical block, the RF and digital signals are modulated to the optical domain by one Mach-Zehnder modulator and a VCSEL direct modulation scheme, whose wavelengths are 1550nm and 870nm, respectively. The optical signal is initially transmitted through one multi-mode optical fiber channel and coupled into the embedded optical waveguide by the Butt coupling method. In order to integrate long (5 to 15 cm) polymer waveguides on flexible FR-4 boards that contain two metal layers separated by a low temperature insulating polymer layer, critical technical issues, which include board flexibility, long range board non-planarity and short range roughness, and coefficient of thermal expansion (CTE) matching, have to be addressed.

At the receiver end, the electrical signal is obtained by the photo detector. The electrical signal is amplified using TIA and separated by an embedded mixed signal splitter, which is identical with the combiner. The recovered digital signal is differentiated to separate channels and transmitted to another FPGA for the purpose of comparing with the transmitted signal.

III. SOP technology for INC Realization

The entire development flow including design, fabrication and test is shown in fig. 2. The INC testbed was fabricated using the PRC baseline process which had been previously characterized through extensive digital and RF design and fabrication test vehicles. The substrates utilized the thin-film build-up microvia technology on high Tg organic based substrates. This photovia dielectric has a dielectric constant 3.4 and a loss of 0.015 at 1 GHz. The build-up structure consisted of three metal layers with two staggered photovia layers. The optical waveguides were fabricated on top of the dielectric layer using photoimageable polysiloxane materials for planarization, bottom cladding, waveguide core, and top cladding layers. The ground rules used for the testbed were 10μm copper thickness, 30μm dielectric thickness, and the optical layers were typically 3-8μm thick. The first metal layer was subtractive etched and was limited to 75μm lines and spaces. Fine lines and spaces of 20-25μm were fabricated on the two build-up metal layers. The microvias were defined with UV lithography and developed to nominal diameters of 75-100μm. The optical waveguide cores were 8-50μm wide for single and multi-mode. The boards were finished with a layer of Taiyo AUS-5 liquid photo imageable solder mask (15μm thickness) and the pad finish used was electroless nickel, immersion gold for assembly of SMT components. Figure 3 shows a typical cross-section of the three metal layer build-up microvia structure used for the INC substrate. After initial substrates were fabricated and tested, additional substrates were co-developed with Endicott Interconnect (EIT, former IBM Endicott) for reliability testing.

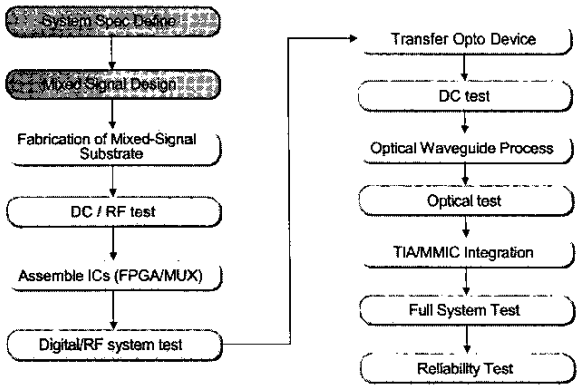


Fig. 2 INC system development flow

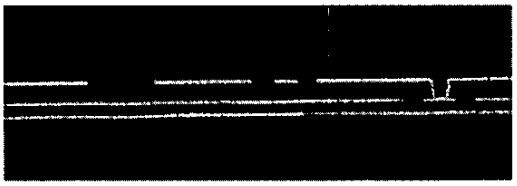


Fig. 3 Cross-sectional view of the multi-layer board with build-up microvia structure

IV. Digital Block Results

The digital block is composed of the transmitting and the receiving parts. They work as a pre- and after- processing for the communication system. The layout had to be considered carefully to reduce the interference from each other. Moreover, there were several power levels and different ground reference plane requirements in both digital and RF block. In this testbed the following techniques were used: 1) *Embedded decoupling capacitors.* The embedded capacitors were supposed to have better properties than the discrete ones with low parasitic inductance and resistance. In case the fabrication of the embedded capacitors failed, forty-two discrete decoupling capacitors were designed. 2) *Split power and ground planes.* There were three voltage levels: 3.3 V, 2.5 V and 1.8 V. A split power plane was used in the testbed. To minimize the coupling though a shared power supply, three ferrite beads were used. The split ground plane occupies the second and third metal layers underneath the signal layer serving digital and RF part respectively. 3) One *50 Ohm zigzag microstrip line* was designed with small delay difference between those lines for a high speed transmission.

Various time-domain waveforms were measured and the results are shown in Fig.4 It is obvious that the waveform at speed of 3.2 Gbps is clear, which means the noise suppression was successful. he outputs of the FPGA verify that the impedance of the transmission line matches well.

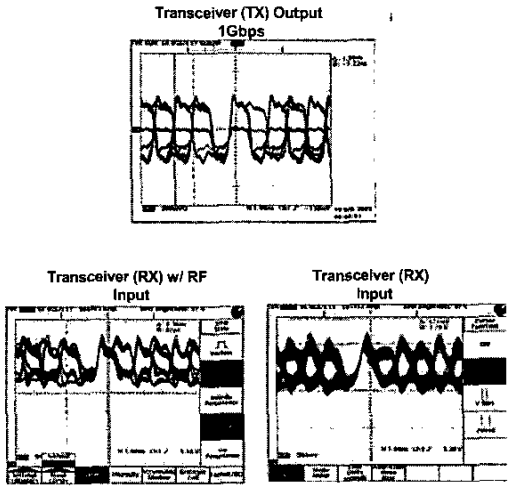


Fig. 4 Digital block measured results

V. Analog Block Results

The analog block of the INC system focuses on the study of mixed signal architectures, which can provide enhanced bandwidth, frequency and data rates in real time. The goal is to combine high-speed broadband digital signals up to 10Gbps and RF carriers in the frequency range between 5-14 GHz. Various passive and active components for the realization of efficient RF-digital interfaces have been implemented and evaluated, and design rules are to be derived for various frequency ranges.

Numerous RF passives, that have been designed and developed in RF testbed, have been integrated in the INC system. A mixed signal combiner has been developed using PRC's multi-layered organic package. The combiner has excellent isolation between digital and RF port and shows only -1dB of insertion loss at 5.8GHz. Linear phase low-pass filter has been developed as a part of the mixed signal combiner. [4]

A Voltage controlled oscillator module has been developed and successfully demonstrated for 5.8GHz operation. The customary designed cross-coupled VCO has been fabricated using commercial based MESFET process without inductors. The bare die IC is wire-bonded to the two embedded inductors which are built on the organic substrate. It is clear that the high-Q inductor is essential for a significantly reduced phase noise of the VCO. The VCO module used for INC testbed shows the phase noise of -110 dBc @ 6MHz offset frequency and -10 dBm of output power. [2]

VI. Optical Block Results

In the optical block, the optical waveguide (WG) structure is integrated on a built-up layer printed wiring board (PWB). The waveguide material is epoxy-based Siloxane oligomer. The waveguide core cross sections are 50 μm x 7 μm, contain an "S" turn at mid section, each turn having 1 cm turn radius, and are up to 14 cm in length. The ends of the waveguides are polished to improve the optical quality. Optical fiber pigtails are used to end-couple light in and out of the array.

Fig. 5 shows a polished cross section of one waveguide in an array of eight embedded waveguides in PWB. The core is accentuated by incandescent light illumination from the opposite end of the waveguide. The power and ground planes in the built-up PWB layer are clearly seen. The indices of refraction of the cross linked waveguide polymer materials for core and cladding are $n_{core} = 1.55$; $n_{clad} = 1.49$, a difference of 3.82%, from which we estimate, given the cross sectional dimensions, that each waveguide can support about 8 modes.

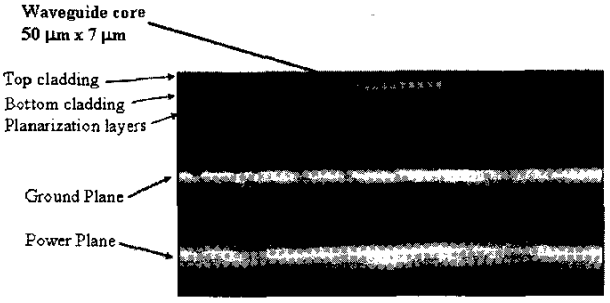


Fig. 5 Polished cross section of the optical waveguide

To test the susceptibility of bent, multimode waveguides (WG) to mode dispersion and poor eye opening, an array of waveguides having a 180° "U" turn path was constructed on a PWB. The turn radius was 1 cm and the total waveguide length was 5 cm. A 10 GHz sinusoidal RF signal was used to drive the optical transmitter at wavelength 1.55 μm. This was followed by an Erbium-doped fiber amplifier (EDFA) with maximum amplification of about 17dBm. A wide open and clear eye diagram with extinction ratio of 11.64dB at 10Gbps was obtained, as shown in Figure 6, indicating no measurable mode dispersion over bent, multimode waveguides that are 5 cm in length.

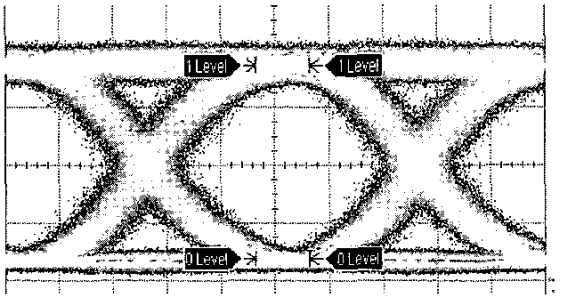


Fig. 6. Measured eye diagram of optical block

VII. Fully Functional INC System Test Results

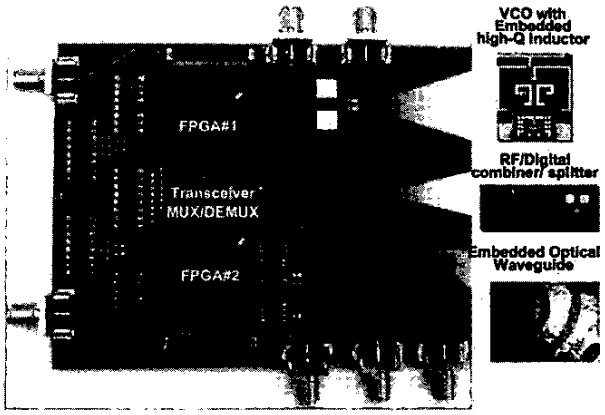
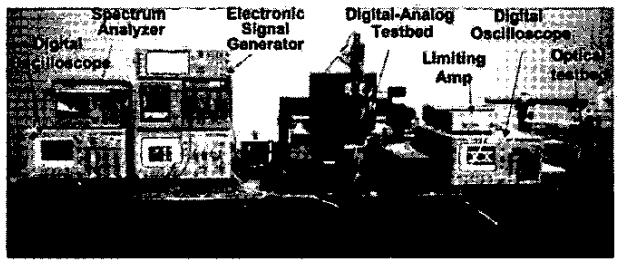


Fig. 7 Fabricated INC board used for the demonstration



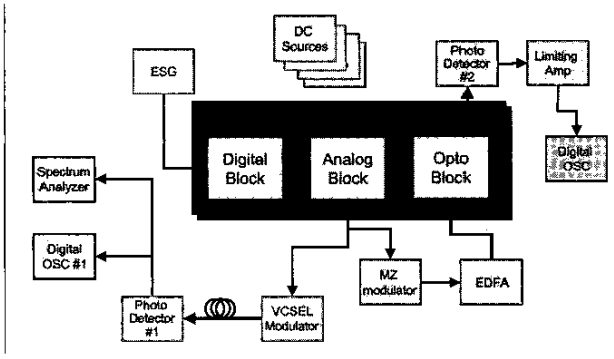


Fig. 8 Photo and diagram of demonstration setup

The fully functional INC system testbed has been fabricated and demonstrated. The final version of INC system has been shown in fig.7. The configuration and a photo of system test setup are shown in fig. 8. Two identical INC boards were used for the demonstration, one for showing digital-RF blocks and the other one for optical block, which requires more stable setup for the accurate aligning the embedded waveguide and optical fiber. Even though the two boards were spatially separated, they were functionally connected by RF and optical cables and connectors. The optical table has been used to minimize vibration when embedded optical waveguides are coupled to optical fibers. The EDFA has been used to compensate for the high total insertion loss of the on-board waveguides. The optical signal goes through a second EDFA before arriving at the receiving end of the system. Photo of optical measurement setup is shown in fig.9.

Fig. 9 Demonstration setup for Optical block

The photo of the setup of the mixed Digital-Analog block is shown in fig.10. Two different optical paths have been demonstrated at the same time, one for using Mach-Zehnder modulator with the embedded waveguide and the other one for using multi-mode fiber with VCSEL modulator. Fig. 11 shows the signal characteristics at each node. At the digital domain, only eye diagram for the digital data stream is observed. On the analog block, the effect of adding RF signal to the digital signal can be clearly seen. The time-domain data shows thicker lips in the eye diagram, which means that the RF signal information is loaded on the envelope of the digital data. In contrast, frequency spectrum shows clear separation between digital and RF signal. The side lobes of the digital signal have been truncated by a low-pass filer before adding the RF signal. At the receiver side, the RF signal can be easily removed by the mixed signal divider after the photo detector.

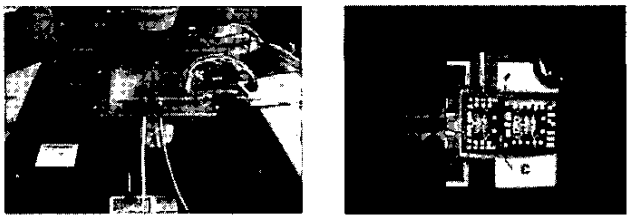


Fig. 10 Demonstration setup for RF and Analog blocks

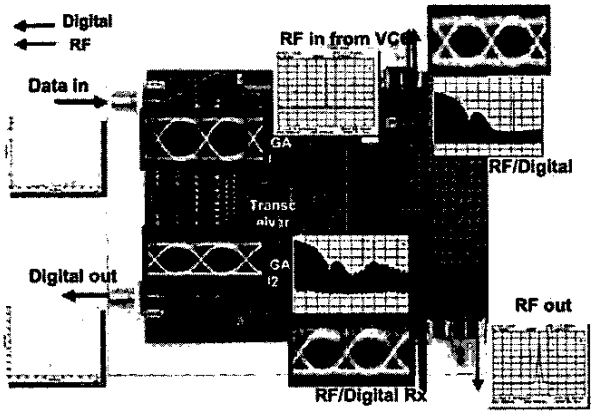


Fig. 11. Measured signals at each node of the system

VIII. Conclusions

One integrated mixed-signal system, so called INC, has been developed and its functionality has been demonstrated. The main purpose of the INC project is to demonstrate the feasibility of SOP technology for the future electronics systems. The system has been designed to deal with digital, analog and optical signal along with the various mixed signal issues. The board has been fabricated in multilayer organic process and the commercial and custom-built ICs have been assembled on the low cost multilayer organic board. The embedded optical waveguides have been fabricated on the board as well. The digital block showed 3.2 Gbps of data stream capability, and the RF block had less than -1.5dB of insertion loss at 5.8GHHz. The optical block achieved 10Gbps throughput over the embedded optical waveguide. The full functionality of INC system has been successfully .

Acknowledgments

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