Power Transmission Lines: A New Interconnect Design to Eliminate Simultaneous Switching Noise

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Abstract

A major bottleneck in high-speed signaling is the simultaneous switching noise (SSN), which is caused by simultaneously switching output buffers. SSN is a result of the coupling between the signal lines and the power delivery network (PDN) in off-chip signaling. This coupling occurs at discontinuities of the transmission line, wherever there is an interruption of the current return path. A particular location where there is a return path discontinuity is the output buffer that is connected to a transmission line. To reduce this discontinuity, current designs try to maintain a low-impedance PDN for the I/O lines up to the output buffers on the chip. This requires a complicated design of the package and interconnections using, for example, planes for the PDN and decoupling capacitors on the package. For GHz signaling, it can be very difficult to maintain sufficiently low impedance. This paper presents a new PDN design, called as the power transmission line, which overcomes these problems.

Introduction

High-speed designs make use of power planes today, as opposed to the proposed power transmission lines. However, predicting the behavior of planes is computationally expensive because of their complicated geometries and multiple resonances. Another disadvantage of power planes is the coupling between signal lines and power planes [1] due to possible slots in the reference planes. From an electromagnetic interference viewpoint, recent research also suggests that power traces can be preferable compared to power planes [2]. Although power planes can be terminated to reduce the resonances using dissipative edge termination [3], this approach has limitations since power planes are two-dimensional with arbitrary boundaries.

In the proposed approach, a transmission line is used to connect the PDN on the printed circuit board (PCB) to the power terminal of an output buffer as shown in Figure 1. Each signal transmission line has a corresponding power transmission line. All power transmission lines are connected with each other on the PCB. This is fundamentally different than the methodology being used today, where the power terminals of the output buffers are connected at the chip and package levels as well.

The signal and power transmission lines are routed with respect to the ground plane as the reference conductor. To reduce reflections, the characteristic impedance of the power transmission line can be matched to the signal transmission line and different termination schemes can be applied. One approach is to use parallel termination for the signal line (i.e., close to the receiver circuit), and series termination for the power line (i.e., close to the power supply at the PCB). In a typical CMOS push-pull buffer, the signal line is connected to the ground plane at a high-to-low transition. Since the ground plane is the reference plane for the signal line, there is no return path discontinuity. At a low-to-high transition, the signal transmission line is connected to the power transmission line. If both the signal and power transmission lines have the same characteristic impedance and assuming that the on-resistance of the transistors are negligible, once again there is no return path discontinuity. The overall interconnection can be considered as a single longer transmission line with a series-parallel termination, starting from the power supply on the PCB and ending at the receiver. Hence SSN caused by the drivers is eliminated at the chip and package levels. The design of the I/O PDN is also greatly simplified, since low impedance PDN is required only at the location on the PCB, where all the power traces are connected. The rest of the I/O PDN consists of only some transmission lines, which can be routed automatically using current design tools. There is no need to design a low-impedance PDN on the package using planes or decoupling capacitors.

In conclusion, we believe that PDN design with power transmission lines can dramatically change the design of high-speed systems today. It would help to design systems in a much more cost-effective and simpler way, while improving the performance.

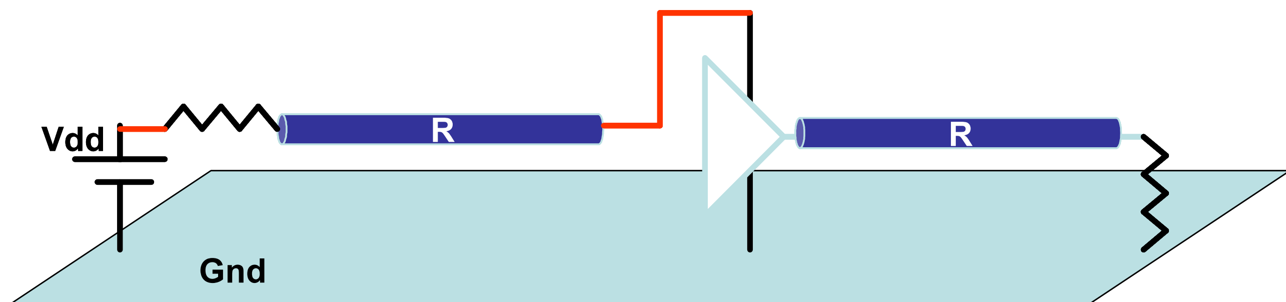

Figure 1 Power transmission line signaling eliminating SSN on the IC and package levels

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Problems with Return Currents in Existing Designs

A major source of SSN and electromagnetic interference (EMI) is the discontinuity of transmission line return currents. One typical example is a microstrip line routed over a slot in the reference plane as shown in Figure 2. For high-speed signals, this causes increased cross-talk between multiple signals crossing the slot as well as signal integrity problems for the aggressor line as well. Examples of this return path problem are given in references such as [1], [4], and [5].

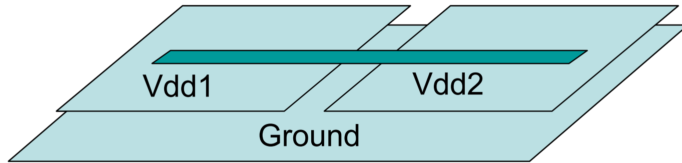

Figure 2 Microstrip over a slot line

A similar return path discontinuity can occur due to routing a transmission line on an electromagnetic bandgap (EBG) structure as shown in Figure 3. Such EBG structures have been proposed to overcome the coupling effects through the power/ground planes. However, the return currents of transmission lines referenced to EBG structures need to be controlled once again to maintain signal integrity [6].

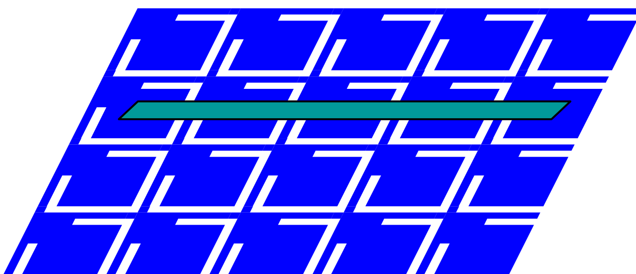

Figure 3 Transmission line referenced to an EBG patterned plane

At via transitions through power (Vdd) and ground planes, the return current has to close the loop by exciting the cavity between the planes as shown in Figure 4. Stitching vias are commonly used to manage these return currents [7]. However, such solutions are difficult to implement for high-speed signals due to the parasitic inductance of such components.

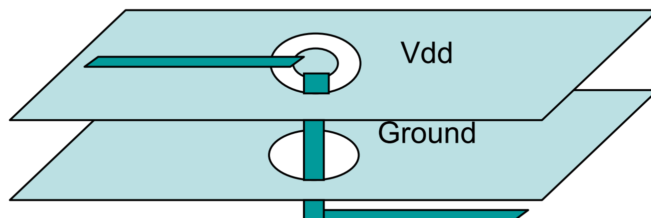

Figure 4 Microstrip to microstrip via transition

All the problems described in Figure 2, Figure 3, and Figure 4 can be avoided in some designs by referencing the transmission line solely to the ground or Vdd plane as shown in Figure 5. However, even for this seemingly ideal case without any return current problems, there is a return path discontinuity that occurs at the driver side [8].

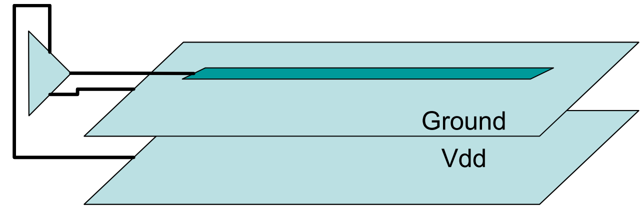

Figure 5 Transmission line referenced to a solid ground plane

The return current problem in Figure 5 can be explained by examining the current loops during low-to-high and high-to-low transitions. Figure 6 shows the current loop for a high-to-low transition, where the driver connects the output signal to the ground plane. Since the image current of the transmission line is also on the ground plane, there is no discontinuity of the return current.

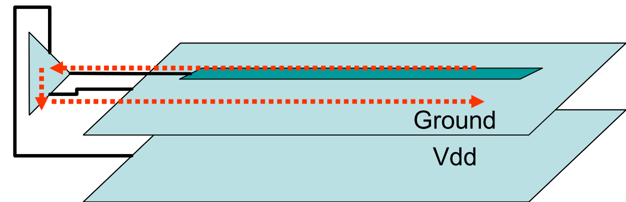

Figure 6 Current loop during a high-to-low transition

During a low-to-high transition, on the other hand, the driver connects the output signal to the Vdd plane as shown in Figure 7. Hence the image current of the transmission line on the ground plane wraps around and excites the Vdd/ground plane. Avoiding this return current problem is very difficult for high-speed signals, because very low impedance is required between the Vdd and ground connections of the driver to reroute the return current to the ground plane.

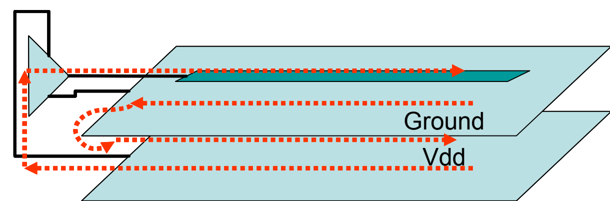

Figure 7 Current loops during a low-to-high transition

A common technique to avoid the coupling of noise due to return current discontinuities is to use differential lines as shown in Figure 8. The return current of each line of a perfectly matched differential pair is in the opposite direction. Hence they cancel each other and do not excite the Vdd/ground planes. However, the differential lines need to be routed symmetrically and the length of each line has to be matched to benefit from differential signaling. This is often times very difficult to achieve due to the imperfections in the printed circuit boards (such as inhomogeneous material

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properties) as well as design constraints in a highly populated board.

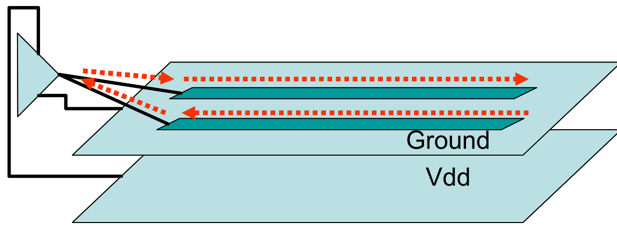

Figure 8 Current loops for differential transmission lines

Power Transmission Line Signaling

By making use of power transmission lines, the benefits of differential signaling can be achieved without requiring an ideal differential line. In this new interface standard, called *Power Transmission Line Signaling*, two transmission lines are connected to a single-ended driver, similar to a differential driver. One transmission line is connected to the output of the driver, whereas the second transmission line connects the Vdd terminal of the driver to the power supply on the printed circuit board. Unlike a differential transmission line, the two transmission lines in power transmission line signaling do not need to be matched or routed close to each other. Also, the power transmission line is the only connection of the driver with the power supply. Hence, no other I/O power delivery network is required on the chip or package. Power planes and decoupling capacitors on the IC package are not needed.

To illustrate how return currents are managed in power transmission line signaling, consider Figure 9. During a low-to-high transition, the driver just connects the two transmission lines with each other. Return currents of both transmission lines are on the ground plane, hence there is no discontinuity of the return current.

Figure 10 shows the case when the driver makes a high-to-low transition. In this case, once again the return current does not experience any discontinuity.

Hence by using power differential lines, the simultaneous switching noise associated with drivers and I/O lines can be completely eliminated. Essentially, this is being achieved by managing the return currents and completely eliminating the I/O power delivery network with all the decoupling capacitors and planes on the chip and package levels.

Termination Schemes

The reflections from both the power transmission line and the signal transmission line can be controlled by appropriately terminating them. The signal waveform depends on how they are terminated. For example, the termination scheme in Figure 1 corresponds to a series-parallel termination scheme, which can swing the output between 0 and Vdd/2. The behavior of power transmission line signaling with respect to terminations can be illustrated by representing the driver as a simple switch as shown in Figure 11. Figure 12 shows the series termination scheme, which allows the output voltage full swing from 0 to Vdd.

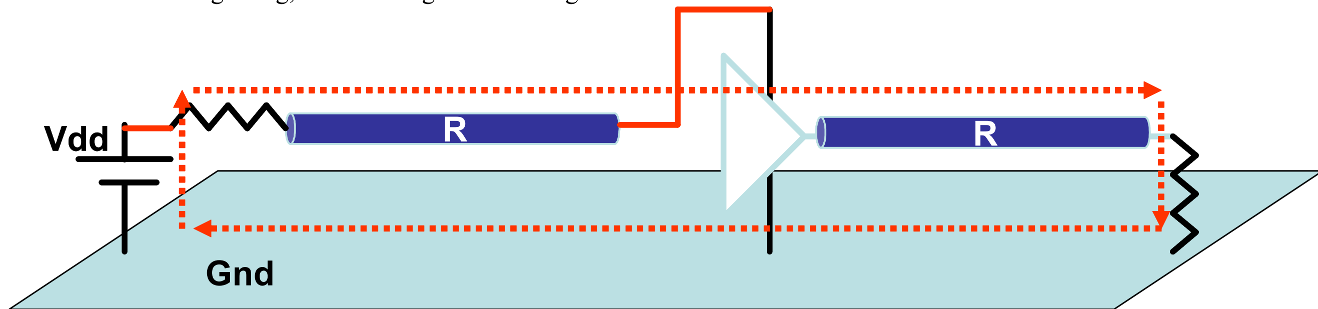

Figure 9 Low-to-high transition using power transmission lines

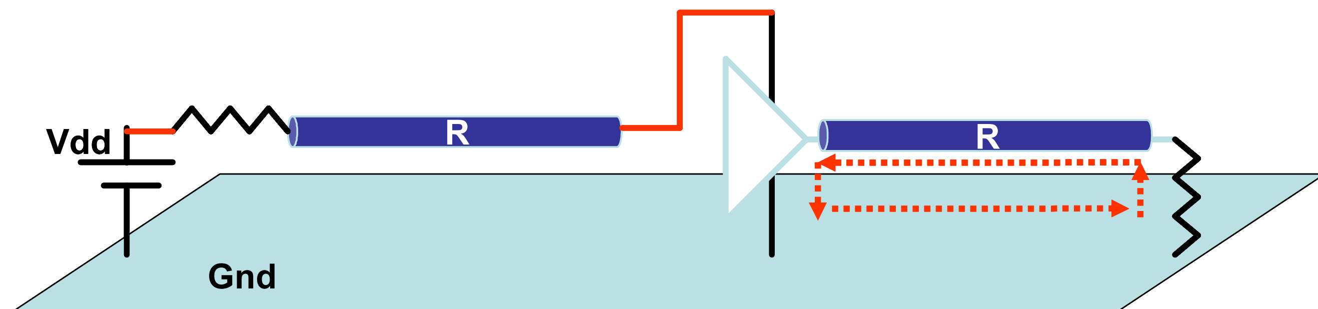

Figure 10 High-to-low transition using power transmission lines

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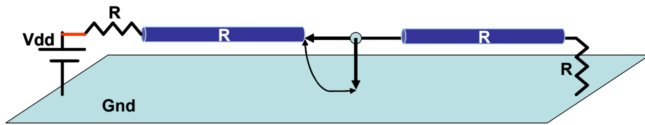

Figure 11 Series-parallel termination using power transmission lines

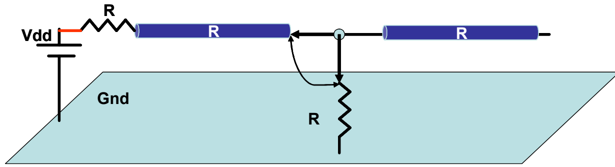

Figure 12 Series termination using power transmission lines

Figure 13 and Figure 14 show the output voltage at the far end of the signal transmission line for series-parallel termination and series termination respectively. A simple switch using time-varying resistors was used to implement the driver in these simulations. The series termination is not as smooth as the series-parallel termination, possibly due to the modeling of the driver.

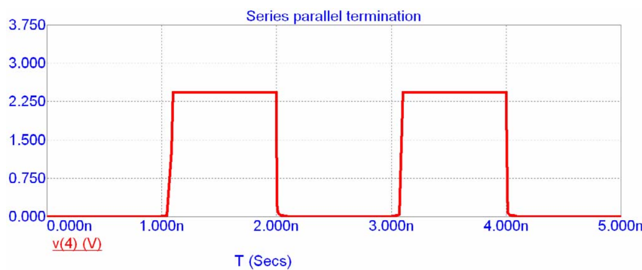

Figure 13 Simulation of the output voltage using series termination in Figure 11

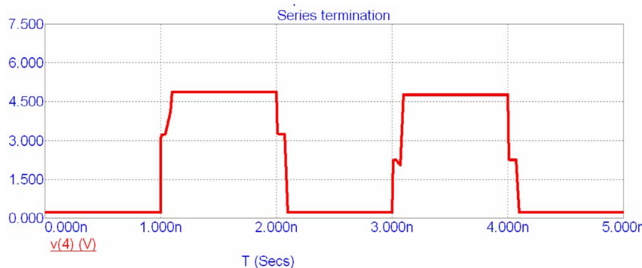

Figure 14 Simulation of the output voltage using series termination in Figure 12

Power Transmission Lines for Core Power Delivery Network

Transmission lines can potentially be applied in the power delivery network for the core logic as well. The benefit in this case would be once again simplified designs, and elimination of delta-I noise. Figure 15 shows a typical design of the power delivery network for the core logic. It involves surface mount capacitors and planes both on the package and board levels.

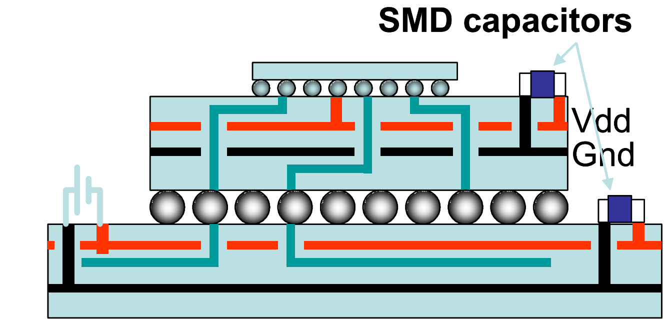

Figure 15 Conventional design for the core power delivery network

The equivalent circuit model for such a design can be sketched as in Figure 16. The interactions between various components of the power delivery network as well as the power/ground planes cause undesirable resonances, which increase the impedance Z as seen by the chip. These resonances, especially at high frequencies, are very difficult to analyze and eliminate.

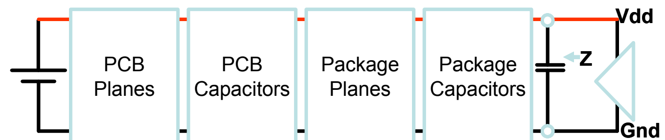

Figure 16 Equivalent circuit model representing the power delivery network in Figure 15

Figure 17 shows a possible application of power transmission line in core decoupling. Once again different termination schemes can be considered. The particular scheme in Figure 17 should be carefully considered with respect to the allowable IR drop in the system. A test vehicle was designed to compare a similar setup with a traditional setup involving power/ground planes. The power transmission line setup is shown in Figure 18.

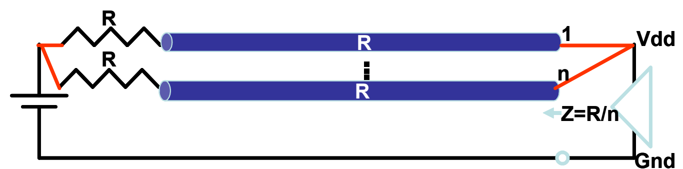

Figure 17 Possible core power delivery network design using power transmission lines

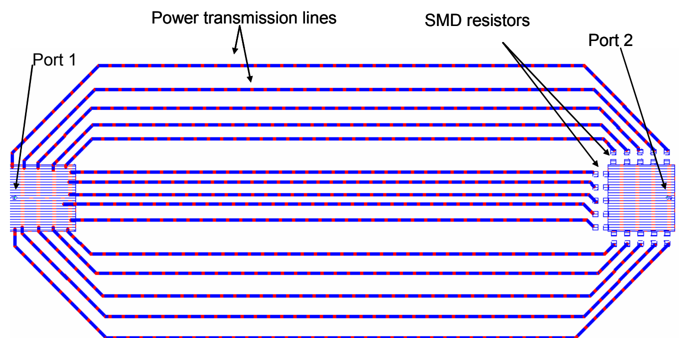

Figure 18 Layout of the test vehicle consisting of 15 power transmission lines

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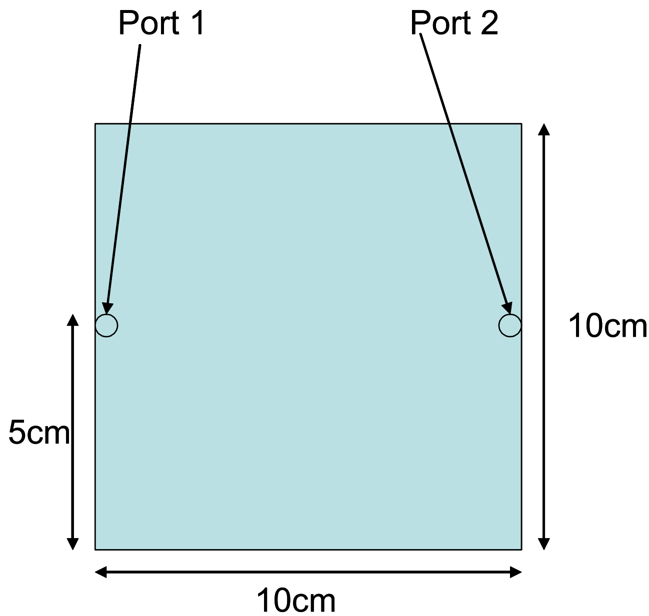

Figure 19 Layout of the test vehicle consisting of solid power planes

The power transmission lines in Figure 18 were terminated using 25Ω resistors. Each transmission line had a width of 500um and was referenced to the ground plane. The test board had the size of 10cm by 10cm. The dielectric used was FR4, with a thickness of 100um. Measurements were taken using a 2-port VNA. The measured S-parameters were then converted to a 1-port impedance by shorting the second port to ground to represent the power supply.

Another test board was measured which had ports at the same locations as shown in Figure 19. This second test board consisted of solid power ground planes. Similarly the second port was shorted in the measured 2-port S-parameters to represent the connection of the power supply at that point.

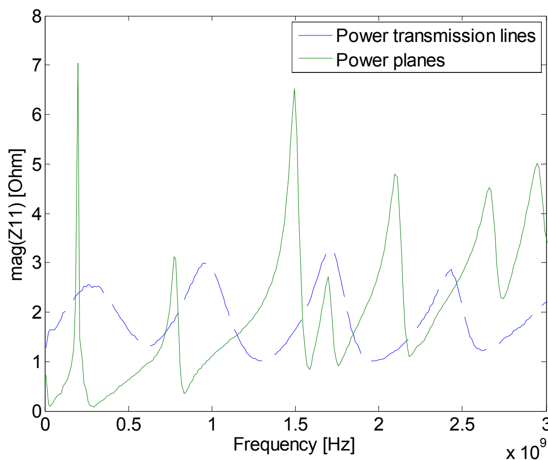

Figure 20 Comparison of the measured impedance of power transmission lines (Figure 18) vs. power planes (Figure 19)

Figure 20 shows the comparison of the test vehicle using power transmission lines with the test vehicle including solid power planes. Using power transmission lines, a lower impedance could be maintained at high frequencies because the sharp cavity resonances can be avoided. In ideal case, the power transmission line network can provide a flat frequency response. This was not achieved due to the impedance mismatch between the surface mount resistors and the characteristic impedance of the power transmission lines in this test vehicle.

Conclusions

The power transmission line signaling has the potential of eliminating simultaneous switching noise on the IC and package due to switching I/O lines. For the first time, it has allowed to provide continuous current return paths for both low-to-high and high-to-low transitions in single-ended signaling. It does not suffer from the difficulties associated with differential signaling such as skew and mismatch in the lengths of the differential pair. By eliminating the I/O power planes and decoupling capacitors completely, it can provide a cost-effective solution as well.

Power transmission lines carry the potential to be used for core decoupling as well. Measurement results show lower impedance compared with a much larger solid power plane, because cavity resonances are eliminated. Further research on termination schemes is necessary to assess the performance of power transmission lines in core decoupling with regards to IR drop.

In conclusion, power transmission line signaling has the potential of providing a technology to design an I/O system that does not generate simultaneous switching noise due to return path discontinuities.

References

1. K. Bharath, E. Engin, M. Swaminathan, K. Uriu, and T. Yamada, “Efficient simulation of power/ground planes for SiP applications,” in Proc. Electronic Components and Technology Conference, Reno, NV, June 2007.
2. Leferink, Frank, "Power and Signal Integrity and Electromagnetic Emission; the Balancing Act of Decoupling, Planes and Tracks," IEEE International Symposium on EMC, 9-13 July 2007
3. Istvan Novak, “Reducing Simultaneous Switching Noise and EMI on Ground/Power Planes by Dissipative Edge Termination, IEEE Topical Meeting on Electrical Performance of Electronic Packaging, October 26-28, 1998, West Point, New York.
4. Helen K. Pan and Christopher Pan, “Stitching a Reference Plane Split Using Routing Layer Traces to Improve I/O Bus Signal Integrity,” PIERS Proceedings, 1682 - 1685, March 26-30, Beijing, China, 2007.
5. Juan Chen, Weimin Shi, Norman, A.J., Ilavarasan, P., "Electrical impact of high-speed bus crossing plane split," IEEE International Symposium on Electromagnetic Compatibility, vol.2, no., pp.861-865, 19-23 Aug. 2002.
6. Sung-Ho Joo, Dong-Yeop Kim, Hai-Young Lee, "An S-Bridged Inductive Electromagnetic Bandgap Power Plane for Suppression of Ground Bounce Noise," IEEE Microwave and Wireless Components Letters, vol.17, no.10, pp.709-711, Oct. 2007.
7. Scott McMorrow, “Handling Signal Return Current”, Printed Circuit Design, September 2002, pp. 12-16.
8. Larry Smith, “Simultaneous Switch Noise and Power Plane Bounce for CMOS Technology”, IEEE Electrical Performance of Electrical Packaging (EPEP) Conference, San Diego, CA October 17-25, 1999.

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