

Electrical-Thermal Co-analysis for Power Delivery Networks in 3D System Integration

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Abstract - In this paper, an electrical-thermal co-analysis method for power delivery networks in 3D system integration is proposed. For electrical analysis, temperature-dependent electrical resistivity of conductors is taken into account. For thermal analysis, Joule heating effect due to the current flowing through conductors is considered. The proposed co-analysis method is carried out using *Rgen* and *ChipJoule* of IBM EIP Tool Suite. An example of 3D integration system including stacked chips, power delivery network, glass-ceramic substrate, through-silicon vias, controlled collapse chip connections (C4s), underfill material, and TIM is analyzed using the proposed method. The simulation results show that the temperature effect on IR drop can not be neglected. The error of not considering thermal effect on IR drop is about 20% in the example.

Keywords - electrical-thermal co-analysis; 3D integration; power delivery network (PDN); IR drop; through-silicon via (TSV); Joule heating; temperature effect

I. INTRODUCTION

With the emerging technology of 3D integration enabled by through-silicon vias (TSVs), heat flux density increases dramatically because of stacked chips in z-direction [1]. As a result, thermal problem in 3D system integration becomes more critical compared to 2D system integration, leading to the point where temperature effects have become important. Therefore, the temperature effects on electrical performance of 3D system should be considered carefully in electrical design. In particular, the non-uniform temperature distribution affects the electrical performance of power delivery networks.

The PDN should be designed to limit IR drop within certain range. Basically, the conductors in the PDN will cause IR drop due to their electrical resistivity. Since their electrical resistivity is a function of temperature, the IR drop of the PDN will be affected by non-uniform thermal distribution in the whole system. Moreover, non-uniform Joule heating generated by the PDN and stacked chips will affect the thermal profile again. Thus, the electrical and thermal fields in 3D systems are fully coupled together. Without considering the thermal effects on the PDN in 3D systems, the total IR drop will be underestimated. In order to obtain accurate PDN characteristics, accurate electrical-thermal co-analysis method is strongly required.

Several electrical-thermal co-analysis methods have been developed, such as the simulator coupling based method [2], Green-function based method [3], and finite difference based method [4]. However, they are focused on on-chip analysis. For accurate PDN design, all system components such as metal planes, packages and chips should be included. Especially in 3D system integration, the PDN consists of not only power planes and metal traces, but also many vertical interconnects such as TSVs and C4s between the stacked chips. In this paper, all of the above system level components are included in the electrical-thermal co-analysis, so that accurate analysis results of the PDN in 3D integrated system can be acquired.

The organization for this paper is as follows. The proposed electrical-thermal co-analysis method for PDN is explained in section II. A 3D integration example and co-analysis results are shown in section III. And the conclusions are shown in section IV.

II. ELECTRICAL-THERMAL CO-ANALYSIS METHOD

In the steady state, the governing equation for voltage distribution in PDN can be expressed as:

$$\nabla \cdot \left(\frac{1}{\rho(x, y, z, T)} \nabla \phi(x, y, z) \right) = 0 \quad (1)$$

where, $\phi(x, y, z)$ represents the voltage distribution and $\rho(x, y, z, T)$ is the electrical resistivity. Since the electrical resistivity is temperature-dependent, it is described by:

$$\rho = \rho_0 [1 + \alpha(T - T_0)] \quad (2)$$

where, ρ_0 is the electrical resistivity at T_0 which is 20 °C, and α is the temperature coefficient of electrical resistance [5]. As temperature increases, the electrical resistivity of the conductors goes up and eventually affects PDN characteristics. The temperature-dependent resistivity of several conductors is shown in Fig. 1.

Moreover, the Ohmic loss due to the current flowing through conductors in PDN is converted to Joule heating. It can be expressed as:

$$P(x, y, z) = \vec{J} \cdot \vec{E}(x, y, z) \quad (3)$$

where, $\vec{J}$ is the current density in PDN and $\vec{E}(x, y, z)$ is the electrical field distribution. The generated Joule heating becomes new excitation for the thermal distribution profile, which can be solved using the heat diffusion equation:

$$\nabla \cdot [k(x, y, z, T) \nabla T(x, y, z)] = -P(x, y, z) \quad (4)$$

where, $k(x, y, z, T)$ is the temperature-dependent thermal conductivity and $T(x, y, z)$ is the temperature distribution [6]. The new temperature distribution will change the electrical resistivity of conductors in PDN again. In this way, the electrical and thermal fields are coupled and affect each other.

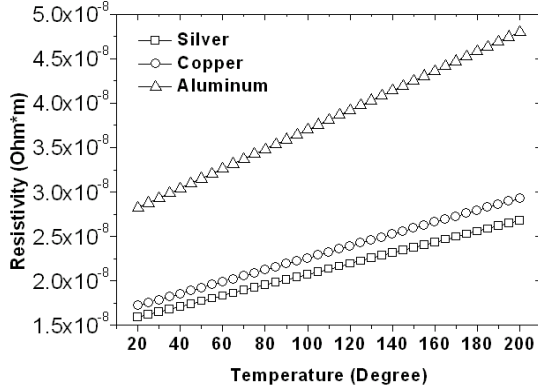


Figure 1. Temperature-dependent resistivity of conductors.

The relationship between thermal and electrical fields can be summarized as in Fig. 2. As shown in this figure, the thermal and electrical fields are coupled together as a closed loop.

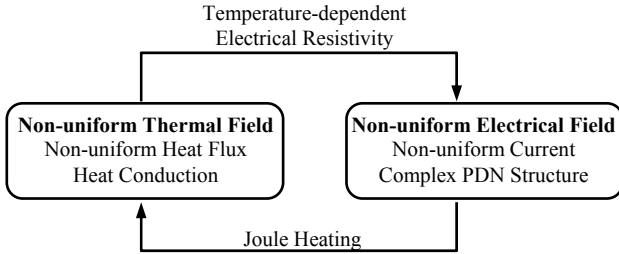


Figure 2. The relationship between thermal and electrical fields.

Based on the above relationship, an electrical-thermal co-analysis method for PDN is proposed. The proposed co-analysis procedure for PDN is shown in Fig. 3 and explained as follows:

- 1) Setting input information including geometry, initial material properties, excitations, and boundary conditions for steady state electrical and thermal analysis.
- 2) Steady state electrical solving for voltage, current, and power distribution profiles in PDN.
- 3) Heat sources (Joule heating) calculation from the power distribution profile.

- 4) Steady state thermal solving to obtain the temperature distribution profile based on the input thermal boundary conditions and new heat sources from step 3.
- 5) Updating electrical resistivity of conductors in PDN based on the temperature distribution profile in step 4.
- 6) Determining whether temperature and voltage distributions converge or not. If they do not converge, it goes back to step 2. If converge, the co-analysis is ended and final results are shown.

In the proposed electrical-thermal co-analysis procedure, the DC IR drop simulation tool *Rgen* and thermal simulation tool *ChipJoule* of IBM EIP Tool Suite are adopted for steady state electrical and thermal analysis, respectively [7]. In electrical analysis, the electrical resistivity of conductors in PDN including copper, tungsten for TSVs, *Sn-0.7Cu* for C4 balls are all considered as temperature-dependent parameters. In the thermal analysis, the thermal conductivities of conductors and dielectrics are considered as constant for simplicity. The top heat sinks are modeled as ideal heat sinks with constant room temperature of 25 °C. Initially, the system temperature including chip temperature is assumed to be room temperature at the beginning of the co-analysis.

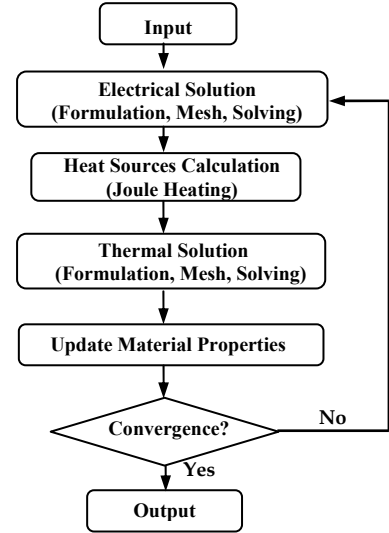


Figure 3. The proposed electrical-thermal co-analysis procedure for PDN.

III. 3D SYSTEM EXAMPLE AND ANALYSIS RESULTS

A 3D integration system with two sets of stacked chips is analyzed employing the proposed co-analysis method. The detailed structure of the 3D system is shown in Fig. 4. Two metal layers are shunted together with multiple-vias in glass-ceramic substrate. A 2.5 V voltage source is placed at the corner of the package. In each set of stacked chips, the memory chip is stacked on top of the CPU chip using TSVs and C4s. The package size is 20 cm * 20 cm and the size of each chip is 1.2 cm * 1.2 cm. The detailed geometry and material parameters are summarized in Table I.

In this example, the power consumption for Chip1 (CPU1), Chip2 (RAM1), Chip3 (CPU2), and Chip4 (RAM2) are 60 W, 10 W, 30 W and 10 W, respectively. The non-uniform power

maps are used for CPUs while uniform power maps are adopted for memories as shown in Fig. 5. The TSV configuration for the stacked chips is illustrated in Fig. 6, in which the top chip and bottom chip use different power supply TSVs in order to reduce the IR drop for the top chip.

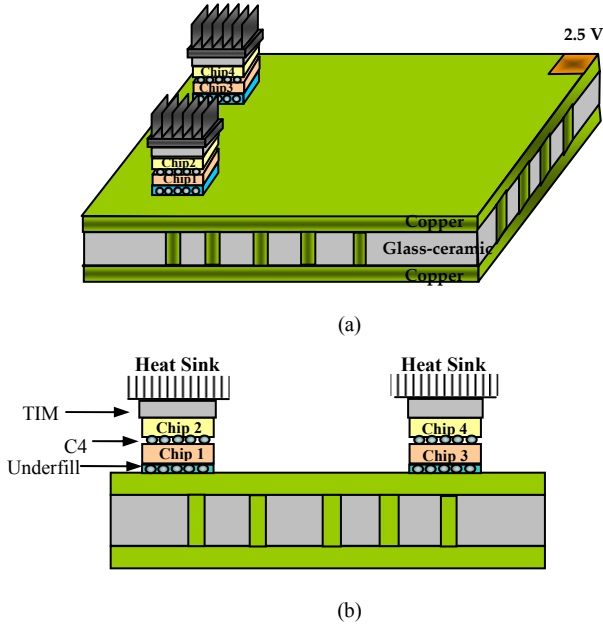


Figure 4. 3D integrated system. (a) Whole system (b) Cross-sectional view.

TABLE I. MATERIAL THICKNESS AND THERMAL CONDUCTIVITY

	Material Thickness (mm)	Thermal Conductivity (W/mK)
Glass-ceramic	0.35	5
Copper	0.036	400
Chip	0.5	110
Underfill	0.2	4.3
C4	0.2	60
TIM	0.2	2
TSV (Tungsten)	0.5	174

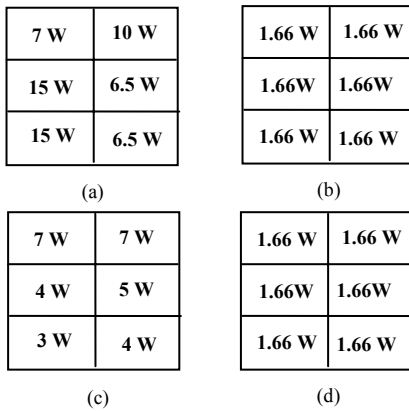


Figure 5. Power map of stacked chips. (a) CPU1 (b) RAM1 (c) CPU2 (d) RAM2.

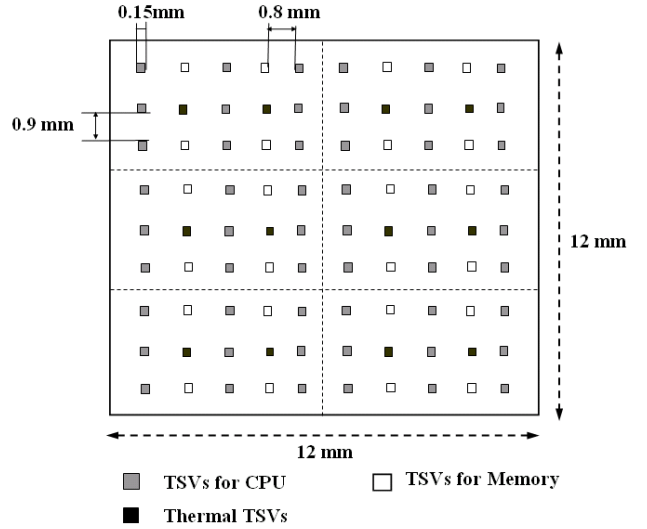


Figure 6. The TSV configuration for stacked chips.

The electrical-thermal co-analysis results of voltage drop of the four chips are shown in Fig. 7. It shows that the voltage drop of the four chips converges after 4 iterations of the co-analysis loop. And it demonstrates that the final IR drop of CPU1 is 34.8 mV, while its initial IR drop at room temperature is 28.3 mV. The temperature effect on the IR drop in CPU1 is 23% increase. For RAM1, CPU2 and RAM2, the temperature effects on the IR drop are 22.7%, 22.9% and 22.2% increase, respectively. The results show that the temperature effect on IR drop should be considered to obtain accurate DC drop. Without considering the temperature effect on the PDN, the IR drop will be under-estimated.

The electrical-thermal co-analysis results of highest temperatures (hot spots) of the four chips are shown in Fig. 8. It shows that temperatures of the chips also converge after 4 iterations of the co-analysis loop. The hot spot temperature difference between RAM1 and CPU1 is about 7.2 °C while the temperature difference between RAM2 and CPU2 is about 3.6 °C. Due to the longer heat conduction path from the bottom chip to the heat sink, the bottom chip has larger equivalent thermal resistance and higher temperature than that of the top chip. Compared to the initial temperature, the final temperature of Die1, Die2, Die3 and Die 4 increase about 265.2%, 236.2%, 144.2% and 129.8%, respectively by including the co-analysis loop.

After the convergence of the electrical-thermal co-analysis loop, final temperature and voltage distributions of the chips can be shown as Fig. 9 and Fig. 10, respectively. Fig. 9 illustrates that the temperature distribution profile of CPU1 matches with its power map in Fig. 5 and the hot spot appears in the block of highest power map in CPU1 (15 W in Fig. 5(a)). Fig. 10 demonstrates that the IR drop at every TSV location is increased due to the Joule heating effect on the PDN. Fig. 10 (a) shows that the final voltage distribution of stacked chips (CPU1 and RAM1) has minimum and maximum IR drop of 32.8 mV and 34.8 mV, while Fig. 10 (b) shows that in the initial voltage distribution, it has minimum and maximum IR

drop of 26.7 mV and 28.3 mV, respectively. Compared to the initial IR drop, the final IR drop increases about 20%.

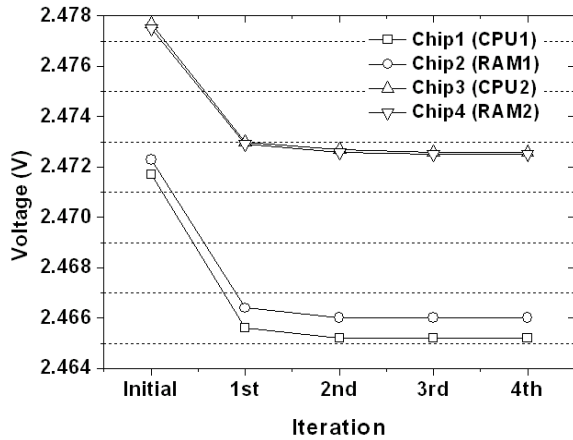


Figure 7. Voltage drop analysis results with electrical-thermal iterations.

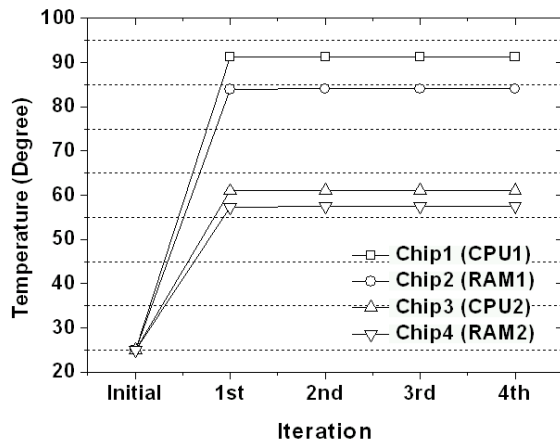


Figure 8. Temperature analysis results with electrical-thermal iterations.

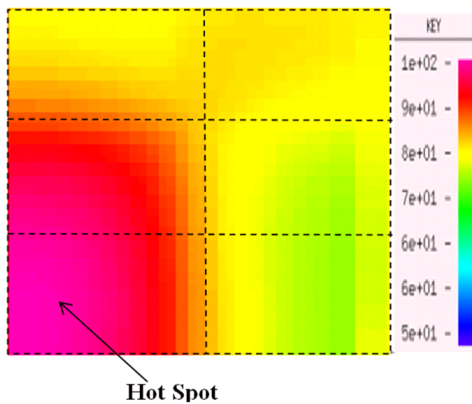
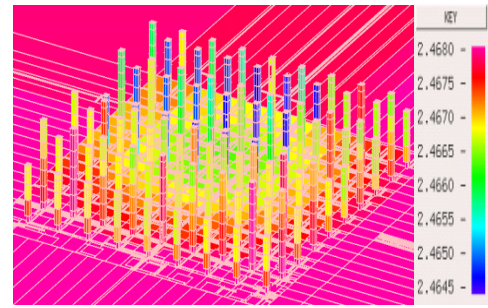
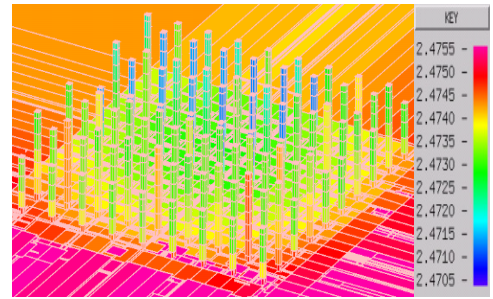


Figure 9. The final temperature distribution of CPU1.



(a)



(b)

Figure 10. The voltage distribution of CPU1 and RAM1. (a) Final voltage distribution (b) Initial voltage distribution at room temperature.

IV. CONCLUSION

In this paper, an electrical and thermal co-analysis method for PDN analysis has been proposed and developed. A 3D integrated system example including planes, substrate, stacked chips, TSVs, C4s and TIM has been analyzed based on the co-analysis method. In the example, about 20% increase of IR drop has been detected using the proposed co-analysis method. The analysis results demonstrate that the electrical-thermal co-analysis should be incorporated into the PDN design procedure to obtain accurate design results.

ACKNOWLEDGMENT

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