Effect of System Components on Electrical and Thermal Characteristics for Power Delivery Networks in 3D System Integration

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Abstract - In this paper, parameterized electrical-thermal co-analysis for power delivery networks (PDN) in 3D system integration is carried out. A 3D integrated system including glass-ceramic substrate, single and stacked dies, power delivery network, through-silicon vias (TSVs), controlled collapse chip connections (C4s), underfill material, and thermal interface material (TIM) is analyzed with several variable parameters. The analysis results show that temperature effects on DC IR drop can not be neglected. The TIM thermal conductivity, C4 density, stacking order of stacked dies, and voltage source location affect the final IR drop and hot spot temperature in the system.

I. INTRODUCTION

Through-silicon via (TSV) technology is a key enabler of high density 3D system integration. However, due to the increased heat flux density of stacked chips in 3D system integration, thermal problem is becoming more critical compared to 2D system [1]. Since electrical circuits will be affected by the thermal field due to their temperature-dependent characteristics, the thermal effect should be included in the electrical design procedure in order to validate the accurate electrical performance. On the other hand, the electrical elements are the sources to generate heat in the system, and these heat sources will affect the thermal field again. Thus, the electrical and thermal fields are coupled together in the system.

Recently, an electrical-thermal co-analysis method for power delivery networks in 3D integration system has been proposed by the authors and a 3D integrated system was analyzed using the method [2]. In the analysis, all the system components such as planes, package, stacked chips, TSVs, C4s and TIM were included. In the design of PDN for 3D system integration, there are many variable parameters which could affect the electrical and thermal performance such as TIM thermal conductivity, C4 density, stacking order of stacked dies, voltage source location, etc. Being aware of the effects of those variable parameters on IR drop and hot spot temperature of the PDN will be critical to designing the PDN which has thermal robustness and low IR drop.

In this paper, a complete parameterized electrical-thermal co-analysis is performed focusing on four variable parameters, that is, TIM thermal conductivity, C4 density, stacking order of stacked dies, and voltage source location. Electrical-thermal co-analysis with those system level parameters provides accurate characteristics of the PDN in 3D integrated system.

In section II, the electrical-thermal co-analysis methodology for PDN analysis is briefly explained. A 3D integrated system example and parameterized analysis results are shown in section III followed by conclusions in section IV.

II. ELECTRICAL-THERMAL CO-ANALYSIS METHODOLOGY

In this paper, the steady state electrical and thermal effects have been analyzed. In the steady state, the governing equations for voltage distribution and thermal distribution can be expressed as:

$$\nabla \cdot \left[\sigma(x,y,z,T)\nabla\phi(x,y,z)\right] = 0 \tag{1}$$

$$\nabla \cdot \left[k(x,y,z,T)\nabla T(x,y,z)\right] = -P(x,y,z) \tag{2}$$

where, $\sigma(x,y,z,T)$ and $k(x,y,z,T)$ represent the temperature-dependent electrical and thermal conductivity in PDN, $\phi(x,y,z)$ and $T(x,y,z)$ represent the voltage distribution and temperature distribution, respectively [2]. The electrical and thermal fields are coupled together due to the temperature-dependent electrical conductivity $\sigma(x,y,z,T)$ and the Joule heat generated by the power delivery networks expressed by

$$P(x,y,z) = \vec{J}(x,y,z)\cdot\vec{E}(x,y,z) = \vec{J}(x,y,z)\cdot(-\nabla\phi(x,y,z)) \tag{3}$$

in which $\vec{J}(x,y,z)$ is the current density in PDN [3]. The relationship between electrical and thermal fields is shown in Fig. 1.

In order to capture the coupling effects between the electrical and thermal fields, the electrical-thermal co-analysis method for PDN in [2] is employed. In the iteration loop shown in Fig. 1, the DC IR drop simulation tool "*Rgen*" and thermal simulation tool "*ChipJoule*" which are IBM EIP Suite tools [4] are employed for steady state electrical and thermal analysis, respectively. In electrical analysis, the electrical conductivities of conductors in PDN including copper, tungsten for TSVs, Sn-0.7Cu for C4 balls are all considered as temperature-dependent parameters. As an example, the temperature-dependent electrical conductivities of copper and tungsten are shown in Fig. 2. In the thermal analysis, the material thermal conductivities are considered as constant for simplicity. The heat sinks are modeled as ideal heat sinks with constant room temperature of 25 $°C$. Only heat conduction boundary condition is applied in the thermal modeling. Initially, the system temperature including dies' temperature is assumed to be room temperature of 25 $°C$ at the beginning of the co-analysis.

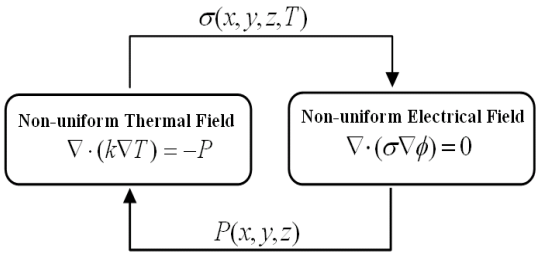


Figure 1. The relationship between electrical and thermal fields.

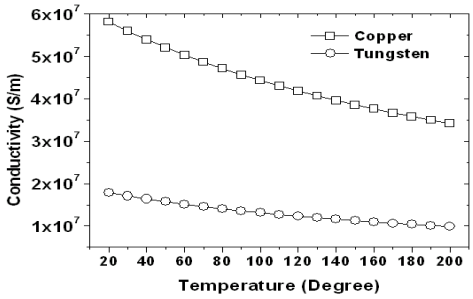
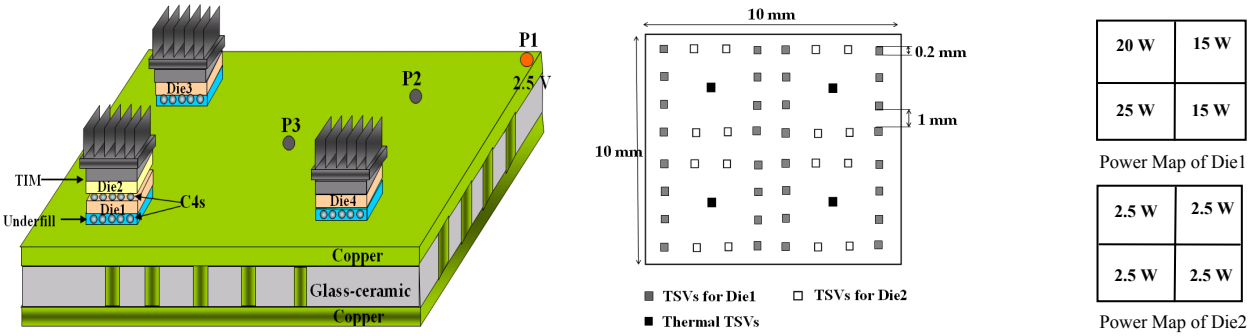


Figure 2. The temperature-dependent electrical conductivities of conductors.

III. System Example and Analysis Results

An example of 3D integrated system is shown in Fig. 3(a). Two metal layers in glass-ceramic substrate are shunted together with multiple vias to reduce the electrical resistance of the PDN. A 2.5 V voltage source is applied at the location P1, the corner of the package. The stacked dies are stacked using TSVs and C4 interface. The TSV configuration for stacked dies is illustrated in Fig. 3(b), in which top die and bottom die use different power supply TSVs. The power consumptions for Die1, Die2, Die3, and Die4 are 75 W, 10 W, 40 W and 20 W, respectively. The uniform power maps are used for Die2, Die3 and Die4, while non-uniform power map is adopted for Die1 as shown in Fig. 3(c). The geometry and material parameters are summarized in Table I.



(a) (b) (c)

Figure 3. The 3D integration package. (a) Whole system view (b) TSV configuration for stacked dies (c) Power maps of Die1 and Die2.

TABLE I. Package Geometry and Material Parameters

	Size (mm * mm)	Material Thickness (mm)	Thermal conductivity (W/mK)
Glass-ceramic	200 * 200	0.35	5
Copper	200 * 200	0.036	400
Die	10 * 10	0.5	110
Underfill	10 * 10	0.2	4.3
C4	0.2 * 0.2	0.2	60
TSV (Tungsten)	0.2 *0.2	0.5	174

A. TIM Thermal Conductivity

The above 3D integration package is analyzed with three different kinds of TIMs. The thermal conductivities of TIM1, TIM2 and TIM3 are 2, 5, 8 W/mK, respectively. The IR drop and temperature of Die1 with multiple electrical-thermal iterations are captured in Fig. 4. It shows that both the IR drop and temperature converge after 4 iterations. Fig. 4(a) shows that with TIM which has higher thermal conductivity, the Die1's temperature becomes lower. Die1's temperature is about 130 $°C$ with TIM1 thermal conductivity of 2 W/mK, while its temperature is reduced to 77.3 $°C$ with TIM2 thermal conductivity of 5 W/mK. Fig. 4(b) shows the effects of TIM and temperature difference on IR drop. With TIM1, the final voltage of Die1 is 2.455 V, while it is 2.459 V with TIM2. The corresponding IR drop is reduced from 45

mV to 41 mV, about 9% decease when TIM1 is changed to TIM2. It demonstrates that temperature effect on IR drop in PDN can not be neglected and TIM will affect not only the temperature but also the IR drop.

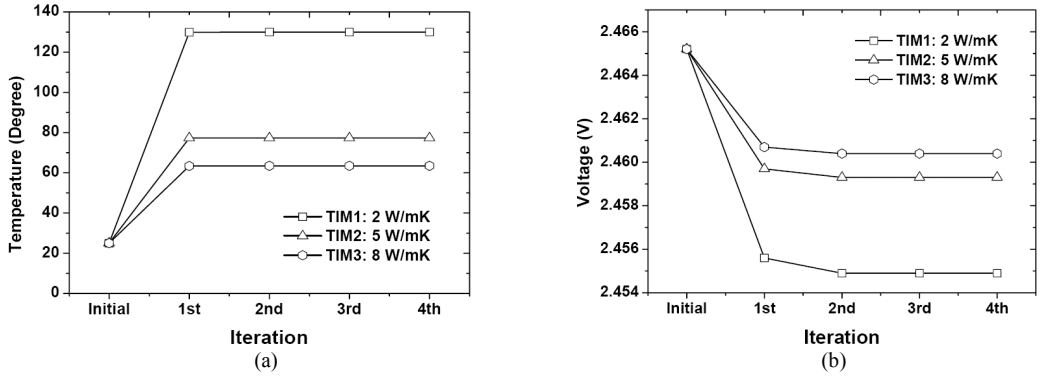


Figure 4. The temperature and IR drop with various TIMs. (a) Temperature (b) IR drop.

B. C4 Density

In the example of 3D package configuration, it is assumed that C4s occupy about 33% of the interface area. In order to study the relationship between C4 density and system performance, the 3D package with TIM2 and three different C4 densities are analyzed. The comparisons are provided in Fig. 5. It shows that with higher C4 density, the bottom Die1 has lower temperature. However, compared to the TIM, the effect of C4 density on temperature is much smaller. This is because the thermal conductivity of C4 is about 60 W/mK, which is much larger than 5 W/mK of TIM2 used in the analysis. Due to relatively smaller temperature change, the C4 density has much less effect on the voltage of Die1 compared to that of TIM as shown in Fig. 5(b).

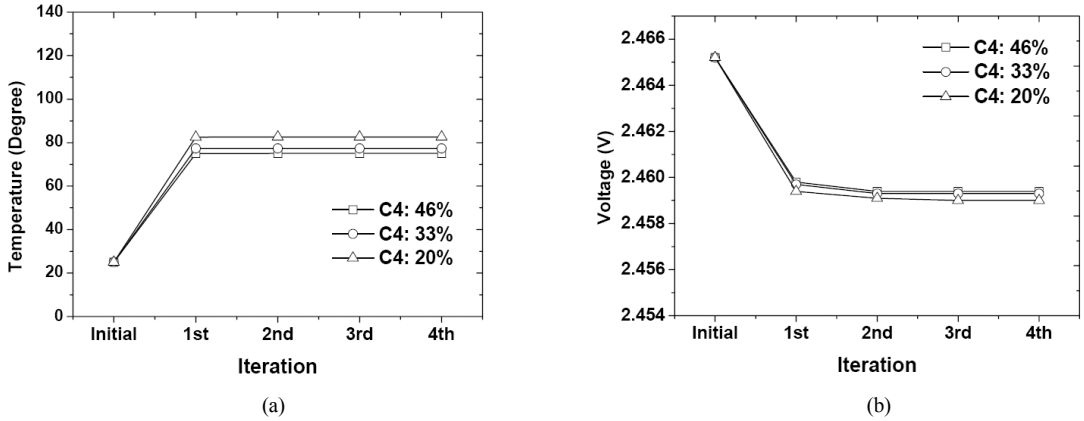


Figure 5. The temperature and IR drop of Die1 with various C4 densities. (a) Temperature (b) IR drop.

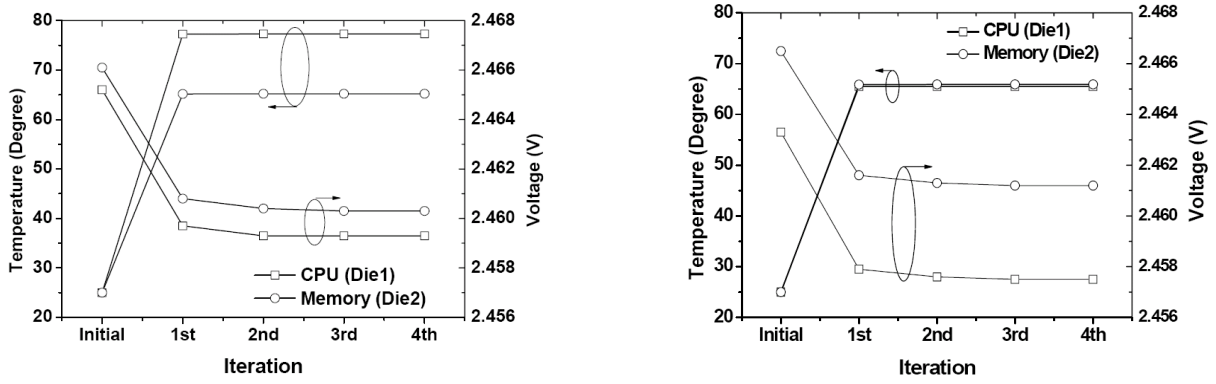
C. Stacking Order

In the package configuration in Fig. 3(a), it is assumed that memory chip (Die2) is stacked on top of CPU chip (Die1). In order to show the stacking order effect, the case of CPU stacked on top of the memory is also analyzed. The IR drop and temperature with TIM2 for those two cases are provided in Fig. 6. Fig. 6(a) illustrates when memory is stacked on top of CPU, the CPU's temperature is much larger than that of the memory and the difference is about $12\,^{\circ}C$. Since the CPU consumes more power and has longer heat conduction path to the heat sink, it has much higher temperature than that of the memory. The highest temperature can be reduced by stacking a high power chip (CPU) on top of a low power chip (Memory). Fig. 6(b) shows that the highest temperature of CPU is reduced to $65.4\,^{\circ}C$, and the temperature difference between the two chips is only $0.5\,^{\circ}C$. From the temperature perspective, it shows that placing the high power consumption chip on top could reduce its hot spot temperature effectively. However, from the IR drop perspective, it is different. Fig. 6(a) and Fig. 6(b) demonstrate that CPU has more IR drop in CPU on top case than that of memory on top case. This is due to longer TSVs used for power supply of CPU when CPU stacks on top of the memory. Therefore, stacking order should be determined by considering both hot spot temperature and maximum IR drop allowed at the same time. There must be a trade off between them.

D. Voltage Source Location

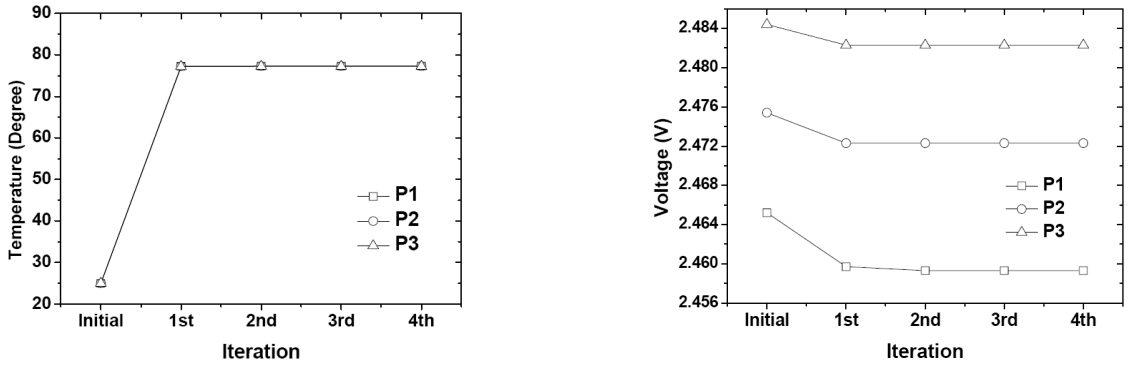
The 3D package example has three different voltage source locations P1, P2 and P3 (see Fig. 3(a)). Fig. 7(a) and Fig. 7(b) illustrate that voltage source location will affect the IR drop without changing the temperature. With voltage source location at P3 which is closest to Die1, the Die1's final voltage is 2.482 V compared to 2.459 V when applying voltage source at P1. The

temperature of Die1 is not affected by the voltage source locations as shown in Fig. 7(a), since its temperature is dominated by the power consumption of the die itself. Therefore, it is important to locate the voltage source as close to the die as possible to reduce its IR drop.



(a) (b)

Figure 6. The temperature and IR drop. (a) Memory on top case (b) CPU on top case.



(a) (b)

Figure 7. The temperature and IR drop of Die1 with TIM2 and three different voltage source locations. (a) Temperature (b) IR drop.

IV. CONCLUSION

In this paper, electrical-thermal co-analysis for PDN of 3D integrated system has been performed with variable parameters analyzed. The co-analysis results demonstrate that the temperature effect on IR drop can not be neglected and it has to be taken into account in PDN design. The thermal conductivity of TIM affects both IR drop and temperature of dies, while the C4 density has much less effects than the TIM. Chip stacking order is also an important factor for determining hot spot temperature and IR drop. The stacking order should be determined by considering trade off between hot spot temperature and maximum IR drop. Finally, voltage source location is a factor which can reduce IR drop without affecting die's temperature.

ACKNOWLEDGMENT

This work was supported by IBM Corporation under the project in Georgia Institute of Technology.

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