Achieving Near Zero SSN Power Delivery Networks by Eliminating Power Planes and Using Constant Current Power Transmission Lines

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Abstract – *Enhanced data rate requires the management of the voltage and timing margins in eye diagrams. This lays a great emphasis on controlling SSN in the power supply network. Thus, the ability of the power delivery network to convey clean power has become more important. In this paper, a practical scheme using power transmission lines is presented. Several accompanying issues are addressed to enable this novel approach for managing noise in the power delivery network. The simulation results demonstrate that with the proposed CC-PTL scheme, SSN-free eye opening can be achieved.*

I. INTRODUCTION

The performance of a system depends highly on the communication speed between the processing unit and memory. Here, one of the major bottlenecks in communication speed is power supply noise [1]. The coupling between signal lines and power delivery network (PDN) in off-chip signaling induces simultaneous switching noise (SSN). Using power/ground planes, SSN is mainly induced by the return current path discontinuity (RPD) and the plane cavity resonance. The return current path in a power plane-based environment is usually disturbed by several kinds of discontinuities such as a power plane split or multiple via holes. Even with a solid return current path, the cavity resonance from the power/ground planes will deteriorate signal transmission. These noise sources constrain the timing margin, and reduce the operating frequency. Therefore, a new type of PDN is required to improve the chip-to-chip communication speed.

The concept of conveying power supply using a transmission line has been suggested previously using power transmission line (PTL) [2]. In that approach, a transmission line replaces the power plane, which eliminates the source of SSN. This can be the most effective method to remove SSN and to increase the per-pin data rate. However, to enable power transmissions lines to work in a real environment, several accompanying issues need to be addressed, namely: 1) DC drop on power supply network caused by DC resistance, 2) Mismatch effect caused by the power transmission line, 3) Line congestion effect due to using lines instead of planes, and 4) Power consumption. First of all, data transition causes the supply current to switch: the high-state of data draws current from the power supply network, but the low-state of data interrupts the current flow. Due to the terminating resistor of the power transmission line, the current through the power transmission line induces DC drop on the power supply network. The resulting DC drop on the power supply network is different from SSN. It is data transition-dependent, and does not affect the data itself. However, the problem arises as mismatch occurs or a PTL supports more than 1 bit. Secondly, since power is supplied through the transmission line, an additional mismatch between the power transmission line and its terminating resistor appears beside a mismatch between the signal transmission line and its terminating resistor. This additional mismatch will not only induce additional voltage reflection but also fail to serve as a backward terminator of the signal transmission line to stop the series of voltage reflections. Hence, the power transmission line reduces the design reliability. Moreover, if one PTL is used per I/O driver, the number of lines on PCB doubles. A solution to relieve line congestion is to support more than one I/O driver with one PTL. Then, the power supply node of several I/O drivers will be tied together so that the amount of current through the power transmission line will vary with the data pattern. This will affect both the power supply node and the output nodes of all the transmitters. Finally, the power consumption should be reasonable when compared with that of the conventional power plane scheme. Once these issues are resolved, the power transmission line will serve as a robust method to deliver clean power with minimum SSN.

In this paper, a practical scheme of using power transmission line for high speed signaling is presented, which is called Constant Current Power Transmission Line (CC-PTL). The proposed CC-PTL scheme solves the first two issues: data transition-dependent DC drop will not occur, and additional mismatch will not happen. This scheme is extended to multiple I/O scheme and verified with simulations. For the multiple I/O scheme, the total power consumption is compared to that of the conventional power plane case along with eye height and jitter.

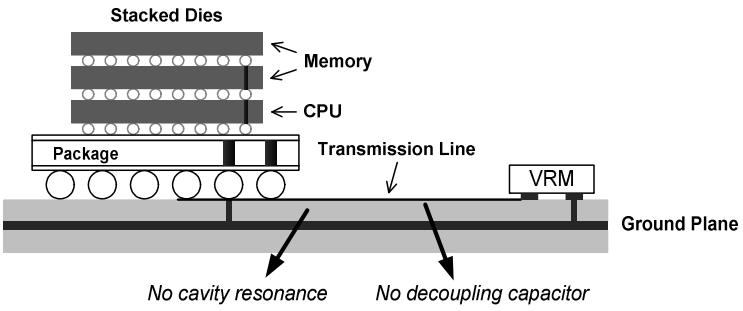


Fig. 1. A system example supplied by a power transmission line

With the newly suggested CC-PTL scheme applied to a real environment, the plane cavity resonance can be removed along with the power plane and decoupling capacitors, as shown in Fig. 1. Also, the return current path loop will be completed without any disturbance, resulting in the absence of RPD.

By eliminating the RPD and plane cavity resonance which are the major noise sources in high speed signaling, this new PDN scheme can improve power integrity, and timing and quality of signals.

II. PROPOSED SCHEME AND SIMULATION RESULTS

A. Single-Ended Signaling

Among the accompanying issues of the conceptual power transmission line scheme in Fig. 2(a), the data-dependent DC drop at the power supply node is illustrated in Fig. 2(b). As the data at the output of the driver, data_tx transits from low to high, current flows through the power transmission line yielding DC drop across the terminating resistance. As a result, the voltage at the power supply node of the driver, TxPwr is a fraction of the original supply voltage. On the other hand, as data_tx transitions from high to low, no current flows through TxPwr so that the node voltage equals the original supply voltage. In case of Fig. 2(b), the impedance values are chosen to dual-match the signal transmission line: Z_0, Z and R_{pmos} equals 50ohm, 25ohm and 25ohm, respectively. While data_tx is high, the voltage at TxPwr drops to 1.875V which is ¾ of the original supply voltage, 2.5V. During the low state of data_tx, TxPwr is floating that the voltage stays to be 2.5V. To remove the DC drop on power supply network, a dummy path is connected to TxPwr as shown in Fig. 3(a). The dummy path consists of a switch and an equivalent resistor. When data_tx is 1, the dummy path is disconnected, and the current flows from the power transmission line toward the signal transmission line. When data_tx is 0, the dummy path is activated so that the same amount of current flows through the dummy path. Consequently, constant current flows through the power transmission line regardless of the data state. It then results in a constant DC drop over the PTL terminating resistance. The potential at TxPwr will be less than the original supply voltage, but constant and independent of the data transition. Moreover, such a DC drop does not reduce the eye amplitude of data_tx and data_rx.

The proposed constant current PTL also solves the additional mismatch problem. When the electrical length of the line is short, the transmission line is a mere wire that connects components. Then, the voltages on the wire at a certain time can be assumed to be the same at all points, and the mismatch effect will not appear. The constant current creates such an environment by eliminating the process to repeatedly charge and discharge the power transmission line. Therefore, the additional mismatch effect is removed as shown in Fig. 4. In the conceptual PTL scheme, when the characteristic impedance of the power transmission line

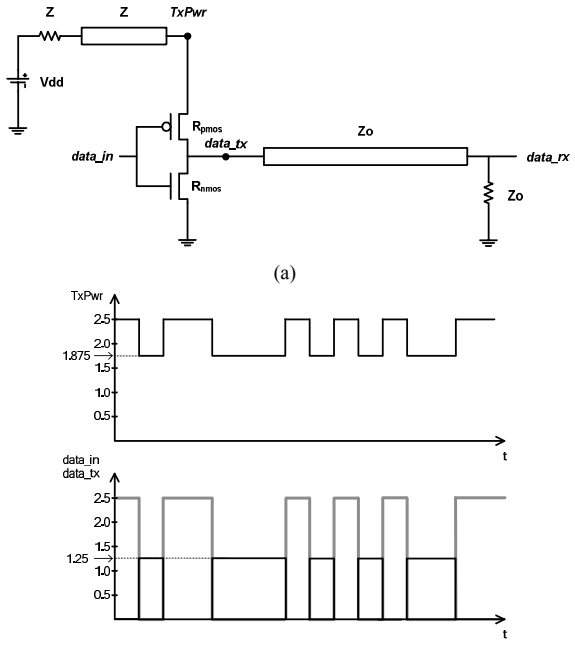


Fig. 2. Conceptual PTL scheme (a) schematic, (b) waveform

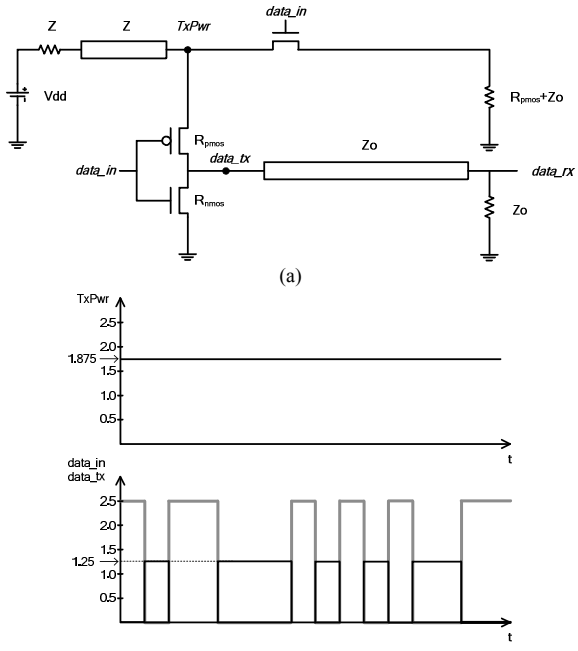


Fig. 3. Proposed CC- PTL scheme (a) schematic, (b) waveform

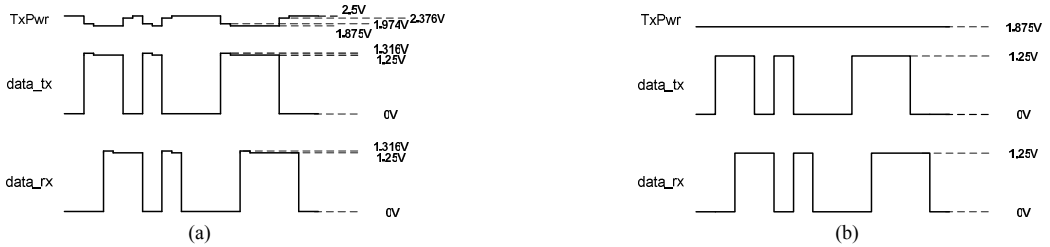


Fig.4. Comparison of mismatching effects (a) conceptual PTL, (b) proposed CC-PTL

is less than the desired value, the distortion due to reflection appears on the power supply node and the data nodes (Fig. 4(a)). However, in the proposed CC-PTL scheme, such a mismatch effect is not found as shown in Fig. 4(b).
The eye diagrams of data_rx in the conventional power plane scheme and the proposed CC-PTL scheme are shown in Fig. 5. The eye height of power plane case is 1.085V, which is only 86.8% of the desired height (Fig. 5(a)), while that of CC-PTL case is 1.18V, which is 94.4% of the desired height (Fig. 5(b)). The jitter of the power plane case is 4.43 psec, while that of the CC-PTL case is 0 psec. The small distortion seen on the eye of CC-PTL case is due to port discontinuity in 3D simulation. The CC-PTL scheme offers better jitter performance as well as larger voltage margin.

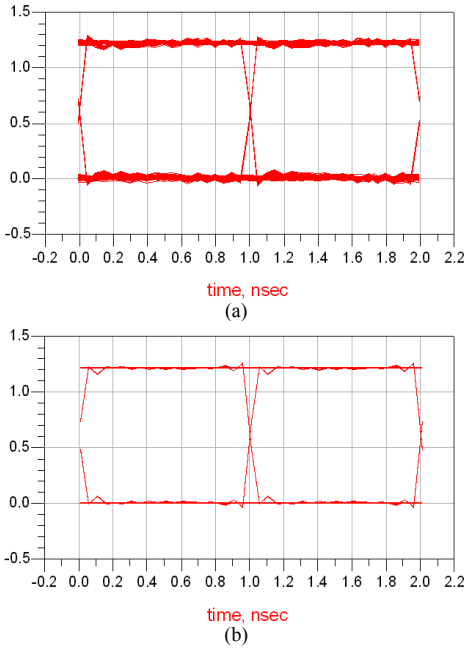


Fig. 5. Eye diagrams of received data, data_rx (a) conventional power plane case, (b) CC-PTL case

B. Differential Signaling

In single-ended signaling, the dummy path is attached intentionally to the circuit. However, in differential signaling, the natural dummy path is created. As shown in Fig. 6(a), two kinds of current loops are formed according to the state of the data. During the high-state of data_tx, the current flows along the dotted-line. During the low-state of data_tx, the current flows along the dashed-line. Both the dotted-line path and the dashed-line path consist of the same components and hence are actually the same current loop. Both current loops have the same kind of influence on TxPwr node and output nodes. The eye diagram of the received data (data_rx - data_rx') in differential signaling with CC-PTL is shown in Fig. 6(b). The eye height is 2.316V, which is 92.6% of the desired size. In Fig. 7, the schematic and the resulting eye diagram of the conventional power plane case are illustrated. Here, the balance of the differential line is intentionally broken by splitting the power plane. The eye height is 1.991V, which is only 79.6% of the desired size. Although a pair of differential lines affords the return current path by itself, signal integrity still depends on the PDN environment for its balance. Hence, the CC-PTL scheme can also be effective in differential signaling when the balance of symmetry between a pair of coupled lines is upset.

III. Extension to Multiple I/Os and Reducing Power Consumption

The only problem of CC-PTL is the increased power consumption in single-ended signaling due to the artificial dummy path and the constant current. Since the current flows during both the low-state and high-state of the data, the power consumption doubles. This problem can be mitigated when the proposed CC-PTL scheme is applied to multi-I/O single-ended signaling.
The total power consumption can be decreased if the target eye height is reduced. It is illustrated in Table 1. Here, it is assumed that the power 'P' is consumed when the eye height is ½ of V_{DD} in the power plane case. The relative amount of power in the CC-PTL case is listed in Table 1. As the eye height reduces from ½ to ⅓ and ¼ of V_{DD}, the power consumption of the CC-PTL

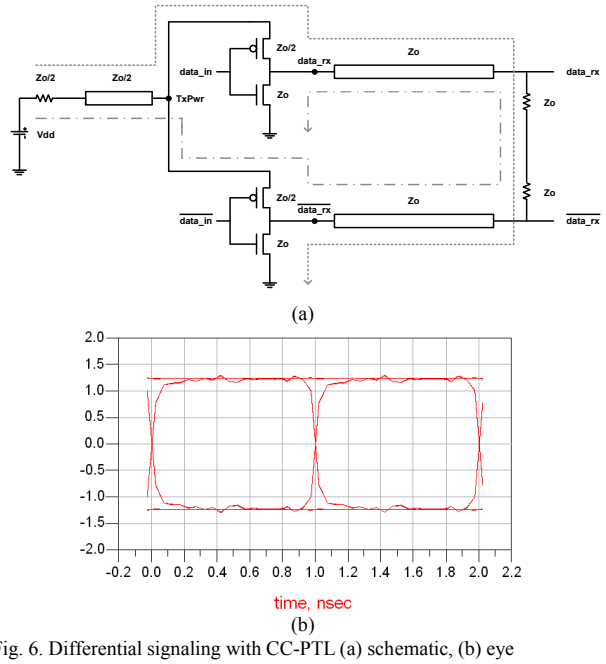


Fig. 6. Differential signaling with CC-PTL (a) schematic, (b) eye

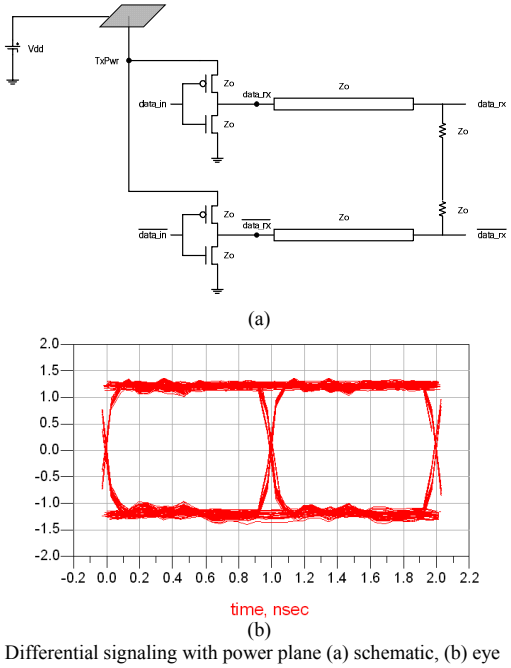


Fig. 7. Differential signaling with power plane (a) schematic, (b) eye

case decreases from 2P to 1.33P and P, respectively. Hence, the trade-off between the target eye height and the power consumption can be used to save power. This is possible because in the power plane case, the actual eye size at the receiver side grows less than the target eye size as the number of I/O driver connected to a PDN increases.

Table 1. Comparison of power consumptions

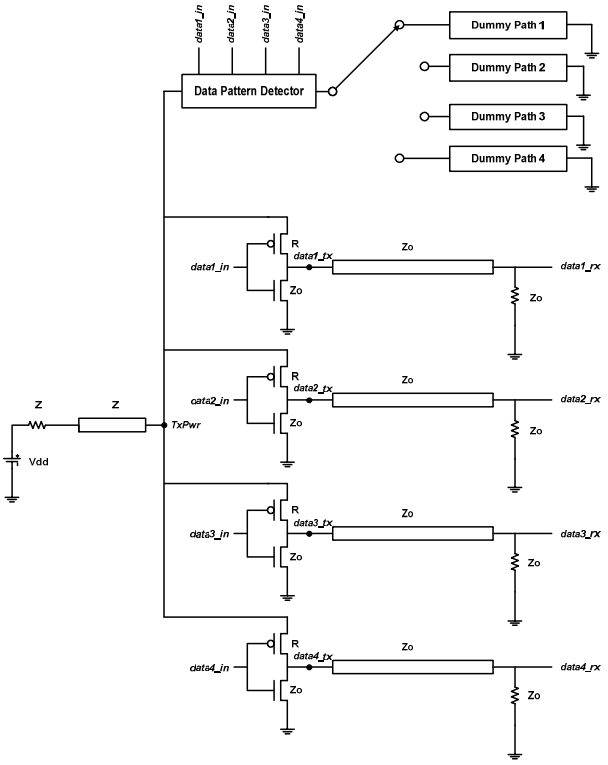
eye height	Power consumption	
	Power Plane	CC-PTL
$V_{DD}/2$	P	2P
$V_{DD}/3$	-	1.33P
$V_{DD}/4$	-	P

With the conventional power plane scheme, SSN due to the plane cavity worsens as the number of I/O driver supplied by the power plane increases. It is shown in Table 2: the growing bit number decreases the eye height. The actual eye height is 1.085V in 1-bit case, which is 86.8% of the target height, and even decreases to be 1.006V in 4-bit case, which is only 80.5% of the target height. Although the target eye height of the power plane scheme is ½ of V_{DD}, the actual achieved eye height is reduced to be closer to ⅓ of V_{DD} in 4-bit case. Moreover, the growing bit number increases the peak-to-peak jitter. The jitter is about 4.43psec, which is about 0.5% of the pulse width in 1-bit case, and increases gradually with the bit number. However, with the SSN-free CC-PTL scheme, the increasing bit number causes hardly any harm to signal integrity. Here, the target eye height is reduced to ⅓ of V_{DD} for reasonable power consumption. The actual eye height of the received signal is nearly equal to the target eye height even with the increasing bit numbers. As a result, the actual eye height of the CC-PTL scheme when its target eye height is ⅓ of V_{DD} is comparable to the actual eye height of the power plane scheme when its target height is ½ of V_{DD}. Moreover, the jitter does not appear. Hence, as the bit number connected to the power supply line increases, the trade-off can be used to achieve better eye opening with reasonable amount of power consumption. Furthermore, the line congestion is relived by extending the proposed CC-PTL scheme to multi-I/O single-ended signaling.

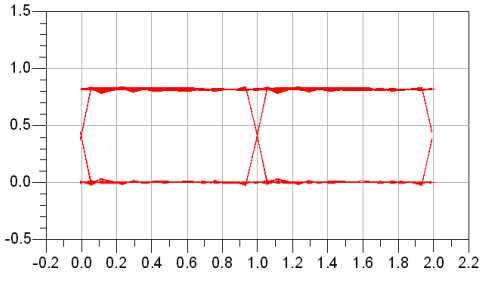
In Fig. 8(a), the schematic of 4-bit single-ended signaling with the CC-PTL scheme is shown. The power supply nodes of four I/O drivers are bound together. Four kinds of dummy paths are connected to TxPwr node, and the data pattern detector selectively activates one dummy path at a time. All the component values are selected to generate the target eye height of ⅓ of V_{DD} and to dual-match the signal transmission line at the same time. The eye diagram of data1_rx is shown in Fig. 8(b). The eye amplitude is 0.803V, 96.4% of the desired height, and the jitter is 0 psec.

Table 2. Comparison of eye openings and jitters

bit	eye height (V)		Jitter (ps) @1Gbps	
	Power Plane (Target: 1.25V)	CC-PTL (Target: 0.833V)	Power Plane	CC-PTL
1	1.085	0.816	4.43	0
2	1.062	0.813	4.43	0
3	1.037	0.809	8.87	0
4	1.006	0.803	8.87	0



(a)



(b)

Fig. 8. CC-PTL scheme for 4-bit I/O (a) schematic, (b) eye

IV. Conclusions

In this paper, a practical scheme of using the power transmission line for high speed signaling is presented. The proposed CC-PTL scheme removes the alternating DC drop on power supply network by using dummy path. The dummy path induces constant current through the power transmission line so that it omits the process of charging and discharging the transmission line. Therefore, CC-PTL is free from any mismatch or discontinuity in the power supply path. The simulation result proves that the CC-PTL scheme provides superior jitter performance and larger eye amplitude. The application of the proposed CC-PTL scheme is extended to differential signaling and multi-I/O single-ended signaling. In addition, the total power consumption is comparable to that of the conventional power plane case.

References

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