Minimizing the Number of Basis Functions in Chip-Package Co-Simulation Using Lauerre-FDTD

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Abstract - Interaction between the chip and package at the system level needs to be predicted in the design process for saving time and cost, which requires chip-package co-simulation. Laguerre-FDTD is an unconditionally stable FDTD scheme which is attractive for chip-package co-simulation since its time-step is not limited by the Courant condition. In Laguerre-FDTD, the transient waveform of the field of interest is represented as the weighted sum of Laguerre basis functions. Therefore, the number of basis functions used in the simulation is directly related to both the simulation run time and the accuracy. Normally, there is a tradeoff between simulation run time and the accuracy. However, this paper proposes a novel solution to minimize the number of basis functions while increasing the accuracy of the output transient waveform of interest. The method for maximizing the efficiency in terms of run time and improving the accuracy of simulation described in this paper is a key step for the automation and practical use of the transient simulation technique using Laguerre polynomials.

I. INTRODUCTION

As the complexity of electronic system goes higher, while the system size shrinks, power/signal integrity assessment through chip-package co-simulation is required to accurately predict the system's behavior as to avoid the system failure. In the transient simulation of the chip and the package structures together, major challenge comes from the multi-scale dimension of the structures, as shown in Fig. 1. Dimensions of the interconnections in the chip and the package are between

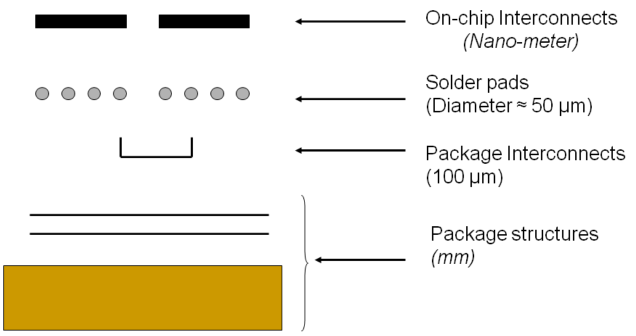


Figure 1. Multi-scale dimension of chip-package structure

nanometer (nm) range and the millimeter (mm) range, resulting in a scale ratio of $1{:}10^6$. Such multi-scale structures are difficult to be analyzed using finite-difference time-domain (FDTD) technique due to Courant stability condition [1] [2].

As an alternative to the FDTD scheme, unconditionally stable FDTD using Laguerre polynomials has been proposed [3], which is called as Laguerre FDTD. In the Laguerre-FDTD, time-steps larger than the Courant limit can be used, enabling faster simulation for multi-scale problems. While ADI-FDTD suffers from dispersion when time-step is larger than Courant time-step [4], since the Laguerre-FDTD is marching-on-degree scheme, selection of time-step does not affect the simulation's accuracy as long as time step is sufficiently small to support Laguerre transform of source and transient response of the system. Since the introduction of the Laguerre-FDTD scheme, several modifications have been made to the algorithm to enhance its performance [5]. The modified algorithm has been named SLeEC which stands for "Simulation using LaguerrE Equivalent Circuit." In [6], it has been shown that SLeEC can significantly reduce the simulation time without compromising the accuracy.

In both Laguerre-FDTD and SLeEC, a time domain wave form is represented as a sum of Laguerre basis functions scaled by Laguerre basis coefficients. Although use of infinite number of basis functions provides perfectly accurate solution, due to finite resource and time, the time domain waveform should be approximated with the finite number of basis functions. Therefore, choosing right number of basis functions is critical to the accuracy of simulation. [6] proposes a criterion to decide the right number of basis functions based on error analysis at the initial value. Although it provides a useful guideline to determine the number of basis functions, it could not remove spurious oscillations at early time, similar to Gibb's effect at Fourier transform which comes from using finite number of Laguerre basis functions. Also, finding the right number of basis function by minimizing error at the initial value could provide a statistically meaningful guideline to minimize error over global time duration. However, it does not always give the best result.

In this paper, a method for minimizing error over global simulated time duration with minimum number of basis functions is proposed, which can accelerate the simulation by upto two times, by reducing the number of basis functions, while enhancing accuracy. Considering that the simulation run time and accuracy have a tradeoff relation, improvement by this method is remarkable. The proposed method has been tested and verified by applying it to two chip-package co-simulation examples.

This paper is organized as follows: The SLeEC methodology is discussed in section II. In section III, limitations of prior work are discussed. Proposed method to overcome such limitations is described in detail in section IV. Simulation result from a test case is provided in section V, followed by the conclusion.

II. SLeEC Methodology

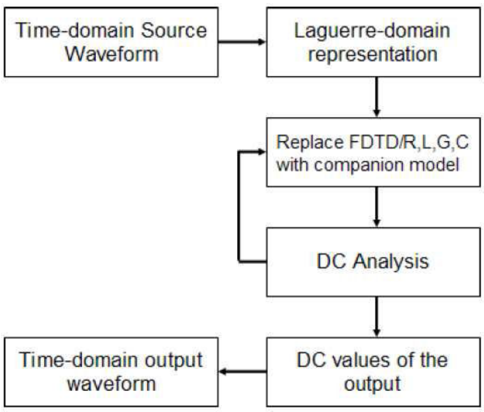


Figure 2. Flowchart of SLeEC methodology

Figure 2. shows a flowchart of SLeEC Methodology. Only a qualitative description of SLeEC is given in this section. Mathematical details are available in [6]. The left column in Figure 2. represents operations done in the time-domain and the right column represents the Laguerre-domain. The first step is to convert a time-domain source waveform from the time domain into the Laguerre domain by representing the time domain waveform using Laguerre basis functions. The Maxwell's equations on FDTD grid in the time-domain is replaced by an equivalent circuit model composed of resistors, voltage controlled-current sources and independent current sources in the Laguerre domain. In the circuit model of the FDTD grid, the DC solution of the nodal voltages represents electric-field Laguerre coefficients and the branch currents represent magnetic-field Laguerre coefficients. For each of the coefficients that represent the source-waveform, a DC analysis is done once. At the end of each DC analysis, the solution is used to update the companion model before the next DC analysis is done using the next value of the Laguerre-domain coefficient of the source-waveform. Although the number of DC analysis is same as the number of Laguerre coefficients representing the source-waveform, inversion of matrix is needed only once since the companion model has the same circuitry and resistors for every DC analysis. The final step is to convert the values obtained from the DC solution of the output field of interest into a time-domain waveform.

III. Limitations of Prior Work

As stated earlier, any time-domain waveform *W(t)* is represented as a sum of Laguerre basis functions scaled by Laguerre basis coefficients W_p as shown in (1).

$$W(t) = \sum_{p=0}^{\infty} W_p \varphi_p(t) \tag{1}$$

In the SLeEC scheme, for efficiency, time-domain waveform *W(t)* is approximated with only first *N* basis functions as long as error from the approximation is negligible.

$$W(t) \cong \sum_{p=0}^{N} W_p \varphi_p(t) \tag{2}$$

To choose proper *N*, the number of basis functions, [5] proposes calculate the energy contained in the time-domain waveform as a summation of the L^1 norm and analysis error at the initial point (in general, time t=0). Minimizing error at the

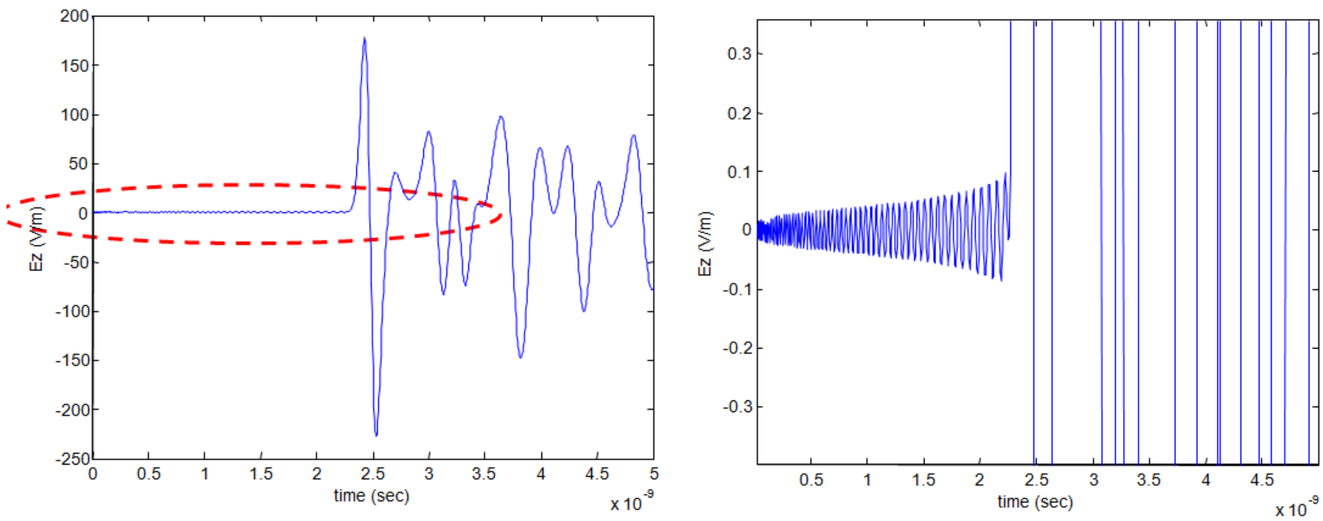


Figure 3. Spurious oscillations (Left: Simulated time-domain waveform, Right: zoomed-in view of the dashed area)

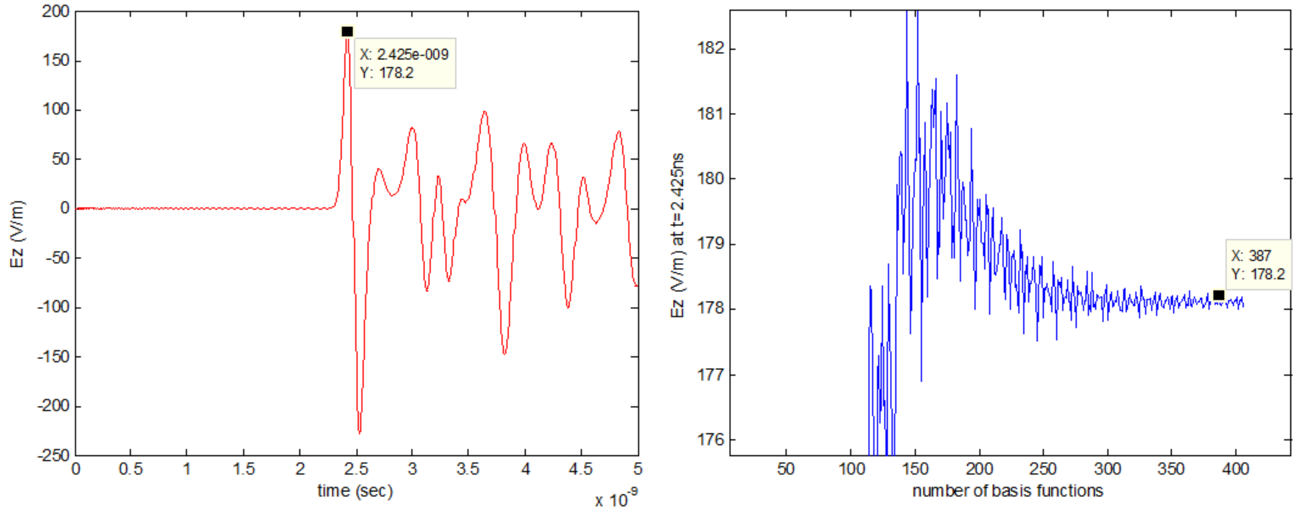


Figure 4. Converging trend (Left: the time-domain solution, Right: the time-domain solution at time t=2.425ns as function of the number of basis functions)

initial point is statistically meaningful in the minimization of error over the whole simulated time duration. However, it does not guarantee the minimum error over all simulated time duration.

Also, as shown in Fig. 3, from the nature of use of the finite number of basis functions, spurious oscillations at early times are inevitable although their magnitudes are not significant.

IV. Obtaining Accurate Transient Waveform

As N goes to infinity, the approximated solution with first N basis functions converges to its exact solution. For fixed time $t=t_{fix}$, while the time-domain solution at the time point is converging to the exact solution as the number of basis function increases, the solution fluctuates near the exact solution and the magnitude of the fluctuation is decaying as shown in Fig. 4. Therefore, applying a low-pass filter on such a converging trend enhances the accuracy of solution by removing small glitches, thus requiring smaller number of basis functions for faster convergence. The following infinite impulse response (IIR) filtering is chosen to wipe out such glitches.

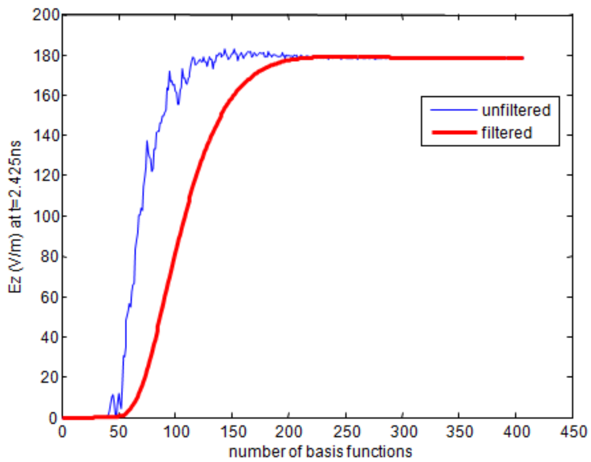


Figure 5. Convergence of the filtered solution

$$W(N,t) \cong \sum_{p=0}^{N} W_p \varphi_p(t) \quad (3)$$

$$W_1(N,t) = \sigma_1 W_1(N-1,t) + \frac{1}{1-\sigma_1} W(N,t) \quad (4)$$

$$W_2(N,t) = \sigma_2 W_2(N-1,t) + \frac{1}{1-\sigma_2} W_1(N,t) \quad (5)$$

W_2 is the filtered solution where σ_1 and σ_2 are related to the strength of the filtering whose values are between 0 and 1. Both σ_1 and σ_2 are empirically chosen as 0.95 in the examples in this paper. As shown in Fig. 5, the filtered solution converges more quickly and smoothly than the unfiltered solution, and is without glitches.

Since the filtered solution converges more quickly to the solution, use of much fewer number of basis functions is allowed, while enhancing the accuracy. Since the simulation run time is directly proportional to the number of basis functions in SLeEC methodology, using fewer basis functions results in the reduced simulation run time. On the other hand, by filtering the solution at each time point, error is minimized for the overall simulated time duration. Therefore, spurious oscillations in early times are made to disappear as shown in Fig. 6.

V. Test Case I - Chip-Package Structure

The bird's eye view of the modeled structure is shown in Fig. 7(a). The on-chip structures, along with the interface between the chip and the package, are shown in Fig. 7(b). The zoom-in of the region marked by the circle in Fig. 7(b) is shown in Fig. 7(c). The on-chip structures in Fig. 7(c) represent the interconnections in M1 and M2 layers of an

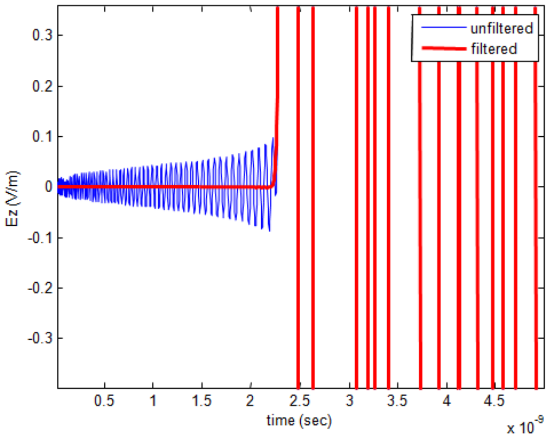


Figure 6. Removal of spurious oscillations by filtering

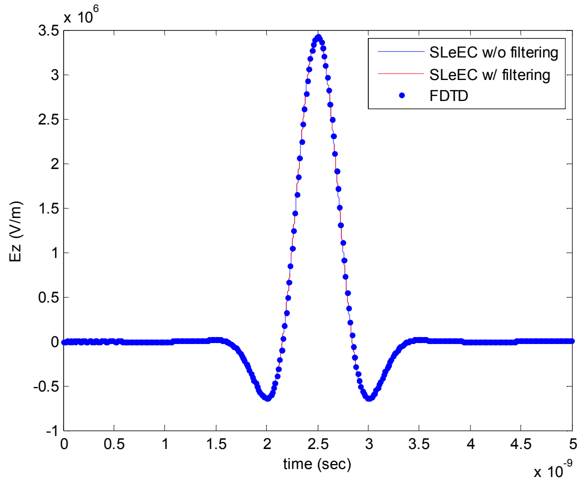


Figure 8. Comparison of simulated time-domain waveform

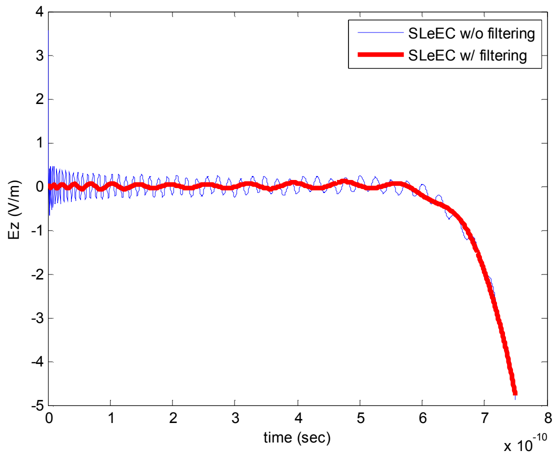
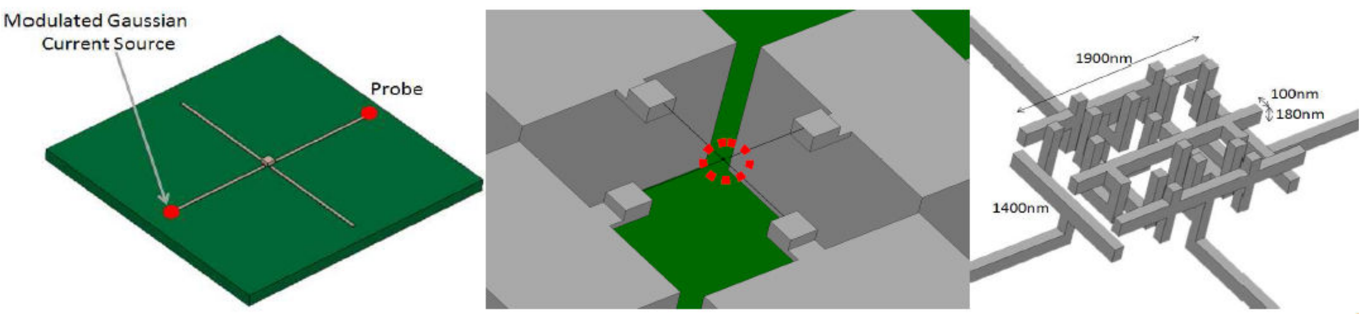


Figure 9. Reduction of spurious oscillations in early time

SRAM cell. The structure has on-chip interconnects in the metal layers M1 and M2, connected by vias and routed on the redistribution layer, through the solder pads, to the package and routed as package-level interconnects. A feature of the chip-package structure is the multi-scale dimension from the nanometer (nm) range to the millimeter (mm) range, resulting in a scale ratio of 1:50,000 in this example. The on-chip structures that are in the nm scale require a very fine mesh, and therefore the simulation time can become prohibitively large using the conventional FDTD scheme due to the Courant time-step condition. The time-domain response of the electric field at the location marked probe in Fig. 7(a) up to 5ns has been computed. A modulated Gaussian current source is used to excite the structure at the end of the package trace as shown in Fig. 7(a). The structure has been simulated using the conventional FDTD, SLeEC without filtering, and SLeEC with the proposed method. The normal SLeEC scheme without filtering requires 502 Laguerre basis functions while SLeEC with the proposed filtering process needs only 368 basis functions, which speeds up the simulation by 33%, from 9 minutes to 6 minutes. Comparison shows very good correlation between SLeEC and FDTD, as shown in Fig. 8. Since the simulated waveforms from SLeEC with and without filtering are perfectly overlapped, they are indistinguishable in the figure. Early time spurious oscillations are suppressed by filtering as shown in Fig. 9. While FDTD takes 30 hours, SLeEC with the proposed method took only 6 minutes to finish the simulation for the same structure with the same number of cells. This represents a 300x speed-up over the conventional FDTD scheme. The simulations were run on a Pentium quad core, 2.4GHz processor with 4GB RAM.



(a) (b) (c)

Figure 7. The bird eye's view of test case

VI. TEST CASE II – COUPLED TRANSMISSION LINES

A second test example consists of coupled transmission lines in PEC box, as shown in Fig. 8. The microstrip lines have a dielectric substrate with permittivity ε_r = 4.3 and thickness $h1$ = 200 um, a perfect electric conductor strip of width W = 0.3 mm, thickness t = 10 um, distance between transmission lines d = 0.3 mm, $h2$ = 1.0 mm, and M = 20.9 mm. The length of both transmissions is 90 mm. The structure is discretized into 100 × 29 × 3 cells where smallest and largest mesh size is 0.01 mm and 1 mm, respectively. Gaussian derivative current source shown in Fig. 8 is excited at one end of one transmission line. Electric fields between conductor and bottom plane at other microstrip line's near and far end are measured. In the FDTD scheme, according to the Courant stability condition, time-step needs to be smaller than 66 fs, which consumes over 7500 iterations and 23 minutes to run the simulation for 5 ns. However, SLeEC could solve the structure within 5 minutes with 470 basis functions using the proposed method, which is 4 times faster. The simulated transient response shows good correlation with the FDTD simulation, as shown in Fig. 9.

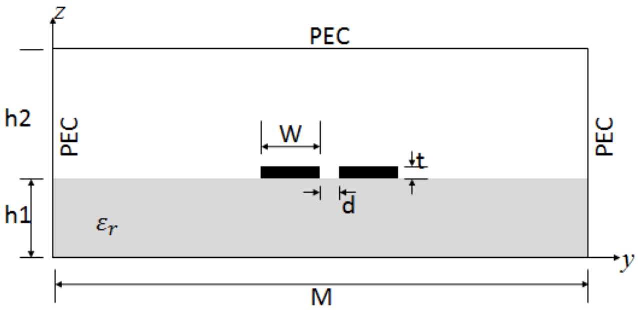


Figure 8. Cross section of test case II.

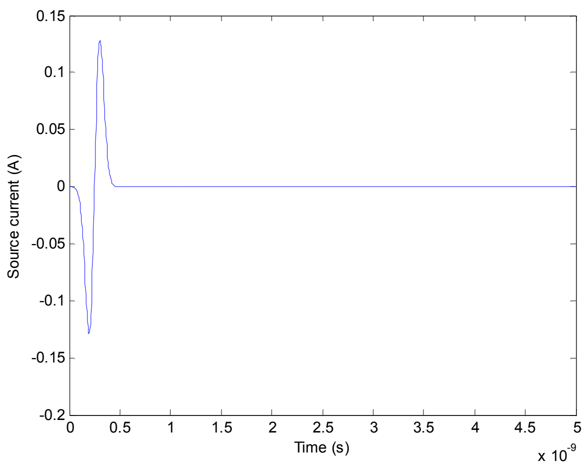


Figure 9. Source waveform

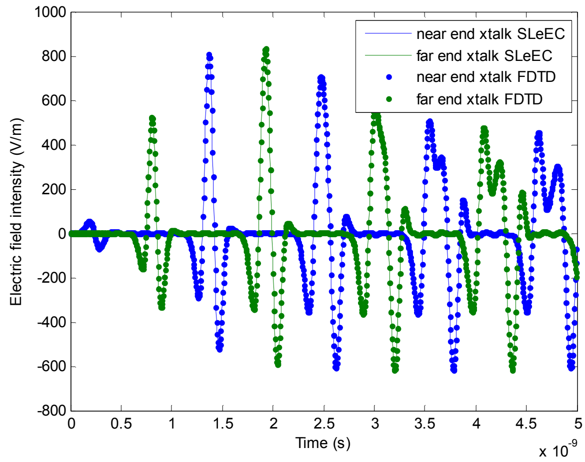


Figure 10. Simulated transient response

VII. CONCLUSIONS

In this paper, a method for reducing the simulation run time and increasing the accuracy using SLeEC methodology is proposed. The proposed method reduces spurious oscillations in early time as well. The proposed method is verified through chip-package co-simulation example and shows that transient simulation results obtained by this method is 300x faster than FDTD while maintaining the accuracy.

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