Decoupling Capacitor Placement in Power Delivery Networks Using MFEM

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***Abstract*— The impedance of the power distribution network (PDN) needs to be minimized in order to prevent unwanted voltage fluctuations at frequencies where current transients occur. To reduce PDN impedance, one can place decoupling capacitors that act as local current sources. However, selecting and placing the right capacitors at the right locations are problematic because of the complexity of modern package and board structures. In addition, decoupling capacitors are not effective at higher frequencies, requiring more complicated techniques such as embedded decoupling. This paper introduces a method of reducing the effort expended by the complex task of decoupling capacitor placement: a genetic algorithm that is customized for the selection and placement of decoupling capacitors. The core engine of this optimizing algorithm is a recently developed technique, the multilayer finite element method (MFEM), which solves for PDN impedances. This paper also highlights a method of incorporating vertical circuit elements into MFEM. Using several test cases, it proves the validity of the inclusion of vertical elements in MFEM and the effectiveness of the optimizer.**

***Index Terms*— Decoupling capacitor, finite element method, genetic algorithm, power delivery network.**

I. Introduction

A POWER delivery network (PDN) is designed to provide a constant voltage, especially to chip pads, even when the chip draws hundreds of amperes of current from DC to the gigahertz range of frequencies. To keep the PDN voltage within a tolerance level, the impedance of the PDN must be maintained below the target impedance throughout the frequency range of interest. When the maximum voltage ripple allowed is 5%, the target impedance is defined as

$$Z_{tar} = \frac{V_{dd} \times 5\%}{I \times 50\%} \tag{1}$$

where V_{dd} is the power supply voltage and I is the current drawn by the device over an entire clock period. It is assumed that 50% of the switching current flows at each rise and fall time [1]. The required target impedance must fall within the frequency band of the transient current [2], and it becomes even smaller as the demand for current increases and the voltage requirement decreases.

Manuscript received September 2, 2010; revised June 14, 2011; accepted August 7, 2011. Recommended for publication by Associate Editor M. Cases upon evaluation of reviewers' comments.

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Digital Object Identifier 10.1109/TCPMT.2011.2165954

As the frequency of the driver excitation reaches or exceeds the gigahertz frequency range, power/ground plane pairs begin to support radial waves. Since the boundaries of the power planes are open circuits, these waves resonate at discrete frequencies. As a result, the voltage on the plane is no longer constant. A typical technique of reducing the excessive voltage fluctuation of the PDN is to place decoupling capacitors across the power pins [3]. However, capacitors are not effective beyond their self-resonant frequencies because they become inductive [4], [5]. For example, although the surface mount discrete capacitors are effective from several kilohertz to hundreds of megahertz, they become ineffective at higher frequencies due to the loop inductance created between the switching circuits and the capacitors. To mitigate this problem, either complementary metal-oxide semiconductor or high-K MIM decoupling capacitors, which are effective above hundreds of megahertz, can be placed on the chip. However, placing a number of capacitors while avoiding routing blockage is very difficult due to the limited space in the on-chip area [6], [7].

Considerable research has been devoted to developing techniques that reduce PDN noise by placing decoupling capacitors. One well-known technique is to reduce the loop inductance formed between the vias of an active device and a decoupling capacitor by placing the capacitor close to the active devices [8]–[11]. Another technique is to place the capacitors where the voltage maxima occur [12]. However, since the different circuits and board layouts require diverse strategies, the selection of right capacitors and their placement is complicated and time consuming. Moreover, placing a number of capacitors in the limited area of the package PDN becomes more challenging as the size of the modern systems decreases.

Selection and placement of decoupling capacitors can be automated by an optimizer. Among many of the optimization algorithms, the genetic algorithm (GA) is a technique that approaches an optimal solution heuristically. Based on the principles of natural selection and evolution, the GA produces several solutions to a given problem. The GA is especially effective at finding a quality solution from a very large number of possible solutions [13], proving to be suitable for decoupling capacitor selection and placement. Although the GA can provide the best solution in the end, it may take longer to complete the optimization than other situation-specific algorithms. Thus, customizing the GA optimizer for a specific situation (in this case, the selection and placement of decoupling capacitors on a PDN) will enhance the efficiency of the optimization. Customization of the GA for a decou-

pling capacitor problem can employ the previously explained techniques of decoupling.

The nature of the GA requires a fitness evaluation at each iteration step, which in turn requires the analysis of a PDN with decoupling capacitors. Since the majority of the computation time for the optimization is spent on the PDN analysis, the computational efficiency of the numerical analysis is highly desirable. In [14], the optimization employs the cavity resonator model to obtain impedance profiles of the PDN. However, the application of the cavity resonator model is limited to the solid rectangular and single plane pair structure, it is not suitable for multilayered and/or irregular structures. The optimizer using the GA for decoupling capacitors in [15] uses the multilayer finite difference method (MFDM), which is ideally suited for solving multilayer-structure problems and is computationally efficient compared to full-wave electromagnetic solvers [16]. However, MFDM creates a uniform square mesh, which is not ideal for irregularly shaped structures. Moreover, for multiscale structures, the rectangular mesh can create too many unknowns, which becomes computationally expensive.

This paper employs multilayer finite element method (MFEM), which is a finite element-based technique for solving PDN impedance problems [17]. Since the method deals with a 2-D Helmholtz equation, its computation is more efficient than that of a general 3-D FEM method while preserving its accuracy at the same time.

The original contributions of this paper are as follows.

1) Development of a new formulation that is an extension of [18] using MFEM for analyzing multilayered PDNs with multiscale geometries.
2) Development of a nonuniform triangular meshing scheme for multilayer structures by collapsing all the layers into a single layer.
3) Development of a customized GA for the selection and the placement of capacitors.

The rest of this paper is organized as follows. Section II outlines MFEM and describes the incorporation methodology of the decoupling capacitor into the model. Section III illustrates the GA and its specialization for decoupling capacitor problems. Section IV shows the results of MFEM with many decoupling capacitors and a problem-specific GA using MFEM. Finally, Section V concludes this paper.

II. Modeling Formulation: MFEM

The optimizer for a decoupling capacitor utilizes MFEM, which yields the computationally efficient and accurate impedance profile of a PDN. A typical PDN structure can be modeled as a planar circuit in which the 3-D is electrically much smaller than the others. Thus, the field along the shortest dimension is assumed to be invariant, leading to the 2-D Helmholtz equation

$$\left(\nabla_T^2 + k^2\right) u = j\omega\mu d J_z \tag{2}$$

where

$$\nabla_T^2 = \left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}\right) \tag{3}$$

in which k is the wave number, u the voltage, d the thickness of the dielectric between the planes, J_z the current density excited normally to the planes, and ∇_T^2 the transverse difference operator [19], [20]. Since the boundaries of the structure are open circuited, the Neumann boundary condition is applied to the formulation.

A. Single Plane Pair

A standard finite-element approximation with a triangular mesh and linear pyramid basis functions leads to the weak form of the partial differential equations [21]

$$\sum \iint_{\Omega} \left(\nabla\phi_p \cdot \nabla\phi_q + \omega^2\mu\varepsilon\phi_p\phi_q + j\omega\mu d J_z\phi_p\right) dxdy = 0 \tag{4}$$

where Ω represents the problem domain and ϕ s the pyramid basis and testing functions. For simplicity, the Cartesian coordinates are converted into simplex coordinates $\{L1, L2, L3\}$ [22] to obtain

$$\begin{aligned} L_p &= \frac{1}{2\Delta}(a_p + b_p x + c_p y) \\ a_p &= x_{p+1}y_{p+2} - x_{p+2}y_{p+1} \\ b_p &= y_{p+1} - y_{p-1} \\ c_p &= x_{p-1} - x_{p+1} \end{aligned} \tag{5}$$

where Δ is the area of the triangle with vertices at $p-1$, p, and $p+1$, and the subscripts are evaluated modulo $3+1$, which circulate at multiples of three. Since pyramid-basis and testing functions are equivalent to the simplex coordinates within the cell, (5) can be considered as nothing but a matrix equation

$$(\overline{\overline{K}} + \overline{\overline{M}})\overline{U} = \overline{F} \tag{6}$$

where $\overline{\overline{K}}$ and $\overline{\overline{M}}$ are stiffness and mass matrices, respectively, the elements of $\overline{U}$ contain the unknown potential at each node, and $\overline{F}$ is the current source vector. The entries of $\overline{\overline{K}}$, $\overline{\overline{M}}$, and $\overline{F}$ are

$$\begin{aligned} k_{p,q} &= \iint_{\Omega} \frac{j}{\omega\mu d}\nabla\phi_p \cdot \nabla\phi_q dxdy \\ m_{p,q} &= \iint_{\Omega} \frac{j\omega\varepsilon}{d}\phi_p\phi q dxdy \\ f_p &= \iint_{\Omega} J_z\phi_p dxdy. \end{aligned} \tag{7}$$

Using the equivalency of the pyramid-basis/testing functions and the simplex coordinates within the cell, we obtain the following:

$$\nabla\phi_p = \nabla L_p = \frac{1}{2\Delta}\left(\hat{x}b_p + \hat{y}c_p\right) \tag{8}$$

which converts $k_{p,q}$ in (7) to

$$k_{p,q} = \frac{j}{\omega\mu d}\frac{b_p b_q + c_p c_q}{4\Delta} \tag{9}$$

which is rewritten in terms of the local coordinates.

Similarly, we obtain $m_{p,q}$ and f_p in simple representations. The Jacobian (10) can be used to transform the Cartesian coordinates into simplex coordinates

$$dxdy = dL_1 dL_2 \frac{\partial(x, y)}{\partial(L_1, L_2)} = 2\Delta d L_1 L_2. \tag{10}$$

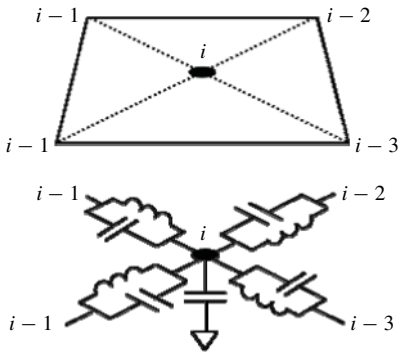


Fig. 1. Equivalent circuit representation of admittance matrix $Y = K + M$.

By noting that the transformed equation is in the form of

$$I = \int\int_{\Omega} L_1^a L_2^b L_3^c dL_1 dL_2 = \frac{a!b!c!}{(a+b+c+2)!} \tag{11}$$

where a, b, and c are integer powers [22], the substitution for $a = 2$, $b = 0$, and $c = 0$ when $i = j$, and for $a = 1$, $b = 1$, and $c = 0$ when $i \neq j$ produces

$$m_{p,q} = \begin{cases} \frac{\Delta}{6}\frac{j\omega\varepsilon}{d}, & p = q \\ \frac{\Delta}{12}\frac{j\omega\varepsilon}{d}, & p \neq q. \end{cases} \tag{12}$$

Similarly, substitution for $a = 1$, $b = 0$, $c = 0$ results in

$$f_p = J_z \frac{\Delta}{3}. \tag{13}$$

B. Equivalent Circuit Representation

Since matrices $\overline{\overline{K}}$ and $\overline{\overline{M}}$ are expressed as the admittance matrices of inductive components and capacitive components, respectively, they can be represented as equivalent circuit models. In order to prove this, one 3×3 local matrix of $\overline{\overline{K}}$ can be evaluated by summing up the first row entries

$$Sum(k_{1,q}) = \sum_{q=1}^{3} \frac{j}{\omega\mu d} \frac{b_1 b_q + c_1 c_q}{4\Delta}. \tag{14}$$

Consider the $b_1 b_q$ and $c_1 c_q$ terms for $q = 1, 2, 3$

$$\begin{aligned} b_1^2 &= (y_2 - y_3)^2 \\ b_1 b_2 &= (y_2 - y_3)(y_3 - y_1) \\ b_1 b_3 &= (y_2 - y_3)(y_1 - y_2) \\ c_1^2 &= (x_3 - x_2)^2 \\ c_1 c_2 &= (x_3 - x_2)(x_1 - x_3) \\ c_1 c_3 &= (x_3 - x_2)(x_2 - x_1). \end{aligned} \tag{15}$$

Hence, the sum of the first row of the local matrix is

$$b_1^2 + b_1 b_2 + b_1 b_3 + c_1^2 + c_1 c_2 + c_1 c_3 = 0. \tag{16}$$

Notice that the sums of the other rows and the columns of $\overline{\overline{K}}$ are also zero, which can be interpreted as follows: the inductive circuit components are connected between the triangle vertices, whereas no components are connected to the system ground. Unlike $\overline{\overline{K}}$, however, the sums of the rows and the columns of $\overline{\overline{M}}$ are not zero, which indicates that the capacitive components are connected not only to the system ground but also between the triangle vertices. The equivalent circuit model of matrix $Y(K + M)$ *for a group of triangular elements* is shown in Fig. 1.

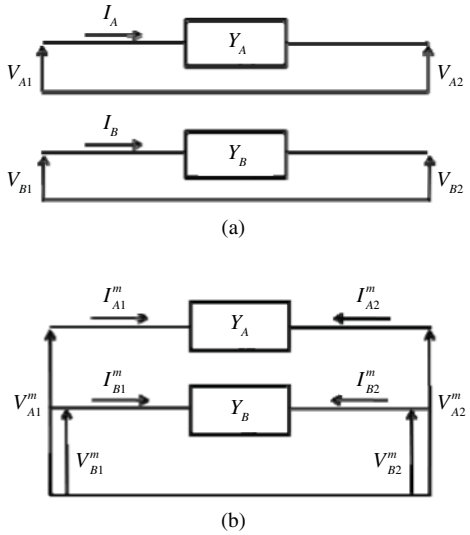


Fig. 2. (a) Two individual networks reference their own ground nodes. (b) Two individual networks reference common ground nodes.

The resulting matrix equation of the single plane pair PDN (6) has the form $Ax = b$, which can be solved by standard linear equation solvers.

C. Multiple Plane Pairs

By virtue of the capability of the equivalent circuit representation, the 2-D finite element method can be applied to multiple plane pairs. As described in Subsection B, each plane pair in the multiple plane pairs can be represented by a unique equivalent circuit model. In a multilayered structure, however, the reference nodes of each equivalent circuit are not in the same layer. Thus, the individual equivalent circuits of each plane pair that references its own ground node cannot be stacked on top of each other without modifying reference nodes. As a result, the reference nodes must be shifted to one common ground to complete the formulation for multiple plane pairs.

Consider two-port networks referencing different ground nodes as shown in Fig. 2. The network has two sub-networks referencing their own ground nodes in which each sub-network can be considered a single plane pair from the multiple plane pairs without the reference node modification. The four-port admittance matrix of this model is

$$\begin{aligned} Y_{A11} V_{A1} + Y_{A12} V_{A2} &= I_A \\ Y_{B11} V_{B1} + Y_{B12} V_{B2} &= I_B. \end{aligned} \tag{17}$$

The electric potential and current relationships between the networks in Fig. 2(a) and (b) are

$$\begin{aligned} I^m_{B1} &= I_B - I_A, & I^m_{A1} &= I_A \\ V_{A1} &= V^m_{A1} - V^m_{B1}, & V_{A2} &= V^m_{A2} - V^m_{B2} \\ V_{B1} &= V^m_{B1}, & V_{B2} &= V^m_{B2}. \end{aligned} \tag{18}$$

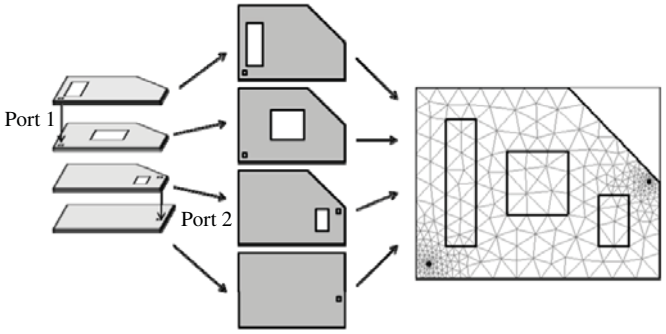


Fig. 3. Diagram of a four-layer structure containing slots on each layer. Sub-domains on each layer are gathered onto one.

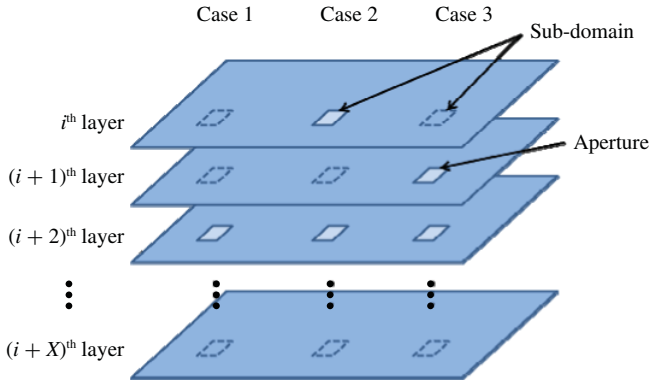


Fig. 4. Three possible situations of the positioning of overlapped sub-domains for apertures.

Hence, rows for the current I_{A1} and I_{B1} of the common ground node network are obtained as follows:

$$\begin{aligned} Y_{A11}(V_{A1}^m - V_{B1}^m) + Y_{A12}(V_{A2}^m - V_{B2}^m) &= I_{A1}^m \\ Y_{B11}(V_{B1}^m) + Y_{B12}(V_{B2}^m) &= I_{A1}^m + I_{B1}^m. \end{aligned} \tag{19}$$

Similarly, by gaining rows for currents I_{A2} and I_{B2}, the system matrix can be completed as follows:

$$\begin{bmatrix} \overline{\overline{Y}}_A & -\overline{\overline{Y}}_A \\ -\overline{\overline{Y}}_A & \overline{\overline{Y}}_A + \overline{\overline{Y}}_B \end{bmatrix} \begin{bmatrix} V_{A1}^m \\ V_{A2}^m \\ V_{B1}^m \\ V_{B2}^m \end{bmatrix} = \begin{bmatrix} I_{A1}^m \\ I_{A2}^m \\ I_{B1}^m \\ I_{B2}^m \end{bmatrix}. \tag{20}$$

The above matrix, which is for a case of two plane pairs with solid planes on each layer, can be extended to a general case. For example, the system matrix for the N plane pairs case can be written as

$$\overline{\overline{Y}} = \begin{bmatrix} \overline{\overline{Y}}_1 & -\overline{\overline{Y}}_1 & & & & \\ -\overline{\overline{Y}}_1 & \overline{\overline{Y}}_1 + \overline{\overline{Y}}_2 & -\overline{\overline{Y}}_2 & & & \\ & -\overline{\overline{Y}}_2 & \overline{\overline{Y}}_2 + \overline{\overline{Y}}_3 & -\overline{\overline{Y}}_3 & & \\ & & \ddots & \ddots & \ddots & \\ & & & -\overline{\overline{Y}}_{N-2} & \overline{\overline{Y}}_{N-2} + \overline{\overline{Y}}_{N+1} & -\overline{\overline{Y}}_{N-1} \\ & & & & -\overline{\overline{Y}}_{N-1} & \overline{\overline{Y}}_{N-1} + \overline{\overline{Y}}_N \end{bmatrix} \tag{21}$$

where $\overline{\overline{Y}}_i, i = 1, 2, \ldots, N$ are the admittance matrices of the ith plane pair counting from the top of the stack.

D. Meshing

A nonuniform triangular mesh is used here to account for irregular geometries and fine apertures. Before the method for solving planes with apertures can be explained, the mesh scheme used for multilayered structures needs to be clearly understood. Since the idea behind MFEM is to approximate the lateral dimensions, no variation of the field is allowed in the vertical direction within a plane pair. Moreover, the equivalent circuits of each single plane pair are connected vertically with appropriate movement of the reference. Thus, the locations of the nodes on a layer must correspond to those of the nodes on the other layers. In order to realize this property, the geometric features on all layers are collected onto one. Then a triangular mesh is created on the layers according to the all the sub-domain outlines. This procedure is best explained by an example of a four-layer structure with apertures on each layer, as shown in Fig. 3. Since the features on each layer are collected onto one layer, the resulting layer contains all the outlines of the features (plane boundaries, holes and gaps) from all the layers. Finally, the layer, which contains the geometric features from all the layers, is discretized by triangular unit cells as shown on the right of Fig. 3.

E. Planes with Apertures

Once the sub-domains are collected onto one layer, they are categorized. The categorized sub-domains for apertures remove the contribution from the system matrix, $\overline{\overline{Y}}_i$, by eliminating the L and C elements corresponding to the mesh elements in that sub-domain. However, the positional interrelations of the sub-domains require different approaches. Consider the following cases in which a sub-domain is on layer i, and as before, layer numbering starts from the topmost layer, as shown in Fig. 4.

1) A sub-domain does not correspond to the aperture on layers i and $i+1$: The contributions of the sub-domain are not removed from $\overline{\overline{Y}}_i$ (case 1).
2) A sub-domain corresponds to the aperture on layer i: The contribution of the sub-domain is removed from $\overline{\overline{Y}}_i$ (case 2).
3) A sub-domain corresponds to the aperture on layer i, or $i, i+1, \ldots, i+X$ all together: The contributions of the sub-domain are removed from $\overline{\overline{Y}}_i$. The sub-domain admittance matrix for the plane pair formed by the ith and $(i+X)^{\text{th}}$ layers is created and added to $\overline{\overline{Y}}_i$ (case 3).

F. Incorporation of the Decoupling Capacitor Model into MFEM

The addition of the decoupling capacitor model between plane layers in MFEM can be explained using the equivalent circuit. As described in the previous subsection, the MFEM formulation can be converted into the equivalent circuit model with inductance and capacitance lumped elements. Inclusion

of decoupling capacitors in the equivalent circuit entails simply vertically connecting an equivalent-circuit element of the capacitor to the corresponding nodes. The equivalent circuit model of the decoupling capacitor is a series connection of capacitance, equivalent series inductance (ESL), and equivalent series resistance (ESR).

Although the concept of adding a circuit element to another circuit is simple, one must incorporate a circuit model into the system matrix carefully. First, the regions that enclose the area in which decoupling capacitors will be connected have to be defined as sub-domains for decoupling capacitors. The size of the sub-domain can be determined by the physical area required by a decoupling capacitor connection. Once a triangular mesh is created, the generated unit triangle inside the sub-domain is chosen for the decoupling capacitor connection.

In order to comprehend the way to represent the inclusion of vertical circuit elements to the MFEM system matrix, one must first understand how vertical capacitive components of a plane pair are represented in the system matrix. The admittance of a capacitive component between two metal planes is

$$Y = \frac{j\omega\varepsilon\Delta}{d} \tag{22}$$

where Δ is the area of the each plane. As shown in (12), the value of the vertical component is decomposed into two different values for matrix representation: 1/6 and 1/12 of the original value. The reason for decomposition into the particular fractions stems from the nature of simplex coordinates (11). Similarly, if a vertical circuit element is to be added to the system, its admittance must first be decomposed into two different values: 1/6 and 1/12 of the original value. Each value is then added to the appropriate locations in the system matrix. For instance, the admittance of a decoupling capacitor can be represented as

$$Y_{\text{decap}} = \frac{1}{\left(\frac{1}{j\omega C_{\text{decap}}} + j\omega ESL + ESR\right)} \tag{23}$$

where C_{decap} is capacitance, ESL is equivalent series inductance, and ESR is equivalent series resistance of the decoupling capacitor. Next, the admittance is decomposed into 1/6 and 1/12 of the original value

$$m_{p,q}^{\text{decap}} = \begin{Bmatrix} \frac{1}{6}Y_{\text{decap}}, & p = q \\ \frac{1}{12}Y_{\text{decap}}, & p \neq q \end{Bmatrix} \tag{24}$$

where p and q are the vertices of a selected unit triangle of a mesh. The 1/6 of the admittance is then added to the diagonal locations, and the 1/12 to the off-diagonal locations of the system matrix. This procedure can be extended to any layer connectivity of the decoupling capacitor by applying the same technique used for multilayer extension. That is, the indefinite admittance matrix of a decoupling capacitor (24) is added to the corresponding nodes in the connecting layers. To account for the coupling caused by the vertical interconnect or a via used for decoupling capacitor connection, the coupling mechanism is assumed to be the plane bounce caused by the return path discontinuity (RPD) of the via. The RPD of the via generates a wrap around current at the via antipad. Thus, by creating an aperture on the plane where the decoupling capacitor is connected, the RPD, or the coupling caused by the via, can be taken into account.

III. Decoupling Capacitor Placement Using a GA

A. GA Optimizer

Manually selecting and placing decoupling capacitors on the PDN to meet the target impedance require a considerable amount of time and effort. To avoid the tedious work, optimization techniques that automatically select and place decoupling capacitors on the PDN can be used. An optimizer using the GA is one of the techniques, which is robust and effective in solving complex, combinational, and related problems [13].

GA is modeled on the concepts of natural selection and evolution, it exploits the ideas from evolutionary biology such as population, crossover, selection, and mutation. Thus, in the case of decoupling capacitor optimization, the data of the decoupling capacitor locations and their types (e.g., capacitance, ESL, ESR) are analogous to genes on a chromosome. Each chromosome contains the following information: capacitor indices, x- and y-locations, and layer connectivity. In addition, cost and physical size of the capacitor can be contained optionally. These values are initially generated randomly at the beginning of the optimization, and the number of the chromosomes (population) is determined by the maximum population number (N_p), which will be input to the optimizer input.

Once the population is initially generated, the core engine is run to produce impedance profiles including the decoupling capacitor data acquired from each of the chromosomes. Once the impedance profiles are obtained, each result is subjected to a quality test. The quality is evaluated using a fitness function that quantifies the optimality of a solution to the target. It is critical that the fitness function be closely related to the solution and be computed quickly. In this paper, the fitness function is defined as

$$fitness = \sum_{i=1}^{Nport} \left(\sum_{k=1}^{Nfreq} \left(\begin{array}{l} (Z_{tar,i} - Z_{i,i}(k)) \sum (Z_{tar,i} > Z_{i,i}(k)) - \\ (Z_{i,i}(k) - Z_{tar,i}) \sum (Z_{tar,i} > Z_{i,i}(k)) \end{array} \right) \right) \tag{25}$$

where $Z_{tar,i}$ represents target impedance at ith port, and $Z_{i,i}(k)$ is self-impedance of ith port at frequency k. If optional parameters such as the cost for each capacitor are added, each parameter is multiplied by appropriate weight coefficients and added to the above fitness function. The results of the fitness function are arranged in descending order of their values. Hence, each chromosome is ranked according to its fitness, completing the simulation for one generation. At this stage, if all the target impedance criteria are met at all the frequency points, the optimization process will be terminated. On the other hand, if the goal is not met by any of the chromosomes, the optimization process will proceed to the next step, breeding, which consists of crossover and mutation steps. Child chromosomes, created by obtaining some portion

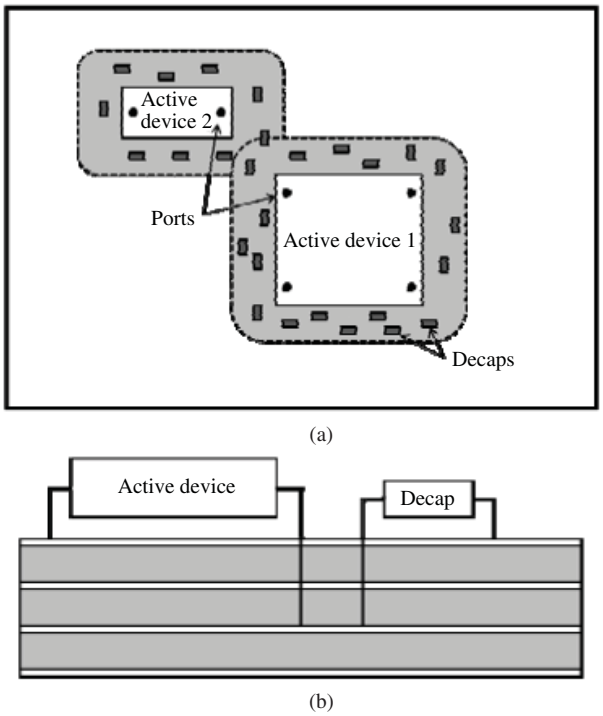


Fig. 5. Scenarios of decoupling capacitor placement. (a) Capacitors are allowed to be located within the shaded region. (b) Connectivity of the capacitors follows that of the nearest active device to minimize the spreading inductance.

of parental genes, mutate themselves. The breeding procedure follows the work in [15].

After the breeding process is ended, the new child chromosomes and their parents are subject to evaluation by the fitness function. Again, if the target impedance requirement is met, the optimization iteration will be terminated, otherwise, another generation will be created and evaluated.

B. GA Customized for Decoupling Capacitor Placement

For more efficient optimization, especially for decoupling capacitor placement, a special strategy can be imposed on the locations of the capacitors. The closer the capacitors are to the noise port, the lower the impedance viewed from the port. Moreover, the decoupling capacitor closely placed to the noise port produces reduced spreading inductance between the port and itself [23], and this strategy, which can maximize the effectiveness of decoupling, can be applied to the initialization step of the GA optimizer when the optimizer places capacitors only at the specified locations close to the ports. In addition, the layer connectivity of the decoupling capacitors follows that of the nearby ports. These scenarios are described in Fig. 5. When a regional limit on decoupling capacitor placement is applied, the area of the region has to be carefully determined. Since a certain amount of physical space is required for the placement of capacitors, even if they are in the forms of a surface mounted device or an embedded passive, the area in the model cannot be unrealistically small. On the other hand, if the area is defined as electrically too large, the strategy for applying the regional limit becomes no longer effective. Therefore, choosing the general vicinity of the active device and maintaining a minimal region is essential.

The overall flow of customized GA for decoupling capacitor choice and placement is depicted in Fig. 6.

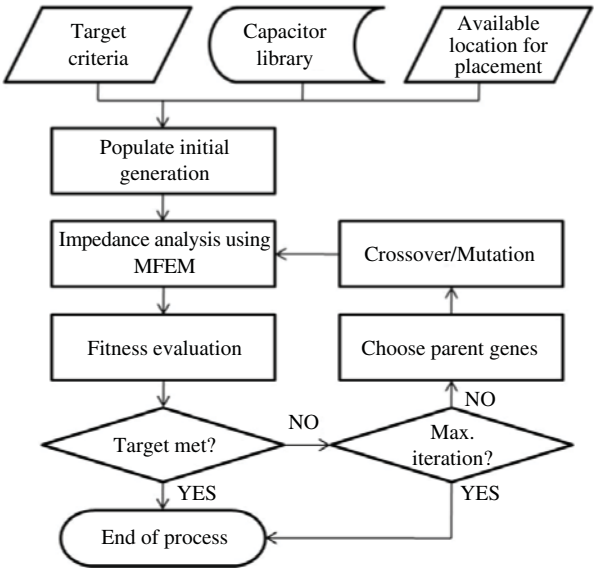


Fig. 6. Process flow of the decoupling capacitor optimization using the proposed GA optimizer.

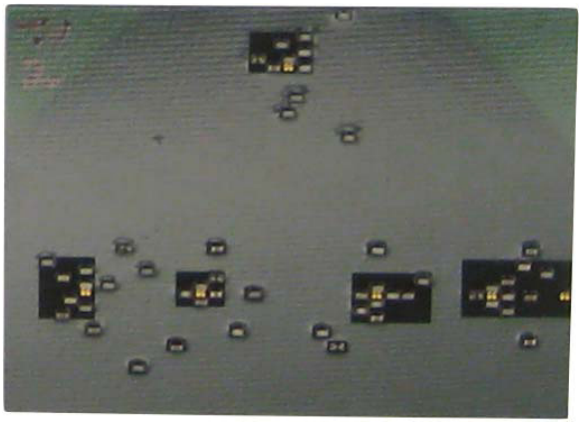


Fig. 7. (a) Test vehicle. (b) Top view of the test vehicle with dimensions. Ports 1 to 5 are the noise ports requiring the self-impedance below the target impedance.

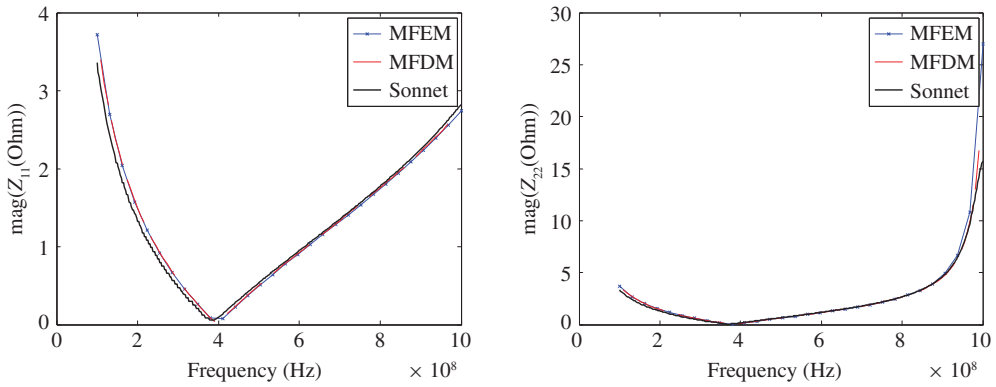


Fig. 8. Self-impedance responses looking into ports 1 and 2 before decoupling capacitors were placed.

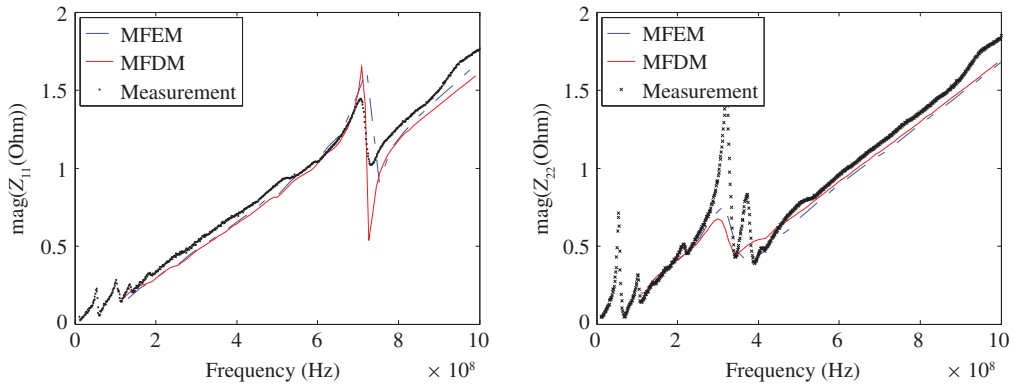


Fig. 9. Self-impedance responses at ports 1 and 2 after the decoupling capacitors were placed.

IV. Test Cases and Results

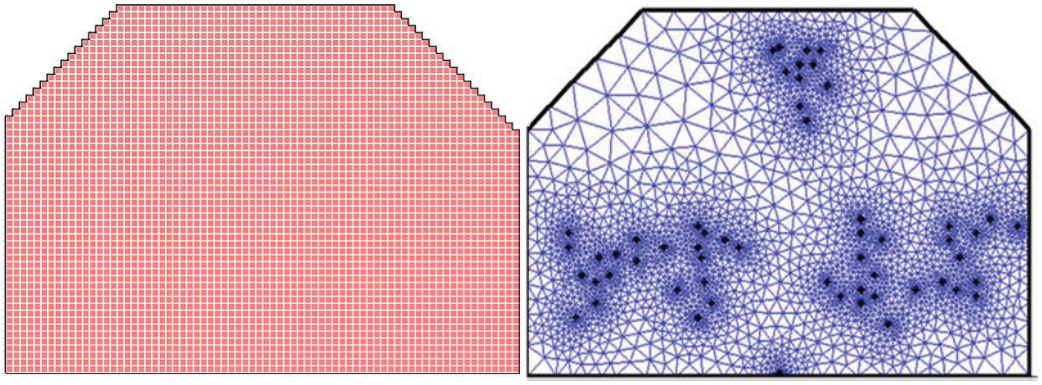
A. Addition of Decoupling Capacitors to MFEM

In the first test case we verified the accuracy of MFEM and the addition of decoupling capacitors with a test vehicle that has two metal plane layers with five ports. The dielectric material is FR-4, with a permittivity of 4.5, a loss tangent of 0.025, and a thickness of 355 μm. The actual test vehicle and the top view of the structure with its dimensions are shown in Fig. 7.

Before examining at the results with decoupling capacitors, we performed software simulations for the bare structure. Fig. 8 shows the self-impedance results at ports 1 and 2. We used MFDM [16], and Sonnet software [24] as references, and the results from the three simulations show good correlations.

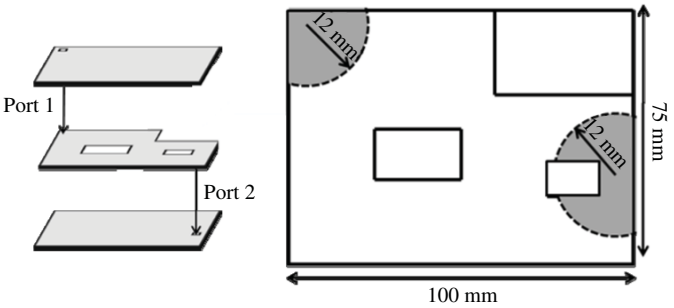
Next, we placed the decoupling capacitors on the bare planes to reduce the self-impedances at the ports, and set the target impedance at 1.5 Ohm at all the ports over the frequency range of 100 MHz to 1 GHz. The GA optimizer randomly selected 55 capacitors from a given library that had 20 different capacitors with their ESL and ESR values, and placed them on the defined regions on the planes. The capacitance values ranged from 680 nF to 33 pF, and ESL and ESR ranged from 0.1 nH to 0.82 nH and from 0.04 Ohm to 3 Ohm, respectively. The inductance of the vias used for decoupling capacitor connection was 0.3 nH, which was calculated by a 3-D inductance extraction tool [25]. Hence, the effective series resonance frequencies of the used capacitors were calculated to be from 20 MHz to 1 GHz.

The measured self-impedance curves at ports 1 and 2 are depicted in Fig. 9 along with results from MFDM and MFEM simulations. Fig. 10 shows the generated meshes for MFDM and MFEM for the test vehicle with decoupling capacitors. To capture small dimensions of the decoupling capacitors, MFDM had to create many square unit-cells all over the plane, while MFEM effectively discretized the multiscale structures using nonuniform triangles. As a result, MFEM resulted in far less number of unknowns (around 3300) than MFDM (around 8000). The resonance and antiresonance frequencies match, and the level of impedances are in good correlation over the frequency range of interest. Some deviation in measurements, especially the antiresonance peaks at port 2, resulted from the relatively large probe inductance compared to the PDN impedance. Thus, the transfer impedance can provide a much more accurate result than the self-impedance, especially for a PDN with moderate impedance [12]. However, in this paper only one-port measurements are conducted due to limited probe accessibility. The impedance exceeded the target impedance (at 1.5 Ohm) at higher frequencies because some decoupling capacitors located close to the ports were removed for measurement probe access. Since the corresponding capacitors were also removed from the MFEM model, the model and the hardware are based on the same structure. Therefore, the provided measurement and simulation results show the



(a) (b)

Fig. 10. Comparison of mesh generations of (a) MFDM. (b) MFEM for the test vehicle with decoupling capacitors.



(a) (b)

Fig. 11. (a) Test case 1. (b) Top view of the layer on which entire sub-domains are integrated. When the regional limit is applied, decoupling capacitors are placed within the shaded region.

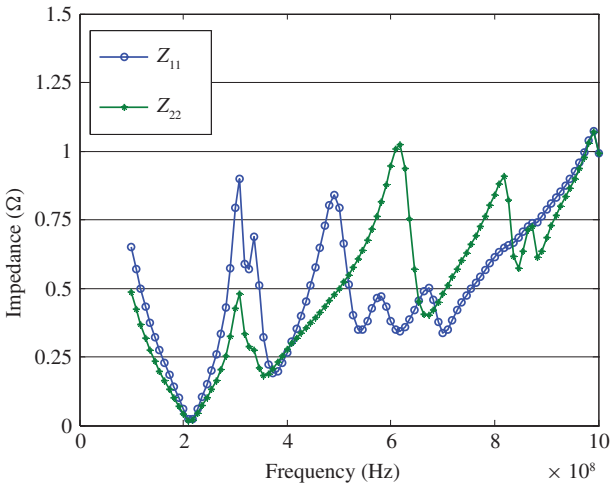


Fig. 12. Self-impedances at ports 1 and 2 of the test case 1 optimized by the customized GA.

accuracy of the incorporation model of decoupling capacitors into MFEM.

B. GA Adapted to Decoupling Capacitor Placement

1) Test Case 1: Multilayer Structure with Slots: An example of a multilayer structure was designed to apply the GA optimizer adapted to decoupling capacitor placement. As shown in Fig. 11(a), the structure consists of three layers with slots on the second layer, two ports between the first plane pair and the second plane pair. The metal planes are 100 mm long, 75 mm wide, and 30 μm thick, and the dielectric is 200 μm with a relative permittivity of 4.5, and loss tangent of 0.02.

We ran the first optimization using the GA, then ran the customized GA optimizer applying the additional regional limit on decoupling capacitor. In the customized optimizer, we set the regional limit at a radial distance of 12.5 mm from nearby ports as shown in Fig. 11(b). In addition, we assigned the connectivity of the capacitors to follow the connectivity of nearby ports to minimize the loop inductance.

We assigned both optimizers to achieve the target impedance of 1 Ohm and designed them to run until either the target was met or the maximum number of iterations was reached. The number of decoupling capacitors, whose self-resonance frequencies exist between 100 MHz and 1 GHz, was 10. We assigned ESL and ESR equally to all the capacitors with values of 0.4 nH and 0.2 mOhm, respectively. For a fair comparison, we applied the equal optimization options, such as the number of populations, rates of crossover and mutation, and the fitness function to both optimizers.

The customized GA accomplished the goal in 12 iterations, and the resulting impedance results are shown in Fig. 12. However, the GA without a regional limit failed to obtain the target impedance within the maximum number of iterations, set at 150. The progress of the fitness evaluations from both optimizations is shown in Fig. 13, in which the progress of the customized GA shows quick achievement of the optimization target. Notice that although the ordinary GA optimizer went through many iteration steps to reach the same level of fitness as that of the customized GA, its progress shows continuous increments. Furthermore, as the optimization proceeds the decoupling capacitors are being more and more closely placed to the ports, and the pattern of the placement at the later step corresponds to that of the customized GA, as shown in Fig. 14. Therefore, we can conclude that a large amount of optimization time can be saved by implementing the regional limit technique to the placement of decoupling capacitors. The

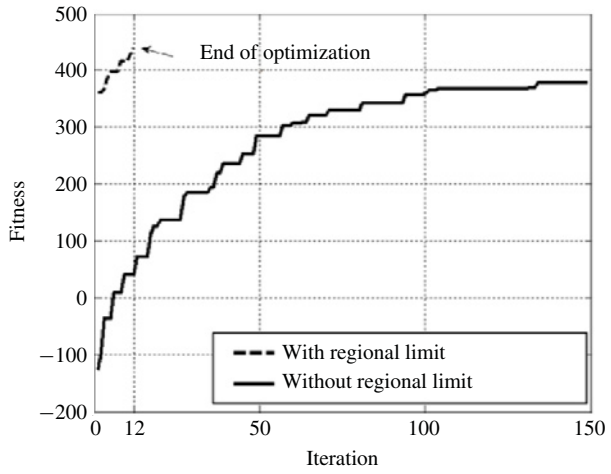


Fig. 13. Fitness progress of the ordinary and customized GA optimizers in test case 1.

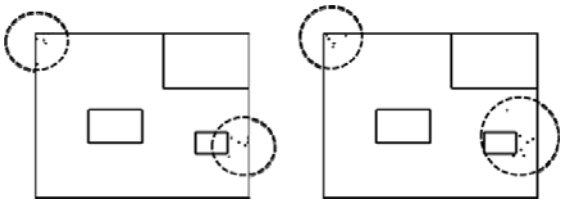


Fig. 14. Final placement of decoupling capacitors of the customized optimizer (left), and the ordinary optimizer in the later optimization steps of (right).

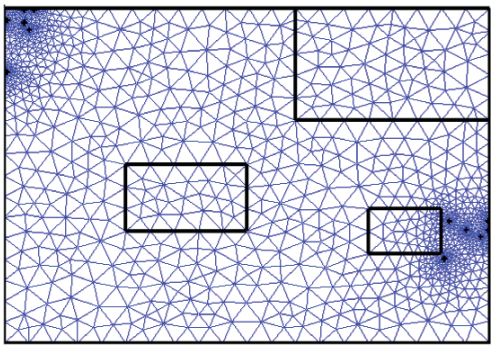


Fig. 15. Mesh generations of MFEM with the final placement of decoupling capacitors.

generated mesh for the final decoupling capacitors placement is shown in Fig. 15.

2) Test Case 2: We applied the customized GA to the bare board of the test vehicle presented in the previous section. As before, we set the target self-impedance at 1.5 Ohm for each port, used the same capacitor library, and determined a via inductance of 0.3 nH [25]. We set the regional limit for capacitor placements at a 10 mm radial distance from nearby ports.

The optimizer achieved the optimization goal with only three iterations, and the resulting impedance response is shown in Fig. 16. Since randomness could have accounted for the quick results, we performed several additional simulations with the same settings. However, we found that the optimizer was able to reach the target at most within five iterations.

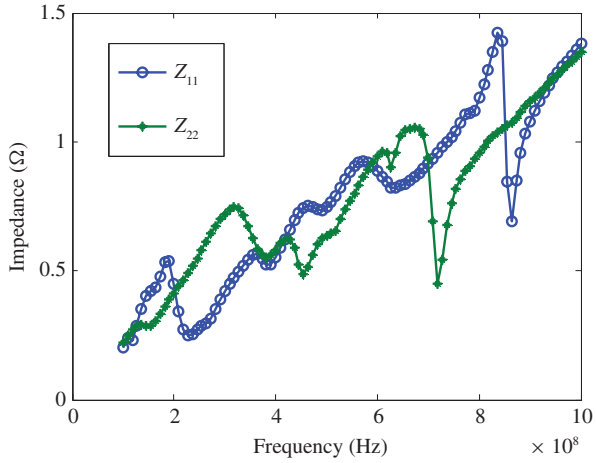


Fig. 16. Self-impedance responses at ports 1 and 2 resulted from the customized GA optimization.

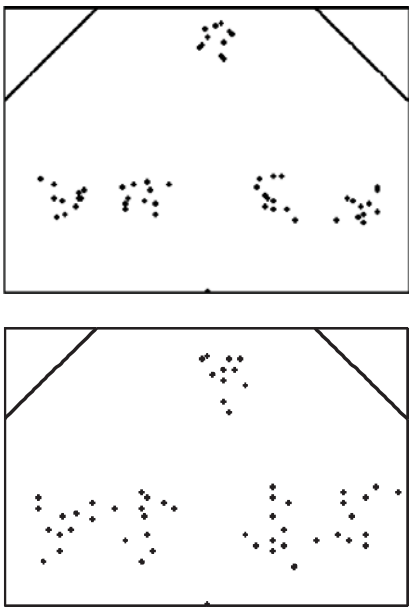


Fig. 17. Decoupling capacitor placement results obtained by the customized GA (top) and the ordinary GA (bottom).

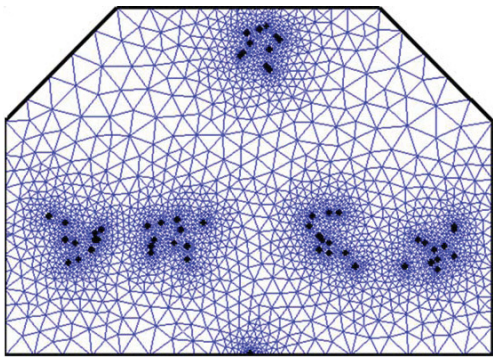


Fig. 18. Mesh generations of MFEM with the optimized placement of decoupling capacitors.

For comparison, the GA optimizer without the regional limit was run under the same conditions. The average number of iterations taken for the GA optimizer to reach the target

exceeded 100, which took more than 6 hours. However, the average optimization time of the customized GA was 10 minutes. The final locations of the decoupling capacitors from both optimizations are shown in Fig. 17. In addition, the placement patterns of the ordinary GA optimizer and the customized GA optimizer were similar after convergence. The generated mesh with the optimized decoupling capacitor placement is shown in Fig. 18.

V. Conclusion

In this paper, we presented the optimization technique of selection and placement of decoupling capacitors using MFEM and the GA. MFEM solves for plane structures by creating an equivalent mesh on all the layers and applying a multilayer technique. Incorporation of the equivalent circuit model of a decoupling capacitor into that of MFEM requires modifications of values of the lumped elements. We improved the ordinary GA by using a technique that limits the locations for decoupling capacitors in the initial optimization step. This technique derives from widely known methods that suggest placing decoupling capacitors as close to the active devices as possible to reduce the loop inductance. Use of this technique significantly reduces computational effort devoted to achieving the target impedance of a PDN.

The effectiveness of our optimization technique can be increased by applying other decoupling techniques to the optimizer. Furthermore, improving the fitness function of the GA may enhance the quality of the optimization.

Acknowledgment

The authors would like to thank Sony Corporation, Tokyo, Japan, for providing the test vehicle.

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