

Electrical-Thermal Co-Simulation of 3D Integrated Systems With Micro-Fluidic Cooling and Joule Heating Effects

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Abstract—In this paper, the electrical-thermal co-simulation of 3D systems with Joule heating, fluidic cooling and air convection effects is proposed. The finite-volume method formulations of voltage distribution equation, heat equations for both fluid flow and solid medium with nonuniform mesh are explained in detail. Based on the proposed iterative co-simulation method, package temperature distribution and voltage drop with Joule heating and fluidic cooling effects can be estimated. Several packaging examples are simulated and the results show that with micro-channel fluidic cooling in high power density 3D integrated packages, the thermal effect on voltage drop is reduced by 10% which is much less than that of using a traditional heat sink.

Index Terms—Finite volume method, fluidic cooling, Joule heating, power delivery network (PDN), thermal effect, through silicon via (TSV), voltage drop.

I. INTRODUCTION

DUE to the continuing growth of integration density using 3D stacking enabled by through silicon via (TSV) technology, the power density of integrated circuit (IC) chips is expected to increase beyond 100 W/cm² in 2016 according to the International Technology Roadmap for Semiconductors (ITRS) [1]. Meanwhile, in order to reduce the power consumption and increase functionality, the power supply voltage of IC chips has been reduced to 1.2 V and below with the scaling of IC fabrication technology [2]. Due to the high power density and low supply voltage of IC chips, large amounts of current need to be supplied through the power delivery network (PDN). The Joule heating (or self-heating) effect is becoming increasingly significant [3], [4] for temperature rise and reliability issues of interconnects.

For power delivery networks, due to the low noise margin and threshold voltage, the dc voltage drop analysis at the package level and board level is becoming as important as chip level IR drop analysis. Due to the temperature-dependent electrical resistivity, the thermal effect causing Joule heating is becoming an important contributor to voltage drop in the power delivery network (PDN). In addition, in order to mitigate the thermal

challenge in 3D integration, emerging new technologies such as micro-channel fluidic cooling is gaining more traction [5]–[8]. Therefore, in order to obtain accurate temperature profile in the 3D package, efficient thermal modeling including Joule heating, air convection and fluidic cooling effects is becoming a critical task.

In the past, dc IR drop analysis based on equivalent circuit approaches [9], [10] has been used. However, the thermal effect on voltage drop has not been considered. In order to capture the thermal effects on dc IR drop in 3D systems, the electrical-thermal co-simulation method has been proposed recently [11], [12]. This was extended to include Joule heating and air convection effects [13]. The computational fluid dynamic (CFD) based thermal modeling of micro-fluidic cooling in 3D stacked IC chips has been studied in [7] and [8]. However, the Joule heating effect from the PDN has not been considered in [7], [8].

In this paper, electrical-thermal co-simulation of power delivery networks with Joule heating, air convection, and fluidic cooling effects is presented. In order to perform electrical-thermal iterations efficiently, voltage distribution equation, heat equations for both solid medium and fluid flow are all formulated and solved using the finite volume method with nonuniform rectangular grid. In the thermal simulation, the modeling of heat conduction, air convection and fluidic cooling are all included to obtain the temperature distribution. In electrical dc voltage drop simulation, by updating the temperature-dependent electrical resistivity of the PDN, voltage distribution is obtained with thermal effects. By establishing convergence between the electrical and thermal equations, the final temperature distribution and dc voltage drop are obtained.

The organization of this paper is as follows. In Section II, the iterative electrical-thermal co-simulation method is presented. The finite-volume formulations for dc voltage drop simulation, thermal simulation with convection and fluidic cooling boundary conditions are explained in detail in Section III. In Section IV, several examples are discussed with Joule heating, convection and fluidic cooling effects. Finally, the conclusion is summarized in Section V.

II. ELECTRICAL-THERMAL CO-SIMULATION METHOD

In steady state, the governing equation for voltage distribution can be expressed as

$$\nabla \cdot \left(\frac{1}{\rho(x, y, z, T)} \nabla \phi(x, y, z) \right) = 0 \quad (1)$$

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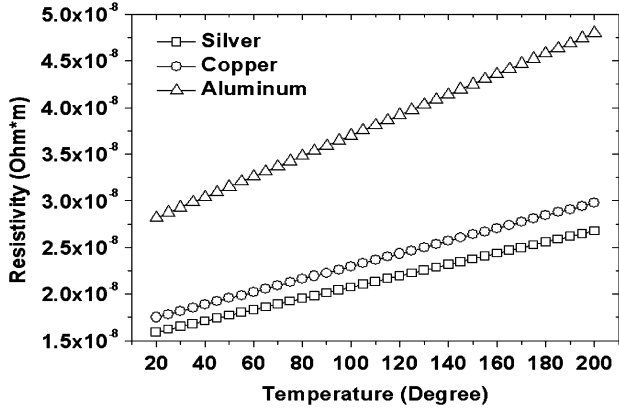


Fig. 1. Temperature-dependent resistivity of silver, copper, and aluminum.

where $\rho(x, y, z, T)$ and $\phi(x, y, z)$ represent the temperature-dependent electrical resistivity and voltage distribution.

For steady-state thermal analysis, the governing heat equations for solid medium and fluid flow can be expressed as

$$\nabla \cdot [k(x, y, z) \nabla T(x, y, z)] = -P(x, y, z) \quad (2a)$$

$$\sigma c_p \bar{v}(x, y, z) \cdot \nabla T(x, y, z) = \nabla \cdot (k_f \nabla T(x, y, z)) \quad (2b)$$

where $k(x, y, z)$ and $T(x, y, z)$ represent the thermal conductivity of solid medium and temperature distribution, respectively; σ , c_p and $\bar{v}(x, y, z)$ represent the density, heat capacity and velocity distribution of the fluid, respectively; k_f is the thermal conductivity of the fluid [14], [15].

In (2a), $P(x, y, z)$ is the total heat source excitation including the heat source from chip and Joule heating converted from the Ohmic loss due to current flowing through conductors in the PDN. The Joule heating can be expressed as

$$P_{\text{Joule}}(x, y, z) = \bar{J} \cdot \bar{E}(x, y, z) \quad (3)$$

where, \bar{J} is the current density and $\bar{E}(x, y, z)$ is the electrical field distribution in the PDN.

Since the electrical resistivity is temperature-dependent, it is described by

$$\rho = \rho_0 [1 + \alpha(T - T_0)] \quad (4)$$

where ρ_0 is the electrical resistivity at T_0 which is 20 °C, and α is the temperature coefficient of the electrical resistance. As shown in Fig. 1, with increasing temperature, the electrical resistivity of the conductors increases and eventually can affect the IR drop in the PDN.

Due to the temperature-dependent electrical resistivity $\rho(x, y, z, T)$ and Joule heating generated in the conductors, the electrical and thermal characteristics couple to each other and form a nonlinear system of equations, as shown in Fig. 2.

To obtain accurate voltage distribution with convection and Joule heating effects, it is required to solve the nonlinear electrical-thermal equations (1)–(4), simultaneously. An iterative electrical-thermal co-simulation method has been developed and used in this paper, as shown in Fig. 3. This is an extension of the method developed in [11]. The iterative simulation technique consists of the following important procedures.

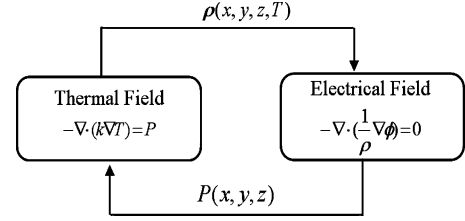


Fig. 2. Relationship between electrical and thermal fields.

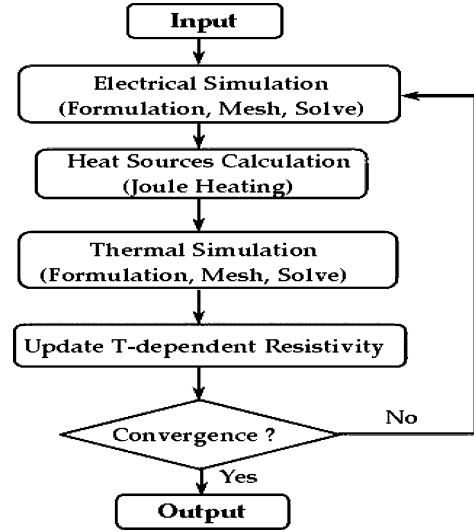


Fig. 3. Iterative electrical-thermal co-simulation procedure.

- 1) Setting input information on package layout parameters, initial material properties, excitations, and boundary conditions for steady state electrical and thermal analysis.
- 2) Steady state electrical voltage distribution simulation for voltage, current, and power distribution profiles in the PDN.
- 3) Heat sources (Joule heat) calculation from the power distribution profile.
- 4) Using the updated Joule heat excitation for steady state thermal simulation with thermal conduction, air convection and fluidic cooling.
- 5) Based on the temperature distribution profile obtained, the electrical resistivity of conductors in the PDN is updated and thereby thermal effect on voltage drop is included.
- 6) Determining the convergence of temperature and voltage distributions. The final thermal and voltage distributions are displayed if convergence is reached. Else, the iterations are continued.

III. FINITE VOLUME FORMULATION

For establishing an iterative co-simulation procedure, voltage distribution equation (1) with temperature-dependent resistivity as well as thermal equations (2a) and (2b) with Joule heating effects need to be solved. In order to update the temperature, Joule heat and dc drop distributions efficiently, the same mesh needs to be used for both electrical and thermal simulations. Since 3D systems have large size planes and small size structures such as TSVs, C4s, apertures, etc., a 3D nonuniform mesh is required

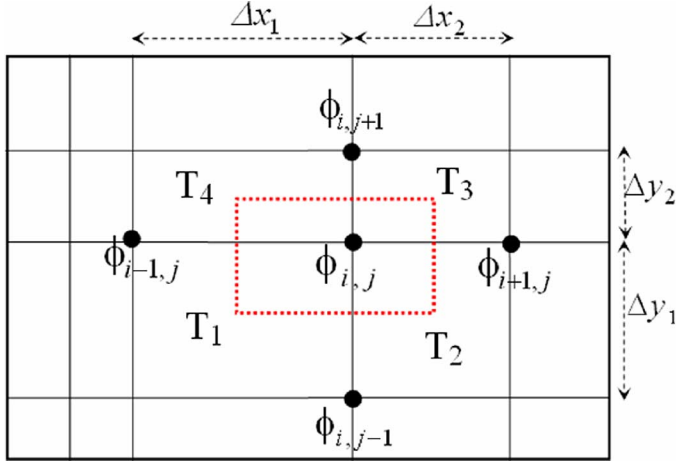


Fig. 4. 2D rectangular grid for computing voltage distribution.

to reduce the number of unknowns, reduce the simulation time and also to capture all geometries accurately. In this paper, a nonuniform rectangular grid has been used.

The formulations for solving the electrical and thermal equations are discussed in this section. Though 3D nonuniform rectangular grid is used in this paper, the finite volume formulation is explained on a 2D nonuniform grid for simplicity.

A. Voltage Distribution Equation

The formulation for solving the voltage distribution equation (1) is performed using temperature-dependent resistivity. In Fig. 4, $\phi_{i,j}$ represents the voltage at grid point (i, j) which is surrounded by four nodes. In Fig. 4, $\Delta x_1, \Delta x_2, \Delta y_1,$ and Δy_2 are the nodal distances between node (i, j) and its adjacent nodes in x and y directions, respectively. It is assumed that the four surrounding cells of node (i, j) have different temperatures $T_1, T_2, T_3,$ and T_4 , which can be obtained from the thermal simulation.

In order to apply the finite volume method, node (i, j) is surrounded by a finite volume cell (dashed line) in Fig. 4. The intersection points between the dashed cell and other four cells are the center points of each cell. By integrating (1) over the dashed cell and applying the divergence theorem, we obtain

$$\int_{\text{dashed line}} \frac{1}{\rho(x, y, z, T)} \nabla \phi(x, y, z) \cdot \hat{n} dl = 0 \quad (5)$$

where \hat{n} is the outward pointing unit normal vector at the boundary of the dashed cell.

Initially, the temperature distribution is assumed uniform and thus the electrical resistivity $\rho(x, y, z, T)$ is a constant. By applying the finite difference approximation to the first order derivative of ϕ in (5), the finite volume scheme at node (i, j) can be obtained as

$$\frac{\phi_{i,j} - \phi_{i-1,j}}{\frac{\rho \Delta x_1}{d}} + \frac{\phi_{i,j} - \phi_{i+1,j}}{\frac{\rho \Delta x_2}{d}} + \frac{\phi_{i,j} - \phi_{i,j-1}}{\frac{\rho \Delta y_1}{w}} + \frac{\phi_{i,j} - \phi_{i,j+1}}{\frac{\rho \Delta y_2}{w}} = 0 \quad (6)$$

where $w = (\Delta x_1 + \Delta x_2)/2$ and $d = (\Delta y_1 + \Delta y_2)/2$. Note that the finite volume scheme of (6) is analogous to the Kirchhoff's Current Law (KCL).

In order to include the temperature effect on voltage distribution, the temperature distribution $T_1, T_2, T_3,$ and T_4 in the surrounding cells are considered. Finally, the finite volume scheme with temperature-dependent resistivity can be generalized as

$$\begin{aligned} & \left(\frac{\Delta y_1}{\rho(T_1) \Delta x_1} + \frac{\Delta y_2}{\rho(T_4) \Delta x_1} \right) (\phi_{i,j} - \phi_{i-1,j}) \\ & + \left(\frac{\Delta y_1}{\rho(T_2) \Delta x_2} + \frac{\Delta y_2}{\rho(T_3) \Delta x_2} \right) (\phi_{i,j} - \phi_{i+1,j}) \\ & + \left(\frac{\Delta x_1}{\rho(T_1) \Delta y_1} + \frac{\Delta x_2}{\rho(T_2) \Delta y_1} \right) (\phi_{i,j} - \phi_{i,j-1}) \\ & + \left(\frac{\Delta x_1}{\rho(T_4) \Delta y_2} + \frac{\Delta x_2}{\rho(T_3) \Delta y_2} \right) (\phi_{i,j} - \phi_{i,j+1}) = 0 \quad (7) \end{aligned}$$

B. Heat Equation for Solid Medium With Convection Boundary Condition

In the thermal simulation, the thermal conductivity " k " is considered to be constant. For the heat equation (2a) with only conduction, since it has the same form as (1), the same finite volume formulation can be applied resulting in

$$\frac{T_{i,j} - T_{i-1,j}}{\frac{\Delta x_1}{kd}} + \frac{T_{i,j} - T_{i+1,j}}{\frac{\Delta x_2}{kd}} + \frac{T_{i,j} - T_{i,j-1}}{\frac{\Delta y_1}{kw}} + \frac{T_{i,j} - T_{i,j+1}}{\frac{\Delta y_2}{kw}} = P_{\text{total}} \quad (8)$$

where, $P_{\text{total}} = \int \int_{\text{dashed cell}} -P(x, y, z) dS$ is the total heat source in the dashed cell.

In order to obtain accurate temperature distribution in the thermal simulation of realistic systems, the convection boundary condition

$$k \frac{\partial T}{\partial n} \Big|_{\text{convection}} = -h_c (T - T_a) \quad (9)$$

needs to be considered. In (9), T_a and h_c represent the ambient temperature and convection coefficient, respectively. The same finite volume formulation procedure [16] can also be applied at the convection boundary with nonuniform mesh, as shown in Fig. 5.

In Fig. 5, node (i, j) at the convection boundary is surrounded by a finite volume cell (dashed line). By integrating (2a) over the dashed cell and applying the divergence theorem, we obtain

$$\int_{\text{dashed line}} k(x, y, z) \nabla T(x, y, z) \cdot \hat{n} dl = \int \int_{\text{dashed cell}} -P(x, y, z) dS \quad (10)$$

By applying the finite difference approximation to the first order derivative of $T(x, y, z)$ in (10) and incorporating (9),

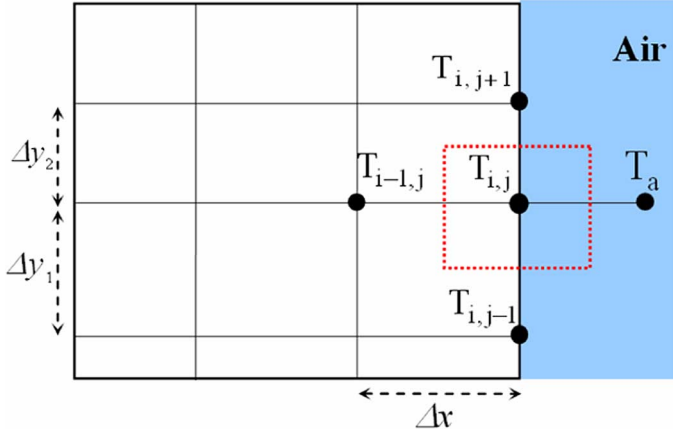


Fig. 5. Convection boundary with nonuniform mesh.

the finite volume scheme for heat equation with convection boundary condition at node (i, j) can be expressed as

$$\frac{T_{i,j} - T_a}{\frac{1}{hcd}} + \frac{T_{i,j} - T_{i-1,j}}{\frac{\Delta x}{kd}} + \frac{T_{i,j} - T_{i,j-1}}{\frac{\Delta y_1}{k\Delta x/2}} + \frac{T_{i,j} - T_{i,j+1}}{\frac{\Delta y_2}{k\Delta x/2}} = P_{\text{total}} \quad (11)$$

where $d = (\Delta y_1 + \Delta y_2)/2$.

C. Heat Equation for Fluid Flow

In fluidic cooling, since the micro-channel cross-sectional dimension is much smaller than its length, the flow velocity along the longitudinal direction is much larger than in the lateral direction. It can therefore be assumed that the water only flows in the longitudinal direction and flow velocity therefore is constant. The average flow velocity “ v ” along y direction has been used for simulating the fluid flow in this paper. As a result, (2b) can be written as

$$\sigma c_p v \frac{\partial T(x, y, z)}{\partial y} = \nabla \cdot (k_f \nabla T(x, y, z)). \quad (12)$$

By integrating (12) over the dashed cell in Fig. 6 and applying the divergence theorem, (12) becomes

$$\int_{S1+S2} \sigma c_p v T \hat{y} \cdot \hat{n} dl = \int_{\text{dashed line}} k_f \nabla T \cdot \hat{n} dl \quad (13)$$

where $S1$ and $S2$ are the upper and bottom boundaries of the dashed cell, as shown in Fig. 6.

For the right hand side of (13), the same formulation can be used. For the left hand side, since the central finite difference scheme can generate instability in certain cases [16], the backward difference approximation is used. The finite volume scheme for solving the heat equation for fluid flow can be expressed as

$$\frac{T_{i,j} - T_{i-1,j}}{\frac{\Delta x_1}{kd}} + \frac{T_{i,j} - T_{i+1,j}}{\frac{\Delta x_2}{kd}} + \frac{T_{i,j} - T_{i,j-1}}{\frac{\Delta y_1}{kw}}$$

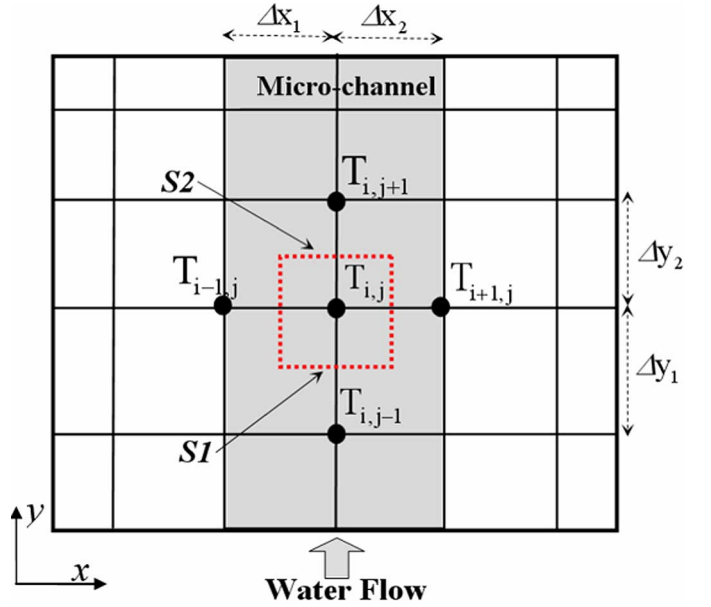


Fig. 6. Nonuniform mesh for simulating micro-channel in IC chip.

$$+ \frac{T_{i,j} - T_{i,j+1}}{\frac{\Delta y_2}{kw}} = \sigma c_p v (T_{i,j} - T_{i,j-1}) \quad (14)$$

where $w = (\Delta x_1 + \Delta x_2)/2$, $d = (\Delta y_1 + \Delta y_2)/2$.

Since the average flow velocity along the longitudinal direction is used in the model, the heat transfer coefficient h needs to be applied at the boundary of the micro-channel to model the heat transfer between the solid medium and the fluid flow. The effect of this boundary condition is important, since eliminating it can cause incorrect chip temperatures [19]. For water flow in micro-channels of IC chip, the Reynolds number is usually less than 2300 and the flow is laminar [20]. For fully developed laminar flow inside rectangular micro-channels with constant heat flux, the Nusselt number can be expressed as [21]

$$Nu = 8.235 \left(1 - \frac{2.0421}{\alpha} + \frac{3.0853}{\alpha^2} - \frac{2.4765}{\alpha^3} + \frac{1.0578}{\alpha^4} - \frac{0.1861}{\alpha^5} \right) \quad (15)$$

where α is the aspect ratio of the rectangular micro-channel.

The average heat transfer coefficient h can be obtained analytically from the Nusselt number and expressed as

$$h = Nu \cdot k / D_h \quad (16)$$

where D_h is the hydraulic diameter of the micro-channel [20]. The same formulation for air convection boundary in Section III-B can be used to model the water convection boundary between the solid medium and water flow.

Based on the above finite volume formulations for voltage distribution equation, heat equations for solid medium and fluid flow with nonuniform rectangular grid, a new steady-state electrical-thermal co-simulation solver “PowerET” has been developed. This solver has been used to simulate voltage distribution

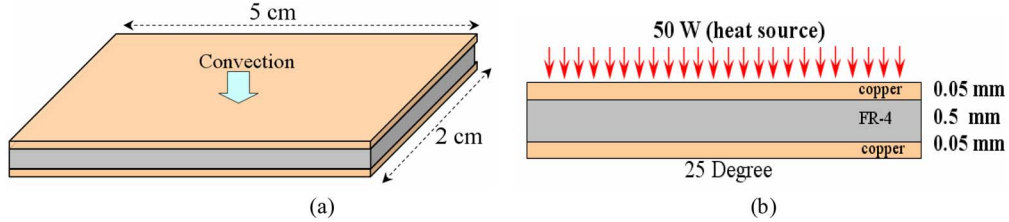


Fig. 7. (a) Two-layer PCB board and (b) heat source configuration.

and thermal distribution with Joule heating, air convection, and fluid cooling effects in this paper.

IV. RESULTS

A. Model Verification Examples

To verify the correctness and accuracy of the model for heat conduction, air convection and Joule heating as described in Section III, two plane examples have been simulated. In addition, two micro-fluidic cooling examples have been simulated to validate the finite volume model for micro-fluidic cooling in thermal simulation.

1) *Plane Example With Heat Conduction and Convection:* A two-layer PCB board with size of 5 cm \times 2 cm is shown in Fig. 7. The thicknesses of copper plane and FR-4 are 50 μ m and 500 μ m, respectively. As shown in Fig. 7(b), a 50 W heat source is placed on the top plane while the bottom surface of the PCB board is set to be 25 $^{\circ}$ C. The thermal conductivities of FR-4 and copper are 0.5 and 400 W/(mK), respectively. The air convection boundary condition is applied to the top surface of the PCB board.

Since the PCB board is rectangular, the temperature of the top plane can be obtained using the analytical equation

$$T = T_a + P \cdot R_{\text{total}} \quad (17)$$

where, T_a is the ambient temperature of 25 $^{\circ}$ C and R_{total} is the total thermal resistance due to heat conduction and air convection.

This PCB board has been simulated using *PowerET* solver with different convection coefficients. The comparisons between the simulated temperature and the results calculated using the analytical equation (17) are depicted in Fig. 8, showing the accuracy of the solution.

2) *Plane Example With Joule Heating Effect:* Another two-layer PCB board with size of 10 cm \times 5 cm is shown in Fig. 9. A voltage source is placed at one end of the top power plane. The current flows from the voltage source to the other end of the board. The thickness of copper plane and dielectric are 36 and 350 μ m, respectively. Air convection is applied to both the top and bottom surfaces of the PCB board. The thermal conductivity of the dielectric is 0.8 W/(mK) in this example. Due to the rectangular shape of the power plane, the voltage drop across the plane can be calculated by using the analytical equation

$$\Delta V = IR = I \frac{\rho L}{S} \quad (18)$$

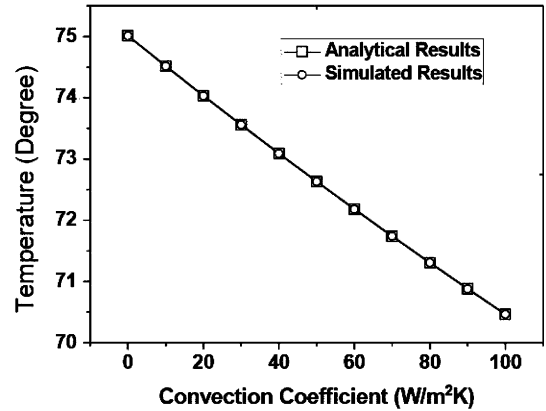


Fig. 8. Temperature of top plane with different convection coefficients.

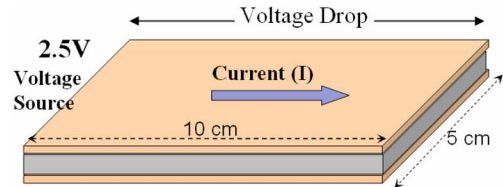


Fig. 9. PCB with rectangular power plane.

where L is the length and S is the cross-sectional area of the power plane, respectively.

Due to Joule heating $P = I \cdot \Delta V$ generated from Ohmic loss, the board temperature can increase. The board temperature can also be obtained using (17).

Without Joule heating effect, analytical equations (17) and (18) can be used to calculate the temperature and voltage drop for the power plane directly. With Joule heating effect, the iterative classic Newton's method [17] can be used to obtain the nonlinear voltage drop and temperature. The rectangular plane has been simulated with and without Joule heating effect using the *PowerET* solver. The comparisons of the simulated voltage drop and temperature against the results from classic Newton's method and analytical equations are depicted in Fig. 10. As can be seen from Fig. 10, without Joule heating effect, the temperature of the power plane is kept at constant room temperature of 25 $^{\circ}$ C [Fig. 10(b)]. Therefore, the voltage drop increases linearly with increasing current, as shown in Fig. 10(a). However, with Joule heating effect under the condition of air convection with heat transfer coefficient of 5 W/(m²K), we observe that the temperature increases nonlinearly with increasing current [Fig. 10(b)]. As a result, the voltage drop also increases nonlinearly with increasing current [Fig. 10(a)]. Moreover, Fig. 10

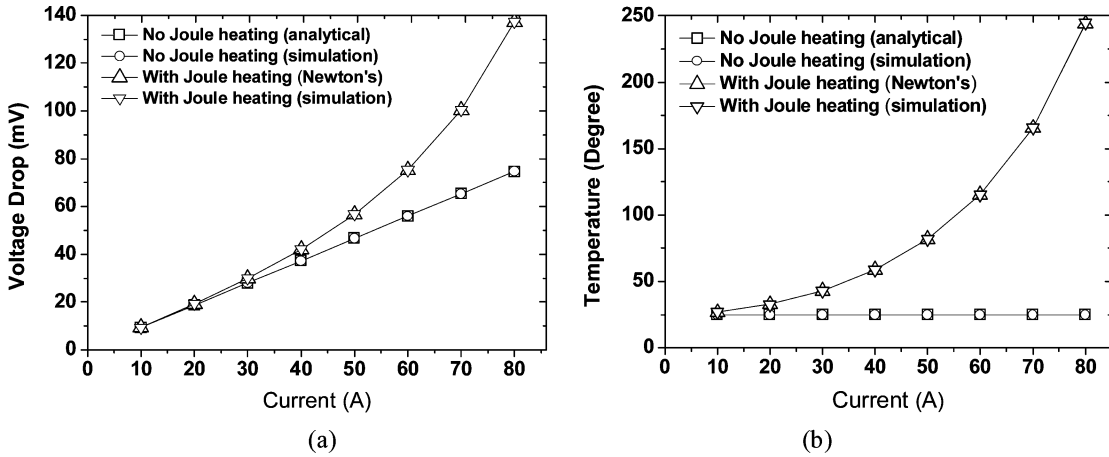


Fig. 10. (a) Voltage drop and (b) temperature of the power plane with and without Joule heating effect.

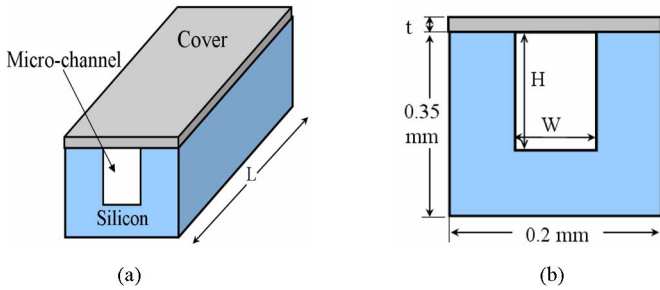


Fig. 11. (a) Micro-channel and (b) its cross-section.

shows that the simulation results match very well with the results from analytical equations (17), (18) and classical Newton’s method, indicating the accuracy of the presented method.

3) *Micro-Fluidic Cooling Example:* To test the accuracy of the model for micro-fluidic cooling, a single micro-channel is first simulated. The micro-channel and its cross-sectional view are shown in Fig. 11. In Fig. 11, the length of the micro-channel is 20 mm and its cross-sectional dimension is $0.12\text{ mm} \times 0.24\text{ mm}$. The bulk silicon thermal conductivity is $150\text{ W/(m}\cdot\text{K)}$ as in [19]. The cover thickness is 0.05 mm and its thermal conductivity is set to be $0.2\text{ W/(m}\cdot\text{K)}$. The heat flux density of $400\,000\text{ W/m}^2$ is applied at the bottom of the silicon substrate. The input water temperature is set to be 20°C . To test the convergence of the micro-fluidic simulation, the cross-section of the micro-channel is meshed with 2×2 , 4×4 , 8×8 , 16×16 , and 32×32 cells (mesh level-1 to mesh level-5), respectively.

With a flow rate of 14.4 mg/s (0.864 ml/min), the simulated average micro-channel outlet temperature and average substrate base temperature with cross-sectional mesh refinement are shown in Fig. 12. It shows that both the micro-channel outlet temperature and base temperature converge with cross-sectional mesh refinement. As can be seen from Fig. 12, using 4×4 meshed cells (mesh level-2) at the cross-section of the micro-channel, the average micro-channel outlet temperature and base temperature are 46.070°C and 41.93°C , respectively. Compared to the final converged outlet temperature and base temperature of 46.074°C and 42.17°C , the errors

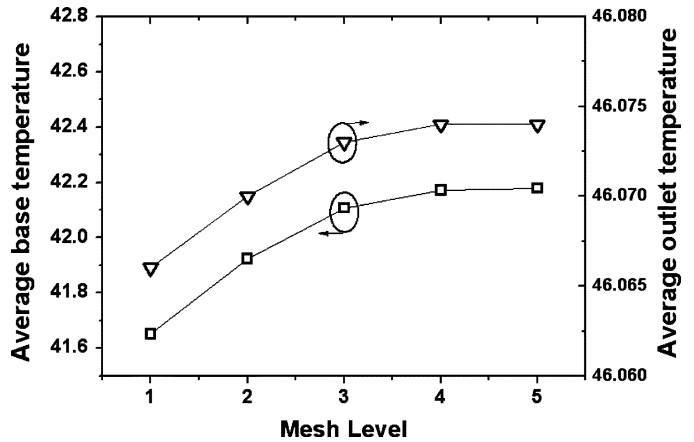


Fig. 12. Average micro-channel outlet and base temperature with mesh refinement showing convergence (unit: Celsius).

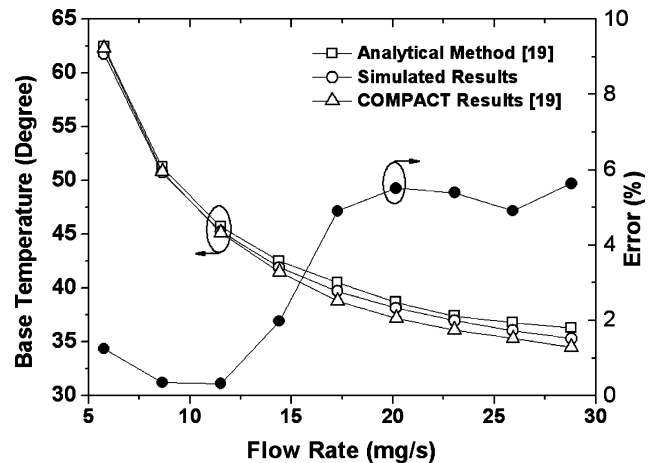


Fig. 13. Average chip base temperatures with different flow rates.

for the average micro-channel outlet temperature and base temperature are both less than 1%. Therefore, using 4×4 meshed cells for the micro-channel cross-section is adequate to obtain accurate results for this example. Using 4×4 meshed cells for the micro-channel cross-section, this example is also simulated with different flow rates ranging from 5.76 mg/s

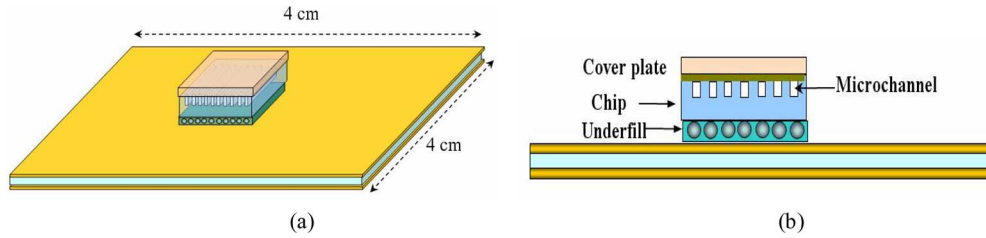


Fig. 14. Package with micro-fluidic cooling, (a) whole system view, (b) cross-sectional view.

TABLE I
MATERIAL THICKNESS AND THERMAL CONDUCTIVITY

	Thickness (mm)	Thermal Conductivity (W/mK)
Substrate	0.35	0.8
Copper	0.036	400
Chip	0.3	110
Underfill	0.2	4.3
C4	0.2	60
Micro-channel	0.2	0.6
Pyrex glass	0.1	1.1
Channel pitch	0.094	

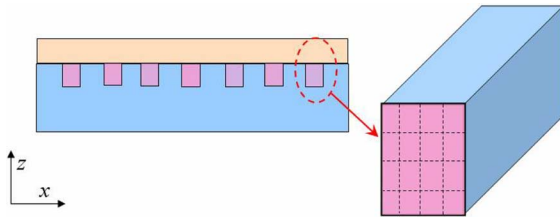


Fig. 15. Cross-sectional mesh of micro-channel.

(0.3456 ml/min), to 28.8 mg/s (1.728 ml/min). The simulated results and comparison with the CFD simulation results using COMPACT and analytical results reported in [19] are shown in Fig. 13. From Fig. 13, it is observed that the simulated results from *PowerET* agree very well with the CFD simulation results using COMPACT and analytical results in [19]. Compared to the simulation results using COMPACT, the error is less than 6%, showing the accuracy of the presented method.

An experimental test vehicle consisting of a silicon chip with fluidic cooling using micro-channels has been described in [6]. In order to verify the model for micro-fluidic cooling against measurement results, the test vehicle in [6] with micro-fluidic cooling has been simulated. The structure is shown in Fig. 14. The chip size is 1 cm \times 1 cm and the power consumption is 45 W. A total number of 51 micro-channels are distributed uniformly on the chip as described in [6]. The cross-sectional dimension of each micro-channel is 0.1 mm \times 0.2 mm. A Pyrex glass cover plate is placed on top of the micro-channels. Natural air convection with convection coefficient of 5 W/(m²K) is applied to both the top and bottom surfaces of the package. The thermal conductivity of silicon chip is set to be 110 W/(m·K). The input water temperature at the inlets of micro-channels is set to be 22 °C and water heat capacity c_p is set to be 4180 J/(Kg·K). The detailed material thickness and thermal conductivity are listed in Table I.

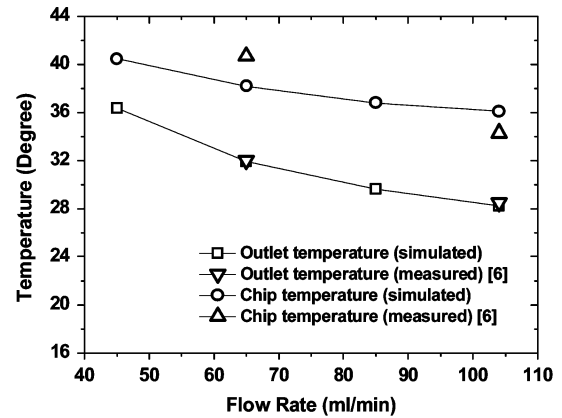


Fig. 16. Average outlet temperature and average chip temperature using simulation and measurements.

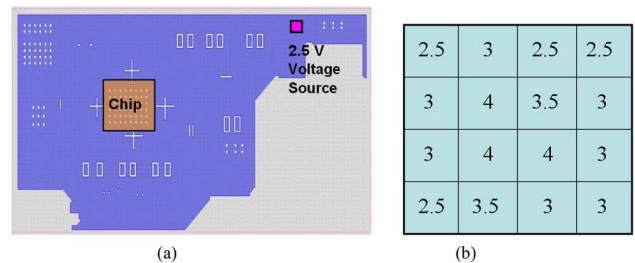


Fig. 17. (a) Cadence board design example, (b) nonuniform chip power map (unit: W).

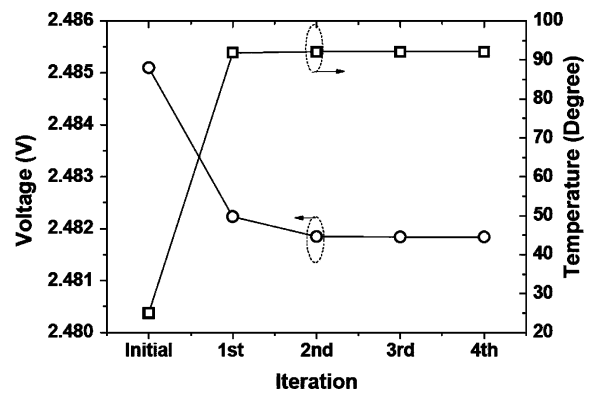


Fig. 18. Chip voltage and temperature with electrical-thermal iterations.

A 3D nonuniform mesh was used to approximate the chip, TSVs, underfill, substrate as well as micro-channels. For each micro-channel, the cross section was also meshed using 4 \times 4 cells, as shown in Fig. 15. This test vehicle has been simulated

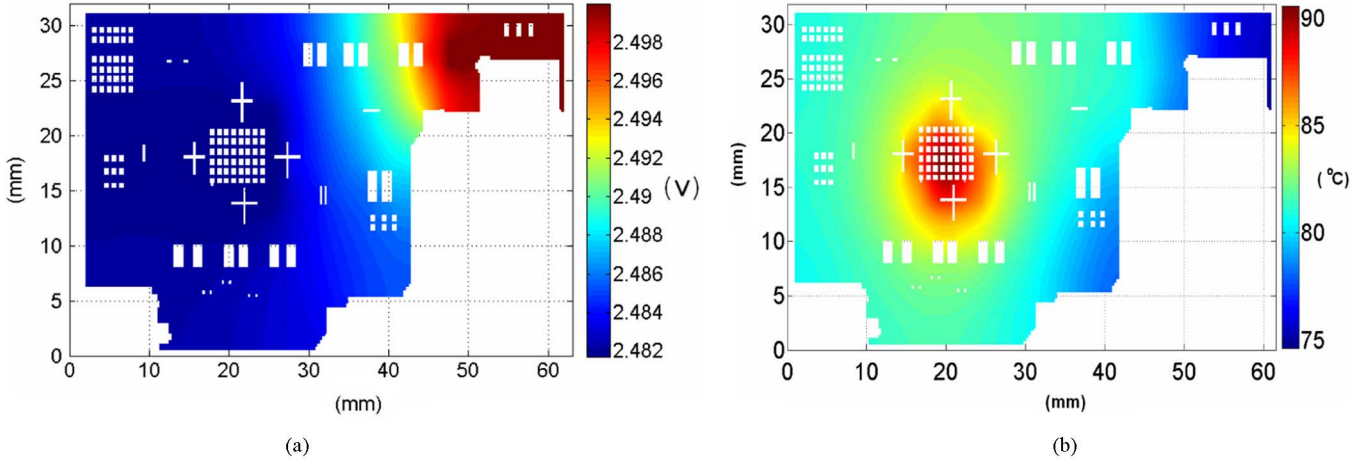


Fig. 19. Final voltage and temperature distributions of the board, (a) voltage, (b) temperature.

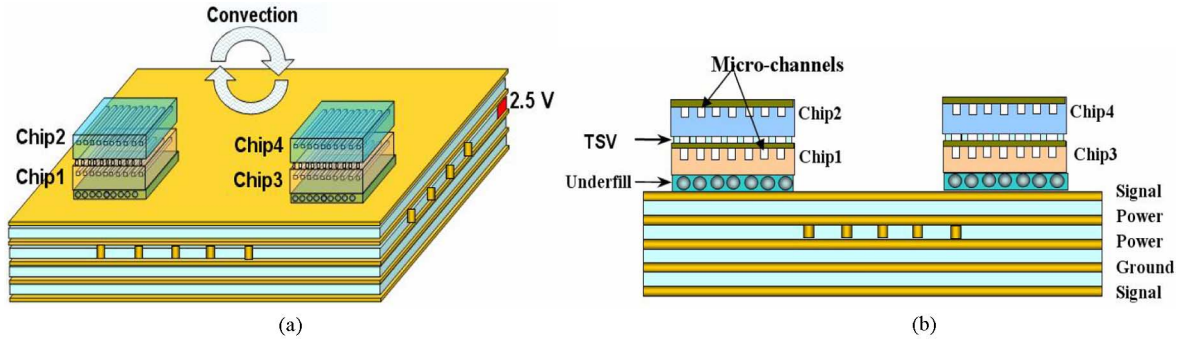


Fig. 20. 3D integrated system with micro-fluidic cooling. (a) Whole system (b) Cross-sectional view.

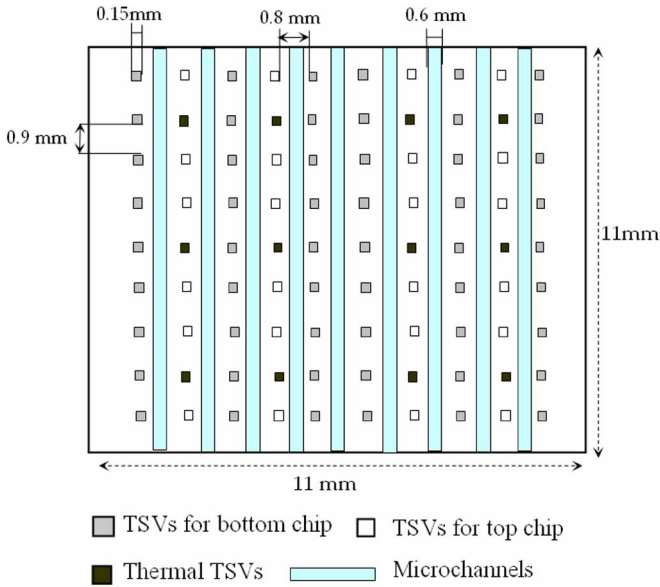


Fig. 21. Micro-channel and TSV configuration for stacked chips.

with different water flow rates using *PowerET* solver. The comparisons of simulated and measured average outlet temperature of the micro-channels and average chip temperature are plotted in Fig. 16. As shown in the figure, with water flow rates of 65 and 104 ml/min, the differences between the simulated av-

TABLE II
MATERIAL THICKNESS AND THERMAL CONDUCTIVITY

	Material Thickness (mm)	Thermal Conductivity (W/mK)
Glass-ceramic	0.35	5
Copper	0.036	400
Chip	0.5	110
Underfill	0.2	4.3
C4	0.2	60
TIM	0.2	2.4
TSV (Tungsten)	0.5	174
Micro-channel	0.2	0.6

erage outlet temperature and measurements [6] are 0.1 °C and 0.28 °C, respectively. The relative error is less than 4.5% for the outlet temperature. For average chip temperature, with water flow rates of 65 and 104 ml/min, the temperature differences between the simulation and measurements are 2.6 °C and 1.7 °C, respectively, as shown in Fig. 16. Their corresponding errors are 13.7% and 13.9%, respectively. The relative larger error for the average chip temperature may due to the average heat transfer coefficient *h* employed in the fluidic cooling model.

B. Practical Design Example

In practical package or board designs, the power delivery network usually has irregular shape with many voids or apertures. In order to simulate practical designs, a new interface,

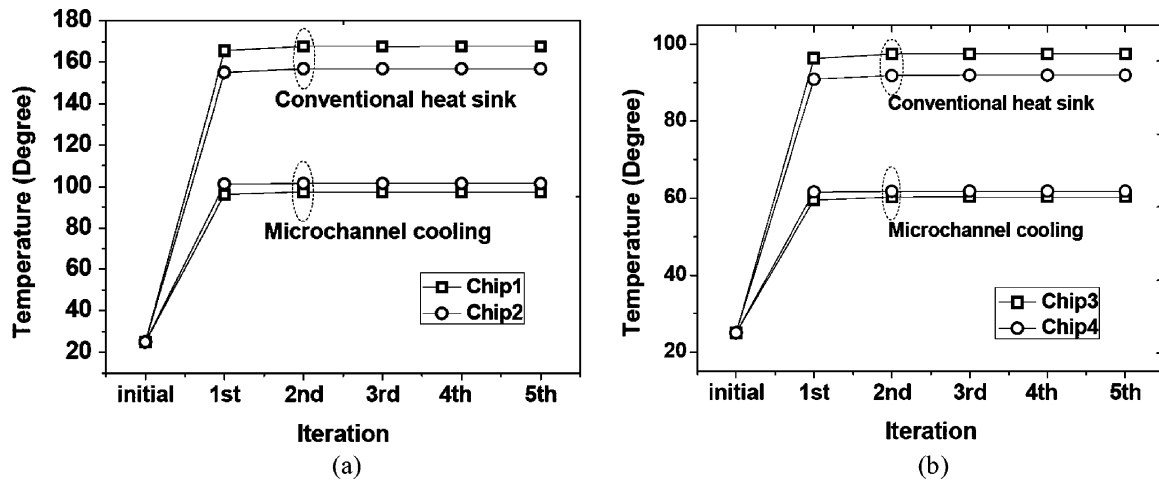


Fig. 22. Temperature of (a) Chip1 and Chip2, (b) Chip3 and Chip4 with electrical-thermal iterations.

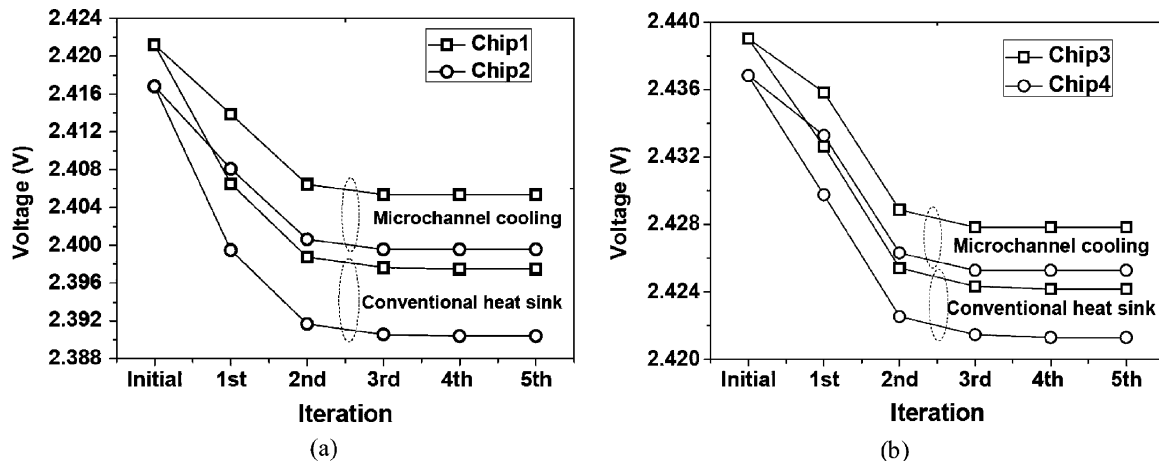


Fig. 23. Voltage of (a) Chip1 and Chip2, (b) Chip3 and Chip4 with electrical-thermal iterations.

which can import board and package design files from *Cadence SPB* software into *PowerET* solver, has been developed. A Cadence board design example is shown in Fig. 17(a). In Fig. 17(a), the board dimension is 60 mm \times 31 mm and the chip is 9 mm \times 9 mm. The chip total power consumption is 50 W and its nonuniform power map is illustrated in Fig. 17(b). The thermal conductivity of thermal interface material (TIM) is 2 W/(mK). The heat sink is modelled as an ideal heat sink with constant room temperature of 25 $^{\circ}$ C. This example has been simulated with convection coefficient of 5 W/(m 2 K) on both sides of the board. The simulated voltage and temperature of the chip with electrical-thermal iterations are shown in Fig. 18. It shows that the final chip temperature is increased to 92.1 $^{\circ}$ C because of the power density from the chip and Joule heating effect from PDN. Compared to an initial voltage drop of 15 mV, the final voltage drop is increased to 18.2 mV. Therefore, the thermal effect on voltage drop is 21.3%. The final temperature and voltage distributions are shown in Fig. 19.

C. 3D Example

1) *3D Package With Micro-Fluidic Cooling*: A 3D integrated system with micro-fluidic cooling is also simulated using *PowerET* solver in this section. The 3D integrated system includes

two sets of stacked chips, 36 micro-channels, hundreds of TSVs, C4s and glass ceramic substrate. The detailed structure of the 3D integrated system is shown in Fig. 20. The package has five metal layers including two signal layers, two power plane layers and one ground plane layer, as shown in Fig. 20(b). The two power plane layers are shorted together with multiple-vias in glass-ceramic substrate in order to reduce the IR drop. A 2.5 V voltage source is placed at the corner of the package. In each set of stacked chips, the top chip is stacked on the bottom chip using TSVs and C4s. The package size is 20 cm \times 20 cm and the size of each chip is 1.1 cm \times 1.1 cm.

In this 3D integrated package, the power consumption for Chip1, Chip2, Chip3, and Chip4 are 100 W, 100 W, 50 W, and 50 W, respectively. The uniform power maps are used for all chips. In order to dissipate heat efficiently for this high power density 3D subsystem, the micro-fluidic cooling method is used, as shown in Fig. 20, with chilled water. In each chip, nine micro-channels with cross-section of 0.6 mm \times 0.2 mm are used. The micro-channel and TSV configuration for the stacked chips is illustrated in Fig. 21. The detailed geometry and material parameters are summarized in Table II.

Air convection with heat transfer coefficient of 5 W/(m 2 K) is applied to both the top and bottom surfaces of the 3D package.

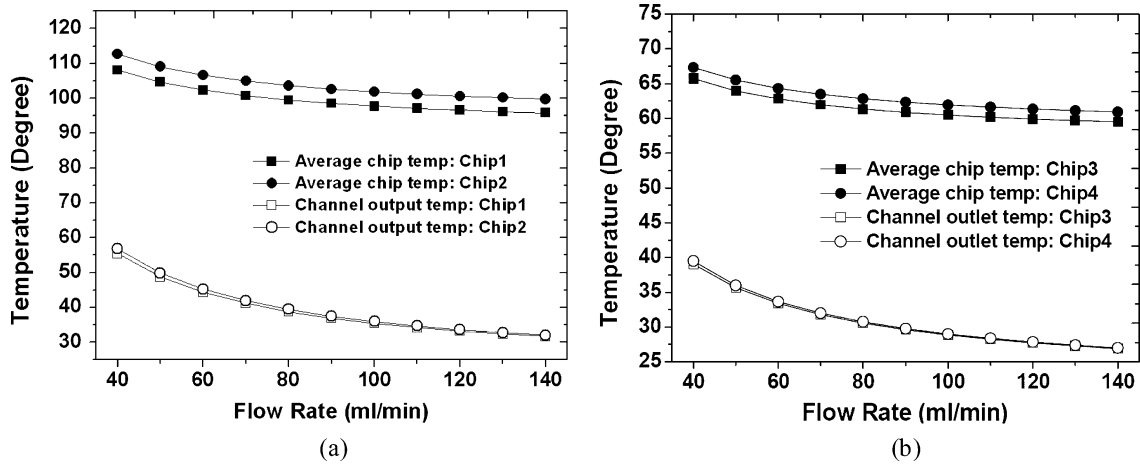


Fig. 24. Velocity effect on chip and micro-channel outlet temperatures, (a) Chip1 and Chip2, (b) Chip3 and Chip4.

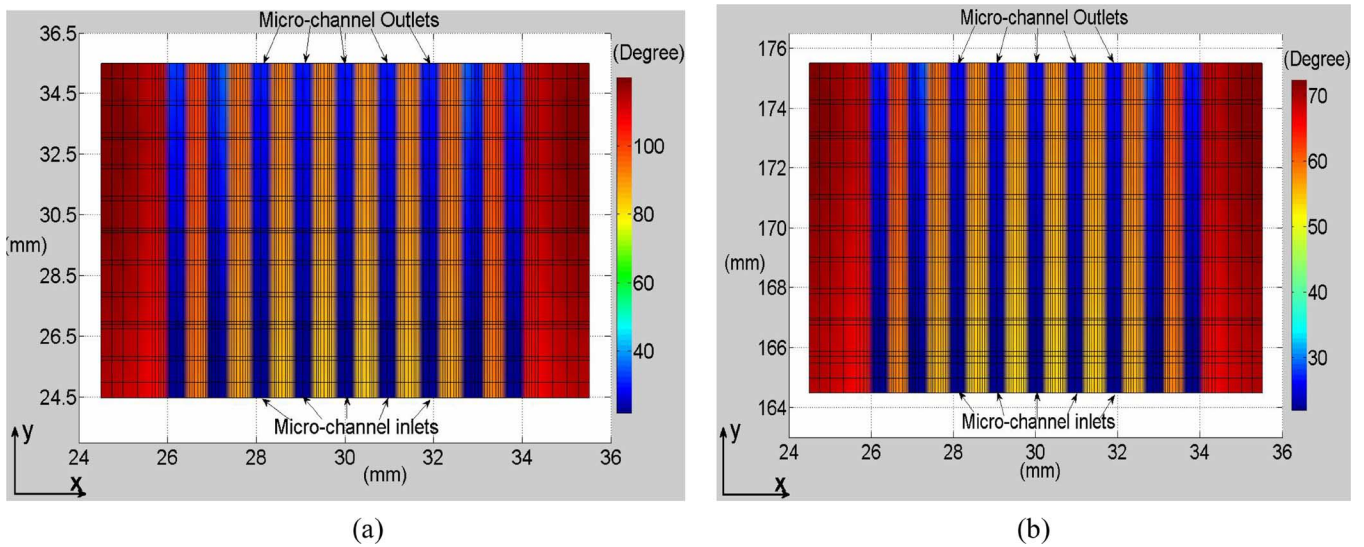


Fig. 25. 2D temperature distributions of micro-channels and chip, (a) Chip1, (b) Chip3 with flow rate of 104 ml/min (top view).

This example is simulated with both Joule heating and fluidic cooling effects. In the simulation, four chips are supplied with same water flow rate. The input water temperature at the inlet of micro-channels is set to 22 °C. In order to see the fluidic cooling effect, the traditional cooling method using heat sink is also simulated for comparison. The TIM thermal conductivity is 2.4 W/(mK) and the heat sink is assumed to be an ideal heat sink with constant room temperature of 25 °C. In the simulation, 3D nonuniform rectangular grid is used with about 166 K unknowns for thermal simulation. For voltage distribution simulation, since only conductor cells are considered as unknowns in the simulation, only 110 K unknowns are used. The simulation took five iterations to converge. The total simulation time was 401.4 s.

With water flow rate of 104 ml/min for each chip, the simulated temperature using micro-fluidic cooling and traditional heat sink is shown in Fig. 22. It shows the simulated results converge in five iterations. As can be seen from Fig. 22, with heat sink, the final temperatures of Chip1, Chip2, Chip3, and Chip4 are 167.6 °C, 156.8 °C, 97.5 °C, and 91.9 °C, respectively. However, using micro-fluidic cooling, their temperatures become 97.5 °C, 101.5 °C, 60.3 °C, and 61.8 °C, respectively.

Therefore, the micro-fluidic cooling technology can greatly reduce the chip temperature for high power density subsystem with 3D stacked ICs.

The simulated voltage using micro-fluidic cooling and traditional heat sink is illustrated in Fig. 23. The initial voltage drops of Chip1, Chip2, Chip3, and Chip4 are 78.8 mV, 83.2 mV, 60.9 mV, and 63.2 mV, respectively. Using traditional heat sink, the final voltage drops of Chip1, Chip2, Chip3, and Chip4 are 102.5 mV, 109.6 mV, 75.8 mV, and 78.7 mV, respectively. Therefore, the thermal effects increase voltage drop of Chip1, Chip2, Chip3, and Chip4 by 30%, 32%, 24%, and 25%, respectively. However, with micro-fluidic cooling, the thermal effects increase voltage drop of Chip1, Chip2, Chip3, and Chip4 by 20%, 20%, 18%, and 18%, respectively. Since the micro-channel fluidic cooling can reduce the chip temperatures to less than 102 °C for Chip1 and Chip2 and less than 62 °C for Chip3 and Chip4, as shown in Fig. 22, the thermal effect on voltage drop of chips is reduced dramatically compared to that of using heat sink.

To investigate the flow velocity effect on the temperature of stacked chips, this example has been simulated with different water flow rates and the results are shown in Fig. 24. It illustrates

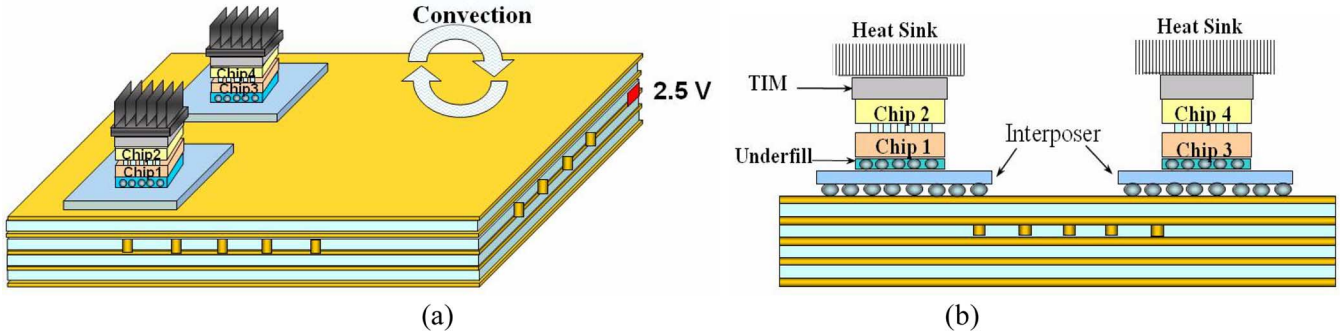


Fig. 26. 3D integrated package with interposers. (a) Whole system. (b) Cross-sectional view.

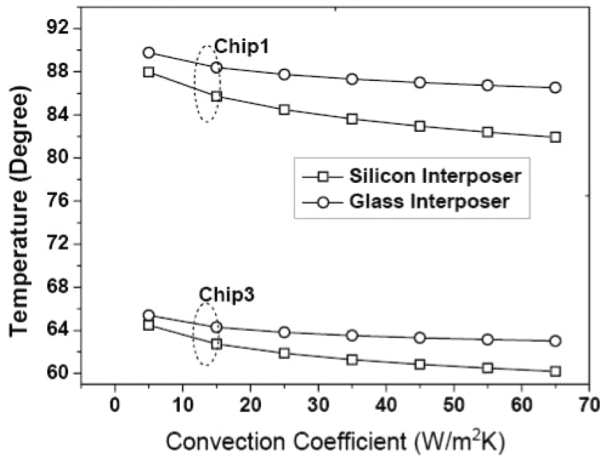


Fig. 27. Chip temperature with different convection coefficients.

that with increasing flow rate, the average temperature of chips and average outlet temperature of micro-channels decrease. For Chip1 and Chip2 with power consumption of 100 W, their maximum temperatures can be reduced to less than 100 °C with flow rate of 130 ml/min. For Chip3 and Chip4 with power consumption of 50 W, their maximum temperatures can be reduced to less than 65 °C with a flow rate of 60 ml/min. In addition, it is observed that with micro-fluidic cooling, the bottom chip has lower temperature than that of the top chip. This is because the bottom chip has shorter distance to the substrate and the thermal resistance from bottom chip to the air is smaller. As a result, air convection can help in dissipating heat from the bottom chip.

After establishing convergence in the electrical-thermal co-analysis, the final temperature distributions of chip and micro-channels are shown in Fig. 25. It shows that the chip temperature is much higher than the water temperature inside the micro-channel. This is due to the relative larger power density of the chip and smaller heat transfer coefficient between the liquid water and silicon chip, which results in large temperature gradient at the boundary.

2) *3D Package With Silicon and Glass Interposers:* In 3D integrated package, silicon interposers are required to spread out the high density I/O signal traces and to match the CTE of silicon ICs. A 3D integrated package with interposers is shown in Fig. 26. The same substrate and TSV configuration are used as in the last example. The power consumption for Chip1, Chip2, Chip3, and Chip4 are 70 W, 10 W, 40 W, and 10 W, respectively.

The uniform power map is used for all the chips. Air convection is applied to the top and bottom surfaces of the package. The 3D package has been simulated with glass and silicon interposers to compare the response, respectively, since glass is being considered as an alternate interposer material [18]. The thermal conductivities of glass and silicon interposers are 1.14 and 148 W/(mK), respectively. The thickness of the interposer is 0.3 mm.

The simulated temperature of Chip1 and Chip3 with glass and silicon interposers is shown in Fig. 27. It shows that with silicon interposer, the temperatures of Chip1 and Chip3 are lower than that of using glass interposer. Moreover, using silicon interposer, the temperatures of Chip1 and Chip3 are decreasing much faster than that of using glass interposer with increasing convection coefficient. With convection coefficient of 35 W/(m²K) the temperature of Chip1 is 83.6 °C using silicon interposer, which is about 3.7 °C lower than that of using glass interposer. This is because the silicon interposer has much higher thermal conductivity than glass interposer, resulting in a smaller thermal resistance from chip to the surrounding air medium. Therefore, more heat can be spread out from chip to air through convection. The cross-sectional temperature distributions of the package using glass and silicon interposers with convection coefficient of 35 W/(m²K) are illustrated in Fig. 28. From Fig. 28, it is observed that with glass interposer, more heat is confined in the package than that of using silicon interposer. For the voltage drop, since the chip temperature difference using glass interposer and silicon interposer is less than 5 °C, as shown in Fig. 27, their final voltage drop difference is less than 1 mV. In this example, 130 K unknowns were used for thermal simulation and 102 K unknowns for voltage distribution simulation. The total simulation time was 126.3 s.

D. CPU Runtime and Memory Usage

The proposed electrical-thermal co-simulation solver, *PowerET*, has been implemented using Matlab and executed on a PC with a 3.2 GHz Xeon(TM) CPU and 3.0 GB memory. The left division solver in Matlab is used in “*PowerET*” simulator to solve the system of equations. The CPU runtime and memory usage with number of cells is illustrated in Fig. 29. As shown in Fig. 29, both the CPU runtime and memory usage of *PowerET* solver are nearly linearly proportional to the number of cells up to 0.6 million. This shows the good scalability of the electrical thermal co-simulation method.

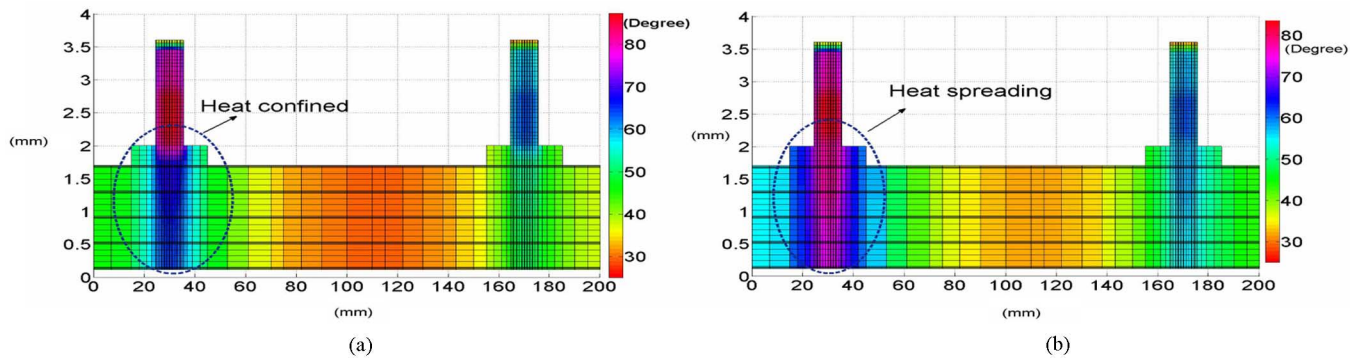


Fig. 28. Cross-sectional temperature distribution of the package with (a) glass and (b) silicon interposers.

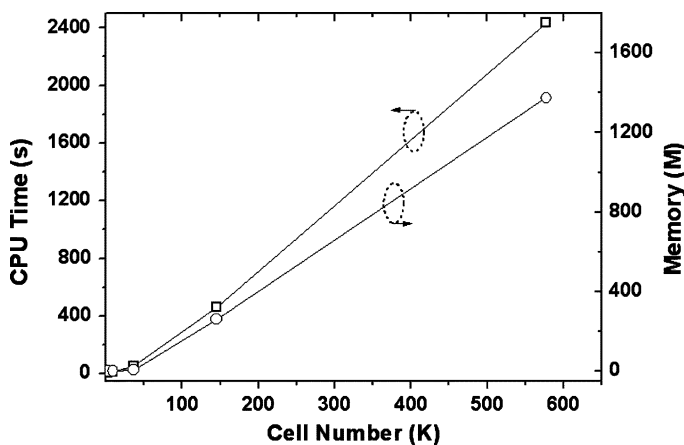


Fig. 29. CPU runtime and memory usage.

V. CONCLUSION

In this paper, the finite volume modelling of voltage distribution equation and heat equations with fluidic cooling and air convection are presented. Electrical-thermal co-simulations of PDN with Joule heating, air convection and micro-fluidic cooling have been carried out. Good agreement between the simulated results, measurement and analytical results validate the correctness and accuracy of the electrical-thermal co-simulation method. Moreover, the simulation shows that micro-fluidic cooling method can remove heat more efficiently than traditional heat sink for high power density 3D sub-systems. Therefore, the thermal effect on the voltage drop in PDN is reduced using micro-fluidic cooling technology.

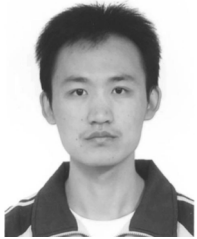
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