Signal Integrity

Jun Fan, Associate Editor

Welcome to the Signal Integrity Column! In this issue, you will find a very interesting paper on power integrity. In modern high-speed digital designs, power distribution networks (PDNs) using power and ground planes are commonly used where decoupling capacitors are necessary to provide charge for logic transitions and, at the same time, to mitigate the noise generated during device switching. With the continuous increase of data rates and current consumption, as well as the decrease of logic levels, PDN design becomes increasingly challenging. More and more decoupling capacitors would be needed, which presents a seemingly unresolvable conflict with the industry trends for lower cost and more compact design. Prof. Madhavan Swaminathan, a well-known pioneer and expert on power integrity, presents his latest research effort in this paper to address this challenge. I hope his innovative idea can inspire the readers of the EMC Magazine to come up with more ideas to address this fundamental power integrity issue necessary for next generations of high-speed digital designs.

If you would like to contribute to this column or have any feedback and comments, please feel free to contact me at jfan@mst.edu. Any topics related to signal and power integrity are welcome, as long as the papers are practically orientated. Submissions will be peer reviewed, and the published papers will be included in the IEEE *Xplore*.

Designing for Power Integrity: Status, Challenges and Opportunities

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Abstract: It has been almost two decades since the target impedance concept was first proposed for the design of power distribution networks. Both academia and industry have come a long way since then by proposing solutions for managing power integrity in packages and printed circuit boards (PCB). This paper briefly reviews the past and identifies challenges that need to be addressed in the future for tackling this problem. These challenges are often times opportunities for research that can lead to interesting and often times innovative solutions. Some ideas for managing power integrity in the future are discussed in this paper.

I. Introduction

The semiconductor industry has been very successful in scaling the transistor over the last five decades. Thanks to Moore's law, this scaling has enabled the integration of a billion transistors on a chip today. However, scaling requires that the voltage be reduced from one computer generation to the next and this essentially has led to the problems related to power distribution. With the current increasing due to the doubling of transistors every 18 months and due to voltage scaling, the demands placed on the power distribution has been steadily increasing. Designing for power integrity refers to managing the power supply noise across the voltage and ground terminals of the transistors such that they function at speed. The chip, package and PCB have their fair share of contribution towards the generation of power supply noise and hence their individual designs and interactions between them play a large role in determining power supply noise. This is depicted in Figure 1 where both the core and I/O circuits need to be powered through the power distribution network (PDN).

In Figure 1, the core circuits corresponds to transistors that communicate with each other within the integrated circuit (IC) while I/O circuits are the Input/Output terminals that are used to communicate between ICs through the package and PCB. As has been well documented by now by several researchers [1], the

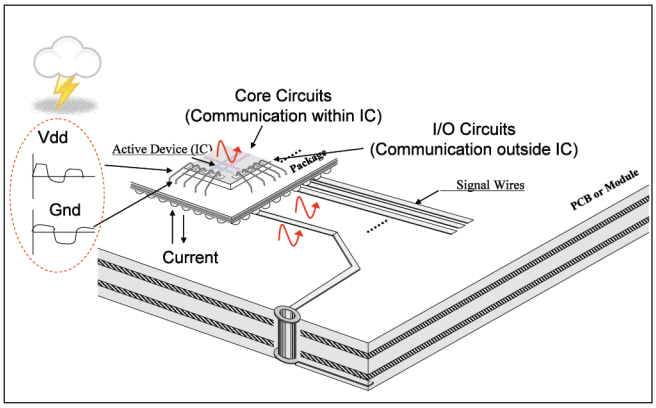

Figure 1: Power supply noise due to core and I/O switching

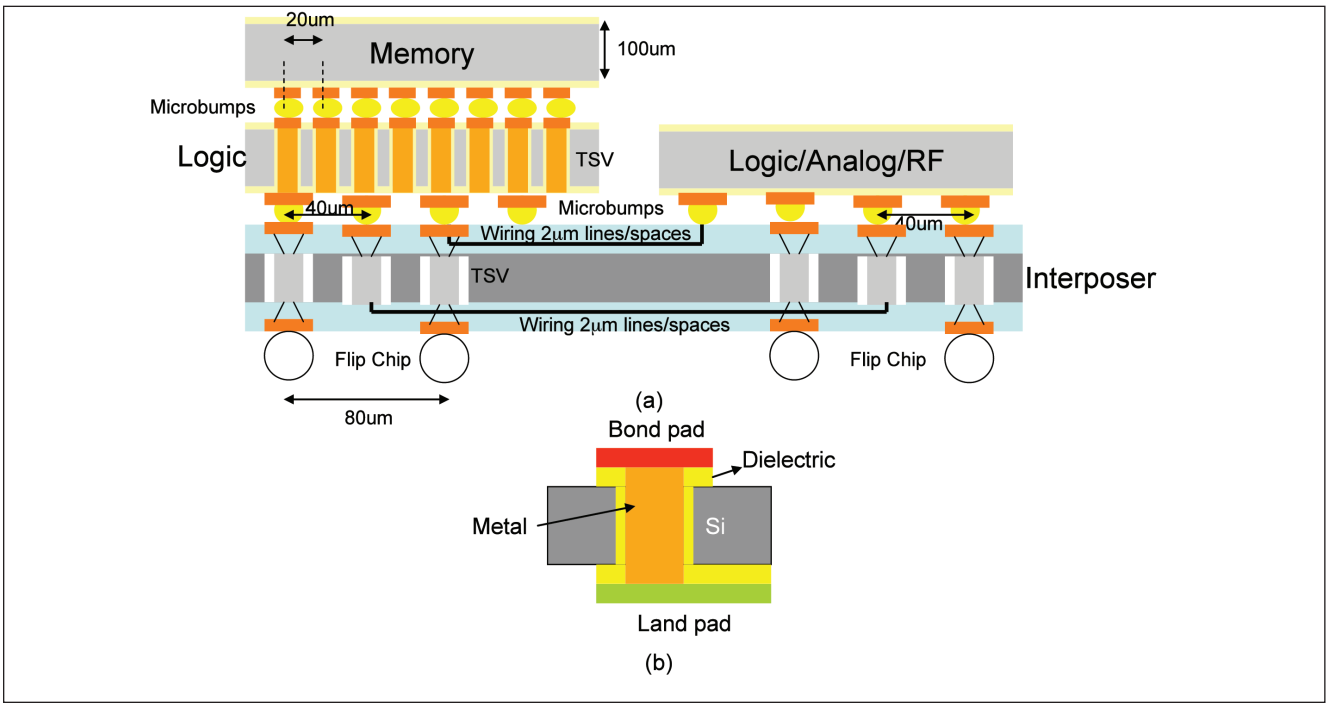

Figure 2: 3D integration (a) Stacked ICs on interposer and (b) Through silicon via structure

voltage fluctuations on the power supply rails of the transistor cause increased jitter and reduction in the voltage margin and therefore power supply fluctuations have a direct influence on the operating frequency.

Over the years, the communication speed between ICs off-chip has steadily been increasing with greater than 6Gbps speeds per I/O terminal being supported as in GDDR5 [2] along with an increase in the number of parallel bits being transmitted. With an objective of reaching >1TBps of communication bandwidth between ICs, the electronics industry is in the process of developing new technologies and signalling schemes to enable it. Examples are 2.5D and 3D integration where ICs are partitioned and communicate with each other through a silicon interposer or are stacked on each other using through silicon vias, as shown in Figure 2 [3].

In Figure 2, the communication between ICs determines the speed of the system and hence the interconnections and package play a very critical role in determining the performance of the system. The focus of this article is primarily on off-chip (or I/O) signalling.

II. The Status

Though power supply noise is a transient phenomenon that occurs due to the switching of transistors, the design of the PDN is best accomplished in the frequency domain. This concept, which originated in the mid 1990s, is the methodology being pursued by most designers today. This methodology involves the optimization of the PDN impedance such that it meets a target impedance value, where the target impedance is defined using Ohm's law. This is illustrated in Figure 3 where the target impedance Z_T allowed looking from the power supply terminals of the transistor or IC towards the Voltage Regulator Module (VRM) is given by:

$$Z_T = \frac{\Delta V}{I} \qquad (1)$$

where ΔV is the allowed ripple (specification of the transistor) and I is the current drawn. If the current drawn by the transistors is known and is assumed as a constant with frequency, then the target impedance is a constant with frequency as well, as shown in Figure 3. Since the PDN has resistance, inductance and capacitance in them, the resulting frequency response is oscillatory with resonances (nulls) and anti-resonances (peaks), as depicted in the figure. The objective of the design process is to ensure that the PDN response never exceeds the target impedance over the frequency bandwidth of interest (typically up to the fundamental of the clock frequency or higher) [4].

On a semi-log scale as shown in Figure 3, the positive slope in the PDN response is due to the inductance, shown as the culprit here (since it increases the impedance), and the negative slope is due to the capacitance, shown as the saviour (since it decreases the impedance). The effect of resistance is not shown in the figure even though it is very important in managing the frequency response. As noted in Figure 3, various parts of the system which include the voltage regulator module (VRM), capacitors (on the chip, package and PCB) and planes contribute towards the impedance depending on the frequency range. This concept can be applied to both core and I/O signalling with the fundamental difference between the two being the long transmission lines in the package and PCB used to communicate between ICs in the latter.

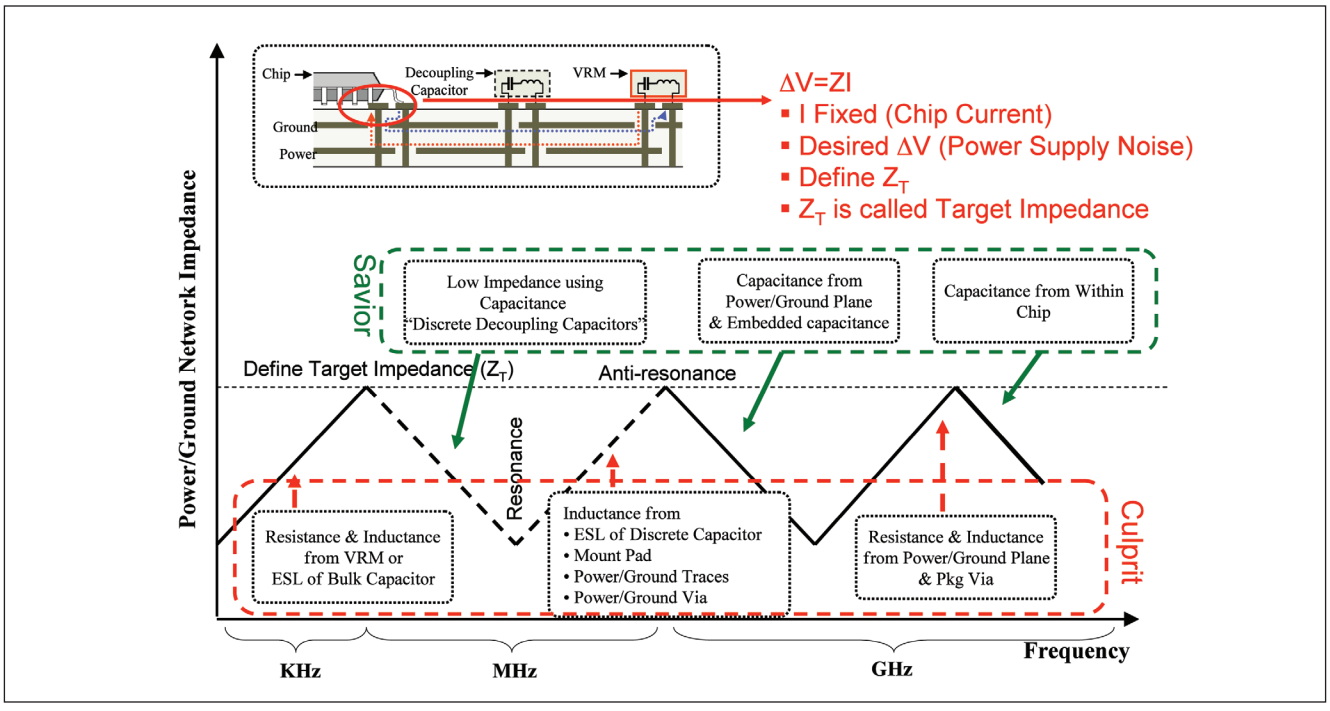

Figure 3: Target impedance and PDN response

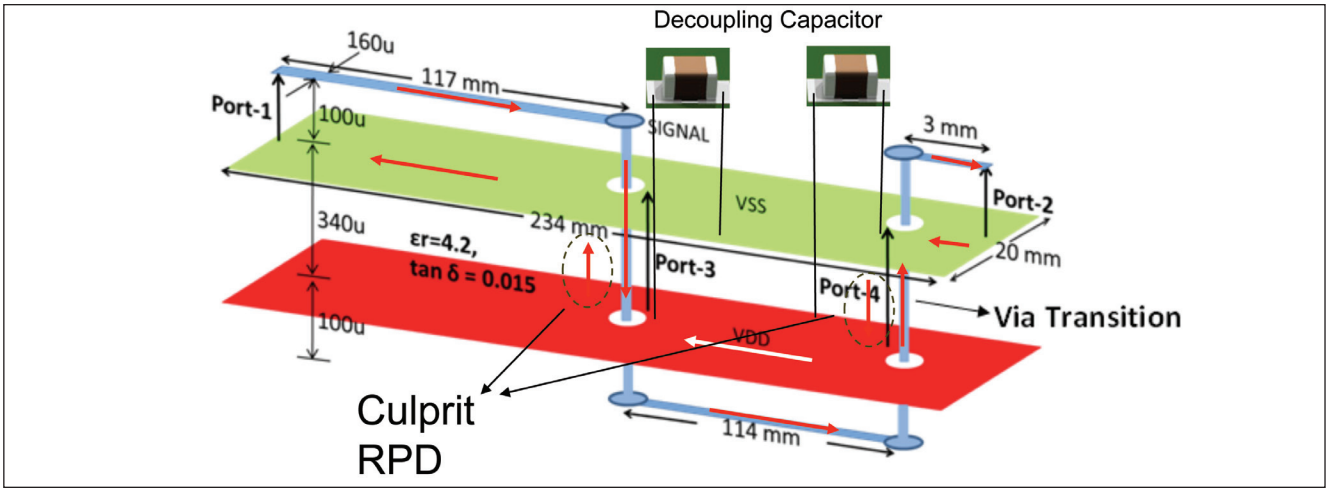

Figure 4: Transmission line signalling, return current, return path discontinuity (RPD) and role of capacitor

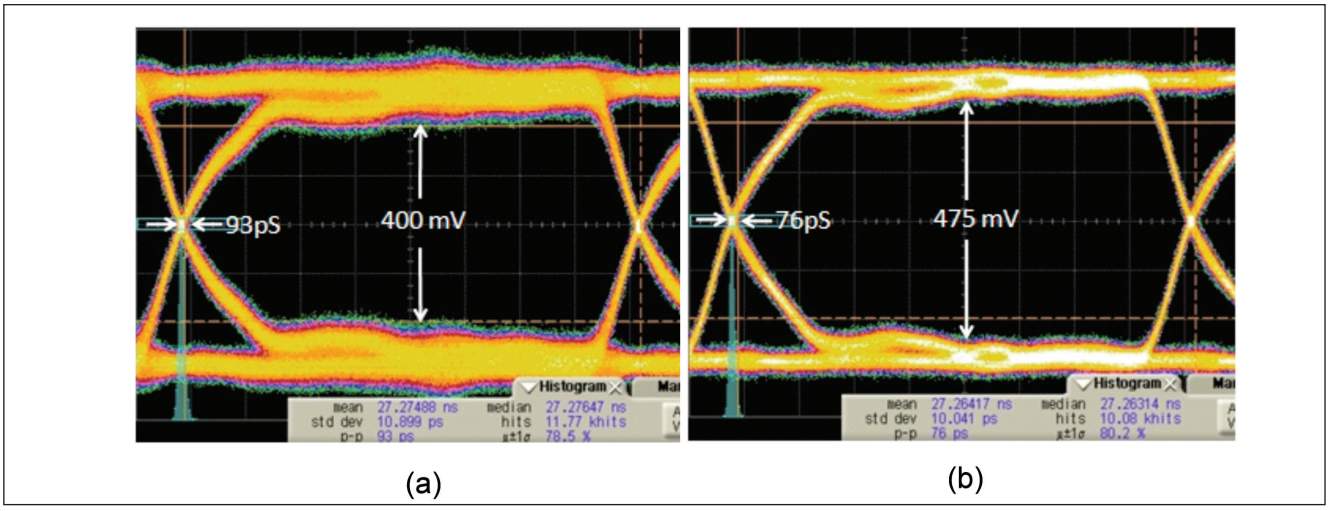

Figure 5: Eye diagrams (a) before capacitors: height=400mV and jitter=93ps and (b) after capacitors: height=475mV and jitter=76ps

The importance of transmission line signaling on signal and power integrity is best illustrated here using a simple four metal layer structure in Figure 4, where an interconnection transitions between the top and bottom layers creating two discontinuities along its path [5]. As is well known from electromagnetic theory, a transmission line supports a forward and return current, where the charging of the interconnection in Figure 4 causes a return current to flow on the plane closest to it.

Following the return currents on the planes, and since the planes support different DC potentials (VDD and VSS), they are not connected to each other. This causes return path discontinuities (RPD) at via locations, which act like displacement current sources, causing electromagnetic disturbance between the two planes. Since the edges of the planes are open circuited, over time standing wave resonances are generated between the planes. As has been shown in [5] and by others, the standing waves create an impedance response between the planes at ports 3 and 4 in Figure 4 similar to the response in Figure 3, causing a variation in the insertion loss of the signal lines between ports 1 and 2 in Figure 4. The channel response measured as an eye diagram at port 2 will be affected by the RPDs. Today, this effect is mitigated either by using capacitors (shown in Figure 4) or by stitching the planes together using vias (if the planes are at the same DC potential) at the discontinuities. This design approach provides the necessary continuity for the return currents, thereby improving the channel response.

The measured eye diagrams for the example in Figure 4 at port 2 using a 600Mbps Pseudo Random Bit Stream (PRBS) at port 1 are shown in Figure 5 where a ~20% improvement in eye height and jitter results from using decoupling capacitors.

The simple example used to illustrate the effect of RPDs on the channel response is one of the root causes for interaction between signal and power distribution in a system. The addition of capacitors to compensate for return path discontinuities in concept is similar to Figure 3 where the impedance of the power distribution is lowered through the addition of capacitors. In 2004, lowering the PDN impedance for improving signal and power integrity was identified as a major requirement in the future [6]. Since then new technologies have emerged from both industry and academia to address these, which include thin dielectrics and embedded decoupling capacitors to name a few in both the package and PCB, which are now commercially available [1].

Over the years, with the complexity of systems growing due to the increase in channel speed and bandwidth, the number of discontinuities in the system is growing rapidly. Managing these discontinuities using capacitors or other means is a major challenge we face today.

III. The Challenge

In a complex package or PCB, the discontinuities along the return path that affect signal integrity are many. An example is illustrated

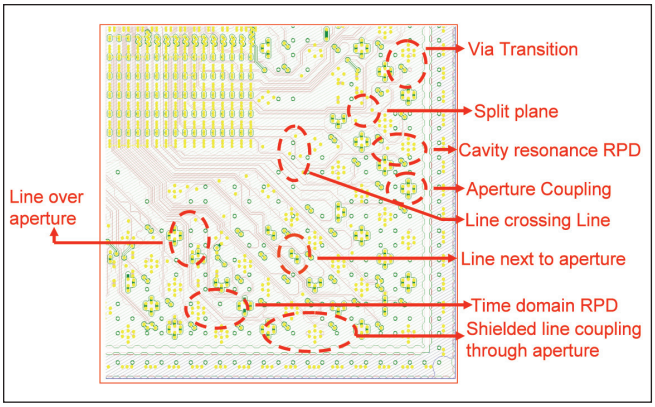

Figure 6: Typical Return Path Discontinuities in a package

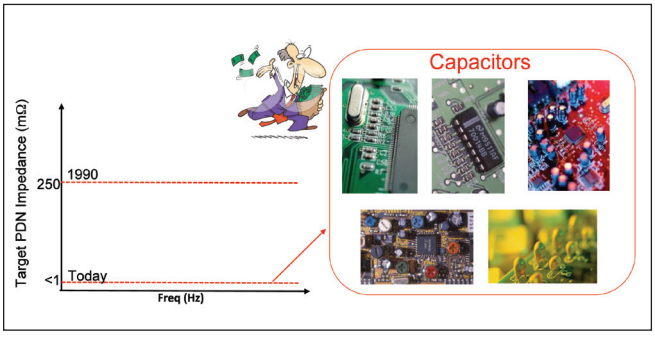

Figure 7: PDN impedance and role of capacitors over last two decades

in Figure 6 where a subset of the discontinuities experienced by the signal lines are shown for one layer of an eight layer package from IBM. Of course, not every discontinuity can be fixed using capacitors since other means need to be used as well such as changing stack-up, re-routing the lines around discontinuities and removing via transitions to name a few.

In most packages and PCB, the severity of the RPDs is a result of two primary effects namely, 1) referencing where a signal line is referenced to either the ground plane, voltage plane or both and 2) cavity resonances due to the standing waves generated between the voltage and ground planes. Over the last decade, several signal and power integrity tools have emerged that has helped immensely to tackle the RPD identification problem. To reduce PDN impedance we have essentially relied on the use of capacitors. Some of the complex systems today use advanced technologies mentioned earlier such as thin dielectrics and embedded high K dielectrics for reducing impedance. Hence, over the last two decades we have successfully reduced the PDN impedance by a large factor to the order of milli-ohms today, as shown in Figure 7.

Today, the capacitors we use in a system are enormous and are often times far greater than the ICs they service. With the electronics industry being very cost conscious, the luxury of relying on capacitors to continuously reduce the PDN impedance from one generation to the next is becoming increasingly difficult. Simply put, adding capacitors is akin to throwing away money as illustrated in Figure 7 and this represents the overwhelming challenge we face today. Ofcourse, not all capacitors relate to mitigating RPDs in the package and PCB since they also support the core circuits

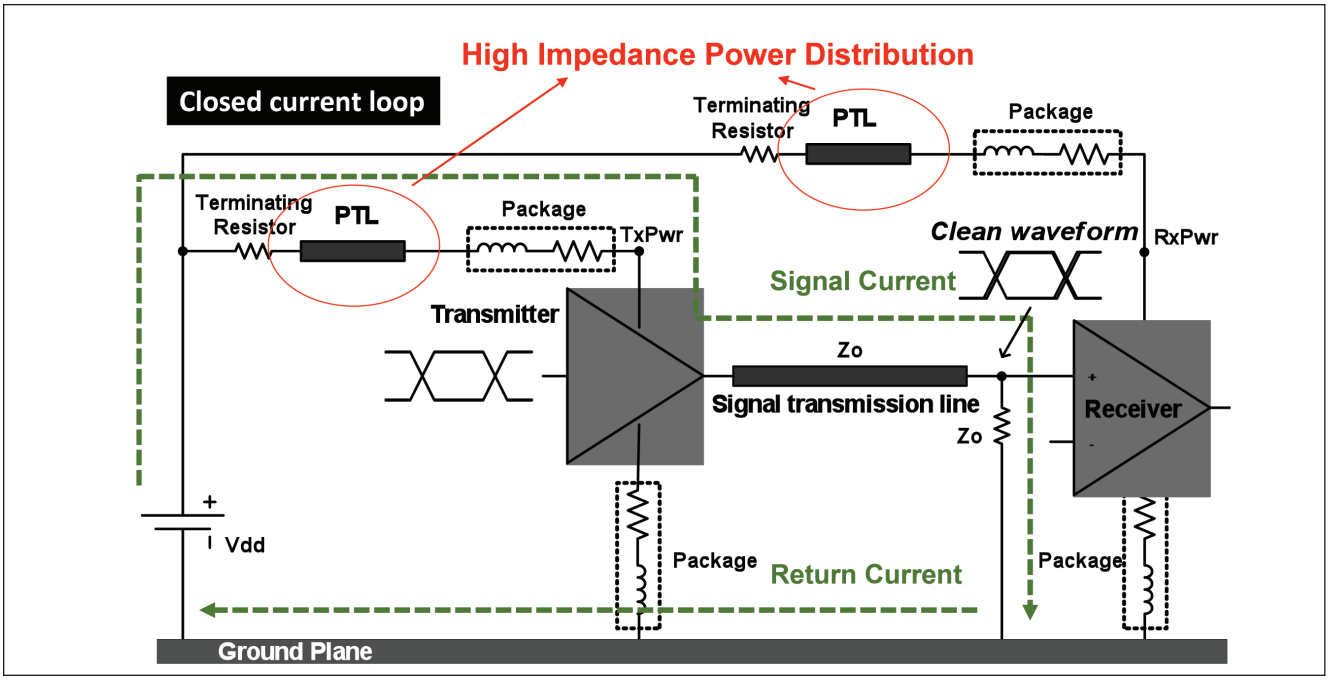

Figure 8: Power transmission line based PDN for chip to chip communication

and therefore the IC designers are equally to blame. But as the designers of the channel for inter-chip communication, can we address this problem through other means, rather than just relying on capacitors.

In [6], another issue that was highlighted was the need for minimizing noise coupling through the power distribution. This led to the development of electromagnetic bandgap (EBG) structures for isolation, where slots in the voltage and ground planes create bandgaps in the frequency response [1], [7]. Though this improves isolation significantly, it introduces more RPDs into the design and also increases power supply noise at the source (due to larger inductance), which can both be very problematic.

The problems identified could very well be opportunities for research. Some ideas are discussed in the next section which by no means are the only solutions, but hopefully acts as a catalyst to transform the way we address these challenges in future years.

IV. The Opportunity

There are two fundamental problems that require a solution today, namely, 1) minimizing return path discontinuities in a design and 2) suppressing power supply noise. These two issues are related to each other and our goal is therefore to find a solution by minimizing the capacitors required. To this end, a possible solution addressing the communication path between two ICs is shown in Figure 8.

In the figure, the voltage plane is removed and replaced with a power transmission line (PTL) [8], where the signal transmission line and PTL are referenced to a common ground plane. This removes the RPDs described in Figure 4 caused by a change in reference planes for the signal lines and eliminates cavity resonances between the voltage and ground planes. Since cavity resonances are the primary source of coupling through the PDN, EBG like structures are no longer required and filters can be designed in the PTL to mitigate coupling at the source. Also since noise coupling occurs locally as cross talk between the transmission lines, this can be mitigated through known methods. Decoupling capacitors are of two types namely, 1) source capacitors that provide charge to the switching circuits and 2) capacitors that are used to mitigate RPDs. The second class of capacitors can be eliminated using the signalling scheme in Figure 8, thereby reducing the total number of capacitors required. Moreover, since the impedance of the PTL is determined based on the on-resistance of the transistor, the impedance of the signal line (typically 50Ω), and the voltage swing required at the receiver, its value is of the order of ohms and not milli-ohms. The termination resistor at the source end in Figure 8 is used to absorb reflections in the network, which can be removed based on the signalling scheme used [10]. PTLs however fix only half the problem by eliminating RPDs since the schematic shown in Figure 8 can still generate power supply noise by causing voltage fluctuations between the TxPwr/RxPwr and ground nodes of both the transmitter and receiver ICs. This issue can be addressed by constructing a PDN that stays pre-charged to a constant voltage at all times. In Figure 8, if the PDN is pre-charged to a constant voltage, then the parasitics of the PDN shown as series resistor and inductor in the figure, will no longer cause fluctuations at the power supply terminals of the ICs. This is possible using a simple modification to the circuit schematic in Figure 8, as shown in Figure 9.

The dummy path transistor in Figure 9 is a PMOS transistor whose gate has an inverted input as compared to the data input (data_in). In the figure the PTL has an impedance of 25Ω to obtain a 1.25V voltage swing across the 50Ω resistor. The receiver IC is not shown in the figure. When the signal transmission line is being charged, the dummy path transistor is OFF and only turns ON during the discharging of the transmission line. If the on-resistance of

the dummy path transistor is adjusted to Rpmos+Z0, then during discharging, the current flowing from the power supply (Vdd) into ground through this transistor will equal the current during the charging of the signal line. Since the current is constant during both cycles, the power supply node TxPwr is always charged to a constant voltage and therefore there is no noise across the power supply terminals of the transistors (at least theoretically!). Details of this signalling scheme are available in [8]. Implementation of the CCPTL scheme on a PCB using off-the-shelf ICs has shown that the improvement in eye height and jitter (peak to peak) at 1.5Gbps can be as large as 15% and 36% respectively (Figure 10), as compared to the conventional schemes used today.

So, imagine a PDN that contains no voltage planes, contains minimum return path discontinuities, uses high impedance structures and requires fewer capacitors than before. The PTL, in some cases, can be routed on the same layer as the signal transmission line, reducing the layers required. Since the PDN is always charged to a constant voltage, the design is very tolerant to manufacturing variations where the mismatch effect between the PTL and signal lines is minimal. Designing such structures becomes much easier due to the absence of resonances and therefore the need for CAD tools that analyse entire packages or PCBs to compute the PDN impedance may no longer be required (not sure if this would be good for the EDA vendors!). In addition, a single PTL can be used to service several drivers, thereby reducing routing congestion, as described later in this section.

In the CCPTL scheme, since constant current is drawn from the power supply during both the charging and discharging of the signal transmission line, the power usage doubles as compared to the more conventional methods. With low power being a main driver for many electronics applications, and since the number of parallel I/Os between ICs are expected to increase, the power usage needs to be reduced. This is possible through coding schemes such as pseudo-balanced signalling [9], [10] and inversion coding [11]. The Pseudo–balanced PTL (PBPTL) which uses 4 to 6 bit coding thereby maintaining a constant current through the PDN, has been shown to reduce power consumption by 50% as compared to CCPTL [10]. Similarly inversion coding with Constant Voltage PTL (CVPTL) where a resistive network is used to vary the current through the PDN to maintain the power supply at the chip terminals at a constant voltage has been shown to reduce power as well [11]. These are some alternate techniques that provide the benefits described earlier, while simultaneously reducing power.

To demonstrate the practicality and scalability of this approach for industrial applications, the PBPTL scheme has been applied to power the output drivers from a Spartan-6 LX45 FG(G) 484 Xilinx Field Programmable Gate Array (FPGA) IC shown in Figure 11a successfully. This implementation supported 12 bit to 18 bit coding using a PTL of impedance 10Ω at 600MHz, where a single PTL was used to feed all the drivers, as shown in Figure 11b. The eye diagram at the far end of a signal line for a PRBS at 600MHz is shown in Figure 12, showing a peak to peak jitter of 100ps and eye height of 1.37V, for a 2.5V power supply, where the improvement in peak to peak jitter was 66% as compared to the more conventional methods [12].

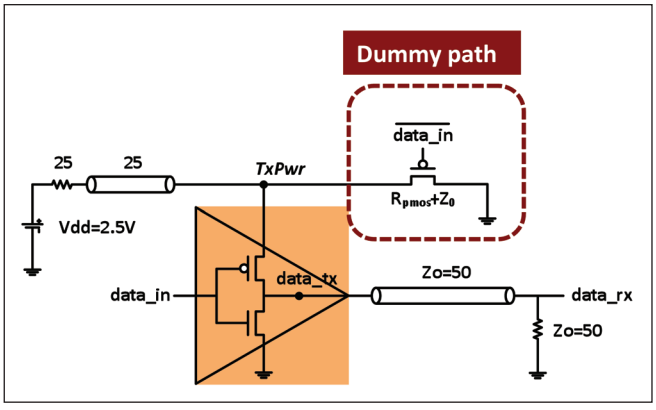

Figure 9: Signalling using Constant Current Power Transmission Line (CCPTL)

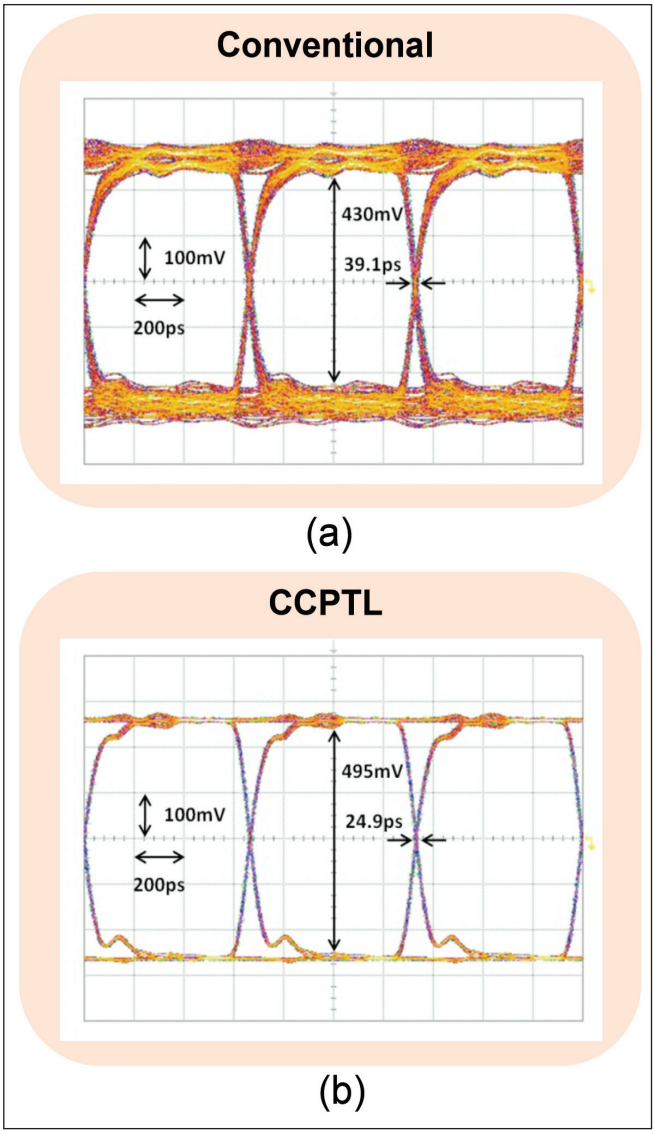

Figure 10: Eye diagrams at 1.5Gbps for (a) conventional and (b) CCPTL signalling for one channel

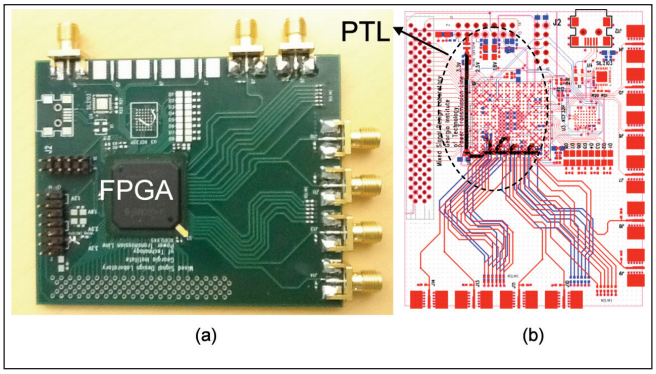

Figure 11: Xilinx FPGA with PBPTL implementation (a) Fabricated Board and (b) Layout showing PTL

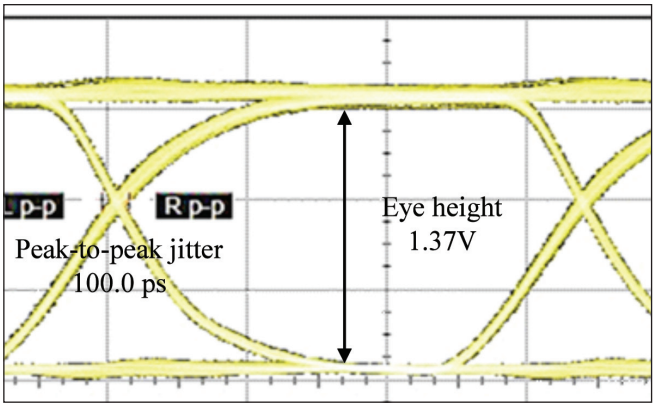

Figure 12: Measured eye diagram of Xilinx FPGA board

V. Conclusion

Packages and boards are becoming very complex. Managing signal integrity is becoming very challenging due to the interaction between the signal and power distribution network, which occurs through return path discontinuities. Given the challenges we face in designing such packages and PCBs, it is time for our community to start thinking outside the box for managing power integrity in the future, rather than just extending already known methods. Stuffing the package and PCB with more and more capacitors to reduce PDN noise is definitely not the answer. This is a great opportunity for all of us to think of new approaches to address the challenges we face. We need the Eureka moment and it is certainly time for our community to innovate!

VI. Acknowledgement

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VII. References

[1] M. Swaminathan and E. Engin, "Power Integrity Modeling and Design for Semiconductors and Systems", Prentice Hall, Nov 2007.
[2] S. Bae, et al, "A 60nm 6 GB/s/pin GDDR5 Graphics DRAM with Multifaceted Clocking and ISI/SSN Reduction Techniques", IEEE International Solid State Circuits Conference, pp 278-279, 2008.
[3] M. Swaminathan and K. J. Han, "Design and Modeling for 3D ICs and Interposers", World Scientific Publishers, Sep. 2013.
[4] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology", IEEEE. Trans. on Advanced Packaging, vol. 22, no. 3, pp. 284 – 291, Aug. 1999.
[5] Madhavan Swaminathan, Daehyun Chung, Stefano Grivet-Talocia, Krishna Bharath, Vishal Laddha, and Jianyong Xie, "Designing and Modeling for Power Integrity", Invited Paper, IEEE Transactions on Electromagnetic Compatibility, pp. 288 – 310, Vol. 52, No. 2, May 2010.
[6] M. Swaminathan, J. Kim, I. Novak and J. Libous, "Power Distribution Networks for System-on-Package", IEEE Trans. on Advanced Packaging, Vol. 27, No. 2, pp. 286-300, May, 2004.
[7] M. H. Nisanci, F. de Paulis, D. di Febo and A. Orlandi, "Practical EBG Application to Multilayer PCB: Impact on Signal Integrity", IEEE EMC magazine, Vol. 2, No. 2, pp. 82-87, 2013.
[8] S. Huh, M. Swaminathan and D. Keezer, "Constant current power transmission line based power delivery network for single-ended signaling," IEEE Trans. on Electromagnetic Compatibility, Vol. 53, Issue: 4, pp: 1050 – 1064, 2011.
[9] D. Oh, F. ware, W. p. Kim, J. H. Kim, J. Wilson, L. Luo, J. Kizer, R. Schmitt, C. Yuan and J. Eble, "Pseudo-differential signaling scheme based on 4b/6b multiwire code", Proceedings of Electrical Performance of Electronic Packaging, pp. 29 – 32, Oct. 2008.
[10] S. Huh, M. Swaminathan and D. Keezer, "Pseudo-balanced Signaling using Power Transmission Lines for Parallel I/O Links", IEEE Transactions on Electromagnetic Compatibility, Vol. 55, Issue: 2, pp: 315-327, 2013.
[11] S. Telikapalli, M. Swaminathan and D. Keezer, "Minimizing simultaneous switching noise at reduced power with constant voltage power transmission lines for High Speed Signaling", International Symposium on Quality Electronic Design (ISQED), pp. 714-718, 2013..
[12] S. K. Kim and M. Swaminathan, "Implementation of Power Transmission Lines for Field Programmable Gate Arrays for Managing Signal and Power Integrity", International Symposium on Electromagnetic Compatibility, 2013.

Biography

Madhavan Swaminathan *is the John Pippin Chair in Electromagnetics in the School of Electrical and Computer Engineering (ECE) and Director of the Interconnect and Packaging Center, Georgia Tech; and the Founder and CTO of E-System Design, a company focusing on the development of CAD tools for achieving signal and power integrity in integrated 3D micro and nano-systems. He is also the co-founder of Jacket Micro Devices (JMD), a company that specialized in integrated RF modules and substrates for wireless applications, that was acquired by AVX Corporation. He formerly held the position of Joseph M. Pettit Professor in Electronics in ECE and Deputy Director of the NSF Microsystems Packaging Center at Georgia Tech. Prior to joining Georgia Tech, he was with IBM working on packaging for supercomputers. He is the author of more than 400 technical articles, holds 27 patents, author of 3 book chapters, primary author and co-editor of 3 books, all in the field of packaging. He is an IEEE Fellow and is a Distinguished Lecturer for the IEEE EMC Society for the 2012-2013 term. Thirty-five PhD and sixteen MS students in Electrical Engineering have graduated under his supervision. He received his M.S and PhD degrees in Electrical Engineering from Syracuse University in 1989 and 1991, respectively. He is available to give a talk on this topic at any of the IEEE EMC chapters.*

EMC Design Tips

Bruce Archambeault, Associate Editor

Welcome to Design Tips! Decoupling capacitor design for printed circuit boards is one topic with the most myths and misunderstandings within the EMC and SI/PI community. The most common practice is to cluster the capacitors close together (usually to save space), however, this gives the worst possible decoupling performance from all the possible options! This article illustrates the effect on inductance from different placements of the decoupling capacitors. The results might surprise you!

Please send me your most useful design tip for consideration in this column. Ideas should not be limited by anything other than your imagination! Please send these submissions to bruce.arch@ieee.org. I'll look forward to receiving many "Design Tips!" Please also let me know if you have any comments or suggestions for this column, or comments on the Design Tips articles.

Positioning Multiple Decoupling Capacitors in Printed Circuit Boards

Bruce Archambeault, Jingook Kim, Ketan Shringapure

In the Spring 2009 EMC Society Newsletter issue the Design Tips showed the typical inductance associated with connecting decoupling capacitors to power/ground-reference planes using standard size surface mount capacitors. Inductance values of 2-3 nH were very typical, even for 0402 size packages, depending on how deep into the PCB the planes were. In the Spring 2010 EMC Society Newsletter issue the Design Tips showed the typical inductance associated with connecting two decoupling capacitors to power/ground-reference planes and the effect of positioning them close together or far apart, while maintaining equal distance to an IC power pin.

In this Design Tips article, we expand to use 16 capacitors positioned around a typical sized ASIC/IC. The equivalent inductance seen by the ASIC/IC is found using the cavity resonance full wave approach. Cases for all the capacitors placed close together, or spread out as much as possible around the ASIC/IC are considered, as well as when the capacitor terminals (power and ground) are alternated. The equivalent inductance is found as a function of how deep into the PCB stackup the power/ground plane pair is located.

Figure 1 shows the four configurations of capacitor placement. The configurations include:

1) Dense, Non-alternating
2) Dense, Alternating
3) Spread out, Non-alternating
4) Spread out, Alternating

The 'dense, non-alternating' configuration is probably the most common configuration used in most PCBs.

Figure 2 shows the equivalent inductance when the capacitor vias are positioned only 40 mils apart. This is much smaller spacing than is typically used for 0402 or 0603 sized surface mount capacitors. The equivalent inductance for large capacitor spacing must be increased due to the large loop area, but the trends will remain the same.

It is no surprise that as the power/ground plane pair are located deeper into the PCB stack up, the equivalent inductance is increased. However, it can be clearly seen that the 'dense, non-alternating' configuration is the worst case (highest equivalent inductance) compared to the other configurations. It can also be seen that when the capacitors are spread out as much as possible, the equivalent inductance does not vary significantly when the capacitors are alternated or not.

Probably the most interesting result is that when the capacitors are positioned in the 'dense, alternating' configuration, the equivalent induc-

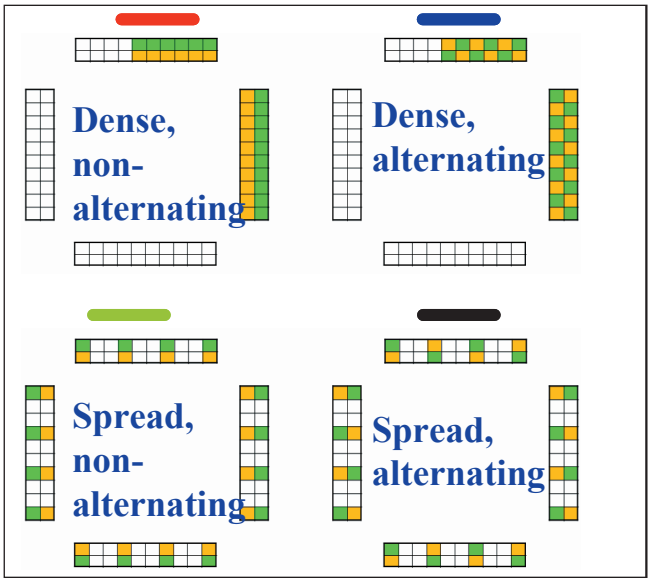

Figure 1. Capacitor Position Configurations

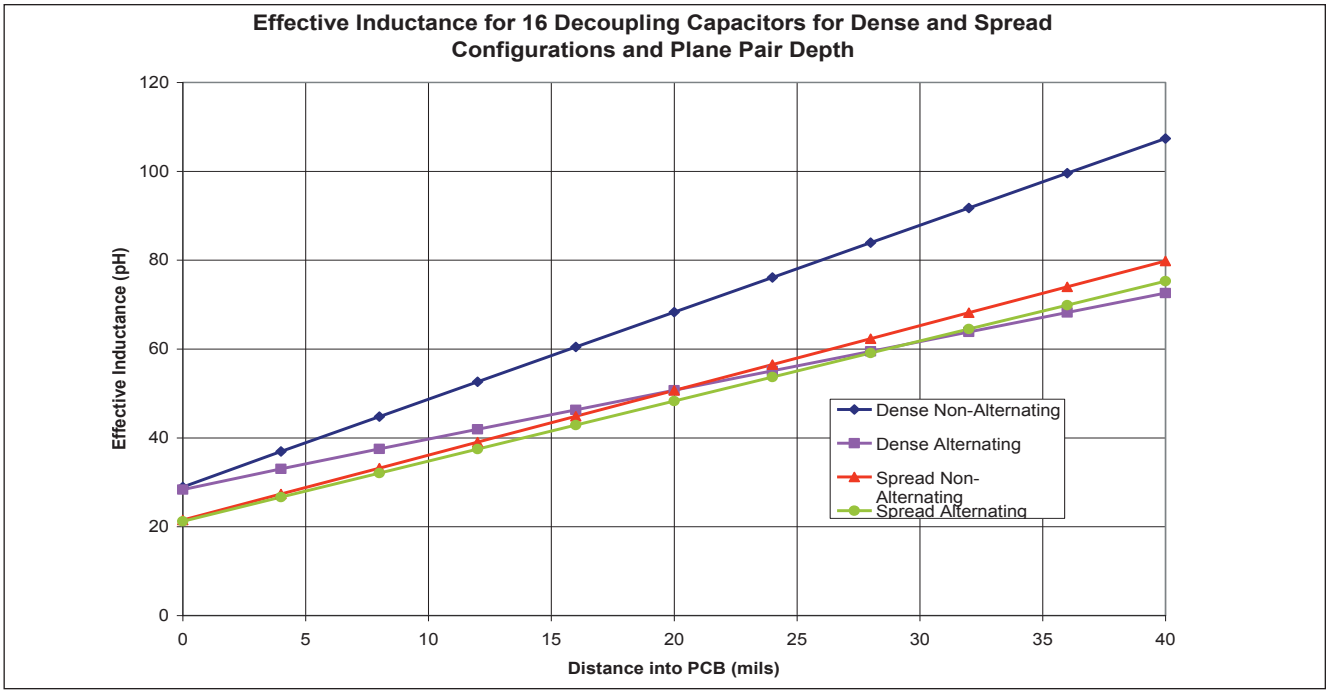

Figure 2. Effective Inductance for Various Capacitor Configurations with 40 mil spacing between Capacitor Vias

tance is approximately the same as when the capacitors are spread out after going a few mils into the PCB stack up. This is because the mutual inductance between the pairs of vias is cancelled with the alternating power/ground pins, reducing the effective inductance.

Conclusion

The most commonly used decoupling capacitor configuration is the worst possible configuration from an equivalent inductance point of view. When possible, the capacitors should be spread out (while maintaining a close distance to the ASIC/IC). If space issues force the capacitors to be positioned close together, then it is important to alternate the power/ground pins to reduce the equivalent inductance. Using these approaches, it may be possible to reduce the total number of capacitors required for decoupling the power/ground plane pair.

Biographies

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